INA228-Q1 85-V, 20-Bit, Ultra-Precise Power/Energy/Charge Monitor With I²C Interface

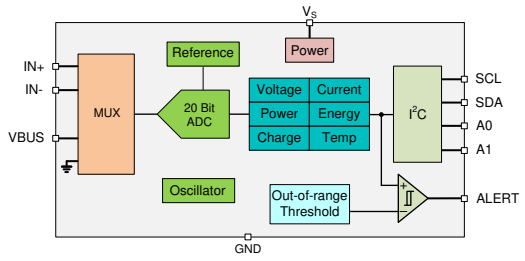
1 Features

- High-resolution, 20-bit delta-sigma ADC
- Wide common-mode range: –0.3 V to +85 V
- Shunt full-scale differential range: ±163.84 mV / ± 40.96 mV
- Bus voltage sense input: 0 V to 85 V
- Accuracy
  - Offset voltage at 48 V_{CM}: ±2 µV (maximum)
  - Offset voltage at 0 V_{CM}: ±2 µV (maximum)
  - Offset drift: ±0.01 µV/°C (maximum)
  - Gain error: ±0.1% (maximum)
  - Gain error drift: ±20 ppm/ °C (maximum)
  - Shunt voltage resolution: 312.5 nV/LSB / 78.125 nV/LSB
  - Bus voltage resolution: 195.31 µV/LSB
- Input bias current: 5 nA (maximum)
- Internal temperature sensor: ±2 °C (maximum)
- Internal precision oscillator: ±1% (maximum)
- Programmable data rate and averaging
- Reports current, bus voltage, power, internal temperature, energy and charge
- High-side and low-side applications
- 3-MHz High-Speed I²C interface with 16 pin-selectable addresses
- Operates from a 2.7-V to 5.5-V supply
  - Operational current: 660 µA
  - Shutdown current: 5 µA

2 Applications

- 48-V automotive battery management systems
- EV / HEV mA - KA sense applications
- DC-DC converters and power inverters
- 48-V Industrial battery packs
- 48-V Power-over-Ethernet (PoE)
- 54-V telecom equipment
- 48-V enterprise servers

Simplified Block Diagram



3 Description

The INA228-Q1 is an ultra-precise digital power monitor with 20-bit delta-sigma ADC specifically designed for current-sensing applications. The device can measure a full-scale differential input of ±163.84 mV or ±40.96 mV across a resistive shunt sense element with common-mode voltage support from –0.3 V to +85 V.

The low offset and gain drift design of the INA228-Q1 allows it to be used in precise systems that do not undergo multi-temperature calibration during manufacturing. Further, the very low offset voltage and noise allow for use in mA to kA sensing applications and provide a wide dynamic range without significant power dissipation losses on the sensing shunt element. The low input bias current of the device permits the use of larger current-sense resistors, thus providing accurate current measurements in the microamp range.

The device allows for selectable ADC conversion times from 50 µs to 4.12 ms as well as sample averaging from 1x to 1024x which further helps reduce the noise of the measured data.

The INA228-Q1 calculates power, energy and charge accumulation by employing the precision ±1% integrated oscillator, all while performing calculations on a sample-by-sample basis for an accurate result. An integrated temperature sensor with error less than ±2 °C provides information about the ambient temperature of the system.

The INA228-Q1 integrates built-in diagnostics to indicate system health status as well as out-of-range conditions. This indication is provided by using the open-drain ALERT pin.

The INA228-Q1 operates from a single supply of 2.7-V to 5.5-V supply, drawing less than 660-µA current during operation and with less than 5-µA current during shutdown. Configurable continuous or single-shot triggered measurement provides further current consumption reduction. The output can be interfaced to an MCU or a battery management System-on-Chip devices through the I²C interface.

The device is specified over the operating range –40 °C to +125 °C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
INA228-Q1	VSSOP (10)	3.00 mm × 3.00 mm

(1) For all available packages, see the package option addendum at the end of the data sheet.

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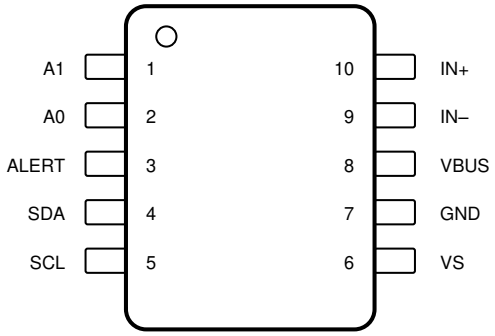
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
June 2020	*	

5 Pin Configuration and Functions

DGS Package
10-Pin VSSOP
Top View



Not to scale

Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	A1	Digital input	I^2C address pin. Connect to GND, SCL, SDA, or VS.
2	A0	Digital input	I^2C address pin. Connect to GND, SCL, SDA, or VS.
3	ALERT	Digital output	Open-drain alert output (Active Low).
4	SDA	Digital input/output	Open-drain bidirectional I^2C data.
5	SCL	Digital input	I^2C clock input
6	VS	Power supply	Power supply, 2.7 V to 5.5 V.
7	GND	Ground	Ground.
8	VBUS	Analog input	Bus voltage input.
9	IN–	Analog input	Connect to load side of shunt resistor.
10	IN+	Analog input	Connect to supply side of shunt resistor.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_S	Supply voltage		6	V
V_{IN+}, V_{IN-} (2)	Differential (V_{IN+}) - (V_{IN-})	-20	20	V
	Common - mode	-0.3	85	V
V_{VBUS}		-0.3	85	V
IO pins		GND – 0.3	Vs + 0.3	V
I_{IN}	Input current into any pin		5	mA
I_{OUT}	Digital output current		10	mA
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) VIN+ and VIN– are the voltages at the IN+ and IN– pins, respectively.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002, all pins(1) HBM ESD Classification Level 2	±2000	V
		Charged device model (CDM), per AEC Q100-011, all pins CDM ESD Classification Level C6	±1000	

(1) AEC Q100-002 indicated that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CM}	Common-mode input range	-0.3	48	85	V
V_S	Operating supply range	2.7	3.3	5.5	V
T_A	Ambient temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC		INA228-Q1 DGS 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	177.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	66.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	99.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	9.7	°C/W
Y_{JB}	Junction-to-board characterization parameter	97.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

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6.5 Electrical Characteristics

at T_A = 25 °C, V_S = 3.3V, V_{SENSE} = V_{IN+} - V_{IN-} = 0V, V_{CM} = V_{IN-} = 48 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT						
V_{CM}	Common-mode input range	V_{SENSE} = 0V; T_A = –40°C to +125°C	–0.3		85	V
V_{VBUS}	Bus voltage input range		0		85	V
CMRR	Common-mode rejection	–0.3V < V_{CM} < 85V, T_A = –40°C to +125°C, ADCRANGE = 1	146	160		dB
V_{DIFF}	Shunt Voltage Input Range	T_A = –40°C to +125°C, ADCRANGE = 0	–163.84		163.84	mV
		T_A = –40°C to +125°C, ADCRANGE = 1	–40.96		40.96	mV
V_{os}	Shunt Offset Voltage	V_{CM} = 48V, T_{CT} > 280µs			±2	µV
		V_{CM} = 0V, T_{CT} > 280µs			±2	µV
dV_{os}/dT	Shunt Offset voltage drift	T_A = –40°C to +125°C			±0.01	µV/°C
V_{os_bus}	V_{BUS} Offset voltage				±5	mV
dV_{os}/dT	V_{BUS} Offset voltage drift	T_A = –40°C to +125°C			±100	µV/°C
PSRR	Power supply rejection ratio	Vs = 2.7 V to 5.5 V, T_A = –40°C to +125°C		0.2	±1	µV/V
I_B	Input bias current	IN+, IN-		0.1	5	nA
Z_{VBUS}	Bus voltage input impedance (VBUS pin)	Active mode		1		MΩ
		Shutdown mode		1.3		GΩ
Z_{SHUNT}	Input differential impedance	IN+, IN-		95		kΩ
DC ACCURACY						
G_{SERR}	Shunt voltage gain error	V_{CM} = 24V			±0.1	%
G_{SERR_DRFT}	Shunt voltage gain error drift				±20	ppm/°C
G_{BERR}	V_{BUS} voltage gain error				±0.1	%
G_{BERR_DRFT}	V_{BUS} voltage gain error drift				±20	ppm/°C
	ADC Resolution			20		Bits
	1 LSB step size	Shunt voltage, ADCRANGE = 0		312.5		nV
		Shunt voltage, ADCRANGE = 1		78.125		nV
		Bus voltage		195.3125		µV
	ADC Conversion-time(1)			50		µs
				84		
				150		
				280		
				540		
				1052		
				2074		
				4120		
CLOCK SOURCE						
F_{OSC}	Internal oscillator frequency		0.99	1	1.01	MHz
F_{OSC_ACC}	Internal oscillator frequency accuracy	T_A = –40°C to +125°C			±1%	
TEMPERATURE SENSOR						
	Temperature sensor measurement range		–40		+125	°C
	Temperature accuracy			±0.1	±2	°C

(1) Subject to oscillator accuracy and drift

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Electrical Characteristics (continued)

at T_A = 25 °C, V_S = 3.3V, V_{SENSE} = V_{IN+} - V_{IN-} = 0V, V_{CM} = V_{IN-} = 48 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
Vs	Supply Voltage		2.7		5.5	V
I_Q	Quiescent current	V_{SENSE} = 0V		640	800	µA
		Shuntdown Mode			5	µA
		I_Q vs temperature, T_A = –40°C to +125°C			1.2	mA
T_{POR}	Device Start-Up time	Power-Up (NPOR)		170		µs
		From shutdown mode		80		
DIGITAL INPUT / OUTPUT						
V_{IH}	Logic input level, high		1.2		VDD	V
V_{IL}	Logic input level, low		GND		0.4	V
V_{OL}	Logic output level, low	I_{OL} = 1 mA	GND		0.4	V
V_{OH}	Logic output level, high	I_{OL} = 1 mA	VDD - 0.4		VDD	V
I_{IO_LEAK}	Digital leakage input current	0 ≤ V_{IN} ≤ V_S	–1		1	µA

6.6 Timing Requirements (I2C)

		MIN	NOM	MAX	UNIT
I2C BUS (FAST MODE)					
F(SCL)	I2C clock frequency	1		400	kHz
t(BUF)	Bus free time between STOP and START conditions	600			ns
t(HDSTA)	Hold time after a repeated START condition. After this period, the first clock is generated.	100			ns
t(SUSTA)	Repeated START condition setup time	100			ns
t(SUSTO)	STOP condition setup time	100			ns
t(HDDAT)	Data hold time	10		900	ns
t(SUDAT)	Data setup time	100			ns
t(LOW)	SCL clock low period	1300			ns
t(HIGH)	SCL clock high period	600			ns
tF	Data fall time			300	ns
tF	Clock fall time			300	ns
tR	Clock rise time			300	ns
I2C BUS (HIGH-SPEED MODE)					
F(SCL)	I2C clock frequency	10		2940	kHz
t(BUF)	Bus free time between STOP and START conditions	160			ns
t(HDSTA)	Hold time after a repeated START condition. After this period, the first clock is generated.	100			ns
t(SUSTA)	Repeated START condition setup time	100			ns
t(SUSTO)	STOP condition setup time	100			ns
t(HDDAT)	Data hold time	10		100	ns
t(SUDAT)	Data setup time	20			ns
t(LOW)	SCL clock low period	200			ns
t(HIGH)	SCL clock high period	60			ns
tF	Data fall time			80	ns
tF	Clock fall time			40	ns
tR	Clock rise time			40	ns

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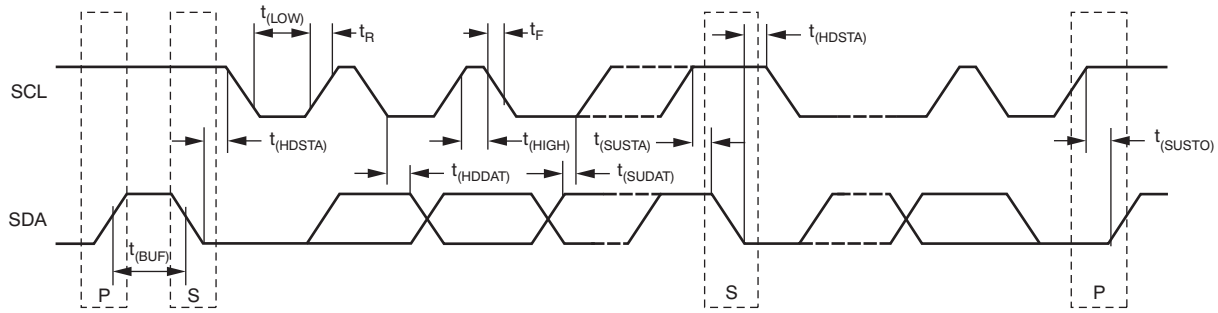

Figure 1. I^2C Bus Timing Diagram

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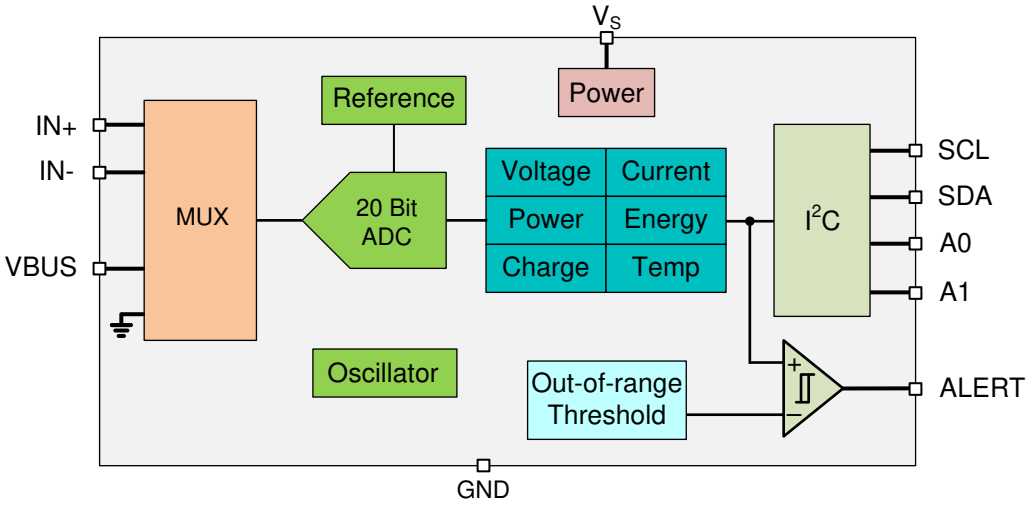
7 Detailed Description

7.1 Overview

The INA228-Q1 device is a digital current sense amplifier with an I^2C digital interface. It measures shunt current, bus voltage and internal temperature while calculating power, energy and charge measurements necessary for accurate decision making in precisely controlled systems. Programmable registers allow flexible configuration for measurement precision as well as continuous or triggered operation. Detailed register information is found in the *Register Maps* section.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 High Voltage Input

The INA228-Q1 device performs three measurements on the power-supply bus of interest. The current that flows through a shunt resistor creates a shunt voltage that is measured at the IN+ and IN– pins. The device also measures the bus supply voltage through the V_{BUS} pin and temperature through the integrated temperature sensor. The differential shunt voltage is measured between the IN+ and IN– pins, while the bus voltage is measured with respect to device ground. The device is powered by a separate supply V_S that can range from 2.7 V to 5.5 V. The bus voltage that is being monitored can range from 0 V to 85 V.

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Feature Description (continued)

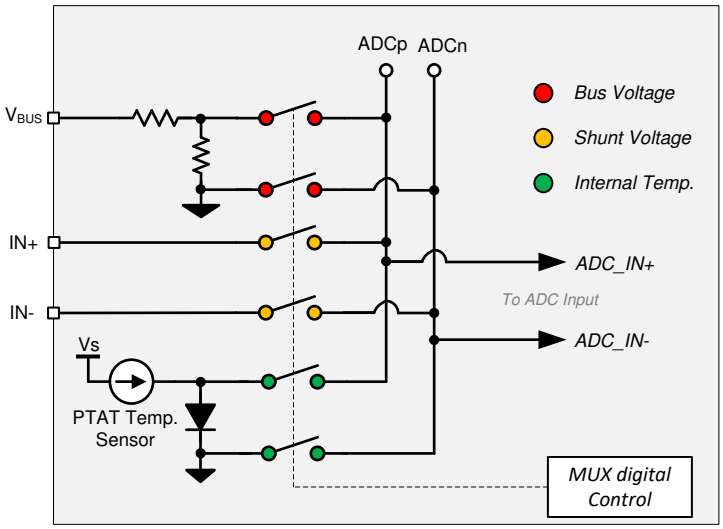

Figure 2. High-Voltage Input Multiplexer

The INA228-Q1 operates with a common-mode range of –0.3 V to +85 V at the input of the IN+, IN–, and V_{BUS} pins. These are designed such that the input common-mode voltage can be higher than the device supply voltage, V_S, while providing protection from hazardous high voltage sources to the other parts of the device.

The INA228-Q1 offers very low input bias current. The low input bias current of the INA228-Q1 has benefits like the reduction of the current consumed by the device in both active and shutdown state. Another benefit of low bias current is the ability to use input filters to reject high-frequency noise before the signal is converted to digital data. In a traditional current-sense amplifier, the addition of input filters comes at the cost of reduced accuracy. However, as a result of the low bias currents, input filters have little effect on the measurement accuracy of the INA228-Q1. Additionally another benefit of low bias current is the ability to use a larger current-sense resistor. This ability allows the device to accurately monitor currents in the micro-ampere range.

7.3.2 Input Range

The INA228-Q1 device supports two input ranges for the shunt voltage measurement. The supported full scale differential input across the IN+ and IN– pins can range up to ±163.84 mV or ±40.96 mV depending on the ADCRANGE bit in CONFIG_1 register. The bus voltage input range can be as high as 85 V, while the internal die temperature sensor range extends from –256 °C to +256 °C however the range of temperature for the device is package limited to –40 °C to 125 °C.

Table 1 provides a description of full scale voltage on shunt, bus, and temperature measurements, along with their associated step size.

Table 1. ADC Full Scale Voltage

PARAMETER	FULL SCALE VOLTAGE	RESOLUTION
Shunt voltage	±163.84 mV (ADCRANGE = 0)	312.5 nV/LSB
	±40.96 mV (ADCRANGE = 1)	78.125 nV/LSB
Bus voltage	0 V to 85 V	195.3125 µV/LSB
Temperature	–40°C to +125°C	7.8125 m°C/LSB

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The device shunt voltage measurements, bus voltage, and temperature measurements can be read through the VSHUNT, VBUS, and DIETEMP registers, respectively. The digital output in VSHUNT and VBUS registers is 20-bits. The shunt voltage measurement can be positive or negative due to bidirectional currents in the system, therefore the data value in VSHUNT can be positive or negative. The VBUS data value is always positive. The output data can be directly converted into voltage by multiplying the digital value to its respective resolution size. The digital output in the DIETEMP register is 16-bit and can be directly converted in °C by multiplying by the above resolution size. This output value can also be positive or negative.

Further the device provides the flexibility to report calculated current in Amperes, power in Watts, charge in Coulombs and energy in Joules as described in *Current Calculation*.

7.3.3 High-Precision Delta-Sigma ADC

The integrated ADC is a high-performance, low-offset, low-drift, delta-sigma ADC designed to support bidirectional current flow at the shunt voltage measurement channel. The measured inputs are multiplexed through the high-voltage input multiplexer to the ADC inputs as shown in Figure 2. The ADC architecture enables lower drift measurement across temperature and consistent offset measurements across the common-mode voltage, temperature, and power supply variations. A low-offset ADC is preferred in current sensing applications to provide a near 0-V offset voltage that maximizes the useful dynamic range of the system.

ADC conversion time for each input can be set independently by the VSHCT, VBUSCT, and VTCT bits in register ADCCONFIG_2, respectively, in the range of 50 µs to 4.12 ms. Furthermore, a sample averaging function in the range of 1x to 1024x is implemented and can be selected by the AVG bits in ADCCONFIG_2 register. The sample conversion time and the averaging are a part of the integrated digital filter described in *Low Latency Digital Filter*.

The INA228-Q1 can measure the shunt voltage, bus voltage, and die temperature, or a combination of any based on the selected MODE bits setting in the ADCCONFIG_2 register. This permits selecting modes to convert only the shunt voltage or bus voltage to further allow the user to configure the monitoring function to fit the specific application requirements. When no averaging is selected, once an ADC conversion is completed, the converted values are independently updated in their corresponding registers where they can be read through the digital interface at the time of input conversion end. The conversion time of each input depends on the selected conversion-time setting (VSHCT, VBUSCT, and VTCT) for each input, respectively. As soon as an input is converted, the following input begins, and the individual input channel sample rate depends on the conversion time and number of inputs enabled for conversion. When averaging is used, the intermediate values are subsequently stored in an accumulator, and the conversion sequence repeats until the number of averages is reached. After all of the averaging has been completed, the final values are updated in the corresponding registers that can then be read. These values remain in the data output registers until they are replaced by the next fully completed conversion results. In this case, reading the data output registers does not affect a conversion in progress.

The ADC has two conversion modes—continuous and triggered—set by the MODE bits in ADCCONFIG_2 register. In continuous-conversion mode, the ADC will continuously convert the input measurements and update the output registers as described above in an indefinite loop. In triggered-conversion mode, the ADC will convert the input measurements as described above, after which the ADC will halt until another single-shot trigger is generated by writing to the MODE bits. If the mode does not change and the device is kept in any of the triggered convert modes, writing the MODE bits will trigger a single-shot conversion. Although the device can be read at any time, and the data from the last conversion remain available, the Conversion Ready flag (CNVRF bit in DIAG_ALRT register) is provided to help coordinate triggered conversions. This bit is set after all conversion and averaging is completed.

The Conversion Ready flag (CNVRF) clears under these conditions:

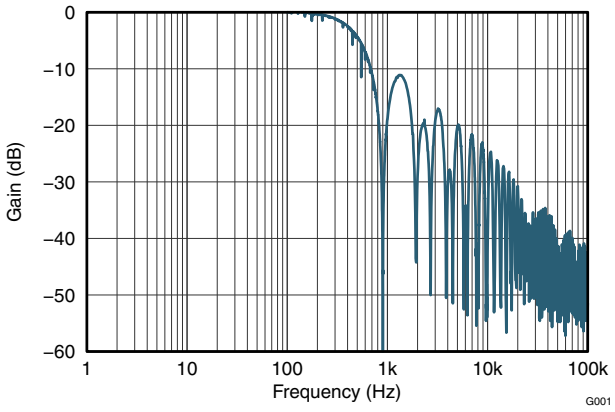
- Writing to the ADCCONFIG_2 register (except for selecting shutdown mode); or
- Reading the DIAG_ALRT Register

When the INA228-Q1 device is used in either one of the conversion modes, a dedicated digital engine is calculating the current, power, charge and energy values in the background as described in *Power, Energy, and Charge Accumulation*. In triggered mode, the accumulation registers (ENERGY and CHARGE) are invalid, as the device does not keep track of elapsed time. For applications that need critical measurements in regards to accumulation of time for energy and charge measurements, it is preferred that the device is configured in continuous conversion mode, as the accumulated results are continuously updated and can provide true system representation of charge and energy consumption in a system All of the calculations are performed in the background and do not contribute to conversion time.

For applications must synchronize with other components in the system, the INA228-Q1 conversion can be delayed by programming the CONVDLY bits in CONFIG_1 register in the range between 0 (no delay) and 510 ms. The resolution in programming the conversion delay is 2 ms. The conversion delay is set to 0 by default. Conversation delay can assist in measurement synchronization when external devices are used for voltage monitoring purposes, but an accurate power result is necessary for further energy calculations (like in battery state-of-health, for example). In such applications, the INA228-Q1 current measurement can be delayed or programmed such that the external voltage measurement and the INA228-Q1 current sensing can be synchronized so the measurements are recorded in the same timestamp. Keep in mind that even though the internal time base for the ADC is precise, synchronization will be lost over time due to internal and external time base mismatch.

7.3.3.1 Low Latency Digital Filter

The device integrates a low-pass digital filter that performs both decimation and filtering on the ADC output data, which helps with noise reduction. The digital filter is automatically adjusted for the different output data rates and always settles within one conversion cycle. The user has the flexibility to choose different output conversion time periods T_{CT} from 50 µs to 4.12 ms. With this configuration the first amplitude notch appears at the Nyquist frequency of the output signal which is determined by the selected conversion time period and defined as f_{NOTCH}= 1 / (2 x T_{CT}). This means that the filter cut-off frequency will scale proportionally with the data output rate as described. Figure 3 shows the filter response when the 540-µs conversion time period is selected.



ADC T_{CT} = 540 µs

Figure 3. Digital LPF Frequency Response

7.3.3.2 ADC Output Data Rate and Noise Performance

The INA228-Q1 noise performance and effective resolution depend on the ADC conversion time. The device also supports digital averaging which can further help decrease digital noise. The flexibility of the device to select ADC conversion time and data averaging offers increased signal-to-noise ratio and achieves the highest dynamic range with lowest offset. The profile of the noise at lower signals levels is predominantly dominated by the system noise that is comprised mainly of 1/f noise or white noise. The INA228-Q1 effective resolution of the ADC can be increased by increasing the conversion time and increasing the number of averages.

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Table 2 summarizes the output data rate conversion settings supported by the device. The fastest conversion setting is 50 µs. Typical noise-free resolution is represented as Effective Number of Bits (ENOB) based on device measured data. The ENOB are calculated based on noise peak-to-peak values, which assures that full noise distribution is taken into consideration.

Table 2. INA228-Q1 Noise Performance

ADC CONVERSION TIME PERIOD [µs]	OUTPUT SAMPLE AVERAGING [SAMPLES]	OUTPUT SAMPLE PERIOD [ms]	NOISE-FREE ENOB (±163.84-mV) (ADCRANGE = 0)	NOISE-FREE ENOB (±40.96-mV) (ADCRANGE = 1)
50	1	0.05	12.8	9.9
84		0.084	12.8	10.9
150		0.15	13.1	11.3
280		0.28	13.6	11.4
540		0.54	14.5	12.5
1052		1.052	14.8	13
2074		2.074	14.9	13.1
4120		4.12	15.7	13.6
50	4	0.2	13.4	11.8
84		0.336	13.5	12.1
150		0.6	14.1	12.1
280		1.12	14.8	12.6
540		2.16	15.4	13.2
1052		4.208	15.5	13.9
2074		8.296	16.4	14.3
4120		16.48	16.5	14.4
50	16	0.8	14.4	12.3
84		1.344	14.7	12.6
150		2.4	15.2	13.2
280		4.48	15.6	13.8
540		8.64	16.2	14.2
1052		16.832	16.5	14.7
2074		33.184	17.1	15.2
4120		65.92	17.7	16
50	64	3.2	15.4	13.4
84		5.376	15.6	13.4
150		9.6	16	14.5
280		17.92	16.7	14.6
540		34.56	17.1	15.3
1052		67.328	17.4	15.7
2074		132.736	18.1	16.4
4120		263.68	18.1	16.5
50	128	6.4	15.7	14
84		10.752	16	14.1
150		19.2	16.9	14.9
280		35.84	17.4	15.4
540		69.12	17.7	15.9
1052		134.656	18.1	15.9
2074		265.472	18.7	16.7
4120		527.36	18.7	16.9

Table 2. INA228-Q1 Noise Performance (continued)

ADC CONVERSION TIME PERIOD [µs]	OUTPUT SAMPLE AVERAGING [SAMPLES]	OUTPUT SAMPLE PERIOD [ms]	NOISE-FREE ENOB (±163.84-mV) (ADCRANGE = 0)	NOISE-FREE ENOB (±40.96-mV) (ADCRANGE = 1)
50	256	12.8	16.5	14.2
84		21.504	16.7	14.5
150		38.4	17.4	15.5
280		71.68	17.4	15.8
540		138.24	18.7	16.4
1052		269.312	18.7	16.7
2074		530.944	18.7	17.1
4120		1054.72	19.7	17.7
50	512	25.6	16.9	15.1
84		43	17.1	15.3
150		76.8	17.7	16
280		143.36	18.1	16.1
540		276.48	18.7	16.9
1052		538.624	19.7	16.9
2074		1061.888	19.7	17.7
4120		2109.44	20	18.1
50	1024	51.2	17.4	15
84		86.016	17.7	15.7
150		153.6	18.7	16.1
280		286.72	18.7	16.5
540		552.96	18.7	16.9
1052		1077.248	19.7	17.7
2074		2123.776	19.7	18.1
4120		4218.88	20	18.7

7.3.4 Current Calculation

For the INA228-Q1 device to report current values in Ampere units, a conversion constant value must be written in the CURRLSBCALC_3 register that is dependant on the maximum measured current and the shunt resistance used in the application. The CURRLSBCALC_3 register is calculated based on Equation 1. The term CURRENT_LSB is the LSB step size for the CURRENT register where the current in Amperes is stored. The value of CURRENT_LSB is based on the maximum expected current as shown in Equation 2, and it directly defines the resolution of the CURRENT register. While the smallest CURRENT_LSB value yields highest resolution, it is common to select a higher round-number (no higher than 8x) value for the CURRENT_LSB in order to simplify the conversion of the CURRENT.

The R_{SHUNT} term is the resistance value of the external shunt used to develop the differential voltage across the input pins.

$$CURRLSBCALC = 13107.2 \times 10^{6} \times CURRENT\_LSB \times R_{SHUNT} \quad (1)$$

where

- 13107.2 x 10e6 is an internal fixed value used to ensure scaling is maintained properly

$$CURRENT\_LSB = \frac{\text{Maximum Expected Current}}{2^{19}} \quad (2)$$

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Note that the current is calculated following a shunt voltage measurement based on the value set in the CURRLSBCALC_3 register. If the value loaded into the CURRLSBCALC_3 register is zero, the current value reported through the CURRENT register is also zero.

After programming the CURRLSBCALC_3 register with the calculated value, the measured current in Amperes can be read from the CURRENT register. The final value is scaled by CURRENT_LSB and calculated in Equation 3:

Current [A] = CURRENT_LSB x CURRENT

where

- CURRENT is the value read from the CURRENT register (3)

7.3.5 Power, Energy, and Charge Accumulation

The current and charge are calculated after a shunt voltage measurement, while the power and energy are calculated after a bus voltage measurement as shown in Figure 4. Power and energy are calculated based on the previous current calculation and the latest bus voltage measurement. If the value loaded into the CURRLSBCALC_3 register is zero, the power, energy and charge values reported are also zero.

The current and power values are considered intermediate results (unless the averaging is set to 1) and are stored in an internal accumulation register. Following every measured sample, the newly-calculated values for current and power are appended to this accumulation register until all of the samples have been measured and averaged. After all of the samples have been measured and the corresponding current and power calculations have been made, the accumulated average for each of these parameters is then loaded to the corresponding output registers where they can then be read.

The energy and charge values are accumulated over time and get updated immediately following a conversion cycle. Therefore the INA228-Q1 averaging function is not applied to these.

These calculations are performed in the background and do not add to the overall conversion time.

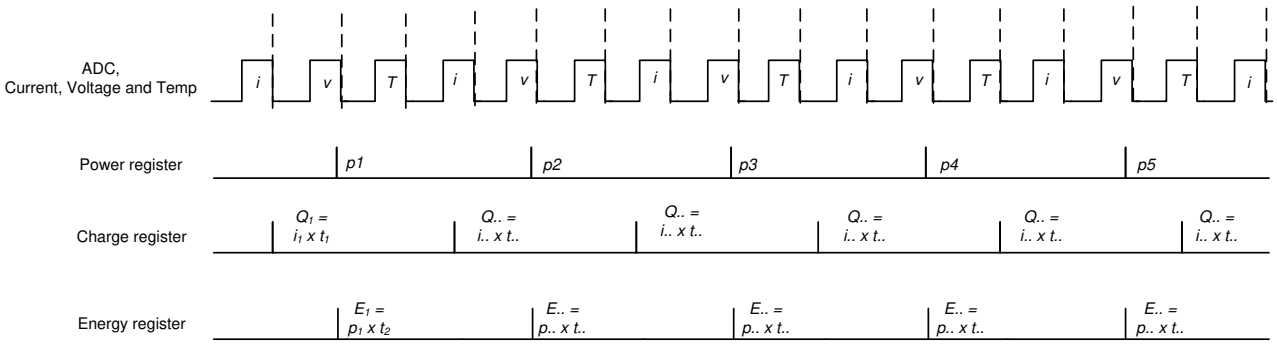

Figure 4. Power, Energy and Charge Calculation Scheme

The power value can be read from the POWER register as a 24-bit value and converted to Watts by using Equation 4:

Power [W] = 3.2 x CURRENT_LSB x POWER

where

- POWER is the value read from the POWER register.
- CURRENT_LSB is the lsb size of the current calculation as described in *Current Calculation*. (4)

The energy value can be read from the ENERGY register as a 40-bit unsigned value in Joules units. The energy value in Joules is converted by using Equation 5:

Energy [J] = 16 x 3.2 x CURRENT_LSB x ENERGY (5)

The charge value can be read from the CHARGE register as a 40-bit, two's complement value in Coulombs. The charge value in Coulomb is converted by using Equation 6:

Charge [C] = CURRENT_LSB x CHARGE

where

- CHARGE is the value read from the CHARGE register.
- CURRENT_LSB is the lsb size of the current calculation as described in *Current Calculation*. (6)

Upon overflow, the ENERGY and CHARGE registers will roll over and start from zero. The register values can also be reset at any time by setting the RSTACC bit in the CONFIG_1 register.

7.3.6 Temperature Measurement and Correction

The INA228-Q1 device has an internal temperature sensor which can measure die temperature from –40 °C to +125 °C. The accuracy of the temperature sensor is ±2 °C. The temperature value is stored inside the DIETEMP register and can be read through the digital interface.

An additional temperature compensation feature is implemented with capability to compensate for shunt resistor temperature dependancy. This feature can be enabled by setting the TEMPCOMP bit in the CONFIG_1 register, while the TEMPCOCONFIG_4 is the register that can be programmed to enter the temperature coefficient of the used shunt. The full scale value of the TEMPCOCONFIG_4 register is 16384 ppm/°C. The temperature compensation is related to room (+25 °C) temperature. The shunt is always assumed to have a positive temperature coefficient and the temperature compensation follows Equation 7:

$$R_{ADJ} = R_{NOM} + \frac{R_{NOM} \text{ x } (DIETEMP - 25) \text{ x } TEMPCOCONFIG\_4}{10^6}$$

where

- R_{NOM} is the nominal shunt resistance in Ohms at 25 °C.
- DIETEMP is the temperature value in the DIETEMP register. (7)

When this feature is enabled and correctly programmed, the CURRENT register data is corrected by constantly monitoring the die temperature and is now a function of temperature.

NOTE

Warning: If temperature compensation is enabled under some conditions, the calculated current result may be lower than the actual value. This condition typically occurs when the device is under normal operation, there is a high value of shunt voltage (>70% of full range), there is a shunt with high temperature-coefficient value (>2000), and there is a high temperature (>100°C). Consider the example of constant current flowing through a high temperature coefficient shunt such that at lower temperatures the shunt voltage is in its upper range. As the temperature increases, the device will correctly report a constant current until the maximum shunt voltage is reached. As temperature continues to increase after the maximum shunt voltage is reached, the device will start reporting lower currents. This is because the effective resistance calculated will continue to increase while the detected shunt voltage will remain constant (maximum).

7.3.7 Clock Source

The device is clocked by a precision internal oscillator trimmed to provide <1% error across temperature. The precision clock is the timing source for ADC conversion and time-count used for calculation of energy and charge. The digital filter response varies significantly with the clock precision, therefore the precision clock ensures filter response and notch frequency consistency across temperature. On power up, the internal oscillator takes roughly 50 µs to reach <1% error stability. Once the clock reaches stable condition, the ADC data output will be accurate to the electrical specifications provided in the *Specifications* section.

7.3.8 Multi-Alert Monitoring System

The INA228-Q1 includes a multipurpose, open-drain ALERT output pin that can be configured to report multiple diagnostics while it can also be used to report ADC conversion ready flag when the device is operating in both triggered or continuous conversion mode. The diagnostics listed in Table 3 are constantly monitored and can be reported through the ALERT pin whenever the monitored output value crosses its associated out-of-range threshold:

Table 3. ALERT Diagnostics Description

INA228-Q1 DIAGNOSTIC	STATUS BIT IN DIAG_ALRT REGISTER (RO)	OUT-OF-RANGE THRESHOLD REGISTER (R/W)	REGISTER DEFAULT VALUE
Shunt Under Voltage Limit	SHNTUL	SUVL	0x8000 h (two's complement)
Shunt Over Voltage Limit	SHNTOL	SOVL	0x7FFF h (two's complement)
Bus Voltage Over-Limit	BUSOL	BOVL	0x7FFF h (two's complement, positive values only)
Bus Voltage Under-Limit	BUSUL	BUVL	0x0000 h (two's complement, positive values only)
Temperature Over-Limit	TMPOL	TEMP_LIMIT	0xFFFF h (unsigned, positive values only)
Power Over-Limit	POL	PWR_LIMIT	0x7FFF h (two's complement)

A read of the DIAG_ALRT register is used to determine which diagnostic has triggered the ALERT pin. This register is also used to monitor other associated diagnostics as well as configure some ALERT pin functions.

- Alert Latch Enable — In case the ALERT pin is triggered, this function will hold the value of the pin even after all diagnostic conditions have cleared. A read of the DIAG_ALRT register will reset the status of the ALERT pin. This function is enabled by setting the ALRLEN bit.
- Conversion Ready Enable — Enables the ALERT pin to assert when an ADC conversion has completed and output values are ready to be read through the digital interface. This function is enabled by setting the CNVR bit. The conversion completed events can also be read through the CNVRF bit regardless of the CNVR bit setting.
- Alert comparison on averaged output — Allows the out-of-range threshold value to be compared to the averaged data values produced by the ADC. This helps to additionally remove noise from the output data when compared to the out-of-range threshold to avoid false alerts due to noise, however the diagnostic will be reported with additional time delay due to time needed for averaging. This function is enabled by setting the SLWALRT bit
- Alert polarity — Allows the device to invert the active state of the ALERT pin. The ALERT pin is active-low when disabled and active-high when the pin is enabled. Note that the ALERT pin is an open-drain output that must be resistive pulled-up under all conditions. This function is enabled by setting the APOL bit.

Other diagnostic functions that are not reported by the ALERT pin but are available by reading the DIAG_ALRT register:

- Math Overflow — Indicated by the MOVF bit, reports when an arithmetic operation has caused an internal register overflow.
- Memory Status — Indicated by the MEMSTAT bit, monitors the health of the device non-volatile trim memory. This bit should always read '1' when the device is operating properly.
- Energy Overflow — Indicated by the ENRGOF bit, reports when the ENERGY register has reached an overflow state due to data accumulation.
- Charge Overflow — Indicated by the CHROF bit, reports when the CHARGE register has reached an overflow state due to data accumulation.

When the ALERT pin is configured to report the ADC conversion complete event, the ALERT pin becomes a multipurpose reporting output. Figure 5 shows an example where the device reports ADC conversion complete events while the INA228-Q1 device is subject to shunt overvoltage (overcurrent) event, bus undervoltage event, overtemperature event and over power-limit event.

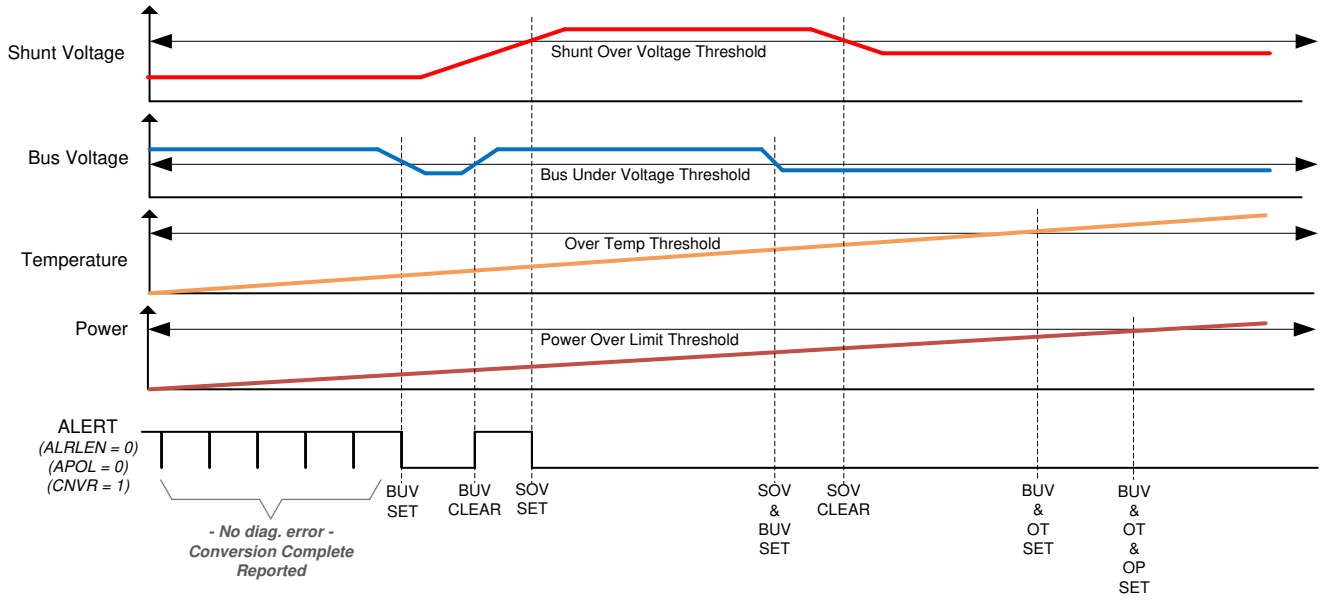

Figure 5. Multi-Alert Configuration

7.4 Device Functional Modes

7.4.1 Shutdown Mode

In addition to the two conversion modes (continuous and triggered), the device also has a shutdown mode (selected by the MODE bits in ADCCONFIG_2 register) that reduces the quiescent current to less than 5 µA and turns off current into the device inputs, reducing the impact of supply drain when the device is not being used. The registers of the device can be written to and read from while the device is in shutdown mode. The device remains in shutdown mode until the ADCCONFIG_2 register is written with a continuous or triggered setting in the MODE bits. There are no special considerations for power-supply sequencing because the common-mode input range and power-supply voltage are independent of each other; therefore, the bus voltage can be present with the supply voltage off, and vice-versa.

7.4.2 Power-On Reset

Power-on reset (POR) is asserted when V_S drops below 2 V (typical) at which all of the registers are reset to their default values. A manual device reset can be initiated by setting the RST bit int the CONFIG_1 register. The default power-up register values are shown in the *Register Maps* section.

7.5 Programming

7.5.1 I²C Serial Interface

The INA228-Q1 operates only as a slave device on both the I²C bus and SMBus. Connections to the bus are made through the open-drain SDA and SCL lines. The SDA and SCL pins feature integrated spike suppression filters and Schmitt triggers to minimize the effects of input spikes and bus noise. Although the device integrates spike suppression into the digital I/O lines, proper layout techniques help minimize the amount of coupling into the communication lines. This noise introduction could occur from capacitively coupling signal edges between the two communication lines themselves or from other switching noise sources present in the system. Routing traces in parallel with ground in between layers on a printed-circuit board (PCB) typically reduces the effects of coupling between the communication lines. Shielded communication lines reduces the possibility of unintended noise coupling into the digital I/O lines that could be incorrectly interpreted as start or stop commands.

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Programming (continued)

The INA228-Q1 supports the transmission protocol for fast mode (1 kHz to 400 kHz) and high-speed mode (1 kHz to 2.94 MHz). All data bytes are transmitted most significant byte first.

To communicate with the INA228-Q1, the master must first address slave devices through a slave address byte. The slave address byte consists of seven address bits and a direction bit that indicates whether the action is to be a read or write operation.

The device has two address pins, A0 and A1. Table 4 lists the pin logic levels for each of the 16 possible addresses. The device samples the state of pins A0 and A1 on every bus communication. Establish the pin states before any activity on the interface occurs. When connecting the SDA pin to either A0 or A1 to set the device address, additional hold time is needed on the MSB of the I2C address to insure correct device addressing.

Table 4. Address Pins and Slave Addresses

A1	A0	SLAVE ADDRESS
GND	GND	1000000
GND	VS	1000001
GND	SDA	1000010
GND	SCL	1000011
VS	GND	1000100
VS	VS	1000101
VS	SDA	1000110
VS	SCL	1000111
SDA	GND	1001000
SDA	VS	1001001
SDA	SDA	1001010
SDA	SCL	1001011
SCL	GND	1001100
SCL	VS	1001101
SCL	SDA	1001110
SCL	SCL	1001111

7.5.1.1 Writing to and Reading Through the I^2C Serial Interface

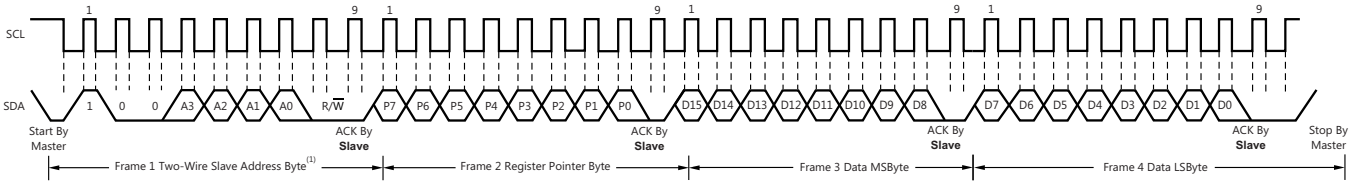
Accessing a specific register on the INA228-Q1 is accomplished by writing the appropriate value to the register pointer. Refer to *Register Maps* for a complete list of registers and corresponding addresses. The value for the register pointer (as shown in Figure 8) is the first byte transferred after the slave address byte with the R/$\overline{W}$ bit low. Every write operation to the device requires a value for the register pointer.

Writing to a register begins with the first byte transmitted by the master. This byte is the slave address, with the R/$\overline{W}$ bit low. The device then acknowledges receipt of a valid address. The next byte transmitted by the master is the address of the register to be accessed. This register address value updates the register pointer to the desired internal device register. The next two bytes are written to the register addressed by the register pointer. The device acknowledges receipt of each data byte. The master may terminate data transfer by generating a start or stop condition.

When reading from the device, the last value stored in the register pointer by a write operation determines which register is read during a read operation. To change the register pointer for a read operation, a new value must be written to the register pointer. This write is accomplished by issuing a slave address byte with the R/$\overline{W}$ bit low, followed by the register pointer byte. No additional data are required. The master then generates a start condition and sends the slave address byte with the R/$\overline{W}$ bit high to initiate the read command. The next byte is transmitted by the slave and is the most significant byte of the register indicated by the register pointer. This byte is followed by an *Acknowledge* from the master; then the slave transmits the least significant byte. The master may or may not acknowledge receipt of the second data byte. The master may terminate data transfer by generating a *Not-Acknowledge* after receiving any data byte, or generating a start or stop condition. If repeated reads from the same register are desired, it is not necessary to continually send the register pointer bytes; the device retains the register pointer value until it is changed by the next write operation.

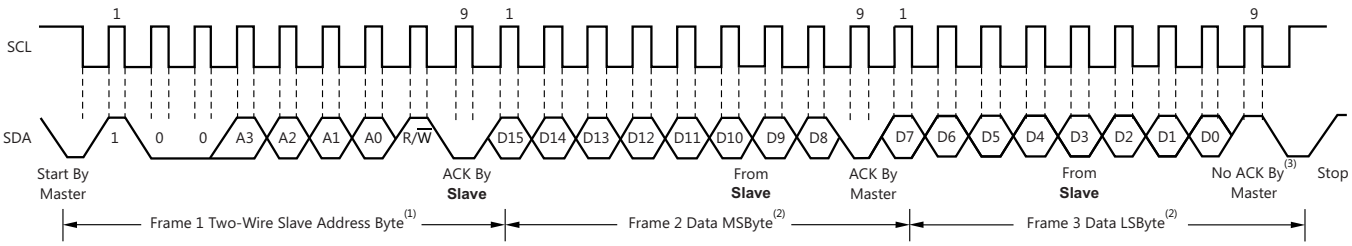
Figure 6 shows the write operation timing diagram. Figure 7 shows the read operation timing diagram. These diagrams are shown for reading/writing to 16 bit registers. Registers with a higher number by bits will behave similarly.

Register bytes are sent most-significant byte first, followed by the least significant byte.



(1) The value of the Slave Address byte is determined by the settings of the A0 and A1 pins. Refer to Table 4.

Figure 6. Timing Diagram for Write Word Format

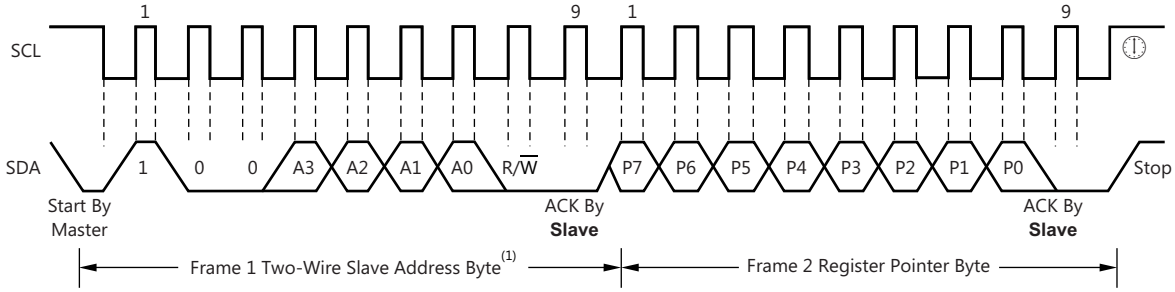


(1) The value of the Slave Address byte is determined by the settings of the A0 and A1 pins. Refer to Table 4.

(2) Read data is from the last register pointer location. If a new register is desired, the register pointer must be updated. See Figure 8.

(3) ACK by Master can also be sent.

Figure 7. Timing Diagram for Read Word Format



(1) The value of the Slave Address Byte is determined by the settings of the A0 and A1 pins. Refer to Table 4.

Figure 8. Typical Register Pointer Set

7.5.1.2 High-Speed I²C Mode

When the bus is idle, both the SDA and SCL lines are pulled high by the pullup resistors. The master generates a start condition followed by a valid serial byte containing high-speed (HS) master code *00001XXX*. This transmission is made in fast (400 kHz) or standard (100 kHz) (F/S) mode at no more than 400 kHz. The device does not acknowledge the HS master code, but does recognize it and switches its internal filters to support 2.94-MHz operation.

The master then generates a repeated start condition (a repeated start condition has the same timing as the start condition). After this repeated start condition, the protocol is the same as F/S mode, except that transmission speeds up to 2.94 MHz are allowed. Instead of using a stop condition, use repeated start conditions to secure the bus in HS-mode. A stop condition ends the HS-mode and switches all the internal filters of the device to support the F/S mode.

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7.6 Register Maps

7.6.1 INA228-Q1 Registers

Table 5 lists the INA228-Q1 registers. All register locations not listed in Table 5 should be considered as reserved locations and the register contents should not be modified.

Table 5. INA228-Q1 Registers

Offset	Acronym	Register Name	Register size (bits)	Section
0h	CONFIG_1	Configuration	16	Go
1h	ADCCONFIG_2	ADC Configuration	16	Go
2h	CURRLSBCALC_3	Shunt Calibration	16	Go
3h	TEMPCOCONFIG_4	Shunt Temperature Coefficient	16	Go
4h	VSHUNT	Shunt Voltage Measurement	24	Go
5h	VBUS	Bus Voltage Measurement	24	Go
6h	DIETEMP	Temperature Measurement	16	Go
7h	CURRENT	Current Result	24	Go
8h	POWER	Power Result	24	Go
9h	ENERGY	Energy Result	40	Go
Ah	CHARGE	Charge Result	40	Go
Bh	DIAG_ALRT	Diagnostic Flags and Alert	16	Go
Ch	SOVL	Shunt Overvoltage Threshold	16	Go
Dh	SUVL	Shunt Undervoltage Threshold	16	Go
Eh	BOVL	Bus Overvoltage Threshold	16	Go
Fh	BUVL	Bus Undervoltage Threshold	16	Go
10h	TEMP_LIMIT	Temperature Over-Limit Threshold	16	Go
11h	PWR_LIMIT	Power Over-Limit Threshold	16	Go
3Eh	MANUFACTURER_ID	Manufacturer ID	16	Go
3Fh	DEVICE_ID	Device ID	16	Go

Complex bit access types are encoded to fit into small table cells. Table 6 shows the codes that are used for access types in this section.

Table 6. INA228-Q1 Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

7.6.1.1 Configuration (CONFIG_1) Register (Offset = 0h) [reset = 0h]

CONFIG_1 is shown in Table 7.

Return to the Summary Table.

Table 7. CONFIG_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RST	R/W	0h	Reset Bit. Setting this bit to '1' generates a system reset that is the same as power-on reset. Resets all registers to default values. 0h = Normal Operation 1h = System Reset sets registers to default values This bit self-clears.
14	RSTACC	R/W	0h	Resets the contents of accumulation registers ENERGY and CHARGE to 0 0h = Normal Operation 1h = Clears registers to default values for ENERGY and CHARGE registers
13-6	CONVDLY	R/W	0h	Sets the Delay for initial ADC conversion in steps of 2 ms. 0h = 0 s 1h = 2 ms FFh = 510 ms
5	TEMPCOMP	R/W	0h	Enables temperature compensation of an external shunt 0h = Shunt Temperature Compensation Disabled 1h = Shunt Temperature Compensation Enabled
4	ADCRANGE	R/W	0h	Shunt full scale range selection across IN+ and IN–. 0h = ±163.84 mV 1h = ± 40.96 mV
3-0	RESERVED	R/W	0h	Reserved. Always reads 0.

7.6.1.2 ADC Configuration (ADCCONFIG_2) Register (Offset = 1h) [reset = FB68h]

ADCCONFIG_2 is shown in Table 8.

Return to the Summary Table.

Table 8. ADCCONFIG_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	MODE	R/W	Fh	The device can operate in either shutdown mode, continuous mode, or triggered mode. The user can select the MUX settings to continuous or triggered mode on bus voltage, shunt voltage or temperature measurement. 0h = Shutdown 1h = Bus Voltage triggered, single shot 2h = Shunt Voltage triggered, single shot 3h = Shunt voltage and Bus voltage triggered, single shot 4h = Temperature measurement triggered, single shot 5h = Temperature and bus voltage measurement triggered, single shot 6h = Temperature and Shunt voltage measurement triggered, single shot 7h = Bus voltage, Shunt voltage and Temperature measurement triggered, single shot 8h = Shutdown 9h = Continuous Bus voltage Ah = Continuous Shunt voltage Bh = Continuous Shunt and Bus voltage Ch = Continuous Temperature measurement Dh = Continuous Bus voltage and Temperature measurement Eh = Continuous Temperature and Shunt voltage Fh = Continuous Bus, Shunt voltage and Temperature
11-9	VBUSCT	R/W	5h	Sets the conversion time of the bus voltage measurement: 0h = 50 µs 1h = 84 µs 2h = 150 µs 3h = 280 µs 4h = 540 µs 5h = 1052 µs 6h = 2074 µs 7h = 4120 µs
8-6	VSHCT	R/W	5h	Sets the conversion time of the shunt voltage measurement: 0h = 50 µs 1h = 84 µs 2h = 150 µs 3h = 280 µs 4h = 540 µs 5h = 1052 µs 6h = 2074 µs 7h = 4120 µs

Table 8. ADCCONFIG_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-3	VTCT	R/W	5h	Sets the conversion time of the temperature measurement: 0h = 50 µs 1h = 84 µs 2h = 150 µs 3h = 280 µs 4h = 540 µs 5h = 1052 µs 6h = 2074 µs 7h = 4120 µs
2-0	AVG	R/W	0h	Selects ADC sample averaging count. The averaging setting applies to all active inputs. When >0h, the output registers are updated after the averaging has completed. 0h = 1 1h = 4 2h = 16 3h = 64 4h = 128 5h = 256 6h = 512 7h = 1024

7.6.1.3 Shunt Calibration (CURRLSBCALC_3) Register (Offset = 2h) [reset = 1000h]

CURRLSBCALC_3 is shown in Table 9.

Return to the Summary Table.

Table 9. CURRLSBCALC_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R/W	0h	Reserved. Always reads 0.
14-0	CURRLSB	R/W	1000h	The register provides the device with a conversion constant value that represents shunt resistance used to calculate current value in Amperes. This also sets the resolution for the CURRENT register. Value calculation under *Current Calculation*.

7.6.1.4 Shunt Temperature Coefficient (TEMPCOCONFIG_4) Register (Offset = 3h) [reset = 0h]

TEMPCOCONFIG_4 is shown in Table 10.

Return to the Summary Table.

Table 10. TEMPCOCONFIG_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R	0h	Reserved. Always reads 0.
13-0	TEMPCO	R/W	0h	Temperature coefficient of the shunt for temperature compensation correction. Calculated in respect to +25°C. The full scale value of the register is 16383 ppm/C. The 16 bit register provides a resolution of 1ppm/°C/LSB 0h = 0 ppm/°C FFFFh = 16383 ppm/°C

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7.6.1.5 Shunt Voltage Measurement (VSHUNT) Register (Offset = 4h) [reset = 0h]

VSHUNT is shown in Table 11.

Return to the Summary Table.

Table 11. VSHUNT Register Field Descriptions

Bit	Field	Type	Reset	Description
23-4	VSHUNT	R	0h	Differential voltage measured across the shunt output. Two's complement value. Conversion factor: 312.5 nV/LSB when ADCRANGE = 0 78.125 nV/LSB when ADCRANGE = 1
3-0	RESERVED	R	0h	Reserved. Always reads 0.

7.6.1.6 Bus Voltage Measurement (VBUS) Register (Offset = 5h) [reset = 0h]

VBUS is shown in Table 12.

Return to the Summary Table.

Table 12. VBUS Register Field Descriptions

Bit	Field	Type	Reset	Description
23-4	VBUS	R	0h	Bus voltage output. Two's complement value, however always positive. Conversion factor: 195.3125 µV/LSB
3-0	RESERVED	R	0h	Reserved. Always reads 0.

7.6.1.7 Temperature Measurement (DIETEMP) Register (Offset = 6h) [reset = 0h]

DIETEMP is shown in Table 13.

Return to the Summary Table.

Table 13. DIETEMP Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	DIETEMP	R	0h	Internal die temperature measurement. Two's complement value. Conversion factor: 7.8125 m°C/LSB

7.6.1.8 Current Result (CURRENT) Register (Offset = 7h) [reset = 0h]

CURRENT is shown in Table 14.

Return to the Summary Table.

Table 14. CURRENT Register Field Descriptions

Bit	Field	Type	Reset	Description
23-4	CURRENT	R	0h	Calculated current output in Amperes. Two's complement value. Value description under *Current Calculation*.
3-0	RESERVED	R	0h	Reserved. Always reads 0.

7.6.1.9 Power Result (POWER) Register (Offset = 8h) [reset = 0h]

POWER is shown in Table 15.

Return to the Summary Table.

Table 15. POWER Register Field Descriptions

Bit	Field	Type	Reset	Description
23-0	POWER	R	0h	Calculated power output. Output value in W. Unsigned representation. Positive value. Value description under *Power, Energy, and Charge Accumulation*.

7.6.1.10 Energy Result (ENERGY) Register (Offset = 9h) [reset = 0h]

ENERGY is shown in Table 16.

Return to the Summary Table.

Table 16. ENERGY Register Field Descriptions

Bit	Field	Type	Reset	Description
39-0	ENERGY	R	0h	Calculated energy output. Unsigned representation. Positive value. Value description under *Power, Energy, and Charge Accumulation*.

7.6.1.11 Charge Result (CHARGE) Register (Offset = Ah) [reset = 0h]

CHARGE is shown in Table 17.

Return to the Summary Table.

Table 17. CHARGE Register Field Descriptions

Bit	Field	Type	Reset	Description
39-0	CHARGE	R	0h	Calculated charge output. Two's complement value. Value description under *Power, Energy, and Charge Accumulation*.

7.6.1.12 Diagnostic Flags and Alert (DIAG_ALRT) Register (Offset = Bh) [reset = 0001h]

DIAG_ALRT is shown in Table 18.

Return to the Summary Table.

Table 18. DIAG_ALRT Register Field Descriptions

Bit	Field	Type	Reset	Description
15	ALRLEN	R/W	0h	When the Alert Latch Enable bit is set to Transparent mode, the Alert pin and Flag bit resets to the idle states when the fault has been cleared. When the Alert Latch Enable bit is set to Latch mode, the Alert pin and Alert Flag bit remain active following a fault until the DIAG_ALRT Register has been read. 0h = Transparent 1h = Latched
14	CNVR	R/W	0h	Setting this bit high configures the Alert pin to be asserted when the Conversion Ready Flag (bit 1) is asserted, indicating that a conversion cycle has completed. 0h = Disable conversion ready flag on ALERT pin 1h = Enables conversion ready flag on ALERT pin

Table 18. DIAG_ALRT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	SLWALRT	R/W	0h	ALERT function is asserted on the completed averaged value. This gives the flexibility to delay the ALERT after the averaged value. 0h = ALERT comparison on non-averaged (ADC) value 1h = ALERT comparison on Averaged value
12	APOL	R/W	0h	Alert Polarity bit sets the Alert pin polarity. 0h = Normal (Active-low open-drain) 1h = Inverted (active-high)
11	ENRGOF	R	0h	This bit indicates the health of the ENERGY register. If the 40 bit ENERGY register has overflowed this bit is set to 1. 0h = Normal 1h = Overflow Clears when the ENERGY register is read.
10	CHROF	R	0h	This bit indicates the health of the CHARGE register. If the 40 bit CHARGE register has overflowed this bit is set to 1. 0h = Normal 1h = Overflow Clears when the CHARGE register is read.
9	MOVF	R/W	0h	This bit is set to 1 if an arithmetic operation resulted in an overflow error. It indicates that current and power data may be invalid. 0h = Normal 1h = Overflow
8	RESERVED	R/W	0h	Reserved. Always read 0.
7	TMPOL	R/W	0h	This bit is set to 1 if the temperature measurement exceeds the threshold limit in the temperature over-limit register. 0h = Normal 1h = Over Temp Event When ALRLEN =1 this bit is cleared by reading the register.
6	SHNTOL	R/W	0h	This bit is set to 1 if the shunt voltage measurement exceeds the threshold limit in the shunt over-limit register. 0h = Normal 1h = Over Shunt Voltage Event When ALRLEN =1 this bit is cleared by reading the register.
5	SHNTUL	R/W	0h	This bit is set to 1 if the shunt voltage measurement falls below the threshold limit in the shunt under-limit register. 0h = Normal 1h = Under Shunt Voltage Event When ALRLEN =1 this bit is cleared by reading the register.
4	BUSOL	R/W	0h	This bit is set to 1 if the bus voltage measurement exceeds the threshold limit in the bus over-limit register. 0h = Normal 1h = Bus Over-Limit Event When ALRLEN =1 this bit is cleared by reading the register.
3	BUSUL	R/W	0h	This bit is set to 1 if the bus voltage measurement falls below the threshold limit in the bus under-limit register. 0h = Normal 1h = Bus Under-Limit Event When ALRLEN =1 this bit is cleared by reading the register.
2	POL	R/W	0h	This bit is set to 1 if the power measurement exceeds the threshold limit in the power limit register. 0h = Normal 1h = Power Over-Limit Event When ALRLEN =1 this bit is cleared by reading the register.

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Table 18. DIAG_ALRT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	CNVRF	R/W	0h	This bit is set to 1 if the conversion is completed. 0h = Normal 1h = Conversion completed Event When ALRLEN =1 this bit is cleared by reading the register or starting a new triggered conversion.
0	MEMSTAT	R/W	1h	This bit is set to 0 if a checksum error had been detected in the device trim memory space. 0h = Memory Checksum Error 1h = Normal Operation

7.6.1.13 Shunt Overvoltage Threshold (SOVL) Register (Offset = Ch) [reset = 7FFFh]

SOVL is shown in Table 19.

Return to the Summary Table.

Table 19. SOVL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	SOVL	R/W	7FFFh	Sets the threshold for comparison of the value to detect Shunt Overvoltage (overcurrent protection). Two's complement value. Clarification on negative values – This comparison uses the actual values. If a negative value such as –10 is entered in this register then a voltage/current measurement result of 0 will trip this alarm. In this situation the meaning of the Shunt Over/Undervoltage may be switched (example: set the Shunt Undervoltage limit to –10 and the Shunt Overvoltage limit to something greater than –10 but still a potentially negative value).

7.6.1.14 Shunt Undervoltage Threshold (SUVL) Register (Offset = Dh) [reset = 8000h]

SUVL is shown in Table 20.

Return to the Summary Table.

Table 20. SUVL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	SUVL	R/W	8000h	Sets the threshold for comparison of the value to detect Shunt Undervoltage (undercurrent protection). Two's complement value.

7.6.1.15 Bus Overvoltage Threshold (BOVL) Register (Offset = Eh) [reset = 7FFFh]

BOVL is shown in Table 21.

Return to the Summary Table.

Table 21. BOVL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Reserved	R	0h	Reserved. Always reads 0.
14-0	BOVL	R/W	7FFFh	Sets the threshold for comparison of the value to detect Bus Overvoltage (overvoltage protection). Unsigned representation, positive value only.

7.6.1.16 Bus Undervoltage Threshold (BUVL) Register (Offset = Fh) [reset = 0h]

BUVL is shown in Table 22.

Return to the Summary Table.

Table 22. BUVL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Reserved	R	0h	Reserved. Always reads 0.
14-0	BUVL	R/W	0h	Sets the threshold for comparison of the value to detect Bus Undervoltage (undervoltage protection). Unsigned representation, positive value only.

7.6.1.17 Temperature Over-Limit Threshold (TEMP_LIMIT) Register (Offset = 10h) [reset = 7FFFh]

TEMP_LIMIT is shown in Table 23.

Return to the Summary Table.

Table 23. TEMP_LIMIT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	TOL	R/W	7FFFh	Sets the threshold for comparison of the value to detect over temperature measurements. Two's complement value. Value in line to DIETEMP register value.

7.6.1.18 Power Over-Limit Threshold (PWR_LIMIT) Register (Offset = 11h) [reset = FFFFh]

PWR_LIMIT is shown in Table 24.

Return to the Summary Table.

Table 24. PWR_LIMIT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	POL	R/W	FFFFh	Sets the threshold for comparison of the value to detect power over-limit measurements. Unsigned representation, positive value only. Value in line to POWER register value.

7.6.1.19 Manufacturer ID (MANUFACTURER_ID) Register (Offset = 3Eh) [reset = 5449h]

MANUFACTURER_ID is shown in Table 25.

Return to the Summary Table.

Table 25. MANUFACTURER_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	MANFID	R	5449h	Reads back TI in ASCII.

7.6.1.20 Device ID (DEVICE_ID) Register (Offset = 3Fh) [reset = 2280h]

DEVICE_ID is shown in Table 26.

Return to the Summary Table.

Table 26. DEVICE_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
15-4	DIEID	R	228h	Stores the device identification bits.
3-0	REV_ID	R	0h	Device revision identification.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Validate and test the design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Input Filtering Considerations

The INA228-Q1 device offers several options for input noise filtering by allowing the user to select the conversion times and number of averages independently in the ADCCONFIG_2 register. The conversion times can be set independently for the shunt voltage and bus voltage measurements to allow added flexibility in configuring the monitoring of the power-supply bus.

The internal ADC has good inherent noise rejection, however the transients that occur at or very close to the sampling rate harmonics can cause problems. Because these signals are at 1 MHz and higher, they can be managed by incorporating filtering at the input of the device. The high frequency enables the use of low-value series resistors on the filter with negligible effects on measurement accuracy. For best results, filter using the lowest possible series resistance (typically 100 Ω or less) and a ceramic capacitor. Recommended values for this capacitor are between 0.1 µF and 1 µF. Figure 9 shows the device with a filter added at the input.

Overload conditions are another consideration for the device inputs. The device inputs are specified to tolerate 20 V across the inputs. A large differential scenario might be a short to ground on the load side of the shunt. This type of event can result in full power-supply voltage across the shunt (as long the power supply or energy storage capacitors support it). Removing a short to ground can result in inductive kickbacks that could exceed the 20-V differential and common-mode rating of the device. Inductive kickback voltages are best controlled by Zener-type transient-absorbing devices (commonly called *transzorbs*) combined with sufficient energy storage capacitance. See the *Transient Robustness for Current Shunt Monitors* reference design which describes a high-side current shunt monitor used to measure the voltage developed across a current-sensing resistor when current passes through it.

In applications that do not have large energy storage electrolytics on one or both sides of the shunt, an input overstress condition may result from an excessive dV/dt of the voltage applied to the input. A hard physical short is the most likely cause of this event, particularly in applications with no large electrolytics present. This problem occurs because an excessive dV/dt can activate the ESD protection in the device in systems where large currents are available. Testing demonstrates that the addition of 10-Ω resistors in series with each input of the device sufficiently protects the inputs against this dV/dt failure up to the 20-V rating of the device. Selecting these resistors in the range noted has minimal effect on accuracy.

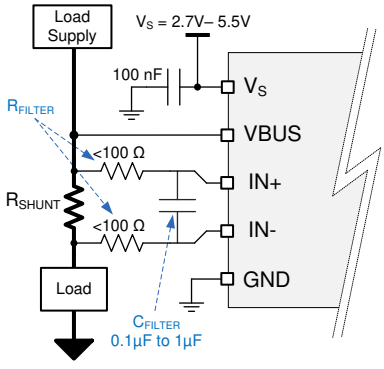


Figure 9. Input Filtering

ADVANCE INFORMATION

8.2 Typical Applications

The low offset voltage and low input bias current of the INA228-Q1 allow accurate monitoring of a wide range of currents. To accurately monitor currents with high resolution, select the value of the shunt resistor so that the resulting sense voltage is close to the maximum allowable differential input voltage range (either ±163.84 mV or ±40.96 mV, depending on register settings). The circuit for monitoring currents in a high-side configuration is shown in Figure 10.

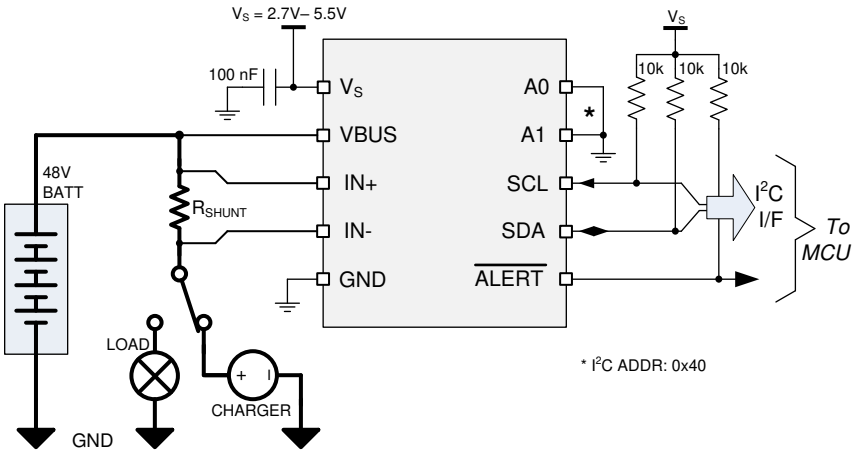


Figure 10. High-Side Sensing Application Diagram

8.2.1 Design Requirements

The INA228-Q1 measures the voltage developed across a current-sensing resistor (R_{SHUNT}) when current passes through it. The device also measures the bus supply voltage and calculates power when calibrated. It also comes with alert capability, where the alert pin can be programmed to respond to a user-defined event or a conversion ready notification.

The design requirements for the circuit shown in Figure 10 are listed in Table 27.

Table 27. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Power-supply voltage (V_S)	5 V
Bus supply rail (V_{CM})	48 V
Maximum sense current (I_{MAX})	±10 A
Maximum sense voltage (V_{SENSE_MAX})	±163.84 mV

8.2.2 Detailed Design Procedure

The maximum value of the shunt resistor is calculated based on the value of the maximum current to be sensed (I_{MAX}) and the maximum allowable sense voltage (V_{SENSE_MAX}). When operating at the maximum current, the input voltage must not exceed the input voltage specification, V_{SENSE_MAX}. Using Equation 8 for the given design parameters, the maximum value for R_{SHUNT} is calculated to be 16.38 mΩ. The closest standard resistor value of 16.2 mΩ is then selected. Also keep in mind that R_{SHUNT} must be able to handle the power dissipated across it in the maximum load condition.

$$R_{SHUNT} < \frac{V_{SENSE\_MAX}}{I_{MAX}} \quad (8)$$

9 Power Supply Recommendations

The input circuitry of the device can accurately measure signals on common-mode voltages beyond its power-supply voltage, V_{VS}. For example, the voltage applied to the V_{VS} power supply terminal can be 5 V, whereas the load power-supply voltage being monitored (the common-mode voltage) can be as high as 85 V. Note that the device can also withstand the full 0 V to 85 V range at the input terminals, regardless of whether the device has power applied or not.

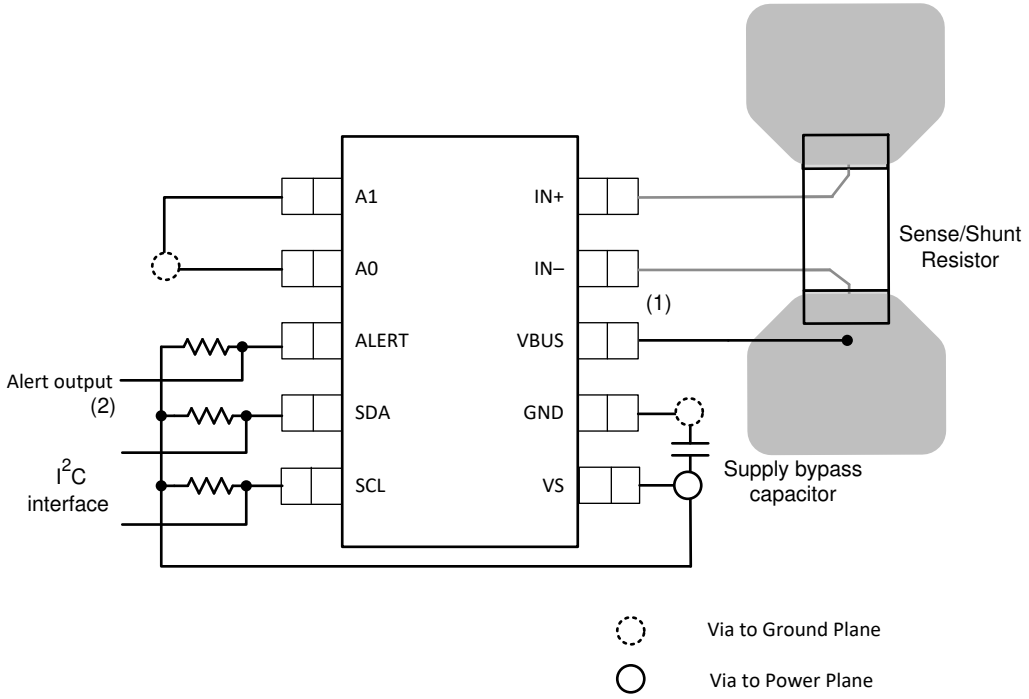
Place the required power-supply bypass capacitors as close as possible to the supply and ground terminals of the device to ensure stability. A typical value for this supply bypass capacitor is 0.1 µF. Applications with noisy or high-impedance power supplies may require additional decoupling capacitors to reject power-supply noise.

10 Layout

10.1 Layout Guidelines

Connect the input pins (IN+ and IN–) to the sensing resistor using a Kelvin connection or a 4-wire connection. These connection techniques ensure that only the current-sensing resistor impedance is detected between the input pins. Poor routing of the current-sensing resistor commonly results in additional resistance present between the input pins. Given the very low ohmic value of the current-sensing resistor, any additional high-current carrying impedance causes significant measurement errors. Place the power-supply bypass capacitor as close as possible to the supply and ground pins.

10.2 Layout Example



(1) Connect the VBUS pin to the voltage powering the load for load power calculations..

(2) Can be left floating if unused.

Figure 11. INA228-Q1 Layout Example

ADVANCE INFORMATION

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PINA228AQDGSRQ1	ACTIVE	VSSOP	DGS	10	2500	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

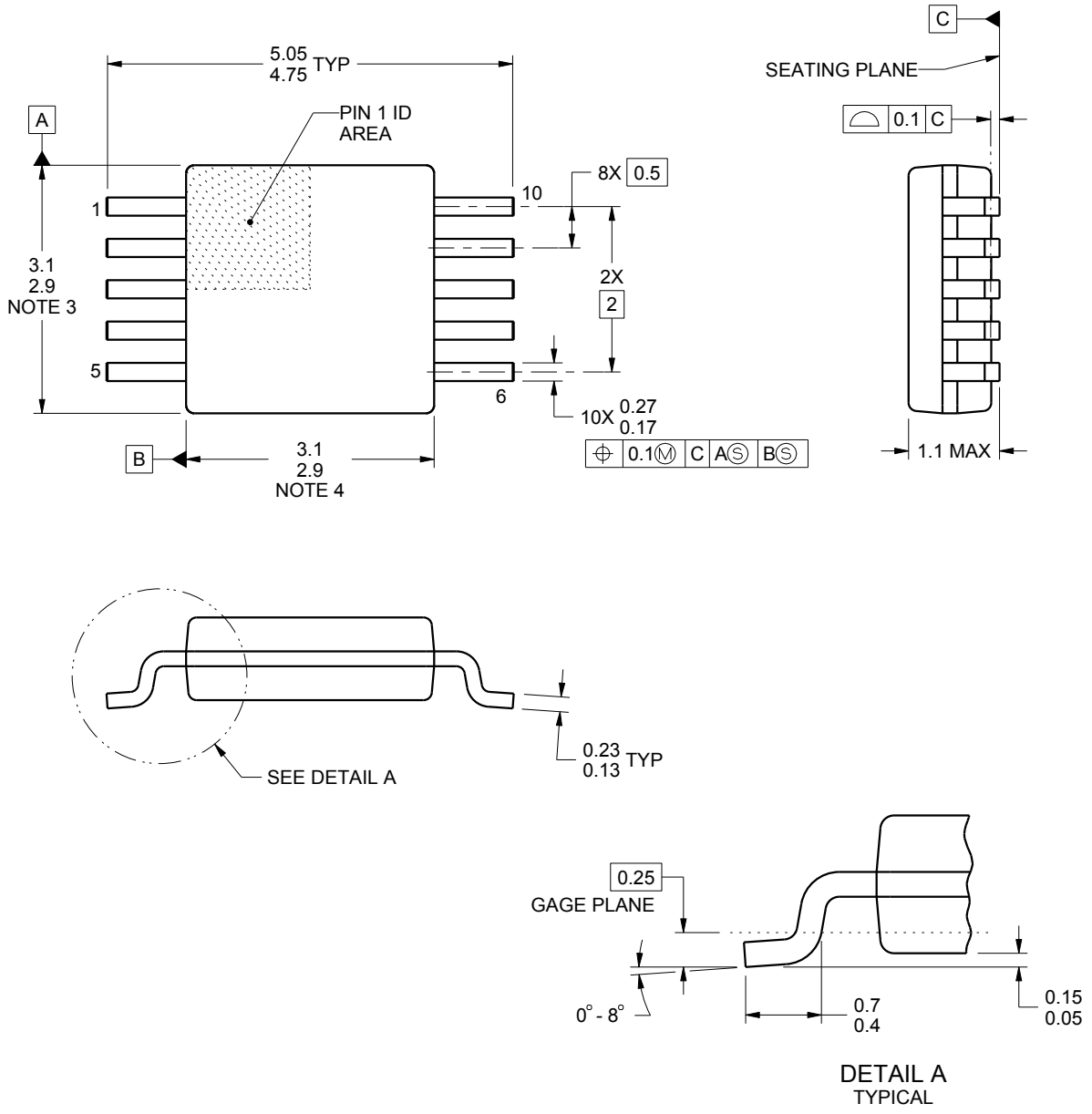
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

PACKAGE OUTLINE

DGS0010A

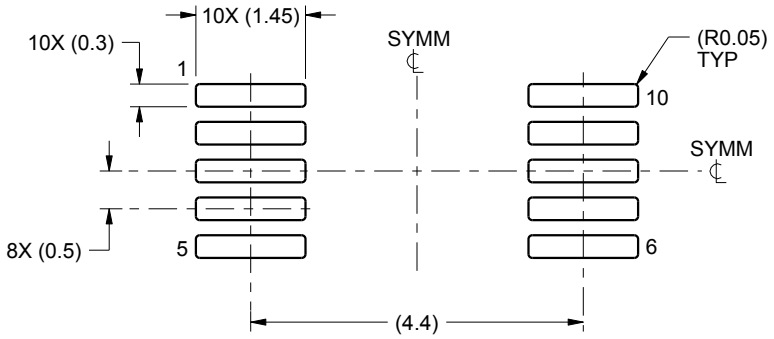
VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

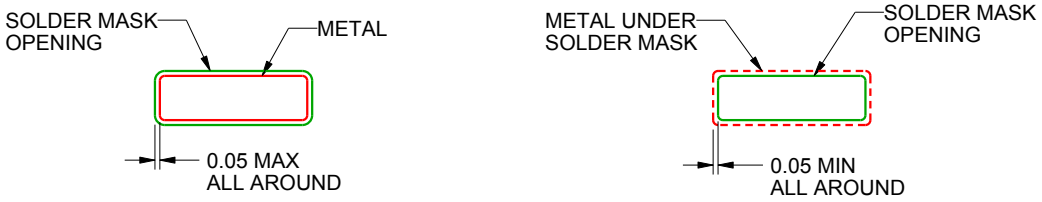


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X

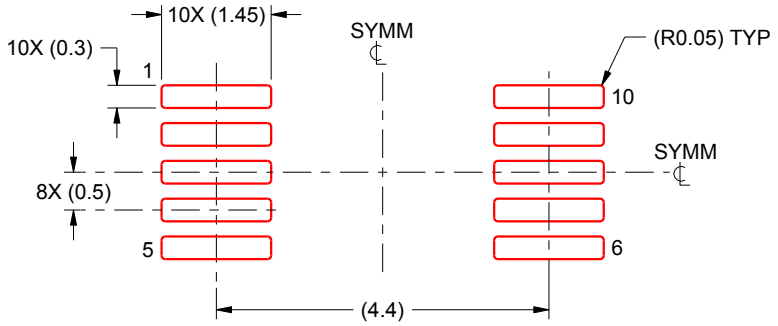


SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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