Stefan Marth – CSE 320 – LAB 3

1. The state transition and output tables for each FSM.

Location FSM Truth Table																		
Current State							Input					Next State						
S0	S1	S2	S3	S4	S5	S6	N	S	E	W	V	S0'	S1'	S2'	S3'	S4'	S5'	S6'
1	0	0	0	0	0	0	X	X	0	X	X	1	0	0	0	0	0	0
1	0	0	0	0	0	0	X	X	1	X	X	0	1	0	0	0	0	0
0	1	0	0	0	0	0	X	0	X	0	X	0	1	0	0	0	0	0
0	1	0	0	0	0	0	X	X	X	1	X	1	0	0	0	0	0	0
0	1	0	0	0	0	0	X	1	X	X	X	0	0	1	0	0	0	0
0	0	1	0	0	0	0	0	X	0	0	X	0	0	1	0	0	0	0
0	0	1	0	0	0	0	1	X	X	X	X	0	1	0	0	0	0	0
0	0	1	0	0	0	0	X	X	X	1	X	0	0	0	1	0	0	0
0	0	1	0	0	0	0	X	X	1	X	X	0	0	0	0	1	0	0
0	0	0	1	0	0	0	X	X	0	X	X	0	0	0	1	0	0	0
0	0	0	1	0	0	0	X	X	1	X	X	0	0	1	0	0	0	0
0	0	0	0	1	0	0	X	X	X	X	0	0	0	0	0	0	1	0
0	0	0	0	1	0	0	X	X	X	X	1	0	0	0	0	0	0	1
0	0	0	0	0	1	0	X	X	X	X	X	0	0	0	0	0	1	0
0	0	0	0	0	0	1	X	X	X	X	X	0	0	0	0	0	0	1

Location FSM Output Table			
Input	Output		
Current State	SW	D	WIN
S0 == CC	0	0	0
S1 == TT	0	0	0
S2 == RR	0	0	0
S3 == SS	1	0	0
S4 ==	0	0	0
S5 ==	0	1	0
S6 == VV	0	0	1

Sword FSM Transition Table		
Input		Output
Current State	SW	Next State
NS	1	HS
NS	0	NS
HS	X	HS

Sword FSM Truth Table				
Current State		Input	Next State	
S0	S1	SW	S0'	S1'
1	0	0	1	0
1	0	1	0	1
0	1	X	0	1

Sword FSM Output Table		
Input		Output
S0	S1	V
1	0	0
0	1	1

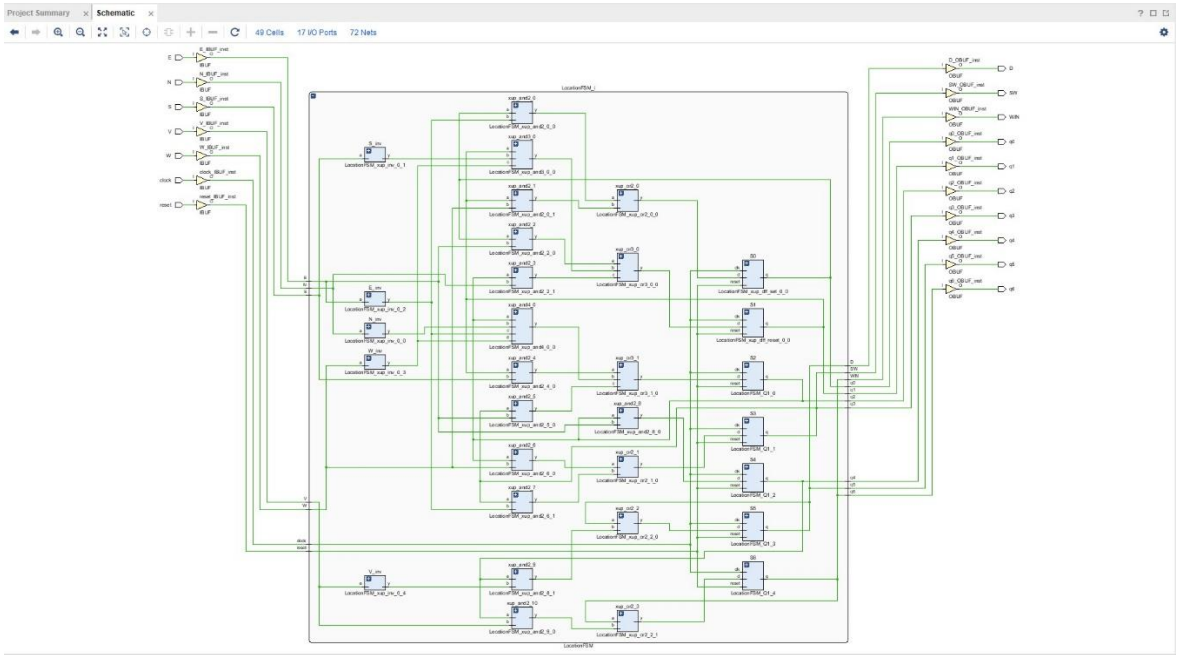
2. The Boolean expressions of the state transition and the output logics for each FSM.

Location FSM Boolean Expressions
D[0] = S0' = S_0E' + S_1W
D[1] = S1' = S_0E + S_1S'W' + S_2N
D[2] = S2' = S_1S + S_2N'E'W' + S_3E
D[3] = S3' = S_2W + S_3E'
D[4] = S4' = S_2E
D[5] = S5' = S_4V' + S_5
D[6] = S6' = S_4V + S_6

For Reference:	
	SW = S_3
	D = S_5
	WIN = S_6
	S0 = set register
	S1-6 = reset

Sword FSM Boolean Expressions
D[0] = S0' = S_0SW'
D[1] = S1' = S_0SW + S_1
V = S_0'S_1

3. A screenshot of the location FSM schematic (please expand the schematic).



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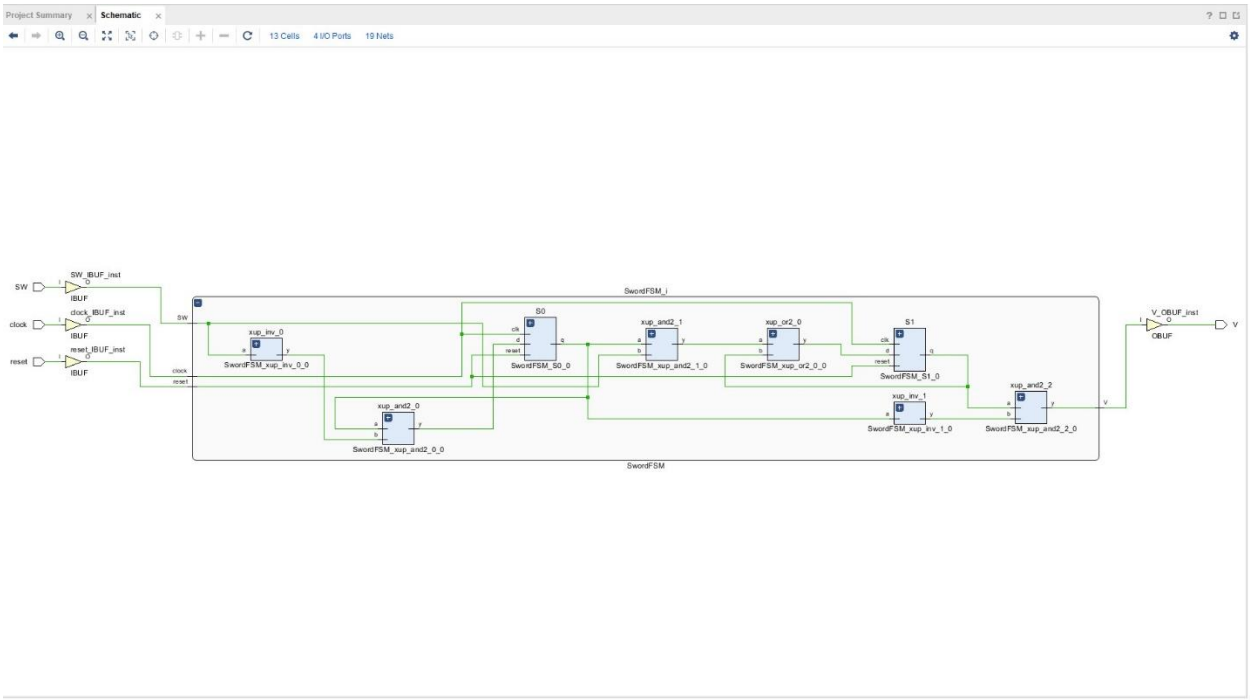
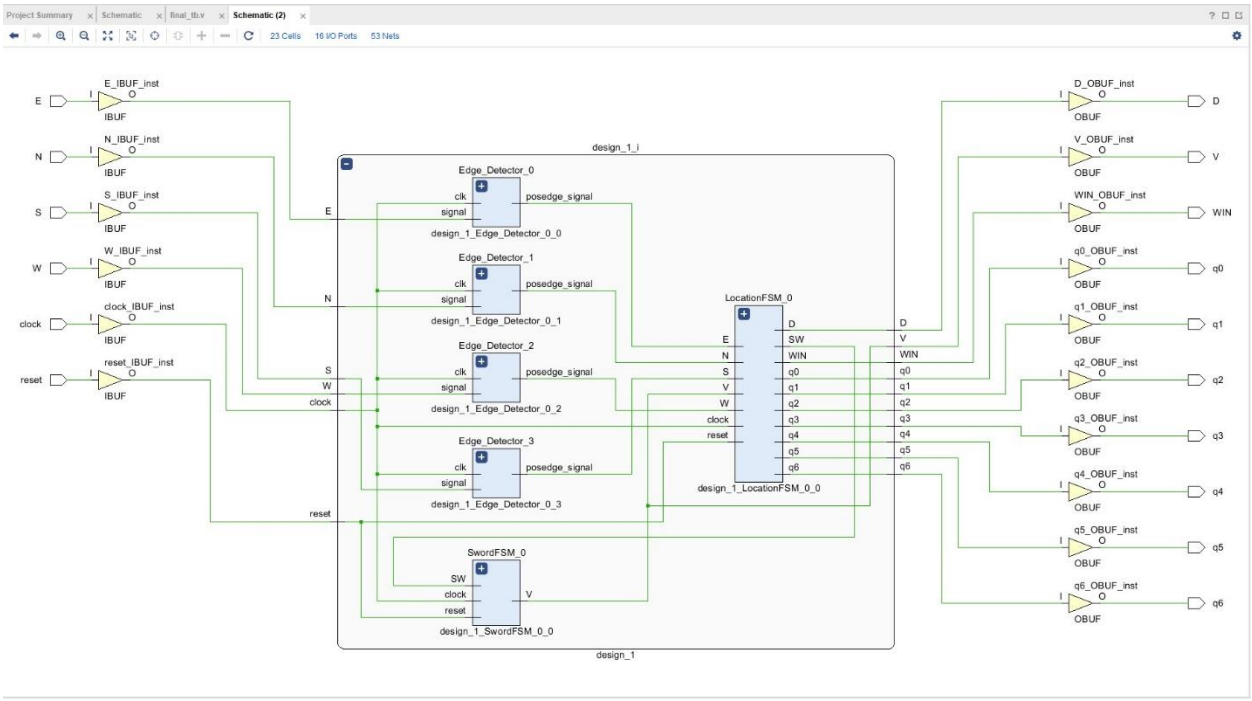
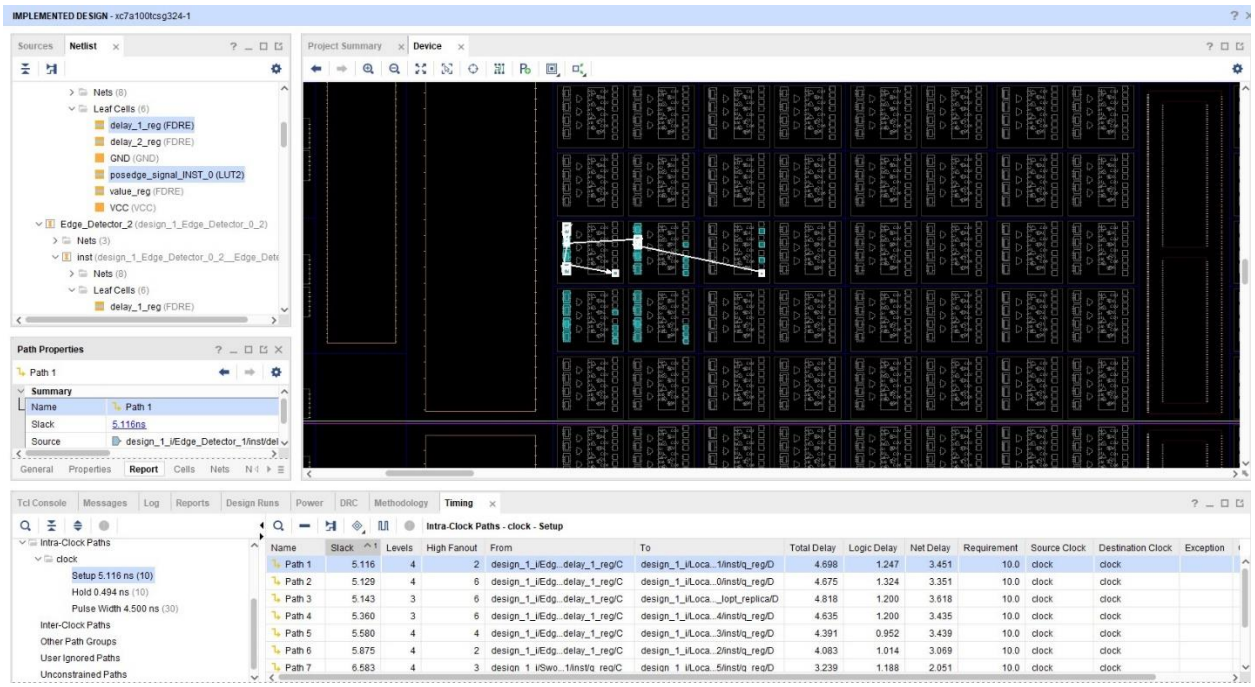
4. A screenshot of the sword FSM schematic (please expand the schematic).



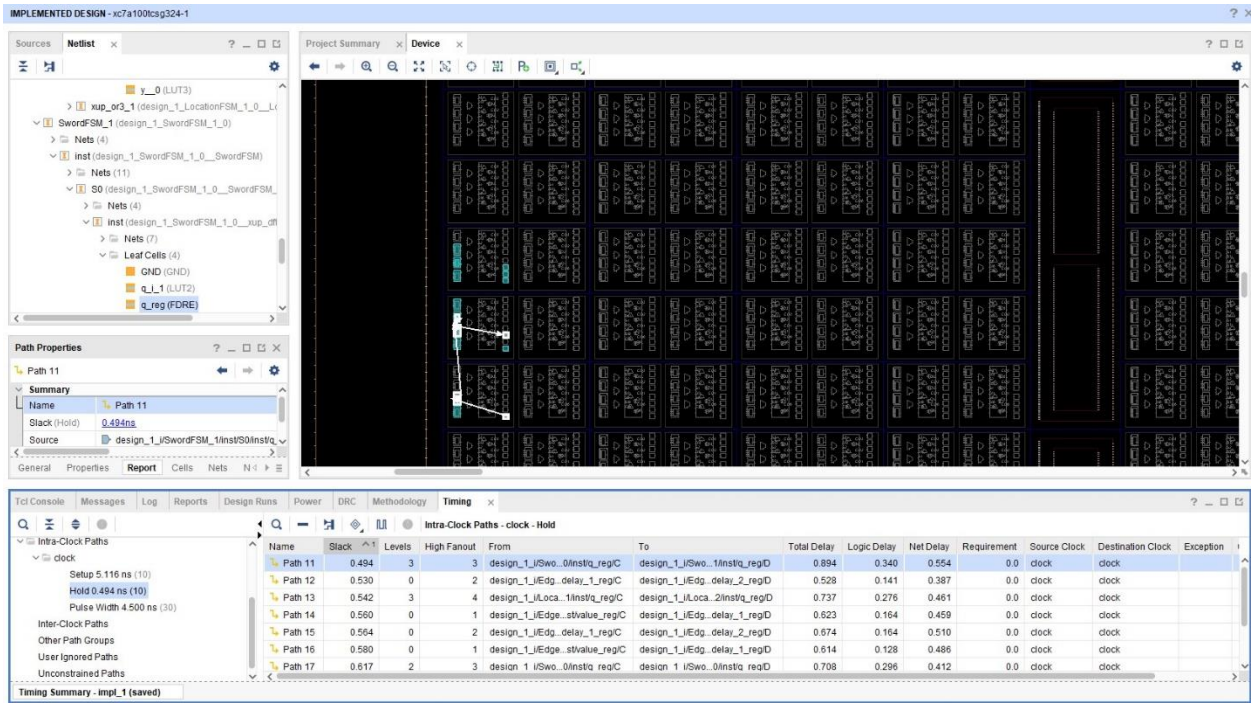
5. A screenshot of the top-level schematic of the entire system.



6. A screenshot of the post-implementation timing report showing the critical path of your design and the worst-case setup time slack.



7. A screenshot of the post-implementation timing report showing the shortest path of your design and the worst-case hold time slack.

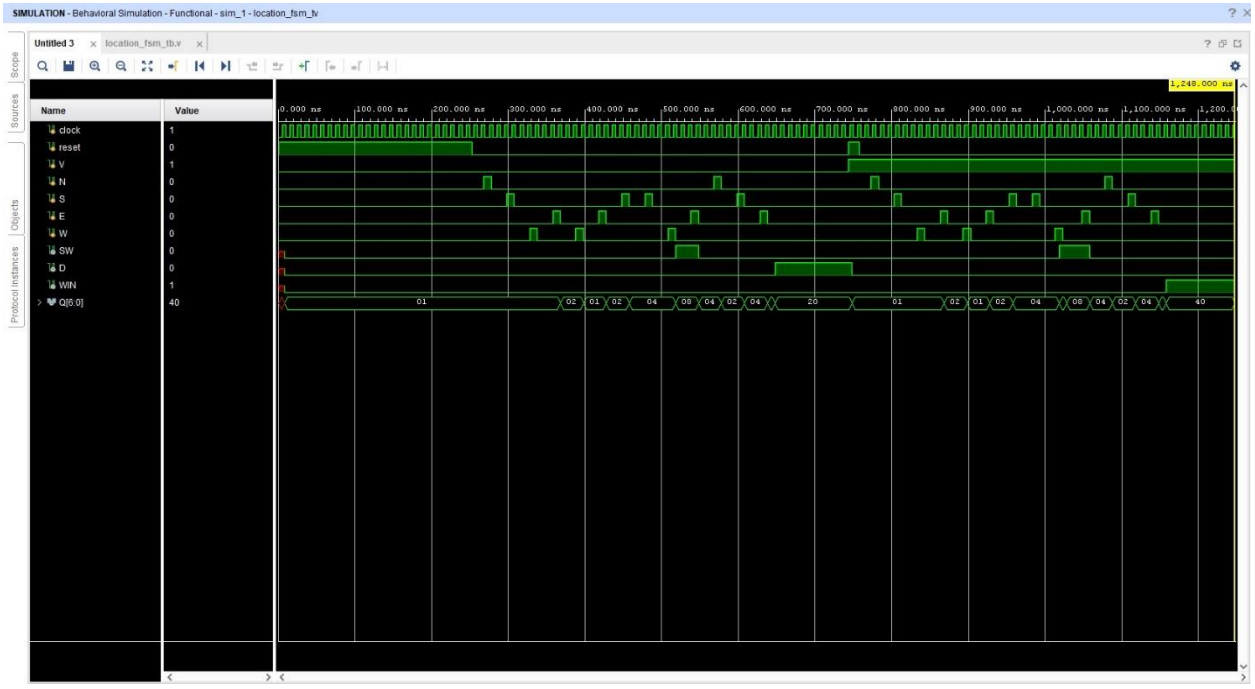


8. Answers to the above questions about timing.
    a. The worst-case setup-time is 5.116 ns, and worst-case hold-slack is 0.494 ns
    b. Since the period is set to 10 ns, I would subtract the setup-time from the period, which would equal 4.884 ns. Taking the inverse, I conclude that the highest clock speed would be 204 MHz.

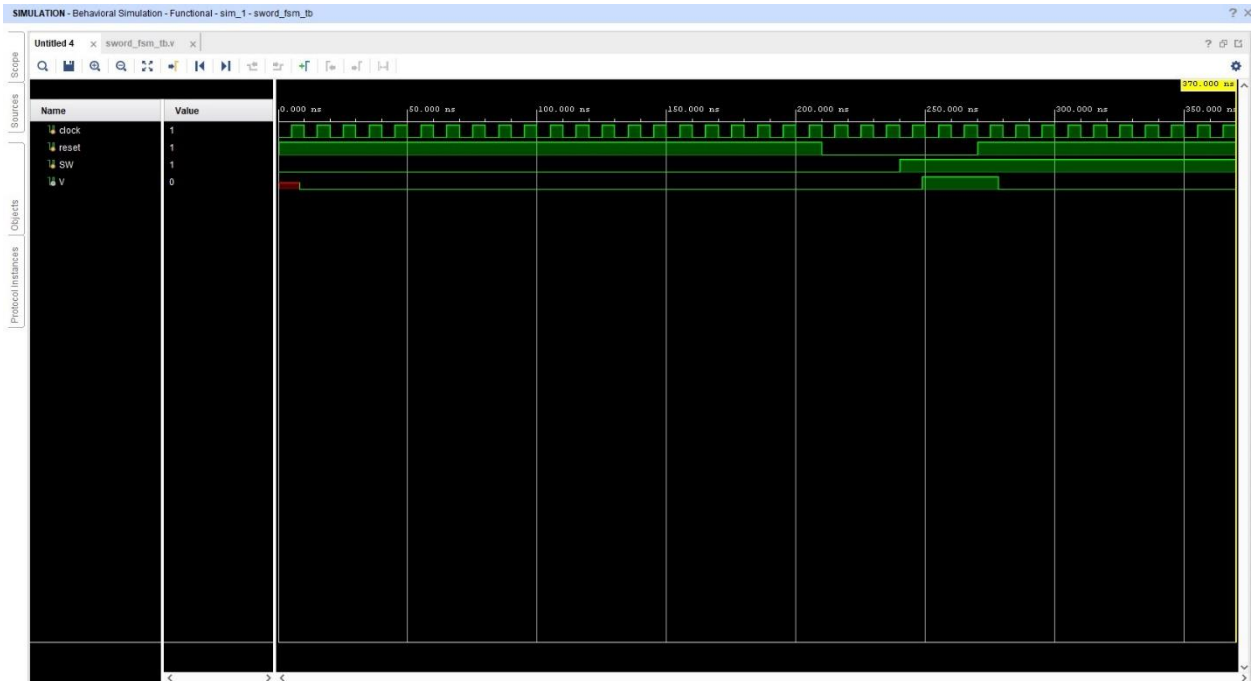
$$Max_{freq} = \frac{1}{(Actual\ period - Worst\ Negative\ Slack)}$$

c. At 5 GHz frequency, the implementation failed the timing. WNS was -2.552 ns and TNS was -37.796 ns. It would not be able to function because the slack time needs to be greater than 0, otherwise there would be no margin. The only way to fix slack time is to reduce the clock frequency.

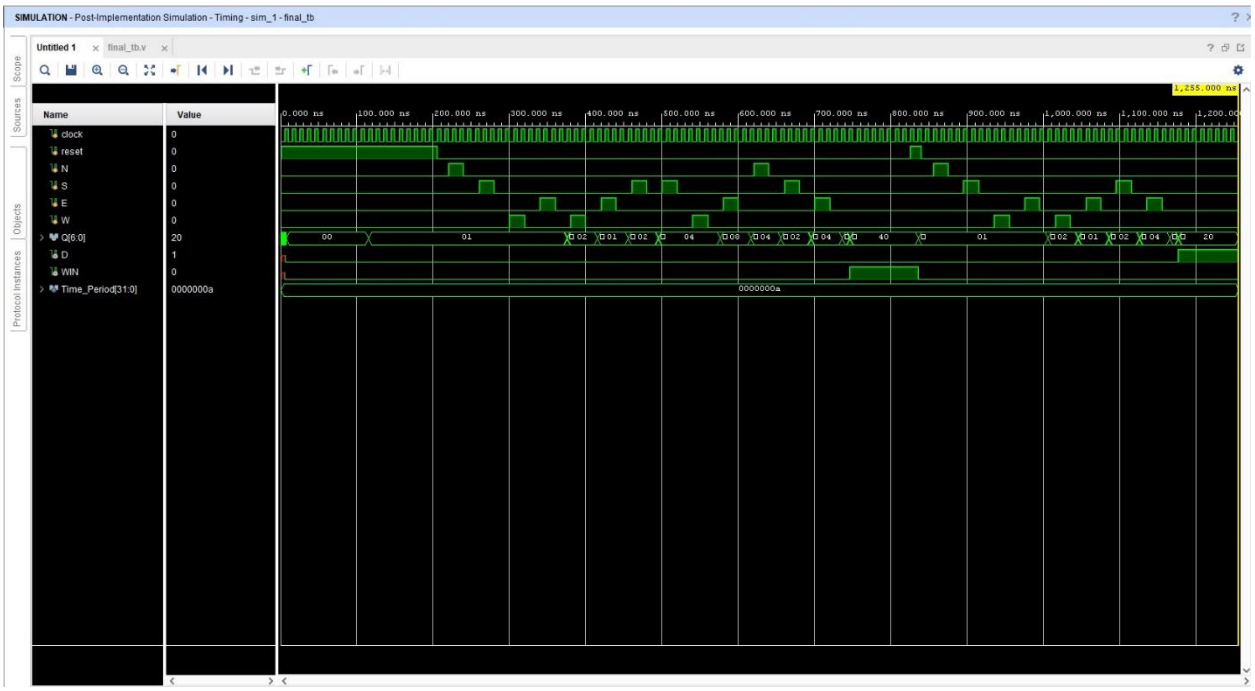
9. A screenshot of the simulation waveform of your location FSM (Location_fsm_tb.v) from behavior simulation.



10. A screenshot of the simulation waveform of your sword FSM (Sword_fsm_tb.v) from behavior simulation.



11. A screenshot of the simulation waveform of your entire system (final_tb.v) from the “Post Implementation Timing Simulation” at the clock frequency of 100MHz.



12. A screenshot of the simulation waveform of your entire system (final_tb.v) from the “Post Implementation Timing Simulation” at the clock frequency of 5GHz.