

Rockchip RK915 Datasheet

**Revision 1.1
Aug. 2021**

Table of Content

Table of Content	2
Chapter 1 Introduction	3
1.1 Overview.....	3
1.2 Features.....	3
1.3 Block Diagram	4
Chapter 2 Package information	5
2.1 Ordering Information	5
2.2 Top Marking.....	5
2.3 Dimension	5
2.4 Ball Pin Number Order	8
2.5 Power/ground IO descriptions	9
2.6 Function IO description	9
2.7 IO pin name descriptions.....	10
Chapter 3 Electrical Specification	11
3.1 Absolute Maximum Ratings.....	11
3.2 Recommended Operating Conditions.....	11
3.3 DC Characteristics	11
Warranty Disclaimer	14

Chapter 1 Introduction

1.1 Overview

RK915 is a low power WLAN connectivity chip for portable media device, which supports IEEE 802.11b/g/n.

RK915 provides a compact ultra-small form factor solution with minimal external components to drive the costs for mass volumes and allows for flexibility in size, form, and function. Taking advanced design techniques and process technology to deliver the lowest active and idle power, RK915 extends the system battery life while maintaining consistent connectivity and still provides a rich set of features.

RK915 is a very highly integrated design with internal PA, TR switch, Balun, LNA for low BOM cost. The chip is embedded with low power and low cost processor to talk with host device. With the internal processor, RK915 firmware can be flexibly developed for meeting different customer production application requirement. There are two package types for RK915, RK915A and RK915B respectively. RK915A integrates LDO for RF analog power supply, and RK915B compared with RK915A, integrates one more LDO for digital power supply.

RK915 provides the automatic hardware calibration solution to tune the RF characteristic to achieve best RF performance, which can avoid RF performance penalty causing by the hardware board differentiation.

1.2 Features

The features listed below which may or may not be present in actual product, may be subject to the third party licensing requirements. Please contact Rockchip for actual product feature configurations and licensing requirements

1.2.1 Wireless Interface

- IEEE 802.11b/g/n Radio, PHY, Baseband and LMAC
- One Transmit and one Receive path(1T1R)
- 2.4GHz band and 20MHz bandwidth
- Integrated TR switch, BALUN, LNA, and Power Amplifier
- Support STA, AP and P2P operation modes
- Support concurrent STA and P2P operation
- Security support WEP, WPA, WPA2
- Frame aggregation for increased MAC efficiency(A-MSDU,A-MPDU) and Low latency immediate High-Throughput Block Acknowledgement
- Intelligent power control, including 802.11 power save mode
- Dynamic power management based on packet signal quality
- DSSS with DBPSK and DQPSK,CCK modulation
- OFDM with BPSK, QPSK, 16QAM and 64QAM modulation. Convolutional Coding Rate:1/2, 2/3, 3/4 and 5/6
- Maximum data rate 11Mbps for 802.11b, 54Mbps for 802.11g and 65Mbps for 802.11n
- Fast receiver Automatic Gain Control(AGC)

1.2.2 SDIO interface

- Compliant with SDIO Specification Version 3.00
- Support 4bit data bus width
- Support 2 Functions
- Support DMA operation for high speed data transfer
- Support Dual-Buffer mode to optimize throughput

1.2.3 Others

- Embedded power regulator for BOM cost save and high power utilization efficiency
- Embedded RTC OSC for low power mode working
- With large enough buffer to reach high TX and RX data throughput, which make sure

better user experience

- Package Type:
 - RK915A: QFN40(body: 5mmx5mm)
 - RK915B: QFN32(body: 4mmx4mm)

1.3 Block Diagram

The following diagram shows the basic block diagram.

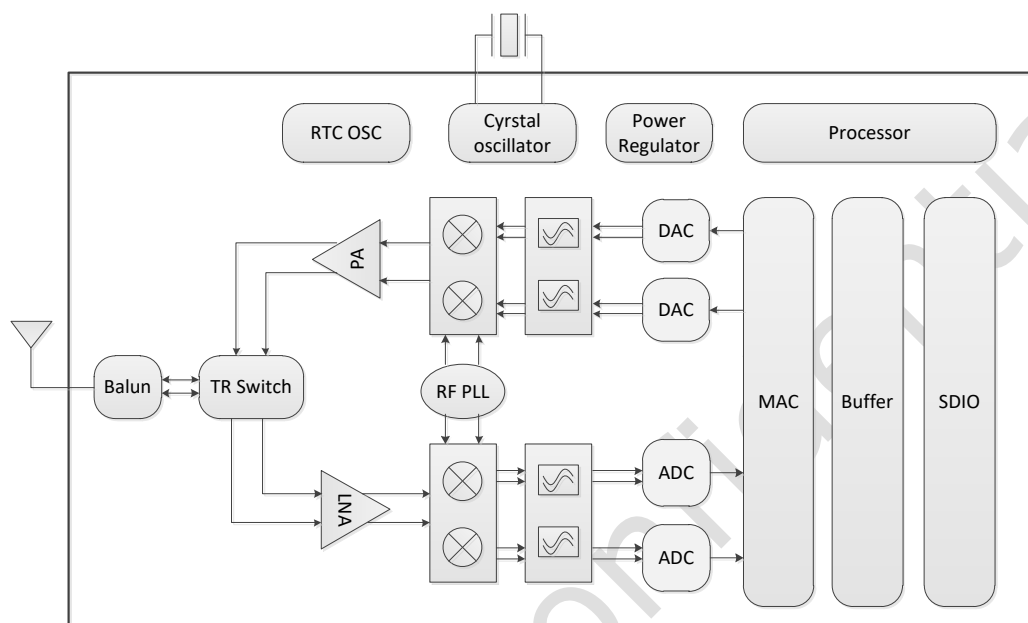


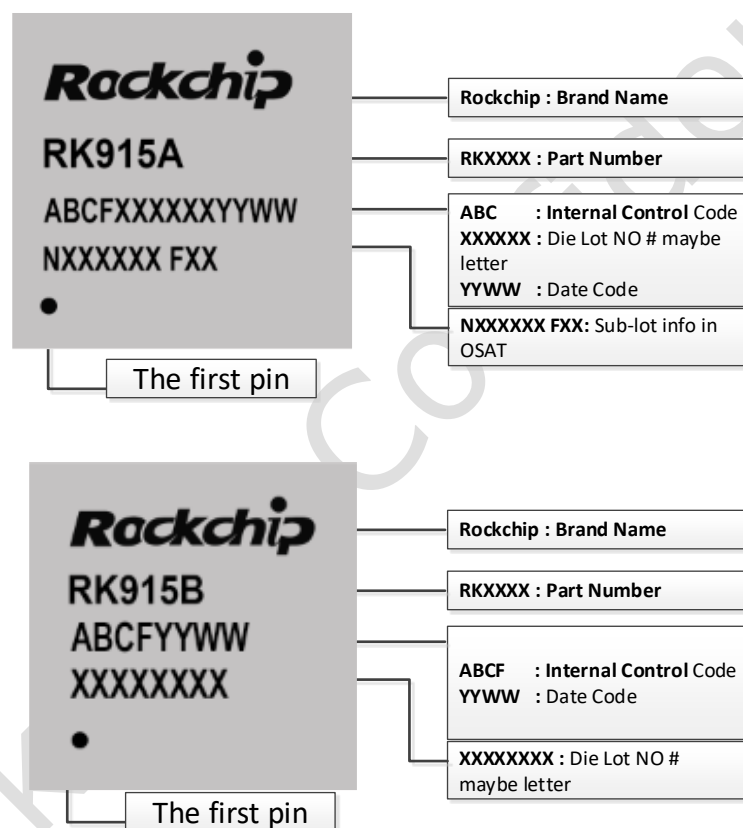
Fig. 1-1 Block Diagram

Chapter 2 Package information

2.1 Ordering Information

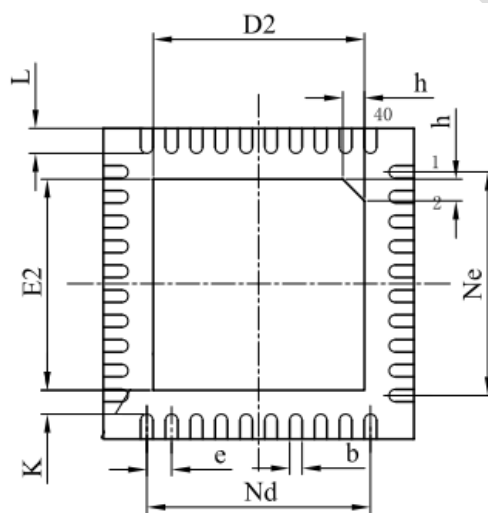
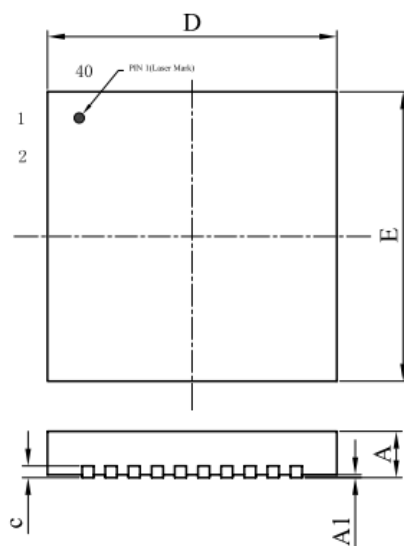
Orderable Device	RoHS status	Package	Package QTY	Device Feature
RK915A	RoHS	QFN40L(5X5)	5000pcs by tape	WLAN Chip support IEEE 802.11b/g/n
RK915B	RoHS	QFN32L(4X4)	5000pcs by tape	WLAN Chip support IEEE 802.11b/g/n

2.2 Top Marking



2.3 Dimension

- RK915A



► Fig. 2-2 Package Bottom View

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	—	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	4.90	5.00	5.10
D2	3.30	3.40	3.50
e	0.40BSC		
Nd	3.60BSC		
E	4.90	5.00	5.10
E2	3.30	3.40	3.50
Ne	3.60BSC		
L	0.35	0.40	0.45
K	0.20	—	—
h	0.30	0.35	0.40

Fig. 2-3 Package Dimension

- RK915B

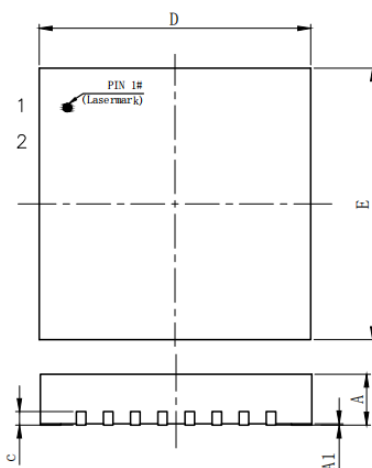


Fig. 2-4 Package Top and Side View

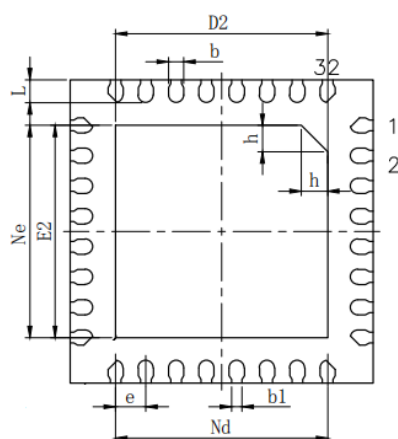


Fig. 2-5 Package Bottom View

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.15	0.20	0.25
b1	0.14REF		
c	0.18	0.20	0.25
D	3.90	4.00	4.10
D2	2.70	2.80	2.90
e	0.40BSC		
Ne	2.80BSC		
Nd	2.80BSC		
E	3.90	4.00	4.10
E2	2.70	2.80	2.90
L	0.25	0.30	0.35
h	0.30	0.35	0.40

Fig. 2-6 Package Dimension

2.4 Ball Pin Number Order

Table 2-1 RK915A Ball Pin Number Order Information

Pin	Pin Name	Pin	Pin Name
1	SDIO_CLK	21	NC_1
2	SDIO_CMD	22	NC_2
3	SDIO_D0	23	NC_3
4	VSS_0	24	NC_4
5	SDIO_D1/GPIO0_A3	25	RF_VDD_1V8_0
6	SDIO_D2/GPIO0_A4	26	VSS_4
7	VSS_1	27	XIN
8	SDIO_D3/GPIO0_A5	28	XOUT
9	CLK32K	29	VSS_5
10	VDD_1V1_0	30	NC_5
11	VDDIO	31	RF_VDD_1V8_1
12	VDD_1V1_1	32	REFRES
13	WL_HOST_WAKE/GPIO0_A7	33	NC_6
14	VSS_2	34	RF_VDD_1V8_2
15	GPIO0_B0	35	VSS_6
16	UART_TX/GPIO0_B1	36	RFIO
17	GPIO0_B2	37	VSS_7
18	VSS_3	38	RF_VDD_3V3
19	NC_0	39	LDO_IN_3V3
20	WL_REG_ON	40	LDO_OUT_1V8

Table 2-2 RK915B Ball Pin Number Order Information

Pin	Pin Name	Pin	Pin Name
1	LDO_IN_3V3	17	NC
2	SDIO_CLK	18	WL_REG_ON
3	SDIO_CMD	19	RF_VDD_1V8_0
4	VSS_0	20	VSS_1
5	SDIO_D0	21	RF_VDD_1V8_1
6	SDIO_D1/GPIO0_A3	22	XIN
7	SDIO_D2/GPIO0_A4	23	XOUT
8	SDIO_D3/GPIO0_A5	24	RF_VDD_1V8_2
9	CLK32K	25	REFRES
10	VDD_1V1_0	26	RF_VDD_1V8_3
11	VDDIO	27	VSS_2
12	VDD_1V1_1	28	RFIO
13	WL_HOST_WAKE /GPIO0_A7	29	VSS_3
14	GPIO0_B0	30	RF_VDD_3V3
15	UART_TX/GPIO0_B1	31	LDO1_OUT_1V8
16	GPIO0_B2	32	LDO2_OUT_1V1

2.5 Power/ground IO descriptions

Table 2-3 RK915A Power/Ground IO information

Group	Pin#	Descriptions
VSS	4,7,14,18,26,29,35,37,Exposed-GND	Ground
VDD_1V1	10,12	Logic Power
VDDIO	11	GPIO Power
RF_VDD_1V8	25,31,34	RF Analog Power
RF_VDD_3V3	38	RF Analog Power
LDO_IN_3V3	39	LDO Analog Power

Table 2-4 RK915B Power/Ground IO information

Group	Pin#	Descriptions
VSS	4,20,27,29,Exposed-GND	Ground
VDD_1V1	10,12	Logic Power
VDDIO	11	GPIO Power
RF_VDD_1V8	19,21,24,26	RF Analog Power
RF_VDD_3V3	30	RF Analog Power
LDO_IN_3V3	1	LDO Analog Power

2.6 Function IO description

Table 2-5 RK915A Function IO description

pin name	Pin#	Func1	Func2	Pad Type®	Drive Strength	Pull□	Power Supply□
SDIO_CLK	1	SDIO_CLK		I/O	8mA	up	VDDIO
SDIO_CMD	2	SDIO_CMD		I/O	8mA	up	
SDIO_D0	3	SDIO_D0		I/O	8mA	up	
SDIO_D1/GPIO0_A3	5	GPIO0_A3	SDIO_D1	I/O	8mA	up	
SDIO_D2/GPIO0_A4	6	GPIO0_A4	SDIO_D2	I/O	8mA	up	
SDIO_D3/GPIO0_A5	8	GPIO0_A5	SDIO_D3	I/O	8mA	up	
CLK32K	9	CLK32K		I/O	8mA	up	
WL_HOST_WAKE /GPIO0_A7	13	GPIO0_A7	WL_HOST_WAKE	I/O	8mA	down	
GPIO0_B0	15	GPIO0_B0		I/O	8mA	down	
UART_TX/GPIO0_B1	16	GPIO0_B1	UART_TX	I/O	8mA	down	
GPIO0_B2	17	GPIO0_B2		I/O	8mA	down	
WL_REG_ON	20	WL_REG_ON		I	8mA	up	RF_VDD_1V8
XIN	27			A	NA	NA	
XOUT	28			A	NA	NA	
REFRES	32			A	NA	NA	
RFIO	36			A	NA	NA	RF_VDD_3V3

Table 2-6 RK915B Function IO description

pin name	Pin#	Func1	Func2	Pad Type①	Drive Strength	Pull③	Power Supply②
SDIO_CLK	2	SDIO_CLK		I/O	8mA	up	VDDIO
SDIO_CMD	3	SDIO_CMD		I/O	8mA	up	
SDIO_D0	5	SDIO_D0		I/O	8mA	up	
SDIO_D1/GPIO0_A3	6	GPIO0_A3	SDIO_D1	I/O	8mA	up	
SDIO_D2/GPIO0_A4	7	GPIO0_A4	SDIO_D2	I/O	8mA	up	
SDIO_D3/GPIO0_A5	8	GPIO0_A5	SDIO_D3	I/O	8mA	up	
CLK32K	9	CLK32K		I/O	8mA	up	
WL_HOST_WAKE /GPIO0_A7	13	GPIO0_A7	WL_HOST_WAKE	I/O	8mA	down	
GPIO0_B0	14	GPIO0_B0		I/O	8mA	down	
UART_TX/GPIO0_B1	15	GPIO0_B1	UART_TX	I/O	8mA	down	
GPIO0_B2	16	GPIO0_B2		I/O	8mA	down	
WL_REG_ON	18	WL_REG_ON		I	8mA	up	RF_VDD_1V8
XIN	22			A	NA	NA	
XOUT	23			A	NA	NA	
REFRES	25			A	NA	NA	
RFIO	28			A	NA	NA	RF_VDD_3V3

Notes :

①: Pad types : I = input , O = output , I/O = input/output (bidirectional) ,

AP = Analog Power , AG = Analog Ground

DP = Digital Power , DG = Digital Ground

A = Analog

②: Power supply means that all the related IOs are in this IO power domain.

③: The pull up/pull down is configurable

2.7 IO pin name descriptions

This sub-chapter will focus on the detailed function description of every pins based on different interface.

Table 2-7 RK915 IO Function Description List

Interface	Pin Name	Direction	Description
MISC	XIN	I	Clock input of 40MHz crystal
	XOUT	O	Clock output of 40MHz crystal
	WL_REG_ON	I	Chip hardware reset
	CLK32K	I	Chip sleep clock input
	WL_HOST_WAKE	O	Chip interrupt output to host

Interface	Pin Name	Direction	Description
SDIO	SDIO_CLK	I	sdio clock
	SDIO_CMD	I/O	sdio command input and response output
	SDIO_D <i>i</i> (<i>i</i> =0~3)	I/O	sdio data input and output

Interface	Pin Name	Direction	Description
UART	UART_TX	O	uart searial data output

Chapter 3 Electrical Specification

3.1 Absolute Maximum Ratings

The below table provides the absolute ratings. Absolute maximum ratings specify the values beyond which the device may be damaged permanently. Long-term exposure to absolute maximum ratings conditions may affect device reliability.

Table 3-1 RK915 Absolute Maximum Ratings

Parameters	Related Power Group	Max	Unit
DC supply voltage for internal digital logic	VDD_1V1	1.21	V
DC supply voltage for digital GPIO@3.3V mode	VDDIO	3.63	V
DC supply voltage for digital GPIO@1.8V mode	VDDIO	1.98	V
DC supply voltage for RF_VDD_3V3	RF_VDD_3V3	3.63	V
DC supply voltage for RF_VDD_1V8	RF_VDD_1V8	1.98	V
DC supply voltage for LDO_IN_3V3	LDO_IN_3V3	3.63	V
Storage Temperature	Tstg	125	°C
Max Conjunction Temperature	Tj	125	°C

3.2 Recommended Operating Conditions

Following table describes the recommended operating condition.

Table 3-2 RK915 Recommended Operating Condition

Parameters	Symbol	Min	Typ	Max	Unit
DC supply voltage for internal digital logic	VDD_1V1	0.99	1.10	1.21	V
DC supply voltage for digital GPIO@3.3V mode	VDDIO	2.97	3.30	3.63	V
DC supply voltage for digital GPIO@1.8V mode	VDDIO	1.62	1.80	1.98	V
DC supply voltage for RF_VDD_3V3	RF_VDD_3V3	2.97	3.30	3.63	V
DC supply voltage for RF_VDD_1V8	RF_VDD_1V8	1.62	1.80	1.98	V
DC supply voltage for LDO_IN_3V3	LDO_IN_3V3	2.97	3.30	3.63	V
Operating Temperature		-20	25	85	°C

3.3 DC Characteristics

Table 3-3 RK915 DC Characteristics

Parameters	Symbol	Min	Typ	Max	Units
Digital GPIO @3.3V mode	Input Low Voltage	Vil	-0.3	NA	0.8 V
	Input High Voltage	Vih	2.0	NA	3.6 V
	Output Low Voltage	Vol	NA	NA	0.4 V
	Output High Voltage	Voh	2.4	NA	V
	Pullup Resistor	Rpu	27	40	65 Kohm
	Pulldown Resistor	Rpd	31	47	83 Kohm

Parameters	Symbol	Min	Typ	Max	Units
Digital GPIO @1.8V mode	Input Low Voltage	Vil	-0.3	NA	0.63 V
	Input High Voltage	Vih	1.2	NA	2.1 V

Parameters		Symbol	Min	Typ	Max	Units
	Output Low Voltage	Vol	NA	NA	0.45	V
	Output High Voltage	Voh	1.35	NA	NA	V
	Pullup Resistor	Rpu	53	90	167	Kohm
	Pulldown Resistor	Rpd	54	99	202	Kohm

Revision History

Date	Revision	Description
2021-8-31	1.1	Update the package QTY
2021-4-13	1.0	Initial Release

Warranty Disclaimer

Rockchip Electronics Co., Ltd makes no warranty, representation or guarantee (expressed, implied, statutory, or otherwise) by or with respect to anything in this document, and shall not be liable for any implied warranties of non-infringement, merchantability or fitness for a particular purpose or for any indirect, special or consequential damages.

Information furnished is believed to be accurate and reliable. However, Rockchip Electronics Co., Ltd assumes no responsibility for the consequences of use of such information or for any infringement of patents or other rights of third parties that may result from its use.

Rockchip Electronics Co., Ltd.'s products are not designed, intended, or authorized for using as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Rockchip Electronics Co., Ltd.'s product could create a situation where personal injury or death may occur, should buyer purchase or use Rockchip Electronics Co., Ltd.'s products for any such unintended or unauthorized application, buyers shall indemnify and hold Rockchip Electronics Co., Ltd and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, expenses, and reasonable attorney fees arising out of, either directly or indirectly, any claim of personal injury or death that may be associated with such unintended or unauthorized use, even if such claim alleges that Rockchip Electronics Co., Ltd was negligent regarding the design or manufacture of the part.

Copyright and Patent Right

Information in this document is provided solely to enable system and software implementers to use Rockchip Electronics Co., Ltd 's products. There are no expressed or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

Rockchip Electronics Co., Ltd does not convey any license under its patent rights nor the rights of others.

All copyright and patent rights referenced in this document belong to their respective owners and shall be subject to corresponding copyright and patent licensing requirements.

Trademarks

Rockchip and Rockchip™ logo and the name of Rockchip Electronics Co., Ltd.'s products are trademarks of Rockchip Electronics Co., Ltd. and are exclusively owned by Rockchip Electronics Co., Ltd. References to other companies and their products use trademarks owned by the respective companies and are for reference purpose only.

Confidentiality

The information contained herein (including any attachments) is confidential. The recipient hereby acknowledges the confidentiality of this document, and except for the specific purpose, this document shall not be disclosed to any third party.

Reverse engineering or disassembly is prohibited.

ROCKCHIP ELECTRONICS CO., LTD. RESERVES THE RIGHT TO MAKE CHANGES IN ITS PRODUCTS OR PRODUCT SPECIFICATIONS WITH THE INTENT TO IMPROVE FUNCTION OR DESIGN AT ANY TIME AND WITHOUT NOTICE AND IS NOT REQUIRED TO UNDATE THIS DOCUMENTATION TO REFLECT SUCH CHANGES.

Copyright © 2021 Rockchip Electronics Co., Ltd.

All rights reserved. No part of this publication may be reproduced, stored in a retrieval system, or transmitted in any form or by any means, electric or mechanical, by photocopying, recording, or otherwise, without the prior written consent of Rockchip Electronics Co., Ltd.