University of Victoria
Department of Computer Science
COMPUTER SCIENCE 355

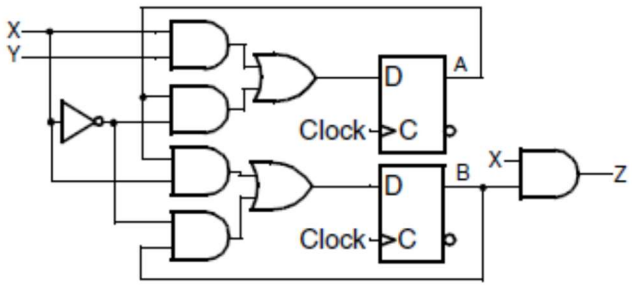
Fall 2023- ASSIGNMENT 2
Due Thursday, November 9, 2023 by 11:59PM on Brightspace

Show all the steps in your work to receive marks; the final solution only will not get credit.

1. [6 marks] A sequential circuit with two *D* flip-flops *A* and *B*, two inputs *X* and *Y*, and one output *Z* is specified by the following input equations:

$$D_A = \bar{X}A + XY, D_B = \bar{X}B + XA, Z = XB$$

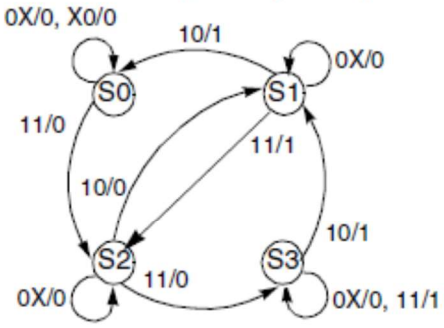
   a. Draw the logic diagram of the circuit.
   b. Derive the state table.
   c. Derive the state diagram.



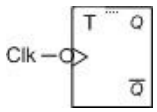
Present state		Inputs		Next state		Output
A	*B*	*X*	*Y*	*A*	*B*	*Z*
0	0	0	0	0	0	0
0	0	0	1	0	0	0
0	0	1	0	0	0	0
0	0	1	1	1	0	0
0	1	0	0	0	1	0
0	1	0	1	0	1	0
0	1	1	0	0	0	1
0	1	1	1	1	0	1
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	0	1	0
1	0	1	1	1	1	0
1	1	0	0	1	1	0
1	1	0	1	1	1	0
1	1	1	0	0	1	1
1	1	1	1	1	1	1

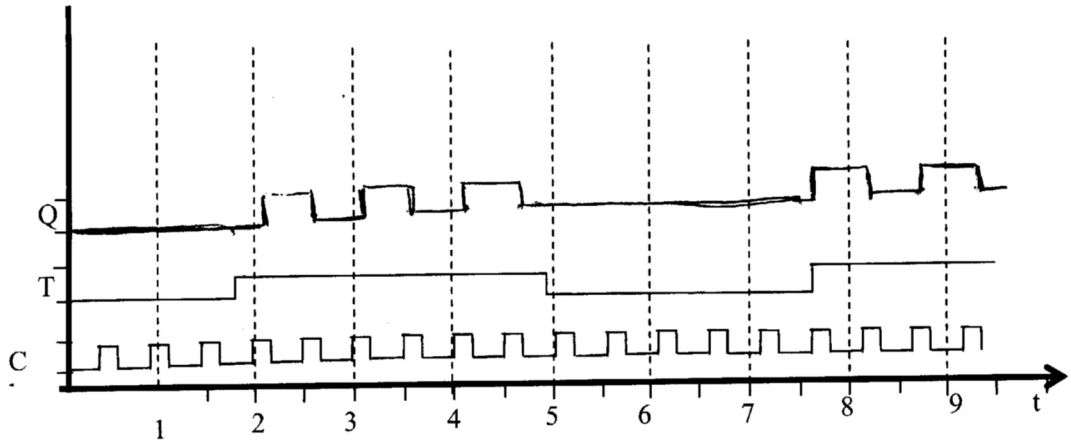
S0 - 00
S1 - 01
S2 - 10
S3 - 11

Format: XY/Z (X = unspecified)



2. [4 marks] For a T Flip Flop, the inputs, T and Clk are as given in the timing diagram below. Complete the timing diagram by drawing the Q output.





T-Flip Flop $Q^+ = \bar{T}Q + T\bar{Q} = T \oplus Q$

T	Q	Q^+
0	0	0
0	1	1
1	0	1
1	1	0

3. [6 marks] A combinational circuit is defined by the following two Boolean functions:

$$F_1 = \overline{X + Z} + XYZ$$
$$F_2 = \overline{X + Z} + \bar{X}YZ$$

a. Design the circuit with a decoder and external OR gates
b. Design the circuit with multiplexers. Choose the right size multiplexer.

$F_1 = \overline{x+z} + xyz = \bar{x}\bar{z} + xyz = \bar{x}\bar{z}\cdot(y+\bar{y}) + xyz$

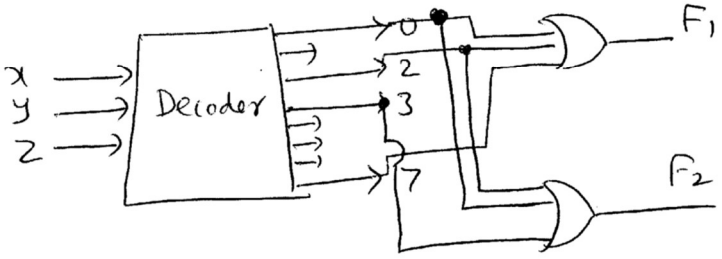
$= \bar{x}y\bar{z} + \bar{x}\bar{y}\bar{z} + xyz$

$010 \quad 000 \quad 111$

$F_2 = \overline{x+z} + \bar{x}yz = \bar{x}y\bar{z} + \bar{x}\bar{y}\bar{z} + \bar{x}yz$

$010 \quad 000 \quad 011$

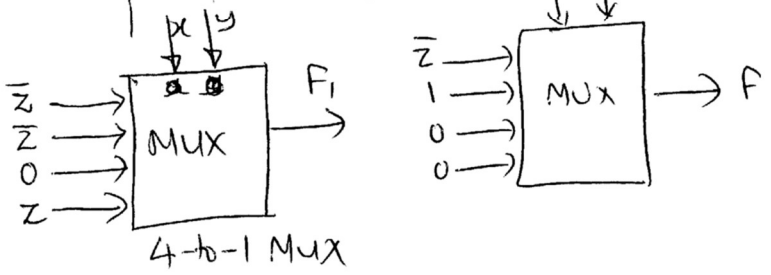
a)



b)

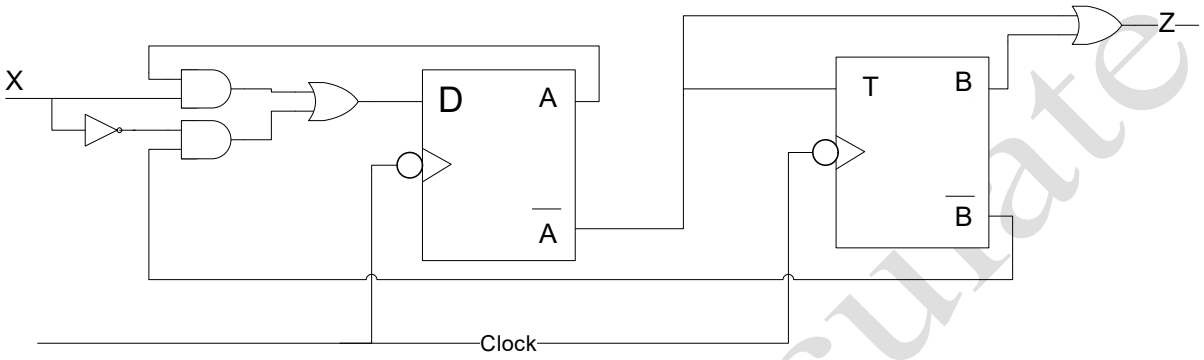
x	y	z	i	F_1		F_2	
0	0	0	0	1	$=\bar{z}$	1	$=\bar{z}$
0	0	1	1	0		0	
0	1	0	2	1	$=\bar{z}$	1	$=1$
0	1	1	3	0		1	
1	0	0	4	0	$=0$	0	$=0$
1	0	1	5	0		0	
1	1	0	6	0	$=z$	0	$=0$
1	1	1	7	1		0	

n variable
(n-1) bit select
$2^{(n-1)}$ line Mux



4. [4 marks] For the following JK flip flop, complete the timing diagram.

5. [6 Marks] For the following circuit with input X and output Z, draw a state diagram describing its behaviour:



1) Input/~~output~~ equations for FF

For A: $D_A = XA + \bar{X}\bar{B}$

For B: $T_B = \bar{A}$

o/p equation

$Z = B + \bar{A}$ Independent of X

2) Next State equations

$A^+ = D_A = XA + \bar{X}\bar{B}$

$B^+ = \bar{T}_B \cdot B + T_B \cdot \bar{B} = AB + \bar{A}\bar{B}$

3) Next State Maps

X \ AB	00	01	11	10
0	1	1		1
1			1	1

A^+

X \ AB	00	01	11	10
0	1		1	
1	1		1	

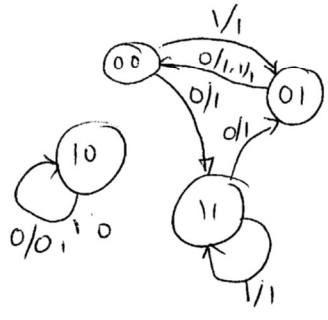
B^+

X \ AB	00	01	11	10
0	1	1	1	
1	1	1	1	

Z

4) State Table from Maps

A	B	Next State X=0 A^+	B^+	Next State X=1 A^+	B^+	Z output X=0	X=1
0	0	1	1	0	1	1	1
0	1	0	0	0	0	1	1
1	1	0	1	1	1	1	1
1	0	1	0	1	0	0	0



6. [6 marks] Design a counter that goes through the sequence:

   1 4 3 5 2 7 and repeat

   using a D flip flop for *A*, a JK flip flop for *B*, and a T flip flop for *C*. Use bit *A* as the least significant bit (LSB) and *C* as the most significant bit (MSB).

7. [6 marks] A Universal Serial Bus (USB) communication link requires a circuit that produces the sequence 00000001. You are to design a synchronous sequential circuit that starts producing this sequence for input *E* = 1. Once the sequence starts, it completes. If *E* = 1, during the last output in the sequence, the sequence repeats. Otherwise, if *E* = 0, the output remains constant at 1.
   (a) Draw the state diagram for the circuit.
   (b) Find the state table and make a state assignment.
   (c) Design the circuit using *D* flip-flops and logic gates. A reset should be included to place the circuit in the appropriate initial state at which *E* is examined to determine if the sequence of constant 1s is to be produced.

Present state	Next State For Input		Output
$D_2D_1D_0$	E=0	E=1	Z
000	001	001	0
001	010	010	0
010	011	011	0
011	100	100	0
100	101	101	0
101	110	110	0
110	111	111	0
111	111	000	1

The state assignment could be different. E. g., state 7 could be 000 with state 0 001. This would permit use of R inputs on the D flip-flops for RESET.