



# ASIC教材

## Chapter9 SOC DRC&LVS

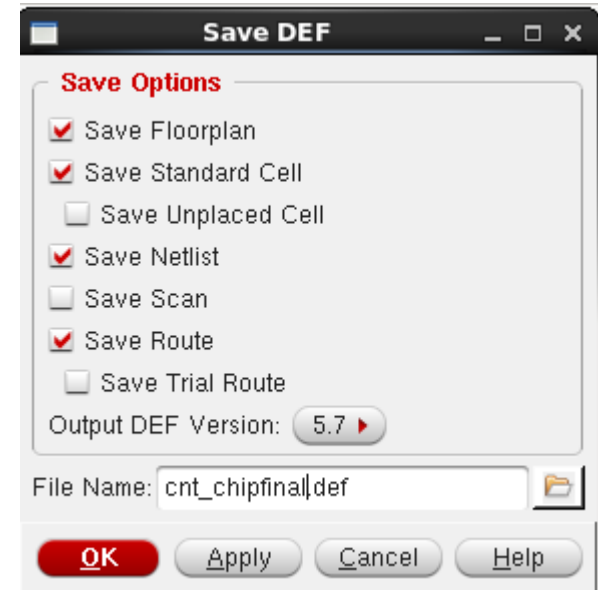
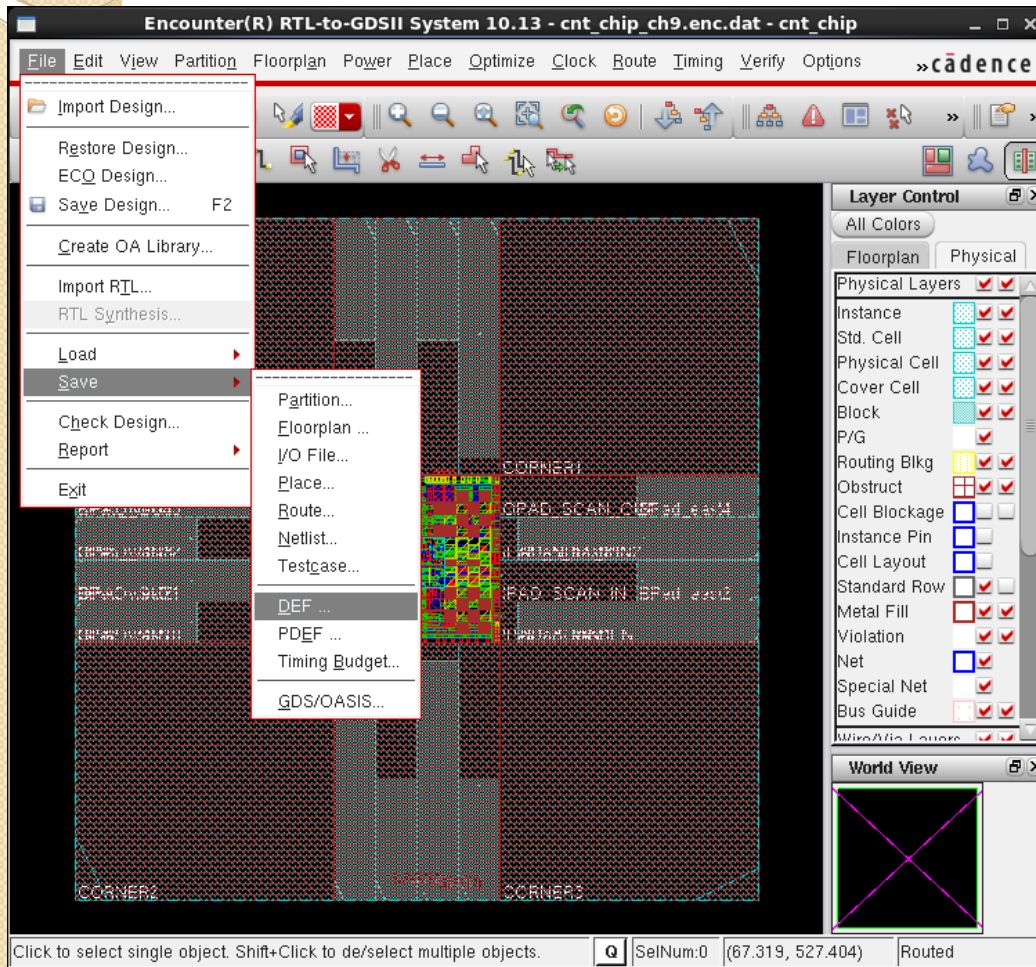
高雄第一科技大學 電子工程系  
B510實驗室

# 目錄

- Add Bonding Pad
- Stream Out GDS
- DRC&LVS

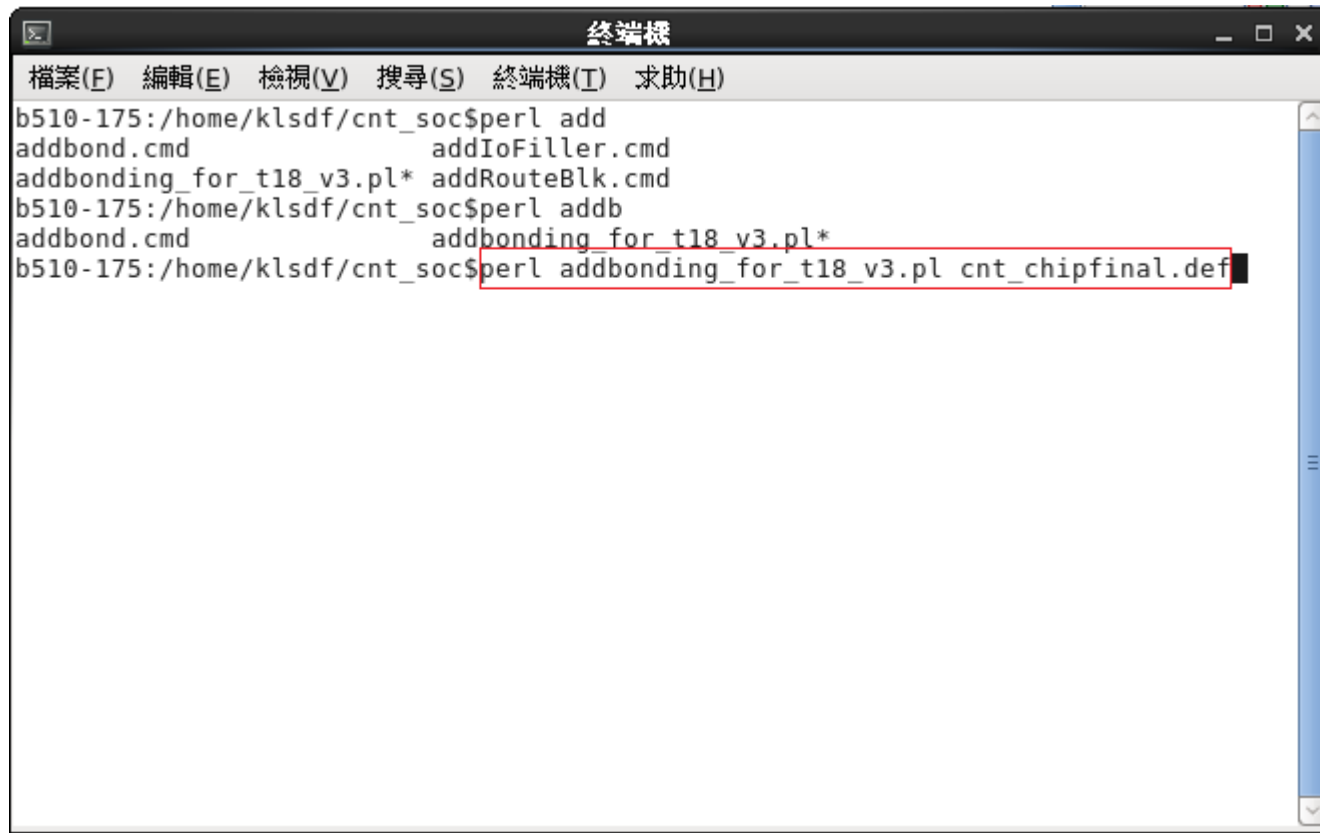
# Add Bonding Pad

- 儲存最後的DEF資訊，加入final區別。



# Add Bonding Pad

- 重新計算Bonding資訊



A terminal window titled "終端機" (Terminal) with a menu bar containing "檔案(F)", "編輯(E)", "檢視(V)", "搜尋(S)", "終端機(T)", and "求助(H)". The terminal shows the following commands and their outputs:

```
b510-175:/home/kl sdf/cnt_soc$perl add
addbond.cmd          addIoFiller.cmd
addbonding_for_t18_v3.pl* addRouteBlk.cmd
b510-175:/home/kl sdf/cnt_soc$perl addb
addbond.cmd          addbonding_for_t18_v3.pl*
b510-175:/home/kl sdf/cnt_soc$perl addbonding_for_t18_v3.pl cnt_chipfinal.def
```

The last command is highlighted with a red box.

# Add Bonding Pad

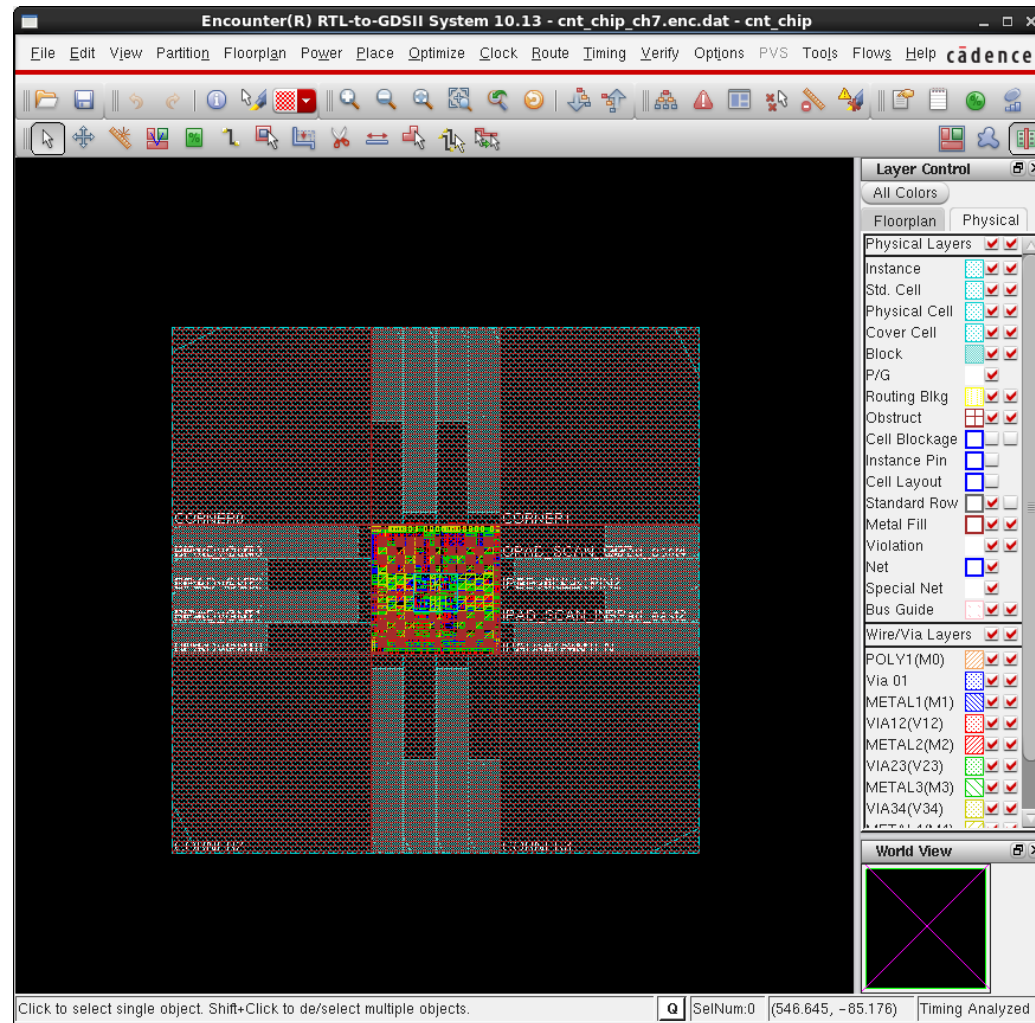
- Encounter 打入 source addbond.cmd



```
#####
# Design Stage: PostRoute
# Design Mode: 90nm
# Analysis Mode: MMMC non-OCV
# Extraction Mode: detail/spef
# Delay Calculation Options: engine=default signOff=true SIAware=false(opt)
# Switching Delay Calculation Engine to feDC
#####
#
Topological Sorting (CPU = 0:00:00.0, MEM = 365.7M, InitMEM = 365.7M)
Start delay calculation (mem=365.695M)...
delayCal using detail RC...
Delay calculation completed. (cpu=0:00:00.0 real=0:00:00.0 mem=365.695M 0)
Topological Sorting (CPU = 0:00:00.0, MEM = 365.7M, InitMEM = 365.7M)
Start delay calculation (mem=365.695M)...
delayCal using detail RC...
Delay calculation completed. (cpu=0:00:00.0 real=0:00:00.0 mem=365.695M 0)
*** CDM Built up (cpu=0:00:00.0 real=0:00:00.0 mem= 365.7M) ***
encounter 2> Writing DEF file 'cnt_chipfinal.def', current time is Wed Dec 26 18
:29:26 2012 ...
unitPerMicron=2000, dbgMicronPerDBU=0.000500, unitPerDBU=1.000000
DEF file 'cnt_chipfinal.def' is written, current time is Wed Dec 26 18:29:26 201
2 ...
encounter 2> source addbond.cmd
```

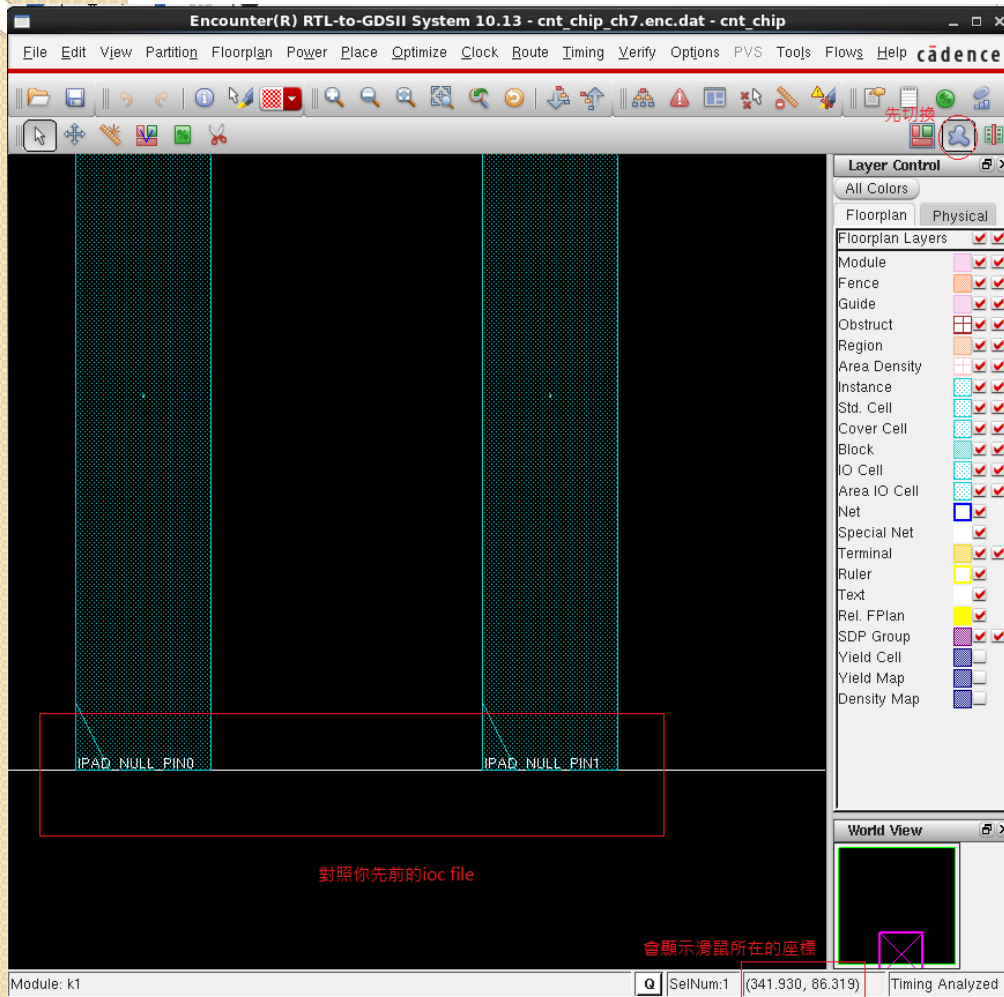
# Add Bonding Pad

- 可以看到pad加入新的元件



# Add Bonding Pad

- 加入IO VSS/VDD Power Label



cnt\_chip\_netlistfinal.dc

power.rpt

cnt\_chip.ioc

1 Version: 1

2

3 Pad: CORNER0 NW PCORNER

4 Pad: IPAD\_CLK N

5 Pad: PAD\_CoreVSS1 N PVSS1DGZ

6 Pad: PAD\_CoreVDD1 N PVDD1DGZ

7 Pad: IPAD\_RST N

8

9 Pad: CORNER1 NE PCORNER

10 Pad: OPAD\_OUT0 W

11 Pad: OPAD\_OUT1 W

12 Pad: OPAD\_OUT2 W

13 Pad: OPAD\_OUT3 W

14

15 Pad: CORNER2 SW PCORNER

16 Pad: IPAD\_NULL\_PIN0 S

17 Pad: PAD\_IOVDD1 S PVDD2DGZ

18 Pad: PAD\_IOVSS1 S PVSS2DGZ

19 Pad: IPAD\_NULL\_PIN1 S |

20

21 Pad: CORNER3 SE PCORNER

22 Pad: IPAD\_SCAN\_EN E

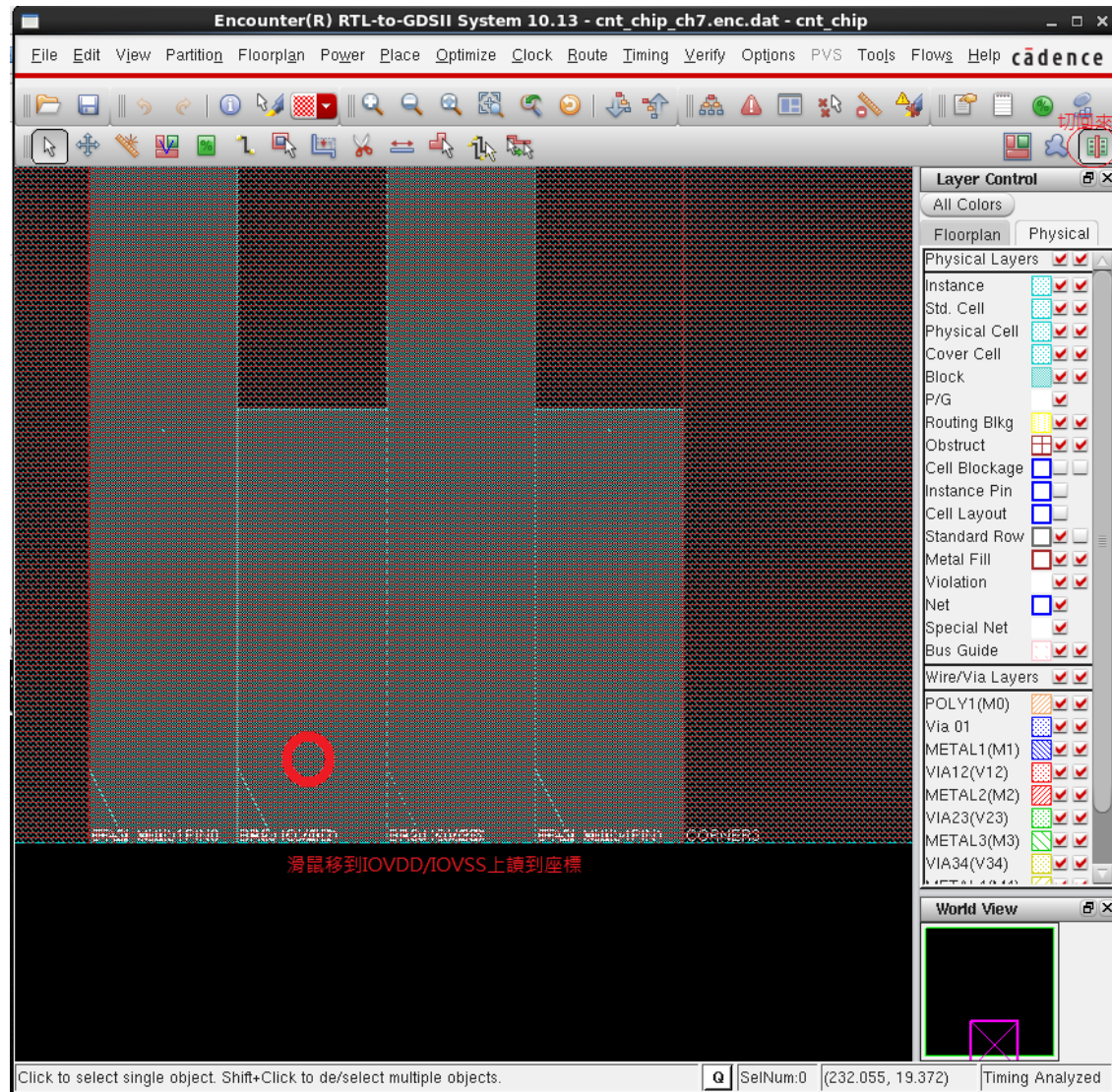
23 Pad: IPAD\_SCAN\_IN E

24 Pad: IPAD\_NULL\_PIN2 E

25 Pad: OPAD\_SCAN\_OUT E



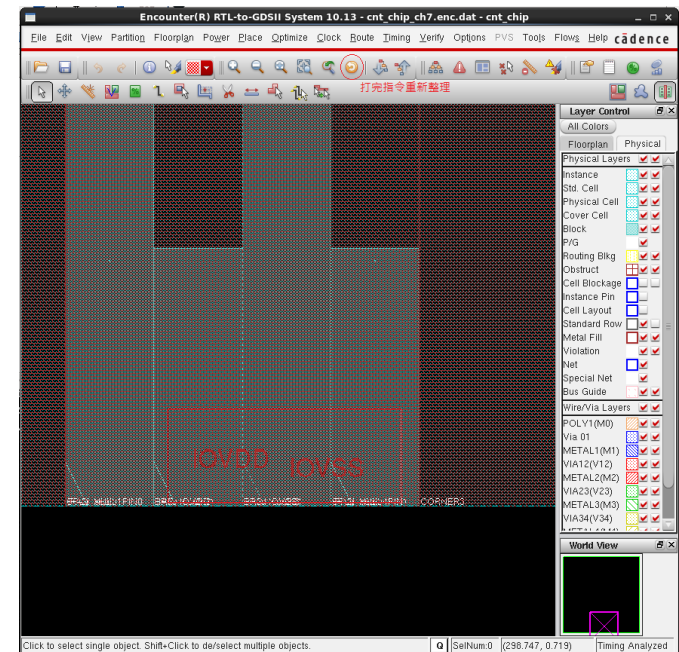
# Add Bonding Pad





# Add Bonding Pad

- 在Encounter Terminal打 `addCustomText`  
`METAL5 IOVDD X Y 10 addCustomText`  
`METAL5 IOVSS X Y 10` 如上面方法沒有跑出標籤則打  
`add_text -layer METAL5 -pt X Y -label IOVDD -height 1`  
`add_text -layer METAL5 -pt X Y -label IOVSS -height 1`  
X Y為上一頁讀到的座標



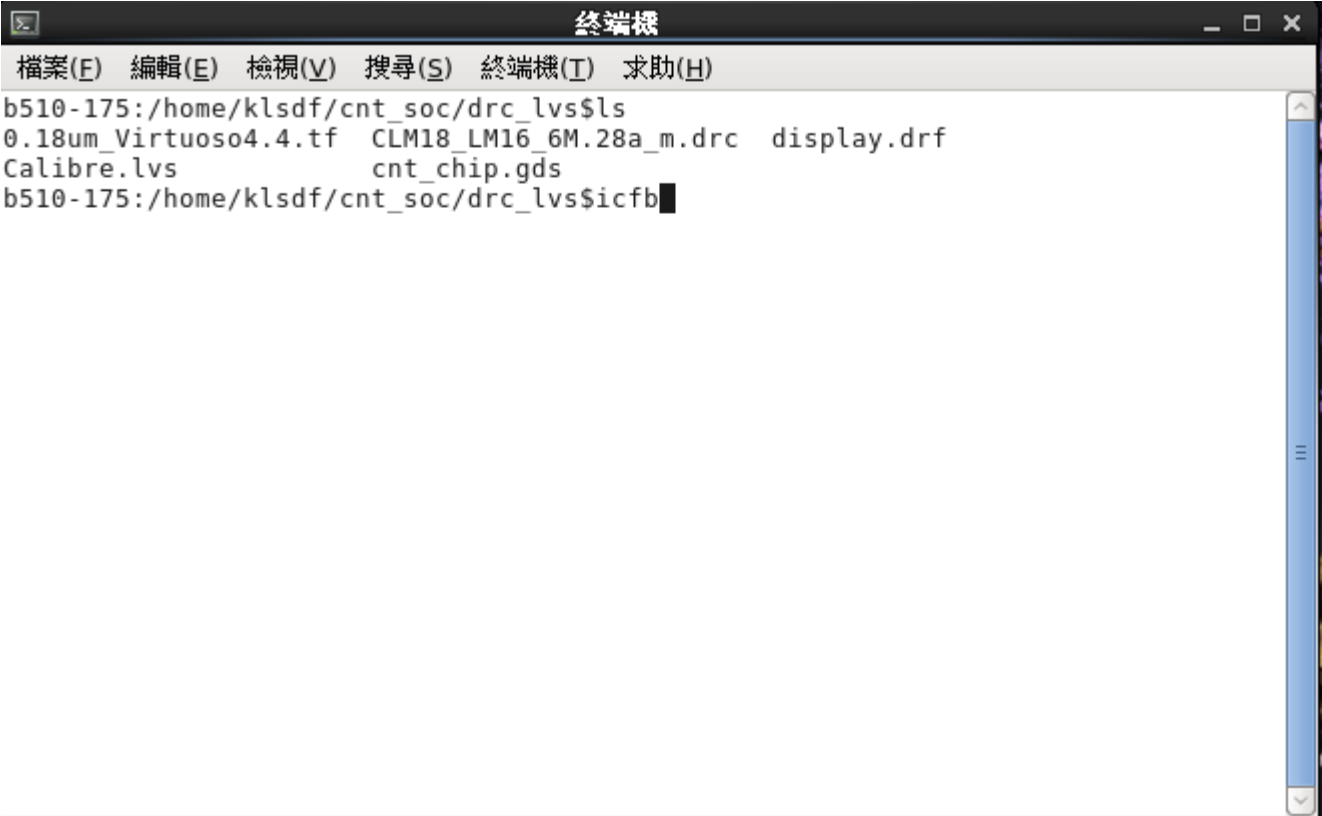
# Stream Out GDS

- 將工作站上的streamout資料夾中的streamout.map與savegds.cmd上傳到執行目錄，之後在 Encounter Terminal 打 source savegds.cmd。
- Savegds.cmd內容如下

```
setStreamOutMode -specifyViaName default \  
-SEviaNames false \  
-virtualConnection false \  
-uniquifyCellNamesPrefix false \  
-snapToMGrid false \  
-textSize 1 \  
-version 3  
  
streamOut 輸出檔名 cnt_chip.gds -mapFile streamOut.map \  
-merge {/usr/techfile/CBDK_TSMC018_Arm_v3.2/CIC/Phantom/tpb973gv.gds \  
/usr/techfile/CBDK_TSMC018_Arm_v3.2/CIC/Phantom/tsmc18_core.gds \  
/usr/techfile/CBDK_TSMC018_Arm_v3.2/CIC/Phantom/tsmc18_io.gds } \  
-stripes 1 -units 1000 -mode ALL
```

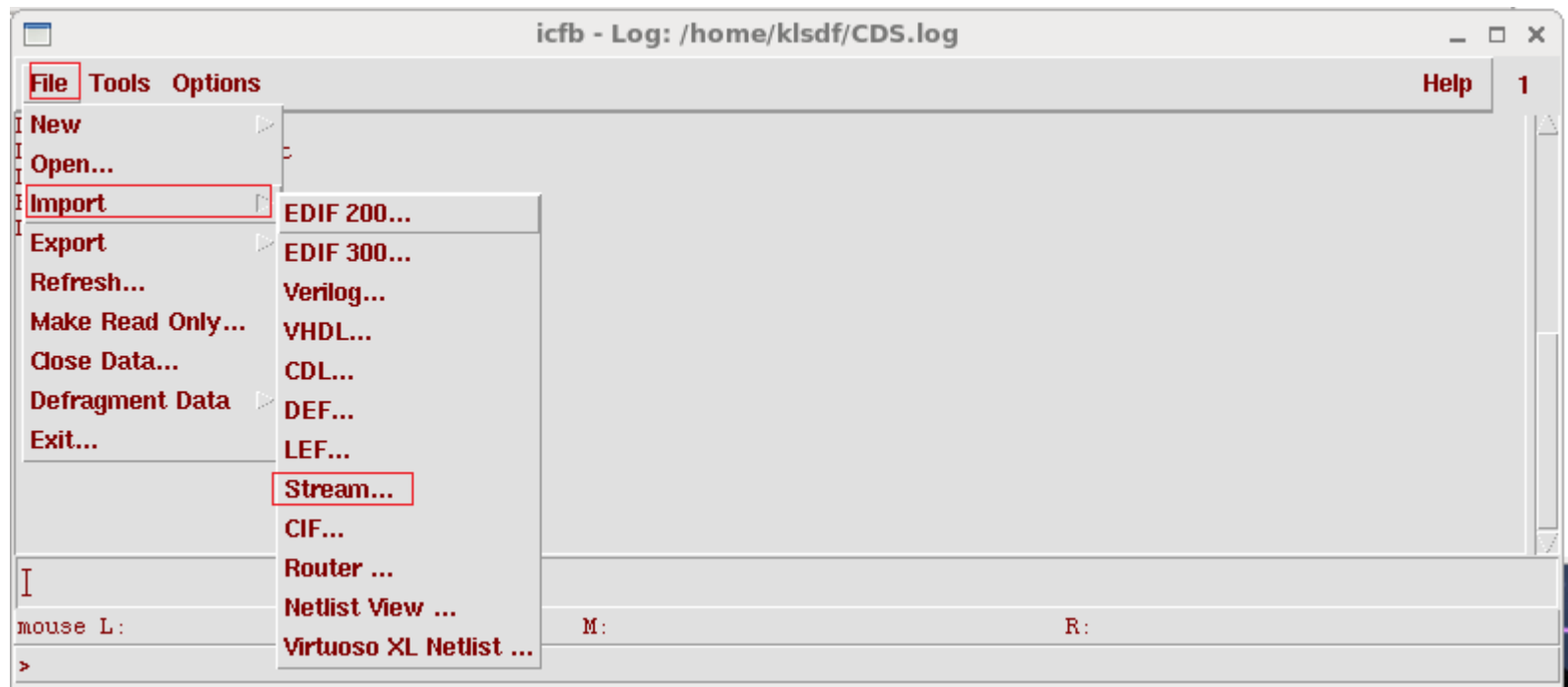
# DRC&LVS

- 將drc\_lvs上傳至工作站並把剛剛產生的gds放入此目錄後執行icfb，因為並不能確保Encounter所產生的繞線等符合製程所以需要另外驗證，有錯則使用icfb做修正。

A screenshot of a terminal window titled "終端機" (Terminal). The window has a menu bar with options: 檔案(E), 編輯(E), 檢視(V), 搜尋(S), 終端機(T), and 求助(H). The terminal output shows the user at the prompt "b510-175:/home/kl sdf/cnt\_soc/drc\_lvs\$ls" listing files: "0.18um\_Virtuoso4.4.tf", "CLM18\_LM16\_6M.28a\_m.drc", "display.drf", "Calibre.lvs", and "cnt\_chip.gds". The user then enters the command "b510-175:/home/kl sdf/cnt\_soc/drc\_lvs\$icfb" at the prompt, and the cursor is positioned at the end of the command.

```
b510-175:/home/kl sdf/cnt_soc/drc_lvs$ls
0.18um_Virtuoso4.4.tf  CLM18_LM16_6M.28a_m.drc  display.drf
Calibre.lvs           cnt_chip.gds
b510-175:/home/kl sdf/cnt_soc/drc_lvs$icfb
```

# DRC&LVS



# DRC&LVS

**Virtuoso® Stream In**

OK Cancel Defaults Apply Help

User-Defined Data And Options User-Defined Data Options Set Fast Options

Template File Load Save Browse... [ ]

Run Directory [ ]

Input File [ ] Browse...

Top Cell Name [ ]

Output ☒ Opus DB ☐ ASCII Dump ☐ TechFile

Library Name [ ]

ASCII Technology File Name [ ] Browse...

Scale UU/DBU 0.00100000

Units ☒ micron ☐ millimeter ☐ mil

Process Nice Value 0-20 [ ]

Error Message File PIP0.LOG Browse...

**Unix Browser**

OK Cancel Apply Open Help

File

0.18um\_Virtuoso4.4.tf

../ (Go up one directory)

0.18um\_Virtuoso4.4.tf

Current Directory

/home/kl sdf/cnt\_soc/drc\_lvs

# DRC&LVS

**Virtuoso® Stream In**

OK Cancel Defaults Apply Help

User-Defined Data And Options User-Defined Data Options Set Fast Options

Template File Load Save Browse... [ ]

Run Directory [ ]

Input File [ ] Browse...

Top Cell Name [ ]

Output ☒ Opus DB ☐ ASCII Dump ☐ TechFile

Library Name [ ]

ASCII Technology File Name [/0.18um\_Virtuoso4.4.tcl] Browse...

Scale UU/DBU [0.00100000]

Units ☒ micron ☐ millimeter ☐ mil

Process Nice Value 0-20 [0]

Error Message File [PIPO.LOG] Browse...

**Unix Browser**

OK Cancel Apply Open Help

File

cnt\_chip.gds

../ (Go up one directory)

cnt\_chip.gds

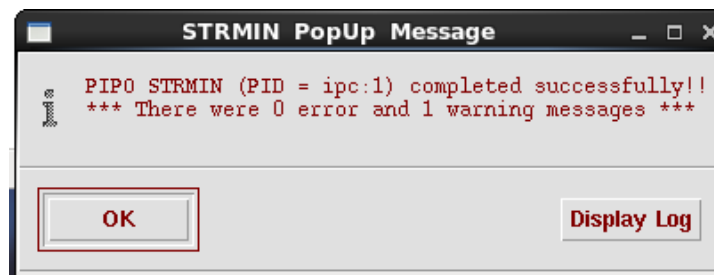
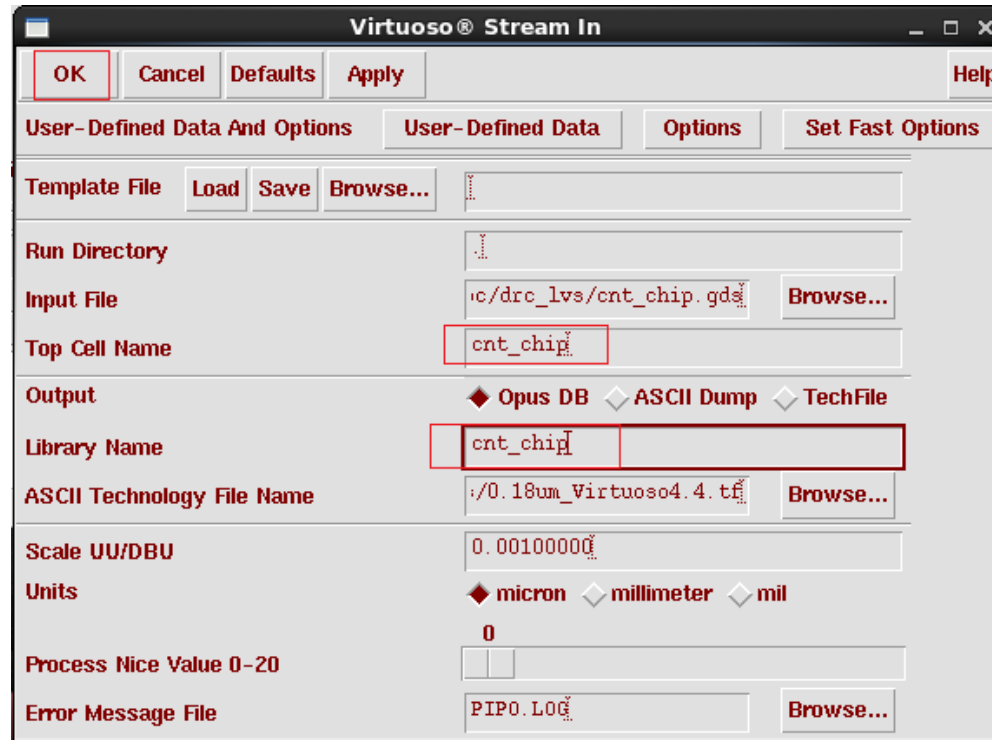
Current Directory

/home/kl sdf/cnt\_soc/drc\_lvs

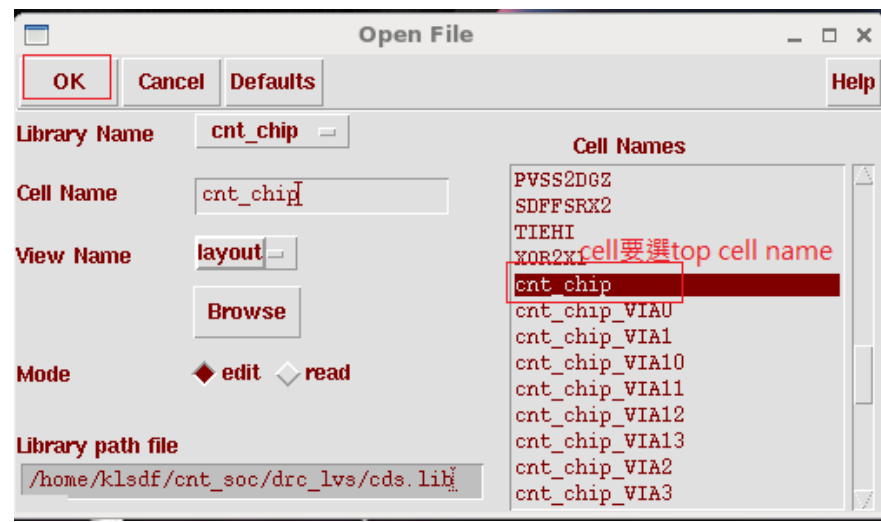
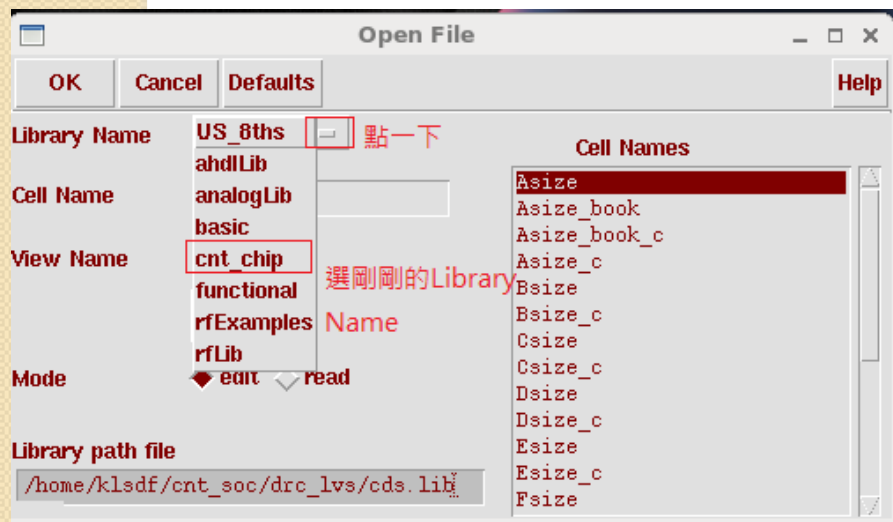
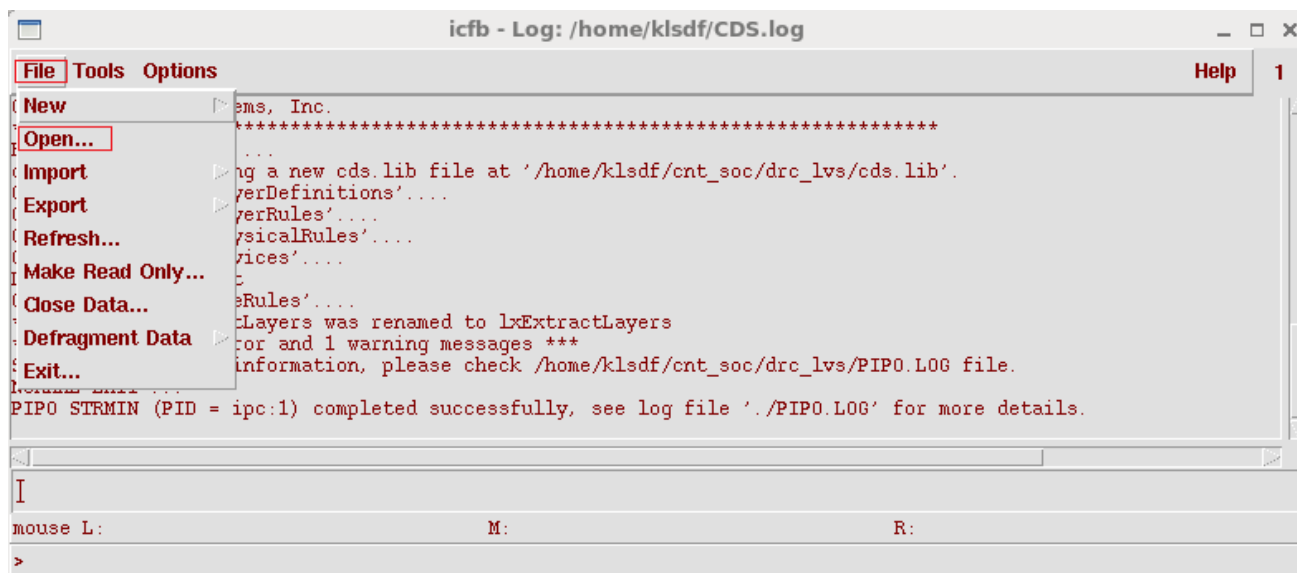


# DRC&LVS

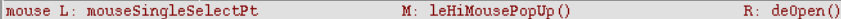
- 按ok後的Warring忽略



# DRC&LVS



- 可以看到Layout圖，如之後DRC LVS有錯可在此修正，但不在本課程的範圍



# DRC&LVS

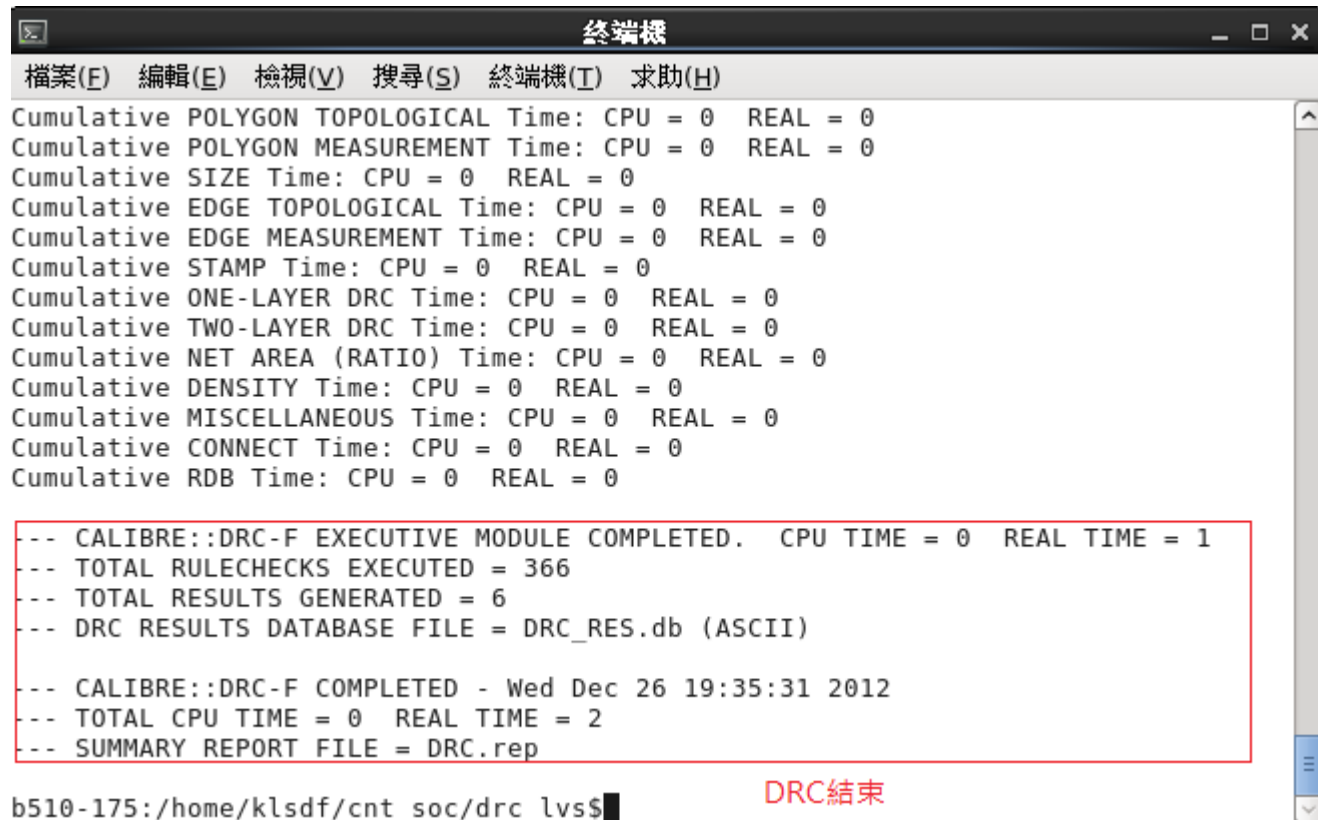
- 更改目錄下的CLM18\_LM16\_6M.28a\_m.drc內容

```
CLM18_LM16_6M.28a_m.drc X
601
602
603 // #DEFINE CHECK_LATCHUP_BY_TEXT // Turn on to recognize IO PAD by following text
604 VARIABLE PAD_TEXT "?" // pin name of PAD
605 VARIABLE VDD_TEXT "AVDDBG" "AVDDR" "AVDWELL" "VDWELL" "VD33APST" "VDD5V" "TAVD33"
"VD33PST" "AVDD" "TAVDD" "TAVD33PST" "TAVDDPST" "AVD33B" "VDD" "AVD33G" "DVDD" "AVDDG"
"AVddb" "VDDG" "VDDPST" "VD33REF" "VD33" "AVD33R" "VDDSA" // pin name of VDD
606 VARIABLE VSS_TEXT "VSSPST" "AVS33R" "AVSSUB" "VSSREF" "VSSAPST" "VS33APST" "DVSS"
"AVS33G" "AVSSBG" "TAVSS" "AVS33B" "AVSSB" "GND" "VSSG" "VSSUB" "VSS" "AVSS" "TAVSSPST"
"AGND" "AVSSR" "AVSSG" // pin name of VSS
607
608 #DEFINE CHECK_LATCHUP_BY_PAD_CONNECTION // Turn on to recognize recognize the MOS
connected to I/O by connection
609
610
611 //
612 // ENVIRONMENT SETUP
613 //-----
614 PRECISION 1000
615 RESOLUTION 5 // Set layout grid check to 0.005
616
617 LAYOUT SYSTEM GDSII
618 LAYOUT PATH "cnt_chip.gds" gds檔名
619 LAYOUT PRIMARY "cnt_chip" top cell name
620
621 DRC RESULTS DATABASE "DRC_RES.db"
622 DRC SUMMARY REPORT "DRC.rep"
623 DRC CHECK TEXT ALL
624 DRC MAXIMUM RESULTS ALL|
625 // DRC INCREMENTAL CONNECT YES
626
627 FLAG OFFGRID YES // For layout grid check. default grid value is resolution size
628 FLAG ACUTE YES
629 FLAG SKEW YES
630 FLAG NONSIMPLE YES
631
632 LAYOUT PROCESS BOX RECORD YES
633
634
```

# DRC&LVS

- Terminal執行drc

calibre -drc CLM18\_LM16\_6M.28a\_m.drc



```
終端機
檔案(E) 編輯(E) 檢視(V) 搜尋(S) 終端機(T) 求助(H)
Cumulative POLYGON TOPOLOGICAL Time: CPU = 0 REAL = 0
Cumulative POLYGON MEASUREMENT Time: CPU = 0 REAL = 0
Cumulative SIZE Time: CPU = 0 REAL = 0
Cumulative EDGE TOPOLOGICAL Time: CPU = 0 REAL = 0
Cumulative EDGE MEASUREMENT Time: CPU = 0 REAL = 0
Cumulative STAMP Time: CPU = 0 REAL = 0
Cumulative ONE-LAYER DRC Time: CPU = 0 REAL = 0
Cumulative TWO-LAYER DRC Time: CPU = 0 REAL = 0
Cumulative NET AREA (RATIO) Time: CPU = 0 REAL = 0
Cumulative DENSITY Time: CPU = 0 REAL = 0
Cumulative MISCELLANEOUS Time: CPU = 0 REAL = 0
Cumulative CONNECT Time: CPU = 0 REAL = 0
Cumulative RDB Time: CPU = 0 REAL = 0

--- CALIBRE::DRC-F EXECUTIVE MODULE COMPLETED. CPU TIME = 0 REAL TIME = 1
--- TOTAL RULECHECKS EXECUTED = 366
--- TOTAL RESULTS GENERATED = 6
--- DRC RESULTS DATABASE FILE = DRC_RES.db (ASCII)

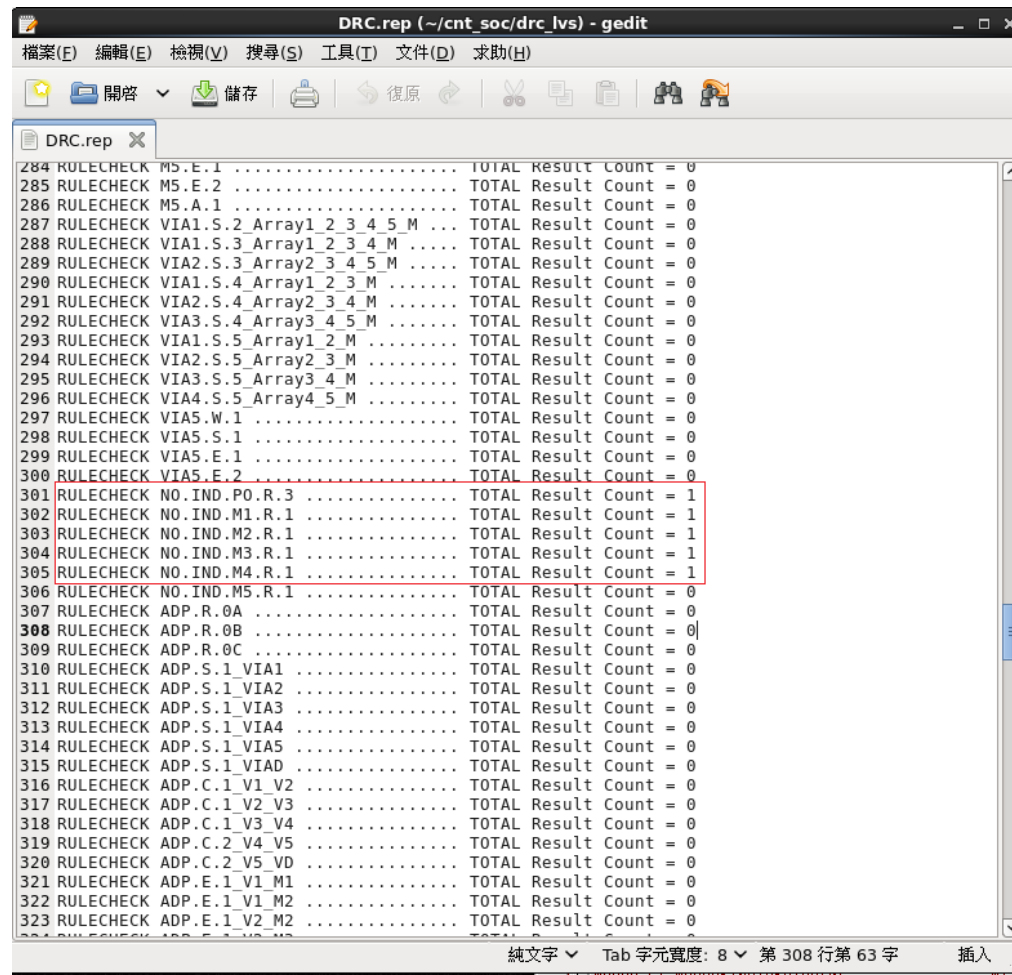
--- CALIBRE::DRC-F COMPLETED - Wed Dec 26 19:35:31 2012
--- TOTAL CPU TIME = 0 REAL TIME = 2
--- SUMMARY REPORT FILE = DRC.rep

b510-175:/home/kl sdf/cnt_soc/drc_lvs$
```

DRC結束

# DRC&LVS

- 觀看DRC.rep，圖中這幾個DRC ERROR指的是Metal 及Poly的density不足，可以不必理會，如有其他的就需要修正。

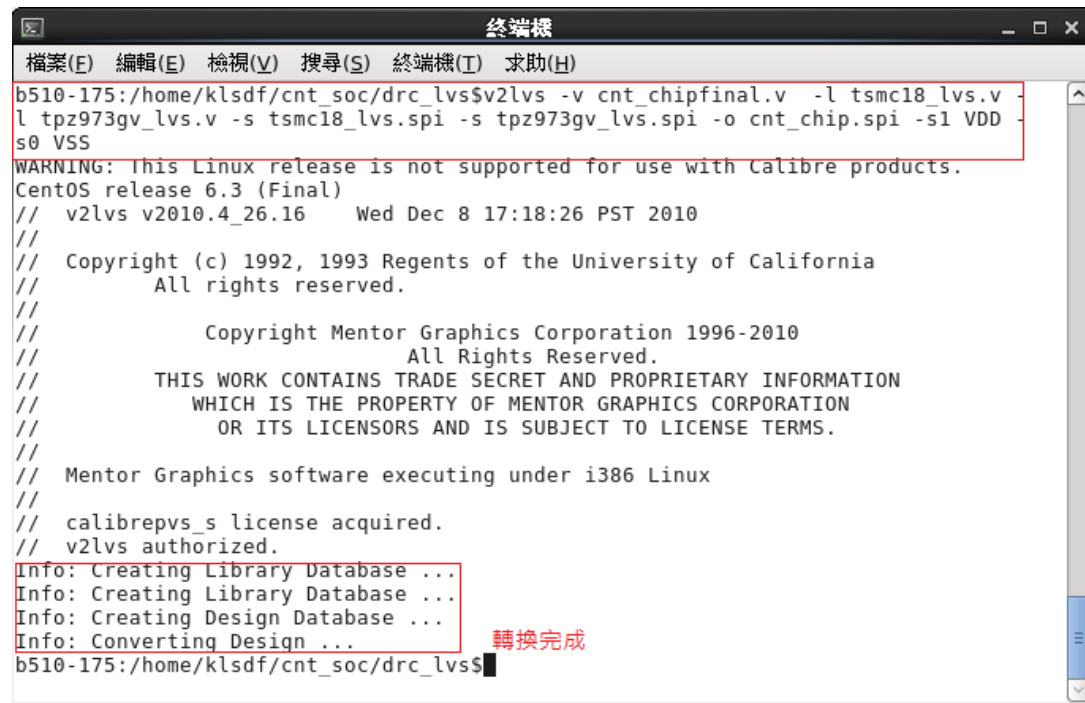


```
DRC.rep (~/.cnt_soc/drc_lvs) - gedit
檔案(F) 編輯(E) 檢視(V) 搜尋(S) 工具(T) 文件(D) 求助(H)
開啓 儲存 復原
DRC.rep
284 RULECHECK M5.E.1 ..... TOTAL Result Count = 0
285 RULECHECK M5.E.2 ..... TOTAL Result Count = 0
286 RULECHECK M5.A.1 ..... TOTAL Result Count = 0
287 RULECHECK VIA1.S.2 Array1_2_3_4_5_M ... TOTAL Result Count = 0
288 RULECHECK VIA1.S.3 Array1_2_3_4_M ..... TOTAL Result Count = 0
289 RULECHECK VIA2.S.3 Array2_3_4_5_M ..... TOTAL Result Count = 0
290 RULECHECK VIA1.S.4 Array1_2_3_M ..... TOTAL Result Count = 0
291 RULECHECK VIA2.S.4 Array2_3_4_M ..... TOTAL Result Count = 0
292 RULECHECK VIA3.S.4 Array3_4_5_M ..... TOTAL Result Count = 0
293 RULECHECK VIA1.S.5 Array1_2_M ..... TOTAL Result Count = 0
294 RULECHECK VIA2.S.5 Array2_3_M ..... TOTAL Result Count = 0
295 RULECHECK VIA3.S.5 Array3_4_M ..... TOTAL Result Count = 0
296 RULECHECK VIA4.S.5 Array4_5_M ..... TOTAL Result Count = 0
297 RULECHECK VIAS.W.1 ..... TOTAL Result Count = 0
298 RULECHECK VIAS.S.1 ..... TOTAL Result Count = 0
299 RULECHECK VIAS.E.1 ..... TOTAL Result Count = 0
300 RULECHECK VIAS.E.2 ..... TOTAL Result Count = 0
301 RULECHECK NO.IND.P0.R.3 ..... TOTAL Result Count = 1
302 RULECHECK NO.IND.M1.R.1 ..... TOTAL Result Count = 1
303 RULECHECK NO.IND.M2.R.1 ..... TOTAL Result Count = 1
304 RULECHECK NO.IND.M3.R.1 ..... TOTAL Result Count = 1
305 RULECHECK NO.IND.M4.R.1 ..... TOTAL Result Count = 1
306 RULECHECK NO.IND.M5.R.1 ..... TOTAL Result Count = 0
307 RULECHECK ADP.R.0A ..... TOTAL Result Count = 0
308 RULECHECK ADP.R.0B ..... TOTAL Result Count = 0
309 RULECHECK ADP.R.0C ..... TOTAL Result Count = 0
310 RULECHECK ADP.S.1_VIA1 ..... TOTAL Result Count = 0
311 RULECHECK ADP.S.1_VIA2 ..... TOTAL Result Count = 0
312 RULECHECK ADP.S.1_VIA3 ..... TOTAL Result Count = 0
313 RULECHECK ADP.S.1_VIA4 ..... TOTAL Result Count = 0
314 RULECHECK ADP.S.1_VIA5 ..... TOTAL Result Count = 0
315 RULECHECK ADP.S.1_VIAD ..... TOTAL Result Count = 0
316 RULECHECK ADP.C.1_V1_V2 ..... TOTAL Result Count = 0
317 RULECHECK ADP.C.1_V2_V3 ..... TOTAL Result Count = 0
318 RULECHECK ADP.C.1_V3_V4 ..... TOTAL Result Count = 0
319 RULECHECK ADP.C.2_V4_V5 ..... TOTAL Result Count = 0
320 RULECHECK ADP.C.2_V5_VD ..... TOTAL Result Count = 0
321 RULECHECK ADP.E.1_V1_M1 ..... TOTAL Result Count = 0
322 RULECHECK ADP.E.1_V1_M2 ..... TOTAL Result Count = 0
323 RULECHECK ADP.E.1_V2_M2 ..... TOTAL Result Count = 0
純文字 Tab 字元寬度: 8 第 308 行第 63 字 插入
```



# DRC&LVS

- 將Verilog Netlist File轉成Spice格式才能做lvs
- 將之前encounter的netlistfinal的.v檔放入此資料夾後打入以下指令
- `v2lvs -v netlistfinalname.v -l tsmc18_lvs.v -l tpz973gv_lvs.v -s tsmc18_lvs.spi -s tpz973gv_lvs.spi -o outputfilename.spi -s1 VDD -s0 VSS`



```
终端機
檔案(E) 編輯(E) 檢視(V) 搜尋(S) 终端機(T) 求助(H)
b510-175:/home/kl sdf/cnt_soc/drc_lvsv2lvs -v cnt_chipfinal.v -l tsmc18_lvs.v
l tpz973gv_lvs.v -s tsmc18_lvs.spi -s tpz973gv_lvs.spi -o cnt_chip.spi -s1 VDD
s0 VSS
WARNING: This Linux release is not supported for use with Calibre products.
CentOS release 6.3 (Final)
// v2lvs v2010.4_26.16 Wed Dec 8 17:18:26 PST 2010
//
// Copyright (c) 1992, 1993 Regents of the University of California
// All rights reserved.
//
// Copyright Mentor Graphics Corporation 1996-2010
// All Rights Reserved.
// THIS WORK CONTAINS TRADE SECRET AND PROPRIETARY INFORMATION
// WHICH IS THE PROPERTY OF MENTOR GRAPHICS CORPORATION
// OR ITS LICENSORS AND IS SUBJECT TO LICENSE TERMS.
//
// Mentor Graphics software executing under i386 Linux
//
// calibrepvs_s license acquired.
// v2lvs authorized.
Info: Creating Library Database ...
Info: Creating Library Database ...
Info: Creating Design Database ...
Info: Converting Design ...
b510-175:/home/kl sdf/cnt_soc/drc_lvss
```

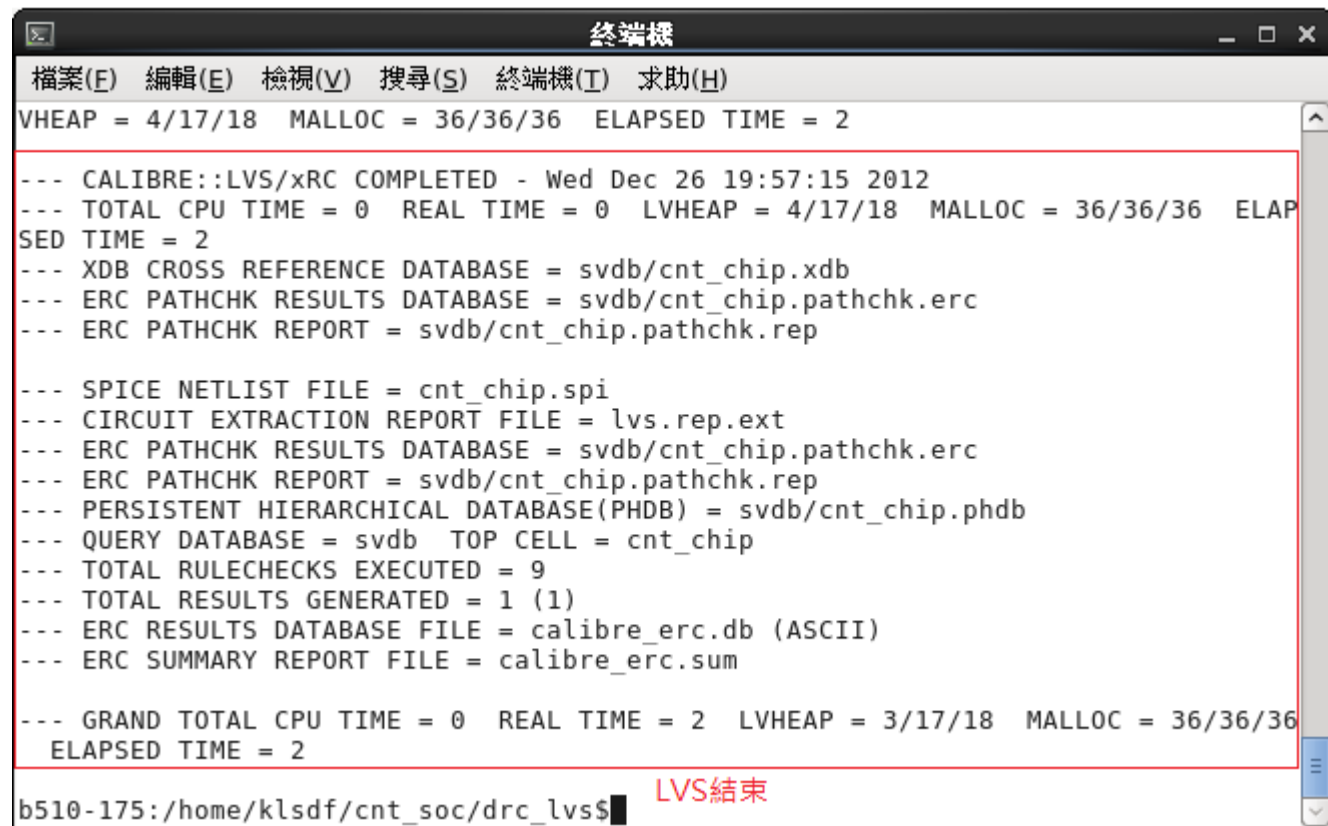
轉換完成

- 修改目錄下的Calibre.lvs



# DRC&LVS

- 執行lvs
- calibre -lvs -spice **spicefilename**.spi -hier -auto Calibre.lvs



```
終端機
檔案(E) 編輯(E) 檢視(V) 搜尋(S) 終端機(T) 求助(H)
VHEAP = 4/17/18  MALLOC = 36/36/36  ELAPSED TIME = 2

--- CALIBRE::LVS/xRC COMPLETED - Wed Dec 26 19:57:15 2012
--- TOTAL CPU TIME = 0  REAL TIME = 0  LVHEAP = 4/17/18  MALLOC = 36/36/36  ELAPSED TIME = 2
--- XDB CROSS REFERENCE DATABASE = svdb/cnt_chip.xdb
--- ERC PATHCHK RESULTS DATABASE = svdb/cnt_chip.pathchk.erc
--- ERC PATHCHK REPORT = svdb/cnt_chip.pathchk.rep

--- SPICE NETLIST FILE = cnt_chip.spi
--- CIRCUIT EXTRACTION REPORT FILE = lvs.rep.ext
--- ERC PATHCHK RESULTS DATABASE = svdb/cnt_chip.pathchk.erc
--- ERC PATHCHK REPORT = svdb/cnt_chip.pathchk.rep
--- PERSISTENT HIERARCHICAL DATABASE(PHDB) = svdb/cnt_chip.phdb
--- QUERY DATABASE = svdb  TOP CELL = cnt_chip
--- TOTAL RULECHECKS EXECUTED = 9
--- TOTAL RESULTS GENERATED = 1 (1)
--- ERC RESULTS DATABASE FILE = calibre_erc.db (ASCII)
--- ERC SUMMARY REPORT FILE = calibre_erc.sum

--- GRAND TOTAL CPU TIME = 0  REAL TIME = 2  LVHEAP = 3/17/18  MALLOC = 36/36/36
    ELAPSED TIME = 2

b510-175:/home/kl sdf/cnt_soc/drc_lvs$
```

LVS結束

# DRC&LVS

- 觀看lvs.rep，看到笑臉即驗證完成。

```
Calibre.lvs x lvs.rep x
1 |
2 |
3 |
4 | #####
5 | ##                                ##
6 | ##          C A L I B R E    S Y S T E M          ##
7 | ##                                ##
8 | ##          L V S    R E P O R T                    ##
9 | ##                                ##
10 | #####
11 |
12 |
13 |
14 REPORT FILE NAME:      lvs.rep
15 LAYOUT NAME:          cnt_chip.spi ('cnt_chip')
16 SOURCE NAME:          cnt_chip.spi ('cnt_chip')
17 RULE FILE:            Calibre.lvs
18 HCELL FILE:           (-automatch)
19 CREATION TIME:        Wed Dec 26 19:57:15 2012
20 CURRENT DIRECTORY:    /home/kl sdf/cnt_soc/drc_lvs
21 USER NAME:            kl sdf
22 CALIBRE VERSION:      v2010.4_26.16    Wed Dec 8 17:14:51 PST 2010
23 |
24 |
25 |
26 | OVERALL COMPARISON RESULTS
27 |
28 |
29 |
30 | #                                #####
31 | #                                #                                * *
32 | #                                #                                |
33 | #                                #                                \_/_/
34 | #                                #####
35 |
36 |
37 Warning:  Ambiguity points were found and resolved arbitrarily.
38 Warning:  Source and layout refer to the same data.
39 |
```