ASIC教材

Chapter9 SOC DRC&LVS

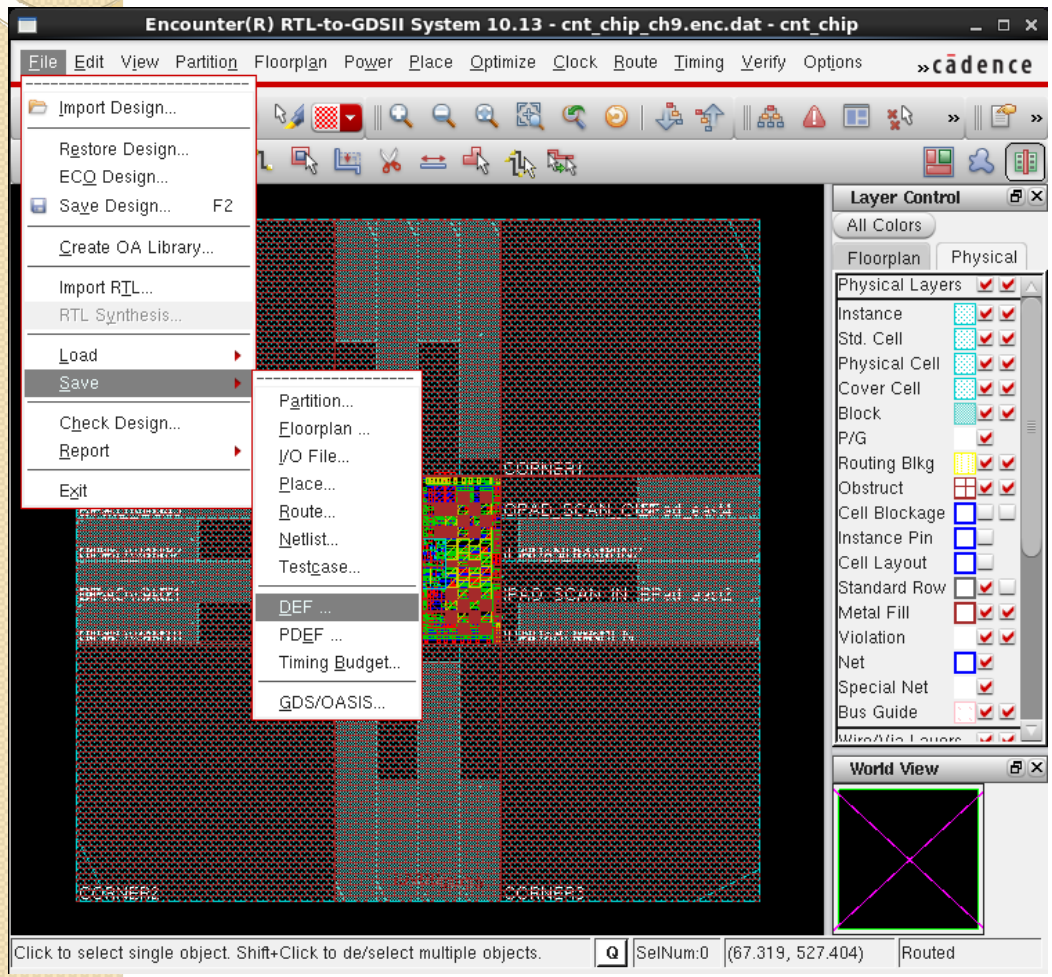
高雄第一科技大學 電子工程系
B510實驗室

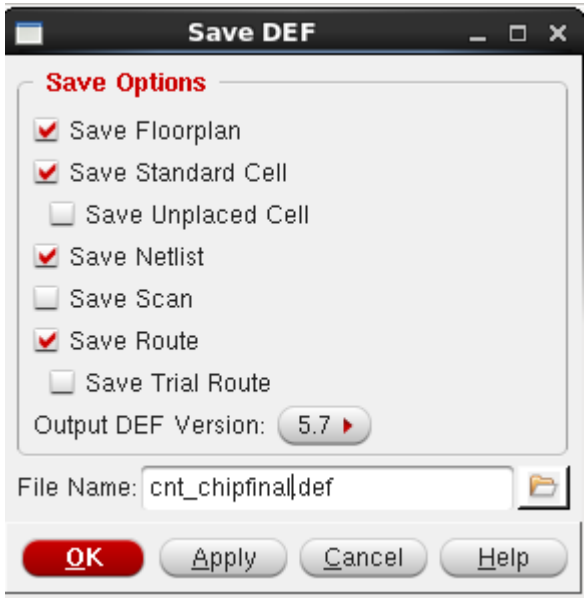
目錄

- Add Bonding Pad
- Stream Out GDS
- DRC&LVS

Add Bonding Pad

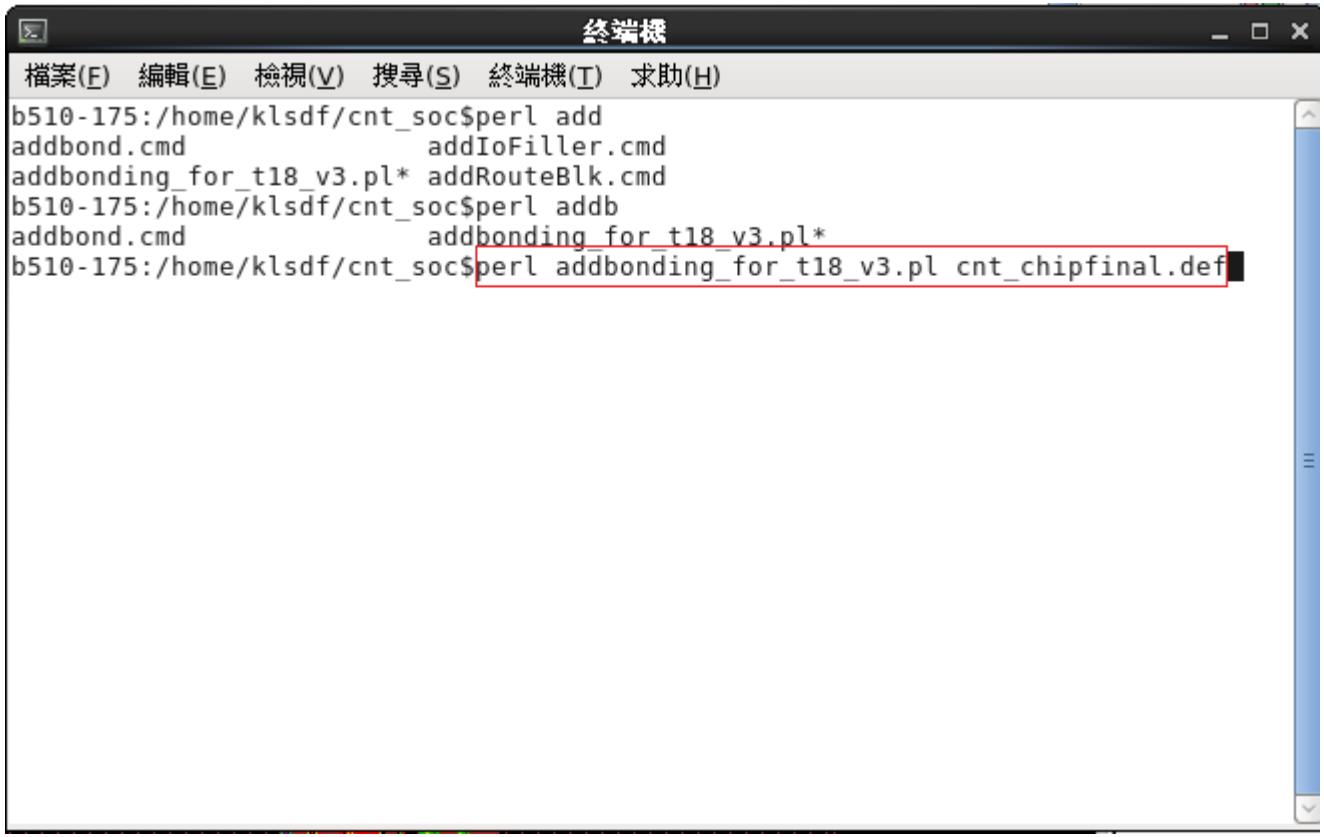
- 儲存最後的DEF資訊，加入final區別。





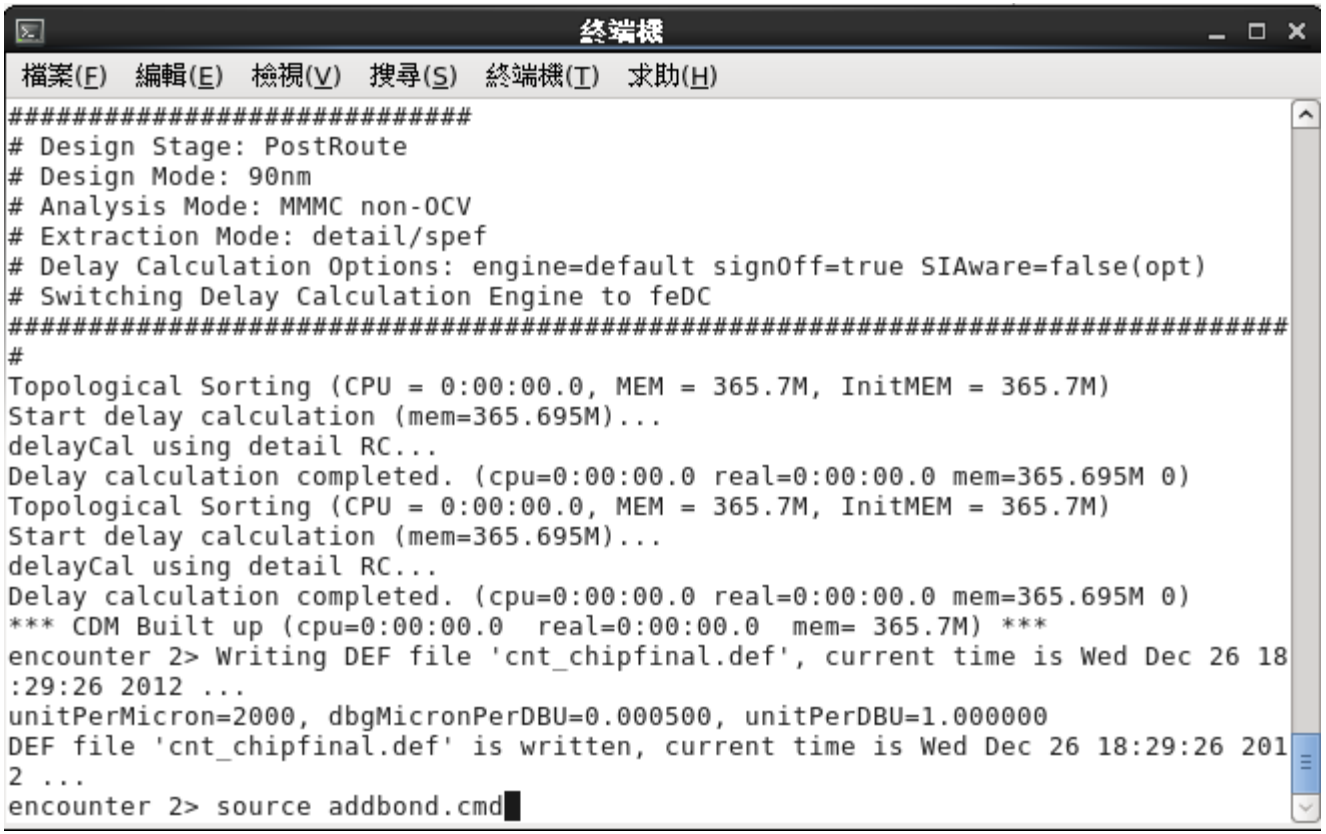
Add Bonding Pad

- 重新計算Bonding資訊



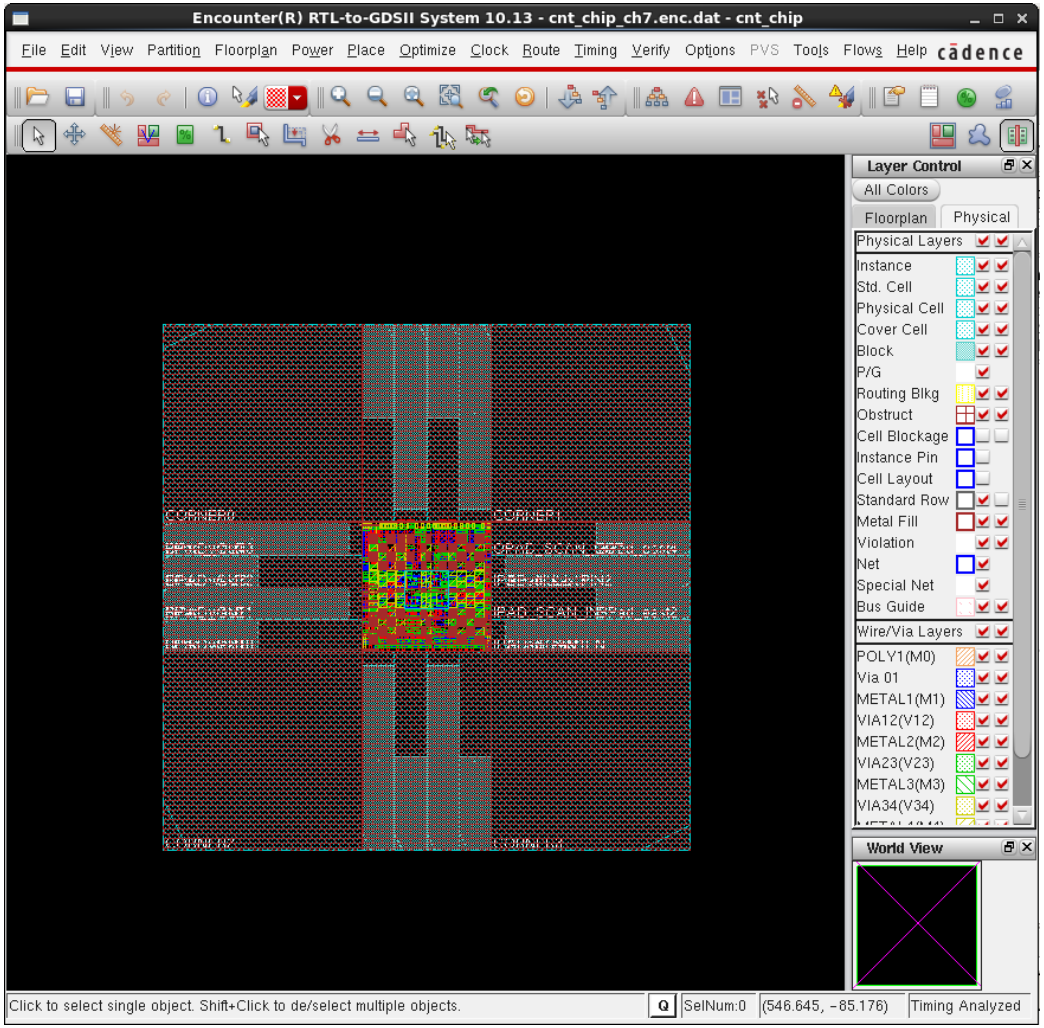
Add Bonding Pad

- Encounter打入source addbond.cmd



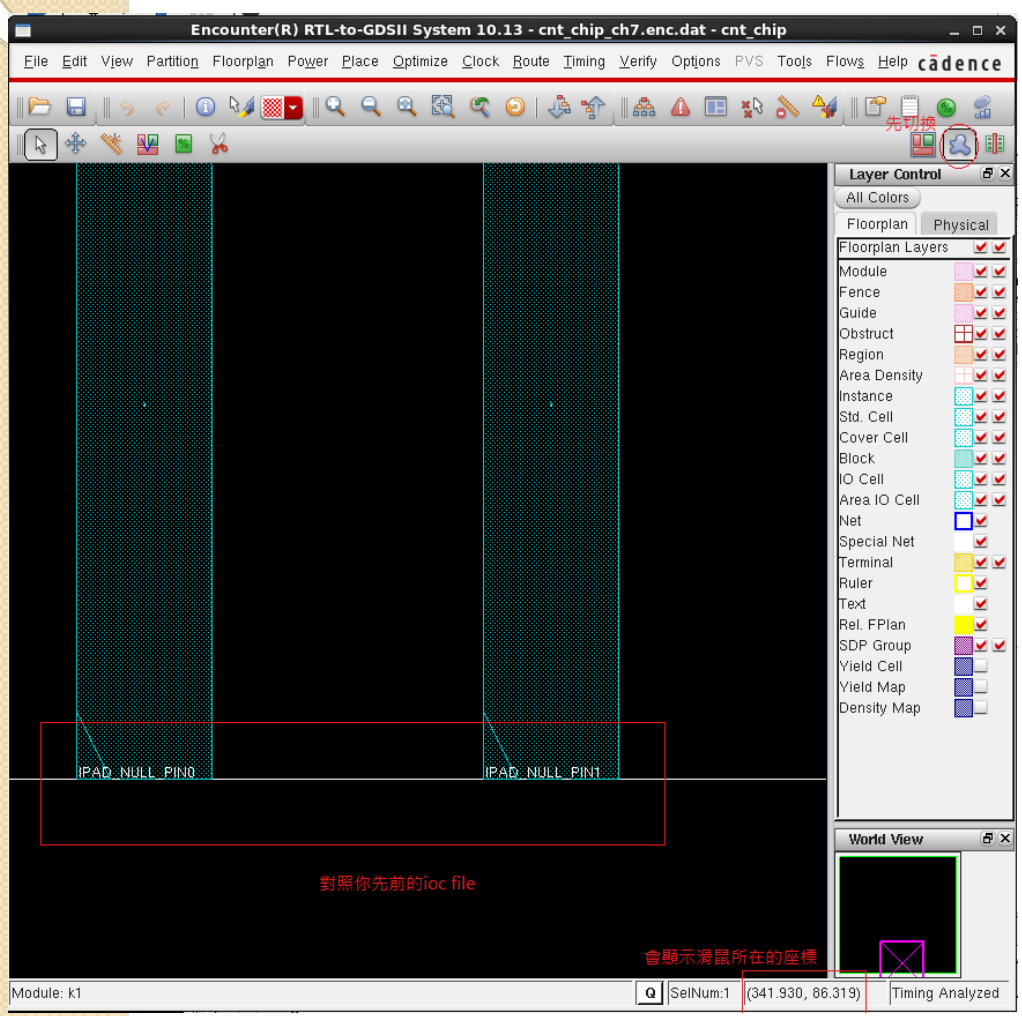
Add Bonding Pad

- 可以看到pad加入新的元件



Add Bonding Pad

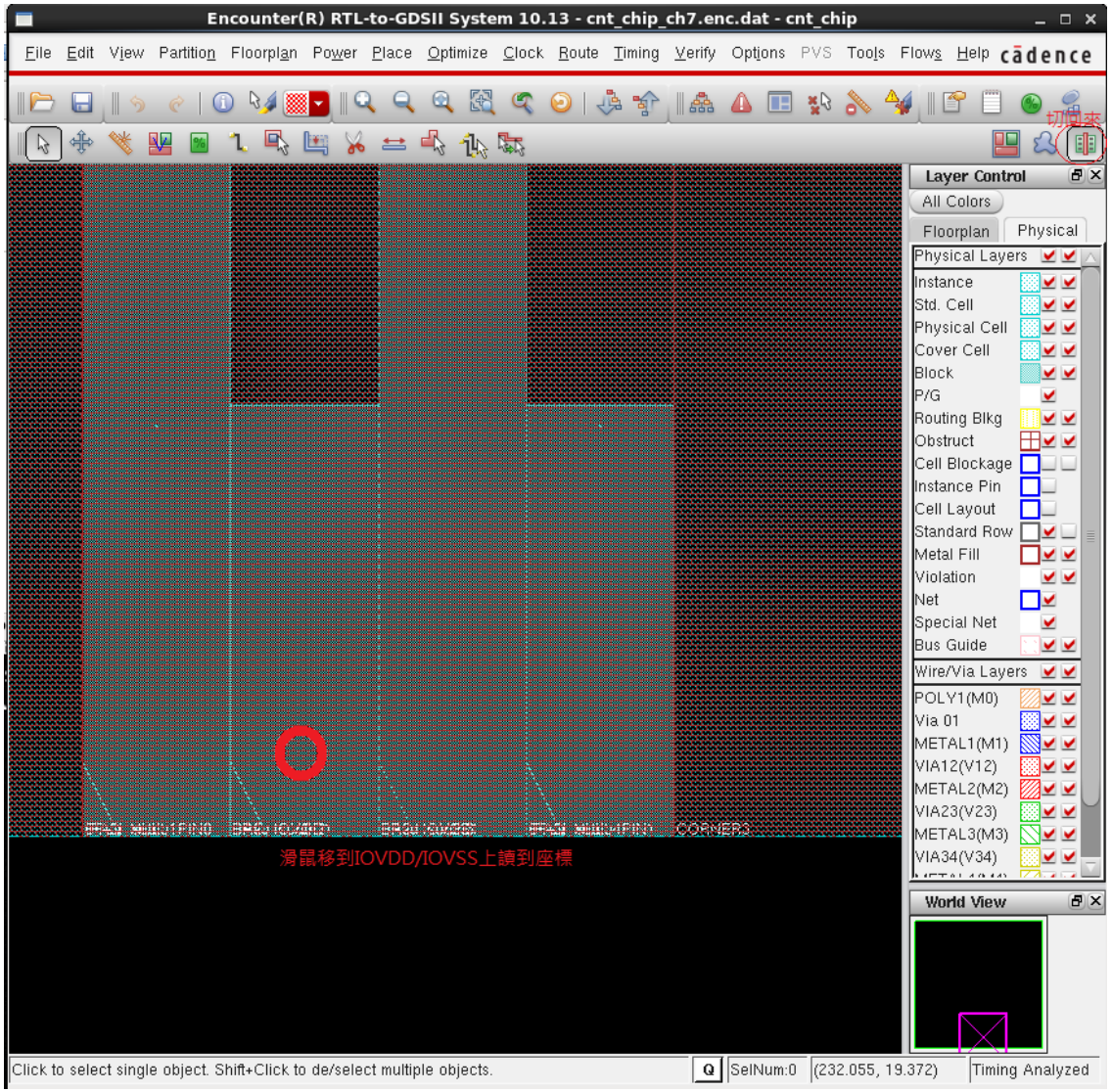
- 加入IO VSS/VDD Power Label



cnt_chip_netlistfinal.dc | power.rpt | cnt_chip.ioc

```
 1 Version: 1
 2
 3 Pad: CORNER0          NW        PCORNER
 4 Pad: IPAD_CLK         N
 5 Pad: PAD_CoreVSS1     N         PVSS1DGZ
 6 Pad: PAD_CoreVDD1     N         PVDD1DGZ
 7 Pad: IPAD_RST         N
 8
 9 Pad: CORNER1          NE        PCORNER
10 Pad: OPAD_OUT0        W
11 Pad: OPAD_OUT1        W
12 Pad: OPAD_OUT2        W
13 Pad: OPAD_OUT3        W
14
15 Pad: CORNER2          SW        PCORNER
16 Pad: IPAD_NULL_PIN0   S
17 Pad: PAD_IOVDD1       S         PVDD2DGZ
18 Pad: PAD_IOVSS1       S         PVSS2DGZ
19 Pad: IPAD_NULL_PIN1   S
20
21 Pad: CORNER3          SE        PCORNER
22 Pad: IPAD_SCAN_EN     E
23 Pad: IPAD_SCAN_IN     E
24 Pad: IPAD_NULL_PIN2   E
25 Pad: OPAD_SCAN_OUT    E
```

Add Bonding Pad



Add Bonding Pad

- 在Encounter Terminal打 addCustomText

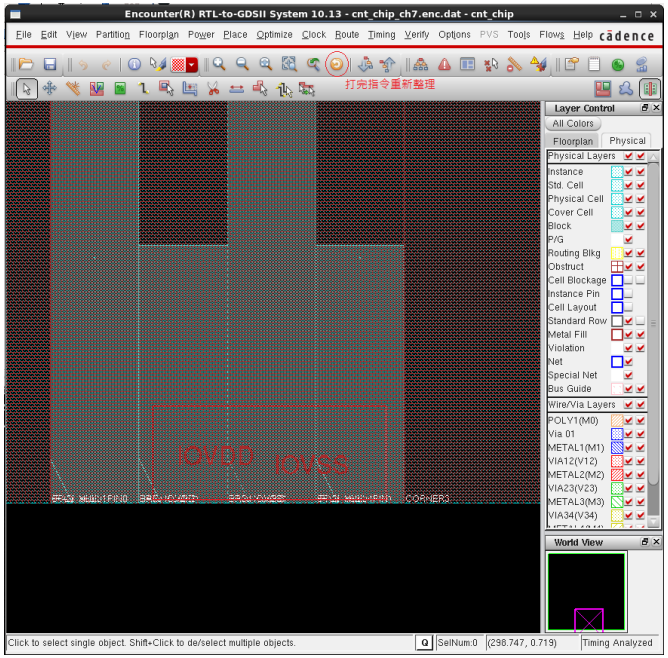
METAL5 IOVDD X Y 10 addCustomText

METAL5 IOVSS X Y 10 如上面方法沒有跑出標籤則打

add_text –layer METAL5 –pt X Y –label IOVDD –height 1

add_text –layer METAL5 –pt X Y –label IOVSS –height 1

X Y為上一頁讀到的座標



Stream Out GDS

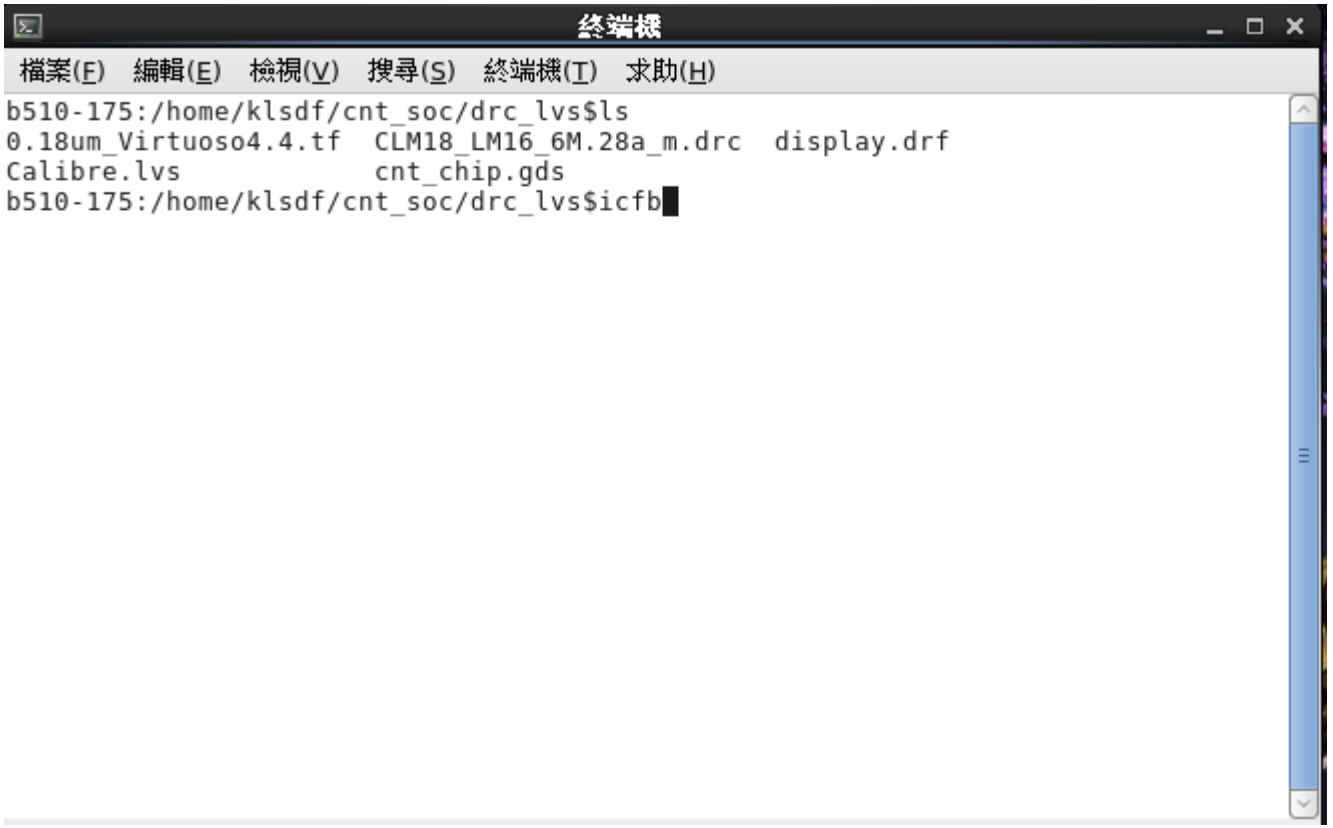
- 將工作站上的streamout資料夾中的streamout.map與savegds.cmd上傳到執行目錄，之後在 Encounter Terminal 打 source savegds.cmd。

- Savegds.cmd內容如下

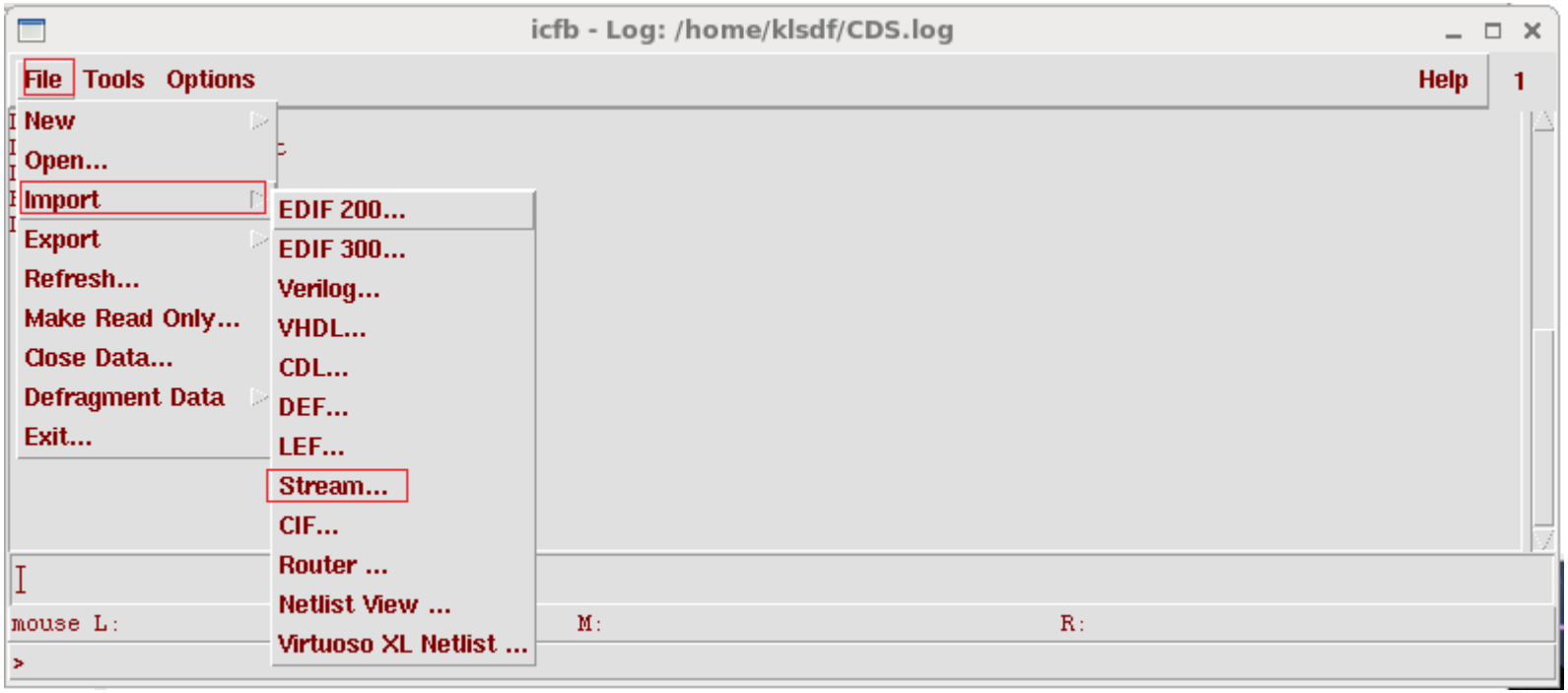
```
setStreamOutMode -specifyViaName default \
-SEvianames false \
-virtualConnection false \
-uniquifyCellNamesPrefix false \
-snapToMGrid false \
-textSize 1 \
-version 3
            輸出檔名
streamOut cnt_chip.gds -mapFile streamOut.map \
-merge {/usr/techfile/CBDK_TSMC018_Arm_v3.2/CIC/Phantom/tpb973gv.gds \
/usr/techfile/CBDK_TSMC018_Arm_v3.2/CIC/Phantom/tsmc18_core.gds \
/usr/techfile/CBDK_TSMC018_Arm_v3.2/CIC/Phantom/tsmc18_io.gds } \
-stripes 1 -units 1000 -mode ALL
```

DRC&LVS

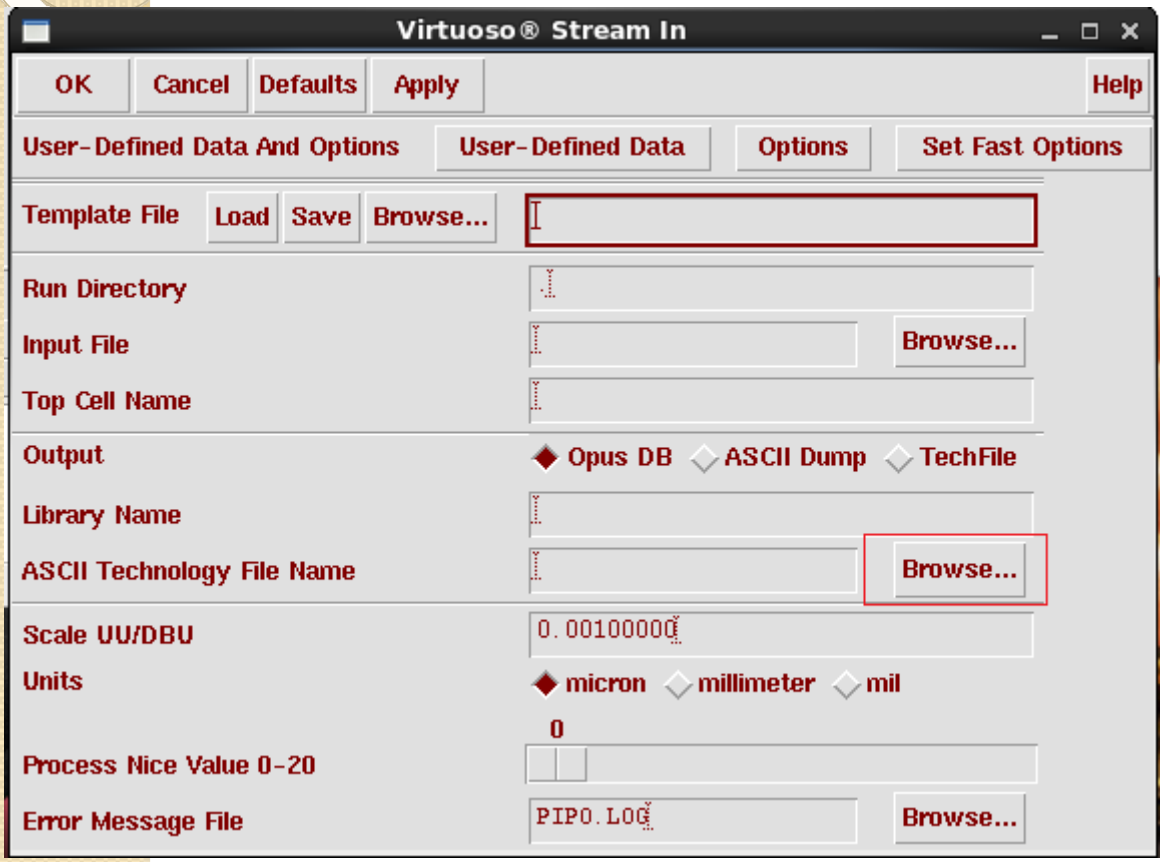
- 將drc_lvs上傳至工作站並把剛剛產生的gds放入此目錄後執行icfb，因為並不能確保Encounter所產生的繞線等符合製程所以需要做另外驗證，有錯則使用icfb做修正。

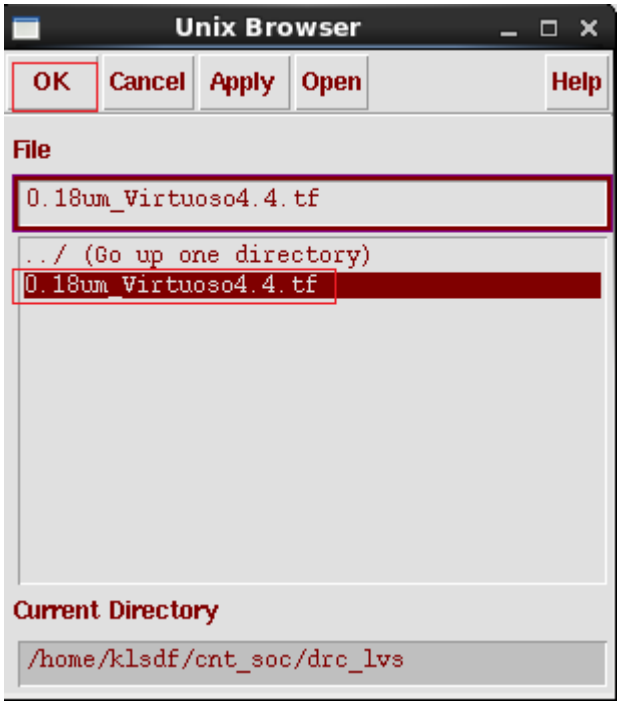


DRC&LVS

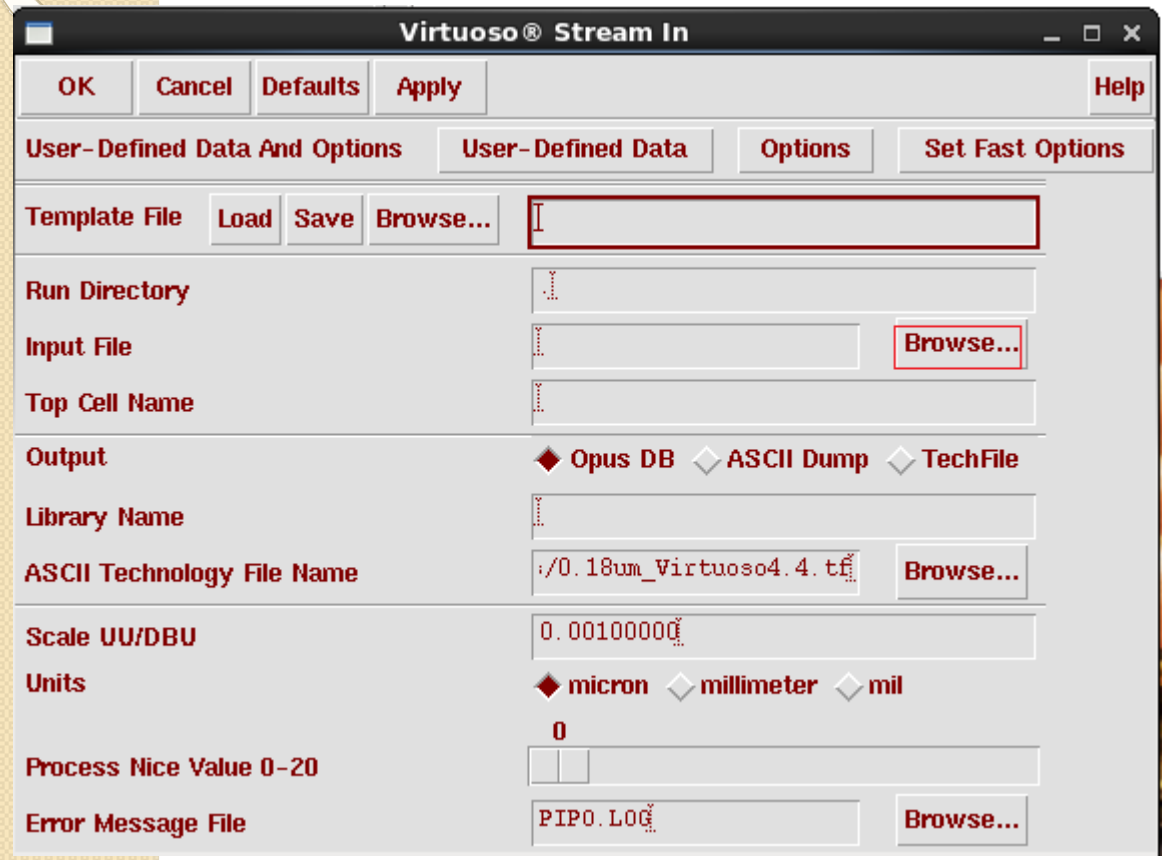

icfb - Log: /home/klsdf/CDS.log
File
Tools
Options
Help
1
New
Open...
Import
Export
Refresh...
Make Read Only...
Close Data...
Defragment Data
Exit...
EDIF 200...
EDIF 300...
Verilog...
VHDL...
CDL...
DEF...
LEF...
Stream...
CIF...
Router ...
Netlist View ...
Virtuoso XL Netlist ...
mouse L:
M:
R:
>

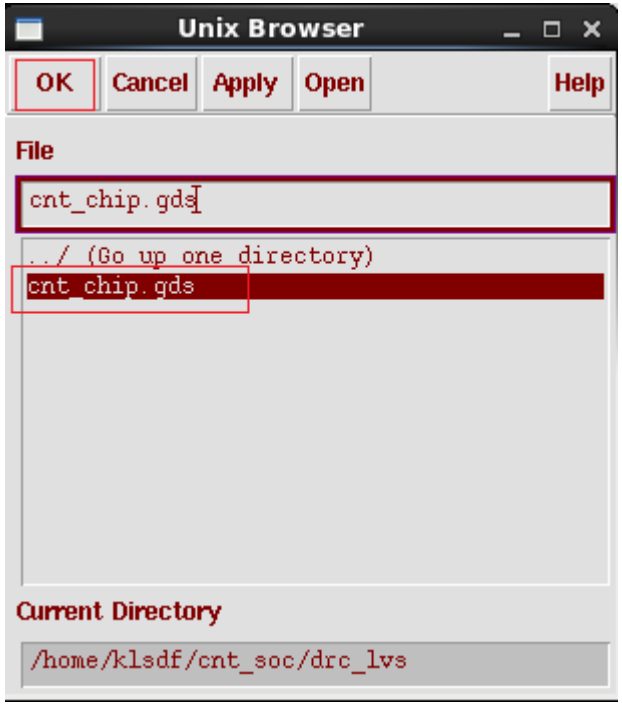
DRC&LVS


Virtuoso® Stream In
OK
Cancel
Defaults
Apply
Help
User-Defined Data And Options
User-Defined Data
Options
Set Fast Options
Template File
Load
Save
Browse...
Run Directory
Input File
Browse...
Top Cell Name
Output
Opus DB
ASCII Dump
TechFile
Library Name
ASCII Technology File Name
Browse...
Scale UU/DBU
0.0010000
Units
micron
millimeter
mil
0
Process Nice Value 0-20
Error Message File
PIPO.LOG
Browse...


Unix Browser
OK
Cancel
Apply
Open
Help
File
0.18um_Virtuoso4.4.tf
../ (Go up one directory)
0.18um_Virtuoso4.4.tf
Current Directory
/home/klsdf/cnt_soc/drc_lvs

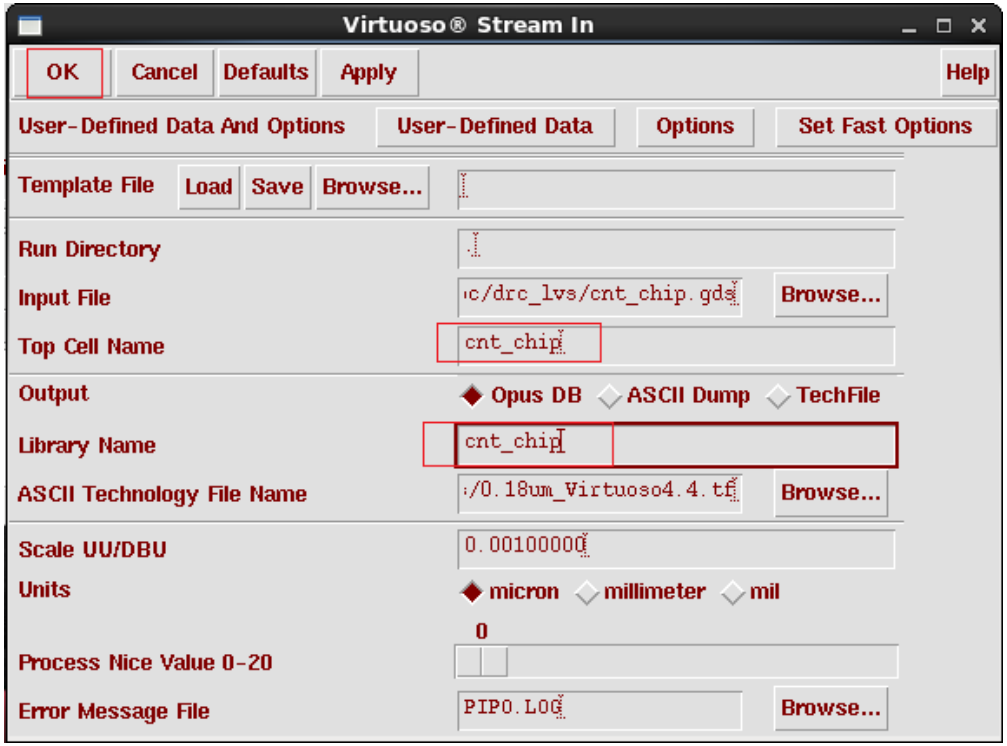
DRC&LVS

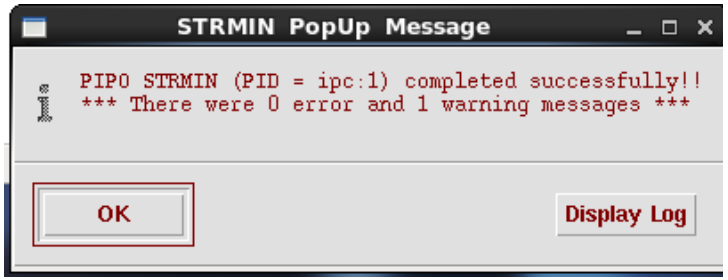

Virtuoso® Stream In
OK
Cancel
Defaults
Apply
Help
User-Defined Data And Options
User-Defined Data
Options
Set Fast Options
Template File
Load
Save
Browse...
Run Directory
Input File
Browse...
Top Cell Name
Output
Opus DB
ASCII Dump
TechFile
Library Name
ASCII Technology File Name
./0.18um_Virtuoso4.4.tf
Browse...
Scale UU/DBU
0.00100000
Units
micron
millimeter
mil
0
Process Nice Value 0-20
Error Message File
PIPO.LOG
Browse...


Unix Browser
OK
Cancel
Apply
Open
Help
File
cnt_chip.gds
../ (Go up one directory)
cnt_chip.gds
Current Directory
/home/klsdf/cnt_soc/drc_lvs

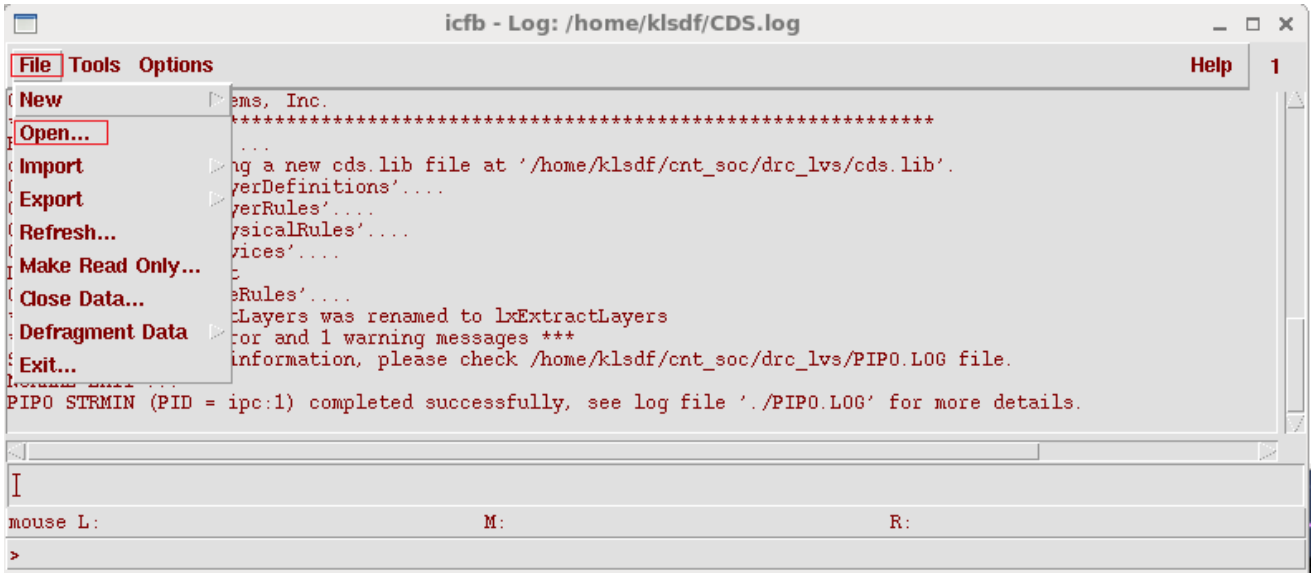
DRC&LVS

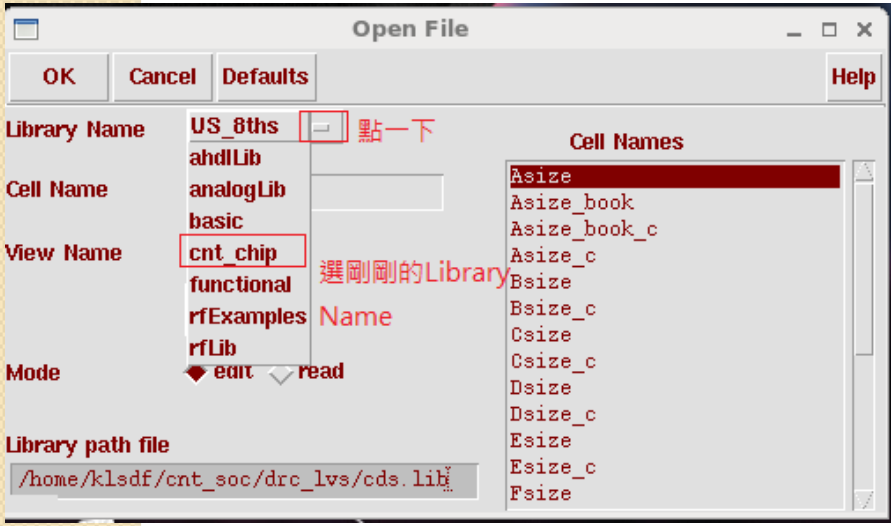
- 按ok後的Warring忽略

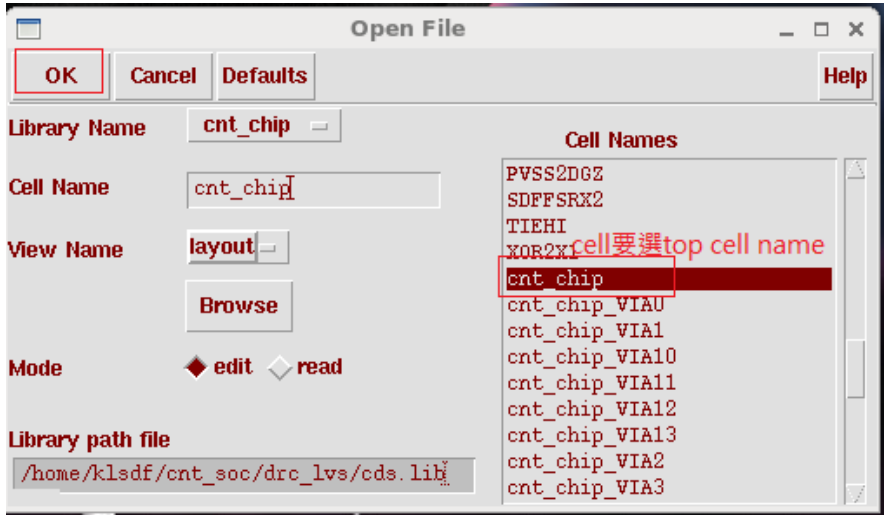




DRC&LVS

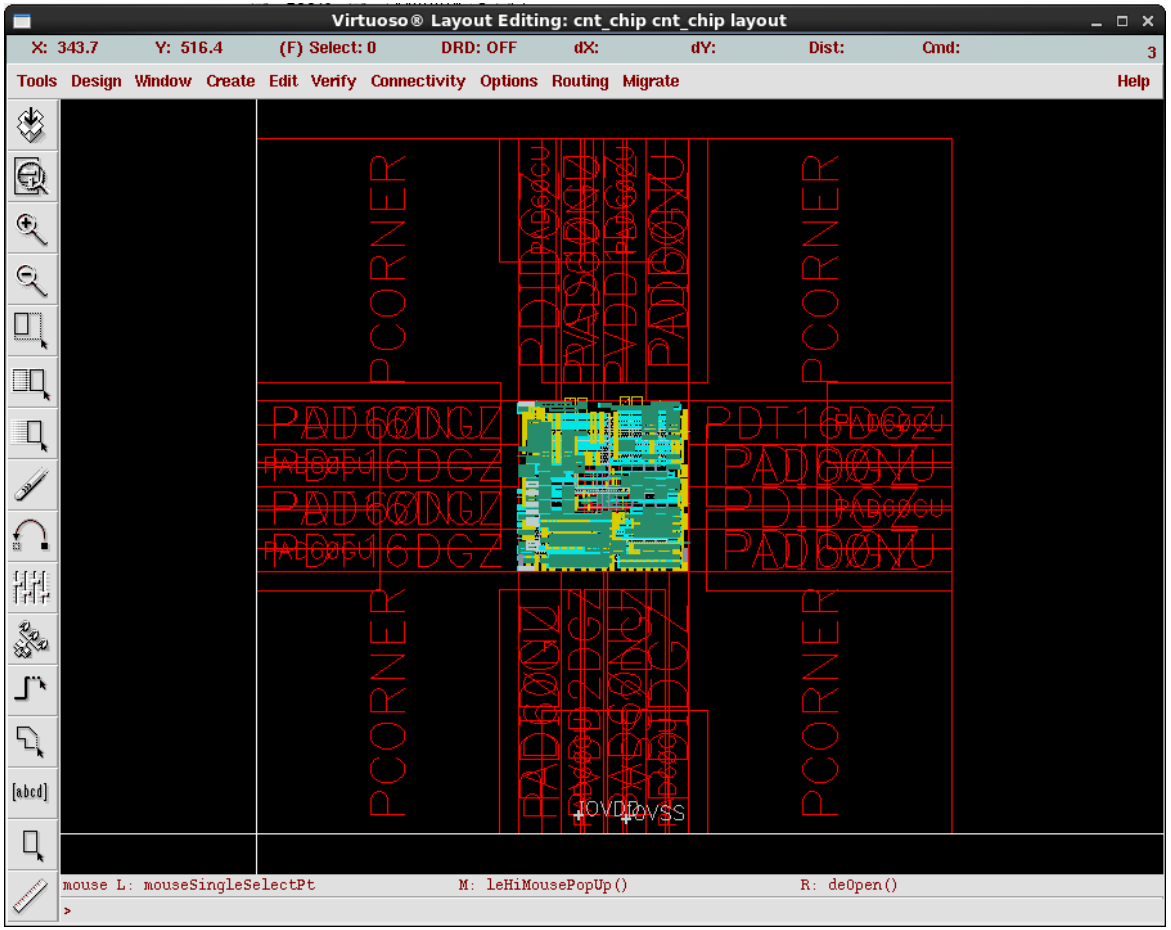

icfb - Log: /home/klsdf/CDS.log
File Tools Options
Help 1
New
Open...
Import
Export
Refresh...
Make Read Only...
Close Data...
Defragment Data
Exit...
ems, Inc.
ng a new cds.lib file at '/home/klsdf/cnt_soc/drc_lvs/cds.lib'.
verDefinitions'....
verRules'....
ysicalRules'....
vices'....
eRules'....
tLayers was renamed to lxExtractLayers
ror and 1 warning messages ***
information, please check /home/klsdf/cnt_soc/drc_lvs/PIPO.LOG file.
PIPO STRMIN (PID = ipc:1) completed successfully, see log file './PIPO.LOG' for more details.
mouse L:
M:
R:
>


Open File
OK
Cancel
Defaults
Help
Library Name
US_8ths
ahdlLib
analogLib
basic
cnt_chip
functional
rfExamples
rfLib
點一下
選剛剛的Library Name
Cell Name
View Name
Mode
edit
read
Cell Names
Asize
Asize_book
Asize_book_c
Asize_c
Bsize
Bsize_c
Csize
Csize_c
Dsize
Dsize_c
Esize
Esize_c
Fsize
Library path file
/home/klsdf/cnt_soc/drc_lvs/cds.lib


Open File
OK
Cancel
Defaults
Help
Library Name
cnt_chip
Cell Name
cnt_chip
View Name
layout
Browse
Mode
edit
read
Cell Names
PVSS2DGZ
SDFFSRX2
TIEHI
XOR2X1
cell要選top cell name
cnt_chip
cnt_chip_VIA0
cnt_chip_VIA1
cnt_chip_VIA10
cnt_chip_VIA11
cnt_chip_VIA12
cnt_chip_VIA13
cnt_chip_VIA2
cnt_chip_VIA3
Library path file
/home/klsdf/cnt_soc/drc_lvs/cds.lib

DRC&LVS

- 可以看到Layout圖，如之後DRC LVS有錯可在此修正，但不在本課程的範圍



DRC&LVS

- 更改目錄下的CLM18_LM16_6M.28a_m.drc內容

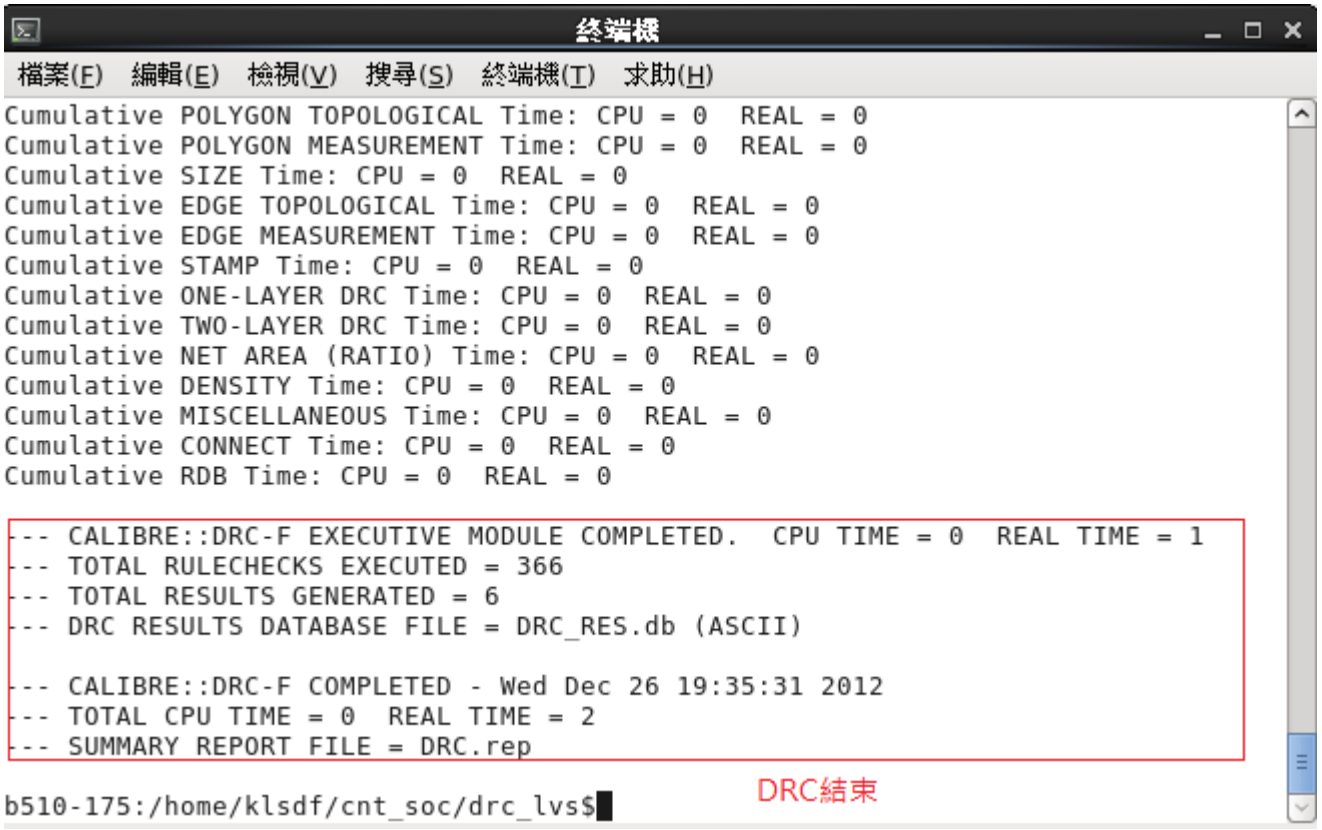
CLM18_LM16_6M.28a_m.drc

```
602
603 //#DEFINE CHECK_LATCHUP_BY_TEXT       // Turn on to recognize IO PAD by following text
604 VARIABLE PAD_TEXT  "?"       // pin name of PAD
605 VARIABLE VDD_TEXT  "AVDDBG" "AVDDR" "AVDWELL" "VDWELL" "VD33APST" "VDD5V" "TAVD33"
    "VD33PST" "AVDD" "TAVDD" "TAVD33PST" "TAVDDPST" "AVD33B" "VDD" "AVD33G" "DVDD" "AVDDG"
    "AVDDB" "VDDG" "VDDPST" "VD33REF" "VD33" "AVD33R" "VDDSA"     // pin name of VDD
606 VARIABLE VSS_TEXT  "VSSPST" "AVS33R" "AVSSUB" "VSSREF" "VSSAPST" "VS33APST" "DVSS"
    "AVS33G" "AVSSBG" "TAVSS" "AVS33B" "AVSSB" "GND" "VSSG" "VSSUB" "VSS" "AVSS" "TAVSSPST"
    "AGND" "AVSSR" "AVSSG"    // pin name of VSS
607
608 #DEFINE CHECK_LATCHUP_BY_PAD_CONNECTION //Turn on to recognize recognize the MOS
    connected to I/O by connection
609
610
611 //
612 // ENVIRONMENT SETUP
613 //------------------
614 PRECISION    1000
615 RESOLUTION     5   //Set layout grid  check to 0.005
616
617 LAYOUT SYSTEM GDSII
618 LAYOUT PATH "cnt_chip.gds"  gds檔名
619 LAYOUT PRIMARY "cnt_chip"  top cell name
620
621 DRC RESULTS DATABASE "DRC_RES.db"
622 DRC SUMMARY REPORT "DRC.rep"
623 DRC CHECK TEXT ALL
624 DRC MAXIMUM RESULTS ALL
625 //DRC INCREMENTAL CONNECT YES
626
627 FLAG OFFGRID YES     // For layout grid check. default grid value is resolution size
628 FLAG ACUTE YES
629 FLAG SKEW YES
630 FLAG NONSIMPLE YES
631
632 LAYOUT PROCESS BOX RECORD YES
633
634
```

DRC&LVS

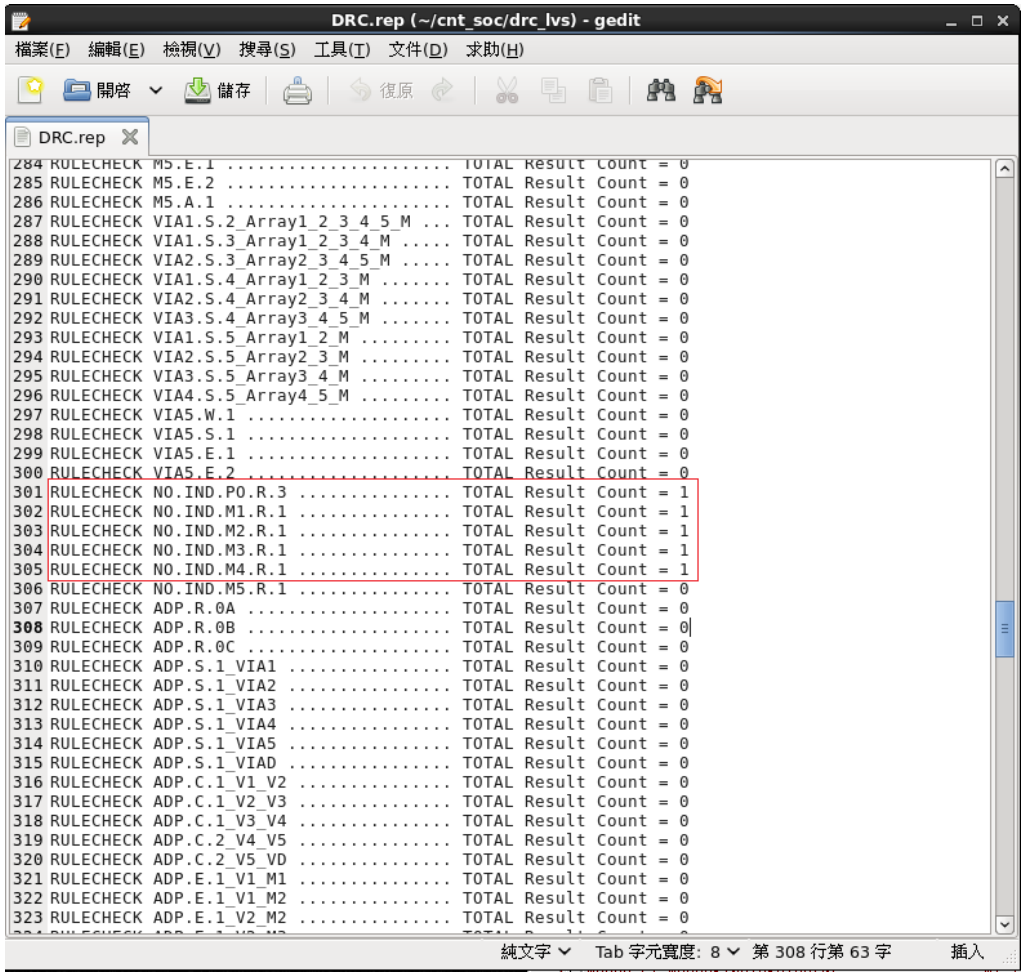
- Terminal執行drc

calibre -drc CLM18_LM16_6M.28a_m.drc



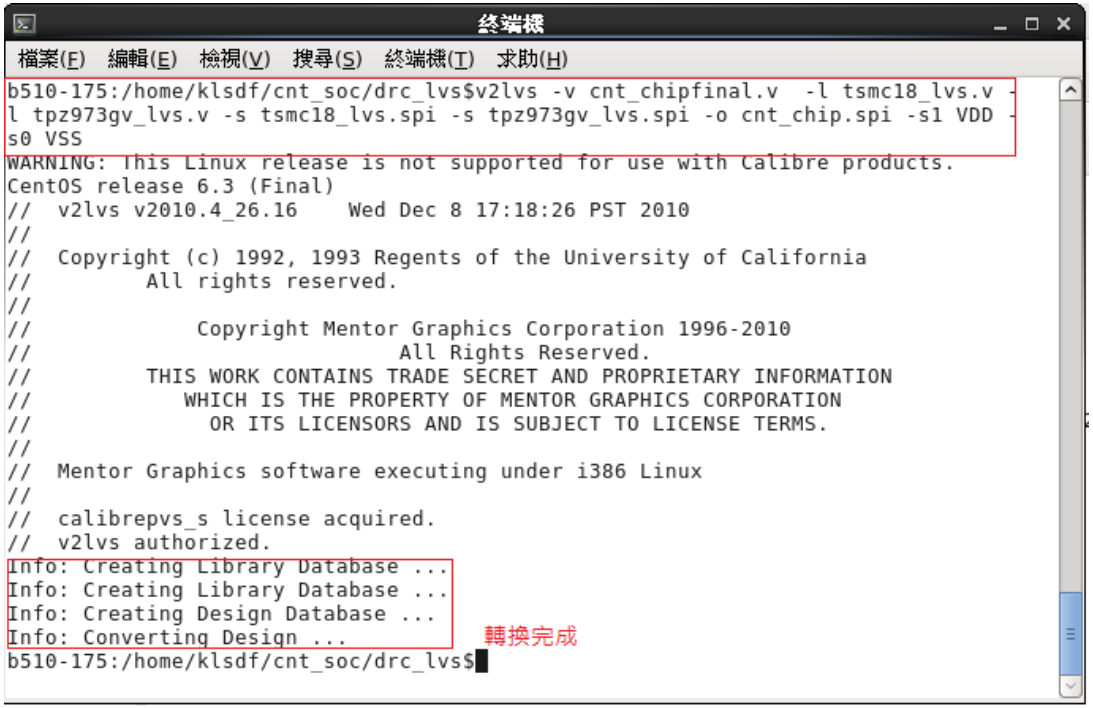
DRC&LVS

- 觀看DRC.rep ，圖中這幾個DRC ERROR指的是Metal 及Poly的density不足，可以不必理會，如有其他的就需要修正。



DRC&LVS

- 將Verilog Netlist File轉成Spice格式才能做lvs
- 將之前encounter的netlistfinal的.v檔放入此資料夾後打入以下指令
- v2lvs –v netlistfinalname.v –l tsmc18_lvs.v –l tpz973gv_lvs.v –s tsmc18_lvs.spi –s tpz973gv_lvs.spi –o outputfilename.spi –s1 VDD –s0 VSS



DRC&LVS

- 修改目錄下的Calibre.lvs

Calibre.lvs

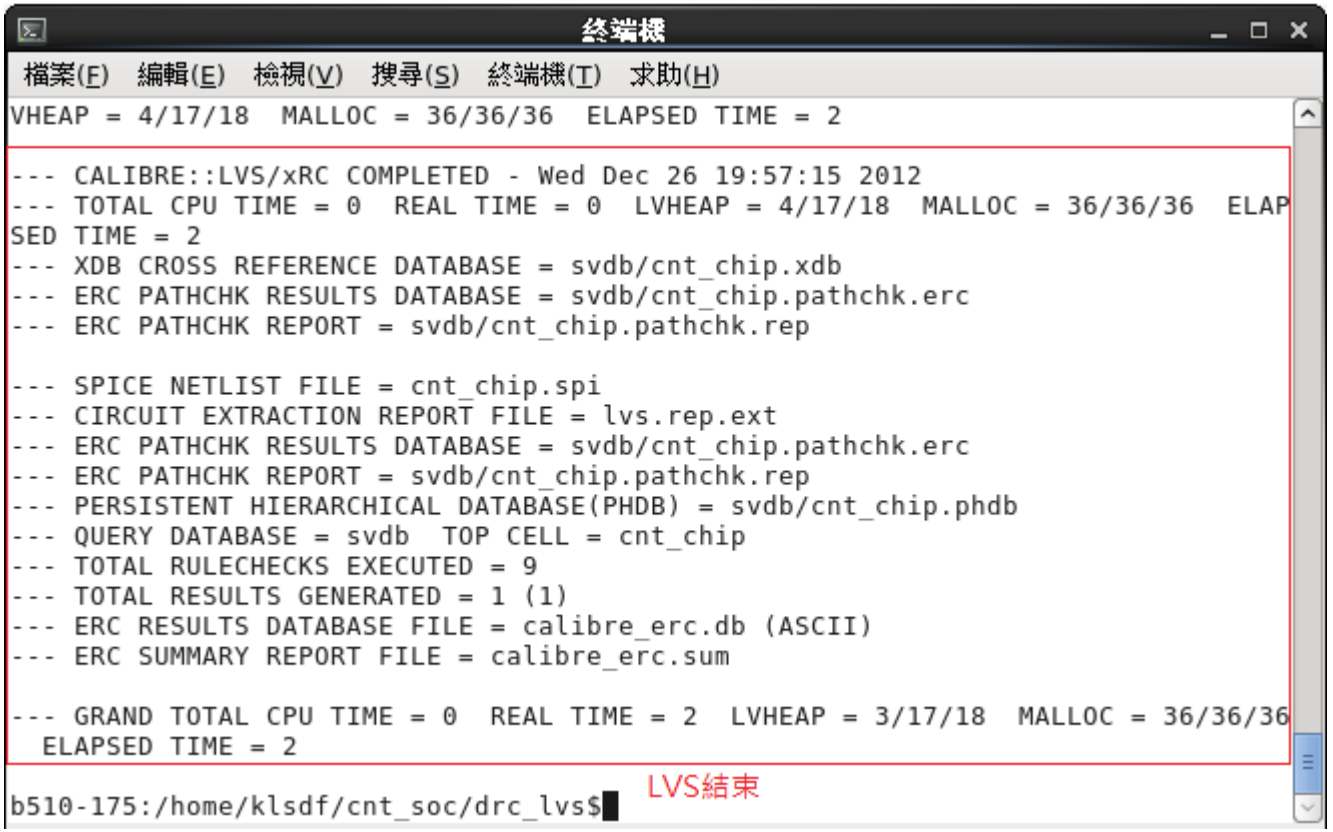
```
388     VARIABLE    MIM_CF  .2425          //  Mimcap Perimeter Cap
389     VARIABLE    MIM_CA_2P0  1.955      //  Mimcap_2p0 Area Cap.
390     VARIABLE    MIM_CF_2P0  .27        //  Mimcap_2p0 Perimeter Cap
391
392
393 //#load table_rsf_cal // load table values here
394
395 LVS HEAP DIRECTORY "/tmp"
396 //#DEFINE CAP_2P0
397
398 //#DEFINE extract_dnwdio
399 //#DEFINE ACCURACY
400
401 #IFDEF RC_DECK
402  #DEFINE ACCURACY
403 #ENDIF
404
405 LAYOUT CASE YES 新增
406 LAYOUT PRIMARY "cnt_chip" Top Cell Name
407 LAYOUT PATH "cnt_chip.gds" GDS FileName
408 LAYOUT SYSTEM GDSII
409 //LAYOUT PATH "layout.net"
410 //LAYOUT SYSTEM SPICE
411 SOURCE CASE YES 新增
412 SOURCE PRIMARY "cnt_chip" Top Cell Name
413 SOURCE PATH "cnt_chip.spi" 剛剛轉出來的spi檔名
414 SOURCE SYSTEM SPICE
415
416 DRC RESULTS DATABASE "calibre_drc.db" ASCII // ASCII or GDSII
417 DRC SUMMARY REPORT "calibre_drc.sum"
418
419 ERC RESULTS DATABASE "calibre_erc.db" ASCII
420 ERC SUMMARY REPORT "calibre_erc.sum"
421
422 LVS REPORT "lvs.rep"
423 LVS REPORT MAXIMUM 1000 // ALL
424
425 #IFDEF RC_DECK
```

Calibre.lvs

```
4664 LVS BOX   PRD12SDGZ
4665 LVS BOX   PRD16DGZ
4666 LVS BOX   PRD16SDGZ
4667 LVS BOX   PRD24DGZ
4668 LVS BOX   PRD24SDGZ
4669 LVS BOX   PRDW08DGZ
4670 LVS BOX   PRDW12DGZ
4671 LVS BOX   PRDW16DGZ
4672 LVS BOX   PRDW24DGZ
4673 LVS BOX   PRO08CDG
4674 LVS BOX   PRO12CDG
4675 LVS BOX   PRO16CDG
4676 LVS BOX   PRO24CDG
4677 LVS BOX   PRT08DGZ
4678 LVS BOX   PRT12DGZ
4679 LVS BOX   PRT16DGZ
4680 LVS BOX   PRT24DGZ
4681 LVS BOX   PRU08DGZ
4682 LVS BOX   PRU08SDGZ
4683 LVS BOX   PRU12DGZ
4684 LVS BOX   PRU12SDGZ
4685 LVS BOX   PRU16DGZ
4686 LVS BOX   PRU16SDGZ
4687 LVS BOX   PRU24DGZ
4688 LVS BOX   PRU24SDGZ
4689 LVS BOX   PRUW08DGZ
4690 LVS BOX   PRUW12DGZ
4691 LVS BOX   PRUW16DGZ
4692 LVS BOX   PRUW24DGZ
4693 //LVS BOX   PVDD1ANA
4694 //LVS BOX   PVDD1DGZ
4695 //LVS BOX   PVDD2ANA
4696 //LVS BOX   PVDD2DGZ    全部註解
4697 //LVS BOX   PVDD2POC
4698 //LVS BOX   PVSS1ANA
4699 //LVS BOX   PVSS1DGZ
4700 //LVS BOX   PVSS2ANA
4701 //LVS BOX   PVSS2DGZ
4702 //LVS BOX   PVSS3DGZ
```

DRC&LVS

- 執行lvs
- calibre -lvs -spice spicefilename.spi -hier -auto Calibre.lvs



DRC&LVS

- 觀看lvs.rep，看到笑臉即驗證完成。