



# ASIC教材

## Chapter5 Innovus檔案載入

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B510實驗室

2018.07



# 目錄

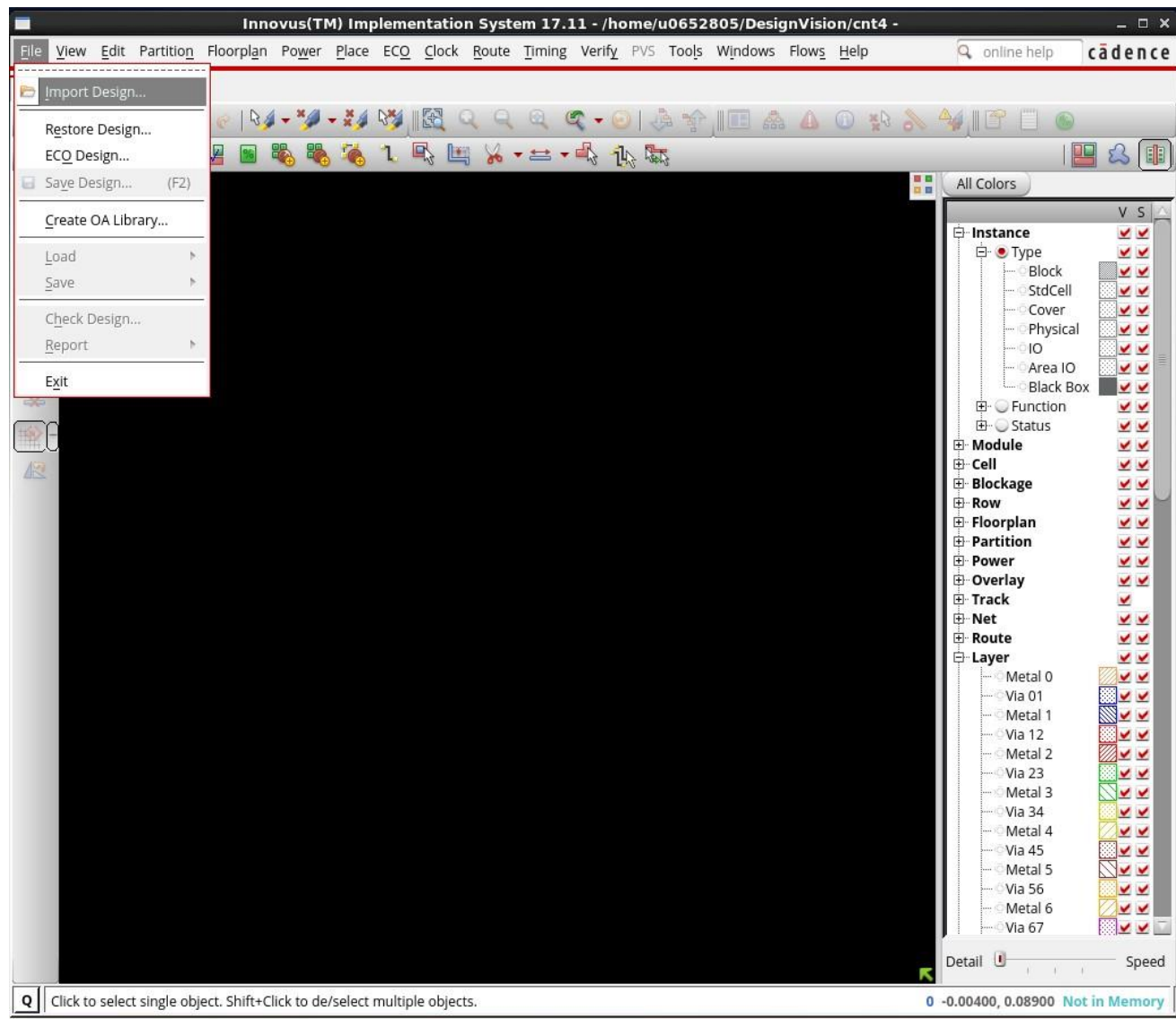
使用Innovus

# 使用Innovus

在家目錄下新增一個cnt\_soc資料夾，把第四章節所準備的.v .sdc .ioc檔放入這個資料夾後執行Innovus。

[illegible]

# 使用Innovus



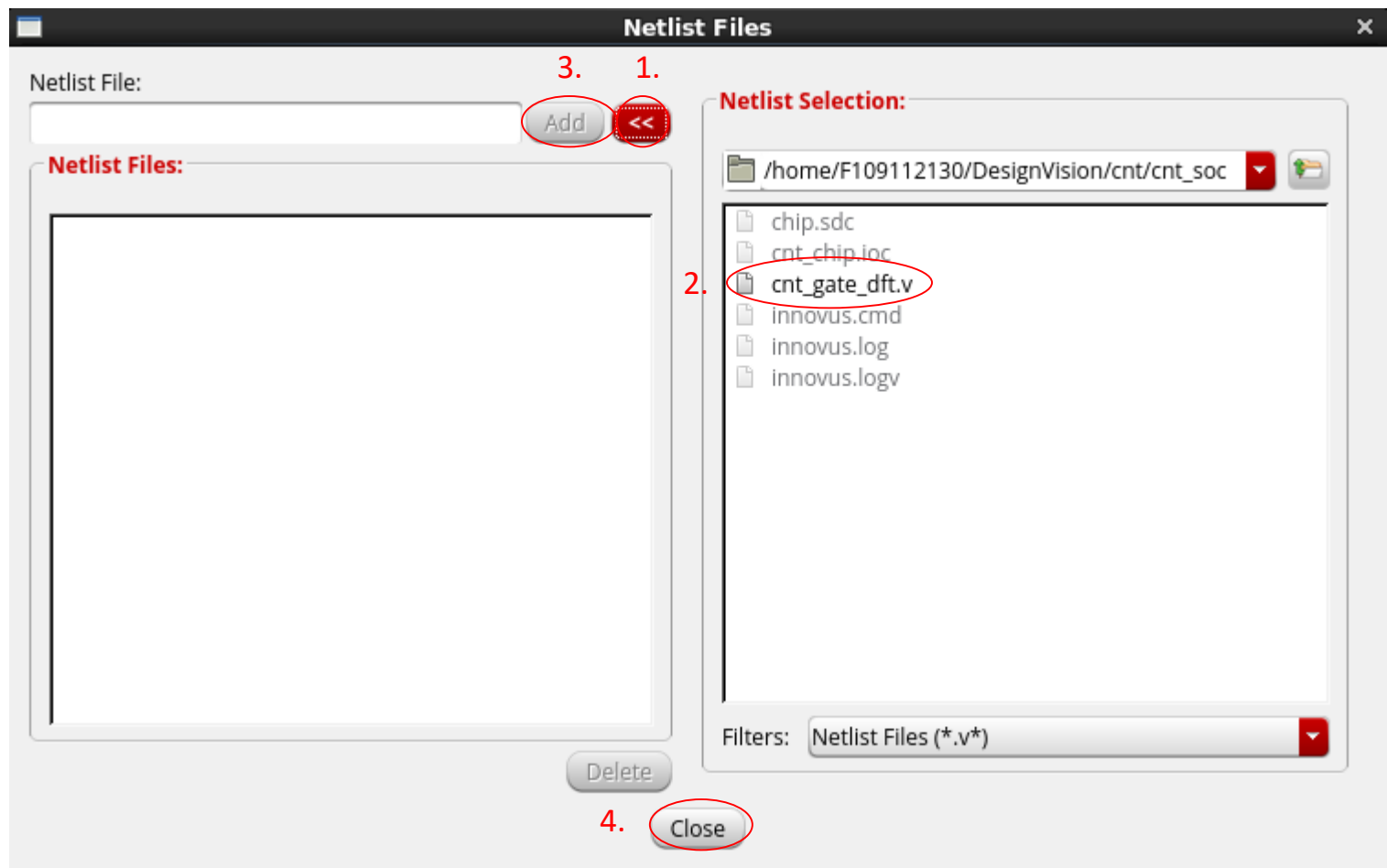
# 使用Innovus

The screenshot shows the 'Design Import' dialog box with the following sections and options:

- Netlist:**
  - ☒ Verilog (with a red annotation '點選載入.v檔' and a circled ellipsis button)
  - ☐ OA
  - Files: [text field]
  - Top Cell: ☐ Auto Assign ☒ By User: [text field]
  - Library: [dropdown menu]
  - Cell: [dropdown menu]
  - View: [dropdown menu]
- Technology/Physical Libraries:**
  - ☐ OA
    - Reference Libraries: [text field]
    - Abstract View Names: [text field]
    - Layout View Names: [text field]
  - ☒ LEF Files [text field]
- Floorplan**
  - IO Assignment File: [text field]
- Power**
  - Power Nets: [text field]
  - Ground Nets: [text field]
  - CPF File: [text field]
- Analysis Configuration**
  - MMMC View Definition File: [text field]
  - Create Analysis Configuration ... [button]

At the bottom are buttons for **OK**, **Save...**, **Load...**, **Cancel**, and **Help**.

# 使用Innovus



# 使用Innovus

**Design Import**

**Netlist:**

☒ Verilog

Files: cnt\_gate\_dft.v ...

Top Cell: ☐ Auto Assign ☒ By User: cnt\_chip

☐ OA

Library: ...

Cell: ...

View: ...

**Technology/Physical Libraries:**

☒ OA

Reference Libraries: ...

Abstract View Names: ...

Layout View Names: ...

☐ LEF Files ...

**Floorplan**

IO Assignment File: ...

**Power**

Power Nets: ...

Ground Nets: ...

CPF File: ...

**Analysis Configuration**

MMMC View Definition File: ...

Create Analysis Configuration ...

**OK** **Save...** **Load...** **Cancel** **Help**

# 使用Innovus

The screenshot shows the 'Design Import' dialog box with the following sections:

- Netlist:**
  - ☒ Verilog
    - Files: cnt\_gate\_dft.v
    - Top Cell: ☐ Auto Assign ☒ By User: cnt\_chip
  - ☐ OA
    - Library:
    - Cell:
    - View:
- Technology/Physical Libraries:**
  - ☐ OA
    - Reference Libraries:
    - Abstract View Names:
    - Layout View Names:
  - ☒ LEF Files
    - c.lef /usr/techfile/CBDK\_TSMC018\_Arm\_v4.0/CIC/SOCE/lef/antenna.lef
- Floorplan:**
  - IO Assignment File:
- Power:**
  - Power Nets:
  - Ground Nets:
  - CPF File:
- Analysis Configuration:**
  - MMMC View Definition File:
  - Create Analysis Configuration ...

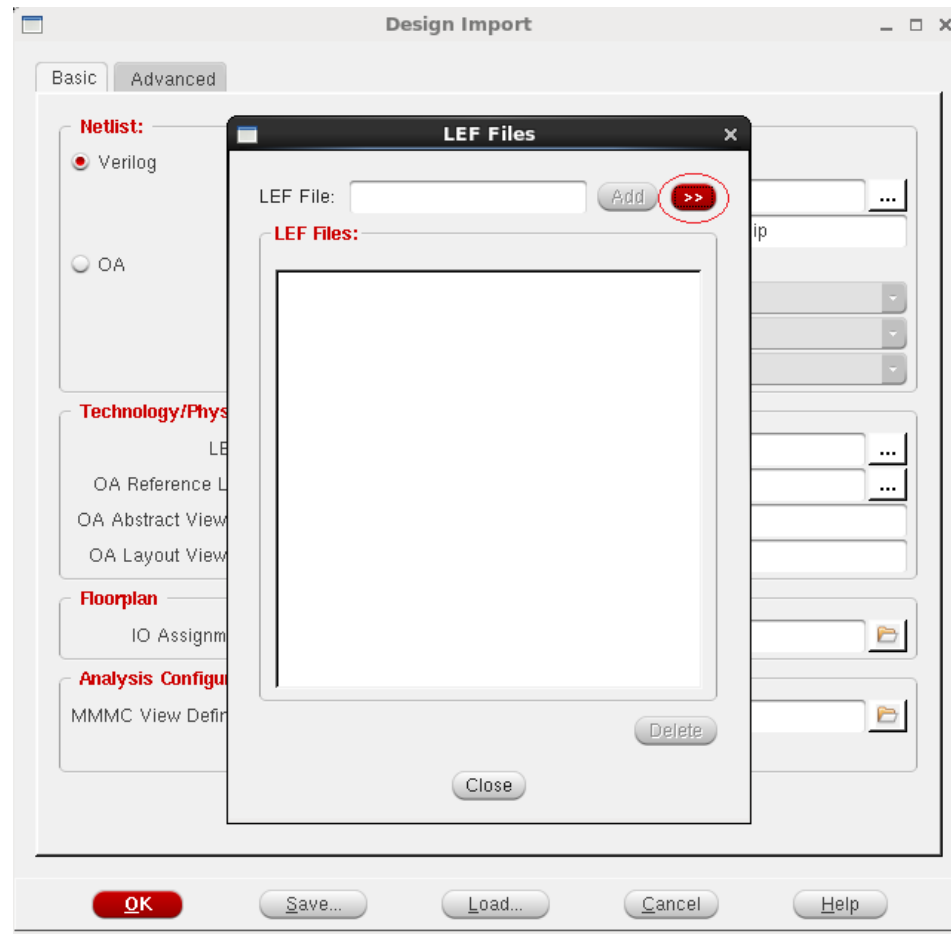
At the bottom are buttons: **OK**, **Save...**, **Load...**, **Cancel**, and **Help**.

1.

2. 載入製成檔案



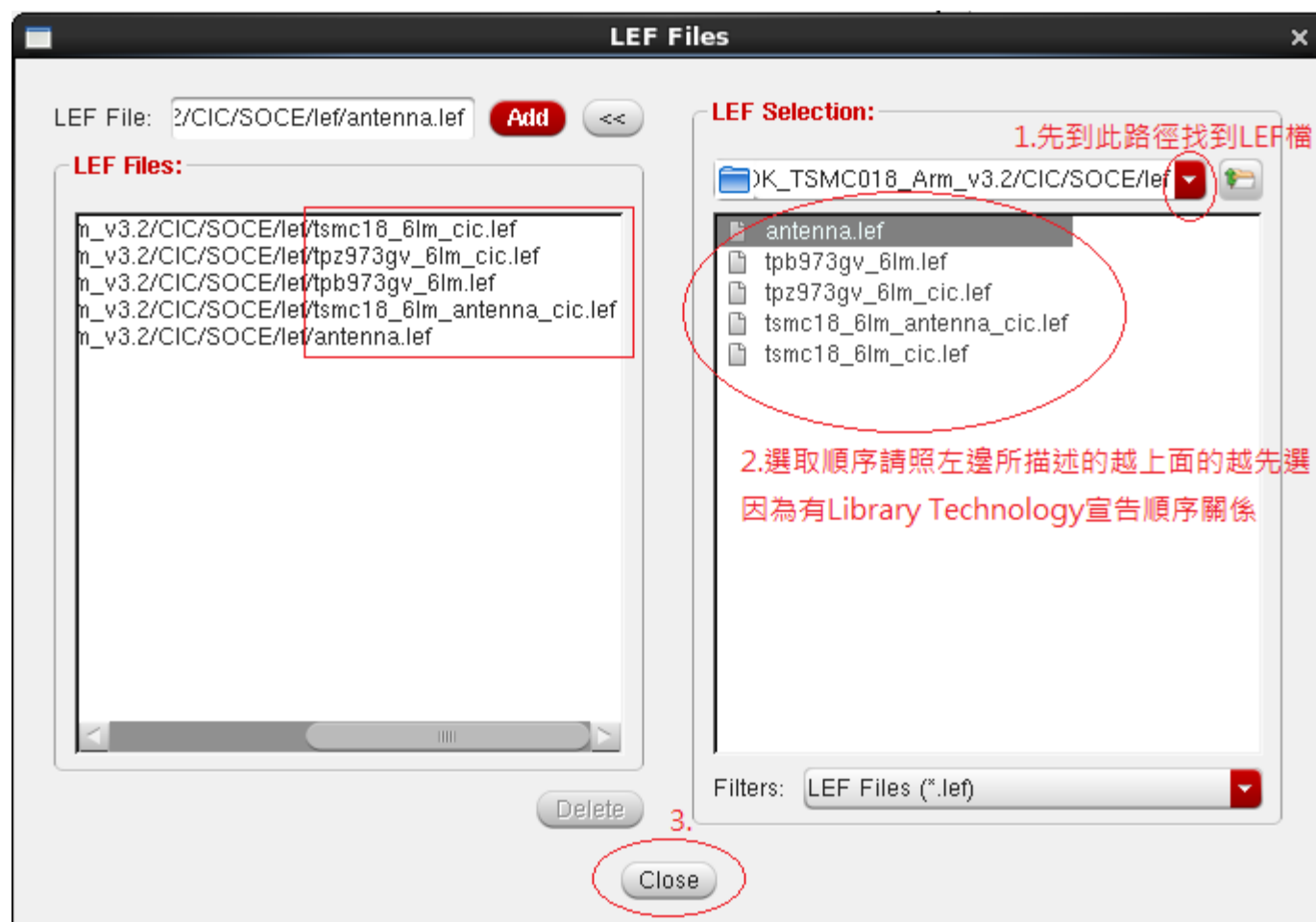
# 使用Innovus



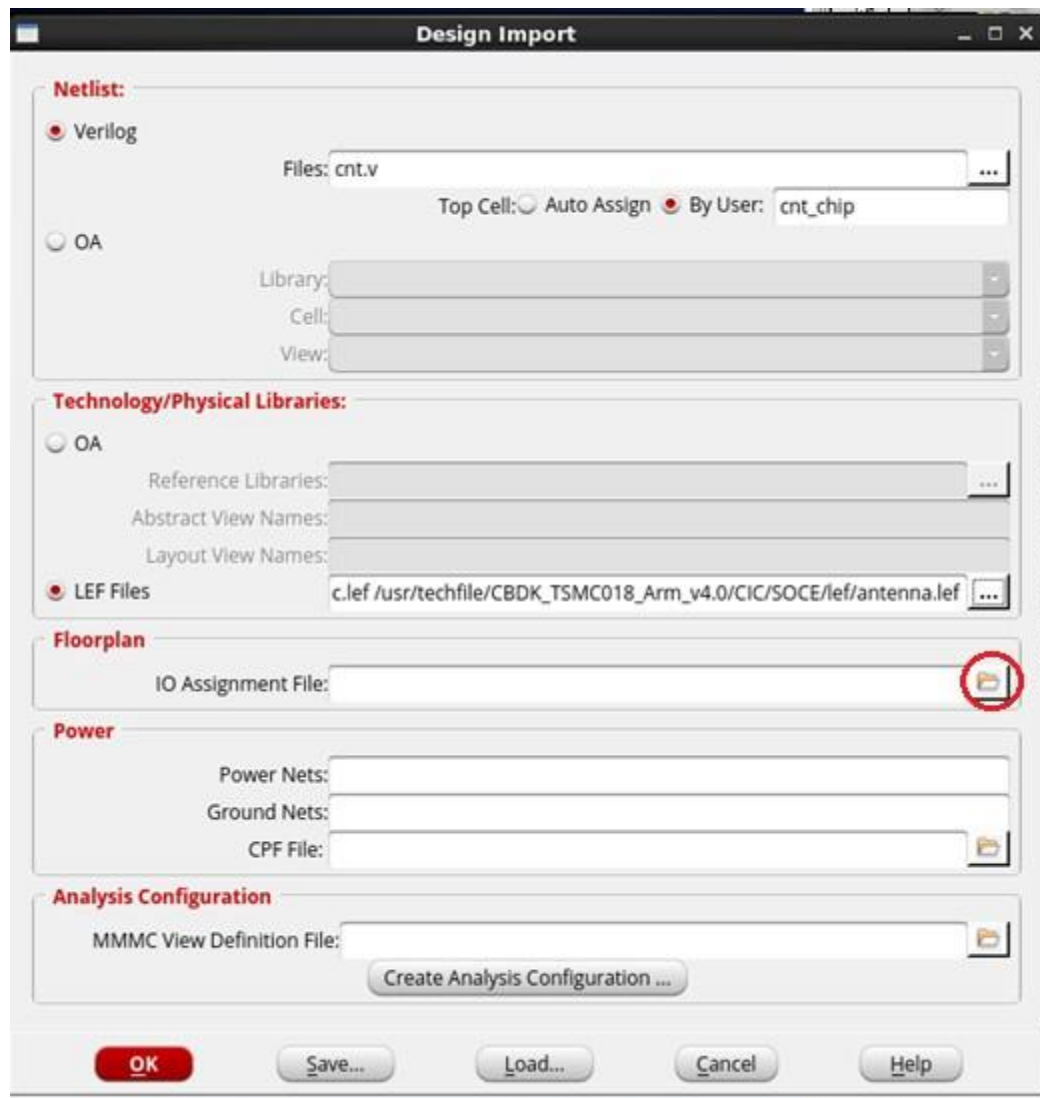
# 使用Innovus

LEF檔案路徑在

**/usr/techfile/CBDK\_TSMC018\_Arm\_v4.0/CIC/SOCE/lef**



# 使用Innovus



# 使用Innovus



# 使用Innovus

**Design Import**

**Netlist:**

☒ Verilog

Files: cnt\_gate\_dft.v

Top Cell: ☐ Auto Assign ☒ By User: cnt\_chip

☐ OA

Library:

Cell:

View:

**Technology/Physical Libraries:**

☐ OA

Reference Libraries:

Abstract View Names:

Layout View Names:

☒ LEF Files

c.lef /usr/techfile/CBDK\_TSMC018\_Arm\_v4.0/CIC/SOCE/lef/antenna.lef

**Floorplan**

IO Assignment File: cnt\_chip.ioc

**Power**

Power Nets: VDD

Ground Nets: VSS

CPF File:

**Analysis Configuration**

MMMC View Definition File:

Create Analysis Configuration ...

**Buttons:** OK, Save..., Load..., Cancel, Help

# 使用Innovus

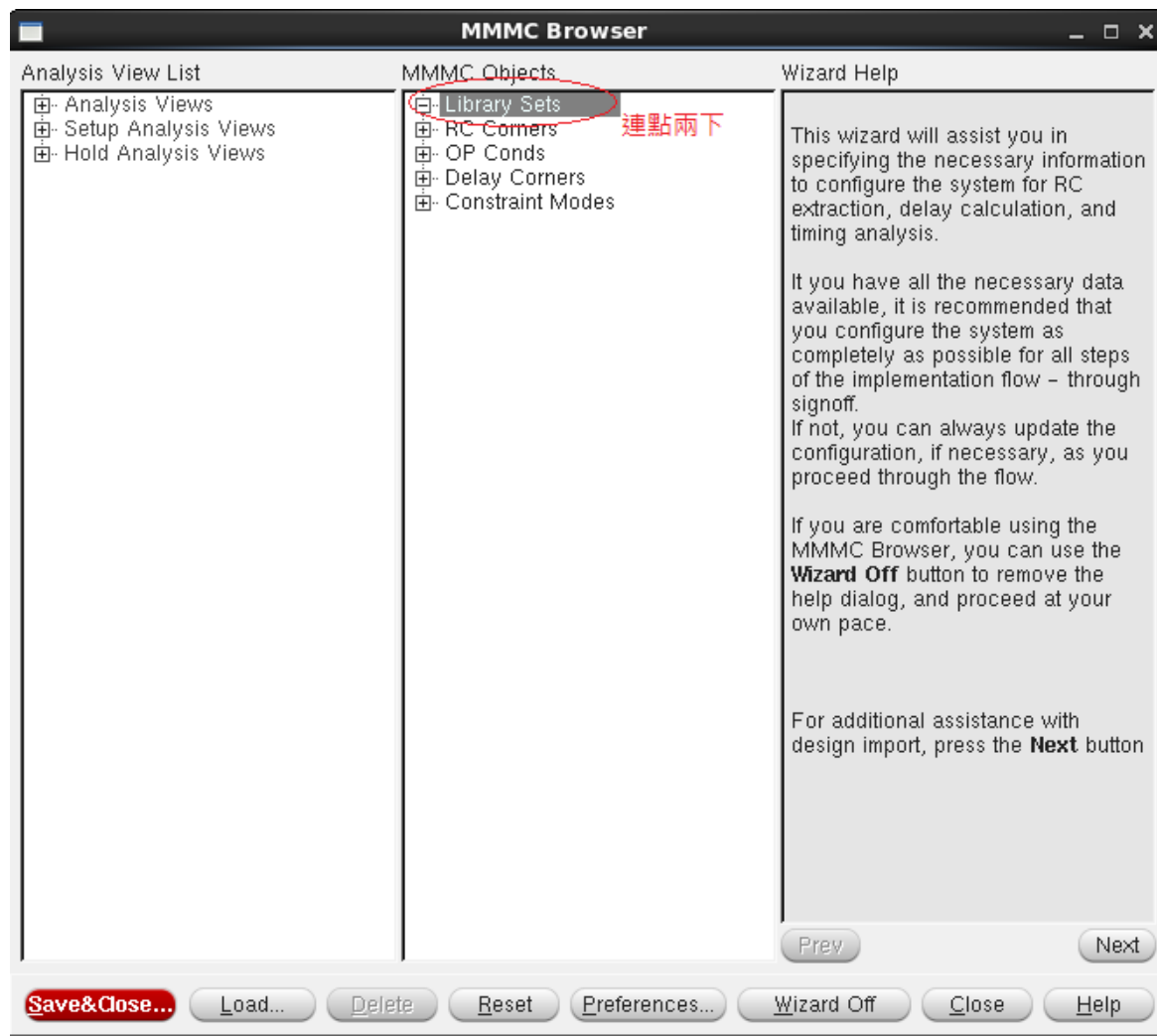
The screenshot shows the 'Design Import' dialog box with the following sections and fields:

- Netlist:**
  - ☒ Verilog
    - Files: cnt\_gate\_dft.v
    - Top Cell: ☐ Auto Assign ☒ By User: cnt\_chip
  - ☐ OA
    - Library:
    - Cell:
    - View:
- Technology/Physical Libraries:**
  - ☐ OA
    - Reference Libraries:
    - Abstract View Names:
    - Layout View Names:
  - ☒ LEF Files
    - c.lef /usr/techfile/CBDK\_TSMC018\_Arm\_v4.0/CIC/SOCE/lef/antenna.lef
- Floorplan**
  - IO Assignment File: cnt\_chip.ioc
- Power**
  - Power Nets: VDD
  - Ground Nets: VSS
  - CPF File:
- Analysis Configuration**
  - MMMC View Definition File:
  - Create Analysis Configuration ...** (highlighted with a red circle)

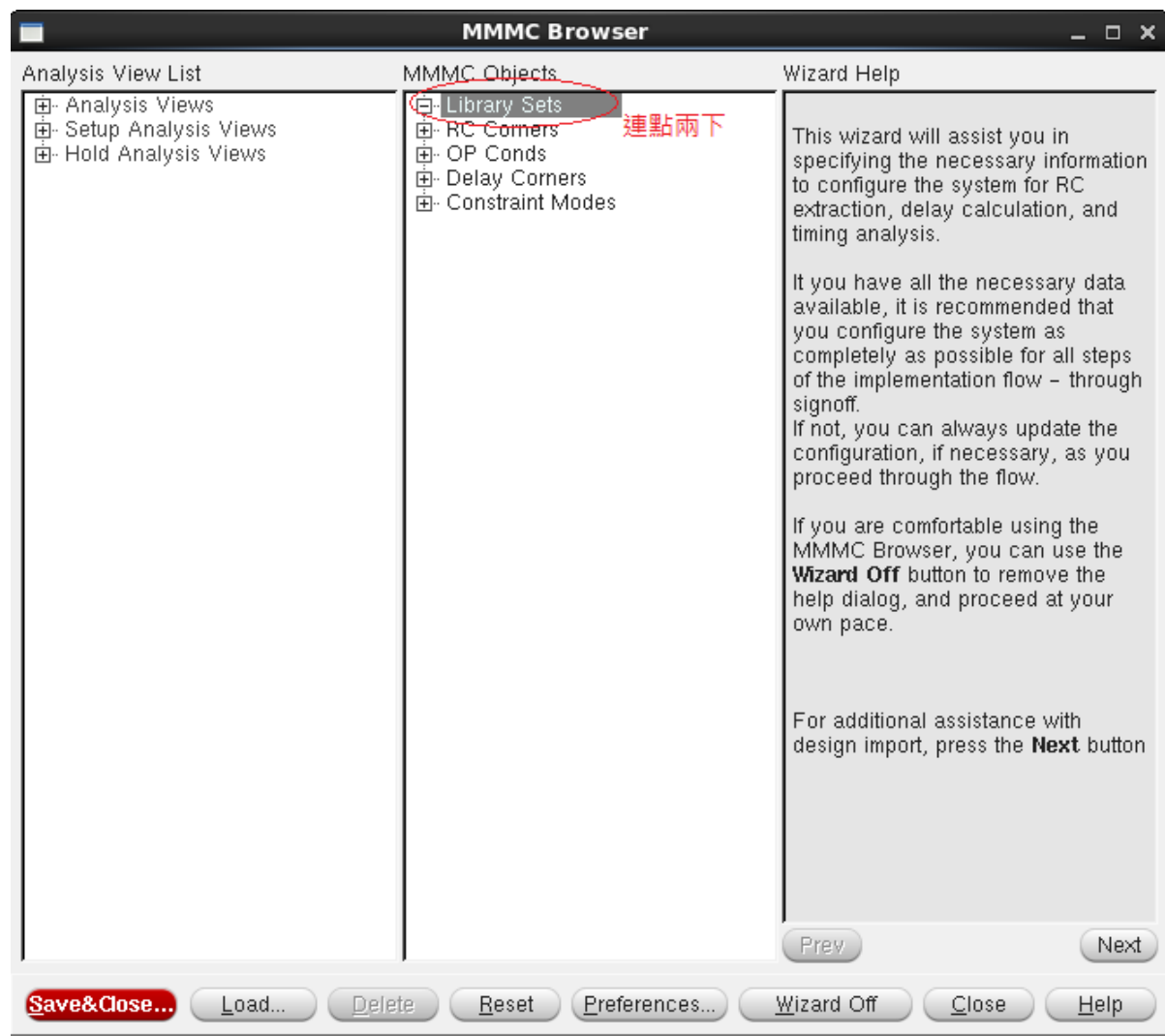
At the bottom of the dialog are buttons for **OK**, **Save...**, **Load...**, **Cancel**, and **Help**.

# 使用Innovus

## 新增Timing Library Set

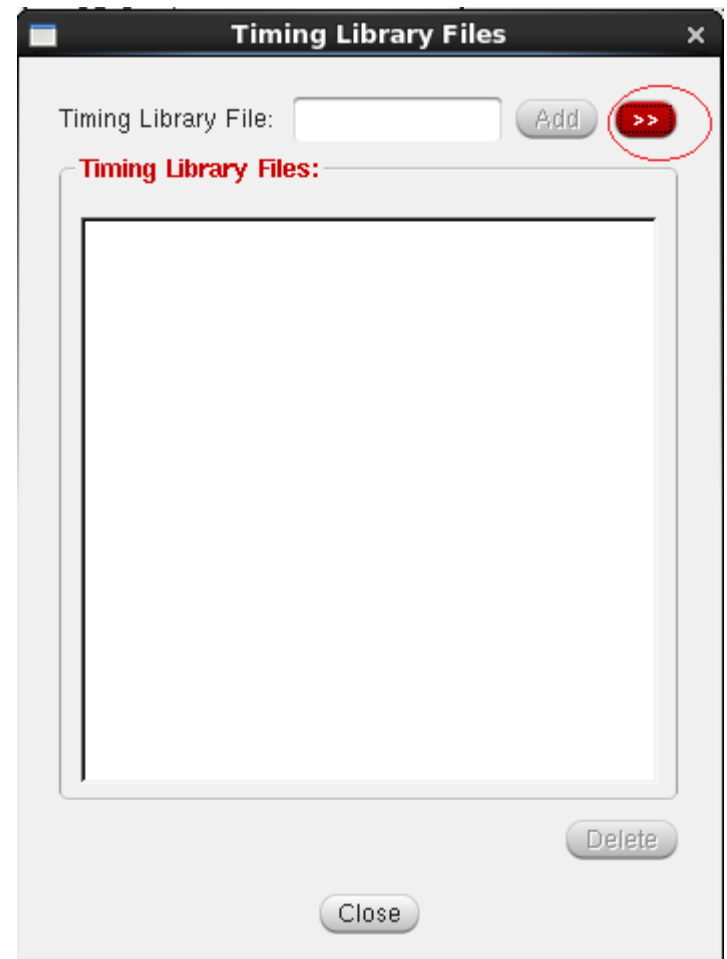
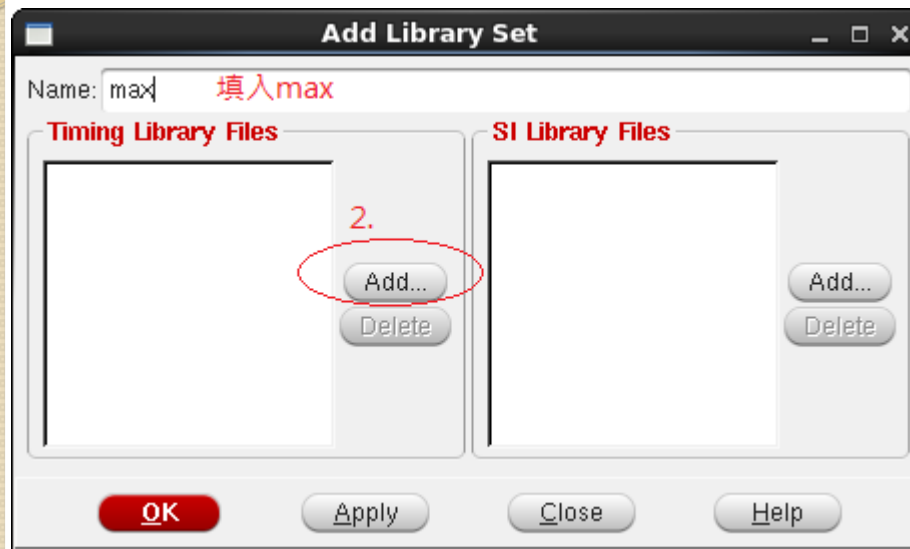


# 使用Innovus





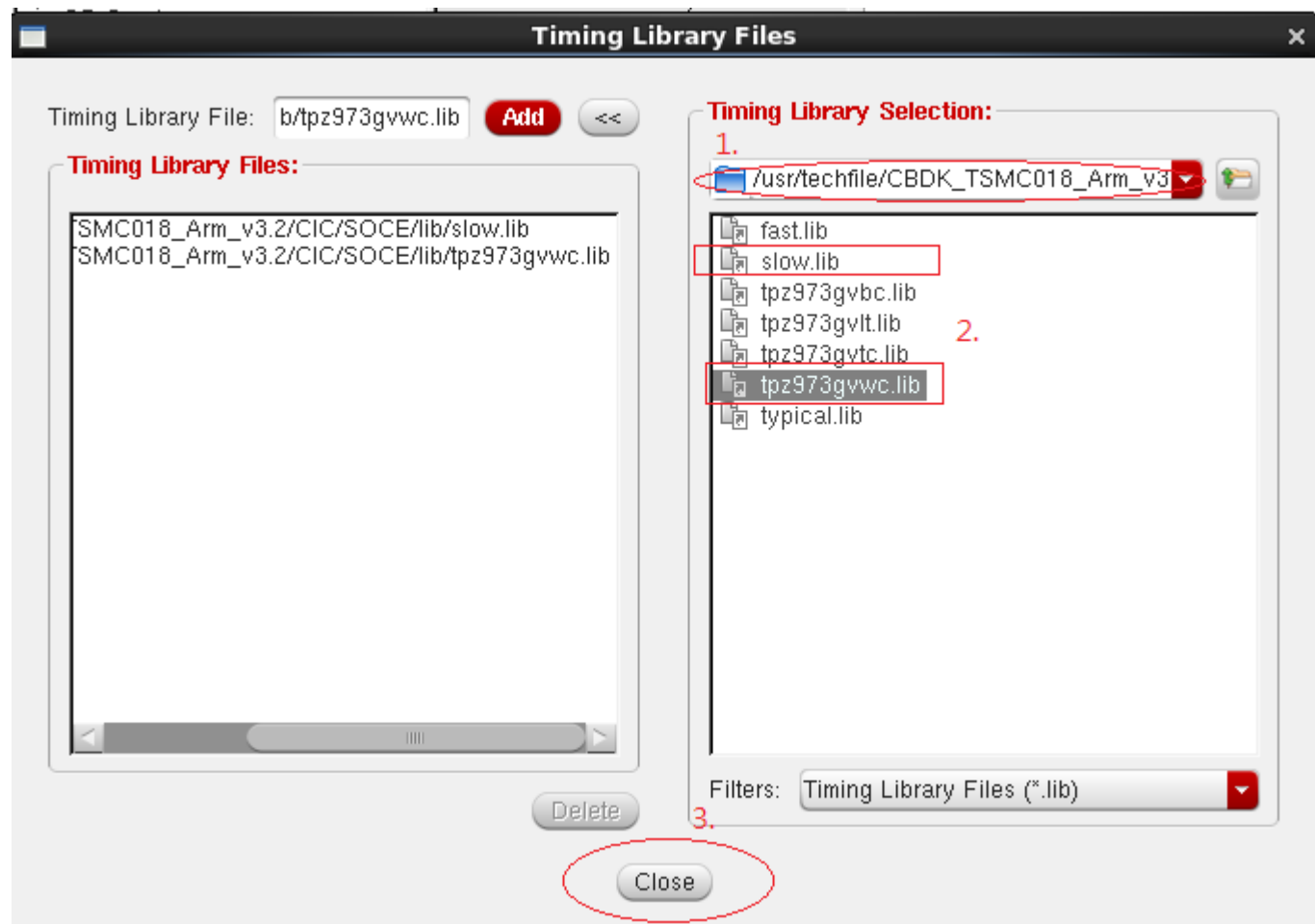
# 使用Innovus



# 使用Innovus

Timing Library 路徑在

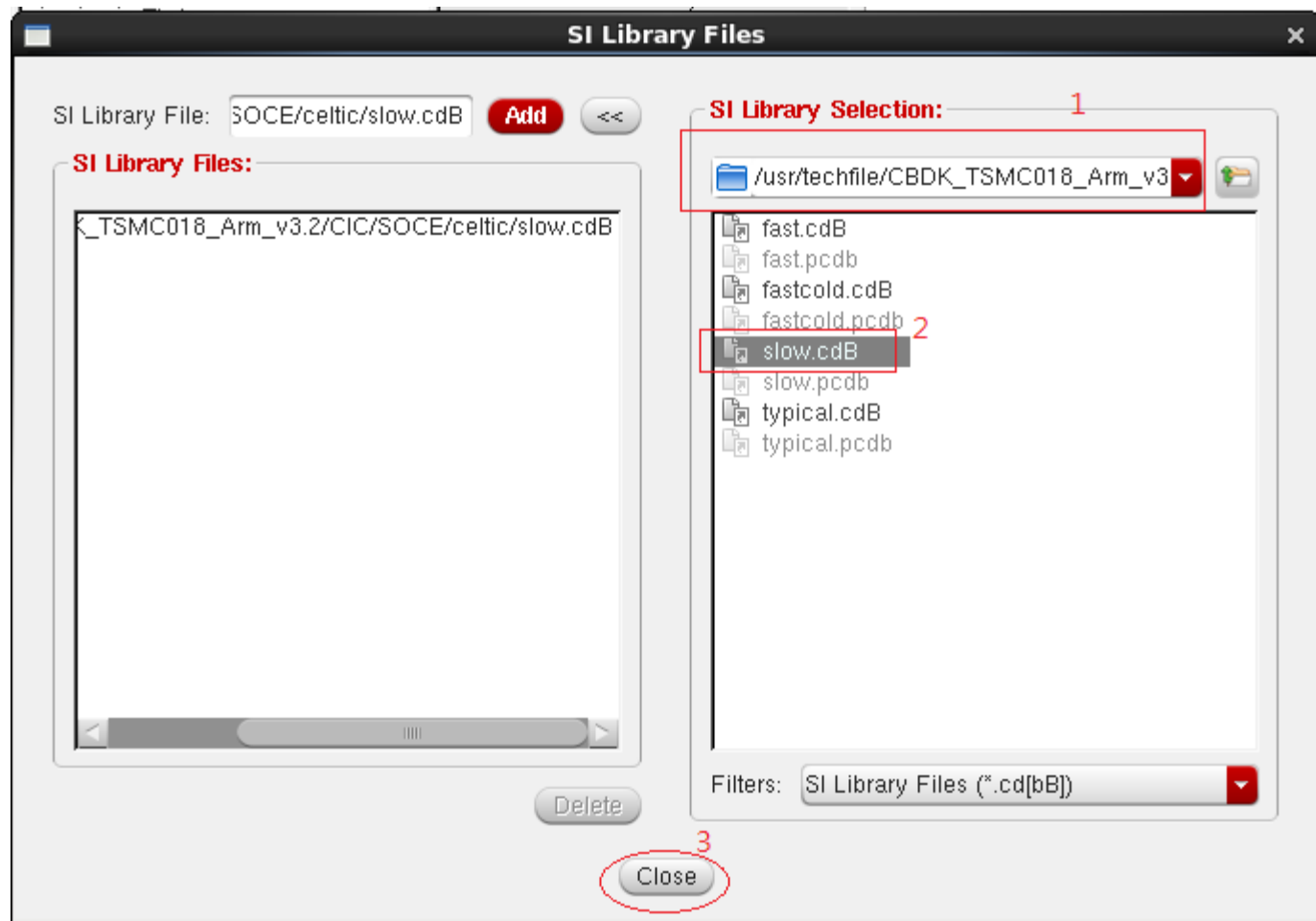
**/usr/techfile/CBDK\_TSMC018\_Arm\_v4.0/CIC/SOCE/lib**



# 使用Innovus

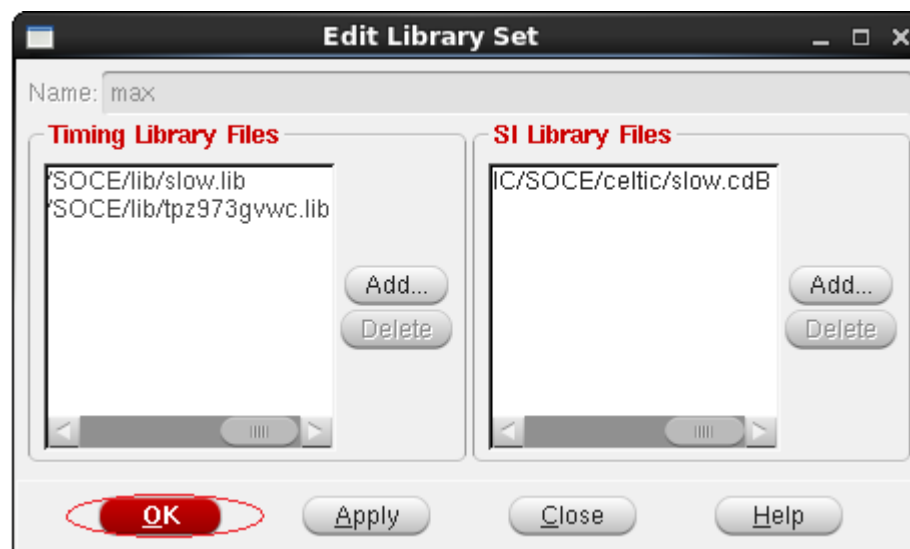
SI Library 路徑在

`/usr/techfile/CBDK_TSMC018_Arm_v3.2/CIC/SOCE/celtic`



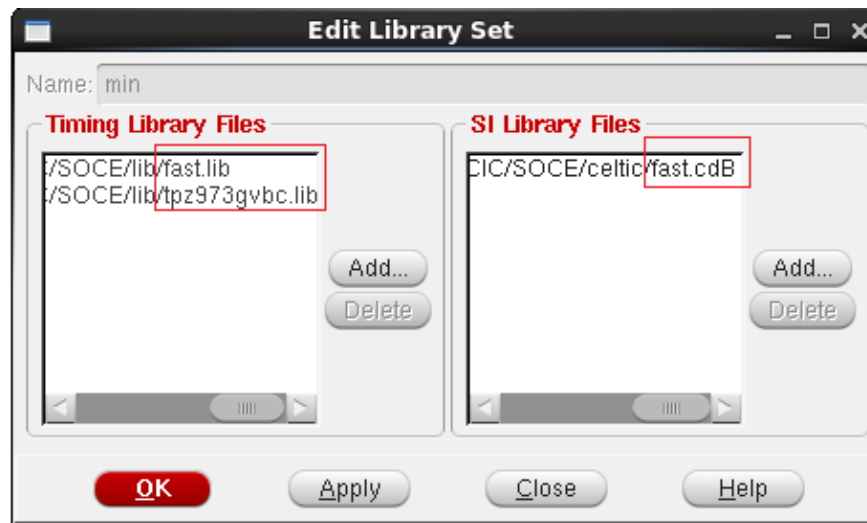
# 使用Innovus

按OK新增。

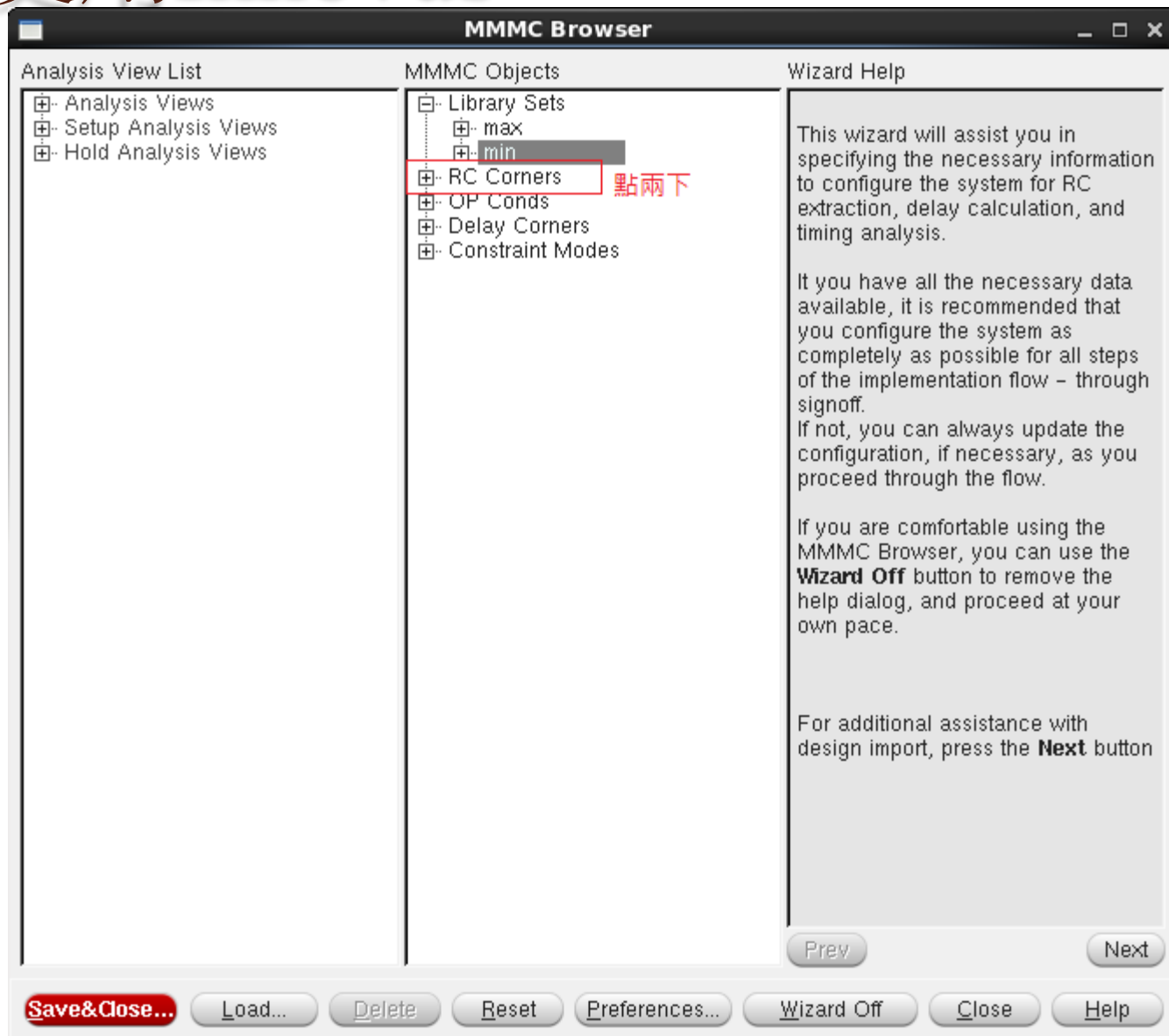


# 使用Innovus

重複以上步驟新增min。



# 使用Innovus



# 使用Innovus

## 新增Cap Table

**Add RC Corner**

Name: RC\_Corner

Cap Table: 1.先填入RC\_Corner

Temperature:

PreRoute Resistance Scale Factor: 1.0

PreRoute Cap Scale Factor: 1.0

PreRoute Clock Resistance Scale Factor: 0.0

PreRoute Clock Cap Scale Factor: 0.0

PostRoute Resistance Scale Factor: 1.0

PostRoute Cap Scale Factor: 1.0

PostRoute Xcap Scale Factor: 1.0

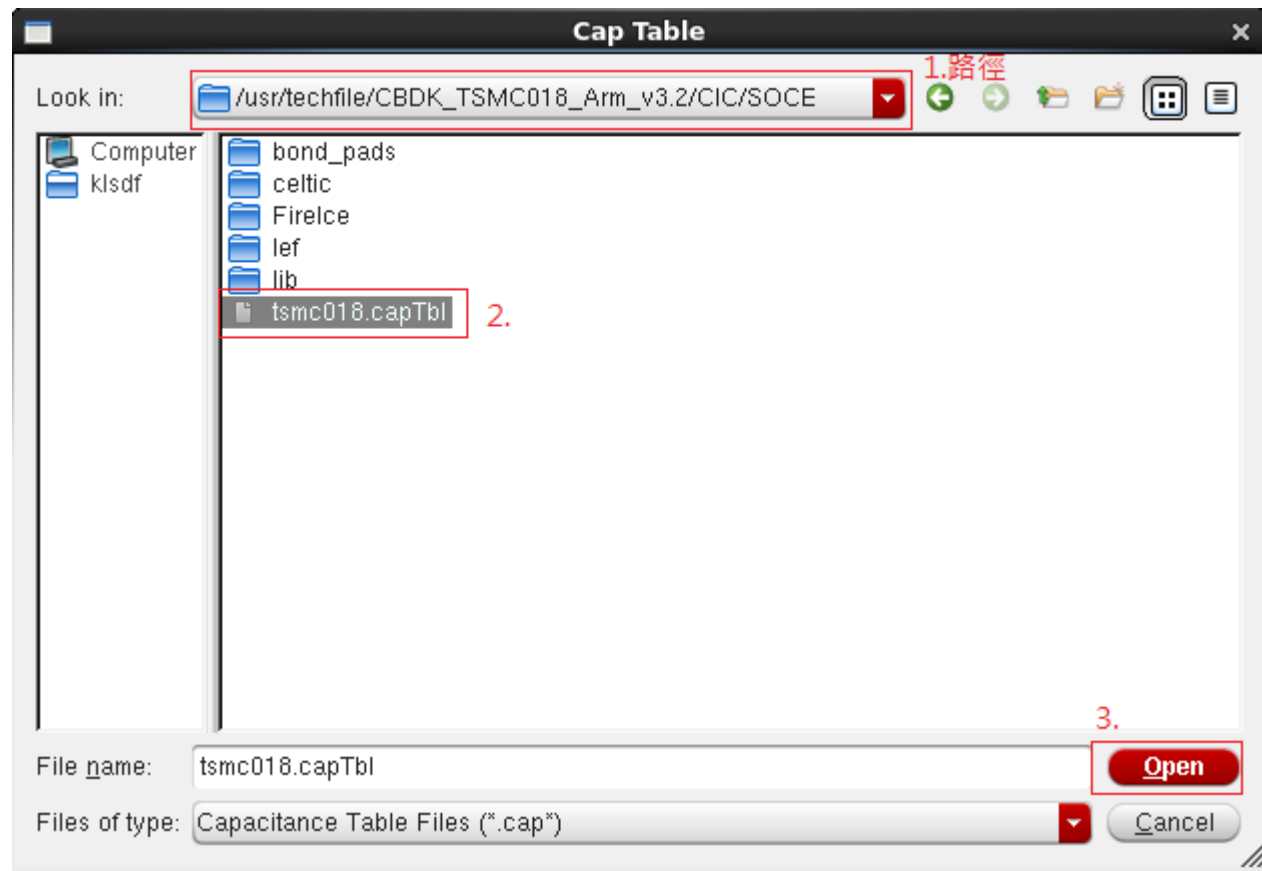
PostRoute Clock Resistance Scale Factor: 0.0

PostRoute Clock Cap Scale Factor: 0.0

QRC Technology File: 2.

**OK** Apply Close Help

# 使用Innovus





# 使用Innovus

**Add RC Corner**

Name: RC\_Corner

Cap Table: C:/SOCE/tsmc018.capTbl

Temperature:

PreRoute Resistance Scale Factor: 1.0

PreRoute Cap Scale Factor: 1.0

PreRoute Clock Resistance Scale Factor: 0.0

PreRoute Clock Cap Scale Factor: 0.0

PostRoute Resistance Scale Factor: 1.0

PostRoute Cap Scale Factor: 1.0

PostRoute Xcap Scale Factor: 1.0

PostRoute Clock Resistance Scale Factor: 0.0

PostRoute Clock Cap Scale Factor: 0.0

QRC Technology File

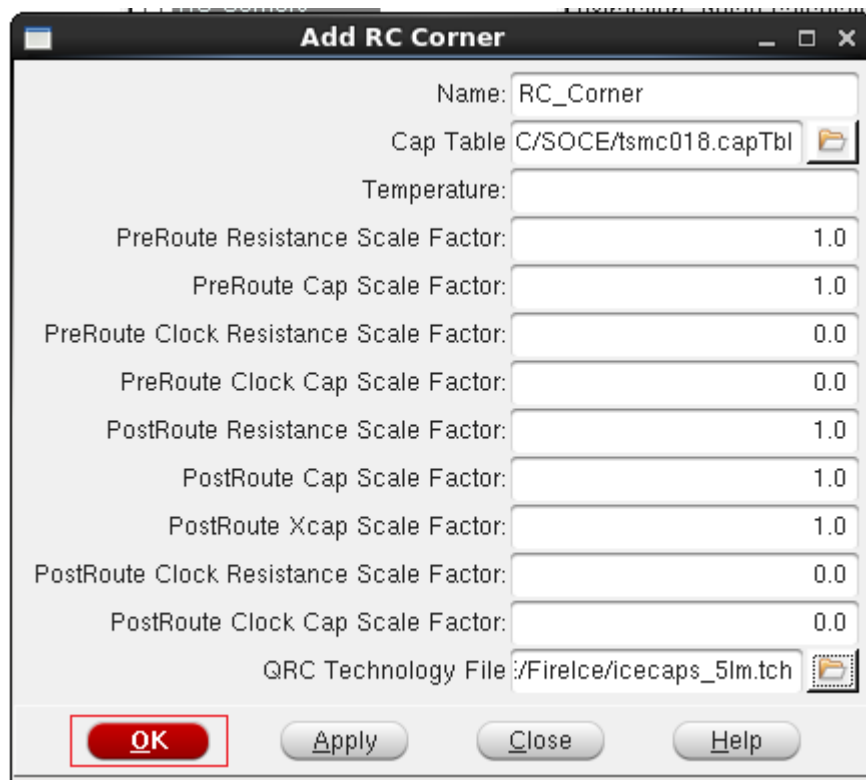
OK Apply Close Help

# 使用Innovus

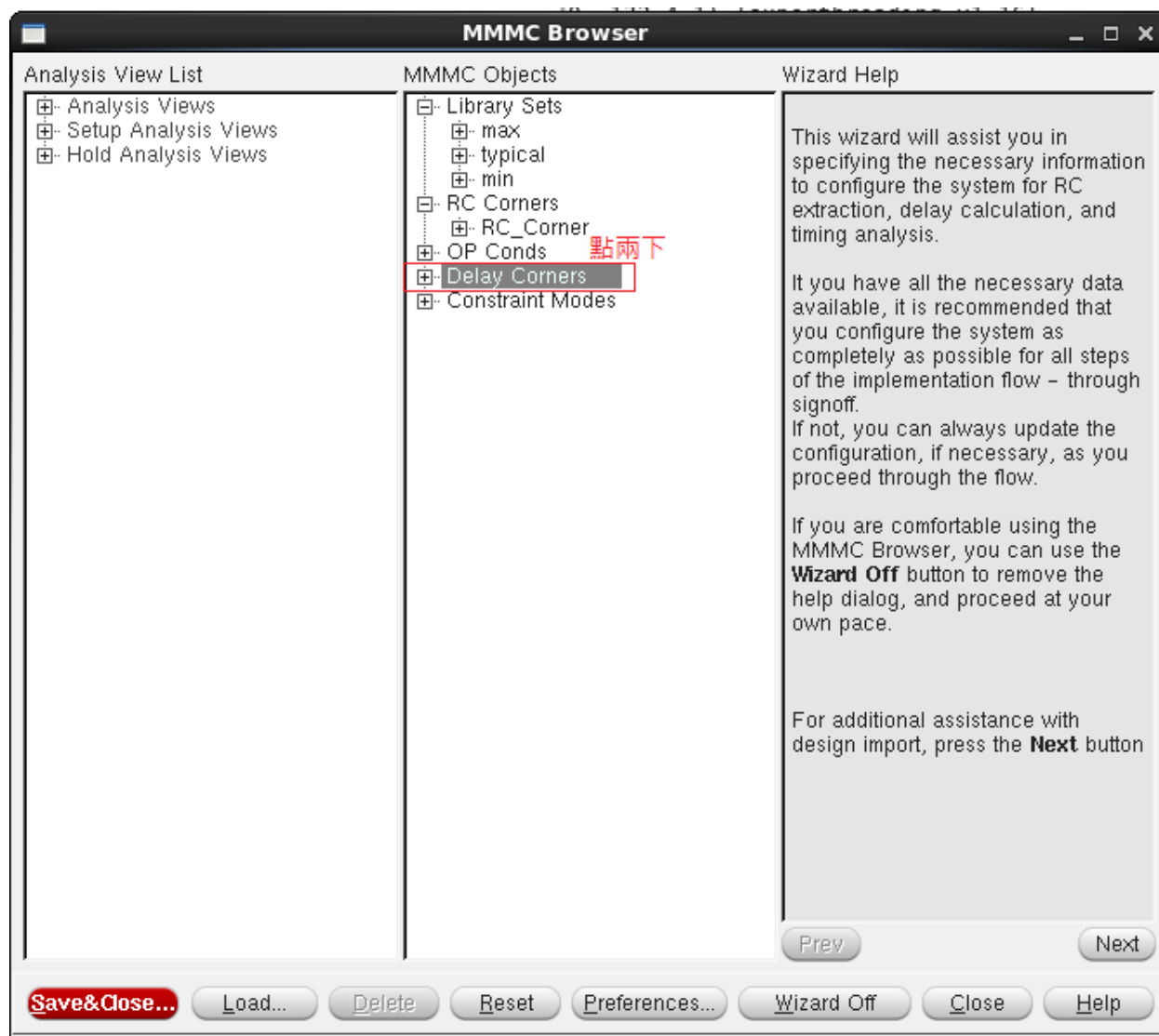


# 使用Innovus

按OK確認



# 使用Innovus



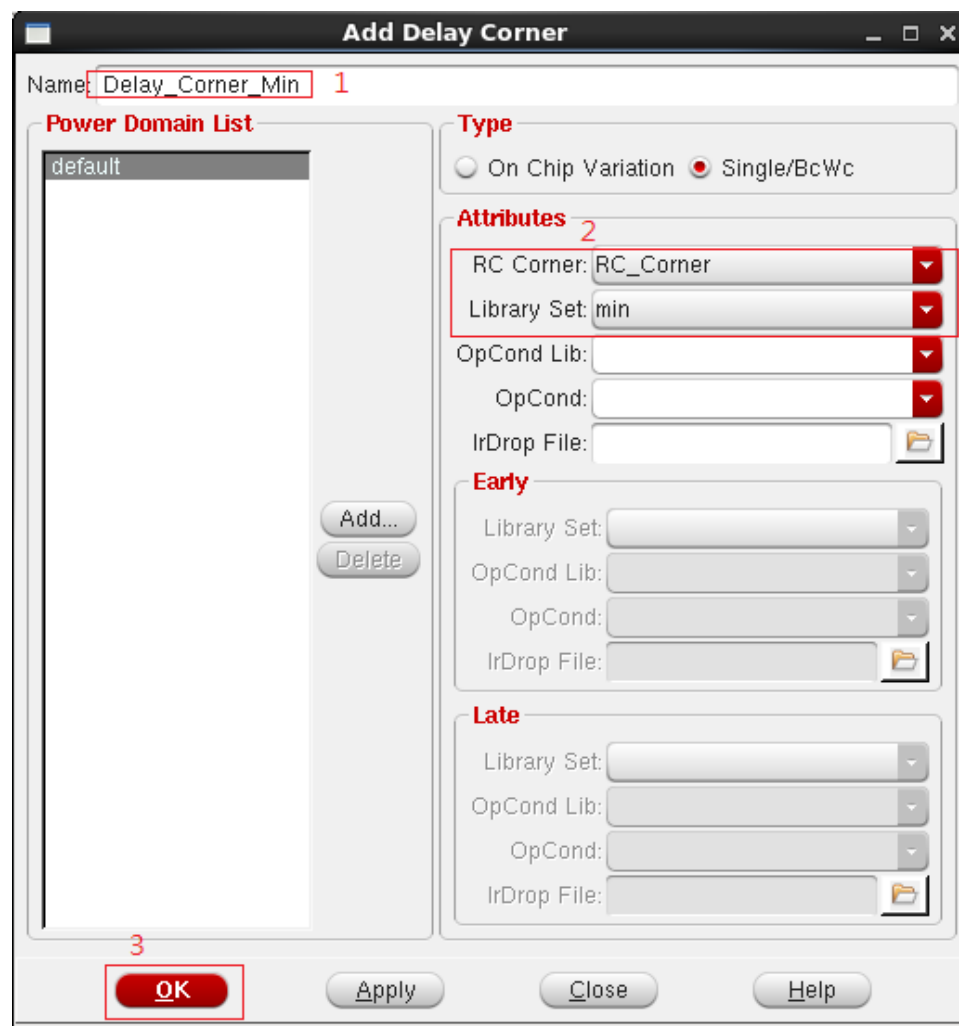
# 使用Innovus

新增Delay\_Corner\_Max



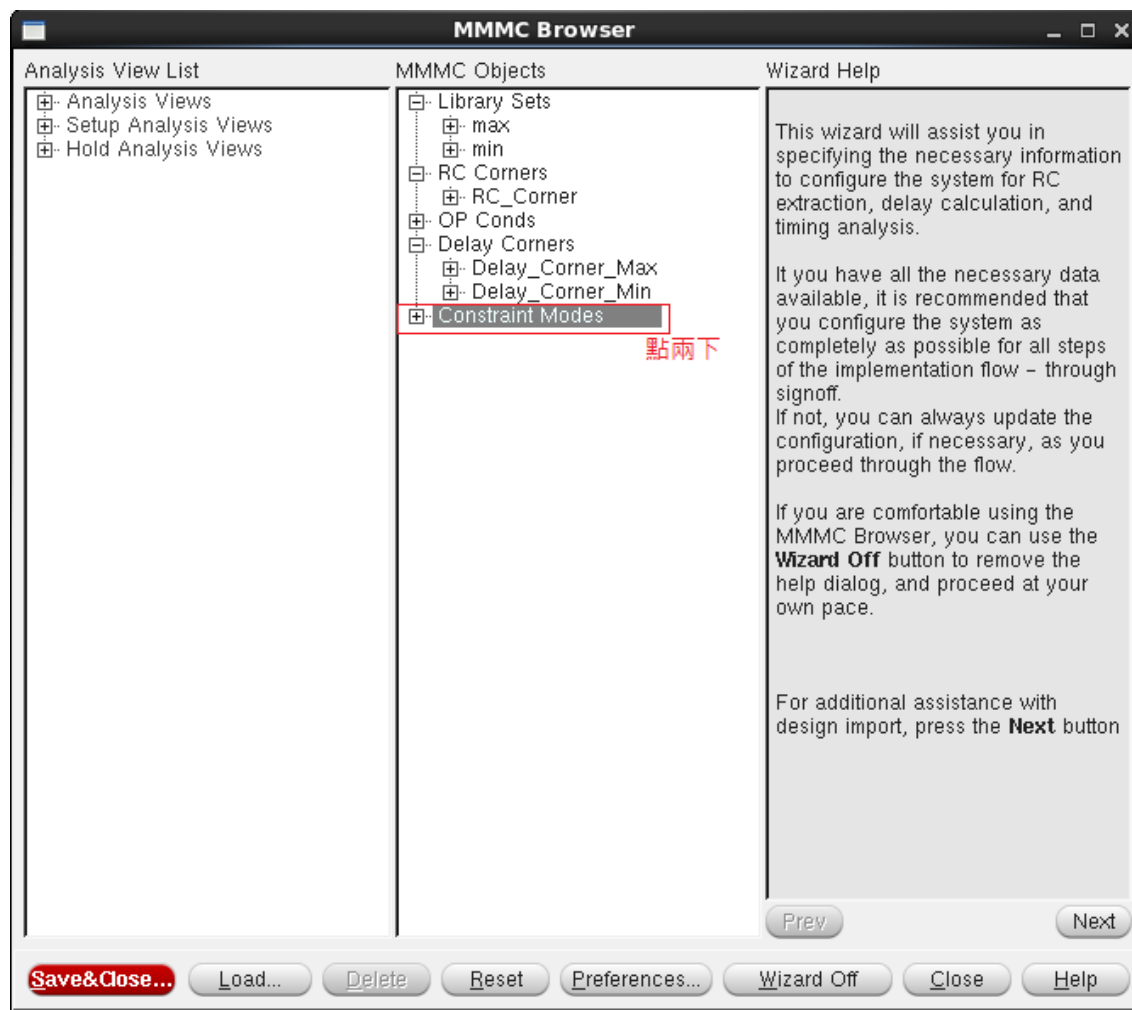
# 使用Innovus

新增Delay\_Corner\_Min



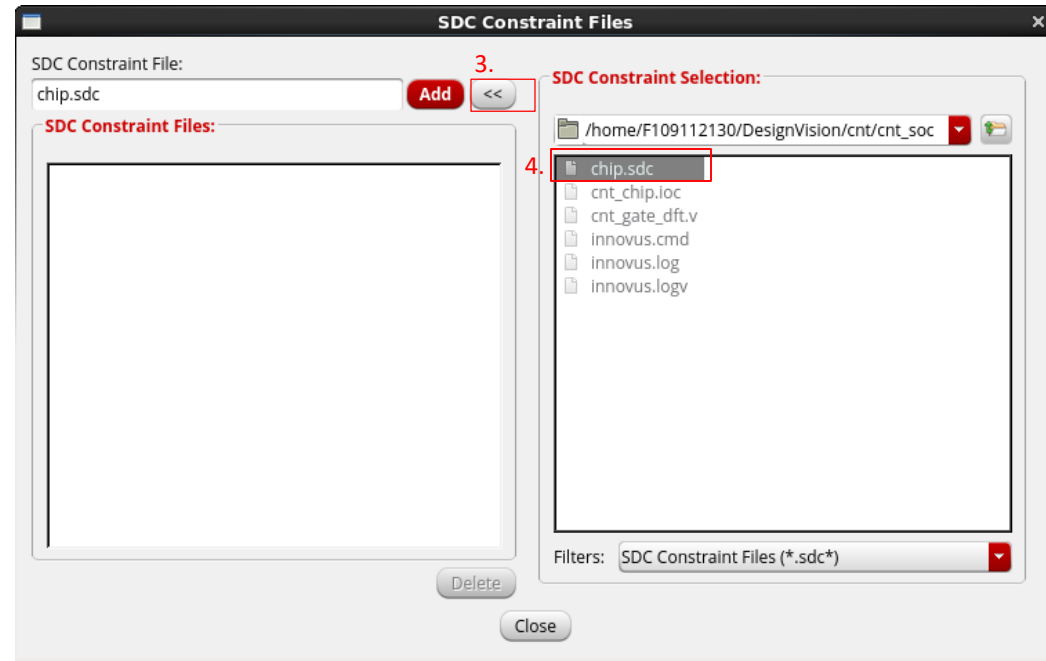
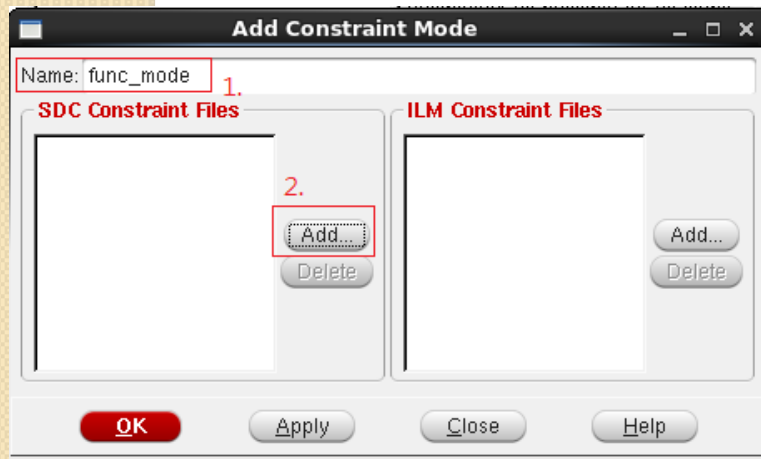
# 使用Innovus

## 匯入SDC File



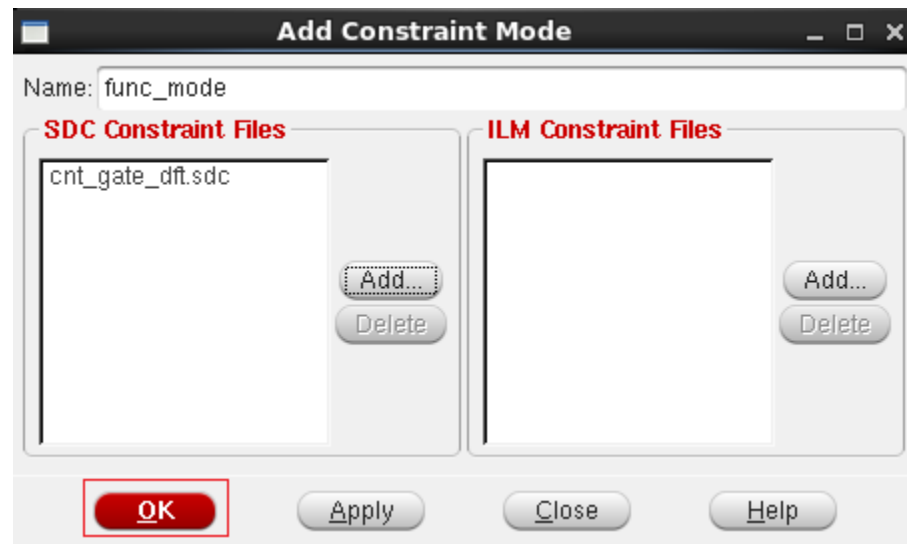
# 使用Innovus

第四章所給予的.sdc檔

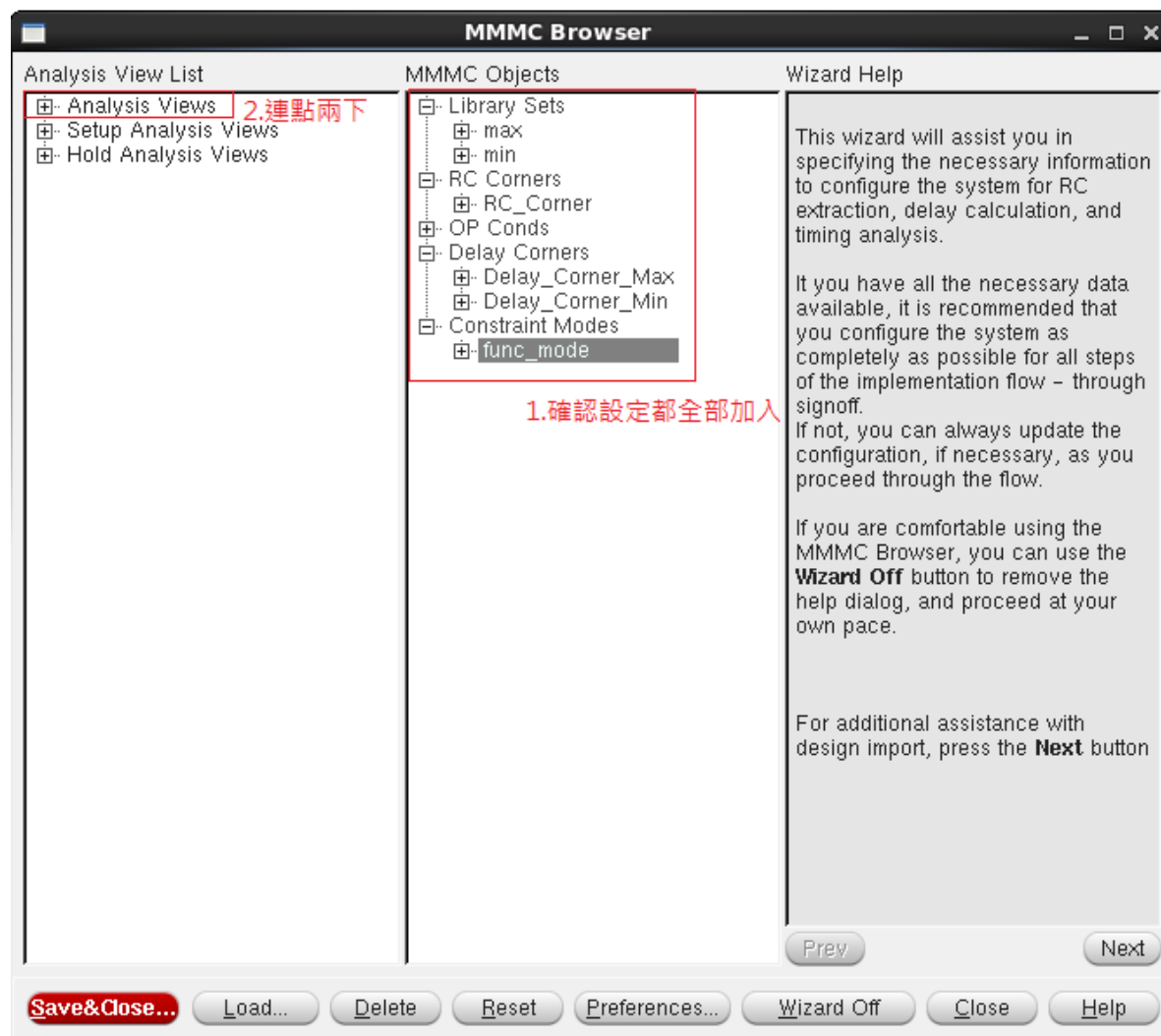




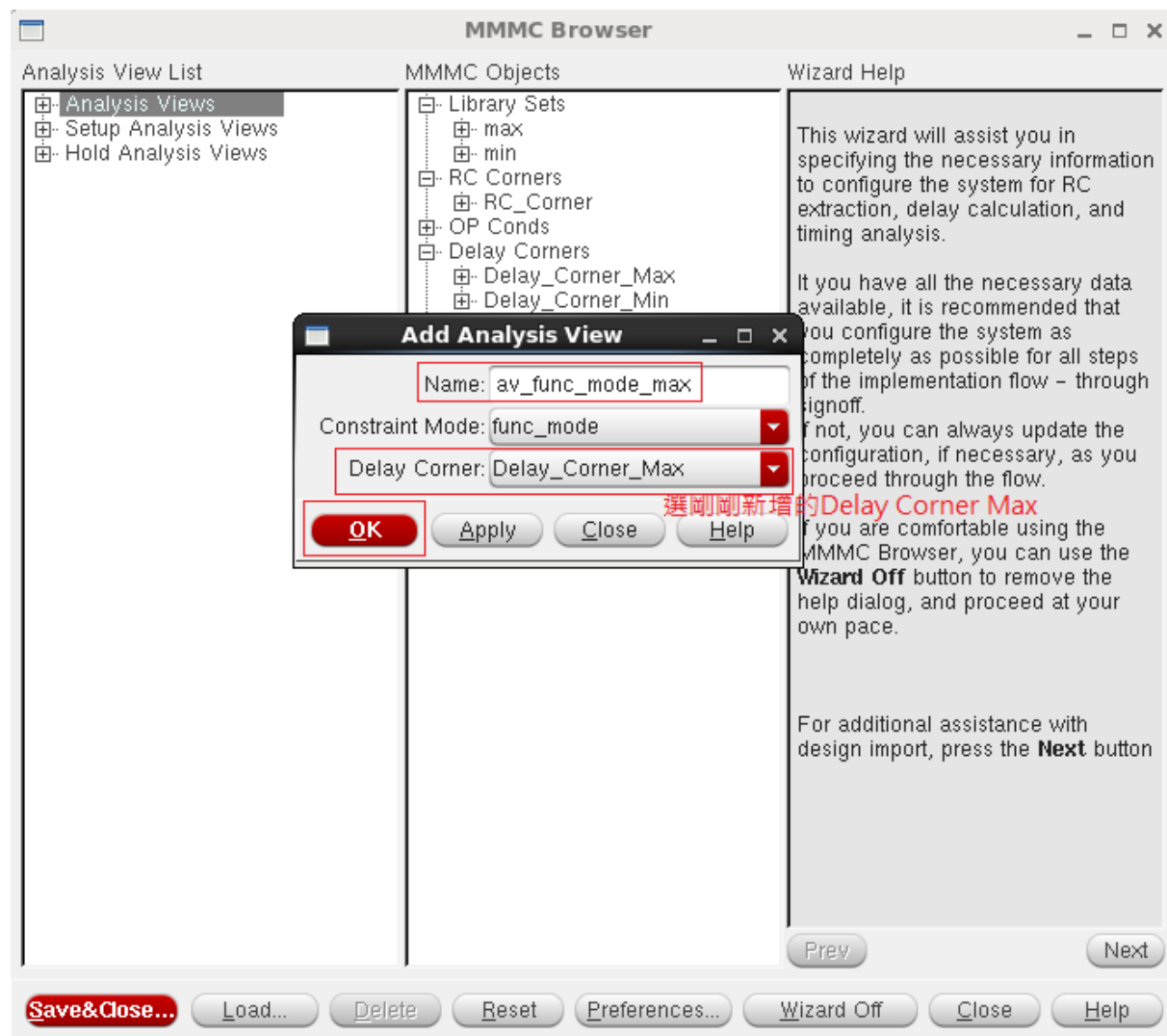
# 使用Innovus



# 使用Innovus

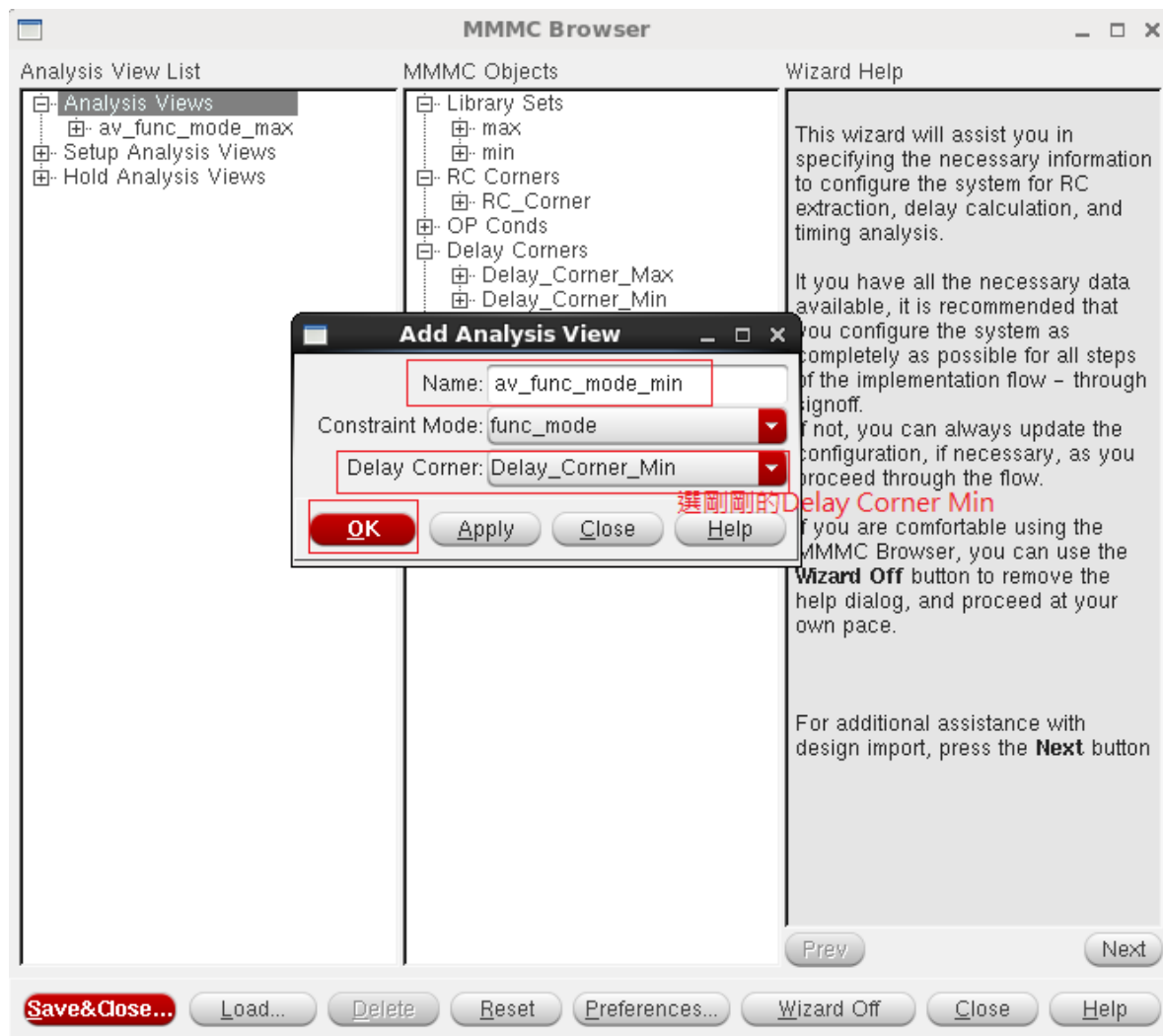


# 使用Innovus

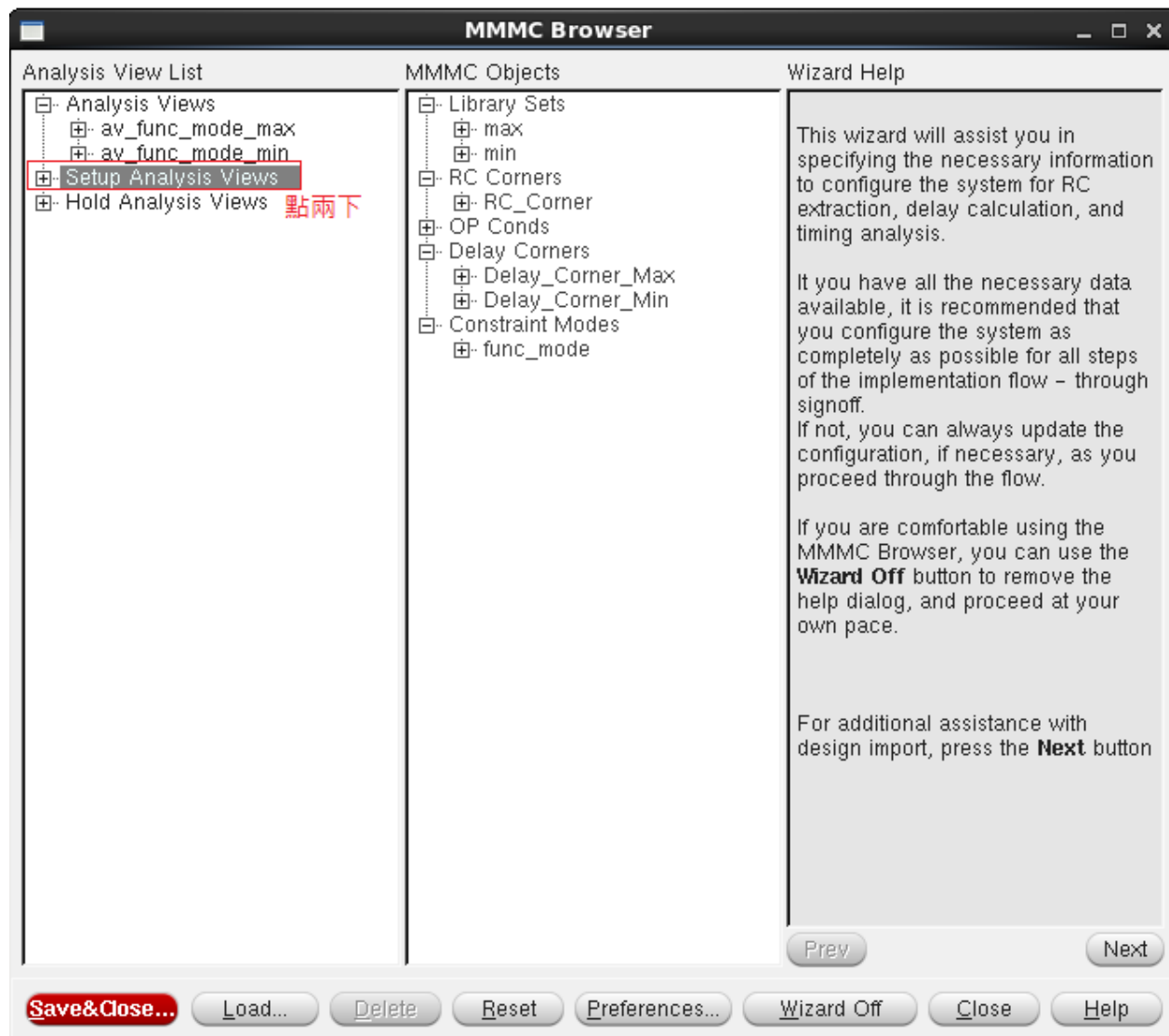


# 使用Innovus

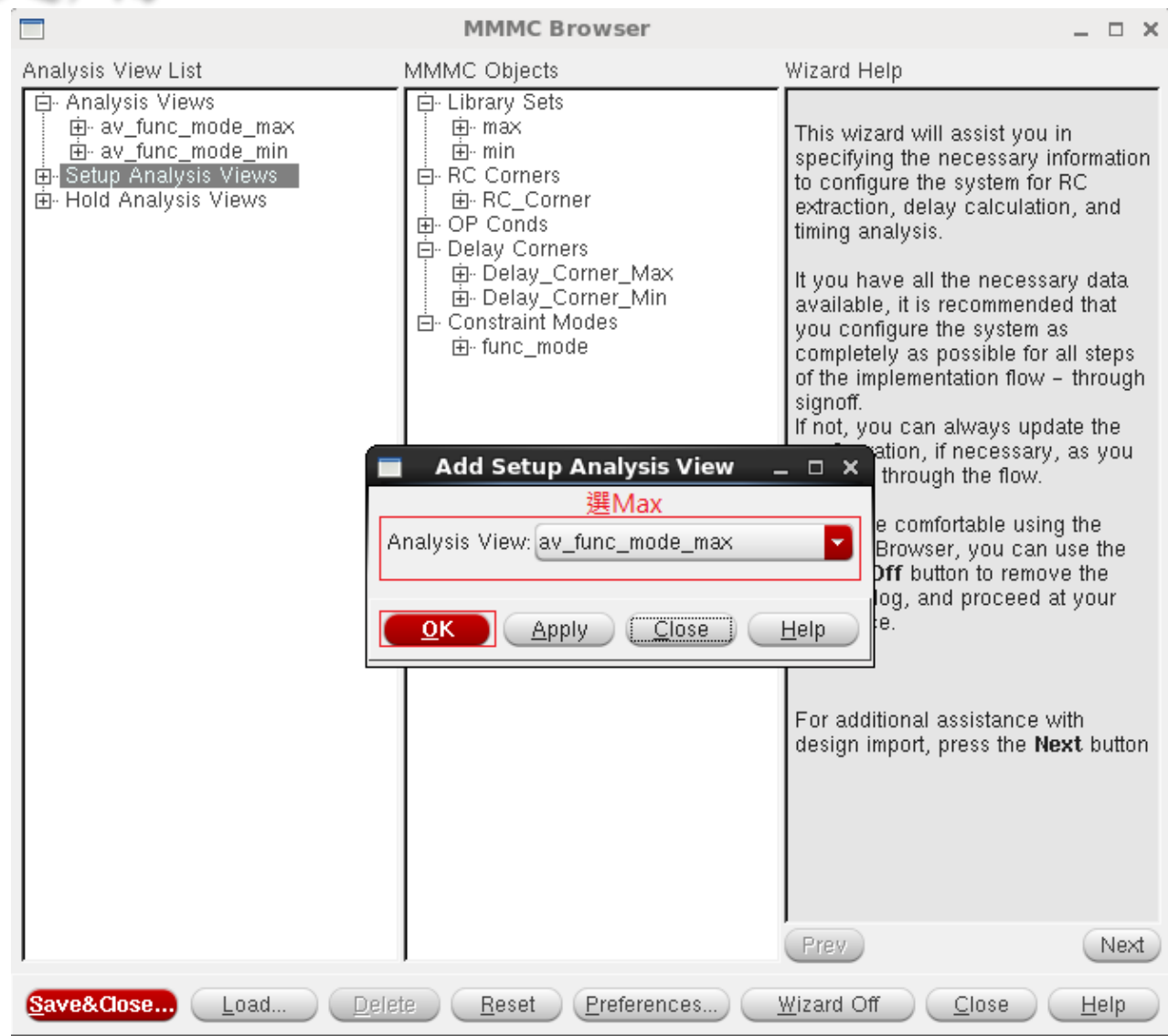
再新增一個av\_func\_mode\_min



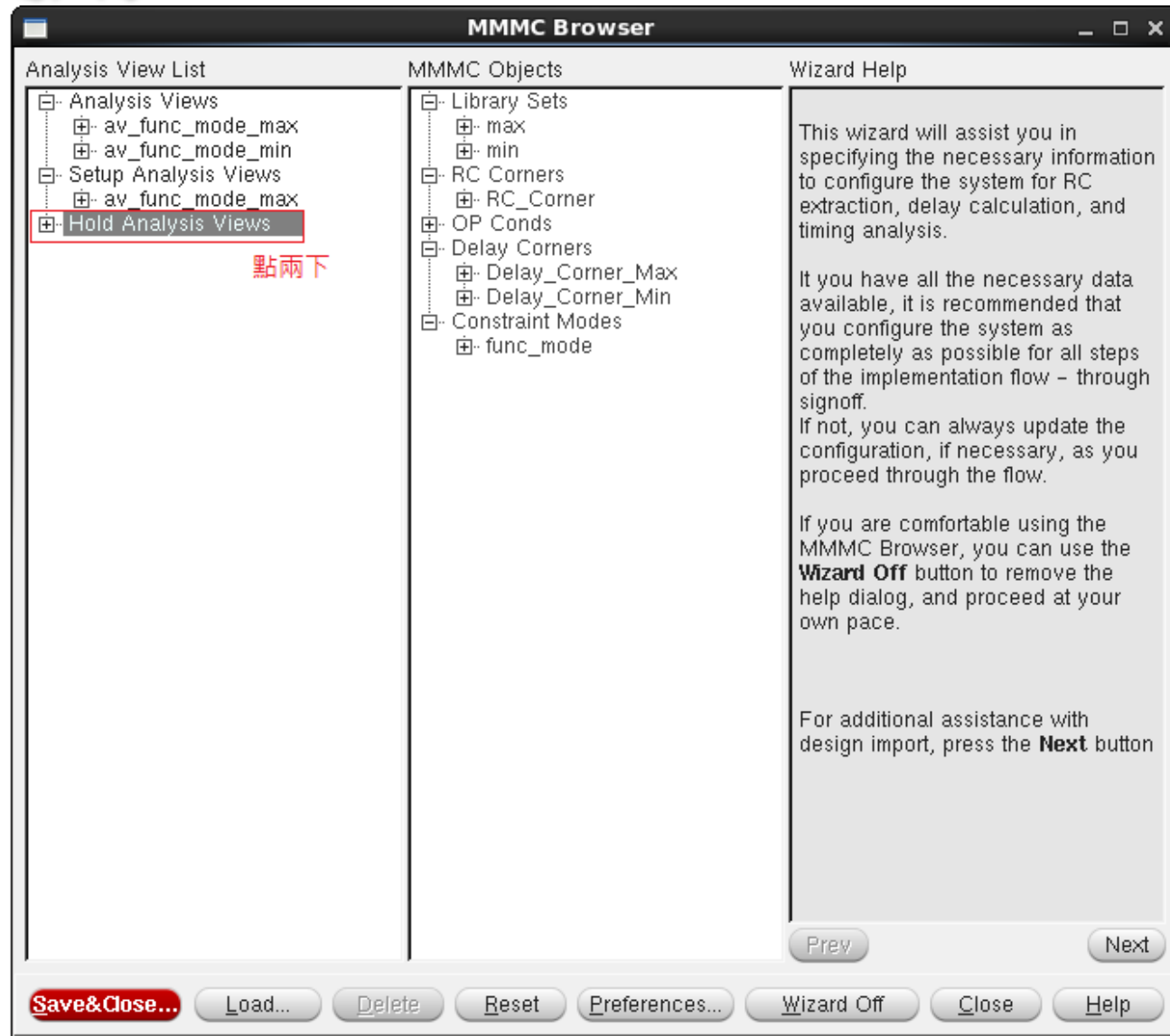
# 使用Innovus



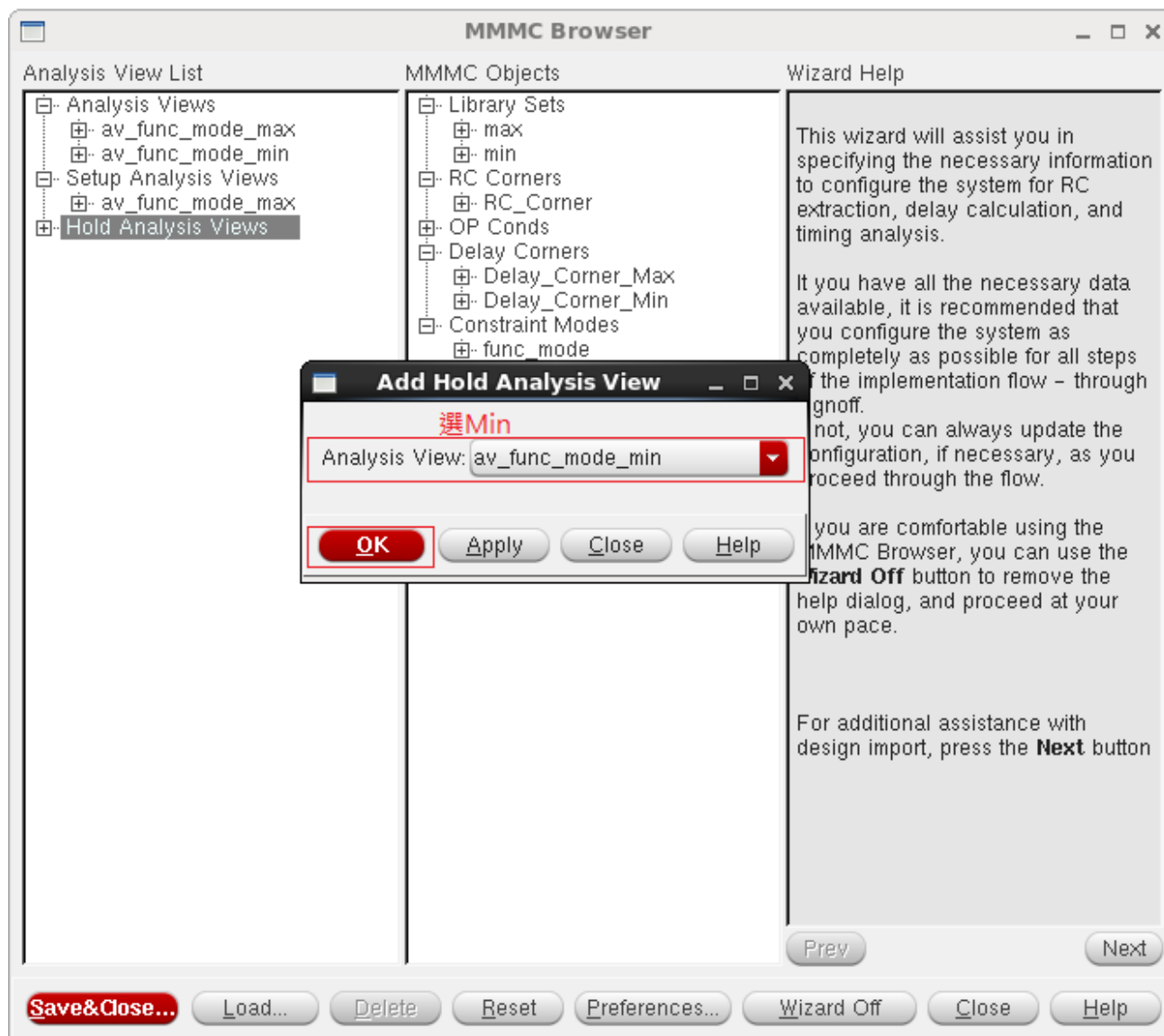
# 使用Innovus



# 使用Innovus



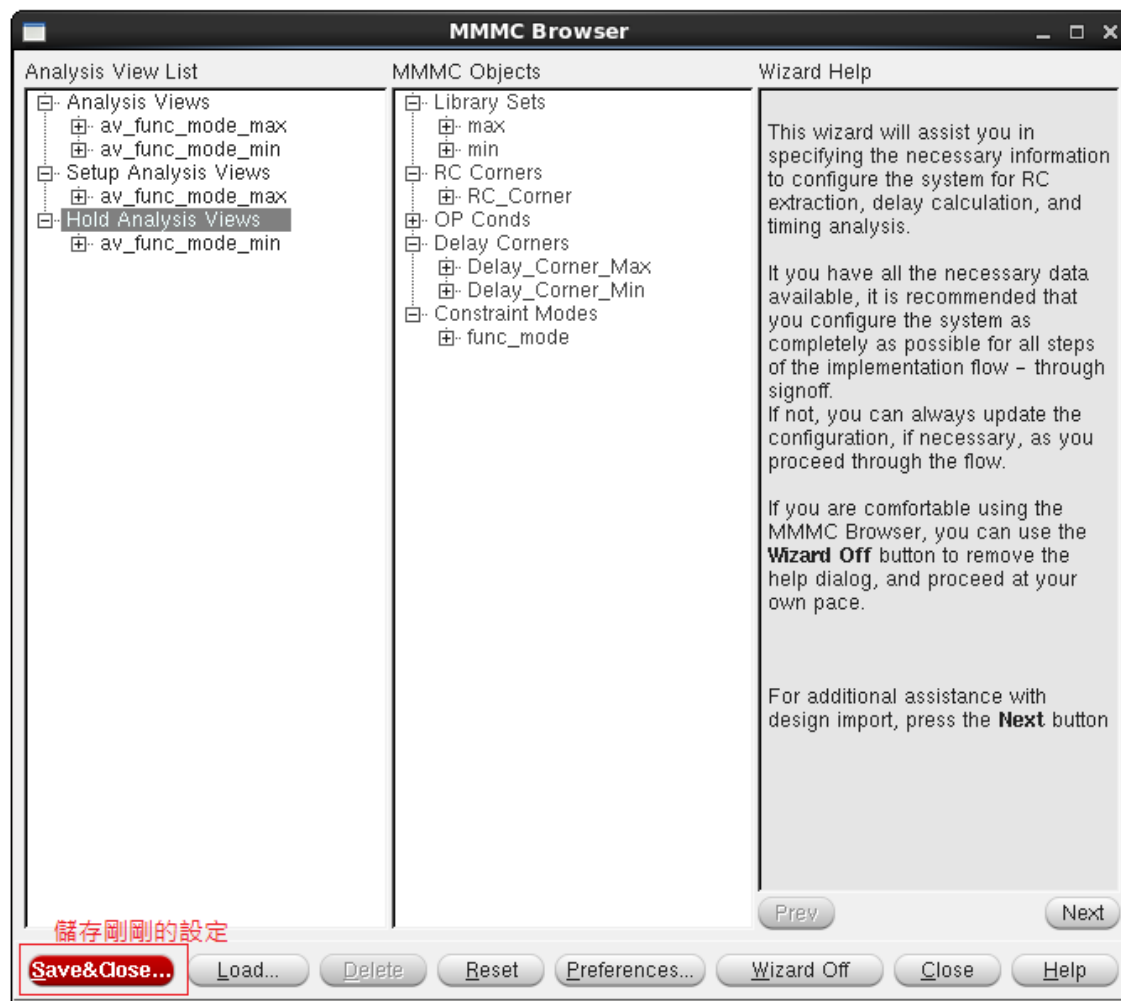
# 使用Innovus



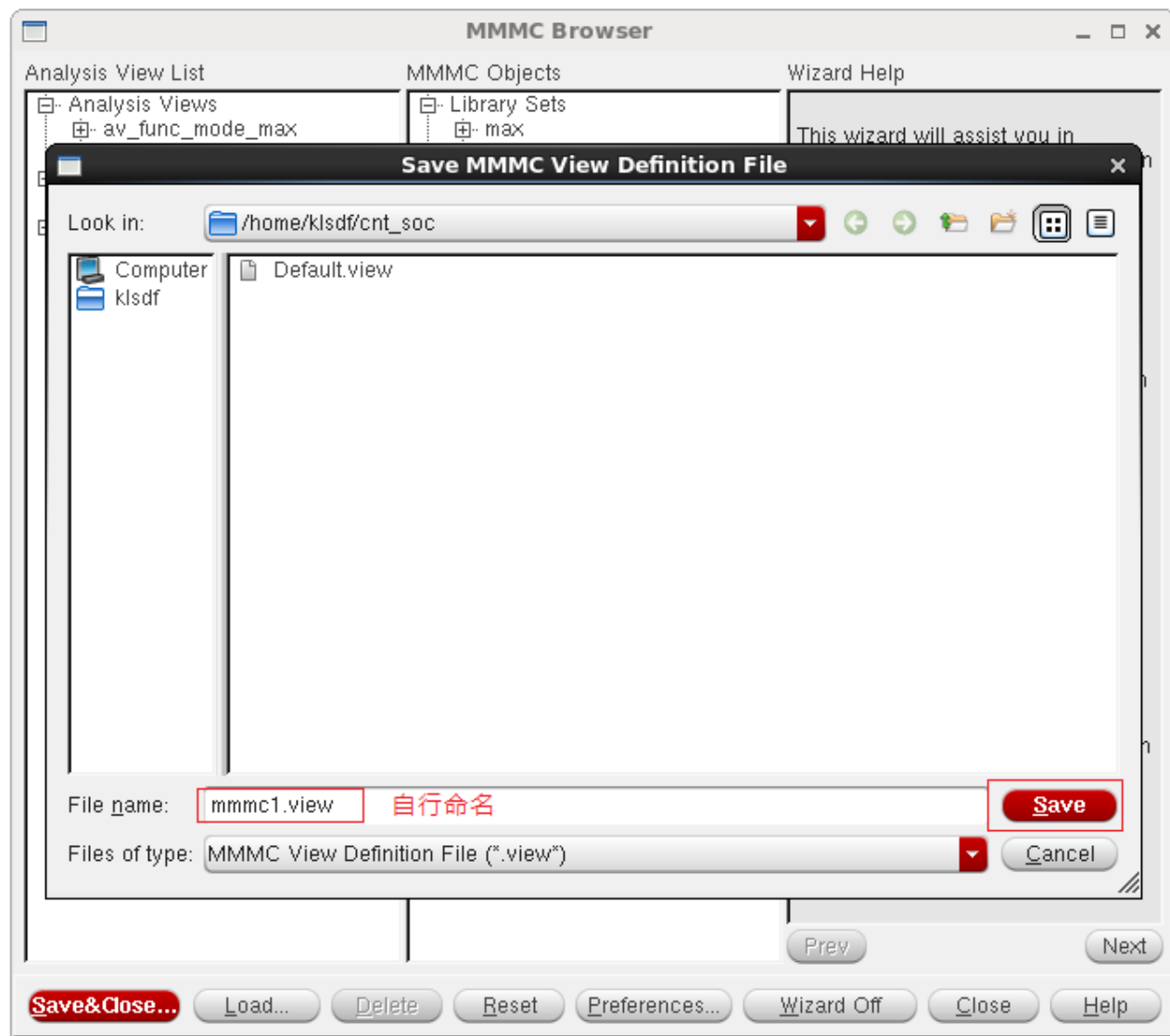


# 使用Innovus

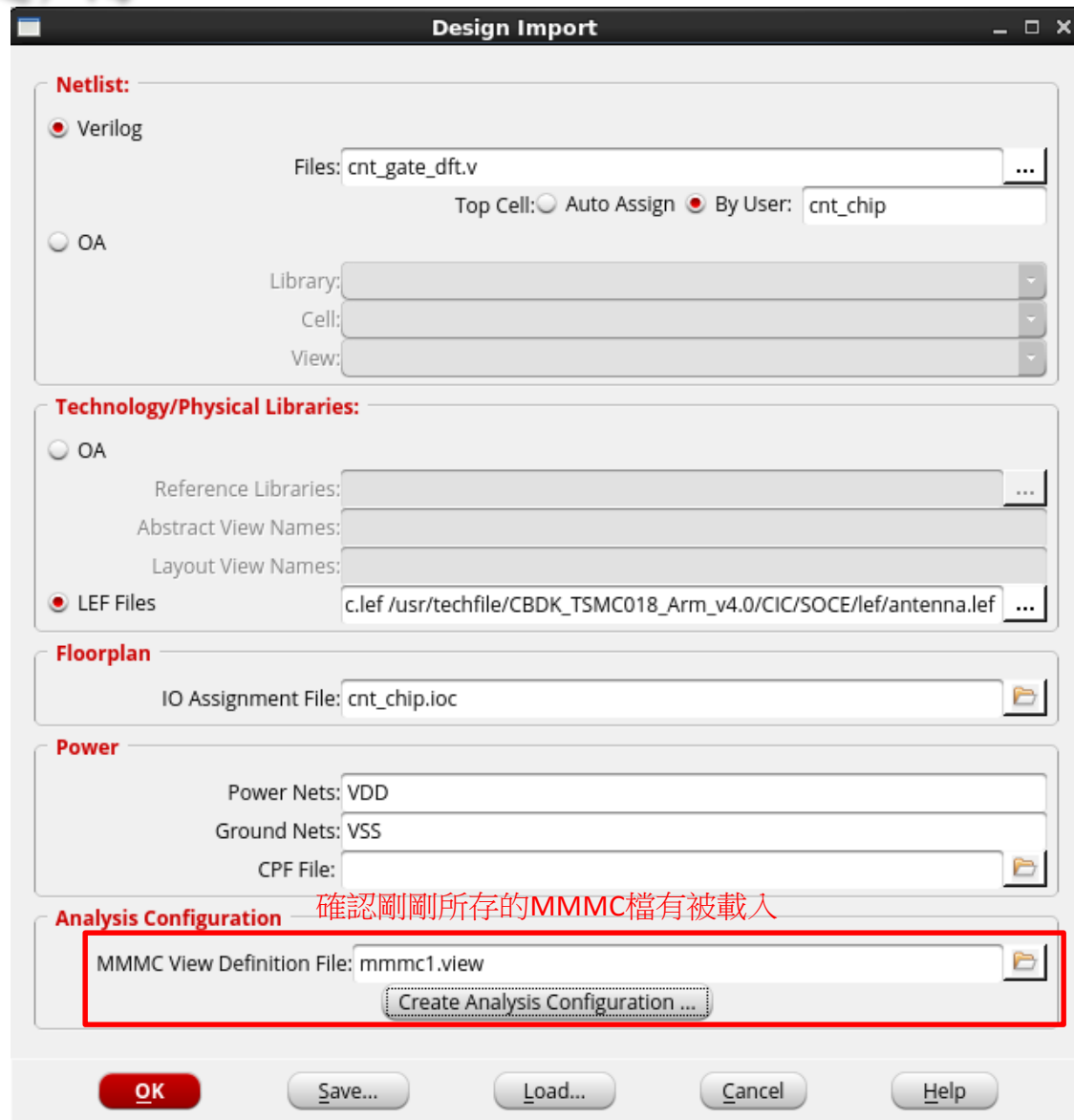
為了不每次做新的設計都要重新設定，儲存剛剛Library設定。



# 使用Innovus



# 使用Innovus



The screenshot shows the 'Design Import' dialog box in the Innovus software. The dialog is organized into several sections with expandable/collapsible headers. The 'Netlist' section is expanded, showing options for Verilog and OA. The 'Technology/Physical Libraries' section is also expanded, showing options for OA and LEF Files. The 'Floorplan' section is expanded, showing the IO Assignment File. The 'Power' section is expanded, showing Power Nets, Ground Nets, and CPF File. The 'Analysis Configuration' section is expanded, showing the MMMC View Definition File. A red rectangle highlights the 'Analysis Configuration' section, and a red arrow points to the 'Create Analysis Configuration ...' button. The text '確認剛剛所存的MMMM檔有被載入' (Confirm that the MMMM file just saved is loaded) is written in red above the red rectangle.

**Design Import**

**Netlist:**

- ☒ Verilog
  - Files: cnt\_gate\_dft.v
  - Top Cell: ☐ Auto Assign ☒ By User: cnt\_chip
  - Library:
  - Cell:
  - View:
- ☐ OA

**Technology/Physical Libraries:**

- ☐ OA
  - Reference Libraries:
  - Abstract View Names:
  - Layout View Names:
- ☒ LEF Files
  - c.lef /usr/techfile/CBDK\_TSMC018\_Arm\_v4.0/CIC/SOCE/lef/antenna.lef

**Floorplan**

IO Assignment File: cnt\_chip.ioc

**Power**

Power Nets: VDD

Ground Nets: VSS

CPF File:

**Analysis Configuration** — 確認剛剛所存的MMMM檔有被載入

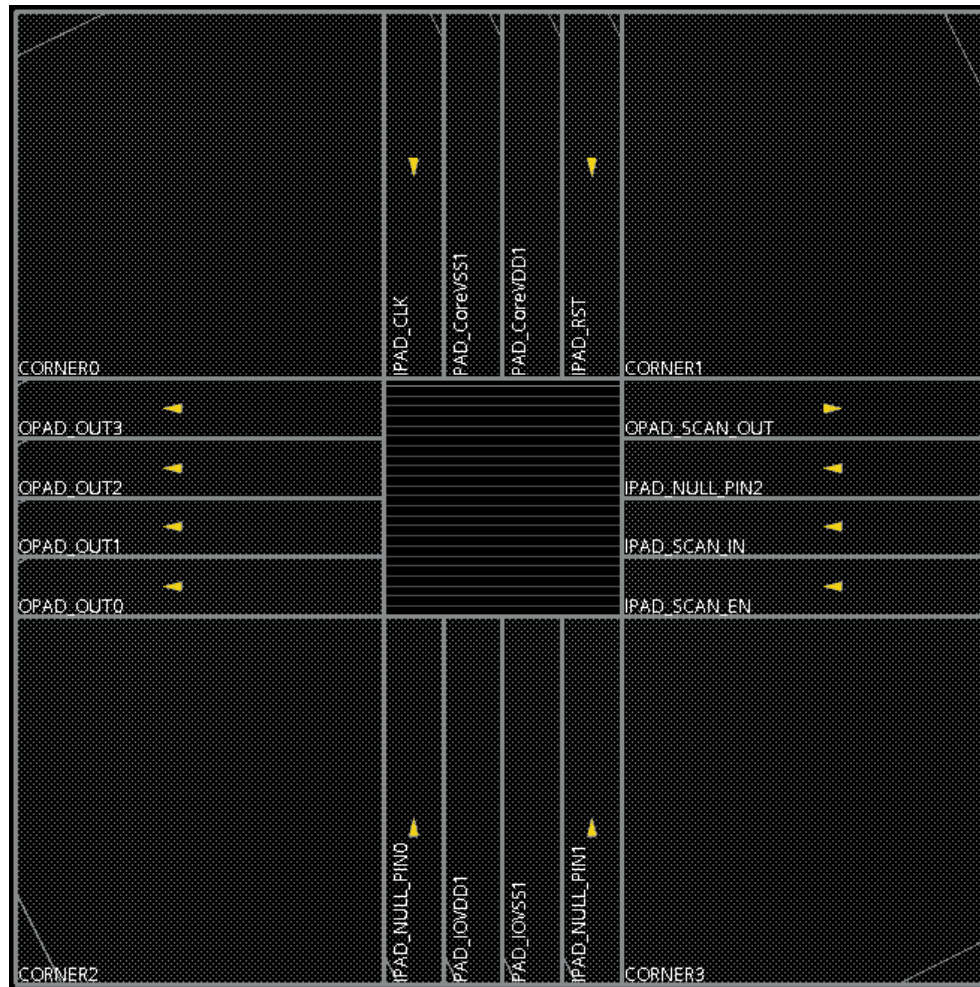
MMMC View Definition File: mmmm1.view

Create Analysis Configuration ...

OK Save... Load... Cancel Help

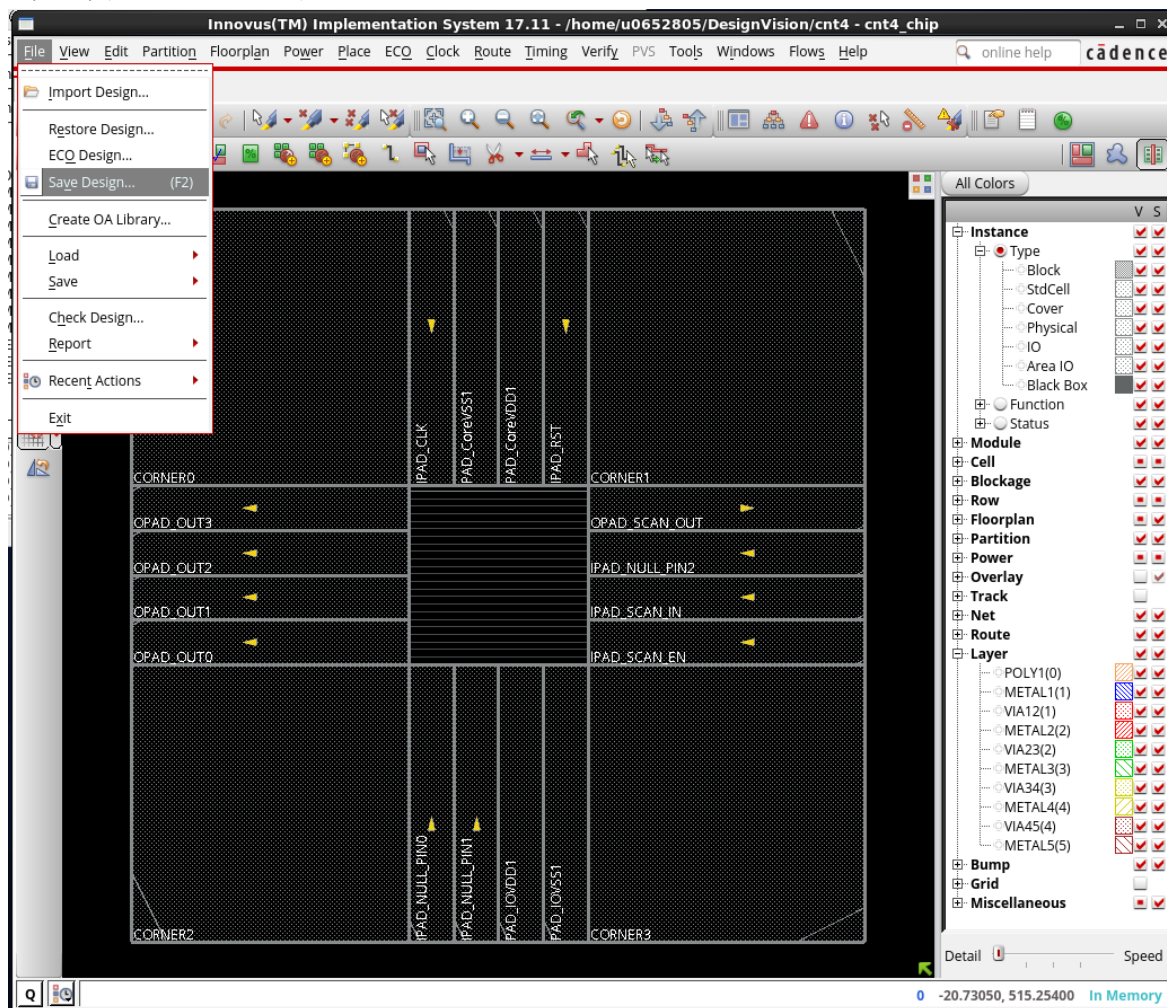
# 使用Innovus

載入成功

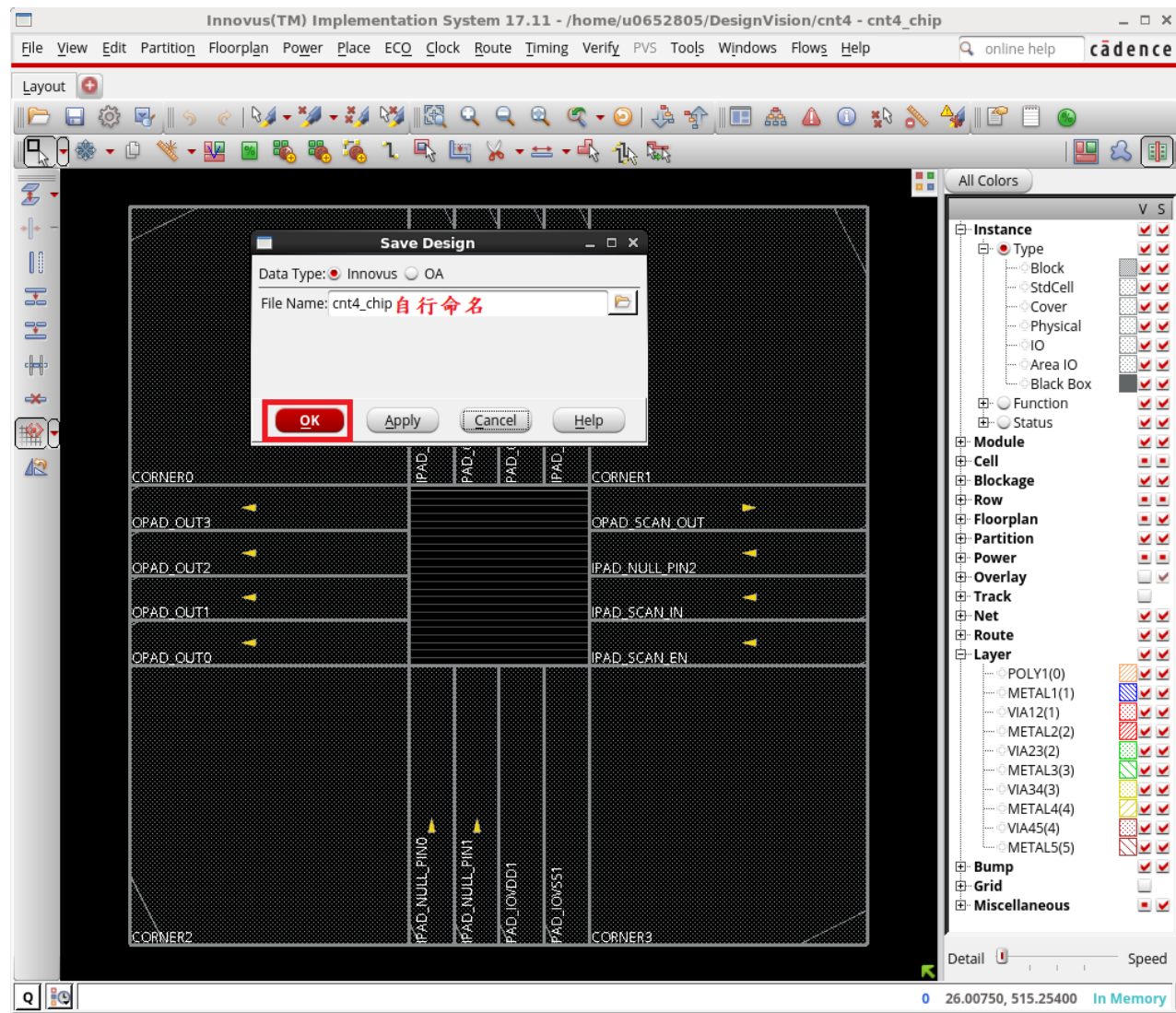


# 使用Innovus

先儲存目前進度



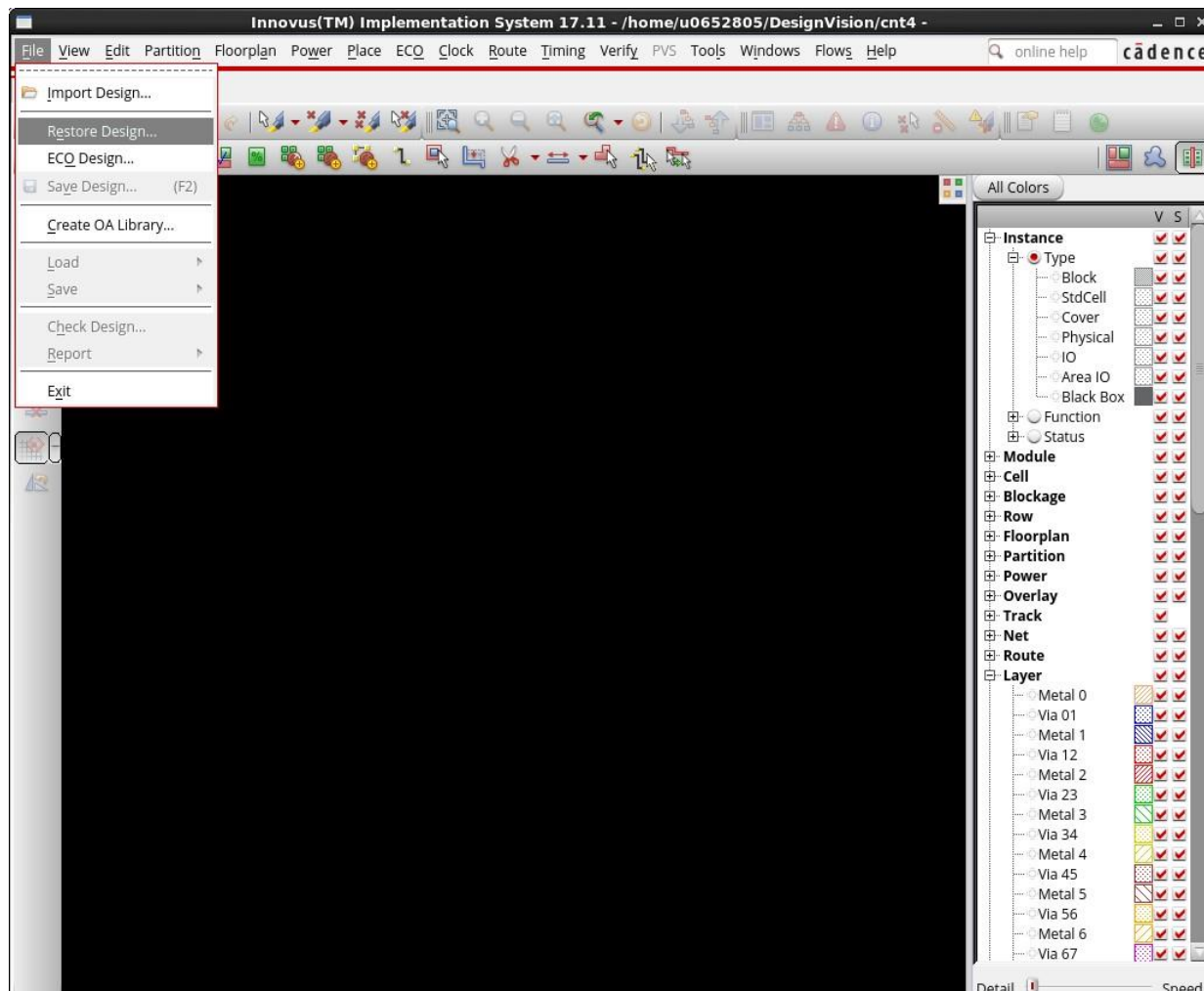
# 使用Innovus



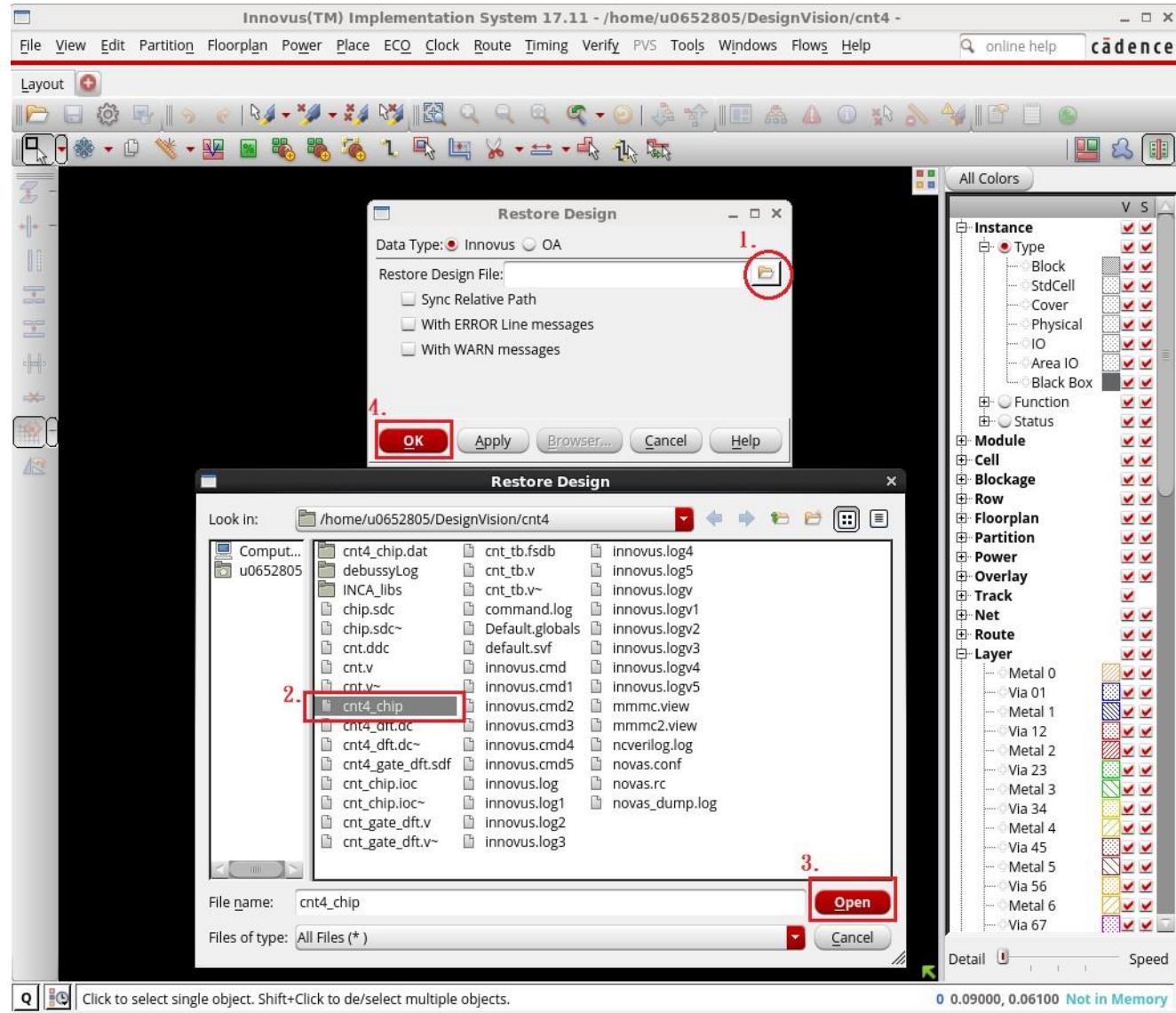


# 使用Innovus

關掉Innovus後重新載入剛剛的進度



# 使用Innovus





看到已經回復剛剛做的進度，以後的章節請善用此功能確保做的進度有存檔。

