ASIC教材

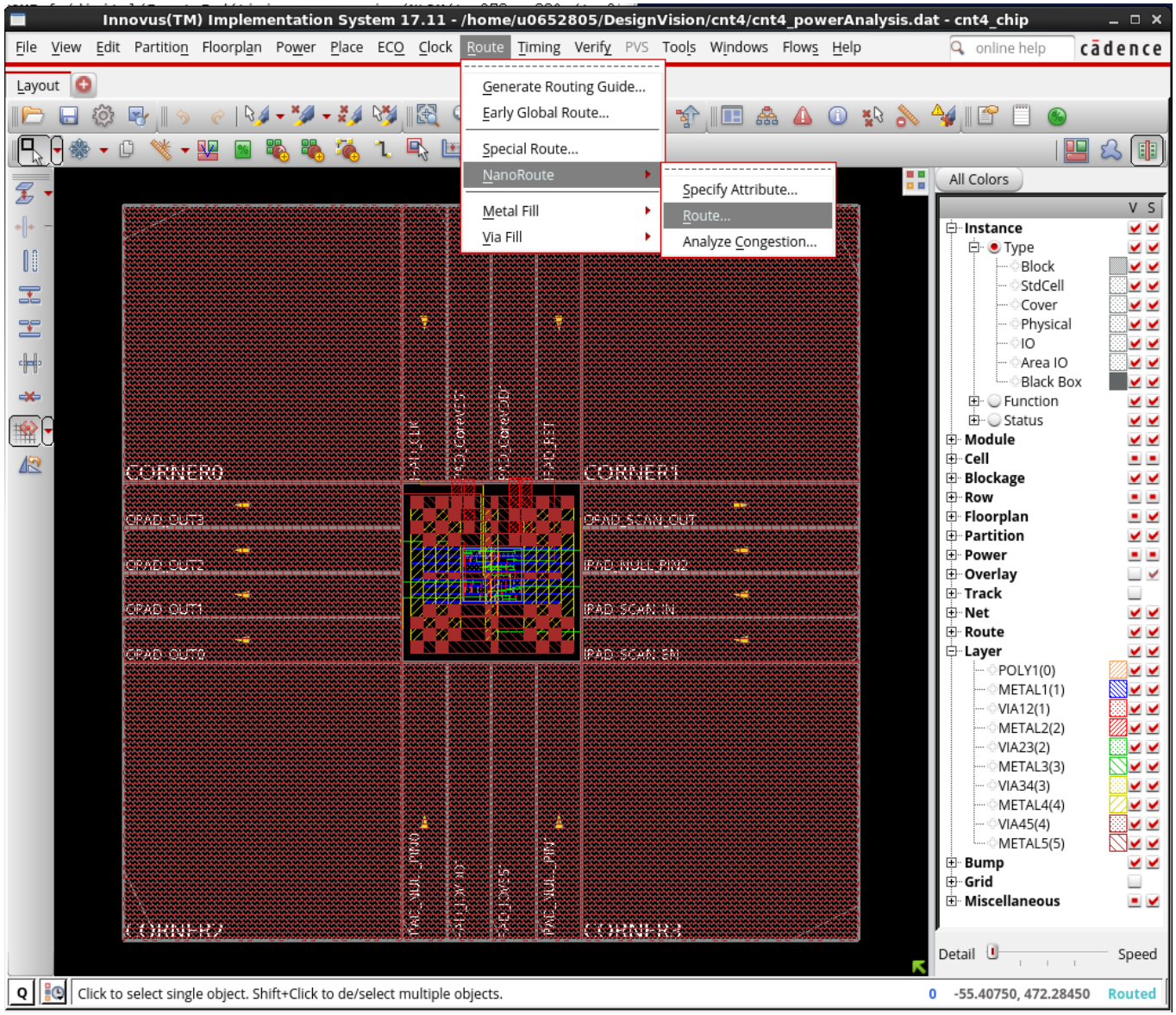
Chapter8 Innovus Routing

高雄科技大學電子工程系
B510實驗室

2021/2/2再編

目錄

Routing

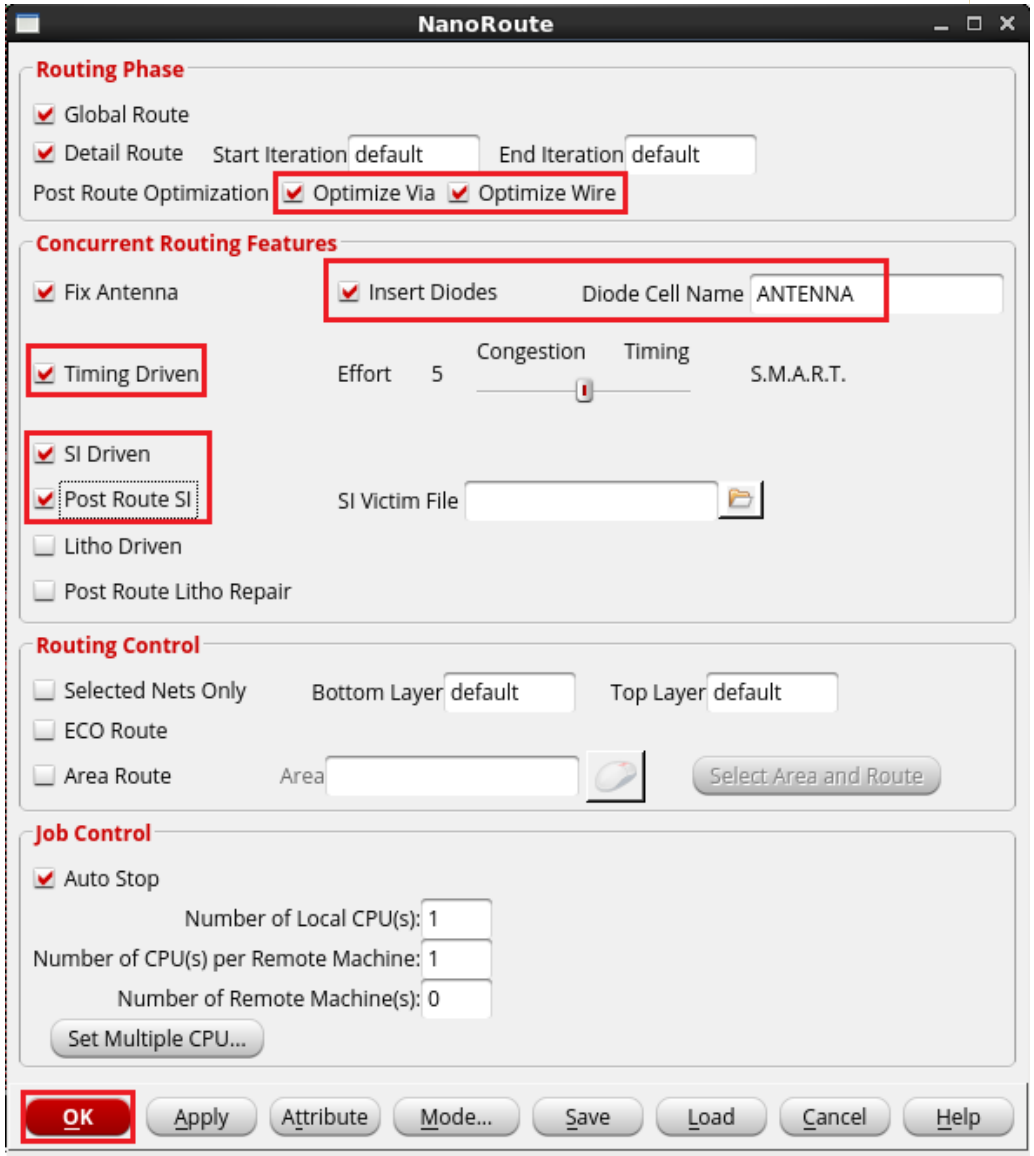

Innovus(TM) Implementation System 17.11 - /home/u0652805/DesignVision/cnt4/cnt4_powerAnalysis.dat - cnt4_chip
File View Edit Partition Floorplan Power Place ECO Clock Route Timing Verify PVS Tools Windows Flows Help
online help
cadence
Layout
Generate Routing Guide...
Early Global Route...
Special Route...
NanoRoute
Metal Fill
Via Fill
Specify Attribute...
Route...
Analyze Congestion...
All Colors
V S
Instance
Type
Block
StdCell
Cover
Physical
IO
Area IO
Black Box
Function
Status
Module
Cell
Blockage
Row
Floorplan
Partition
Power
Overlay
Track
Net
Route
Layer
POLY1(0)
METAL1(1)
VIA12(1)
METAL2(2)
VIA23(2)
METAL3(3)
VIA34(3)
METAL4(4)
VIA45(4)
METAL5(5)
Bump
Grid
Miscellaneous
CORNER0
CORNER1
CORNER2
CORNER3
Detail
Speed
Click to select single object. Shift+Click to de/select multiple objects.
-55.40750, 472.28450
Routed

Routing

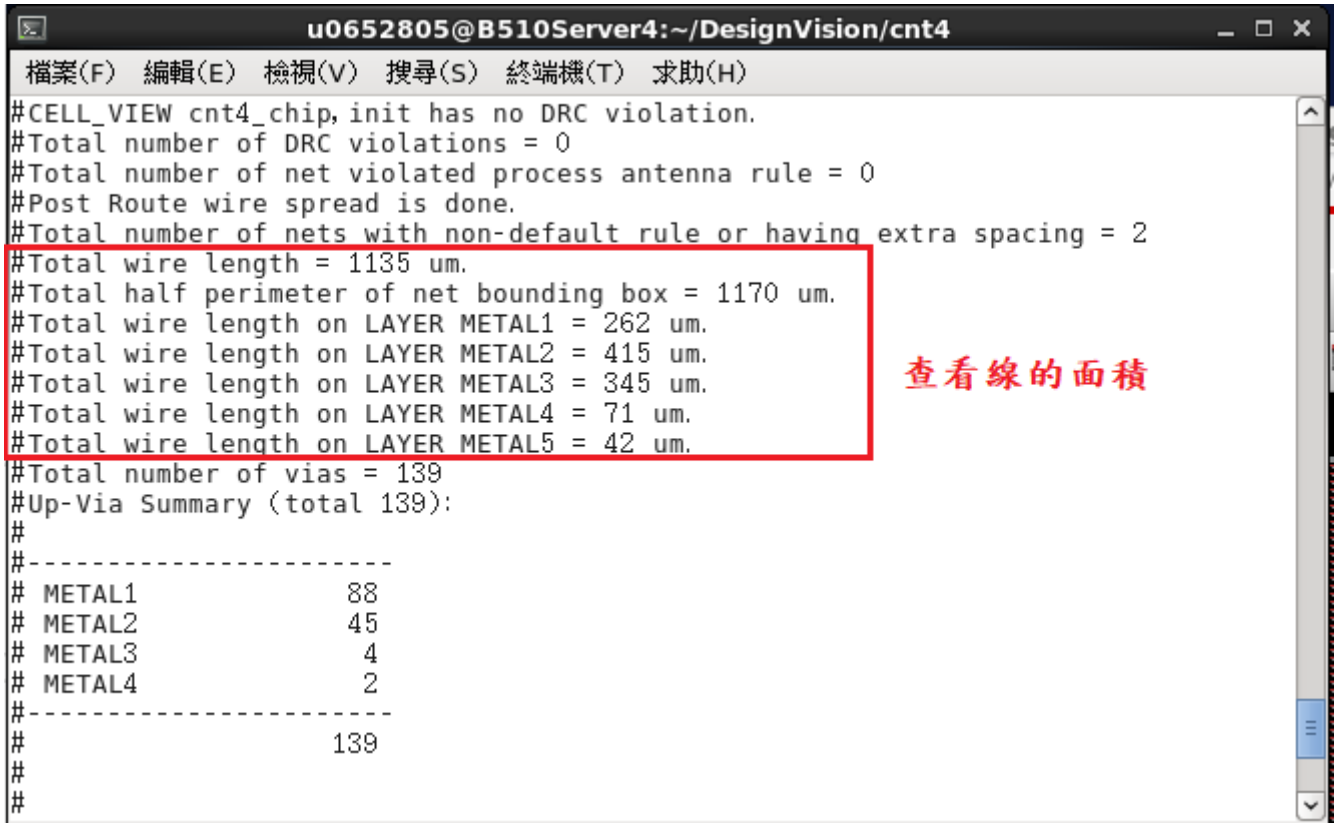
Timing Driven為
以Timing考量之Routing

Diodes為解決天線效應
ANTENNA為使用的
Diodes

SI Driven為在Routing
時同時考慮Cross talk



Routing


u0652805@B510Server4:~/DesignVision/cnt4
檔案(F) 編輯(E) 檢視(V) 搜尋(S) 終端機(T) 求助(H)
#CELL_VIEW cnt4_chip,init has no DRC violation.
#Total number of DRC violations = 0
#Total number of net violated process antenna rule = 0
#Post Route wire spread is done.
#Total number of nets with non-default rule or having extra spacing = 2
#Total wire length = 1135 um.
#Total half perimeter of net bounding box = 1170 um.
#Total wire length on LAYER METAL1 = 262 um.
#Total wire length on LAYER METAL2 = 415 um.
#Total wire length on LAYER METAL3 = 345 um.
#Total wire length on LAYER METAL4 = 71 um.
#Total wire length on LAYER METAL5 = 42 um.
#Total number of vias = 139
#Up-Via Summary (total 139):
#
#------------------------
METAL1 88
METAL2 45
METAL3 4
METAL4 2
#------------------------
139
#
#
查看線的面積

Routing

Report Timing: 先將Timing Mode改成onChipVariation。
setAnalysisMode -analysisType onChipVariation -cppr both

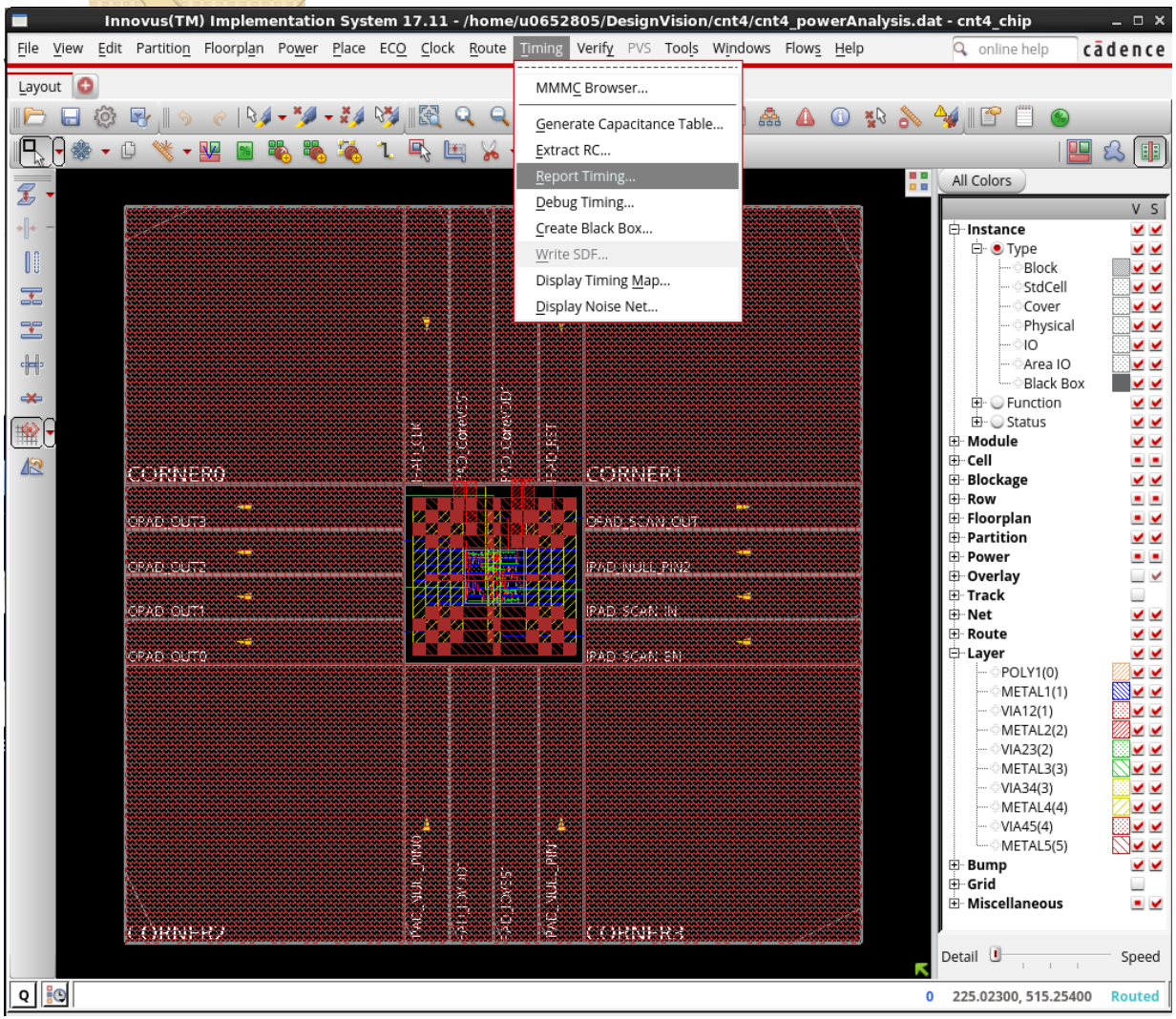
```
-clockPropagation  -cppr
innovus 1> setAnalysisMode -analysisType onChipVariation -cppr both
```

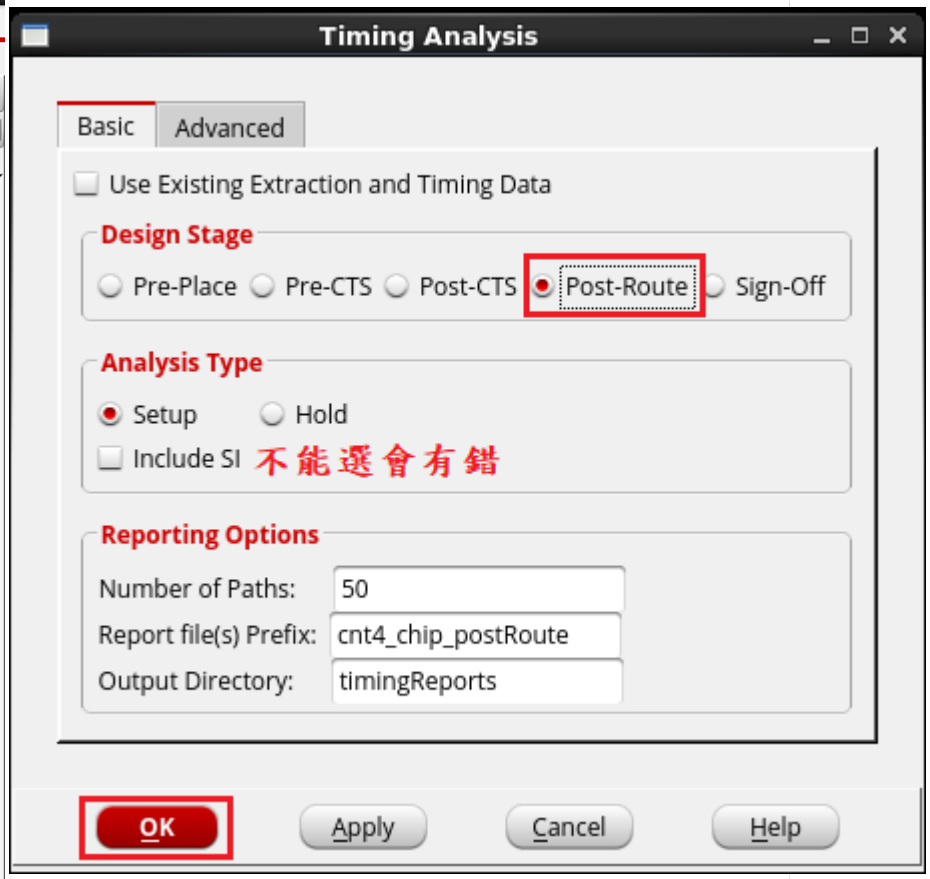
開啟模式: setDelayCalMode -SIAware true

```
u0652805@B510Server4:~/DesignVision/cnt4
檔案(F)  編輯(E)  檢視(V)  搜尋(S)  終端機(T)  求助(H)
|     Violating Paths:|    0    |    0    |    0    |
|           All Paths:|   21    |    7    |   14    |
+---------------------+---------+---------+---------+

+-----------------+-----------------------------------+------------------+
|                 |                Real               |       Total      |
|     DRVs        +-------------------+---------------+------------------|
|                 |  Nr nets(terms)   |  Worst Vio    |  Nr nets(terms)  |
+-----------------+-------------------+---------------+------------------+
|    max_cap      |       0 (0)       |    0.000      |       0 (0)      |
|    max_tran     |       0 (0)       |    0.000      |       0 (0)      |
|    max_fanout   |       0 (0)       |       0       |       0 (0)      |
|    max_length   |       0 (0)       |       0       |       0 (0)      |
+-----------------+-------------------+---------------+------------------+

Density:  64.165%
---------------------------------------------------------
Reported timing to dir timingReports
Total CPU time:  0.44 sec
Total Real time:  1.0 sec
Total Memory Usage:  1129.386719 Mbytes
innovus 3>
innovus 3> setDelayCalMode -SIAware true
innovus 4>
```

Routing

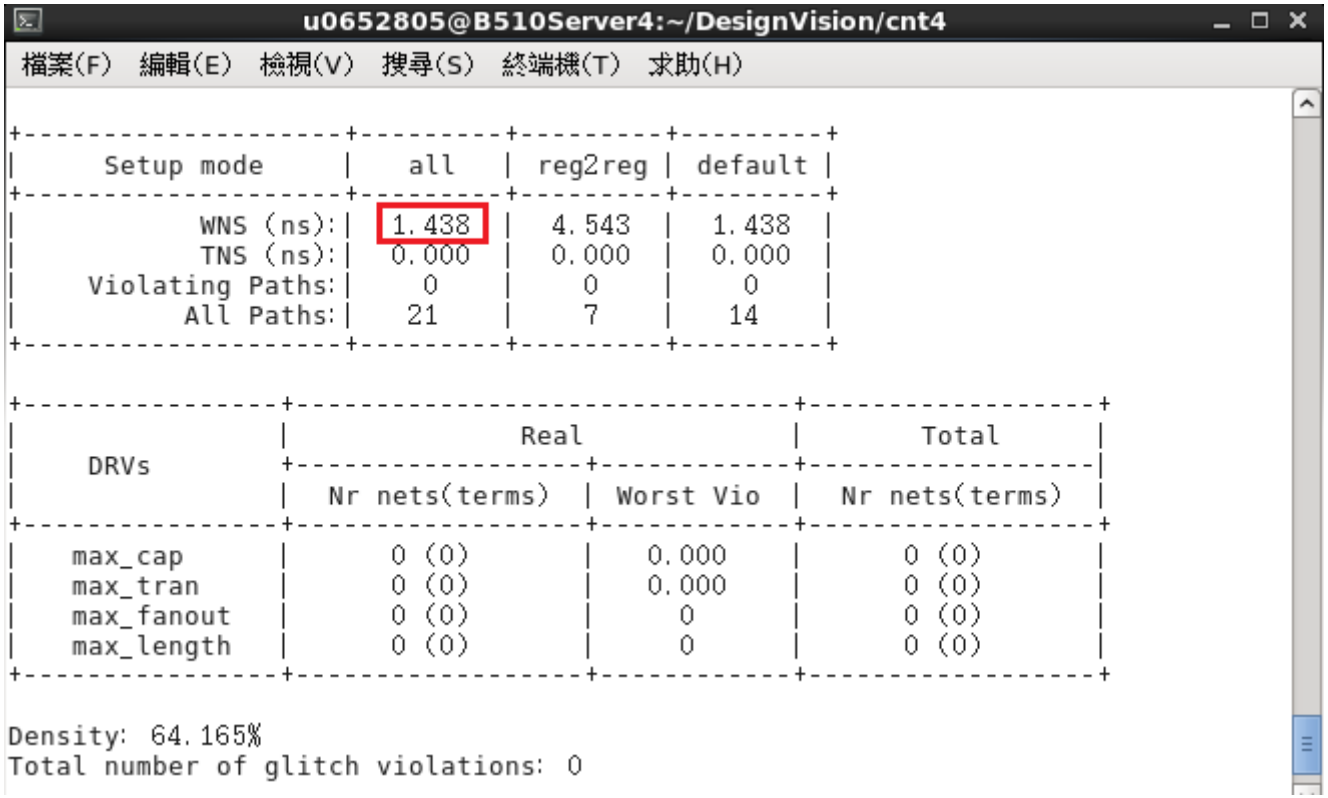
Report Timing





Routing

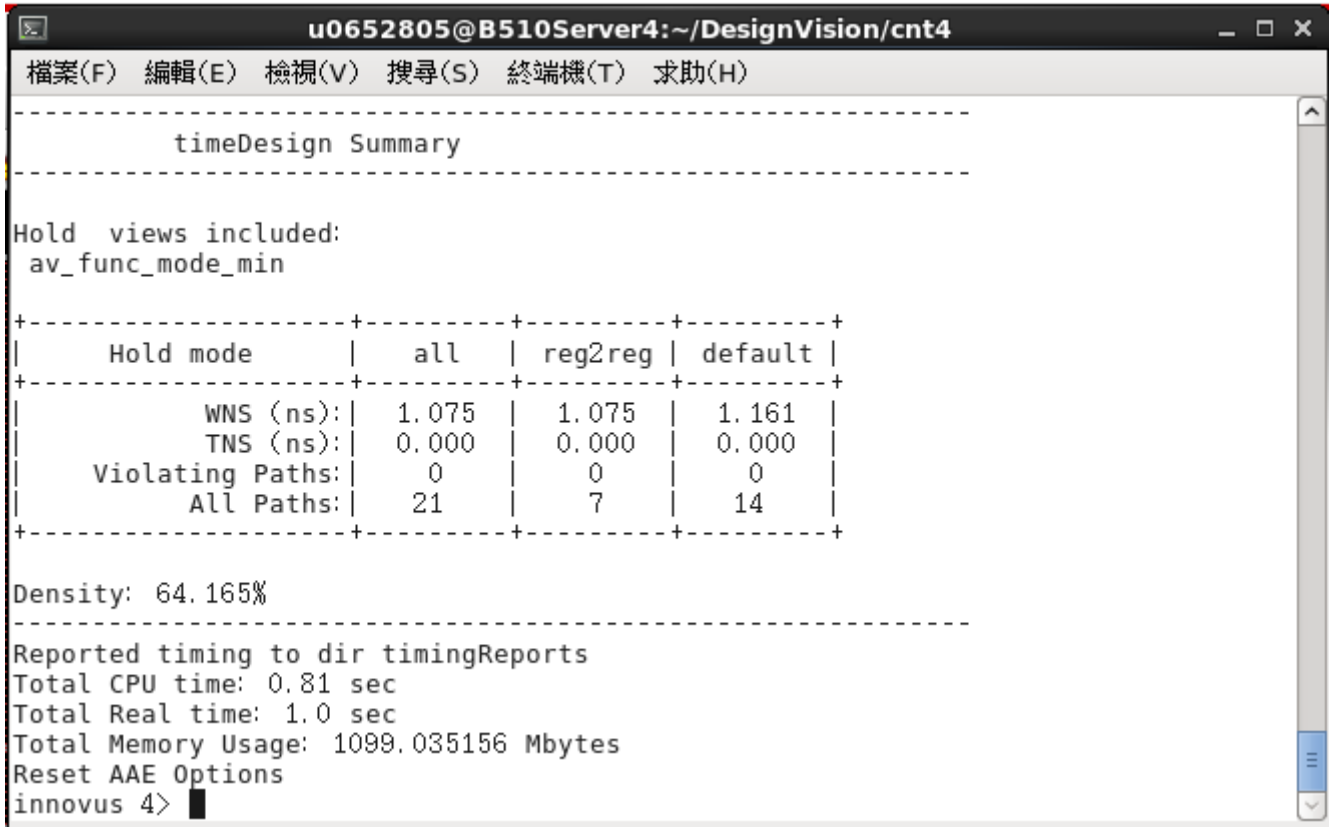
如果WNS為負需做Optimize



Routing

觀察Hold Time

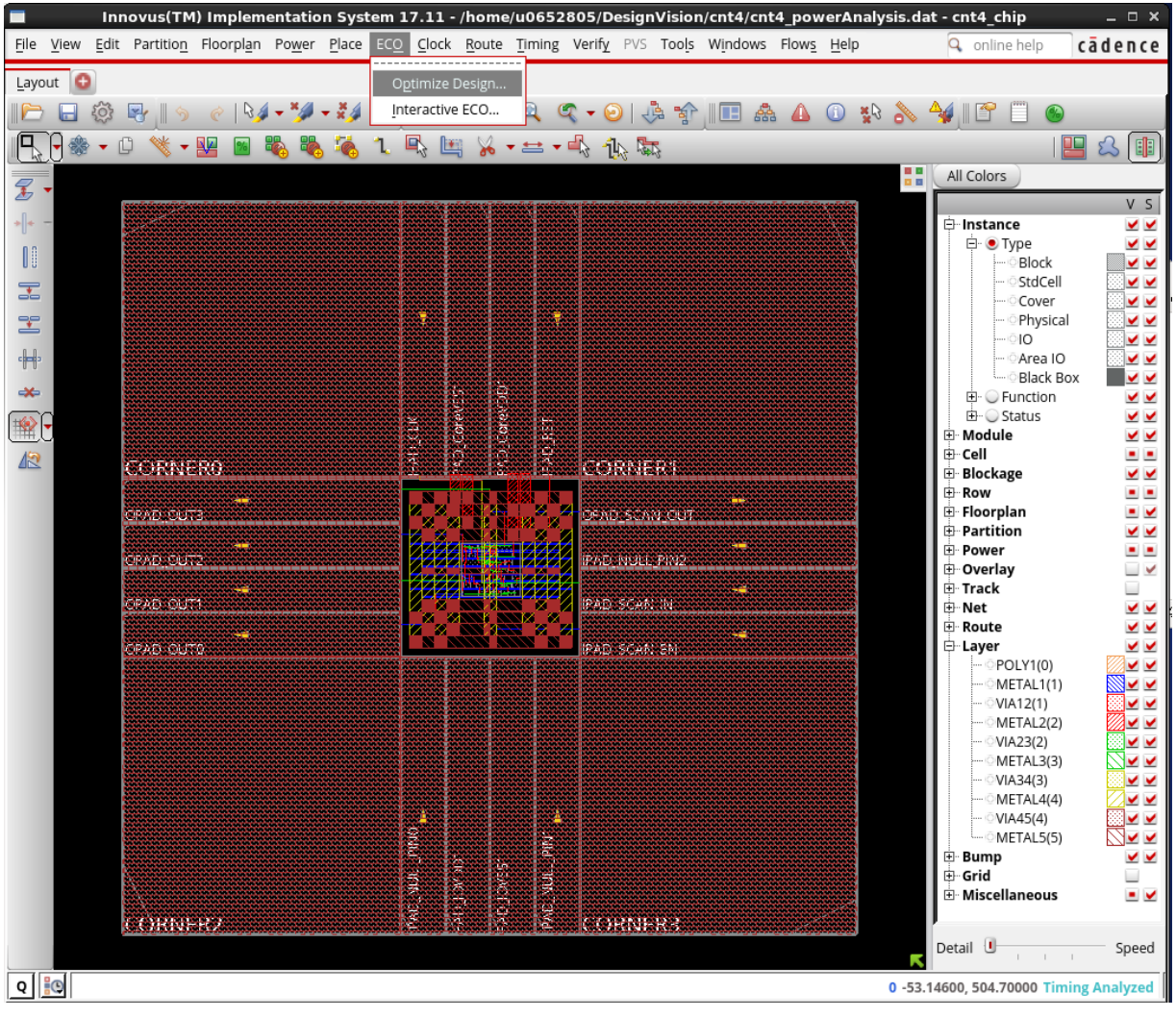
Routing


u0652805@B510Server4:~/DesignVision/cnt4
檔案(F) 編輯(E) 檢視(V) 搜尋(S) 終端機(T) 求助(H)
timeDesign Summary
Hold views included:
av_func_mode_min
Hold mode | all | reg2reg | default
WNS (ns): | 1.075 | 1.075 | 1.161
TNS (ns): | 0.000 | 0.000 | 0.000
Violating Paths: | 0 | 0 | 0
All Paths: | 21 | 7 | 14
Density: 64.165%
Reported timing to dir timingReports
Total CPU time: 0.81 sec
Total Real time: 1.0 sec
Total Memory Usage: 1099.035156 Mbytes
Reset AAE Options
innovus 4>

Routing

Post Route Optimization

如果Setup&Hold Time的WNS都為正可不做此步

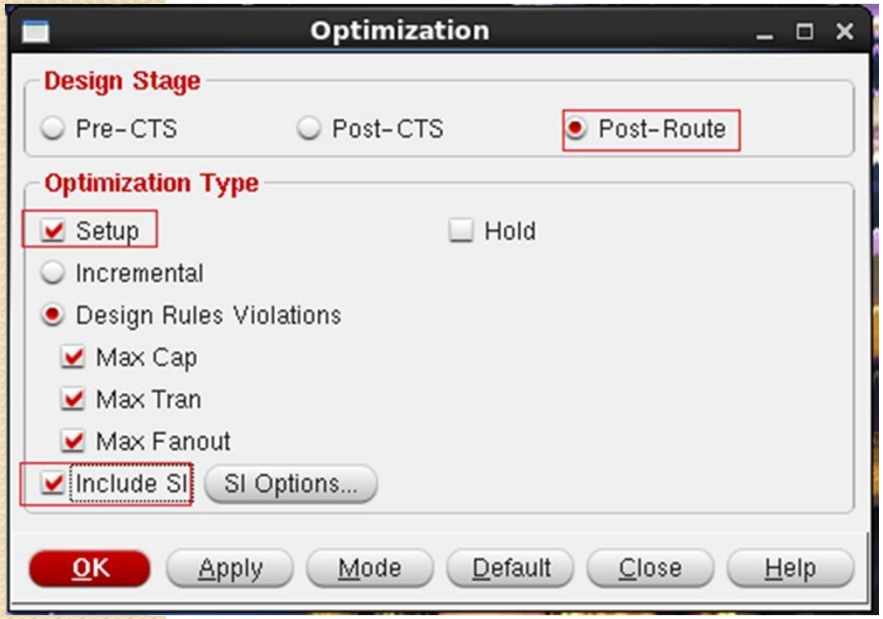


Routing

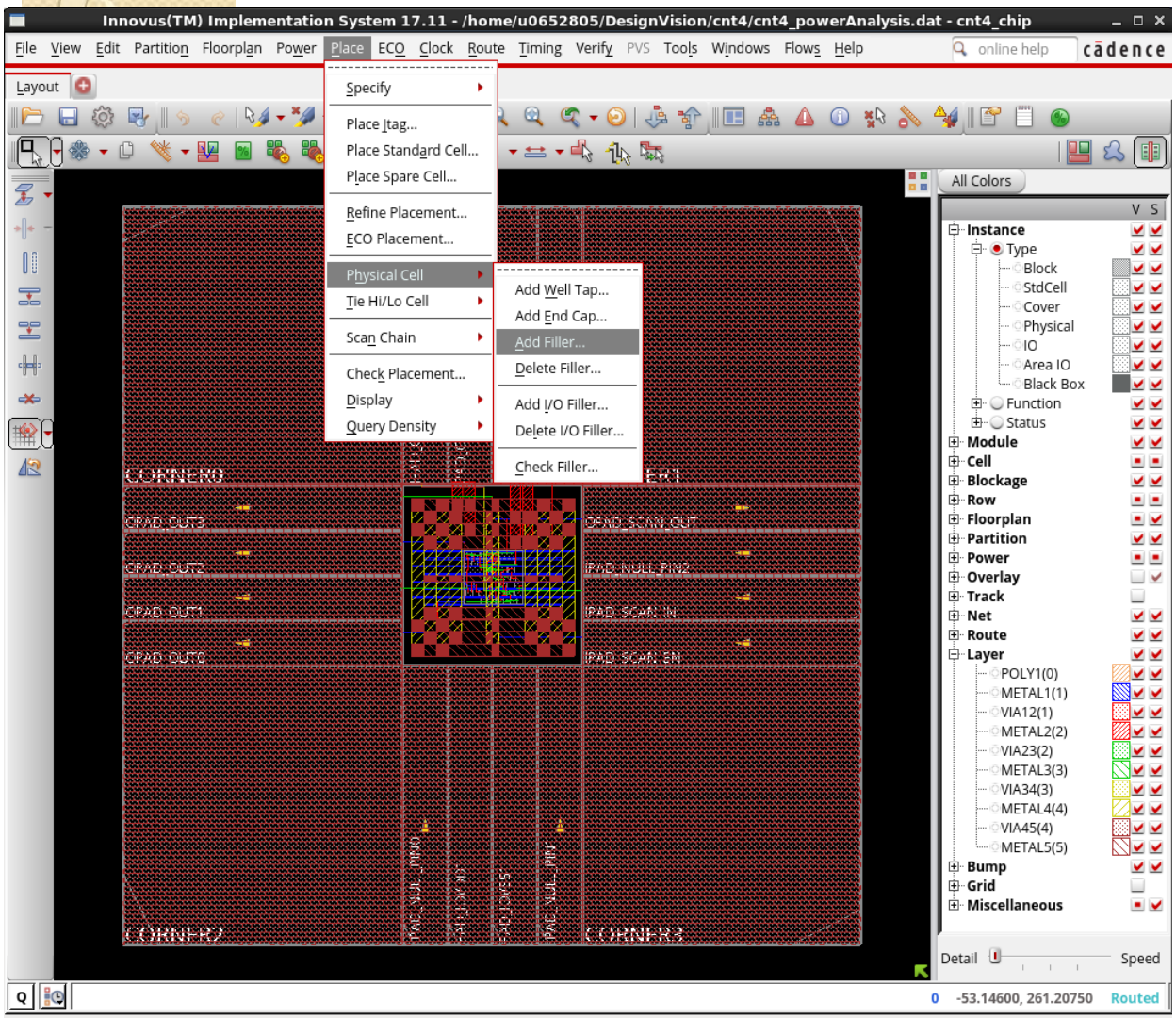
Post Route Optimization

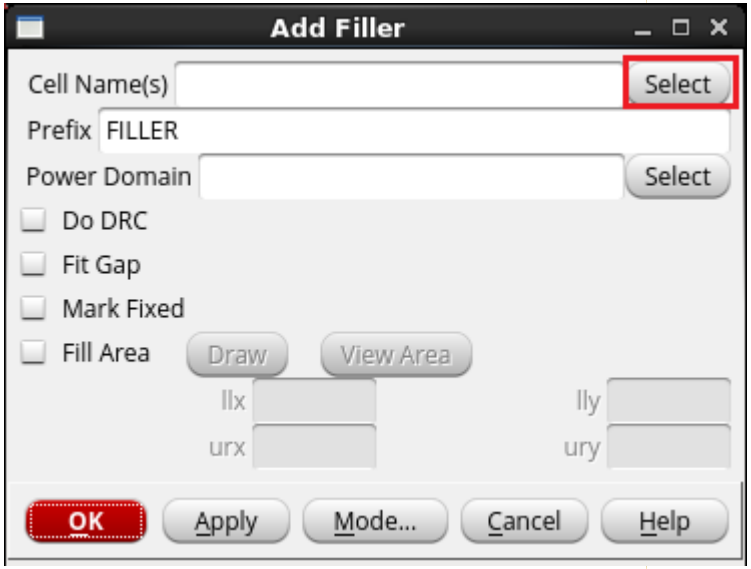
如果Setup&Hold Time的WNS都為正可不做此步。

如只有Setup Time有問題照左圖，如果有Hold Time則右圖。

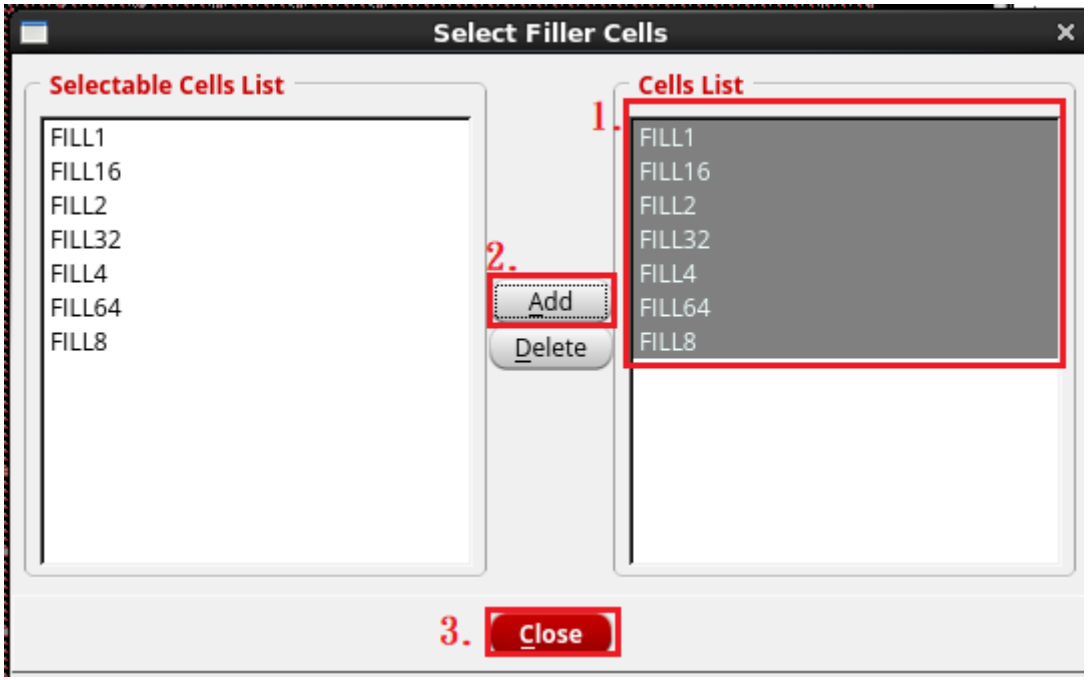


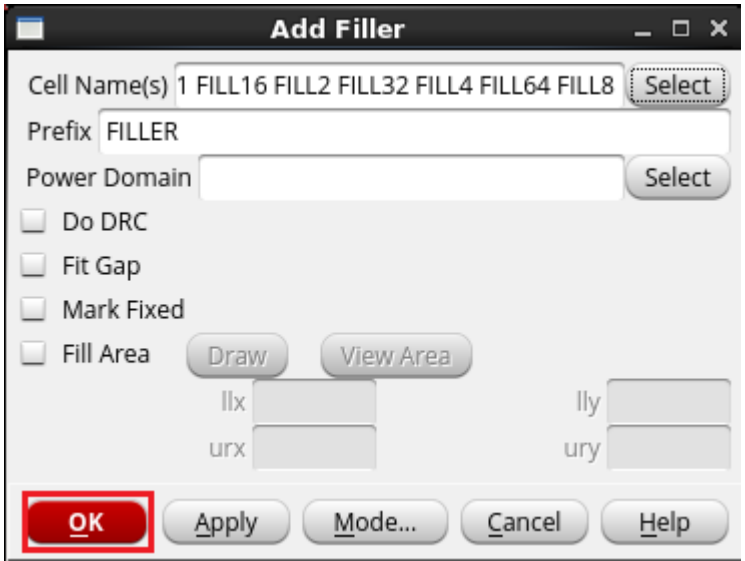
Add Filler


Innovus(TM) Implementation System 17.11 - /home/u0652805/DesignVision/cnt4/cnt4_powerAnalysis.dat - cnt4_chip
File View Edit Partition Floorplan Power Place ECO Clock Route Timing Verify PVS Tools Windows Flows Help
online help
cadence
Layout
Specify
Place Jtag...
Place Standard Cell...
Place Spare Cell...
Refine Placement...
ECO Placement...
Physical Cell
Tie Hi/Lo Cell
Scan Chain
Check Placement...
Display
Query Density
Add Well Tap...
Add End Cap...
Add Filler...
Delete Filler...
Add I/O Filler...
Delete I/O Filler...
Check Filler...
All Colors
Instance
Type
Block
StdCell
Cover
Physical
IO
Area IO
Black Box
Function
Status
Module
Cell
Blockage
Row
Floorplan
Partition
Power
Overlay
Track
Net
Route
Layer
POLY1(0)
METAL1(1)
VIA12(1)
METAL2(2)
VIA23(2)
METAL3(3)
VIA34(3)
METAL4(4)
VIA45(4)
METAL5(5)
Bump
Grid
Miscellaneous
CORNER0
CORNER1
CORNER2
CORNER3
CPAD_OUT3
CPAD_OUT2
CPAD_OUT1
CPAD_OUT0
IPAD_SCAN_OUT
IPAD_NULL_PIN2
IPAD_SCAN_IN
IPAD_SCAN_EN
Detail
Speed
0
-53.14600, 261.20750
Routed


Add Filler
Cell Name(s)
Select
Prefix
FILLER
Power Domain
Select
Do DRC
Fit Gap
Mark Fixed
Fill Area
Draw
View Area
llx
lly
urx
ury
OK
Apply
Mode...
Cancel
Help

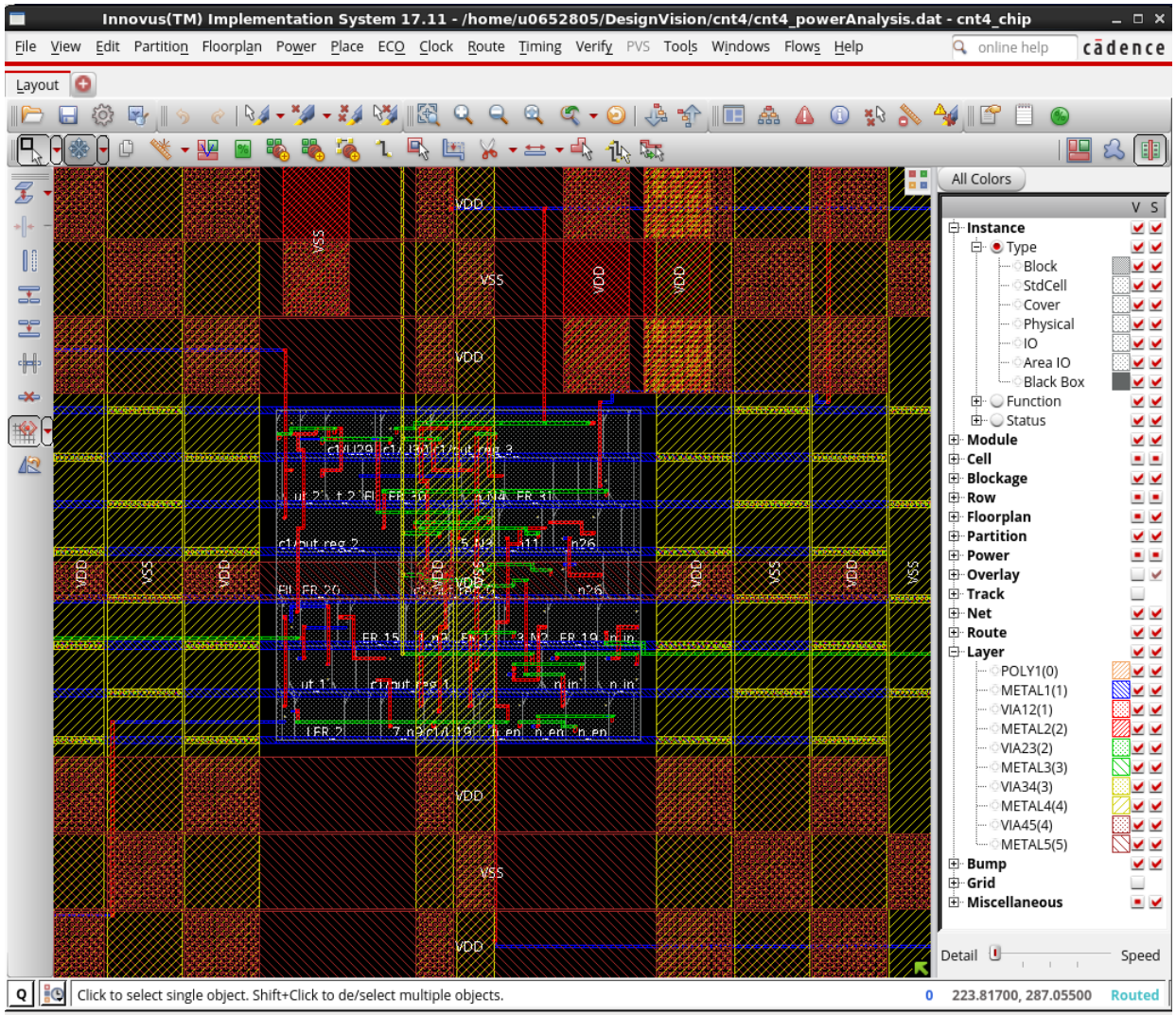
Add Filler


Select Filler Cells
Selectable Cells List
FILL1
FILL16
FILL2
FILL32
FILL4
FILL64
FILL8
Cells List
1.
FILL1
FILL16
FILL2
FILL32
FILL4
FILL64
FILL8
2.
Add
Delete
3.
Close


Add Filler
Cell Name(s) 1 FILL16 FILL2 FILL32 FILL4 FILL64 FILL8
Select
Prefix FILLER
Power Domain
Select
Do DRC
Fit Gap
Mark Fixed
Fill Area
Draw
View Area
llx
lly
urx
ury
OK
Apply
Mode...
Cancel
Help

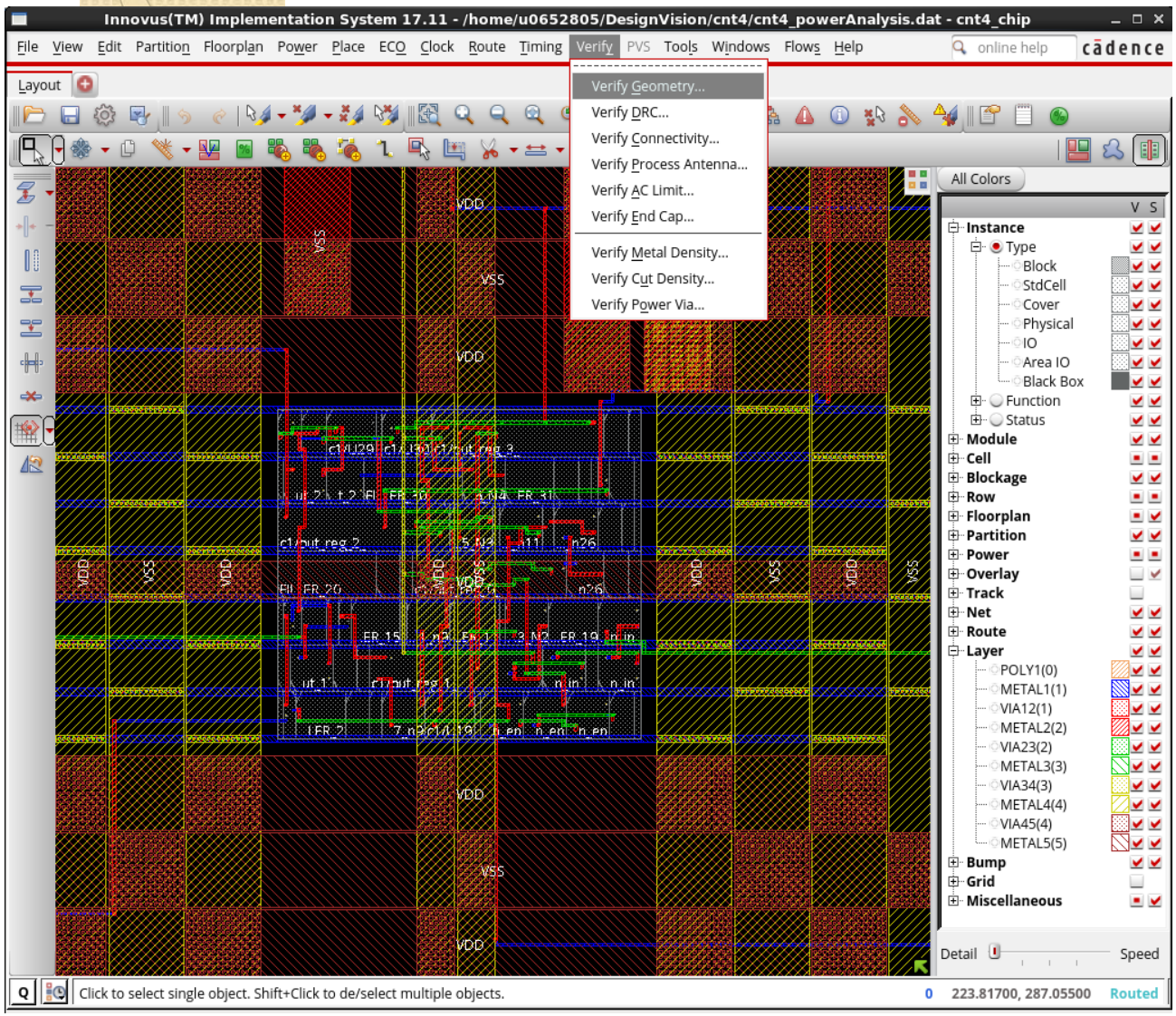
Add Filler

放大之後可以看到Core被Filler填滿

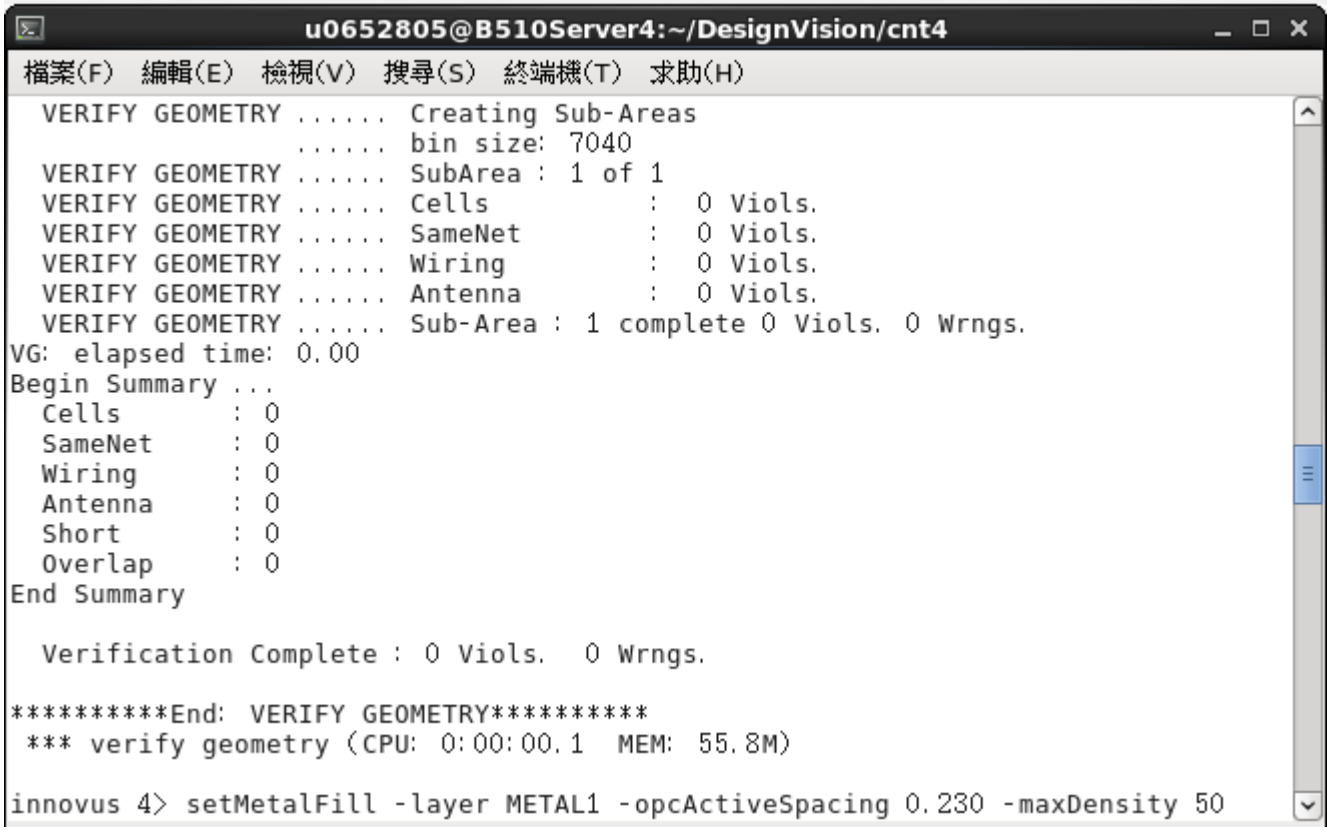


Add Filler

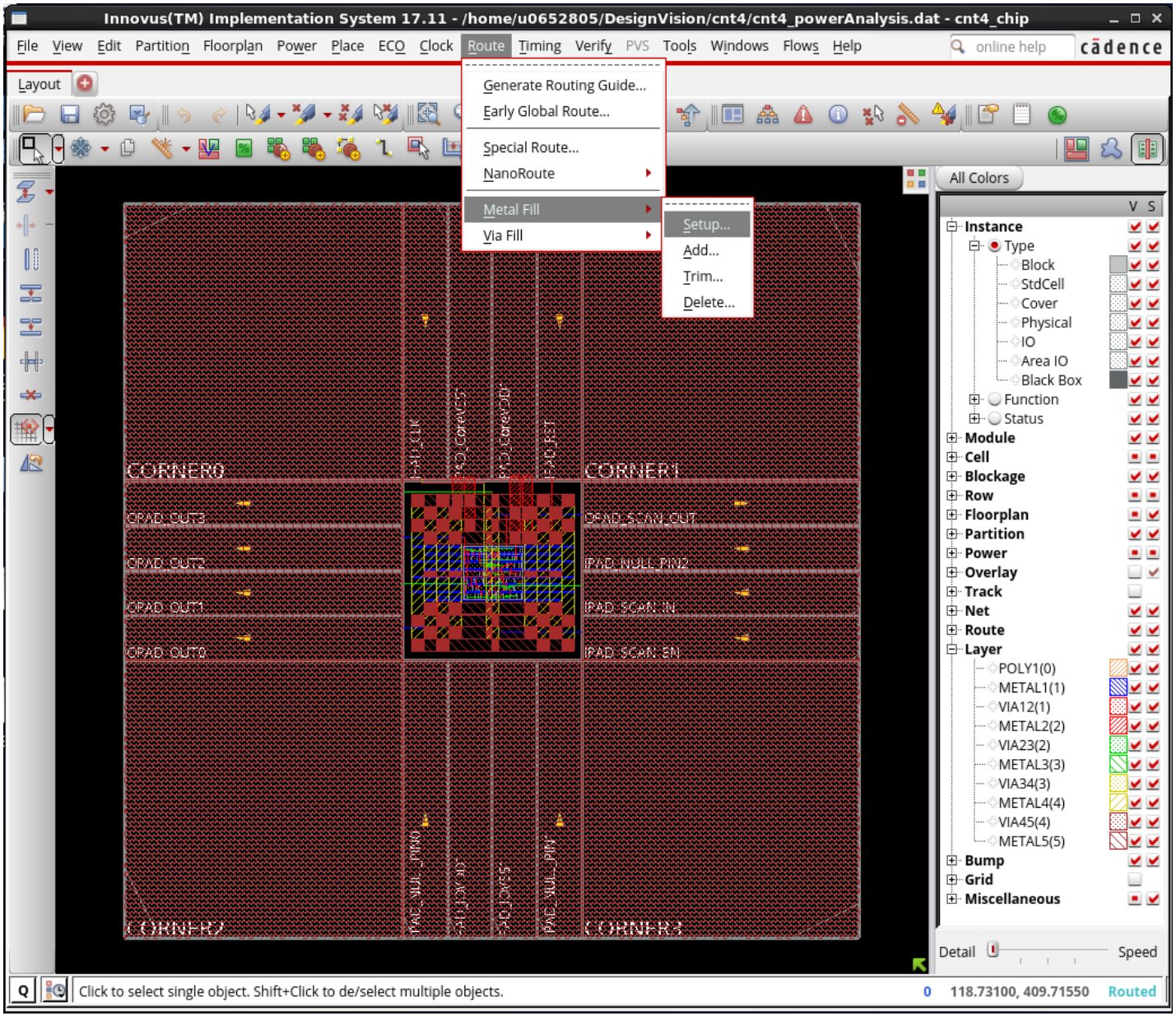
Verify



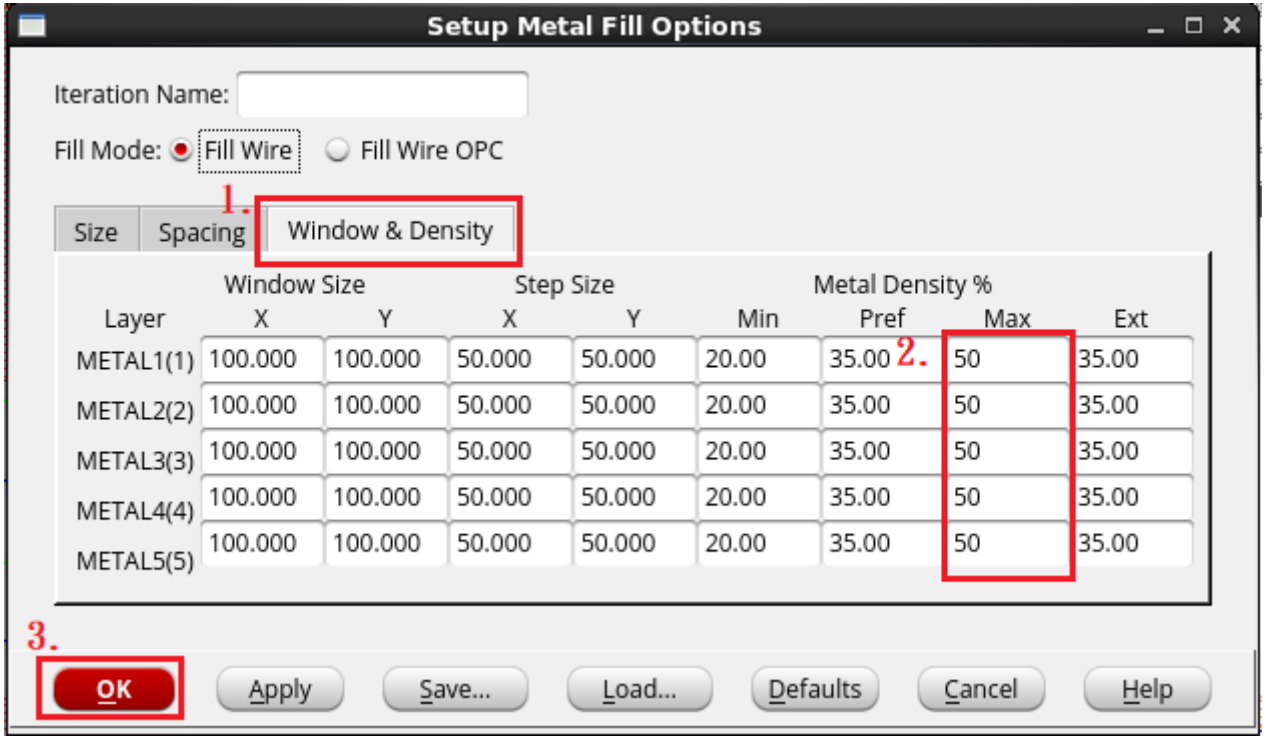
Add Filler


u0652805@B510Server4:~/DesignVision/cnt4
檔案(F) 編輯(E) 檢視(V) 搜尋(S) 終端機(T) 求助(H)
VERIFY GEOMETRY ..... Creating Sub-Areas
..... bin size: 7040
VERIFY GEOMETRY ..... SubArea : 1 of 1
VERIFY GEOMETRY ..... Cells : 0 Viols.
VERIFY GEOMETRY ..... SameNet : 0 Viols.
VERIFY GEOMETRY ..... Wiring : 0 Viols.
VERIFY GEOMETRY ..... Antenna : 0 Viols.
VERIFY GEOMETRY ..... Sub-Area : 1 complete 0 Viols. 0 Wrngs.
VG: elapsed time: 0.00
Begin Summary ...
Cells : 0
SameNet : 0
Wiring : 0
Antenna : 0
Short : 0
Overlap : 0
End Summary
Verification Complete : 0 Viols. 0 Wrngs.
**********End: VERIFY GEOMETRY**********
*** verify geometry (CPU: 0:00:00.1 MEM: 55.8M)
innovus 4> setMetalFill -layer METAL1 -opcActiveSpacing 0.230 -maxDensity 50

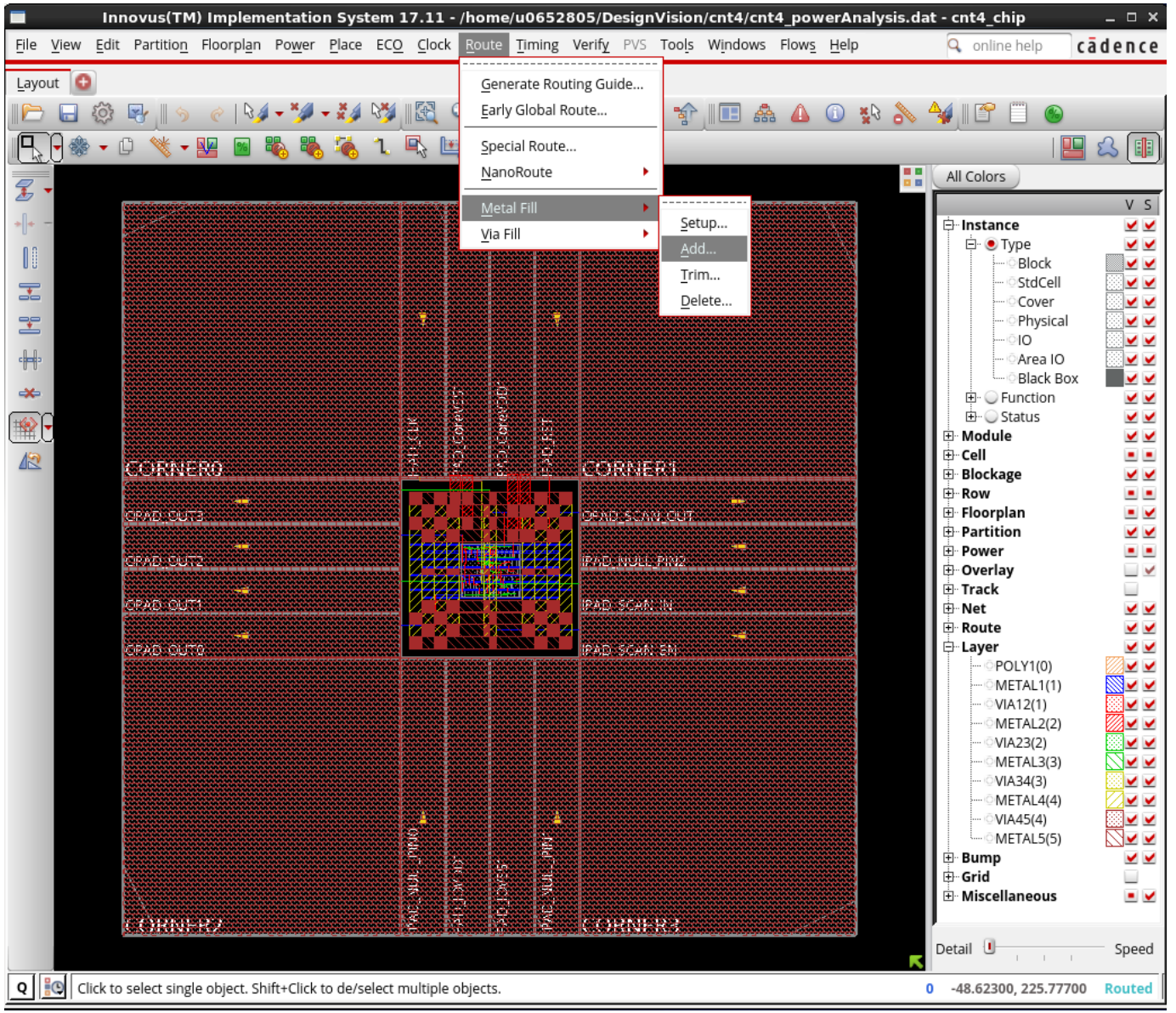
Add dummy Metal



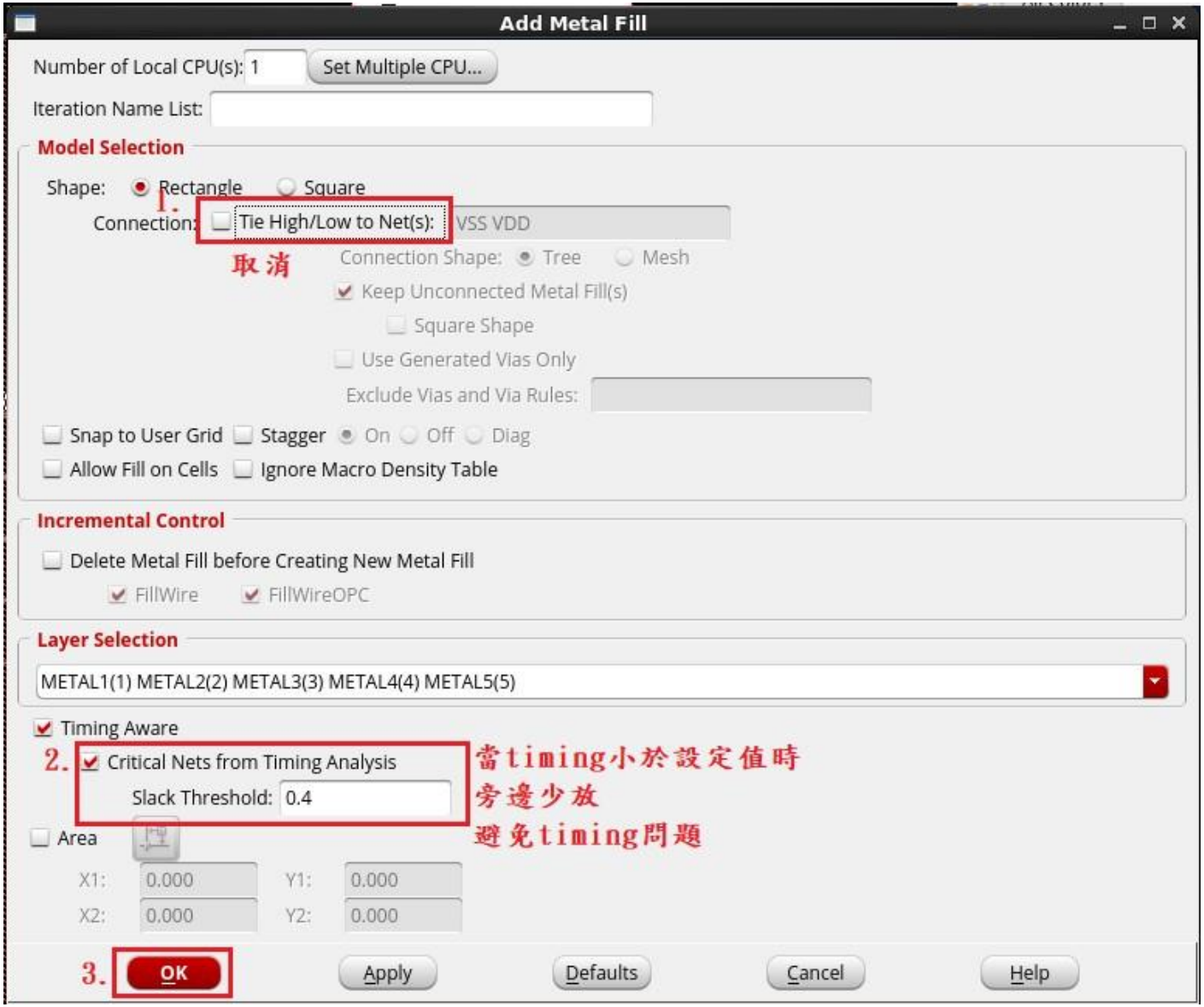
Add dummy Metal



Add dummy Metal

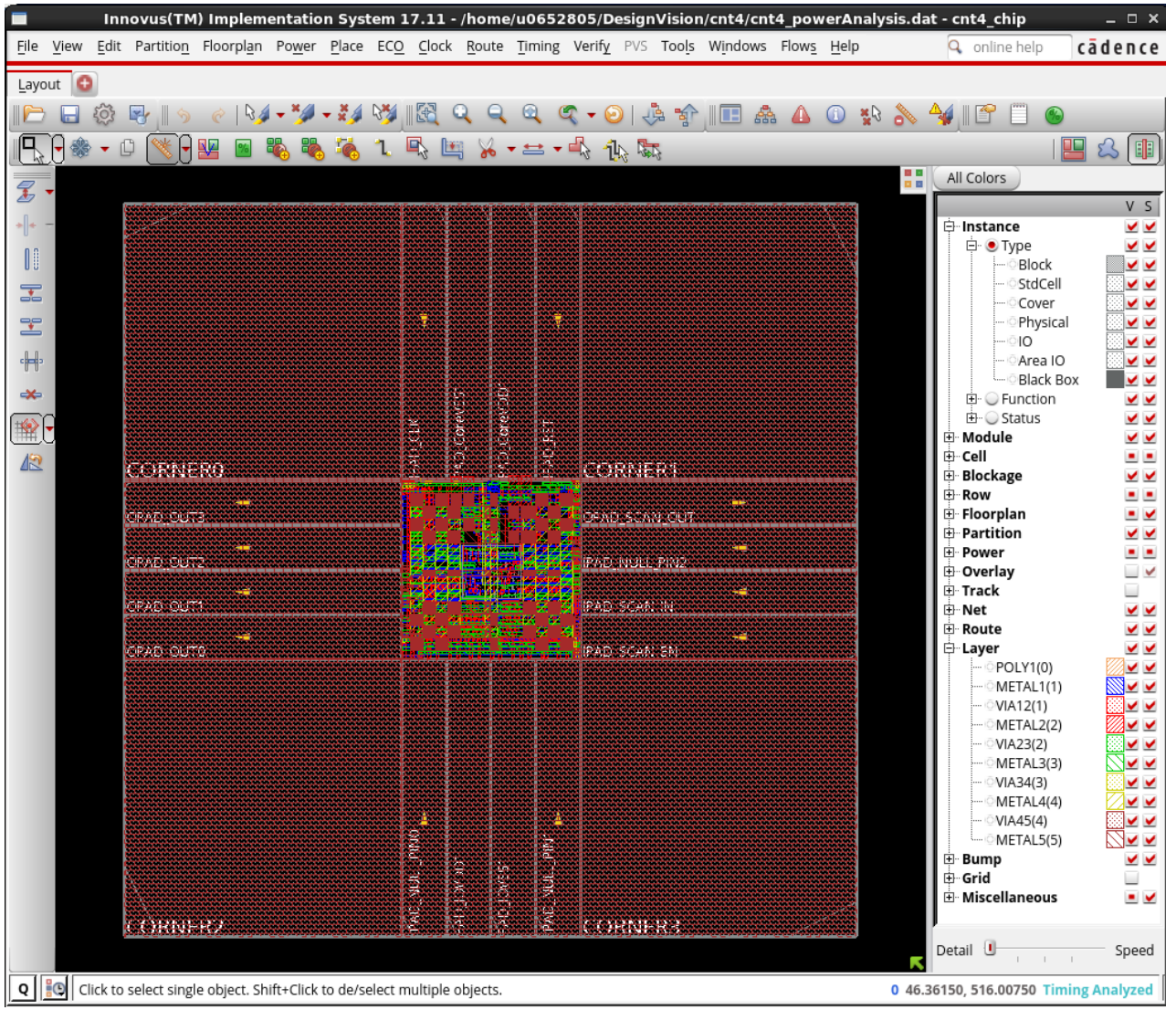


Add dummy Metal



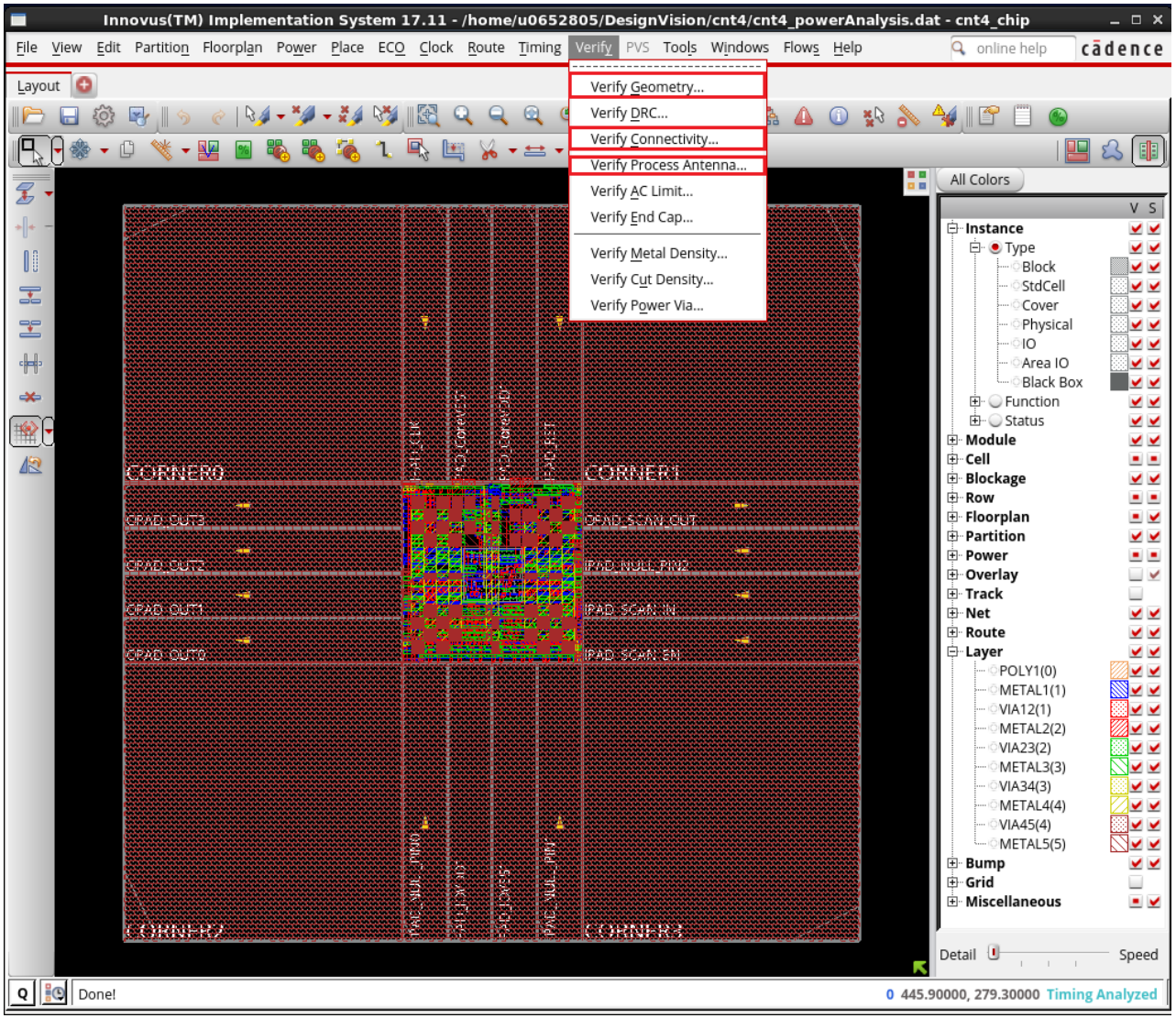
Add dummy Metal

可看到Dummy Metal已填滿



Add dummy Metal

Verify 這三個直接按ok後 確認無Viols即可



Add dummy Metal

u0652805@B510Server4:~/DesignVision/cnt4

檔案(F) 編輯(E) 檢視(V) 搜尋(S) 終端機(T) 求助(H)

```
  VERIFY GEOMETRY ......  Creating Sub-Areas
                  ......  bin size:  7040
  VERIFY GEOMETRY ......  SubArea :  1 of 1
  VERIFY GEOMETRY ......  Cells          :  0 Viols.
  VERIFY GEOMETRY ......  SameNet        :  0 Viols.
  VERIFY GEOMETRY ......  Wiring         :  0 Viols.
  VERIFY GEOMETRY ......  Antenna        :  0 Viols.
  VERIFY GEOMETRY ......  Sub-Area :  1 complete 0 Viols.  0 Wrngs.
VG:  elapsed time:  0.00
Begin Summary ...
  Cells       : 0
  SameNet     : 0
  Wiring      : 0
  Antenna     : 0
  Short       : 0
  Overlap     : 0
End Summary

  Verification Complete :  0 Viols.   0 Wrngs.

**********End:  VERIFY GEOMETRY**********
 *** verify geometry (CPU:  0:00:00.1   MEM:  0.0M)

innovus 4> VERIFY_CONNECTIVITY use new engine.
```

u0652805@B510Server4:~/DesignVision/cnt4

檔案(F) 編輯(E) 檢視(V) 搜尋(S) 終端機(T) 求助(H)

```
 *** verify geometry (CPU:  0:00:00.1   MEM:  0.0M)

innovus 4> VERIFY_CONNECTIVITY use new engine.

******** Start:  VERIFY CONNECTIVITY ********
Start Time:  Tue Dec 18 16:05:12 2018

Design Name:  cnt4_chip
Database Units:  2000
Design Boundary:  (0.0000,  0.0000) (490.0000,  490.0000)
Error Limit = 1000;  Warning Limit = 50
Check all nets

Begin Summary
  Found no problems or warnings.
End Summary

End Time:  Tue Dec 18 16:05:12 2018
Time Elapsed:  0:00:00.0

******** End:  VERIFY CONNECTIVITY ********
  Verification Complete :  0 Viols.   0 Wrngs.
  (CPU Time:  0:00:00.0   MEM:  0.000M)
```

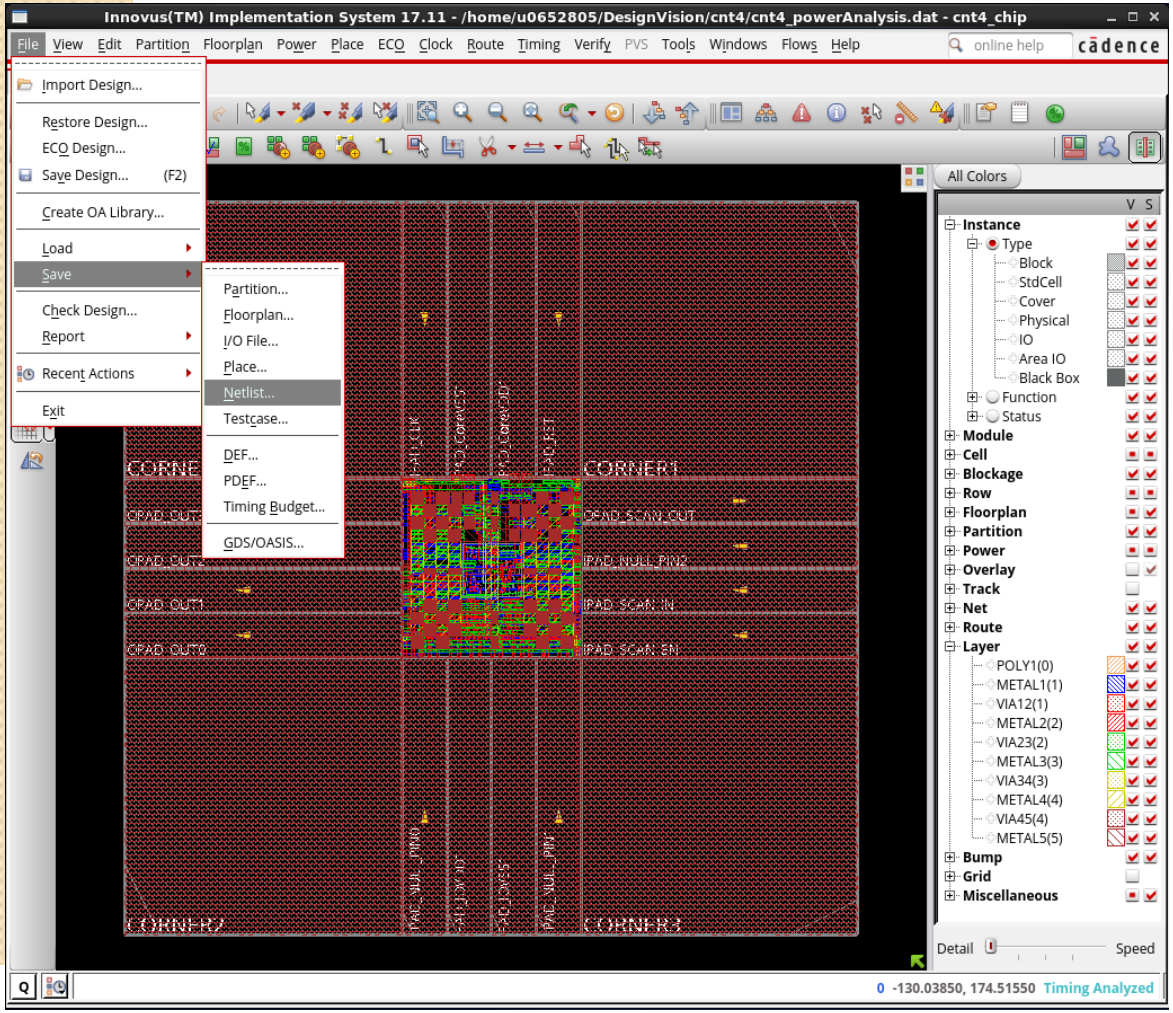
u0652805@B510Server4:~/DesignVision/cnt4

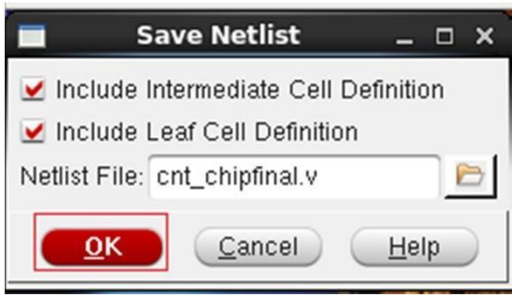
檔案(F) 編輯(E) 檢視(V) 搜尋(S) 終端機(T) 求助(H)

```
Design Boundary:  (0.0000,  0.0000) (490.0000,  490.0000)
Error Limit = 1000;  Warning Limit = 50
Check all nets

Begin Summary
  Found no problems or warnings.
End Summary

End Time:  Tue Dec 18 16:05:12 2018
Time Elapsed:  0:00:00.0

******** End:  VERIFY CONNECTIVITY ********
  Verification Complete :  0 Viols.   0 Wrngs.
  (CPU Time:  0:00:00.0   MEM:  0.000M)

innovus 4>
******* START VERIFY ANTENNA ********
Report File:  cnt4_chip.antenna.rpt
LEF Macro File:  cnt4_chip.antenna.lef
Verification Complete:  0 Violations
******* DONE VERIFY ANTENNA ********
(CPU Time:  0:00:00.0   MEM:  0.000M)

innovus 4>
```

PrimeTime PowerAnalysis

做完上述Routing等動作後，已趨近完成階段，做最後一次的Power分析是最接近真實電路的狀況。先儲存Netlist，檔名加Final區別。

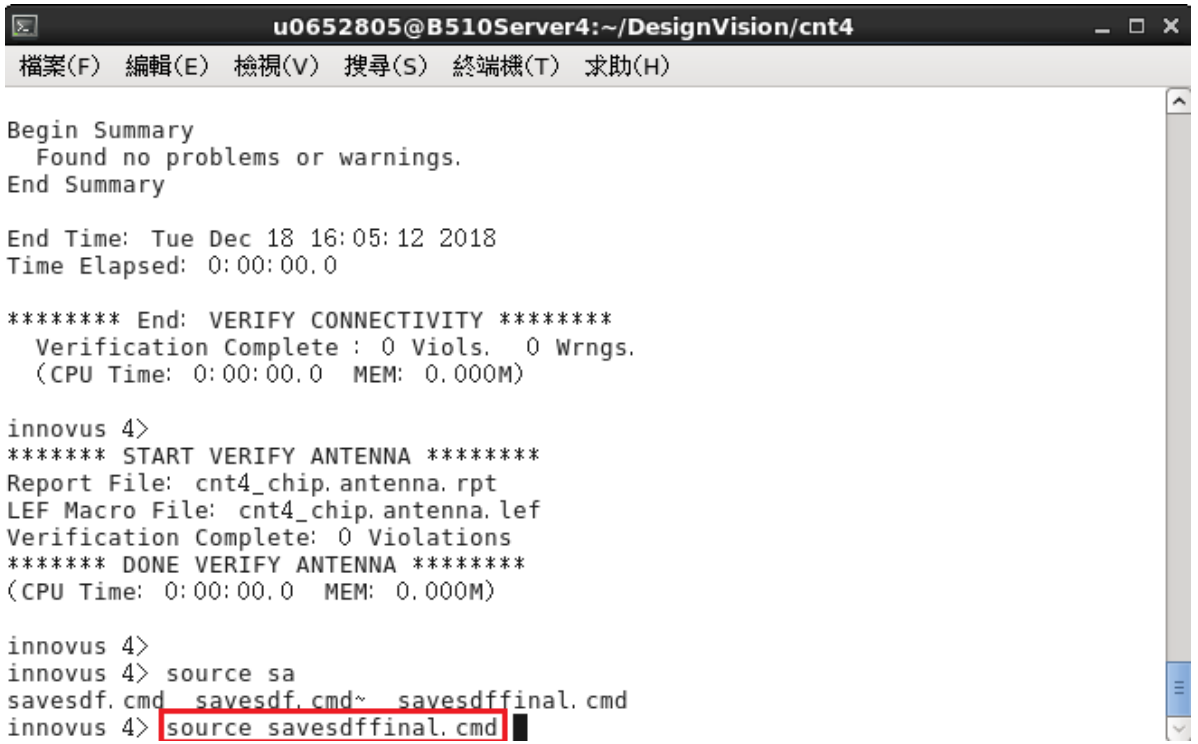




PrimeTime PowerAnalysis

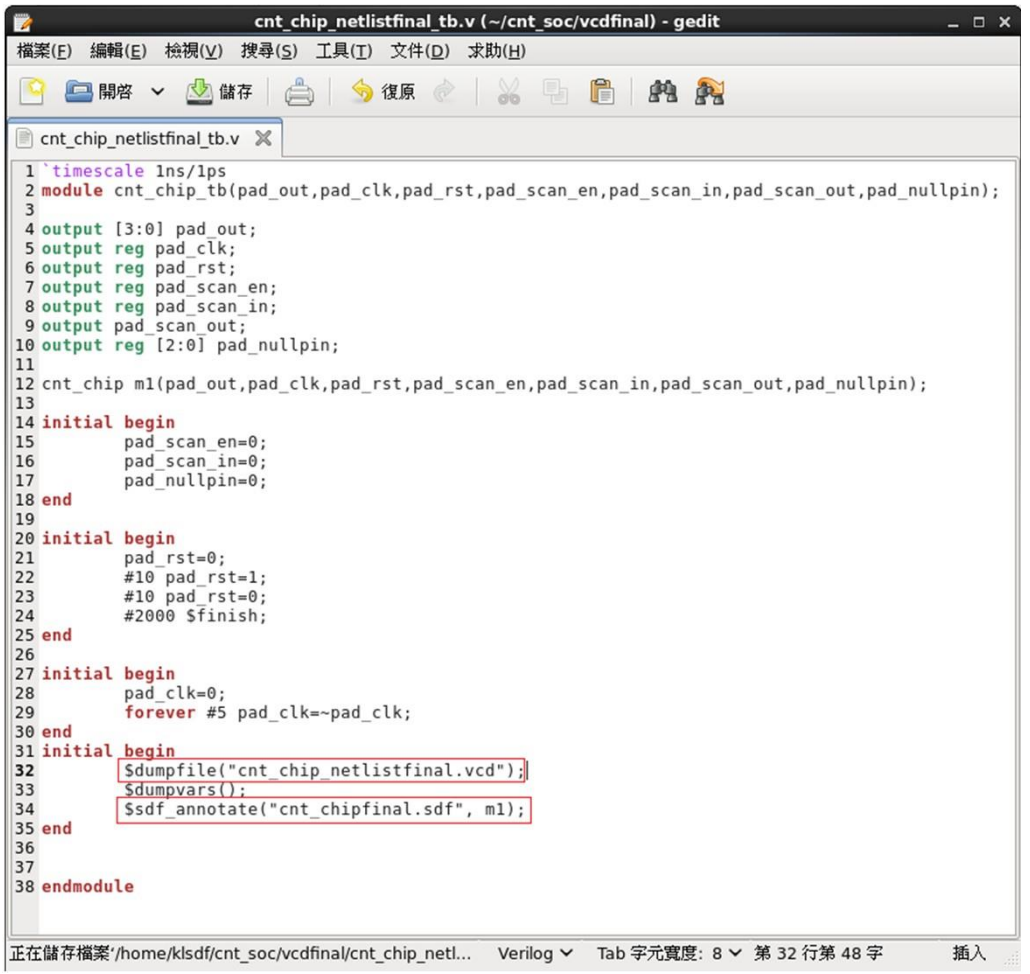
儲存SDF，複製Chap7的savesdf.cmd，將儲存檔名多加final並修改內容如下，並直接用Innovus打source savesdffinal.cmd

```
setAnalysisMode -analysisType bcwc
write_sdf -max_view av_func_mode_max \
        -min_view av_func_mode_min \
        -edges noedge -splitsetuphold -remashold -splitrecrem \
        -min_period_edges none cnt_chipfinal.sdf
```



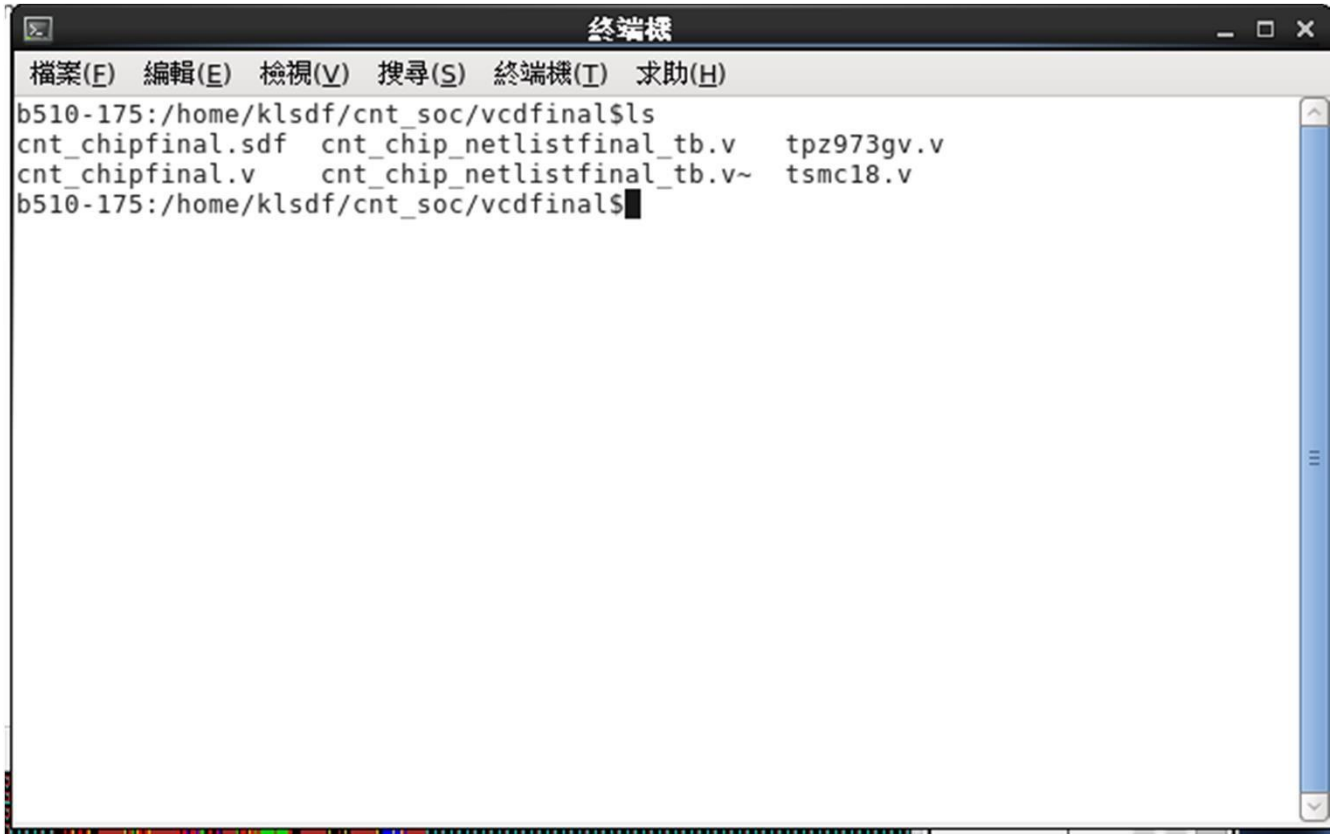
PrimeTime PowerAnalysis

複製Chap7的Testbench只改dumpfile與sdf_annotate另存為cnt_chip_netlistfinal_tb.v



PrimeTime PowerAnalysis

新增一個vcdfinal的資料夾確認有以下檔案後，照Chap7 p31所教的產生vcd



PrimeTime PowerAnalysis

PrimeTime DC File，至工作站的pt資料夾下抓取下來修改。

cnt_chip_netlistfinal.dc

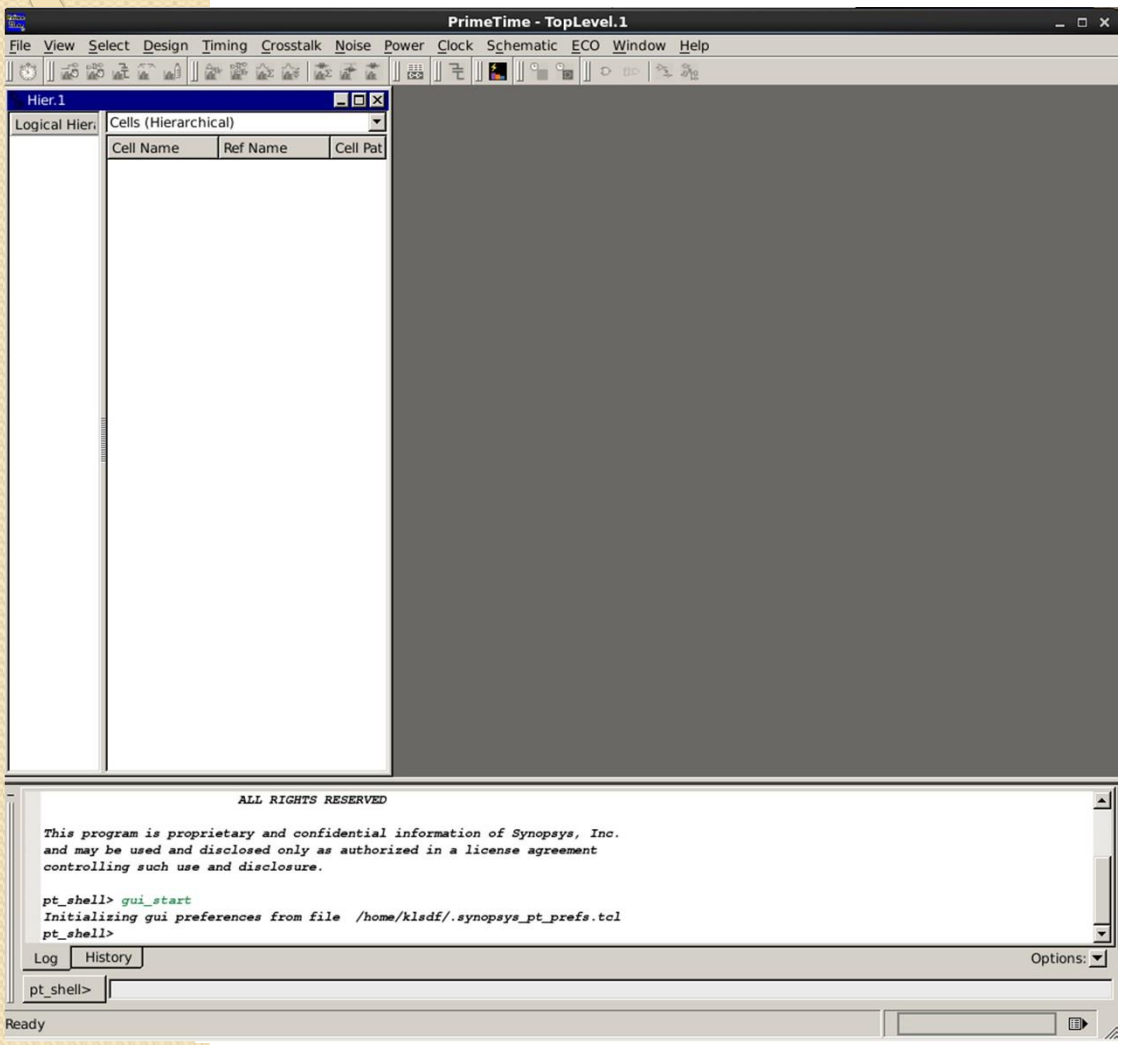
```
1  set designer "SOC"
2  set company "VLSIDA Lab."
3
4  set lib_base /cad/techfile
5
6  #/*TSMC018 1p6m*/
7  set search_path "/usr/techfile/CBDK_TSMC018_Arm_v3.2/CIC/SynopsysDC/db $search_path"
8  set link_library "* slow.db fast.db tpz973gvwc.db tpz973gvbc.db"
9  set target_library "slow.db fast.db"
10
11
12 set power_enable_analysis TRUE
13 set power_analysis_mode time_based
14
15 read_verilog ./cnt_chip_netlistfinal.v
16 current_design cnt_chip
17 link
18
19 # -strip_path  [testbench name] / [include module name] [vcd name]
20 read_vcd -strip_path cnt_chip_tb/m1 ./cnt_chip_netlistfinal.vcd
21
22
23 set_power_analysis_options -waveform_format fsdb -waveform_output pwr -waveform_interval 1
24 update_power
25
26 redirect -bg -file power.rpt {report_power -hierarchy}
27 report_power
```

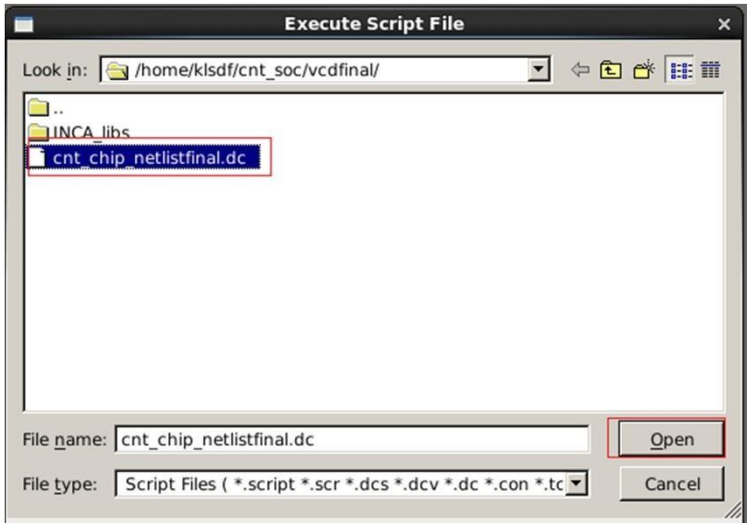
主程式netlist

TestBench裡Module與Intance Name與VCD檔名

PrimeTime PowerAnalysis

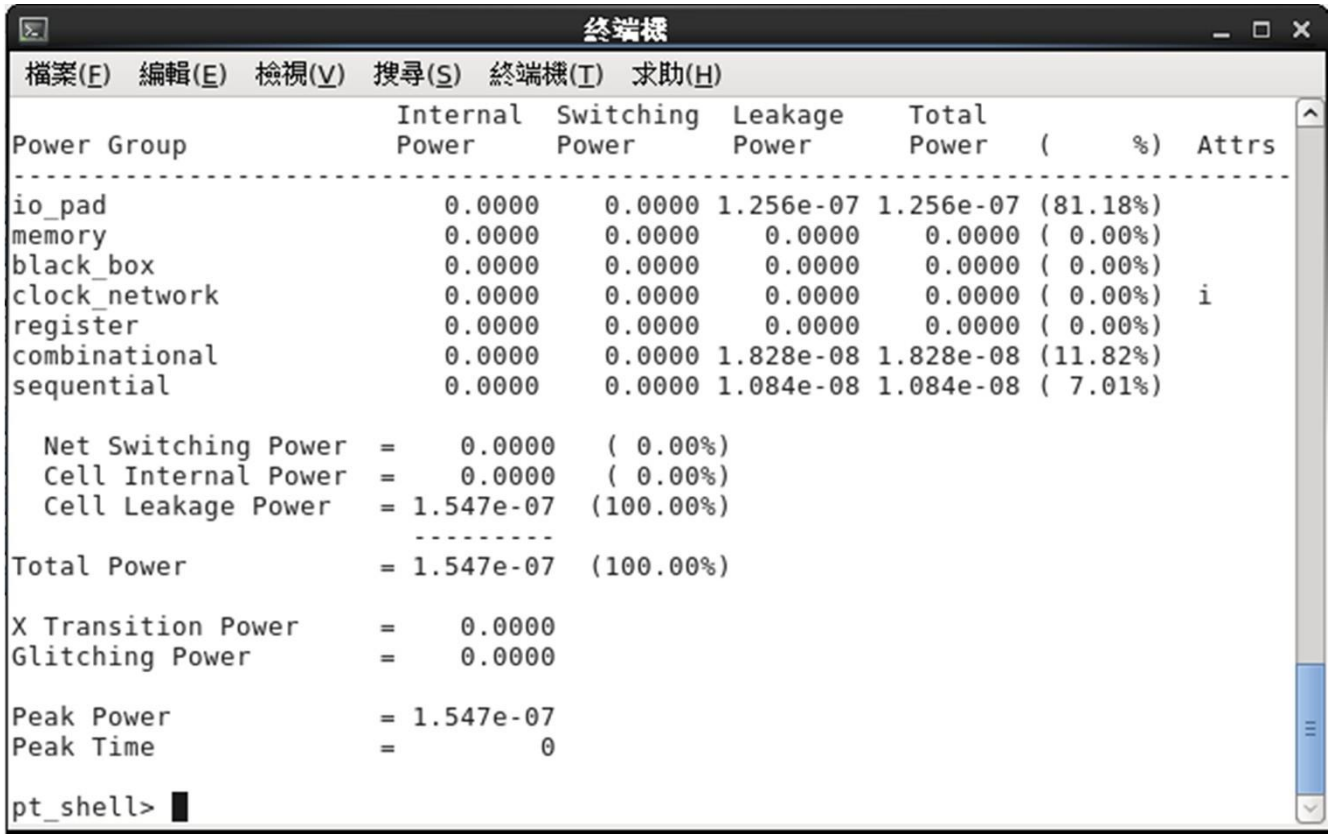
在Terminal打pt執行PrimeTime並載入dc





PrimeTime PowerAnalysis

載入成功後就可以在Terminal看到power資訊



PrimeTime PowerAnalysis

目錄下有power.rpt用gedit打開觀看細部power資訊

cnt_chip_netlistfinal.dc | power.rpt

```
 1 [457]  Start Time:  Wed Dec 26 18:18:52 2012
 2
 3 ****************************************
 4 Report : Time Based Power
 5         -hierarchy
 6 Design : cnt_chip
 7 Version: E-2010.12-SP3-1
 8 Date   : Wed Dec 26 18:18:52 2012
 9 ****************************************
10
11
12
13                                      Switch   Int      Leak      Total
14 Hierarchy                            Power    Power    Power     Power    %
15 ------------------------------------------------------------------------------
16 cnt_chip                                0.000    0.000 1.55e-07  1.55e-07 100.0
17   k1 (cnt)                              0.000    0.000 2.56e-08  2.56e-08  16.5
18
19
20                                      Peak     Peak            Glitch   X-tran
21 Hierarchy                            Power    Time            Power    Power
22 ------------------------------------------------------------------------------
23 cnt_chip                             1.55e-07       0-1          0.000    0.000
24   k1 (cnt)                           2.56e-08       0-1          0.000    0.000
25 [457]  Finish Time:  Wed Dec 26 18:18:52 2012
26
```