ASIC教材

Chapter3 Gate-Level模擬

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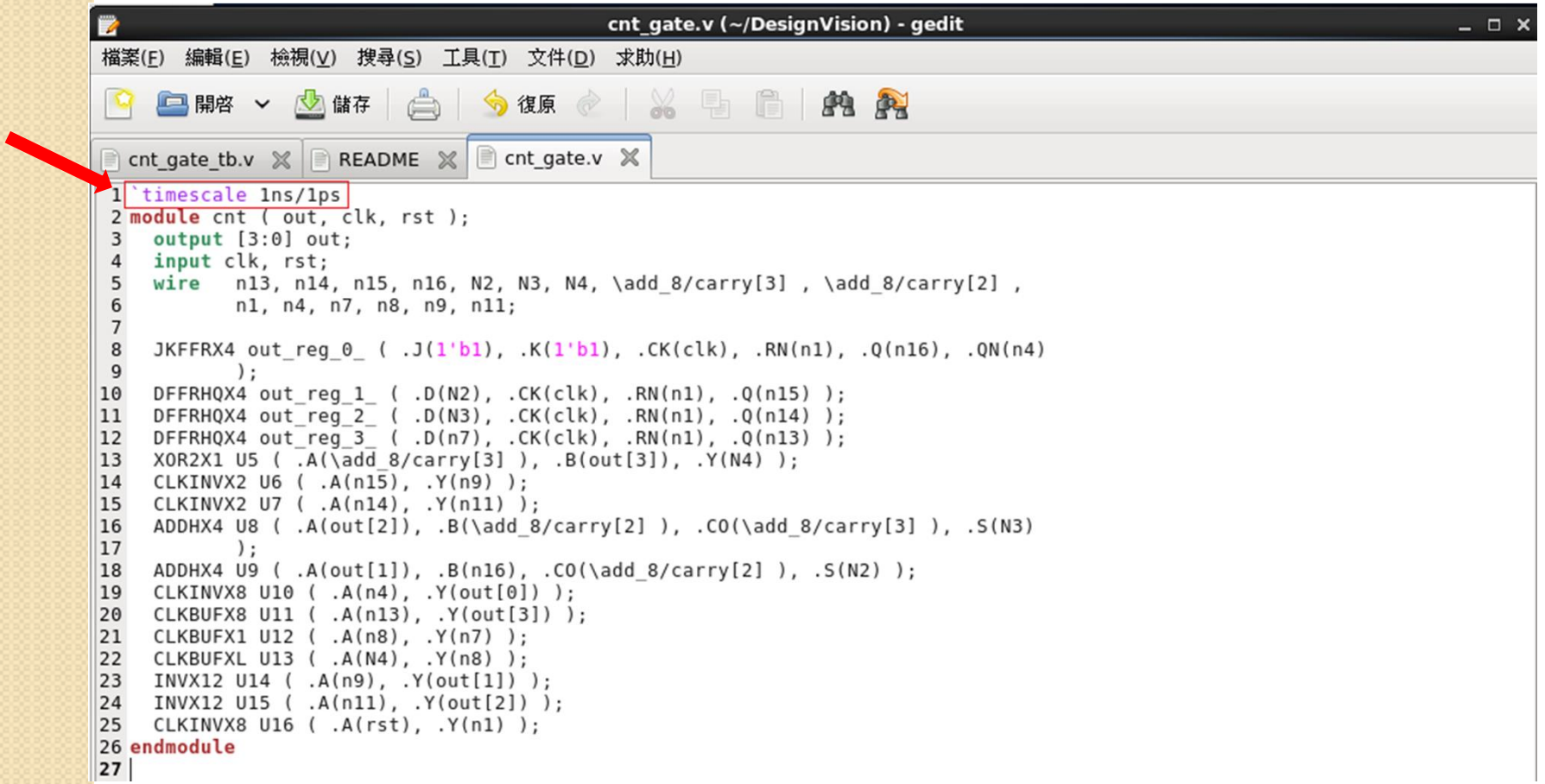
2021/1/29再編

目錄

- Gate-Level 模擬。
- Debussy驗證。

Gate-Level 模擬

- 在剛剛的cnt_gate.v增加timescale，不然等等會跟製程檔案不同時間單位會無法模擬。



Gate-Level 模擬

- 新增一個cnt_gate_tb.v。
- $sdf_annotate就是要把Chapter 2所產生的SDF匯入進行模擬。第一個參數填入SDF的檔名，第二個為Instance Name。

```
1  `timescale 1ns/1ps
2  module cnt_tb();
3  wire [3:0] out;
4  reg clk,rst;
5  cnt c1(out, clk, rst);
6
7  initial begin
8     rst=0;
9     #1 rst=1;
10    #1 rst=0;
11    #10000 $finish;
12
13 end
14
15 initial begin
16    clk=0;
17    forever #5 clk=~clk;
18 end
19
20 initial begin
21    $sdf_annotate("cnt_gate.sdf",c1);
22    $fsdbDumpfile("cnt_gate_tb.fsdb");
23    $fsdbDumpvars;
24 end
25
26 endmodule
27
28
29
```

Clock Period照DV合成設定

第二章自行設定的名稱

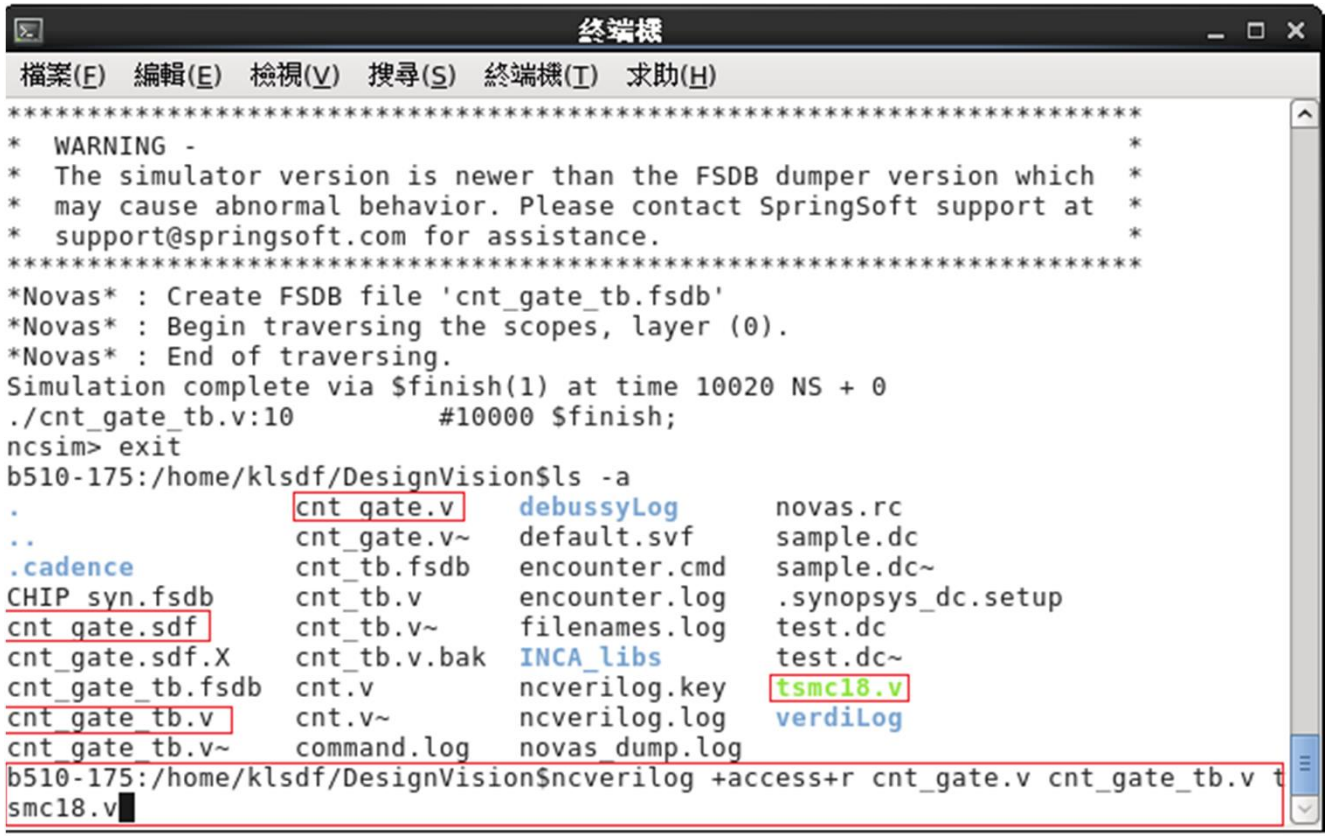
填入SDF要套用的Module Instance Name

Gate-Level 模擬

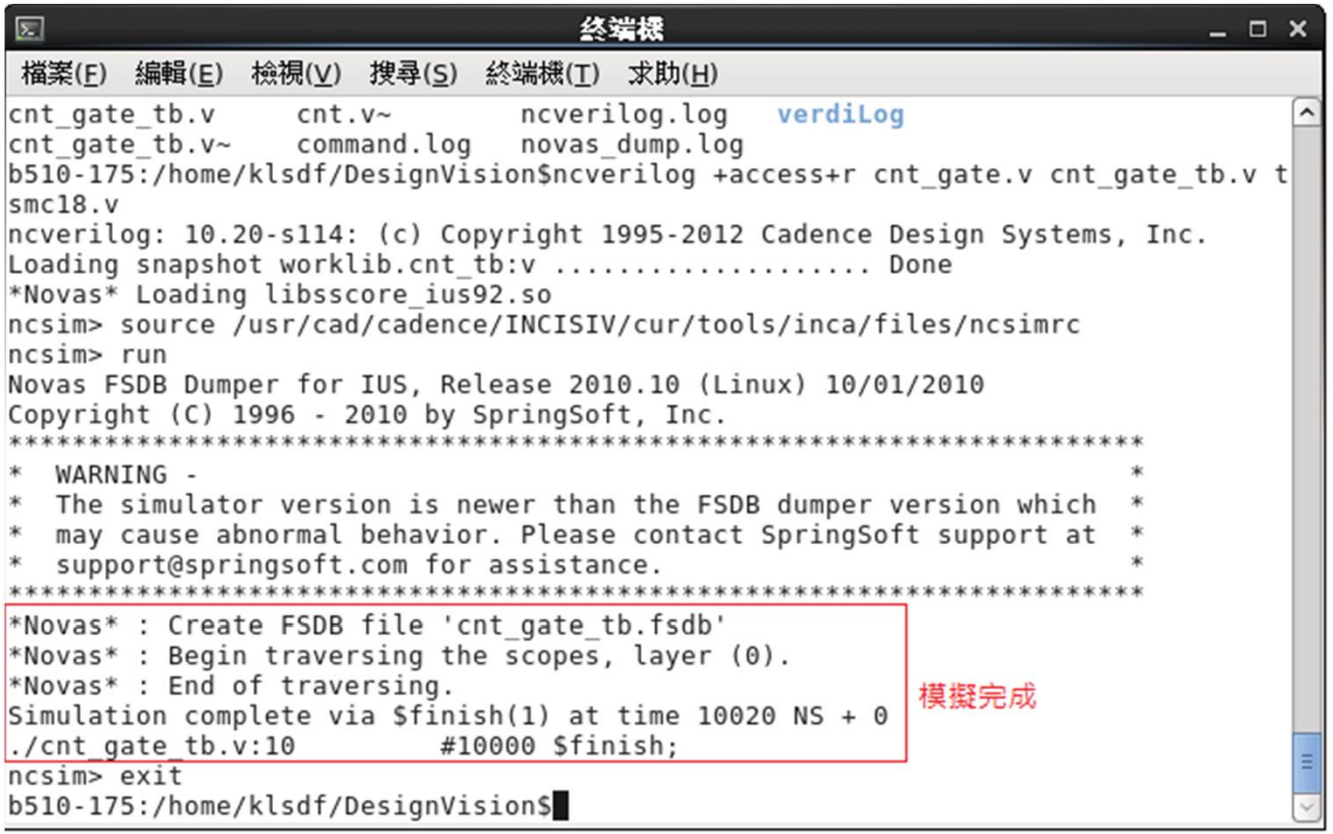
- 把教材中的tsmc18.v上傳到同一個目錄中，之後打入

  ncverilog +access+r cnt_gate.v cnt_gate_tb.v tsmc18.v

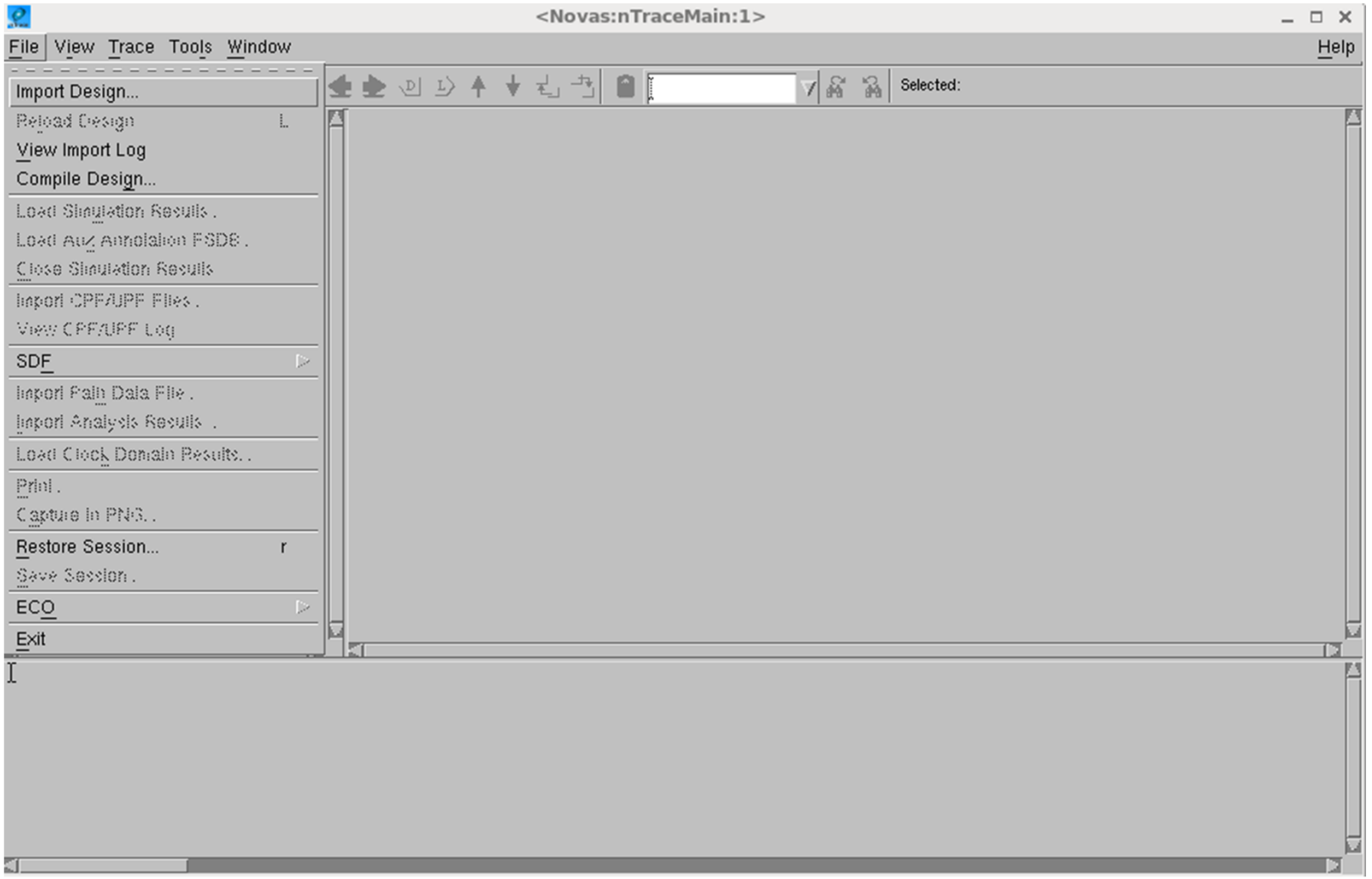
  將三個.v一起進行模擬。



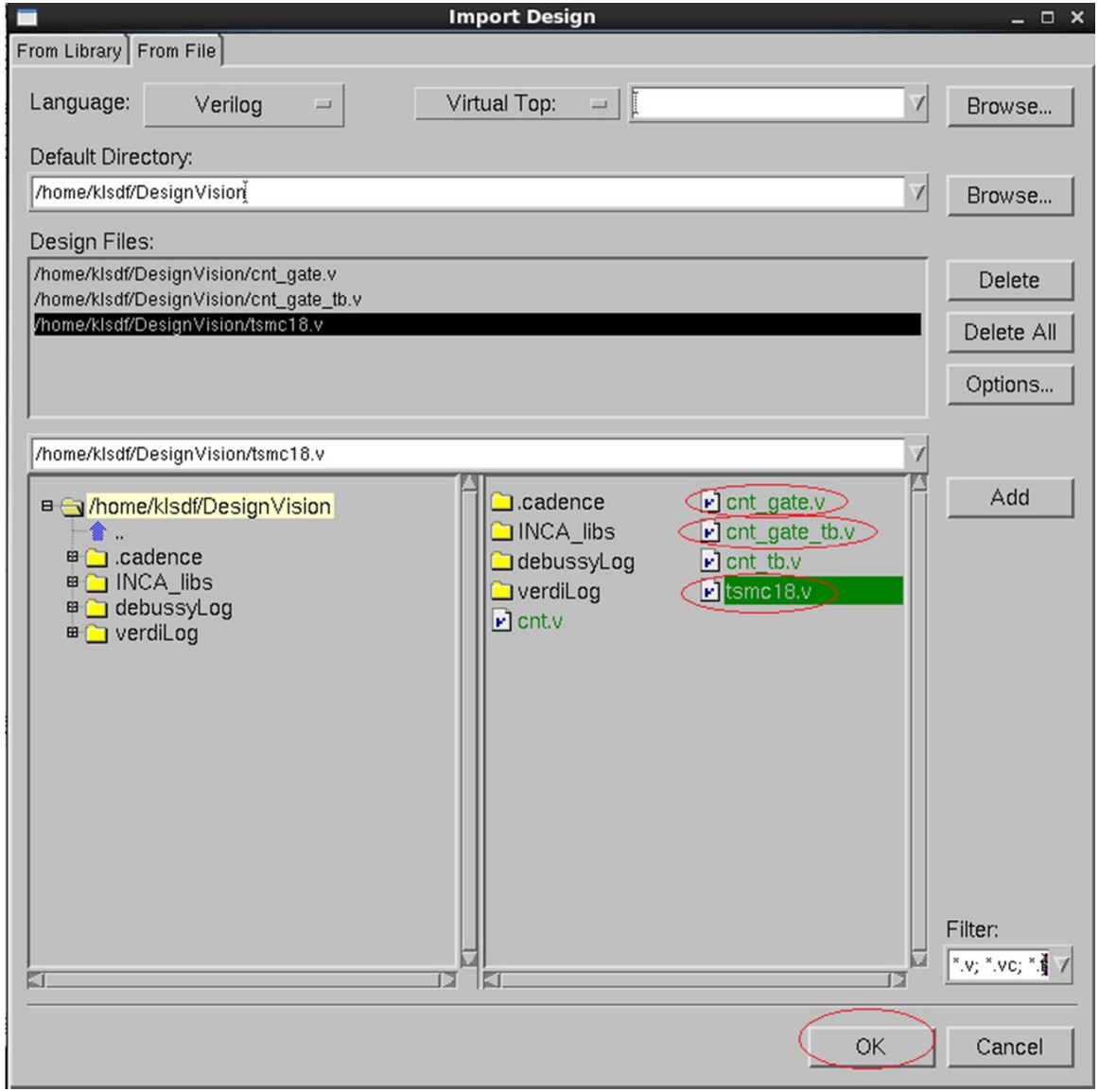
Gate-Level 模擬



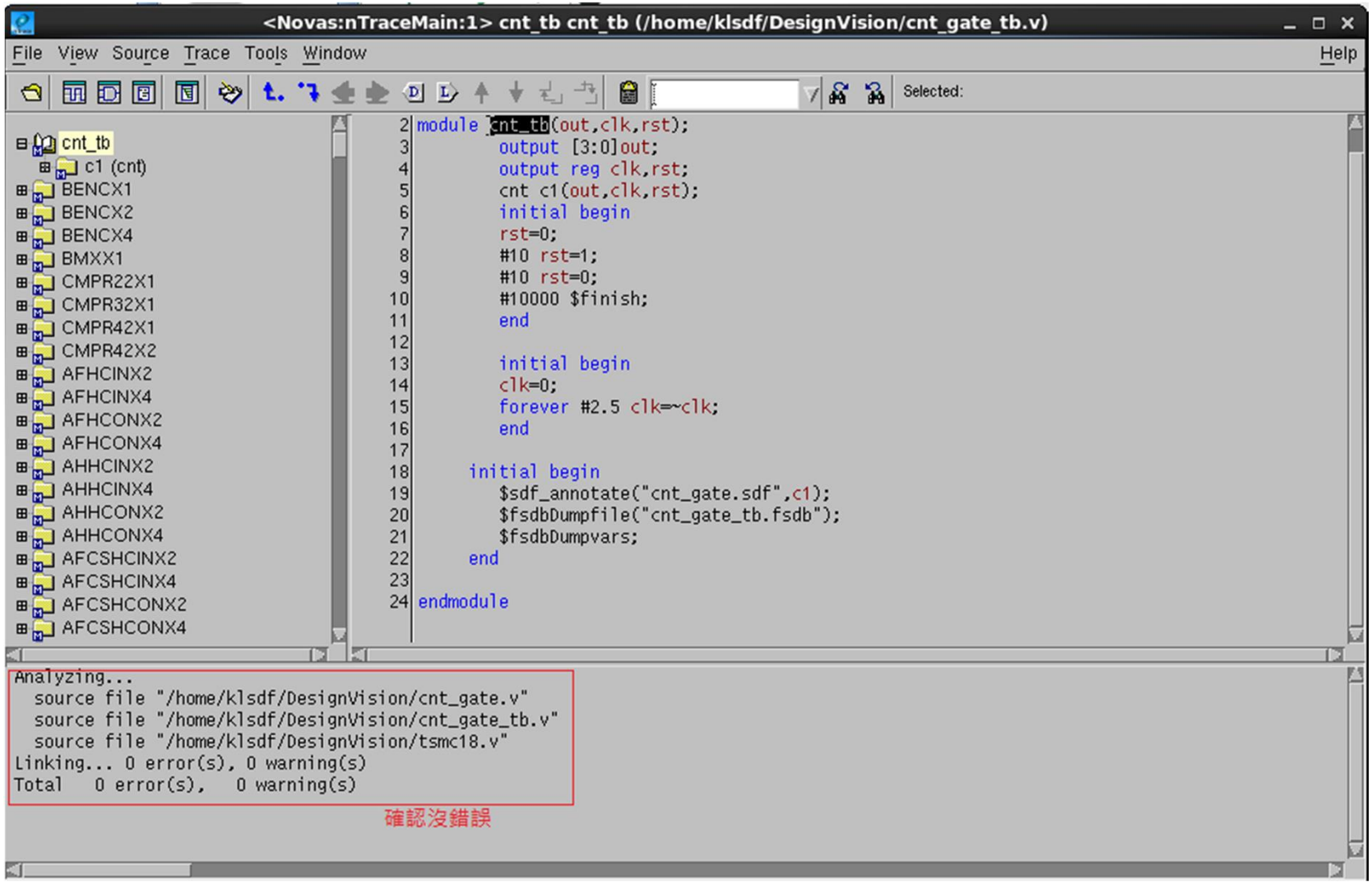
Debussy驗證


<Novas:nTraceMain:1>
File View Trace Tools Window
Help
Import Design...
Reload Design L
View Import Log
Compile Design...
Load Simulation Results...
Load Aux Annotation FSDB...
Close Simulation Results
Import CPF/UPF Files...
View CPF/UPF Log
SDF
Import Path Data File...
Import Analysis Results...
Load Clock Domain Results...
Print...
Capture In PNG...
Restore Session... r
Save Session...
ECO
Exit
Selected:

Debussy驗證

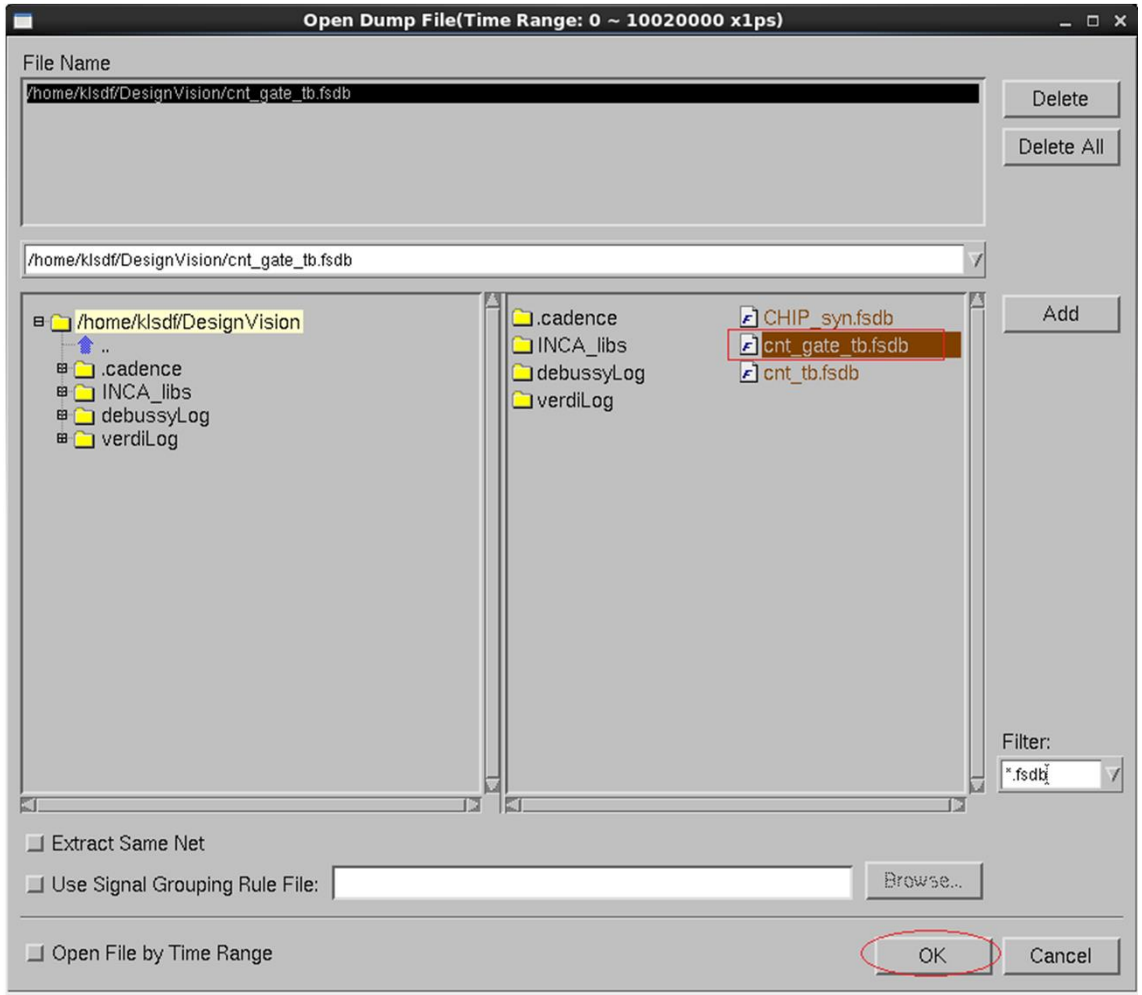

Import Design
From Library
From File
Language:
Verilog
Virtual Top:
Browse...
Default Directory:
/home/klsdf/DesignVision
Browse...
Design Files:
/home/klsdf/DesignVision/cnt_gate.v
/home/klsdf/DesignVision/cnt_gate_tb.v
/home/klsdf/DesignVision/tsmc18.v
Delete
Delete All
Options...
/home/klsdf/DesignVision/tsmc18.v
Add
/home/klsdf/DesignVision
..
.cadence
INCA_libs
debussyLog
verdiLog
.cadence
INCA_libs
debussyLog
verdiLog
cnt.v
cnt_gate.v
cnt_gate_tb.v
cnt_tb.v
tsmc18.v
Filter:
*.v; *.vc; *.
OK
Cancel

Debussy驗證

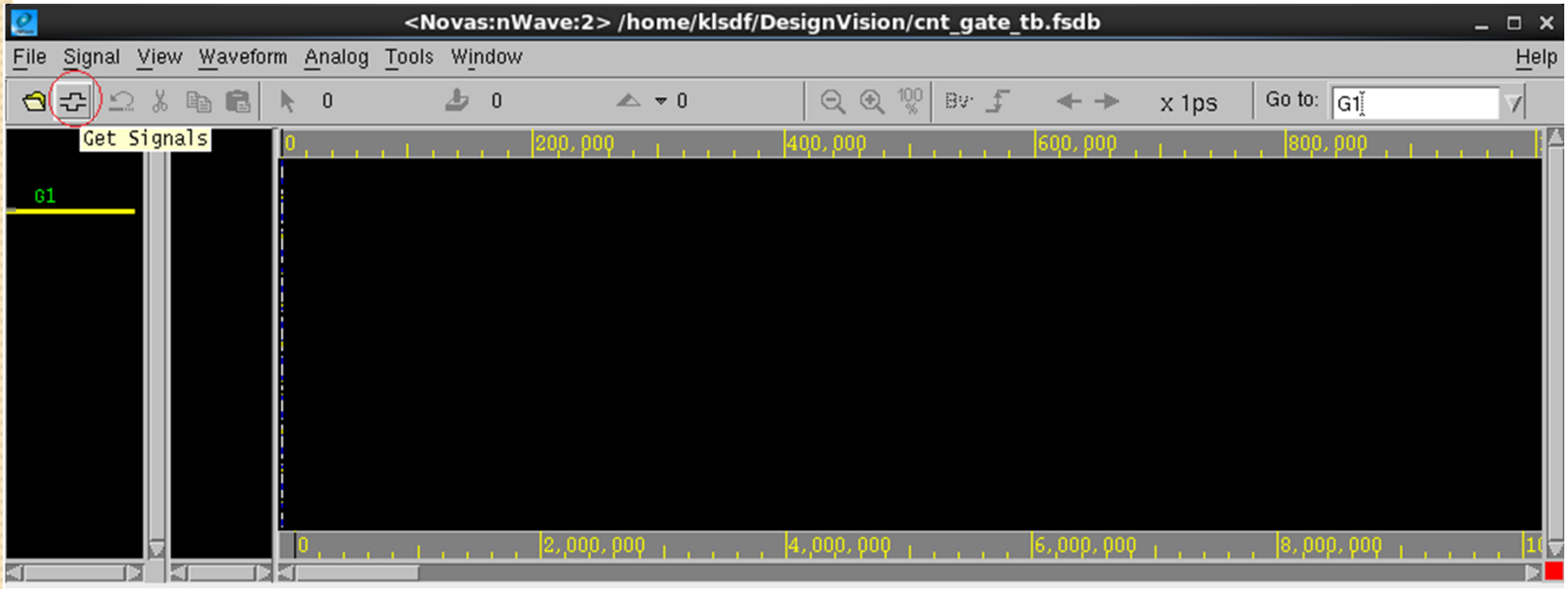

<Novas:nTraceMain:1> cnt_tb cnt_tb (/home/klsdf/DesignVision/cnt_gate_tb.v)
File View Source Trace Tools Window Help
Selected:
cnt_tb
c1 (cnt)
BENCX1
BENCX2
BENCX4
BMXX1
CMPR22X1
CMPR32X1
CMPR42X1
CMPR42X2
AFHCINX2
AFHCINX4
AFHCONX2
AFHCONX4
AHHCINX2
AHHCINX4
AHHCONX2
AHHCONX4
AFCSHCINX2
AFCSHCINX4
AFCSHCONX2
AFCSHCONX4
2 module cnt_tb(out,clk,rst);
3 output [3:0]out;
4 output reg clk,rst;
5 cnt c1(out,clk,rst);
6 initial begin
7 rst=0;
8 #10 rst=1;
9 #10 rst=0;
10 #10000 $finish;
11 end
12
13 initial begin
14 clk=0;
15 forever #2.5 clk=~clk;
16 end
17
18 initial begin
19 $sdf_annotate("cnt_gate.sdf",c1);
20 $fsdbDumpfile("cnt_gate_tb.fsdb");
21 $fsdbDumpvars;
22 end
23
24 endmodule
Analyzing...
source file "/home/klsdf/DesignVision/cnt_gate.v"
source file "/home/klsdf/DesignVision/cnt_gate_tb.v"
source file "/home/klsdf/DesignVision/tsmc18.v"
Linking... 0 error(s), 0 warning(s)
Total 0 error(s), 0 warning(s)
確認沒錯誤

Debussy驗證

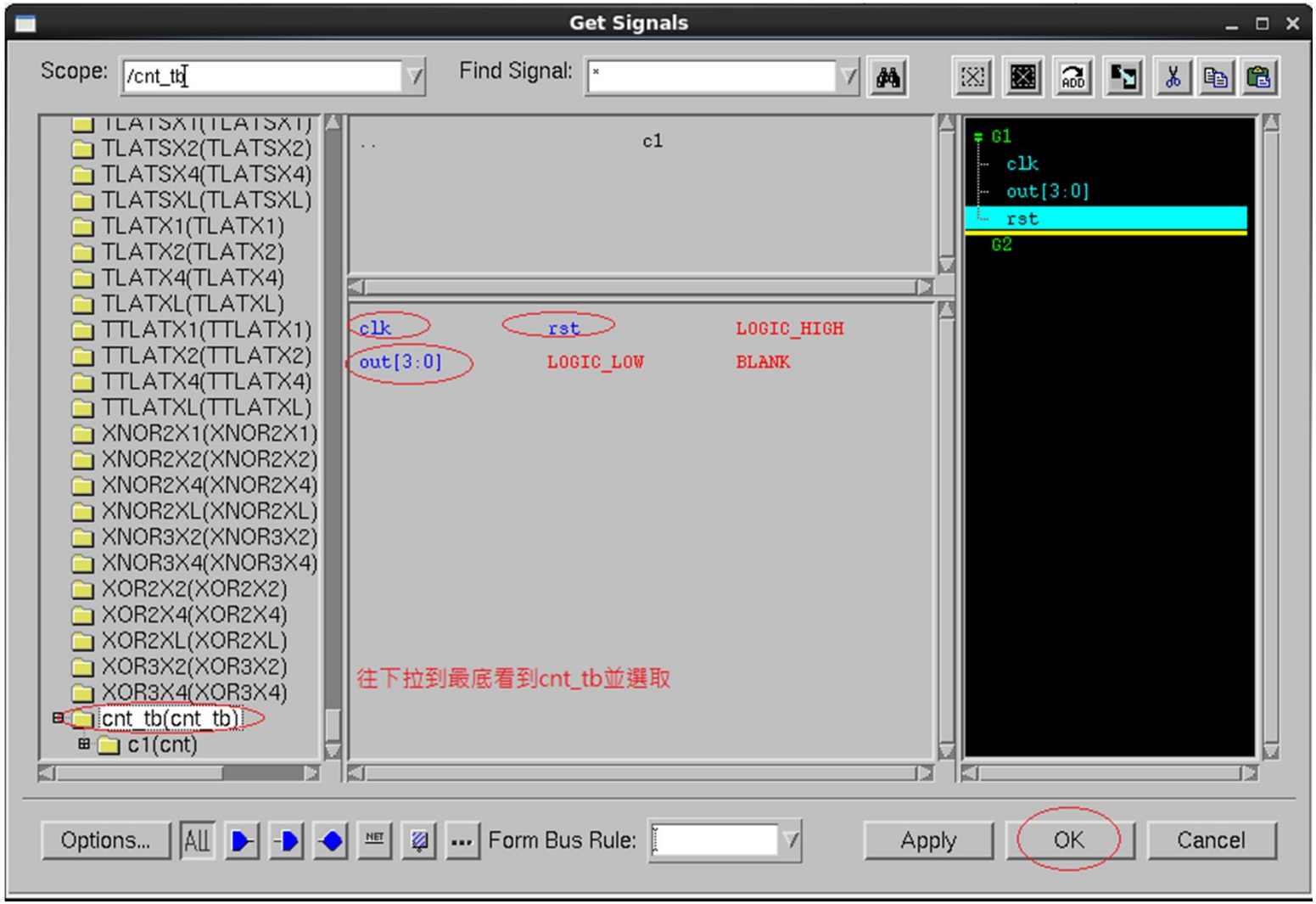
- 波形驗證(步驟請照Chapter1教的)



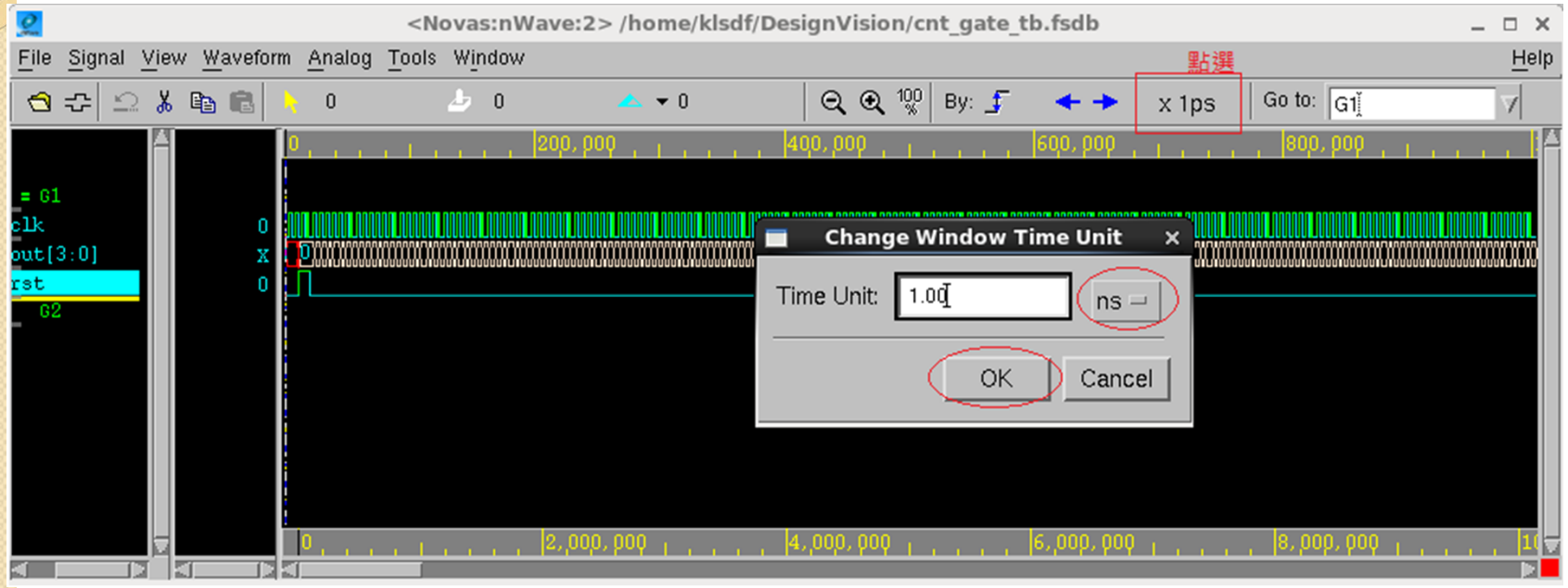
Debussy驗證


<Novas:nWave:2> /home/klsdf/DesignVision/cnt_gate_tb.fsdb
File Signal View Waveform Analog Tools Window
Help
Get Signals
Go to:
G1
200,000
400,000
600,000
800,000
2,000,000
4,000,000
6,000,000
8,000,000

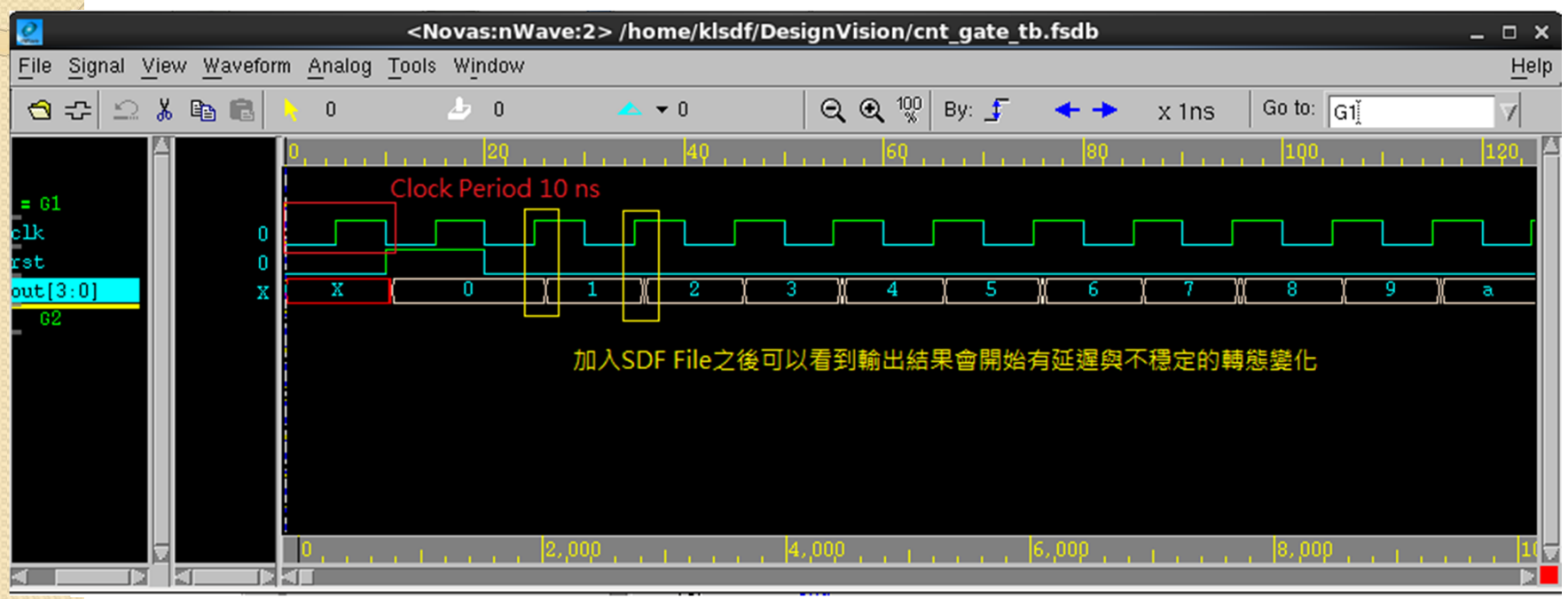
Debussy驗證


Get Signals
Scope: /cnt_tb
Find Signal:
TLATSX2(TLATSX2)
TLATSX4(TLATSX4)
TLATSXL(TLATSXL)
TLATX1(TLATX1)
TLATX2(TLATX2)
TLATX4(TLATX4)
TLATXL(TLATXL)
TTLATX1(TTLATX1)
TTLATX2(TTLATX2)
TTLATX4(TTLATX4)
TTLATXL(TTLATXL)
XNOR2X1(XNOR2X1)
XNOR2X2(XNOR2X2)
XNOR2X4(XNOR2X4)
XNOR2XL(XNOR2XL)
XNOR3X2(XNOR3X2)
XNOR3X4(XNOR3X4)
XOR2X2(XOR2X2)
XOR2X4(XOR2X4)
XOR2XL(XOR2XL)
XOR3X2(XOR3X2)
XOR3X4(XOR3X4)
cnt_tb(cnt_tb)
c1(cnt)
c1
clk
rst
LOGIC_HIGH
out[3:0]
LOGIC_LOW
BLANK
往下拉到最底看到cnt_tb並選取
G1
clk
out[3:0]
rst
G2
Options...
Form Bus Rule:
Apply
OK
Cancel

Debussy驗證


<Novas:nWave:2> /home/klsdf/DesignVision/cnt_gate_tb.fsdb
File Signal View Waveform Analog Tools Window
Help
點選
x 1ps
Go to: G1
= G1
clk
out[3:0]
rst
G2
Change Window Time Unit
Time Unit: 1.00
ns
OK
Cancel
200,000
400,000
600,000
800,000
2,000,000
4,000,000
6,000,000
8,000,000

Debussy驗證


<Novas:nWave:2> /home/klsdf/DesignVision/cnt_gate_tb.fsdb
File Signal View Waveform Analog Tools Window
Help
Go to: G1
x 1ns
= G1
clk
rst
out[3:0]
G2
Clock Period 10 ns
加入SDF File之後可以看到輸出結果會開始有延遲與不穩定的轉態變化