



ASIC教材

Chapter8 Innovus Routing

高雄科技大學電子工程系
B510實驗室

2021/2/2再編



目錄

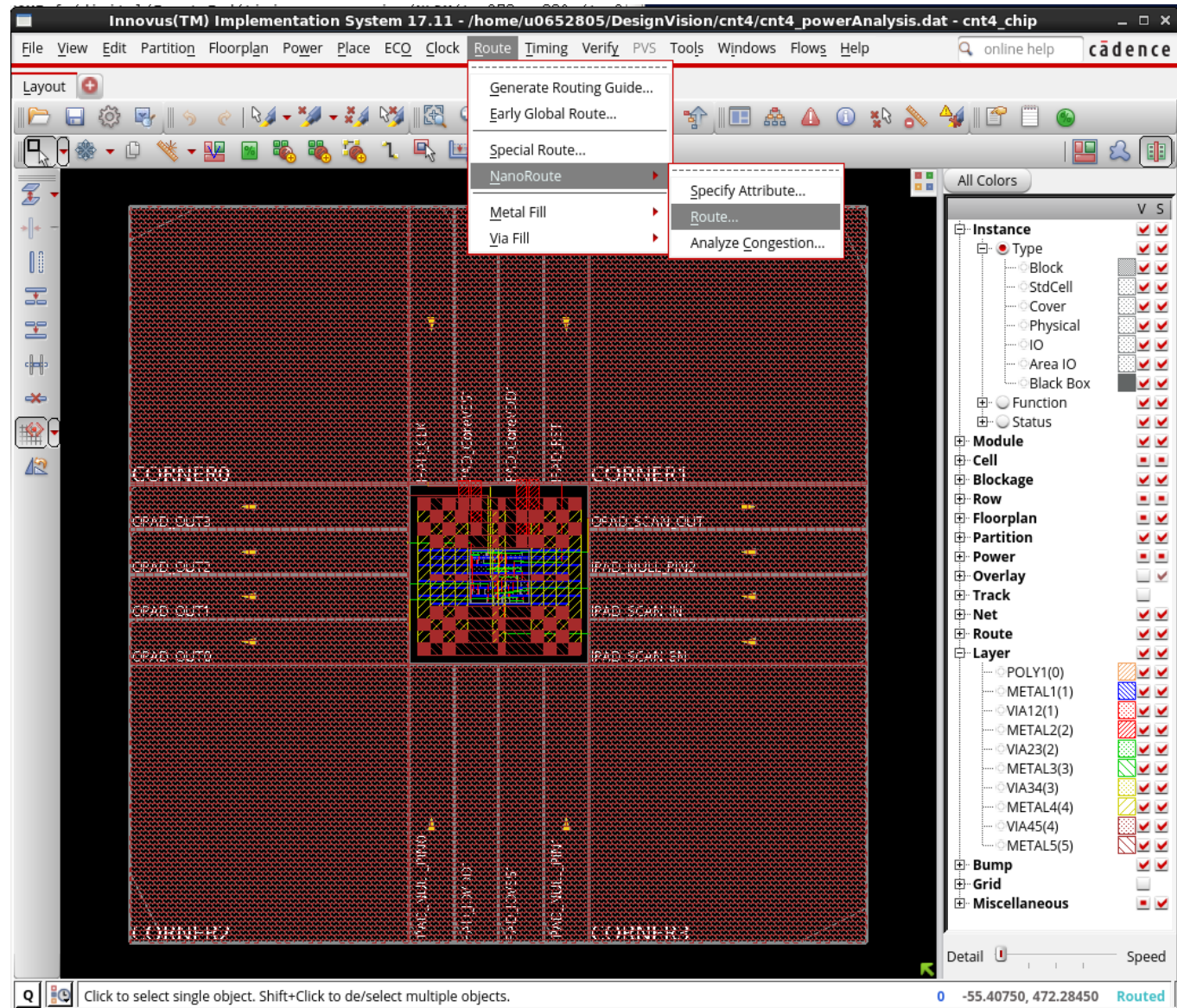
Routing

Add Filler

Add dummy Metal

PrimeTime PowerAnalysis

Routing

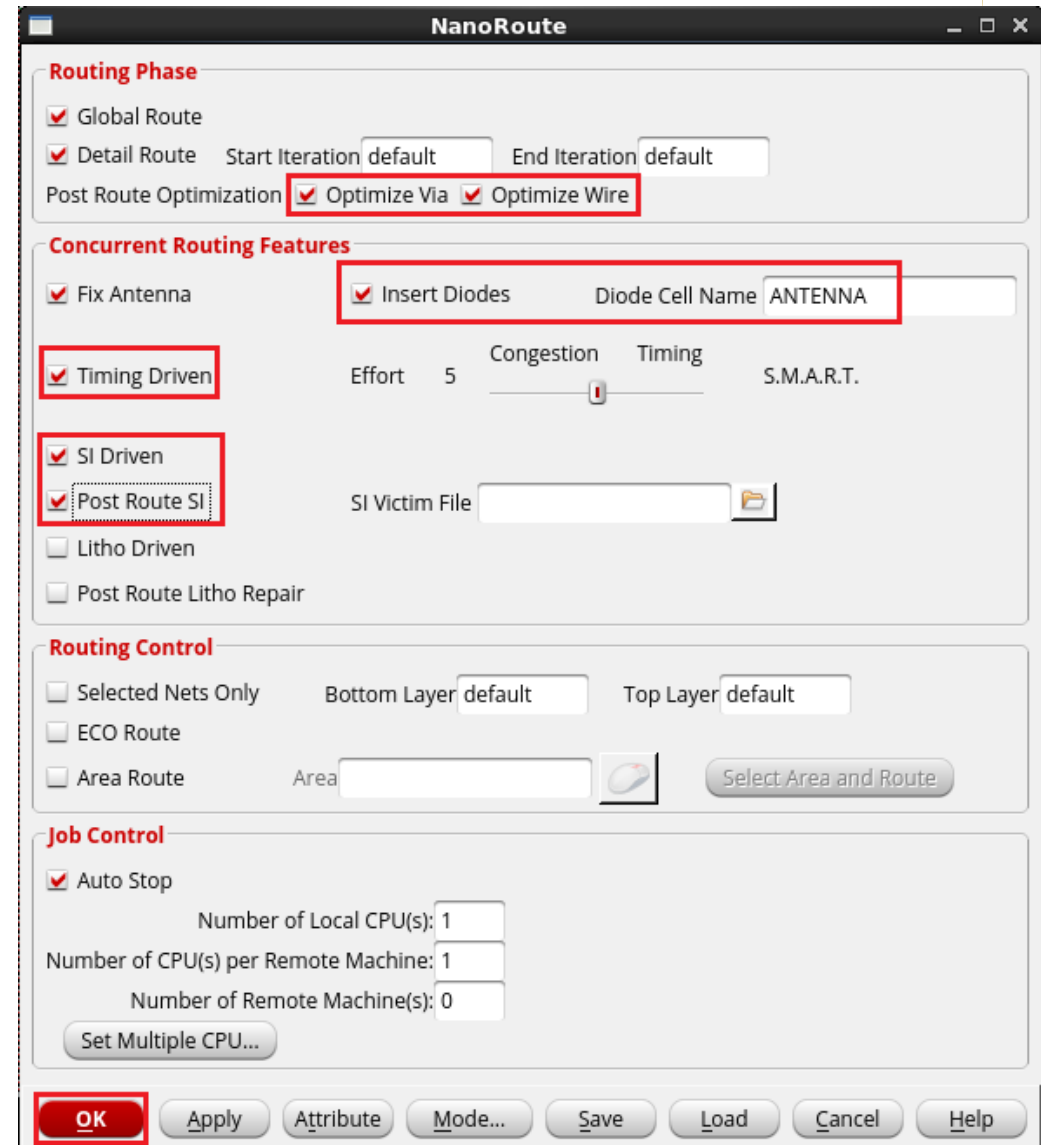


Routing

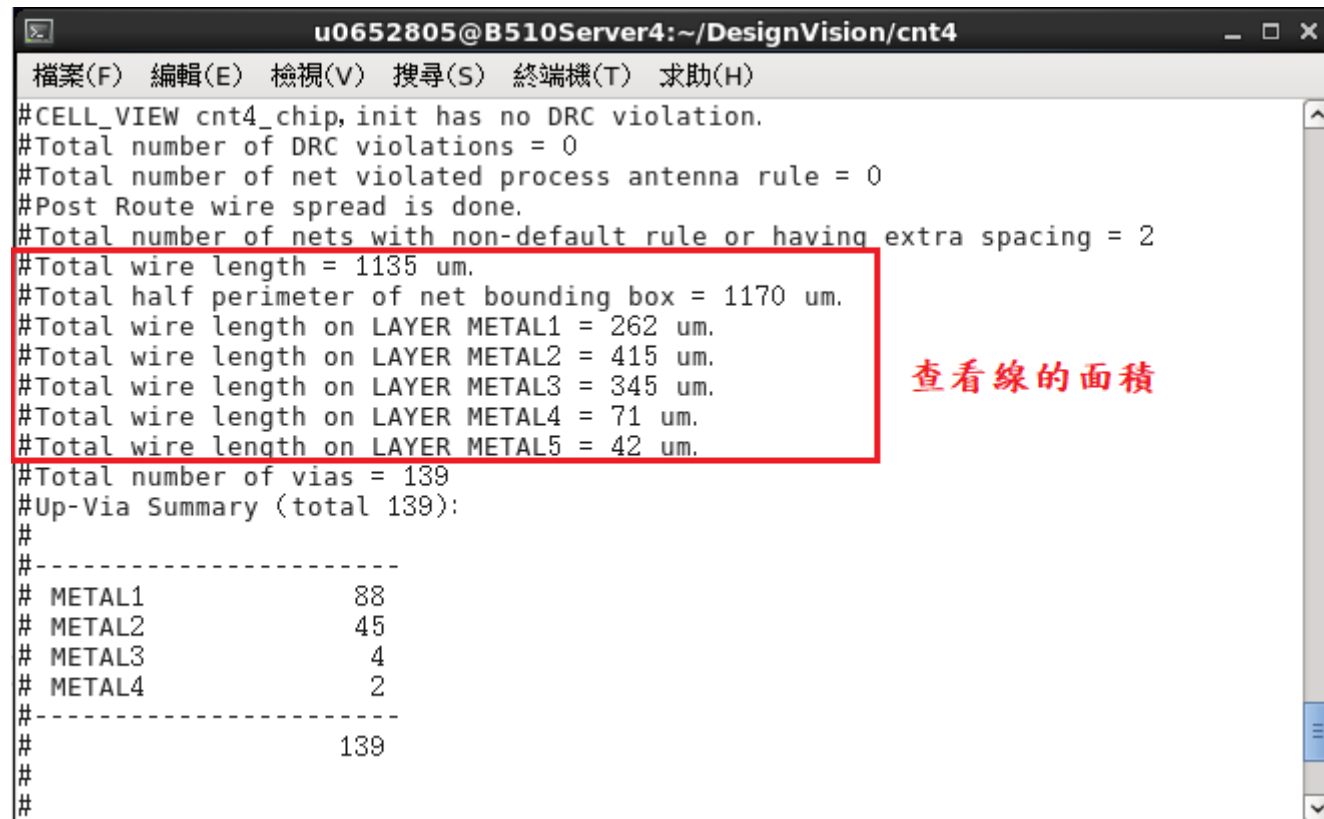
Timing Driven為
以Timing考量之Routing

Diodes為解決天線效應
ANTENNA為使用的
Diodes

SI Driven為在Routing
時同時考慮Cross talk



Routing



The screenshot shows a terminal window titled "u0652805@B510Server4:~/DesignVision/cnt4". The window contains a menu bar with options: 檔案(F), 編輯(E), 檢視(V), 搜尋(S), 終端機(T), 求助(H). The main text area displays the following output:

```
#CELL_VIEW cnt4_chip, init has no DRC violation.
#Total number of DRC violations = 0
#Total number of net violated process antenna rule = 0
#Post Route wire spread is done.
#Total number of nets with non-default rule or having extra spacing = 2
#Total wire length = 1135 um.
#Total half perimeter of net bounding box = 1170 um.
#Total wire length on LAYER METAL1 = 262 um.
#Total wire length on LAYER METAL2 = 415 um.
#Total wire length on LAYER METAL3 = 345 um.
#Total wire length on LAYER METAL4 = 71 um.
#Total wire length on LAYER METAL5 = 42 um.
#Total number of vias = 139
#Up-Via Summary (total 139):
#
#-----
# METAL1          88
# METAL2          45
# METAL3           4
# METAL4           2
#-----
#                  139
#
#
```

A red rectangular box highlights the following lines of text:

```
#Total wire length = 1135 um.
#Total half perimeter of net bounding box = 1170 um.
#Total wire length on LAYER METAL1 = 262 um.
#Total wire length on LAYER METAL2 = 415 um.
#Total wire length on LAYER METAL3 = 345 um.
#Total wire length on LAYER METAL4 = 71 um.
#Total wire length on LAYER METAL5 = 42 um.
```

To the right of the highlighted text, the Chinese text "查看線的面積" (View wire area) is written in red.

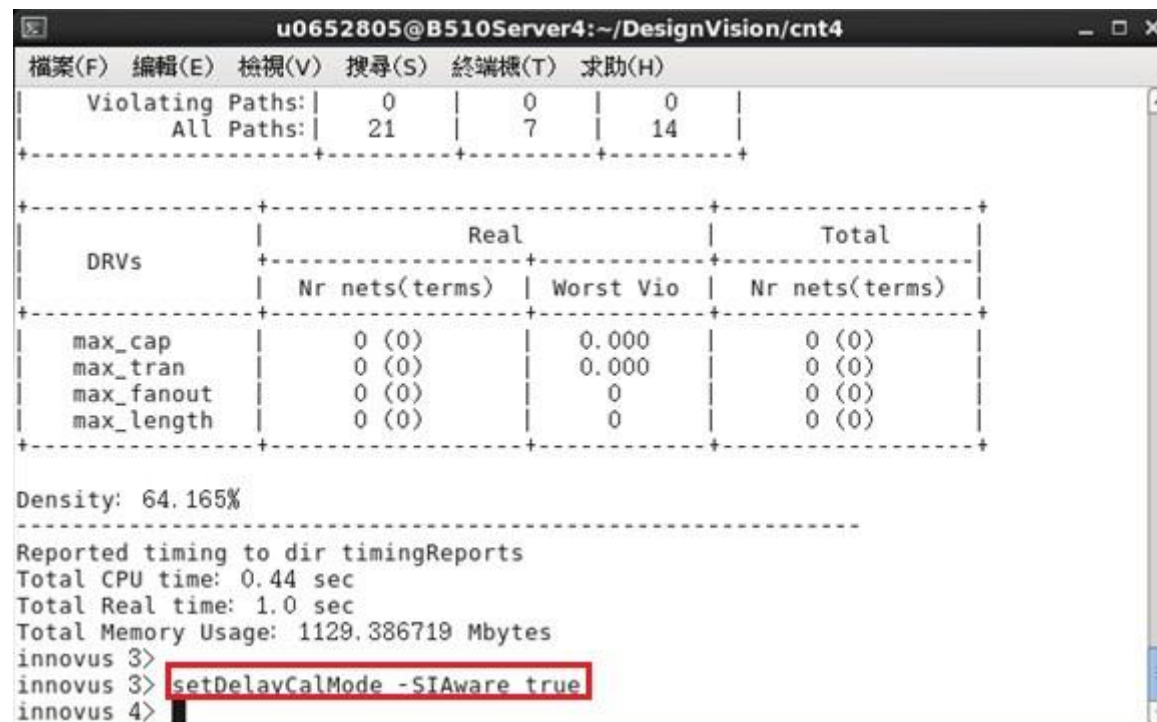
Routing

Report Timing: 先將 Timing Mode 改成 onChipVariation。

setAnalysisMode -analysisType onChipVariation -cpr both

```
-clockPropagation -cpr  
innovus 1> setAnalysisMode -analysisType onChipVariation -cpr both
```

開啟模式: setDelayCalMode -SIAware true



The screenshot shows a terminal window titled "u0652805@B510Server4:~/DesignVision/cnt4". The window displays routing results and commands. The routing results include a table of violating paths and a table of DRV parameters. The commands section shows the execution of "setDelayCalMode -SIAware true".

Violating Paths:	0	0	0
All Paths:	21	7	14

DRVs	Real		Total
	Nr nets(terms)	Worst Vio	Nr nets(terms)
max_cap	0 (0)	0.000	0 (0)
max_tran	0 (0)	0.000	0 (0)
max_fanout	0 (0)	0	0 (0)
max_length	0 (0)	0	0 (0)

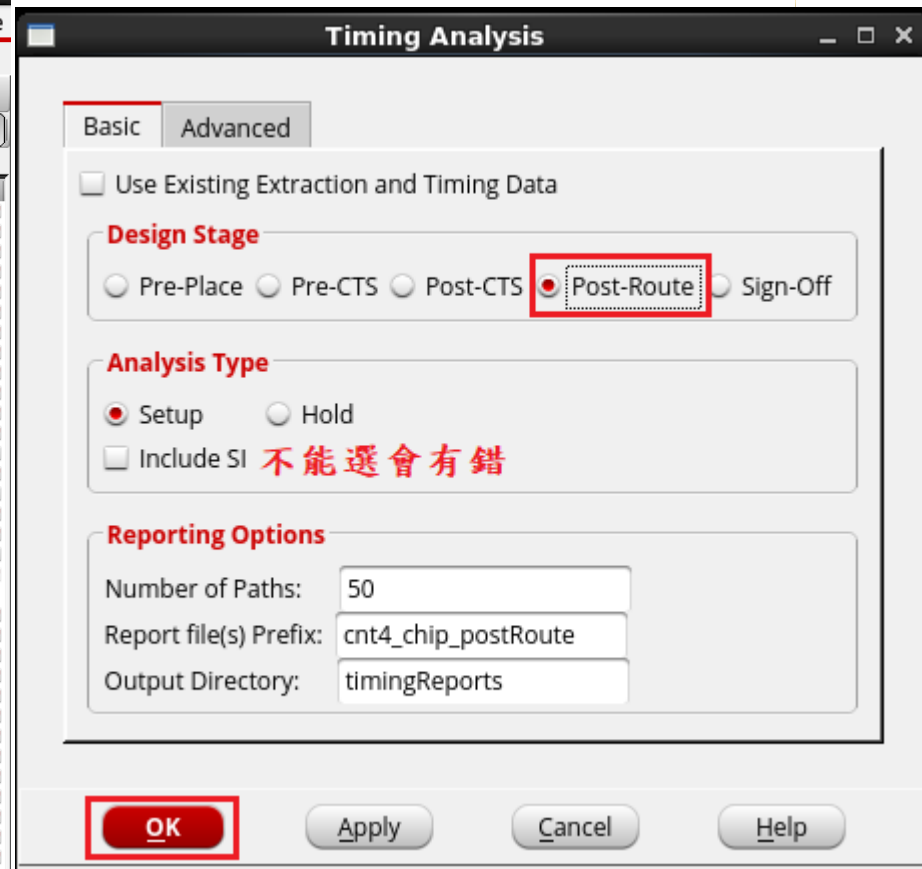
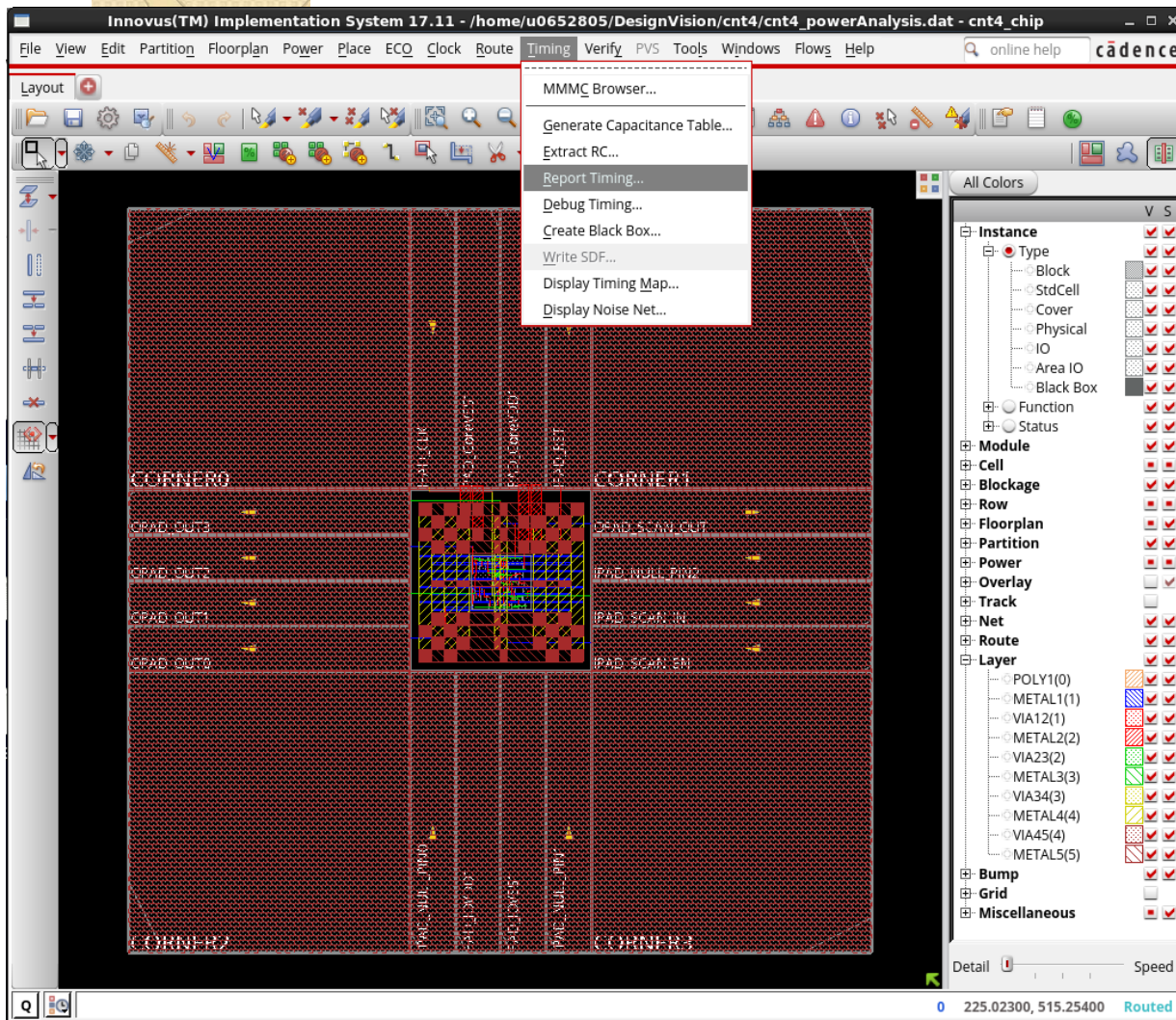
Density: 64.165%

Reported timing to dir timingReports
Total CPU time: 0.44 sec
Total Real time: 1.0 sec
Total Memory Usage: 1129.386719 Mbytes

```
innovus 3>  
innovus 3> setDelayCalMode -SIAware true  
innovus 4>
```

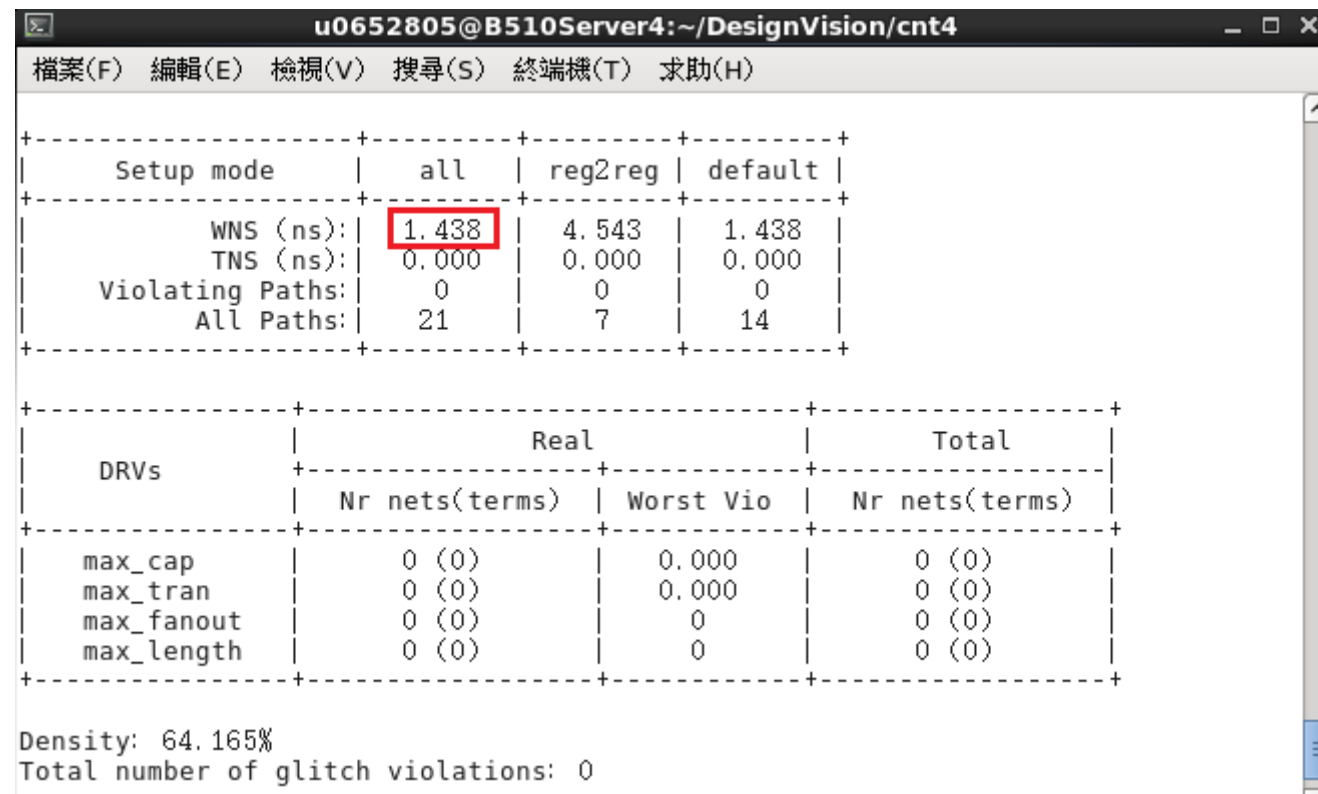
Routing

Report Timing



Routing

如果WNS為負需做Optimize



The screenshot shows a terminal window titled "u0652805@B510Server4:~/DesignVision/cnt4". The menu bar includes "檔案(F)", "編輯(E)", "檢視(V)", "搜尋(S)", "終端機(T)", and "求助(H)". The main content displays two tables of routing statistics. The first table compares "all", "reg2reg", and "default" setup modes. The "all" mode shows a WNS of 1.438 ns, which is highlighted with a red box. The second table shows DRV statistics for "Real" and "Total" modes, including metrics like max_cap, max_tran, max_fanout, and max_length. At the bottom, it reports a density of 64.165% and zero glitch violations.

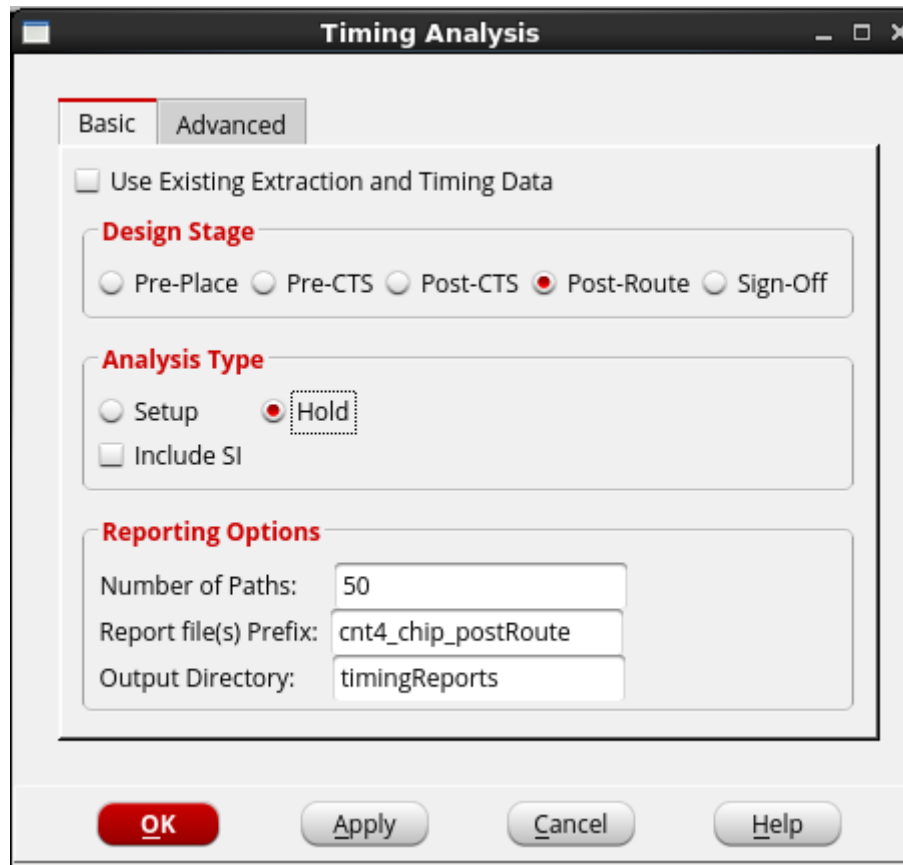
Setup mode	all	reg2reg	default
WNS (ns):	1.438	4.543	1.438
TNS (ns):	0.000	0.000	0.000
Violating Paths:	0	0	0
All Paths:	21	7	14

DRVs	Real		Total
	Nr nets(terms)	Worst Vio	Nr nets(terms)
max_cap	0 (0)	0.000	0 (0)
max_tran	0 (0)	0.000	0 (0)
max_fanout	0 (0)	0	0 (0)
max_length	0 (0)	0	0 (0)

Density: 64.165%
Total number of glitch violations: 0

Routing

觀察Hold Time



The image shows a 'Timing Analysis' dialog box with a dark title bar and standard window controls. It has two tabs: 'Basic' (selected) and 'Advanced'. The 'Basic' tab contains three sections: 'Use Existing Extraction and Timing Data' (unchecked), 'Design Stage' (radio buttons for Pre-Place, Pre-CTS, Post-CTS, Post-Route (selected), and Sign-Off), 'Analysis Type' (radio buttons for Setup and Hold (selected), and an unchecked 'Include SI' checkbox), and 'Reporting Options' (text fields for 'Number of Paths' (50), 'Report file(s) Prefix' (cnt4_chip_postRoute), and 'Output Directory' (timingReports)). At the bottom are four buttons: 'OK' (red), 'Apply', 'Cancel', and 'Help'.

Timing Analysis

Basic Advanced

☐ Use Existing Extraction and Timing Data

Design Stage

☐ Pre-Place ☐ Pre-CTS ☐ Post-CTS ☒ Post-Route ☐ Sign-Off

Analysis Type

☐ Setup ☒ Hold

☐ Include SI

Reporting Options

Number of Paths: 50

Report file(s) Prefix: cnt4_chip_postRoute

Output Directory: timingReports

OK Apply Cancel Help

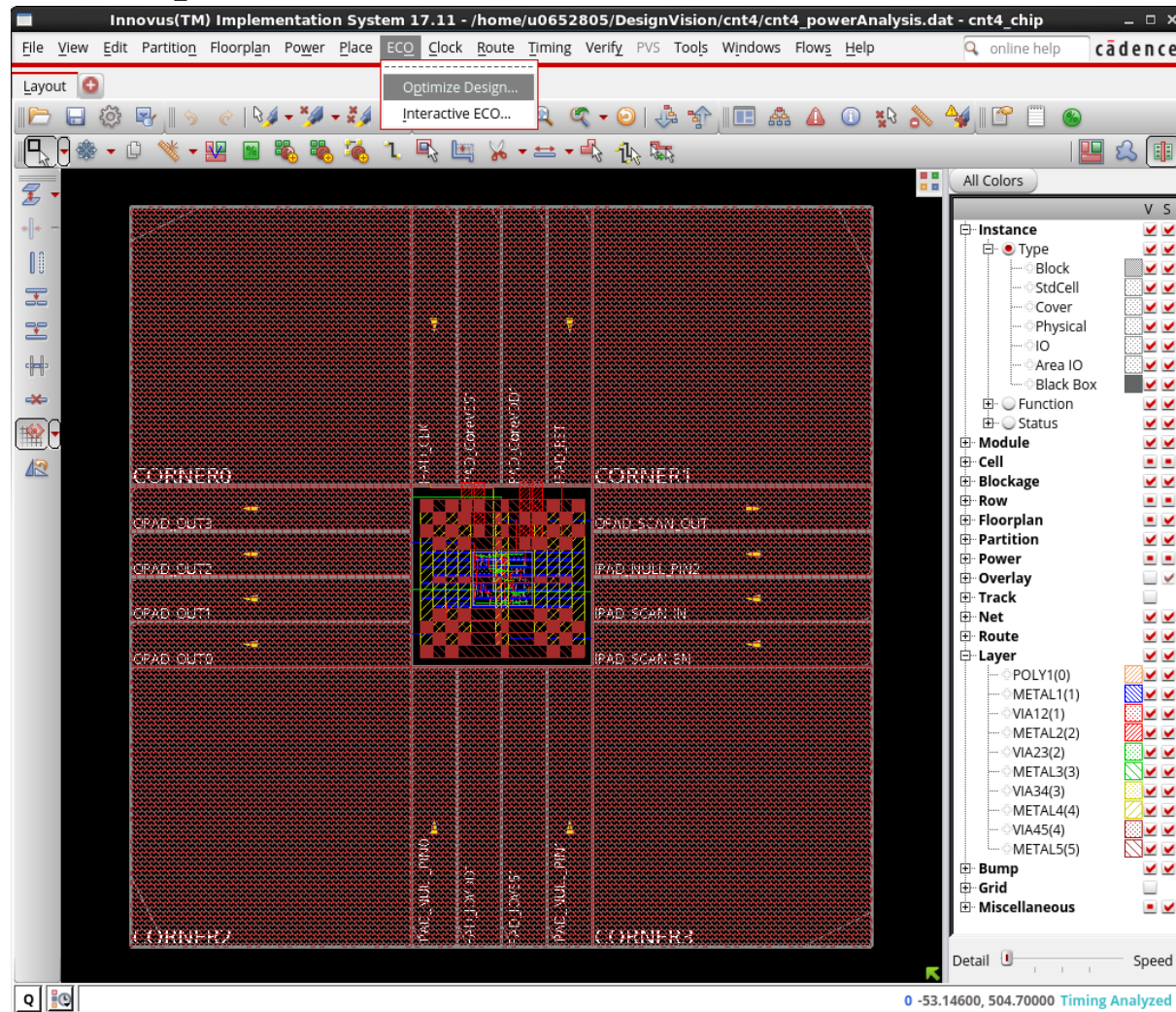
Routing

```
u0652805@B510Server4:~/DesignVision/cnt4
檔案(F) 編輯(E) 檢視(V) 搜尋(S) 終端機(T) 求助(H)
-----
timeDesign Summary
-----
Hold views included:
av_func_mode_min
+-----+-----+-----+
| Hold mode | all | reg2reg | default |
+-----+-----+-----+
| WNS (ns): | 1.075 | 1.075 | 1.161 |
| TNS (ns): | 0.000 | 0.000 | 0.000 |
| Violating Paths: | 0 | 0 | 0 |
| All Paths: | 21 | 7 | 14 |
+-----+-----+-----+
Density: 64.165%
-----
Reported timing to dir timingReports
Total CPU time: 0.81 sec
Total Real time: 1.0 sec
Total Memory Usage: 1099.035156 Mbytes
Reset AAE Options
innovus 4>
```

Routing

Post Route Optimization

如果Setup&Hold Time的WNS都為正可不作此步

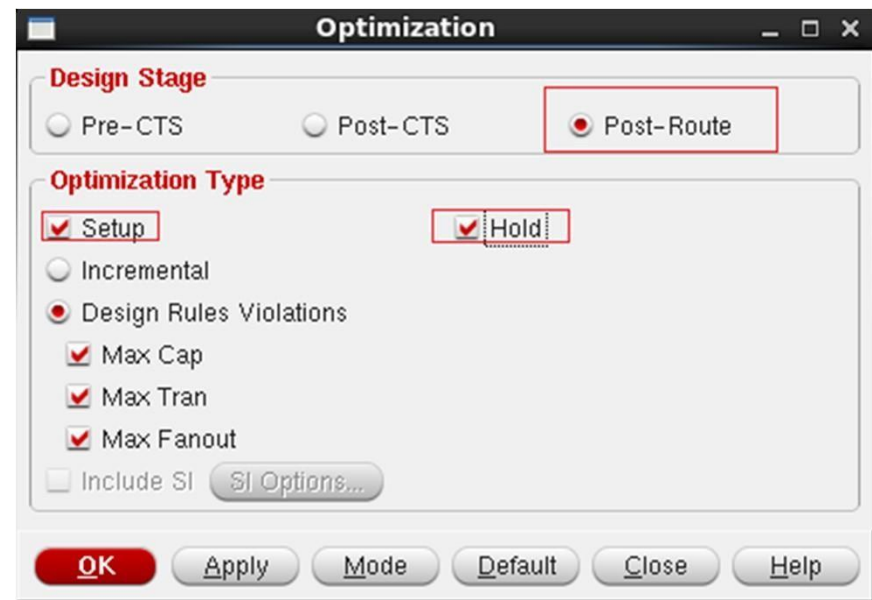
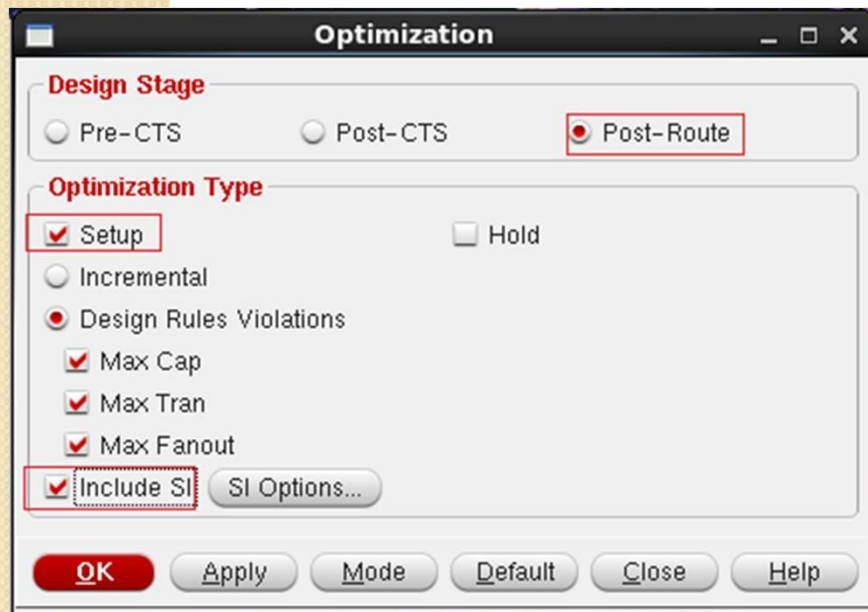


Routing

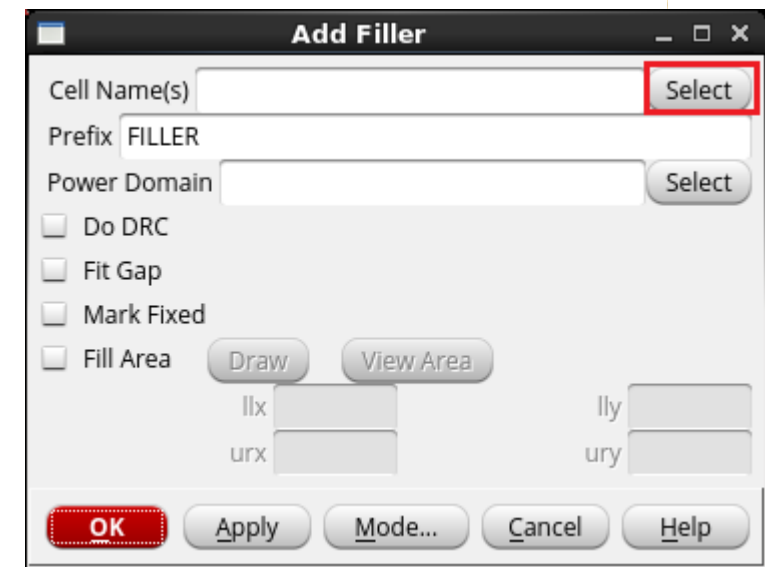
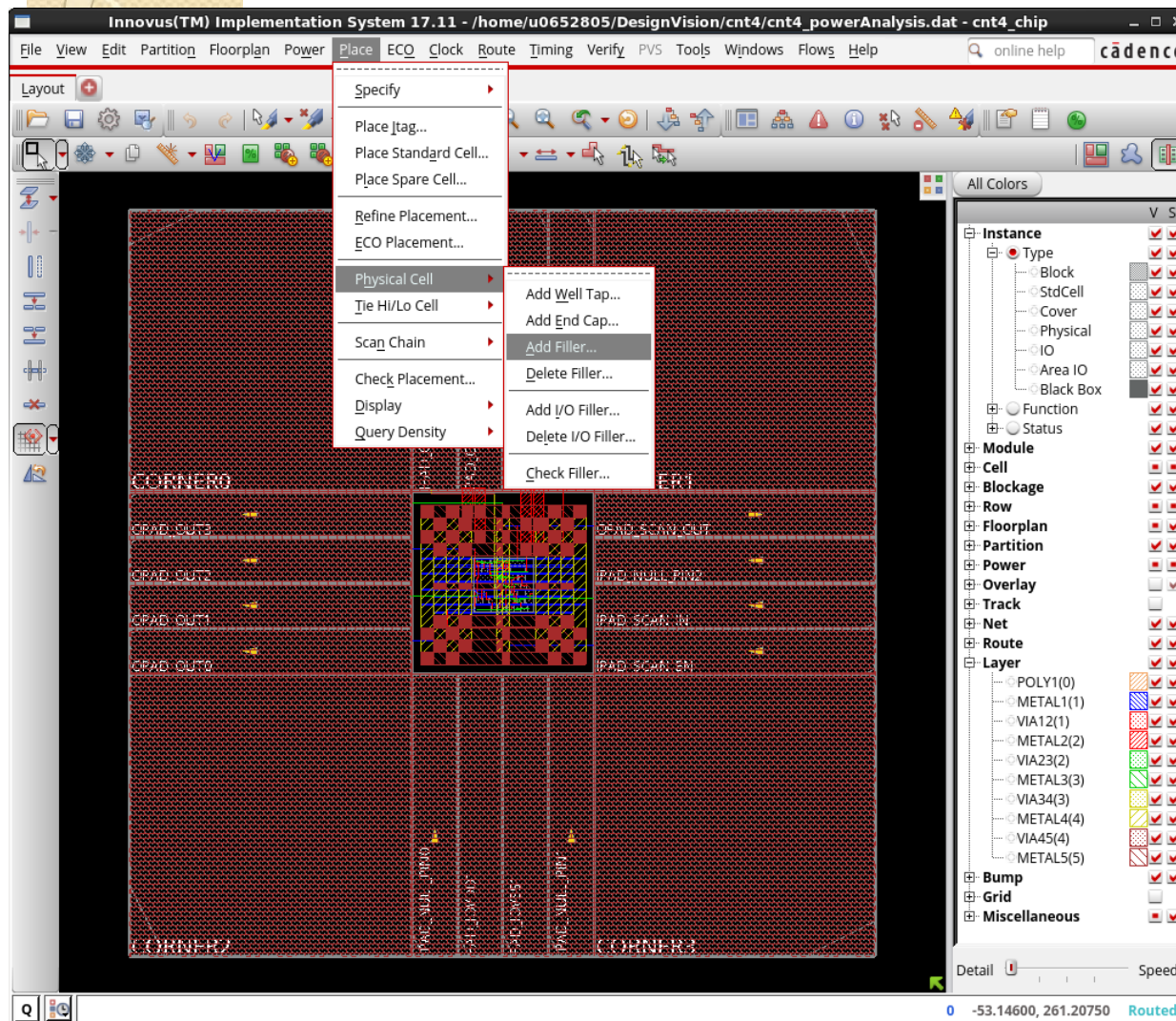
Post Route Optimization

如果Setup&Hold Time的WNS都為正可不做此步。

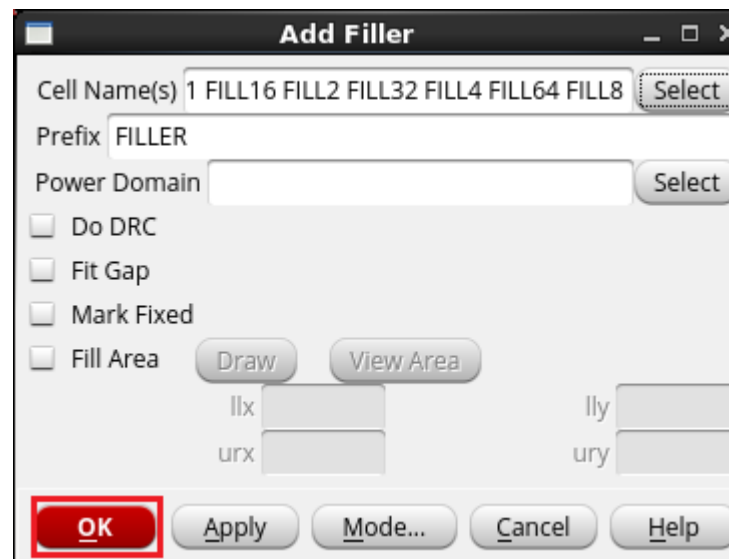
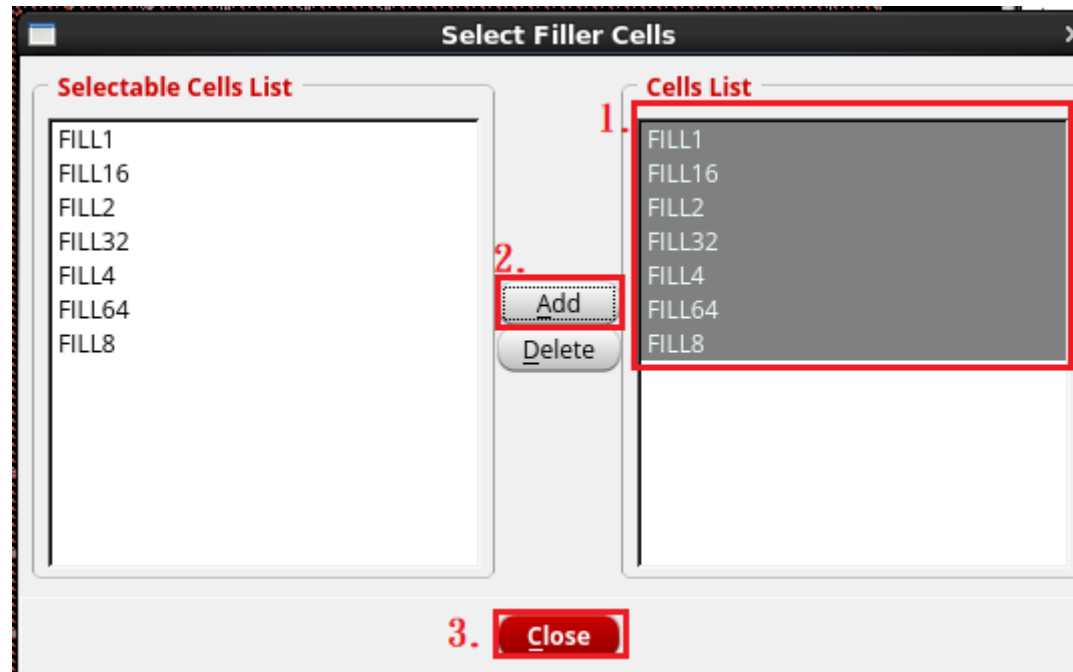
如只有Setup Time有問題照左圖，如果有Hold Time則右圖。



Add Filler

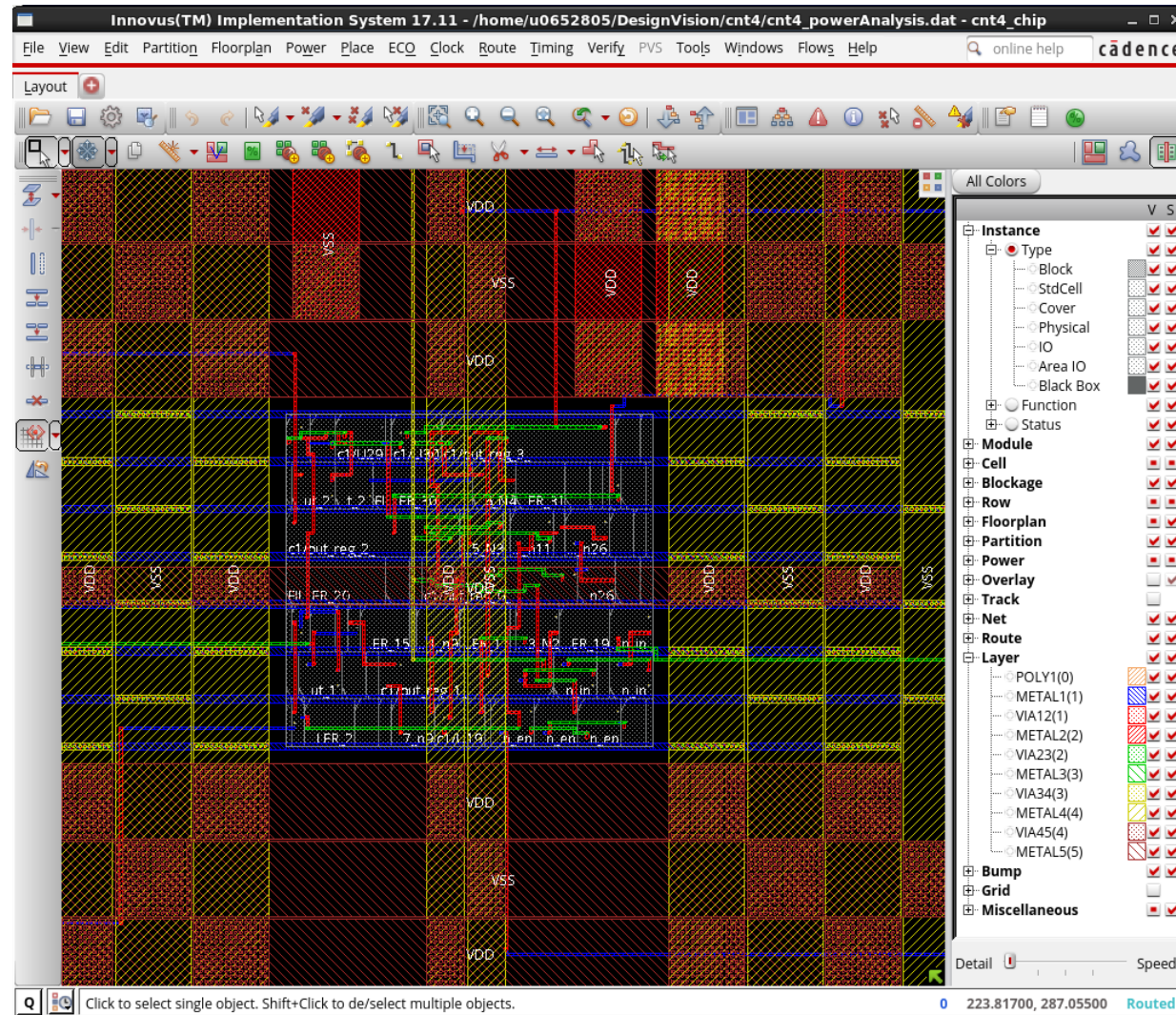


Add Filler



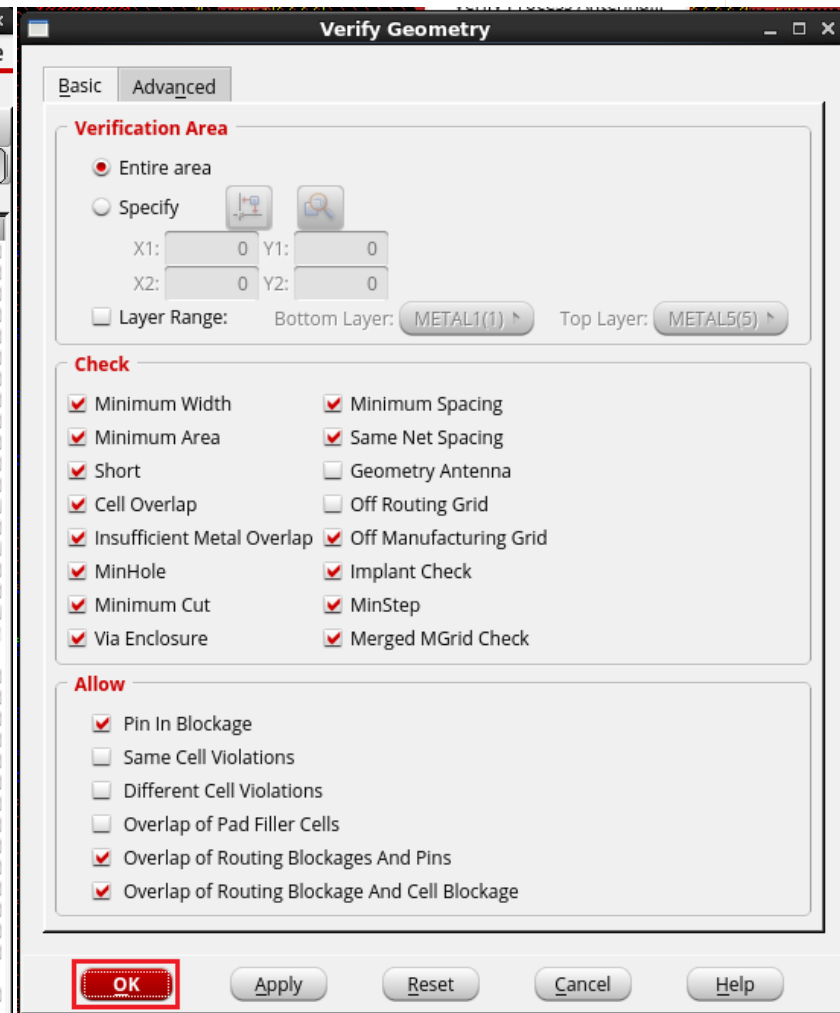
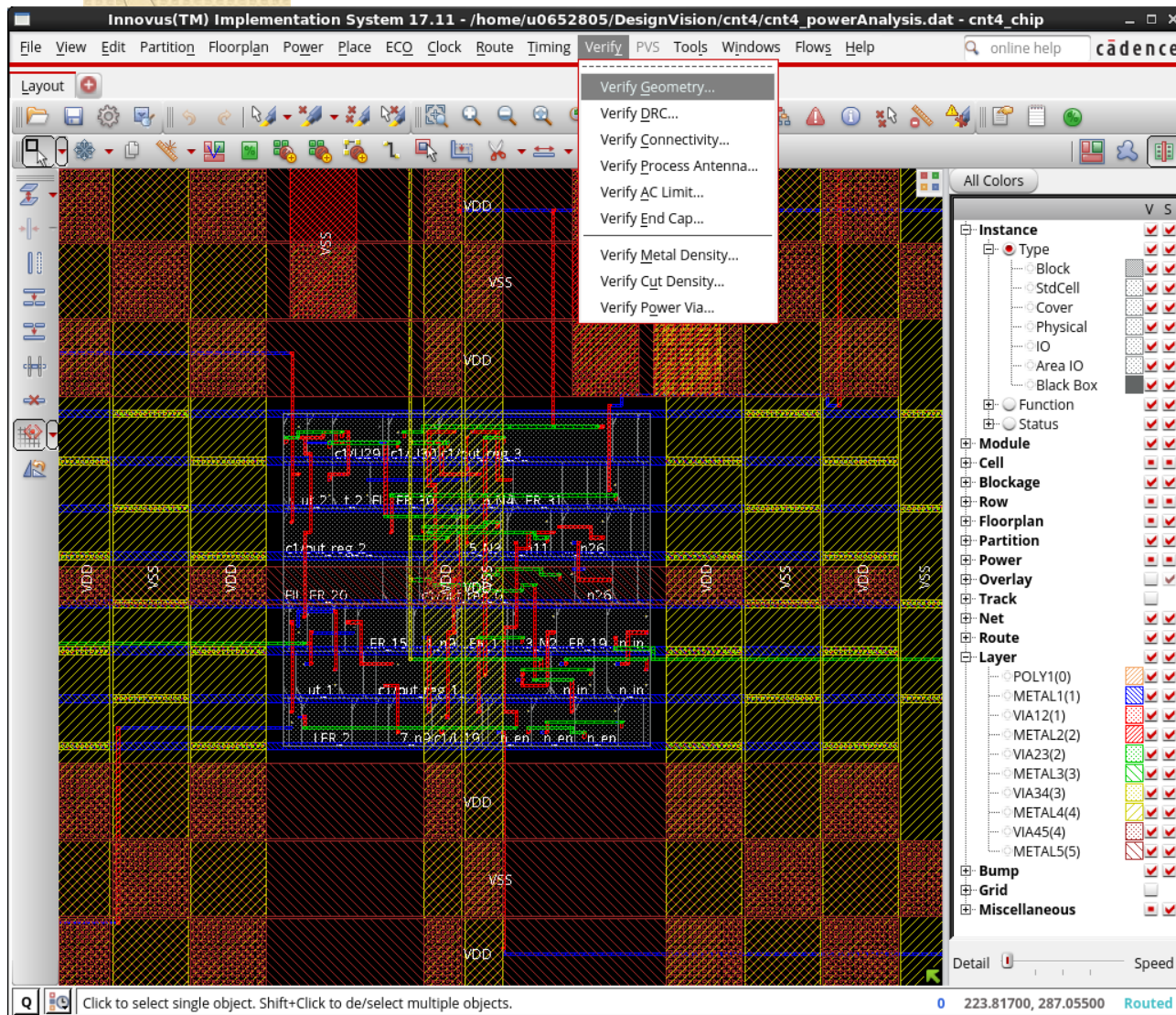
Add Filler

放大之後可以看到Core被Filler填滿



Add Filler

Verify



Add Filler

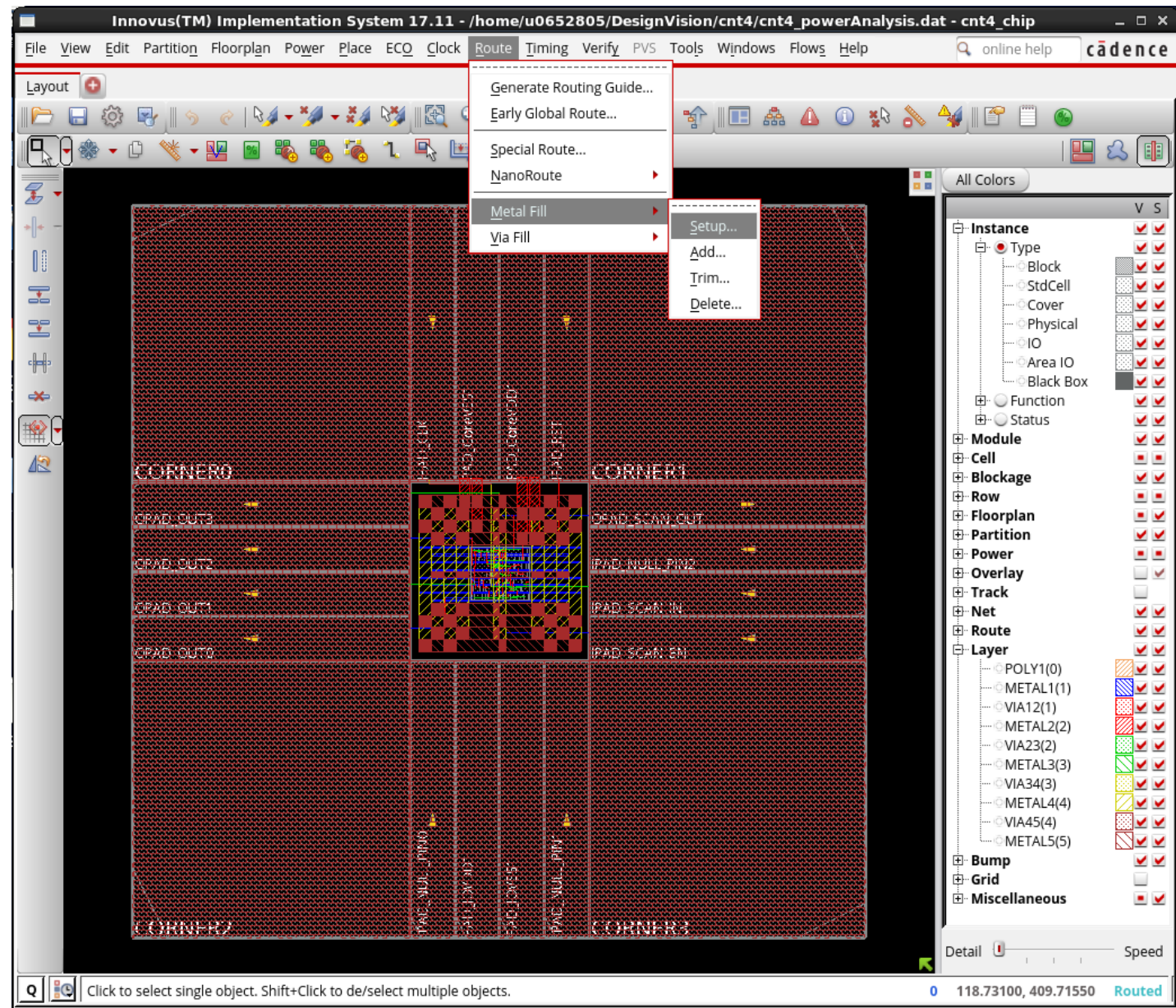
```
u0652805@B510Server4:~/DesignVision/cnt4
檔案(F) 編輯(E) 檢視(V) 搜尋(S) 終端機(T) 求助(H)
  VERIFY GEOMETRY ..... Creating Sub-Areas
                        ..... bin size: 7040
  VERIFY GEOMETRY ..... SubArea : 1 of 1
  VERIFY GEOMETRY ..... Cells           : 0 Viols.
  VERIFY GEOMETRY ..... SameNet          : 0 Viols.
  VERIFY GEOMETRY ..... Wiring           : 0 Viols.
  VERIFY GEOMETRY ..... Antenna          : 0 Viols.
  VERIFY GEOMETRY ..... Sub-Area : 1 complete 0 Viols. 0 Wrngs.
VG: elapsed time: 0.00
Begin Summary ...
  Cells       : 0
  SameNet     : 0
  Wiring      : 0
  Antenna     : 0
  Short       : 0
  Overlap     : 0
End Summary

  Verification Complete : 0 Viols. 0 Wrngs.

*****End: VERIFY GEOMETRY*****
*** verify geometry (CPU: 0:00:00.1 MEM: 55.8M)

innovus 4> setMetalFill -layer METAL1 -opcActiveSpacing 0.230 -maxDensity 50
```

Add dummy Metal



Add dummy Metal

Setup Metal Fill Options

Iteration Name:

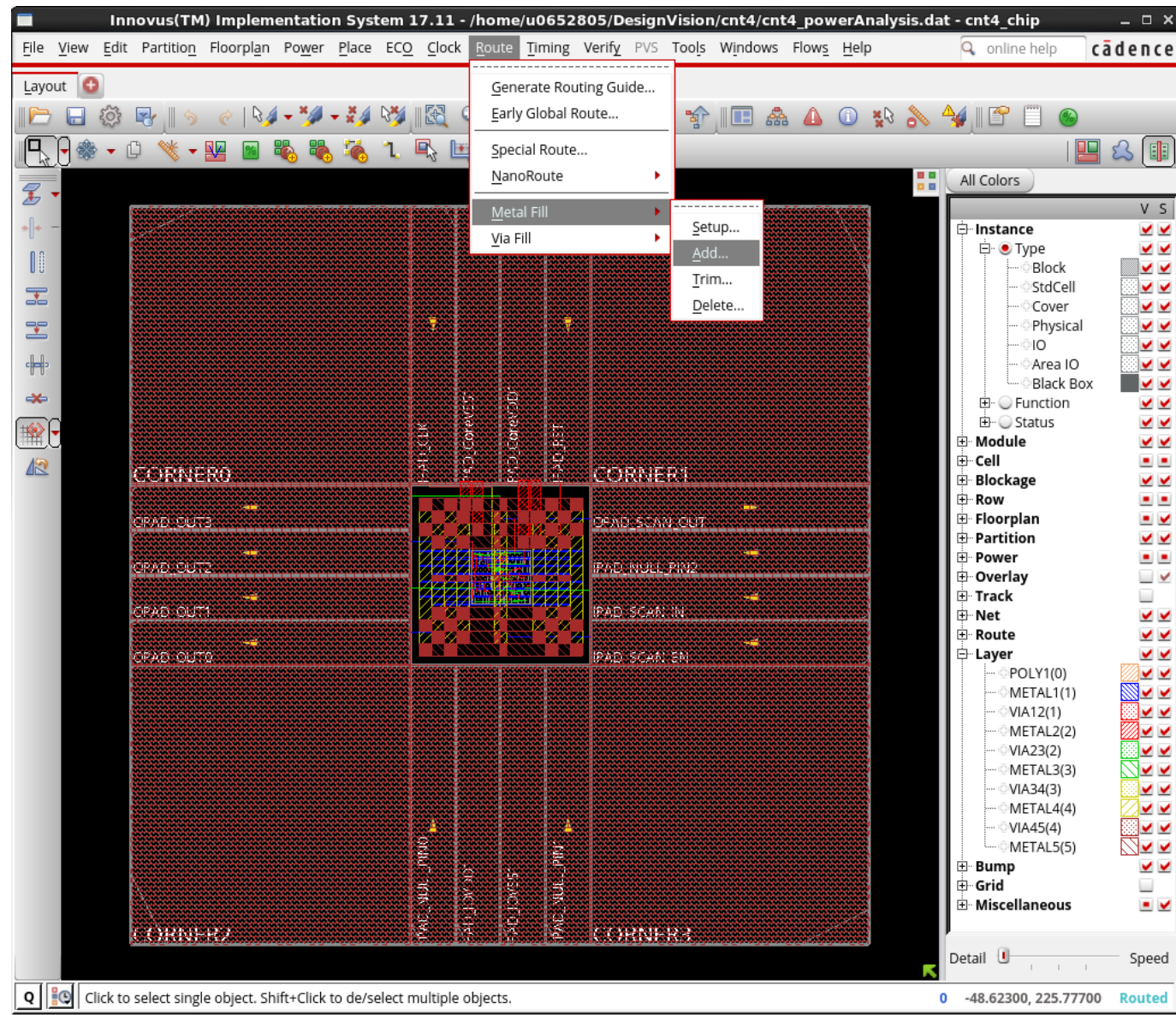
Fill Mode: ☒ Fill Wire ☐ Fill Wire OPC

1. **Window & Density**

Layer	Window Size		Step Size		Metal Density %			
	X	Y	X	Y	Min	Pref	Max	Ext
METAL1(1)	100.000	100.000	50.000	50.000	20.00	35.00 2.	50	35.00
METAL2(2)	100.000	100.000	50.000	50.000	20.00	35.00	50	35.00
METAL3(3)	100.000	100.000	50.000	50.000	20.00	35.00	50	35.00
METAL4(4)	100.000	100.000	50.000	50.000	20.00	35.00	50	35.00
METAL5(5)	100.000	100.000	50.000	50.000	20.00	35.00	50	35.00

3. **OK** Apply Save... Load... Defaults Cancel Help

Add dummy Metal



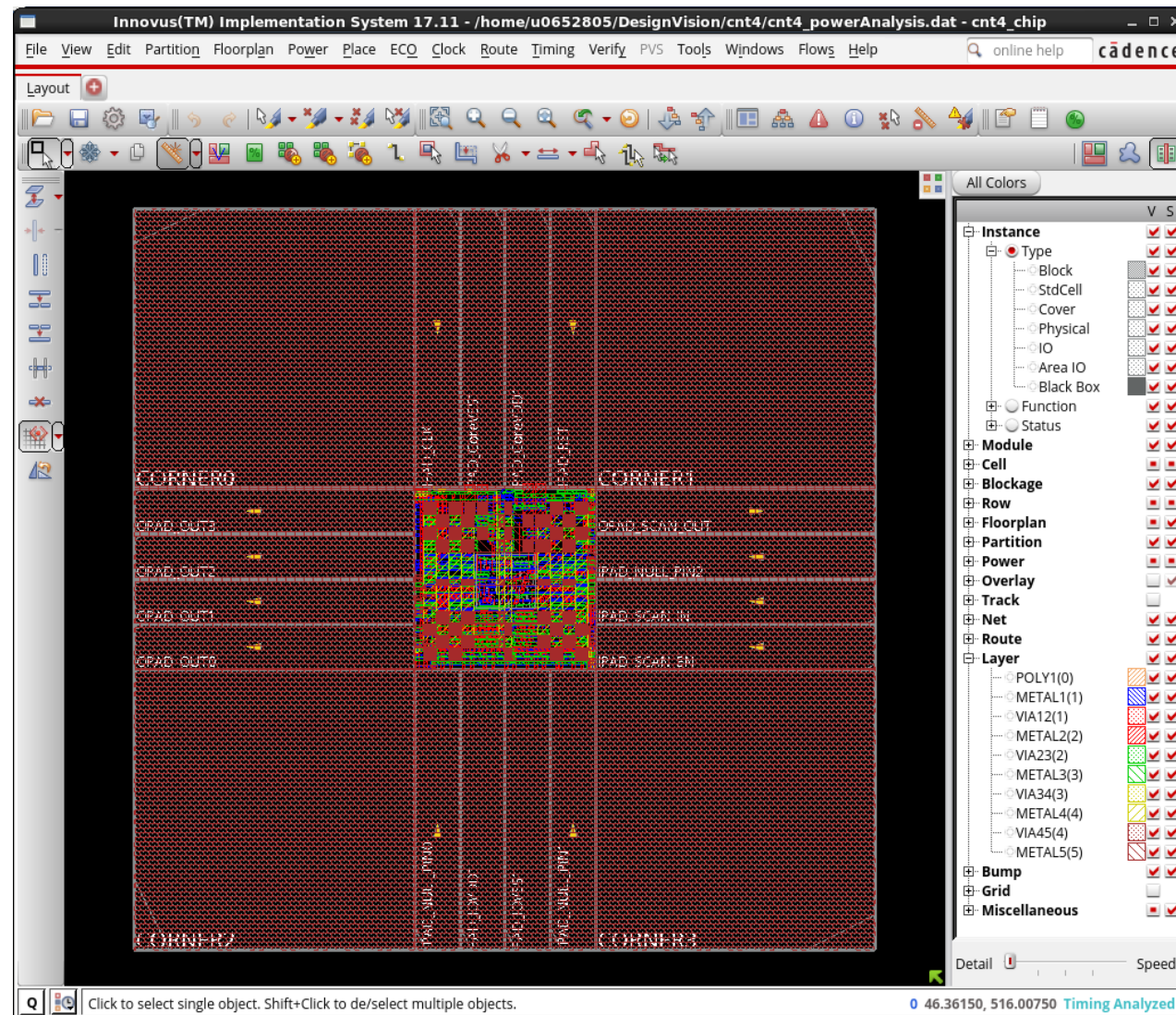
Add dummy Metal

The screenshot shows the 'Add Metal Fill' dialog box with the following settings and annotations:

- Number of Local CPU(s):** 1 (with a 'Set Multiple CPU...' button)
- Iteration Name List:** (empty text field)
- Model Selection**
 - Shape:** ☒ Rectangle ☐ Square
 - Connection:** ☐ Tie High/Low to Net(s): VSS VDD (Annotated with '1.' and a red box)
 - Connection Shape:** ☒ Tree ☐ Mesh
 - ☒ Keep Unconnected Metal Fill(s)
 - ☐ Square Shape
 - ☐ Use Generated Vias Only
 - Exclude Vias and Via Rules: (empty text field)
 - ☐ Snap to User Grid ☐ Stagger ☒ On ☐ Off ☐ Diag
 - ☐ Allow Fill on Cells ☐ Ignore Macro Density Table
- Incremental Control**
 - ☐ Delete Metal Fill before Creating New Metal Fill
 - ☒ FillWire ☒ FillWireOPC
- Layer Selection**
 - METAL1(1) METAL2(2) METAL3(3) METAL4(4) METAL5(5) (dropdown menu)
- ☒ Timing Aware
 - 2.** ☒ Critical Nets from Timing Analysis (Annotated with a red box and text: '當timing小於設定值時 旁邊少放 避免timing問題')
 - Slack Threshold: 0.4
 - ☐ Area
 - X1: 0.000 Y1: 0.000
 - X2: 0.000 Y2: 0.000

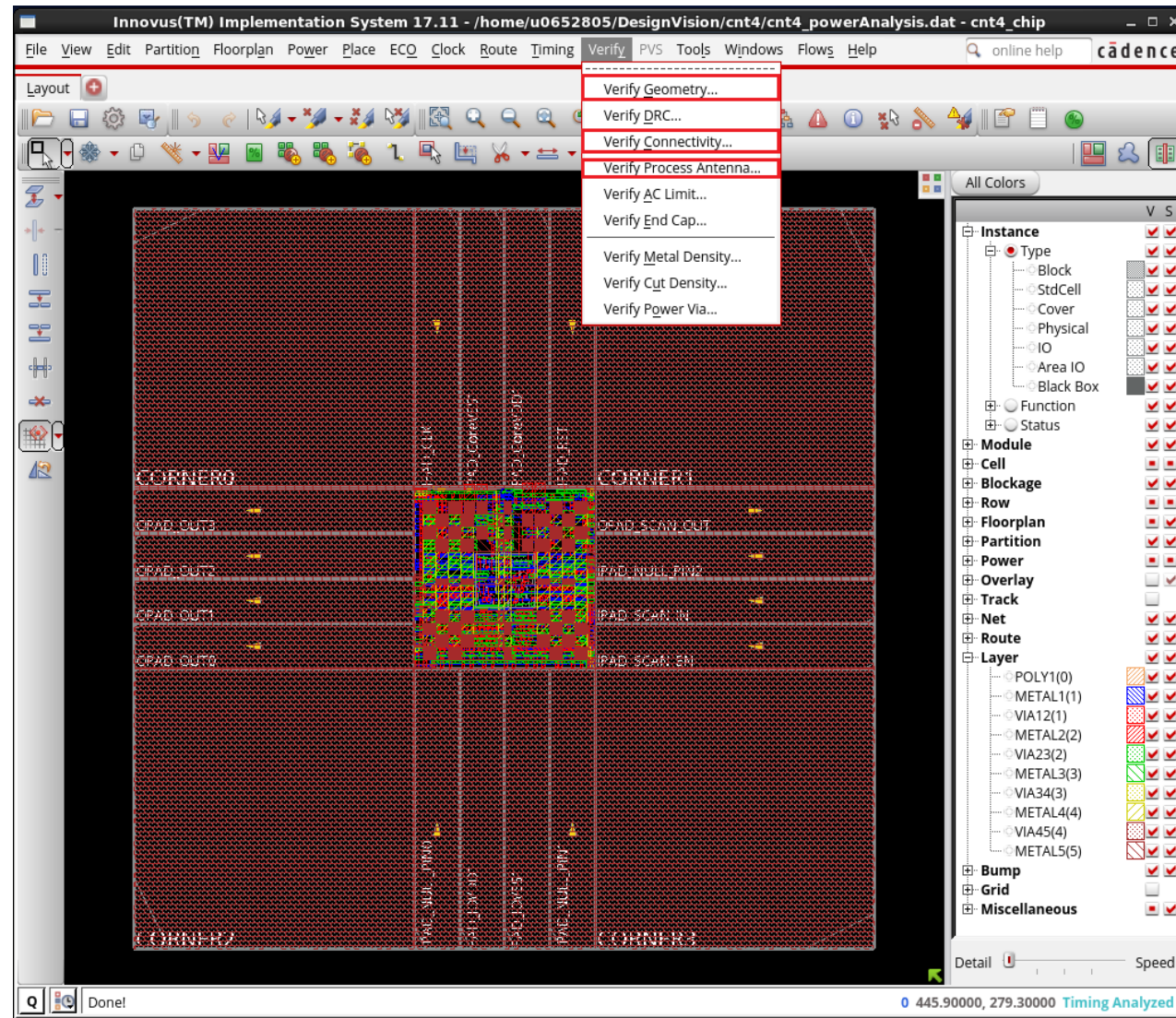
At the bottom, the **OK** button is annotated with '3.' and a red box.

可看到Dummy Metal已填滿



Add dummy Metal

Verify 這三個直接按ok後 確認無Viols即可



Add dummy Metal

```
u0652805@B510Server4:~/DesignVision/cnt4
檔案(F) 編輯(E) 檢視(V) 搜尋(S) 終端機(T) 求助(H)
VERIFY GEOMETRY ..... Creating Sub-Areas
..... bin size: 7040
VERIFY GEOMETRY ..... SubArea : 1 of 1
VERIFY GEOMETRY ..... Cells : 0 Viols.
VERIFY GEOMETRY ..... SameNet : 0 Viols.
VERIFY GEOMETRY ..... Wiring : 0 Viols.
VERIFY GEOMETRY ..... Antenna : 0 Viols.
VERIFY GEOMETRY ..... Sub-Area : 1 complete 0 Viols. 0 Wrngs.
VG: elapsed time: 0.00
Begin Summary ...
Cells : 0
SameNet : 0
Wiring : 0
Antenna : 0
Short : 0
Overlap : 0
End Summary

Verification Complete : 0 Viols. 0 Wrngs.

*****End: VERIFY GEOMETRY*****
*** verify geometry (CPU: 0:00:00.1 MEM: 0.0M)

innovus 4> VERIFY_CONNECTIVITY use new engine.
```

```
u0652805@B510Server4:~/DesignVision/cnt4
檔案(F) 編輯(E) 檢視(V) 搜尋(S) 終端機(T) 求助(H)
*** verify geometry (CPU: 0:00:00.1 MEM: 0.0M)

innovus 4> VERIFY_CONNECTIVITY use new engine.

***** Start: VERIFY CONNECTIVITY *****
Start Time: Tue Dec 18 16:05:12 2018

Design Name: cnt4_chip
Database Units: 2000
Design Boundary: (0.0000, 0.0000) (490.0000, 490.0000)
Error Limit = 1000; Warning Limit = 50
Check all nets

Begin Summary
Found no problems or warnings.
End Summary

End Time: Tue Dec 18 16:05:12 2018
Time Elapsed: 0:00:00.0

***** End: VERIFY CONNECTIVITY *****
Verification Complete : 0 Viols. 0 Wrngs.
(CPU Time: 0:00:00.0 MEM: 0.000M)
```

```
u0652805@B510Server4:~/DesignVision/cnt4
檔案(F) 編輯(E) 檢視(V) 搜尋(S) 終端機(T) 求助(H)
Design Boundary: (0.0000, 0.0000) (490.0000, 490.0000)
Error Limit = 1000; Warning Limit = 50
Check all nets

Begin Summary
Found no problems or warnings.
End Summary

End Time: Tue Dec 18 16:05:12 2018
Time Elapsed: 0:00:00.0

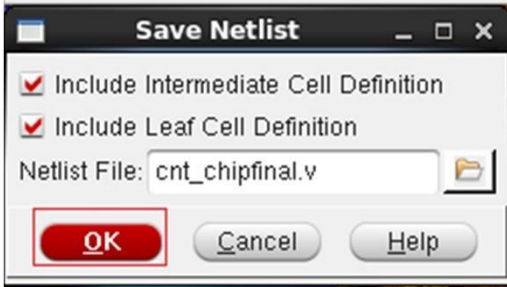
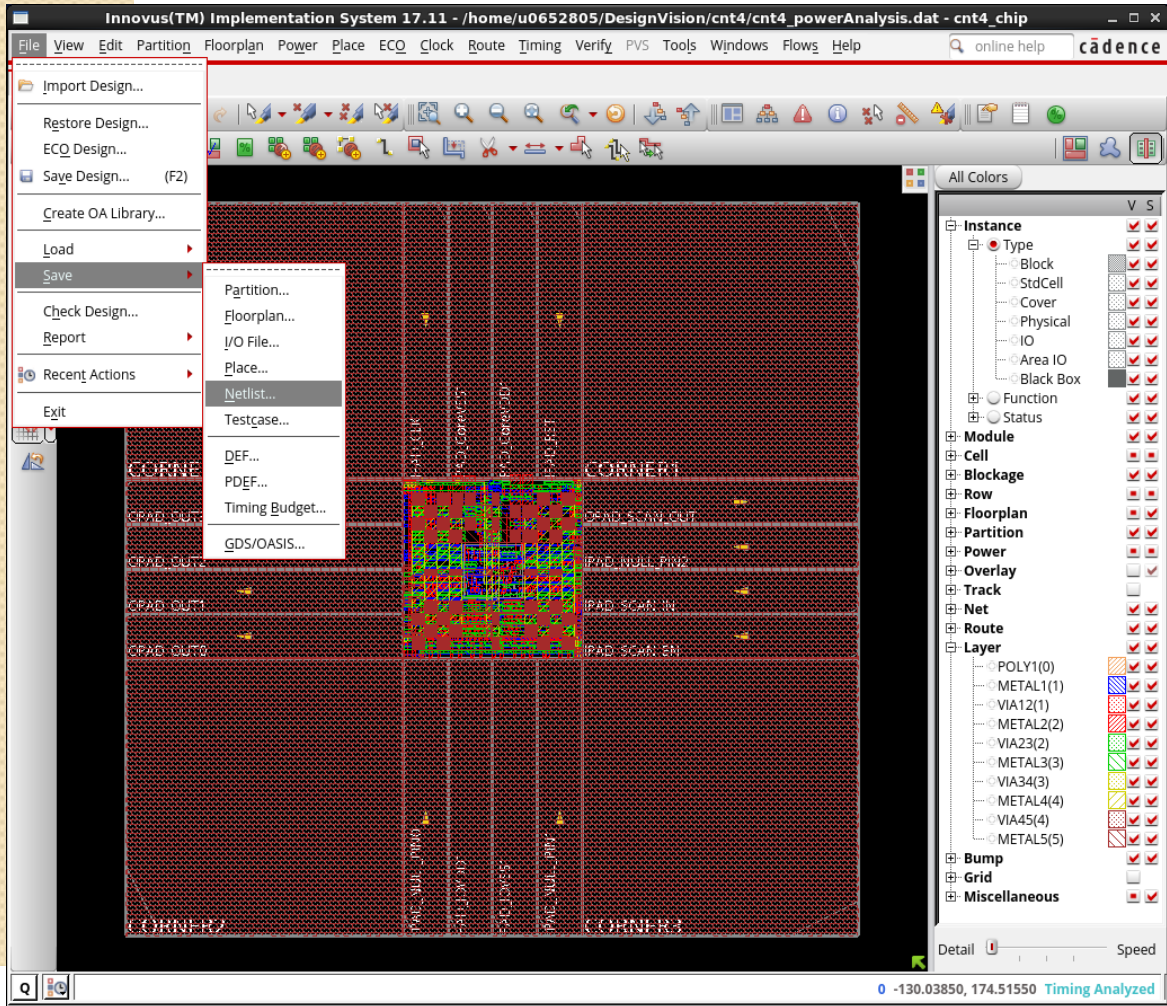
***** End: VERIFY CONNECTIVITY *****
Verification Complete : 0 Viols. 0 Wrngs.
(CPU Time: 0:00:00.0 MEM: 0.000M)

innovus 4>
***** START VERIFY ANTENNA *****
Report File: cnt4_chip.antenna.rpt
LEF Macro File: cnt4_chip.antenna.lef
Verification Complete: 0 Violations
***** DONE VERIFY ANTENNA *****
(CPU Time: 0:00:00.0 MEM: 0.000M)

innovus 4> █
```


The screenshot shows the 'File' menu of the Innova Design application. The menu is open, displaying the following options: 'Import Design...', 'Restore Design...', 'ECO Design...', 'Save Design...', 'Create OA Library', 'Load', 'Save' (highlighted), 'Check Design...', 'Report', 'Recent Actions', and 'Exit'. The 'Save' option is currently selected and highlighted in grey. The background of the application window is a light blue grid.

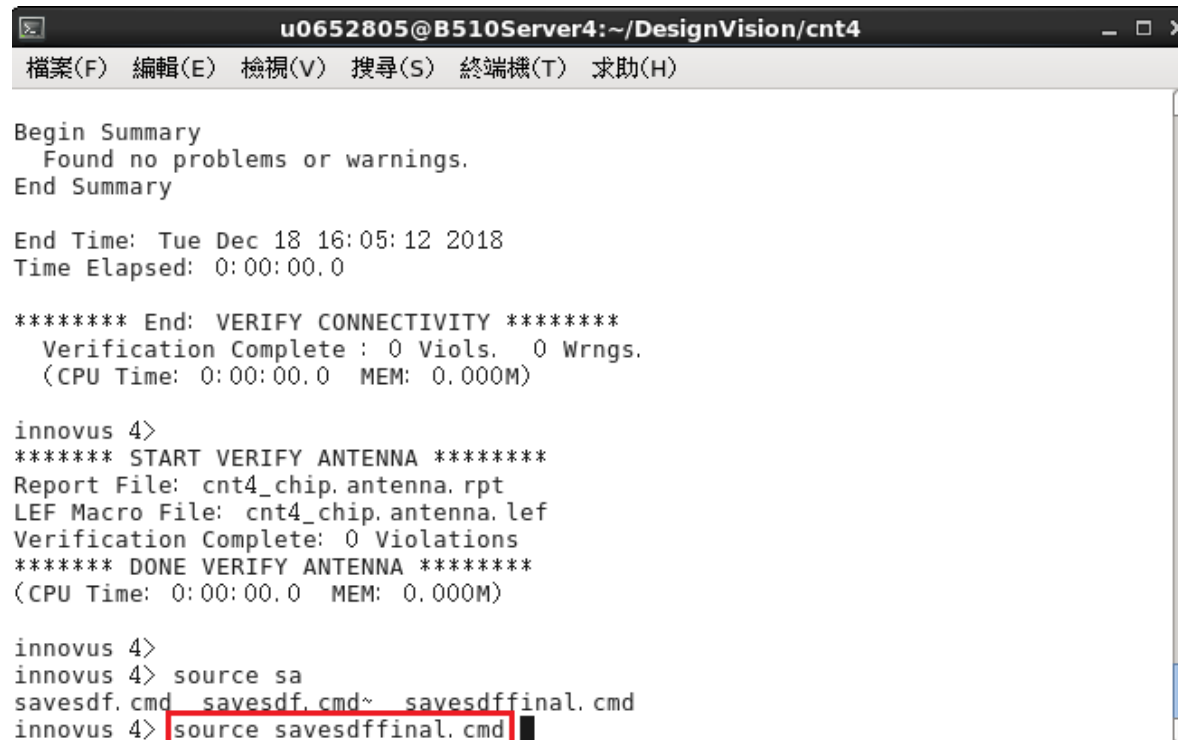
做完上述Routing等動作後，已趨近完成階段，做最後一次的Power分析是最接近真實電路的狀況。先儲存Netlist，檔名加Final區別。



PrimeTime PowerAnalysis

儲存SDF，複製Chap7的savesdf.cmd，將儲存檔名多加final並修改內容如下，並直接用Innovus打source savesdffinal.cmd

```
setAnalysisMode -analysisType bcwc
write_sdf -max_view av_func_mode_max \
  -min_view av_func_mode_min \
  -edges noedge -splitsetuphold -remashold -splitrecrem \
  -min_period_edges none cnt_chipfinal.sdf
```



```
u0652805@B510Server4:~/DesignVision/cnt4
檔案(F) 編輯(E) 檢視(V) 搜尋(S) 終端機(T) 求助(H)

Begin Summary
  Found no problems or warnings.
End Summary

End Time: Tue Dec 18 16:05:12 2018
Time Elapsed: 0:00:00.0

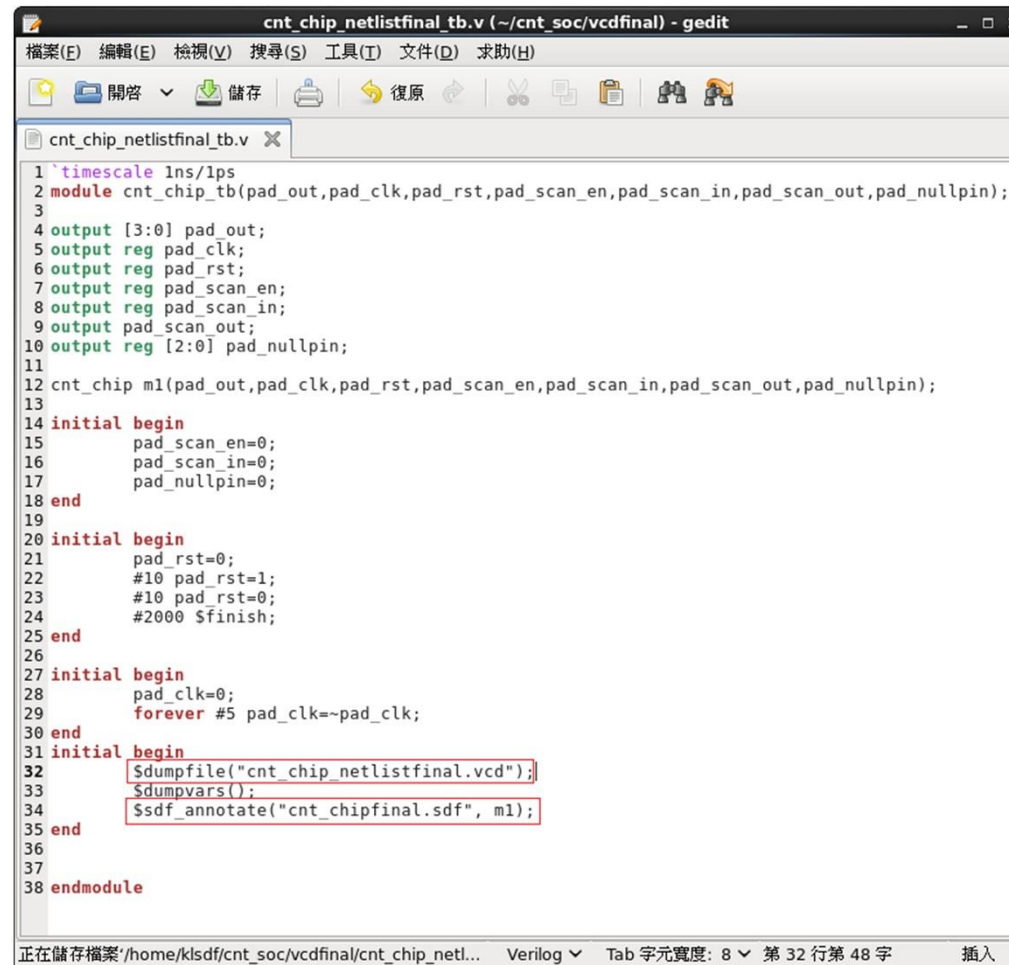
***** End: VERIFY CONNECTIVITY *****
Verification Complete : 0 Viols. 0 Wrngs.
(CPU Time: 0:00:00.0 MEM: 0.000M)

innovus 4>
***** START VERIFY ANTENNA *****
Report File: cnt4_chip.antenna.rpt
LEF Macro File: cnt4_chip.antenna.lef
Verification Complete: 0 Violations
***** DONE VERIFY ANTENNA *****
(CPU Time: 0:00:00.0 MEM: 0.000M)

innovus 4>
innovus 4> source sa
savesdf.cmd savesdf.cmd savesdffinal.cmd
innovus 4> source savesdffinal.cmd
```

PrimeTime PowerAnalysis

複製Chap7的Testbench只改dumpfile與sdf_annotate另存為
cnt_chip_netlistfinal_tb.v

A screenshot of a text editor window titled 'cnt_chip_netlistfinal_tb.v (~cnt_soc/vcdfinal) - gedit'. The window shows a Verilog testbench for a module named 'cnt_chip'. The code includes a timescale of 1ns/1ps, a module definition for 'cnt_chip_tb' with inputs 'pad_out', 'pad_clk', 'pad_rst', 'pad_scan_en', 'pad_scan_in', 'pad_scan_out', and 'pad_nullpin'. It defines several output signals: 'pad_out' [3:0], 'pad_clk', 'pad_rst', 'pad_scan_en', 'pad_scan_in', 'pad_scan_out', and 'pad_nullpin' [2:0]. An instance of 'cnt_chip' is created as 'm1'. There are three initial blocks: the first initializes 'pad_scan_en', 'pad_scan_in', and 'pad_nullpin' to 0; the second initializes 'pad_rst' to 0, then sets it to 1 for 10 time units, back to 0 for 10 time units, and finally finishes at 2000 time units; the third initializes 'pad_clk' to 0 and then toggles it every 5 time units forever. At the end of the testbench, it calls '\$dumpfile' to save the waveform to 'cnt_chip_netlistfinal.vcd', '\$dumpvars' to save the variables, and '\$sdf_annotate' to generate the power analysis file 'cnt_chipfinal.sdf' for the instance 'm1'. The status bar at the bottom indicates the file is being saved to '/home/ksdf/cnt_soc/vcdfinal/cnt_chip_netl...', it is Verilog, the tab width is 8, and the cursor is at line 32, column 48.

```
1 `timescale 1ns/1ps
2 module cnt_chip_tb(pad_out,pad_clk,pad_rst,pad_scan_en,pad_scan_in,pad_scan_out,pad_nullpin);
3
4 output [3:0] pad_out;
5 output reg pad_clk;
6 output reg pad_rst;
7 output reg pad_scan_en;
8 output reg pad_scan_in;
9 output pad_scan_out;
10 output reg [2:0] pad_nullpin;
11
12 cnt_chip m1(pad_out,pad_clk,pad_rst,pad_scan_en,pad_scan_in,pad_scan_out,pad_nullpin);
13
14 initial begin
15     pad_scan_en=0;
16     pad_scan_in=0;
17     pad_nullpin=0;
18 end
19
20 initial begin
21     pad_rst=0;
22     #10 pad_rst=1;
23     #10 pad_rst=0;
24     #2000 $finish;
25 end
26
27 initial begin
28     pad_clk=0;
29     forever #5 pad_clk=~pad_clk;
30 end
31 initial begin
32     $dumpfile("cnt_chip_netlistfinal.vcd");
33     $dumpvars();
34     $sdf_annotate("cnt_chipfinal.sdf", m1);
35 end
36
37
38 endmodule
```

正在儲存檔案 /home/ksdf/cnt_soc/vcdfinal/cnt_chip_netl... Verilog Tab 字元寬度: 8 第 32 行第 48 字 插入

PrimeTime PowerAnalysis

新增一個vcdfinal的資料夾確認有以下檔案後，照Chap7 p31所教的產生vcd

A screenshot of a terminal window titled "終端機" (Terminal). The window has a menu bar with options: 檔案(E), 編輯(E), 檢視(V), 搜尋(S), 終端機(T), and 求助(H). The terminal shows the command "ls" being executed in the directory "/home/kl sdf/cnt_soc/vcdfinal". The output lists several files: "cnt_chipfinal.sdf", "cnt_chip_netlistfinal_tb.v", "tpz973gv.v", "cnt_chipfinal.v", "cnt_chip_netlistfinal_tb.v~", and "tsmc18.v". The prompt "b510-175:/home/kl sdf/cnt_soc/vcdfinal\$" is visible at the bottom of the terminal.

```
終端機
檔案(E) 編輯(E) 檢視(V) 搜尋(S) 終端機(T) 求助(H)
b510-175:/home/kl sdf/cnt_soc/vcdfinal$ls
cnt_chipfinal.sdf  cnt_chip_netlistfinal_tb.v  tpz973gv.v
cnt_chipfinal.v   cnt_chip_netlistfinal_tb.v~  tsmc18.v
b510-175:/home/kl sdf/cnt_soc/vcdfinal$
```

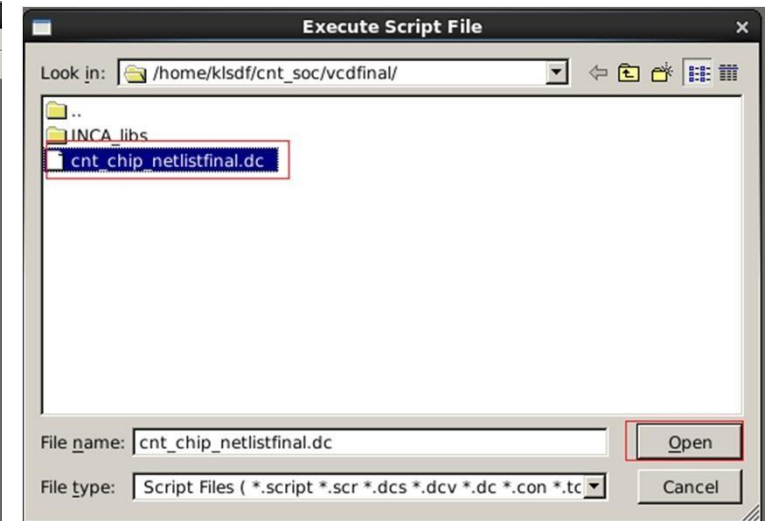
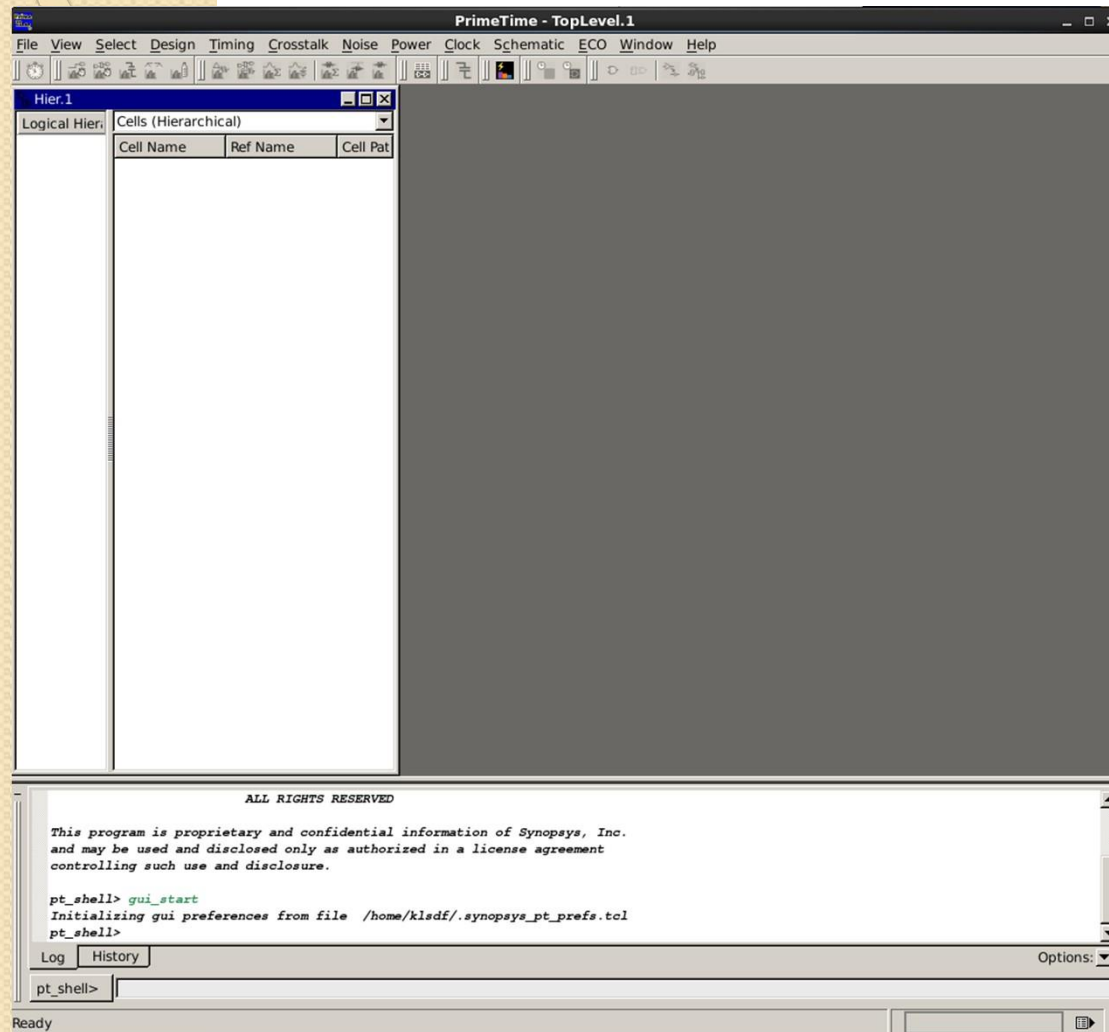
PrimeTime PowerAnalysis

PrimeTime DC File，至工作站的pt資料夾下抓取下來修改。

```
cnt_chip_netlistfinal.dc X
1 set designer "SOC"
2 set company "VLSIDA Lab."
3
4 set lib_base /cad/techfile
5
6 #/*TSMC018 1p6m*/
7 set search_path "/usr/techfile/CBDK_TSMC018_Arm_v3.2/CIC/SynopsysDC/db $search_path"
8 set link_library "* slow.db fast.db tpz973gvwc.db tpz973gvbc.db"
9 set target_library "slow.db fast.db"
10
11
12 set power_enable_analysis TRUE
13 set power_analysis_mode time_based
14
15 read_verilog ./cnt_chip_netlistfinal.v
16 current_design cnt_chip
17 link
18
19 # -strip_path [testbench name] / [include module name] [vcd name]
20 read_vcd -strip_path cnt_chip_tb/m1 ./cnt_chip_netlistfinal.vcd
21
22 TestBench裡Module與Intance Name與VCD檔名
23 set power_analysis_options -waveform_format fsdb -waveform_output pwr -waveform_interval 1
24 update_power
25
26 redirect -bg -file power.rpt {report_power -hierarchy}
27 report_power
```

PrimeTime PowerAnalysis

在Terminal打pt執行PrimeTime並載入dc



載入成功後就可以在Terminal看到power資訊

PrimeTime PowerAnalysis

目錄下有power.rpt用gedit打開觀看細部power資訊

```
cnt_chip_netlistfinal.dc x power.rpt x
1 [457] Start Time: Wed Dec 26 18:18:52 2012
2
3 *****
4 Report : Time Based Power
5         -hierarchy
6 Design : cnt_chip
7 Version: E-2010.12-SP3-1
8 Date   : Wed Dec 26 18:18:52 2012
9 *****
10
11
12
13
14 Hierarchy
15 -----
16 cnt_chip
17   k1 (cnt)
18
19
20
21 Hierarchy
22 -----
23 cnt_chip
24   k1 (cnt)
25 [457] Finish Time: Wed Dec 26 18:18:52 2012
26 |
```

	Switch Power	Int Power	Leak Power	Total Power	%
cnt_chip	0.000	0.000	1.55e-07	1.55e-07	100.0
k1 (cnt)	0.000	0.000	2.56e-08	2.56e-08	16.5

	Peak Power	Peak Time	Glitch Power	X-tran Power
cnt_chip	1.55e-07	0-1	0.000	0.000
k1 (cnt)	2.56e-08	0-1	0.000	0.000