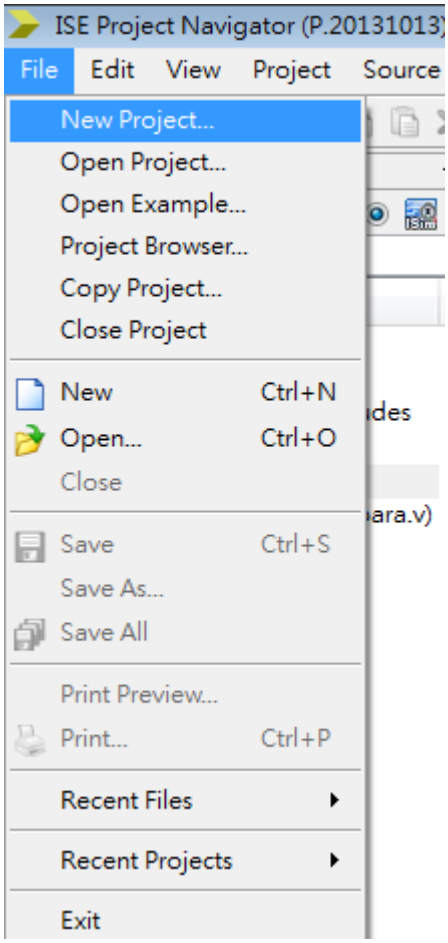
Xilinx ISE 14.7 Training

1. 以 **Xilinx ISE** 做為驗證環境

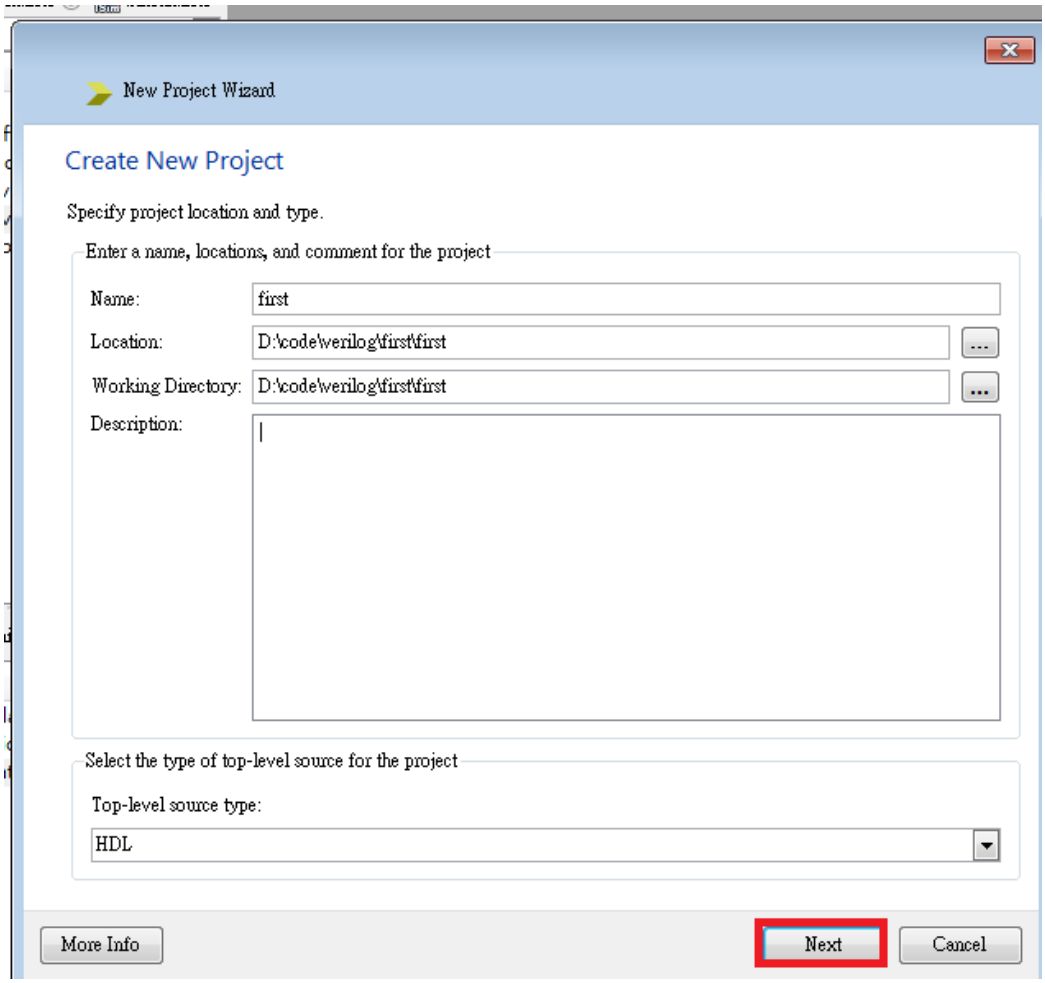
(配合 **cnt.v** , 及**cnt_tb.v** 為例)

New project:

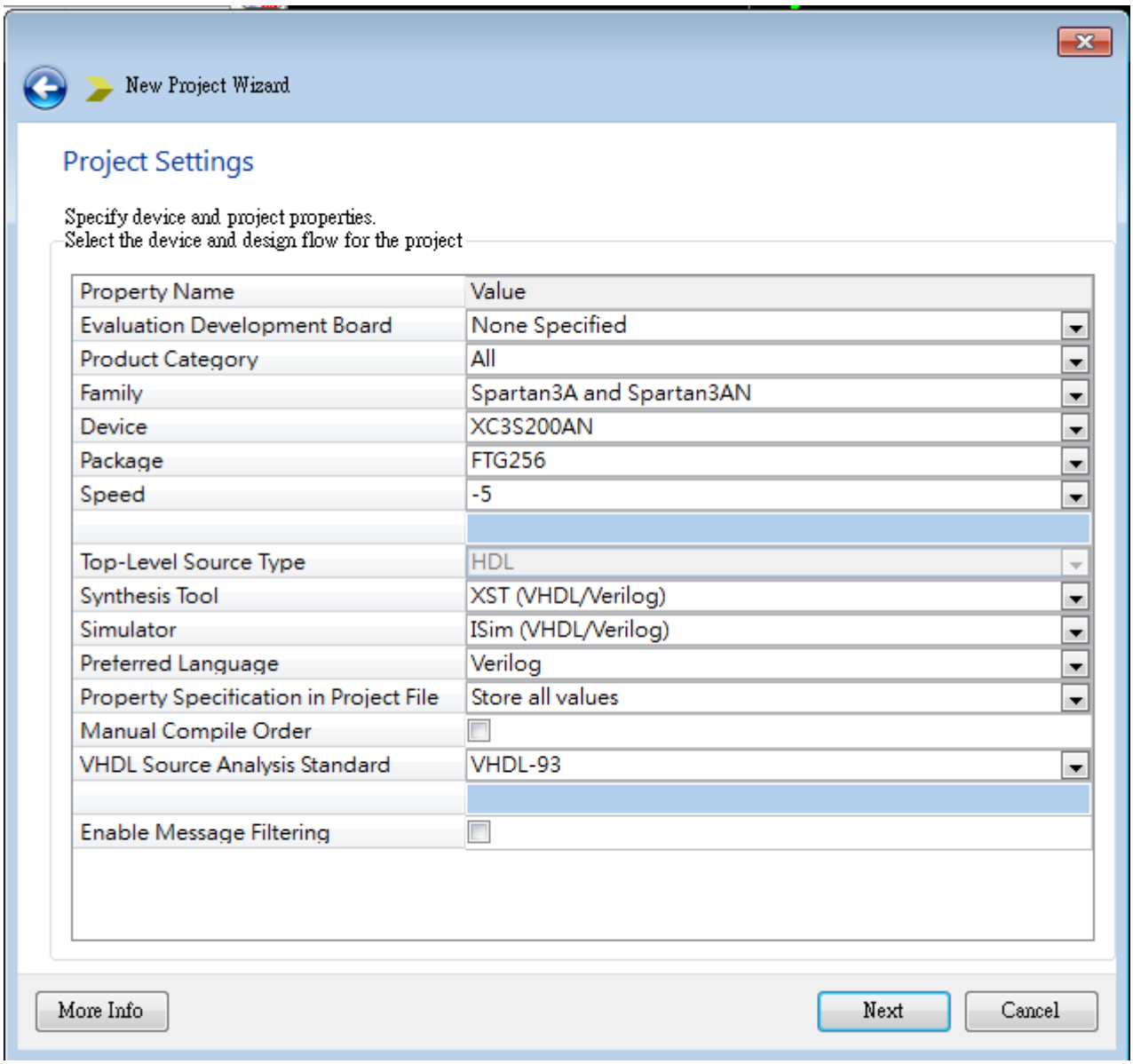
(1) File子New Project

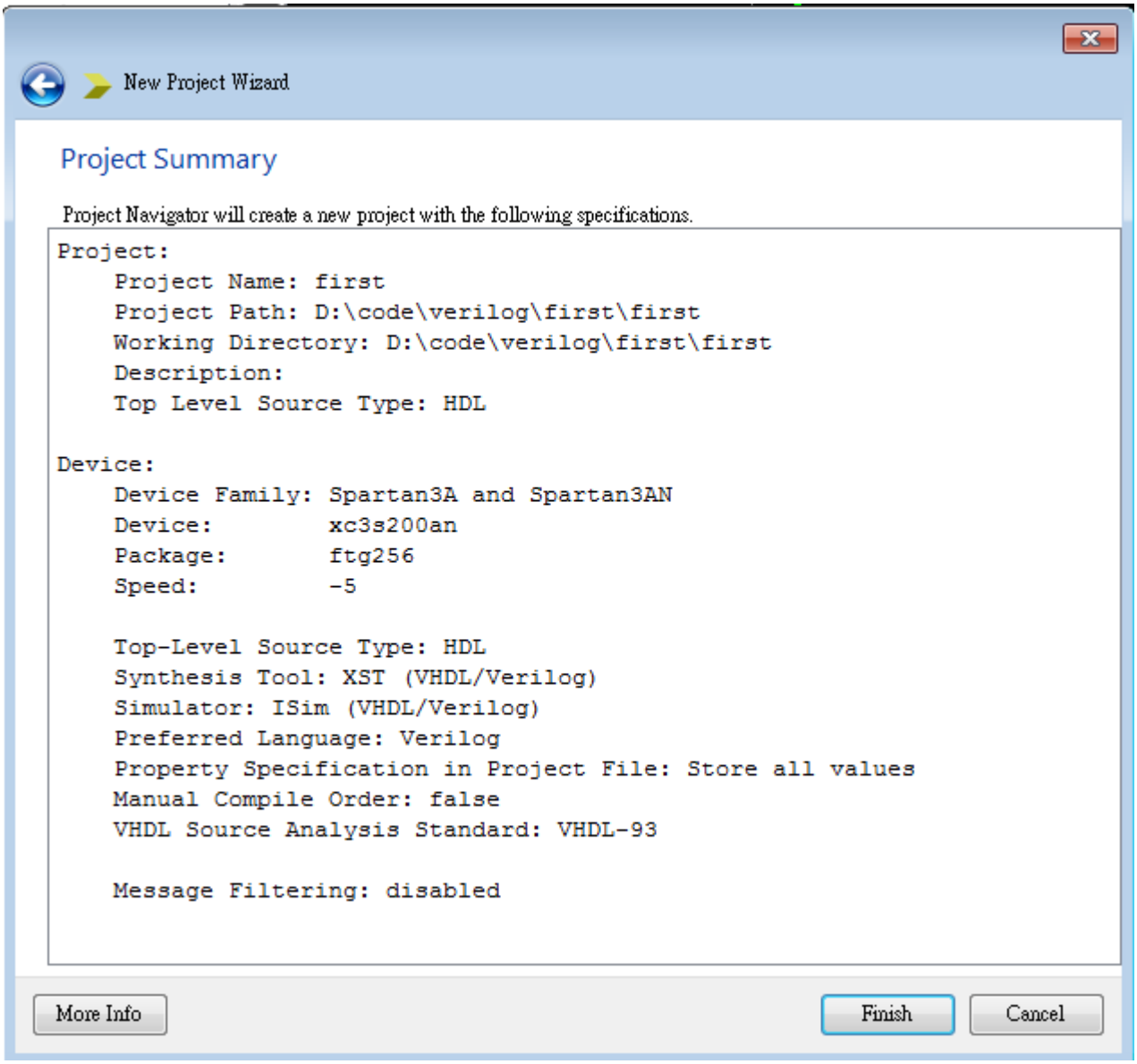


(2) Create New Project: Project Name, Project Location, Top-Level Source Type

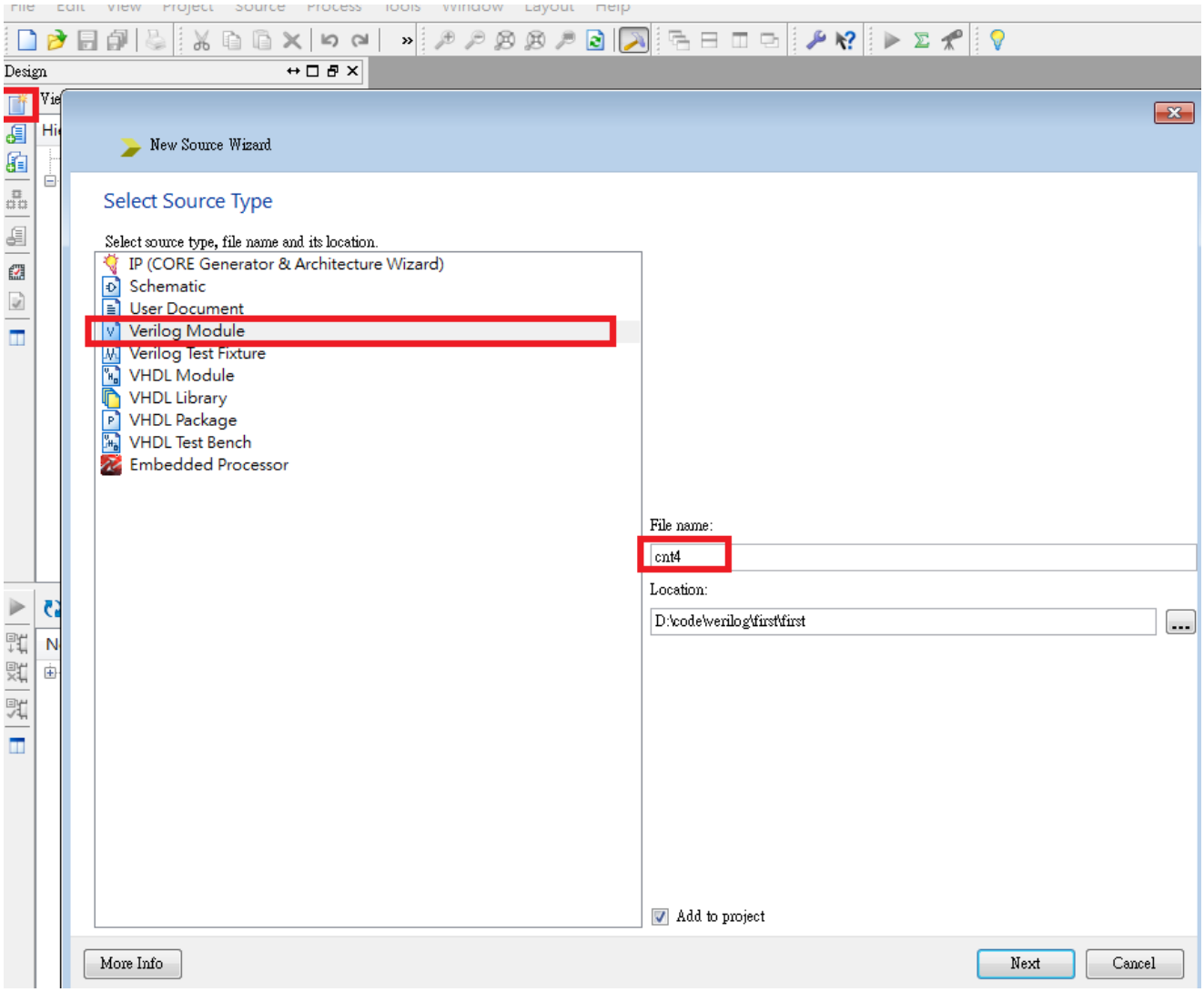


(3) Device Properties: Family, Device, Package, Speed 子看 FPGA board 上的 chip

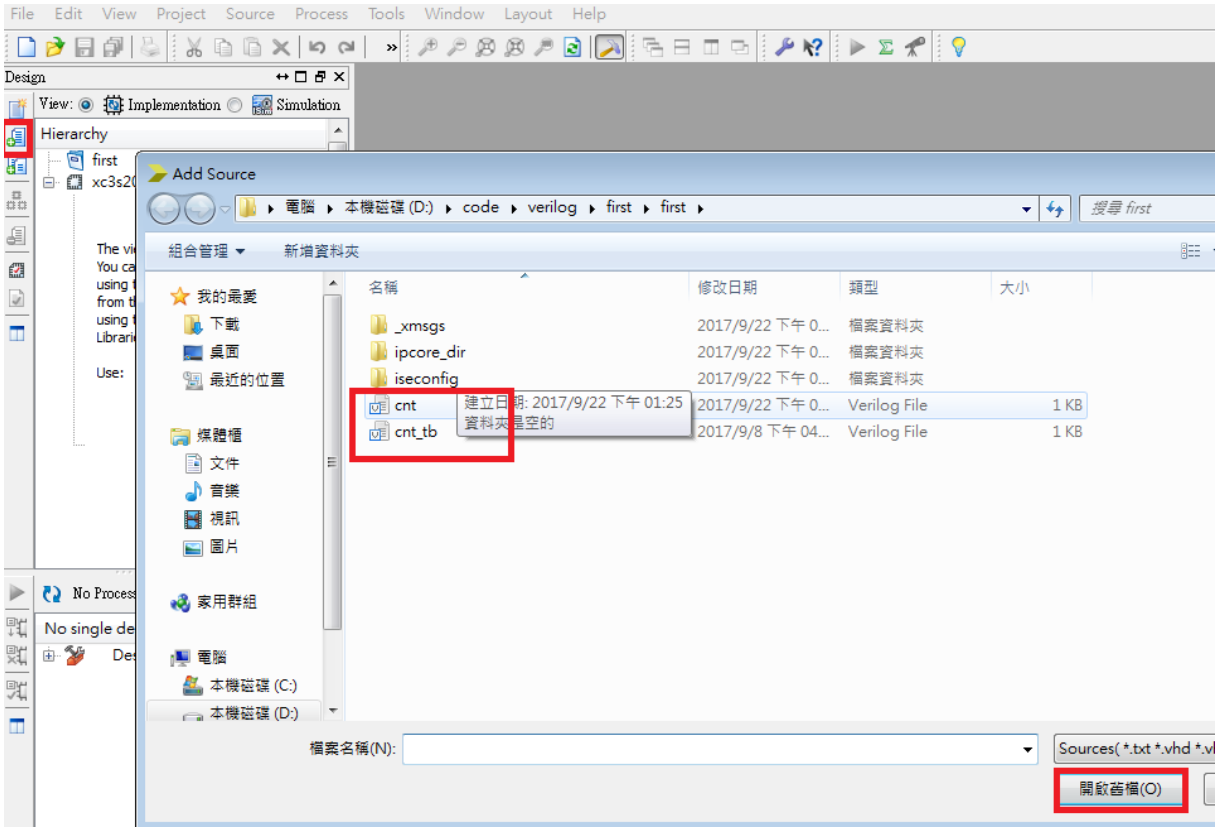



New Project Wizard
Project Summary
Project Navigator will create a new project with the following specifications.
Project:
Project Name: first
Project Path: D:\code\verilog\first\first
Working Directory: D:\code\verilog\first\first
Description:
Top Level Source Type: HDL
Device:
Device Family: Spartan3A and Spartan3AN
Device: xc3s200an
Package: ftg256
Speed: -5
Top-Level Source Type: HDL
Synthesis Tool: XST (VHDL/Verilog)
Simulator: ISim (VHDL/Verilog)
Preferred Language: Verilog
Property Specification in Project File: Store all values
Manual Compile Order: false
VHDL Source Analysis Standard: VHDL-93
Message Filtering: disabled
More Info
Finish
Cancel

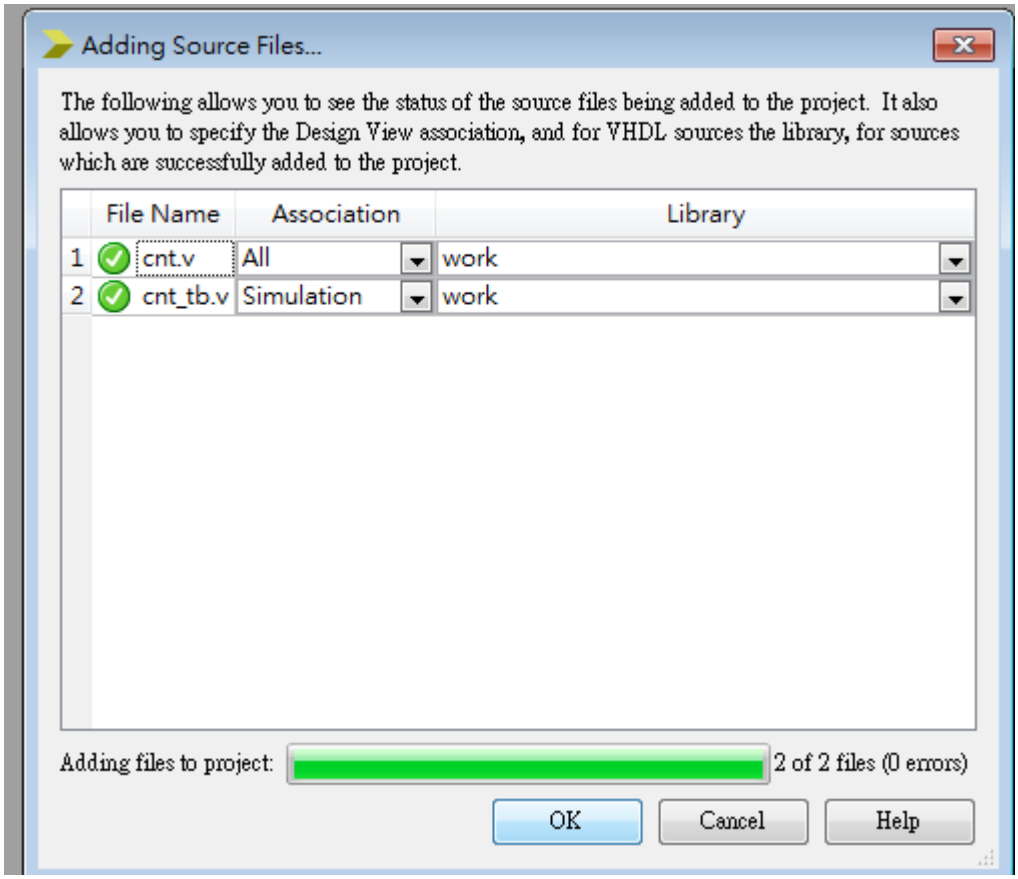
(4) Create New Source: 若需直接在 ISE 上寫程式，則使用此項。若程式已經寫好，則跳過此 選項。



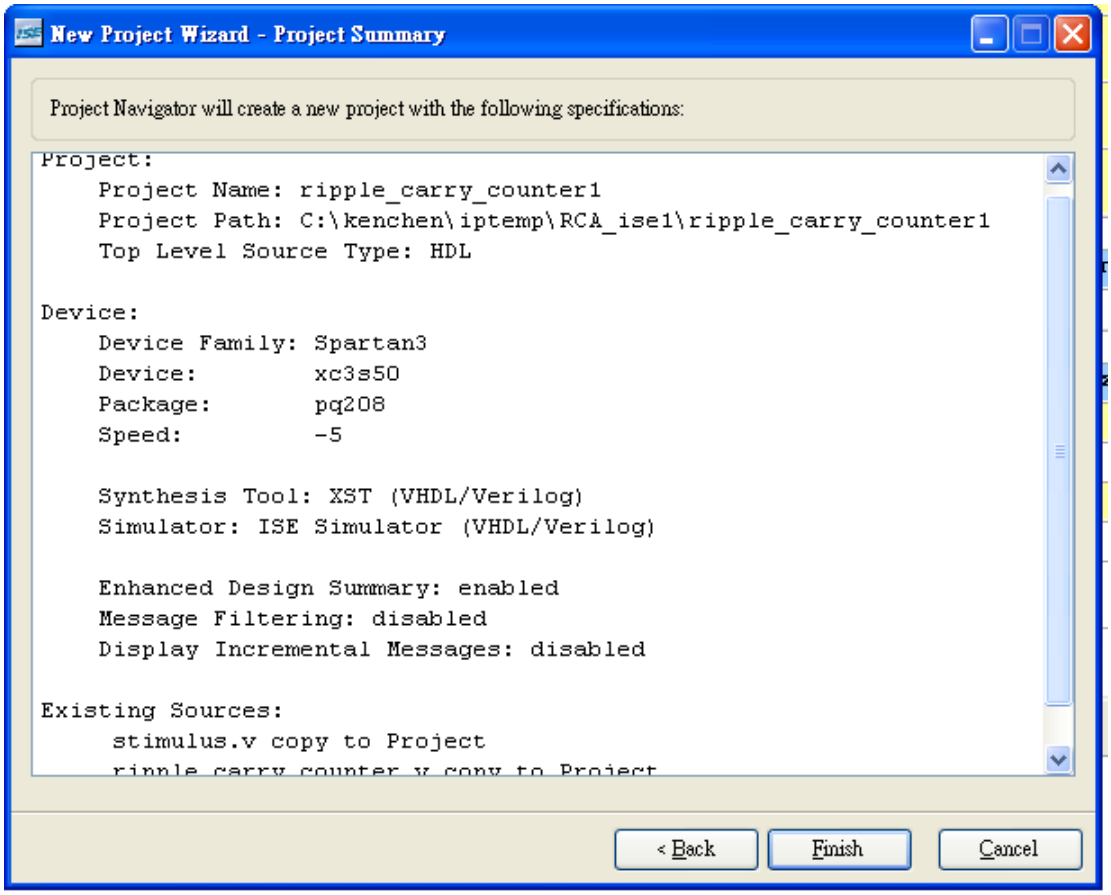
(5) Add Existing Sources: 選取 cnt4.v 及 cnt_tb.v(測試檔)



兩隻程式已經被加入:

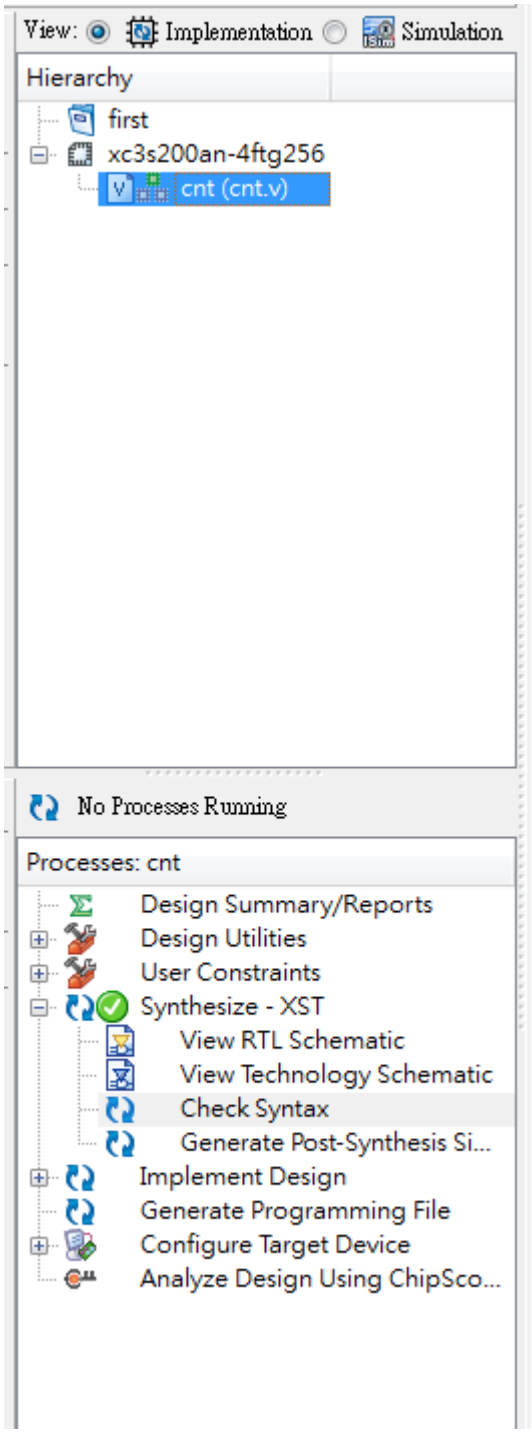


(6) Project Summary:

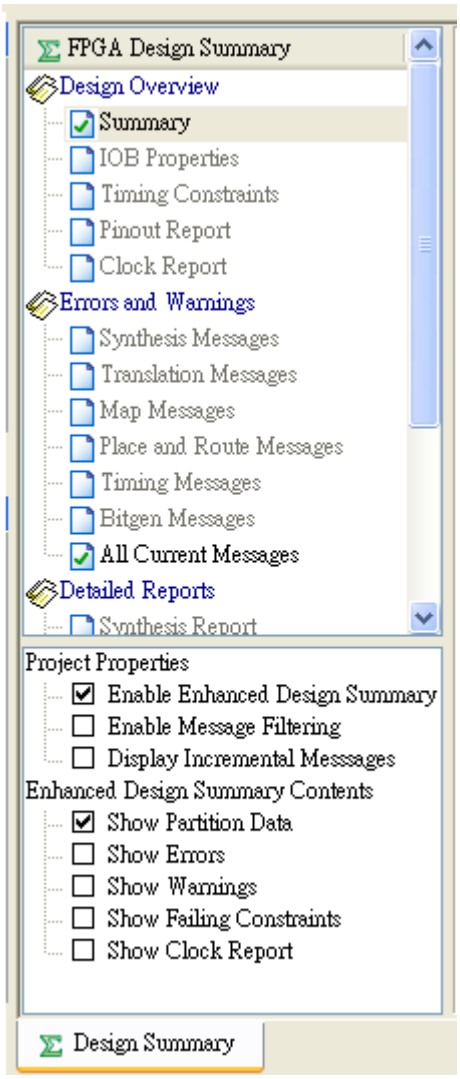


(7) 主畫面**:**

Sources, Processes:



FPGA Design Summary:



Report: 基本報告

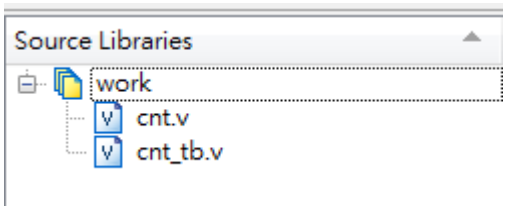
Libraries:

cnt Project Status (09/22/2017 - 14:14:29)			
Project File:	first.xise	**Parser Errors:**	No Errors
Module Name:	cnt	**Implementation State:**	Synthesized
Target Device:	xc3s200an-4ftg256	• **Errors:**	No Errors
Product Version:	ISE 14.7	• **Warnings:**	No Warnings
Design Goal:	Balanced	• **Routing Results:**	
Design Strategy:	Xilinx Default (unlocked)	• **Timing Constraints:**	
Environment:	System Settings	• **Final Timing Score:**	

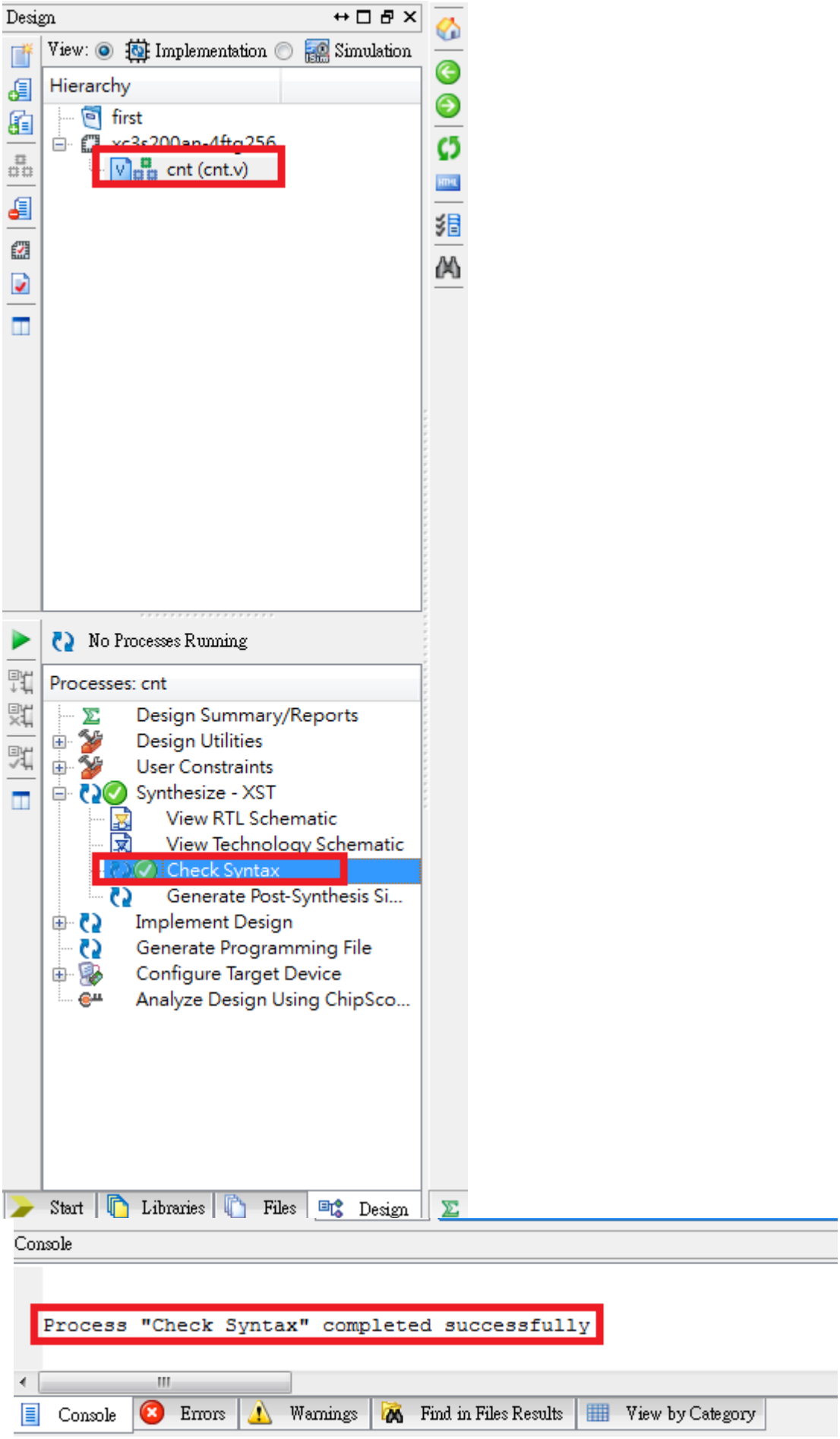
Device Utilization Summary (estimated values) [-]			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slices	2	1792	0%
Number of Slice Flip Flops	4	3584	0%
Number of 4 input LUTs	4	3584	0%
Number of bonded IOBs	6	195	3%
Number of GCLKs	1	24	4%

Detailed Reports [-]					
Report Name	**Status**	**Generated**	**Errors**	**Warnings**	**Infos**
Synthesis Report	Current	週五 九月 22 14:14:28 2017	0	0	0
Translation Report					
Map Report					
Place and Route Report					
Power Report					
Post-PAR Static Timing Report					
Bitgen Report					

Secondary Reports [-]		
Report Name	**Status**	**Generated**

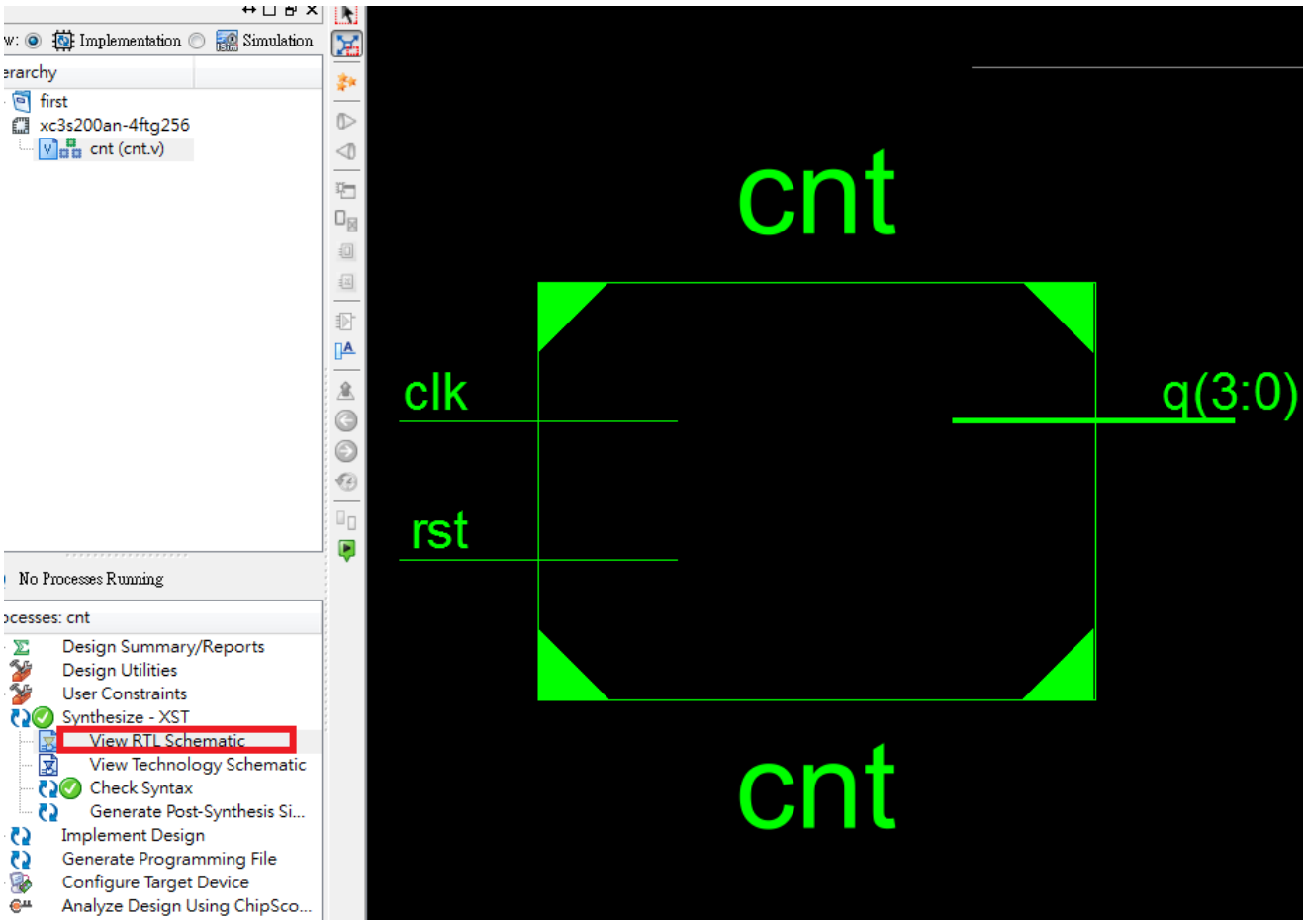


(8)**Check Syntax:** 檢查 **code** 的語法是否有錯



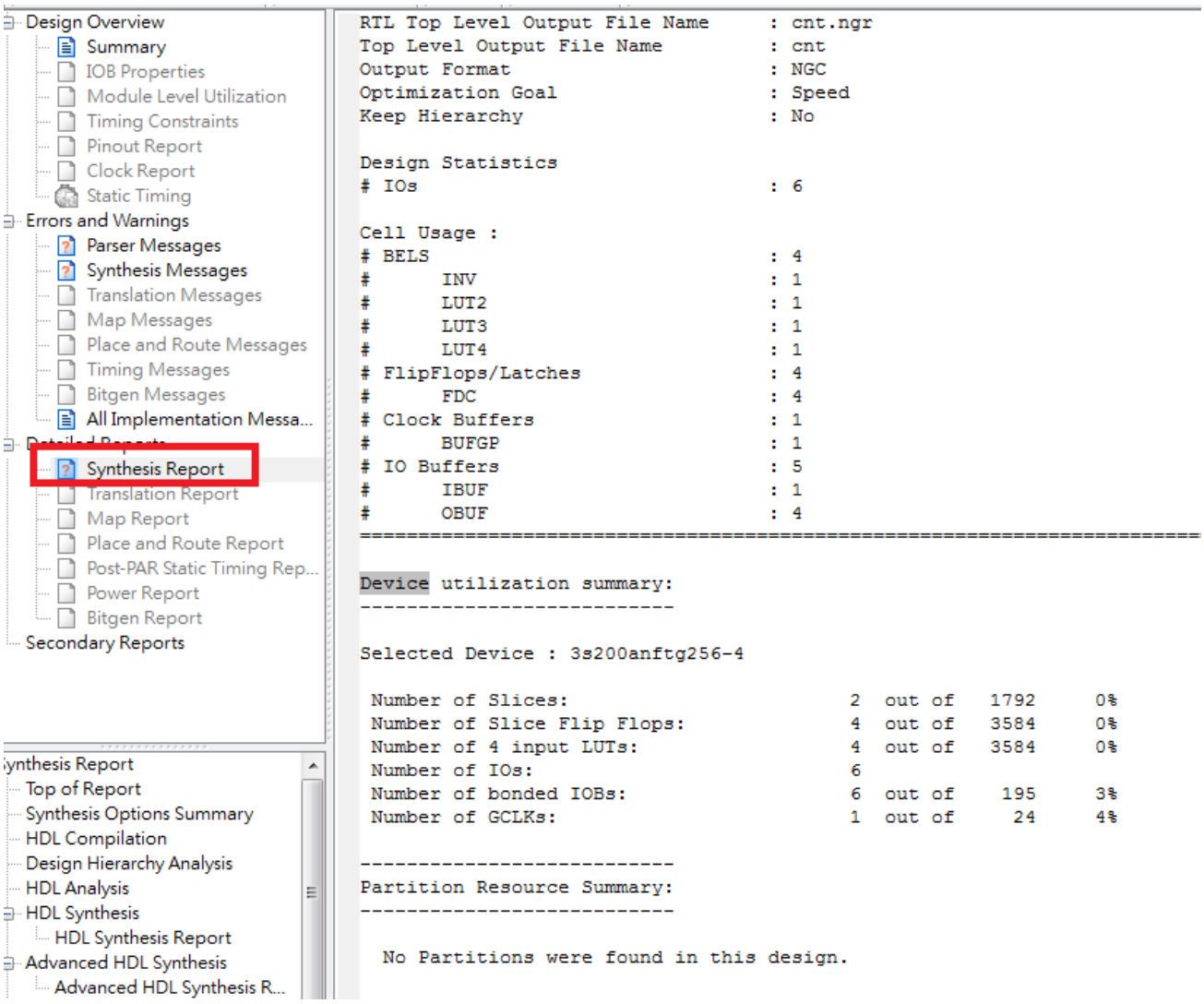
(9) View RTL Schematic: RTL code 的裝構圖

Sources子 Design: 內合主程式構成之 modules



(10) View Synthesis Report: 合成結果

Device utilization summary: 使用 device 的資源有多少



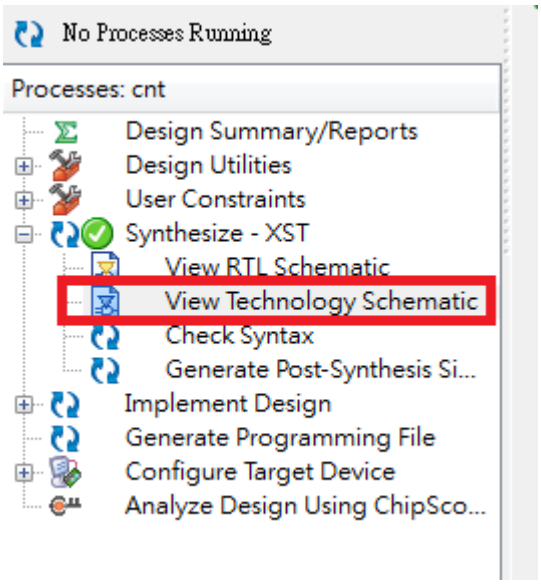
Timing Summary: 最快頻率可以到多少

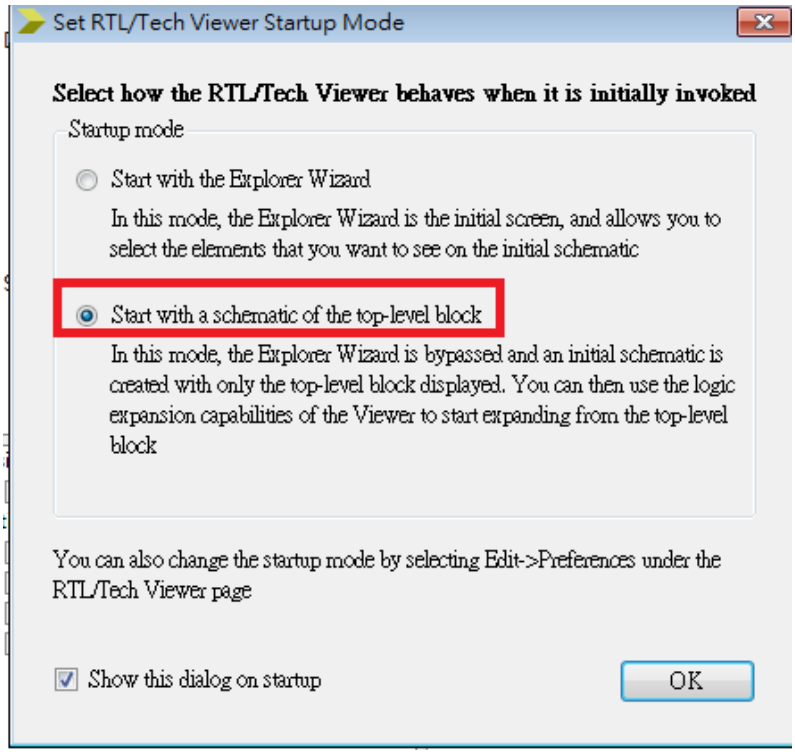
```
Timing Summary:
---------------
Speed Grade: -4

   Minimum period: 2.544ns (Maximum Frequency: 393.082MHz)
   Minimum input arrival time before clock: No path found
   Maximum output required time after clock: 5.744ns
   Maximum combinational path delay: No path found

Timing Detail:
--------------
All values displayed in nanoseconds (ns)
```

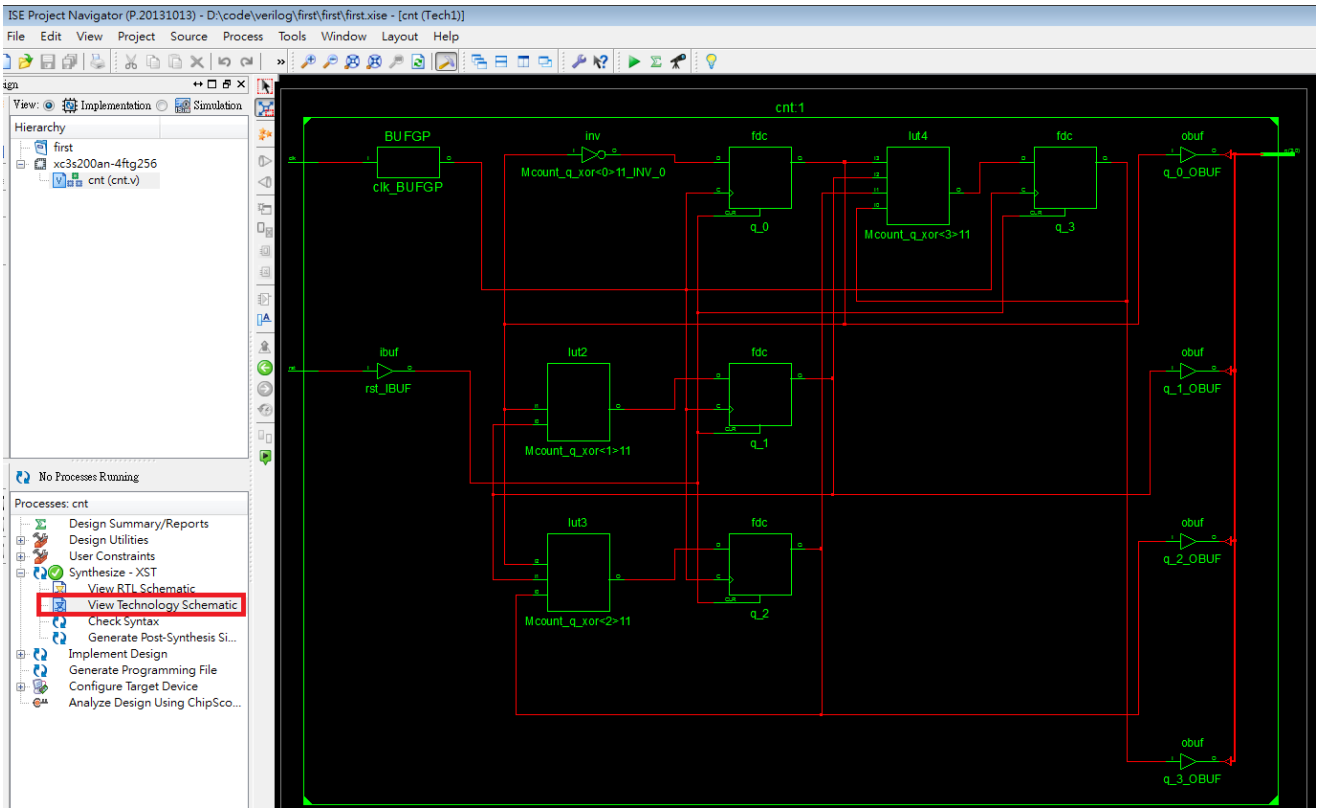
最長路徑:

```
================================================================================
Timing constraint: Default OFFSET OUT AFTER for Clock 'clk'
  Total number of paths / destination ports: 4 / 4
--------------------------------------------------------------------------------
Offset:              5.744ns (Levels of Logic = 1)
  Source:            q_0 (FF)
  Destination:       q<0> (PAD)
  Source Clock:      clk rising

  Data Path: q_0 to q<0>
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FDC:C->Q              5   0.591   0.633  q_0 (q_0)
     OBUF:I->O                 4.520          q_0_OBUF (q<0>)
    ----------------------------------------
    Total                      5.744ns (5.111ns logic, 0.633ns route)
                                       (89.0% logic, 11.0% route)

================================================================================


Total REAL time to Xst completion: 5.00 secs
Total CPU time to Xst completion: 5.10 secs

-->
```

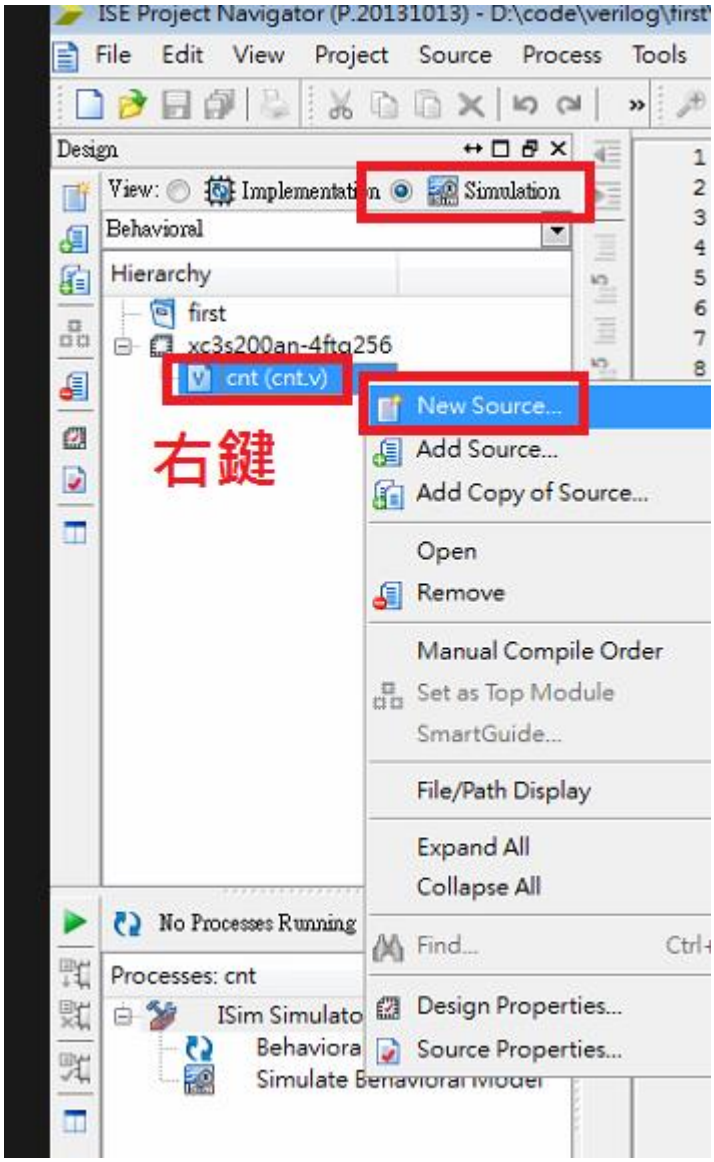
(11) Processes子 View Technology Schematic: 經合成後的電路圖

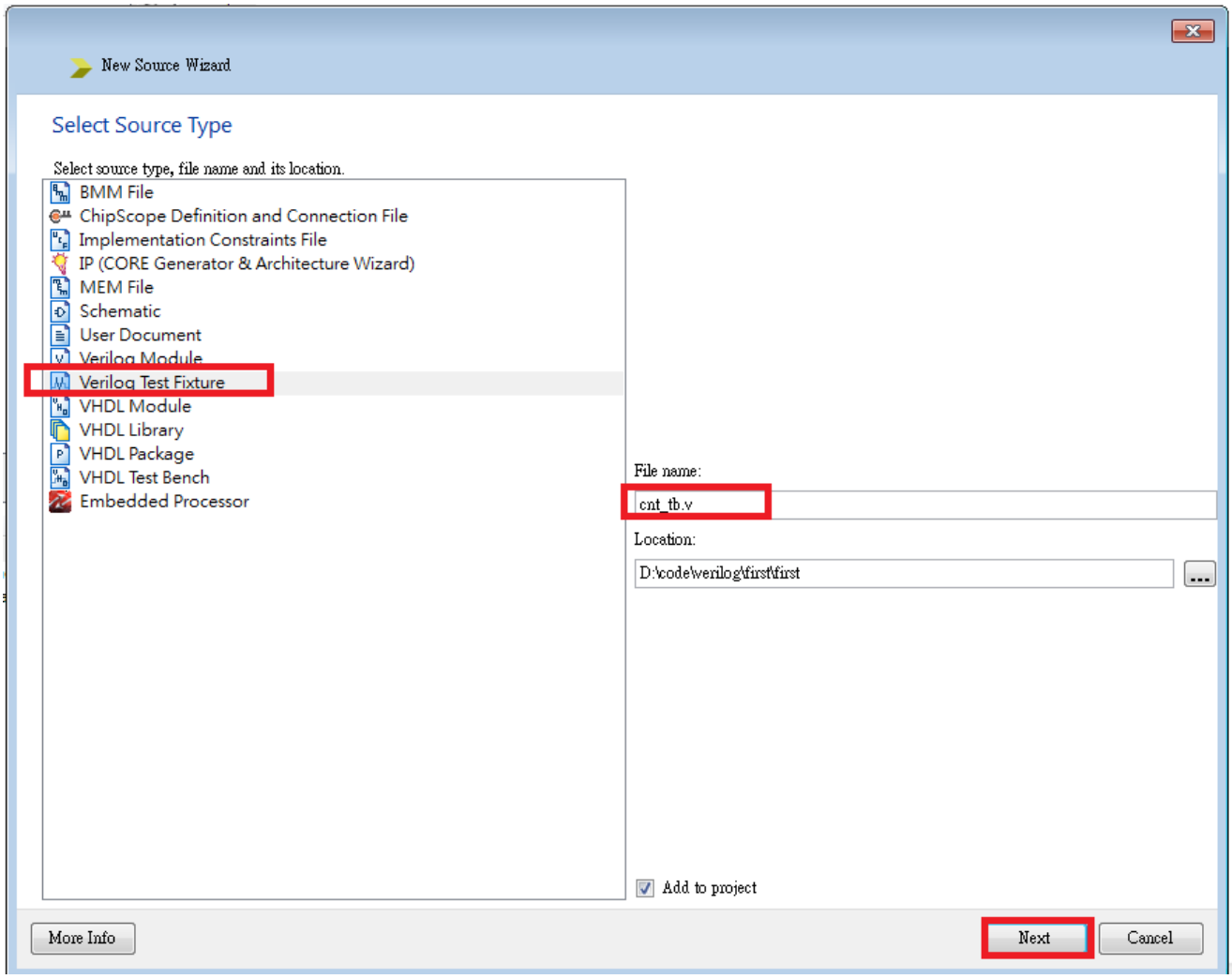


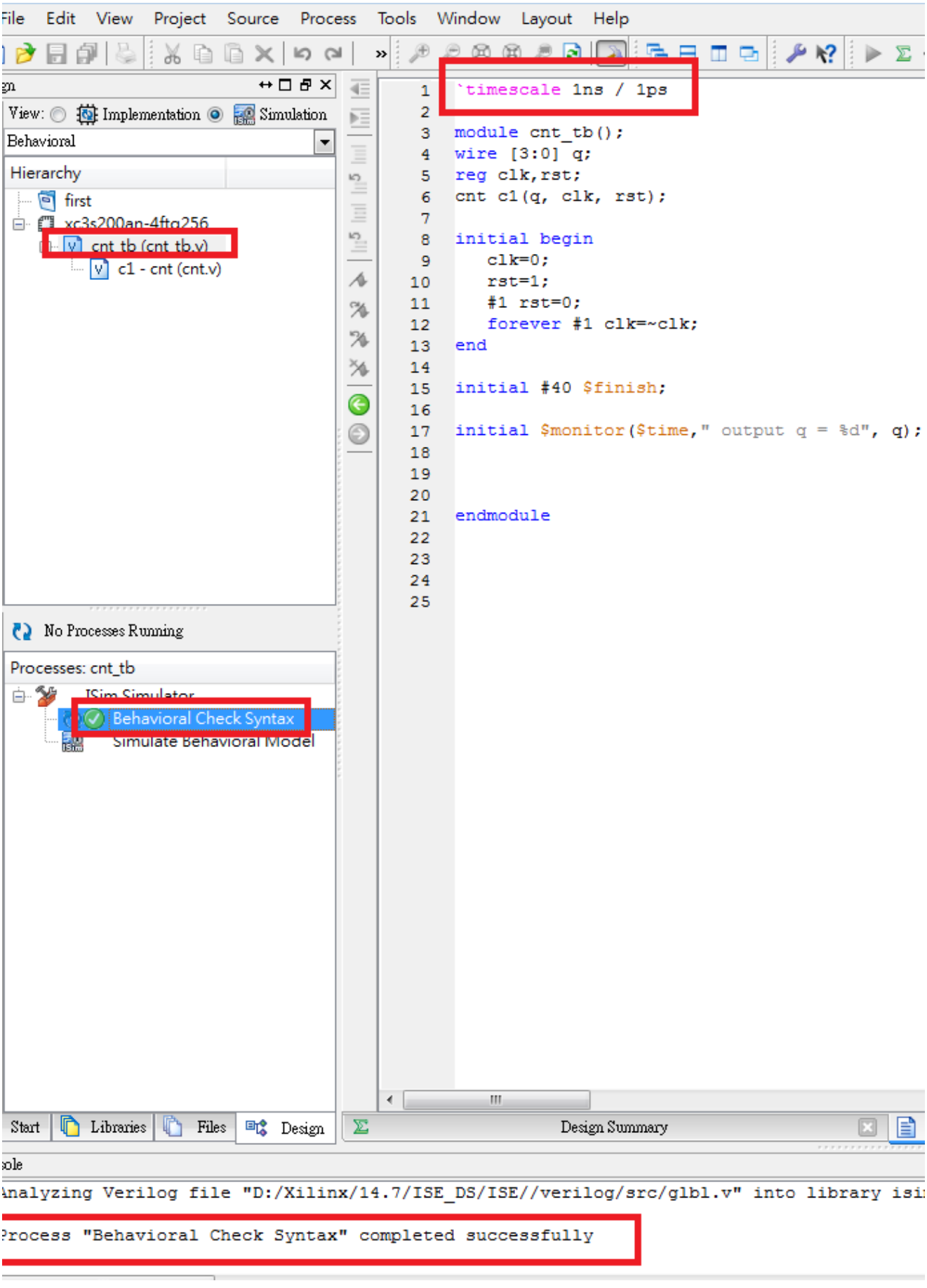




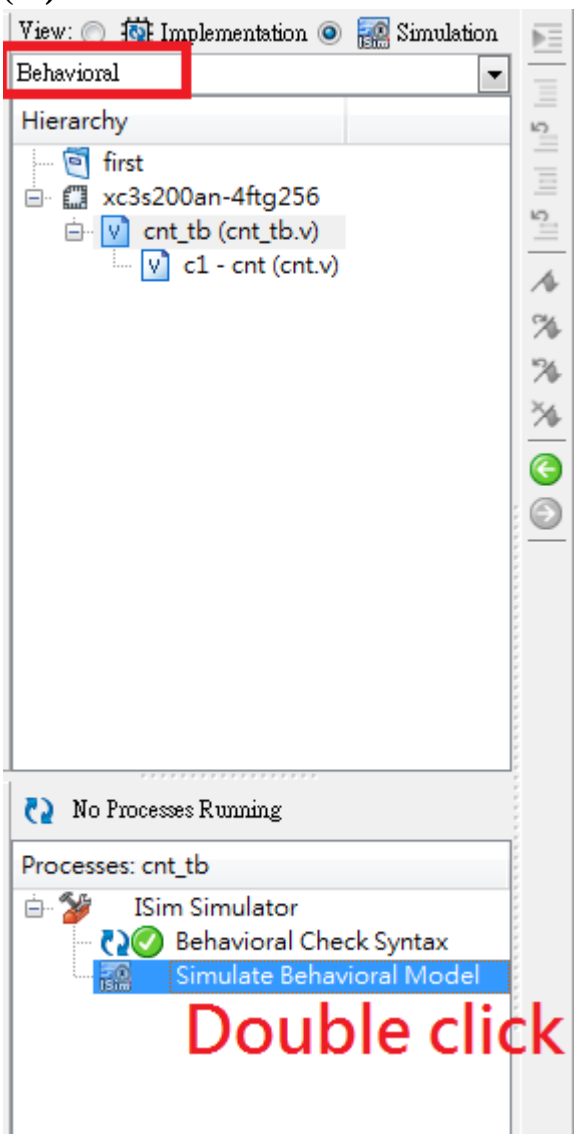
(12)Create New Test Fixture: 新增測試程式擋。

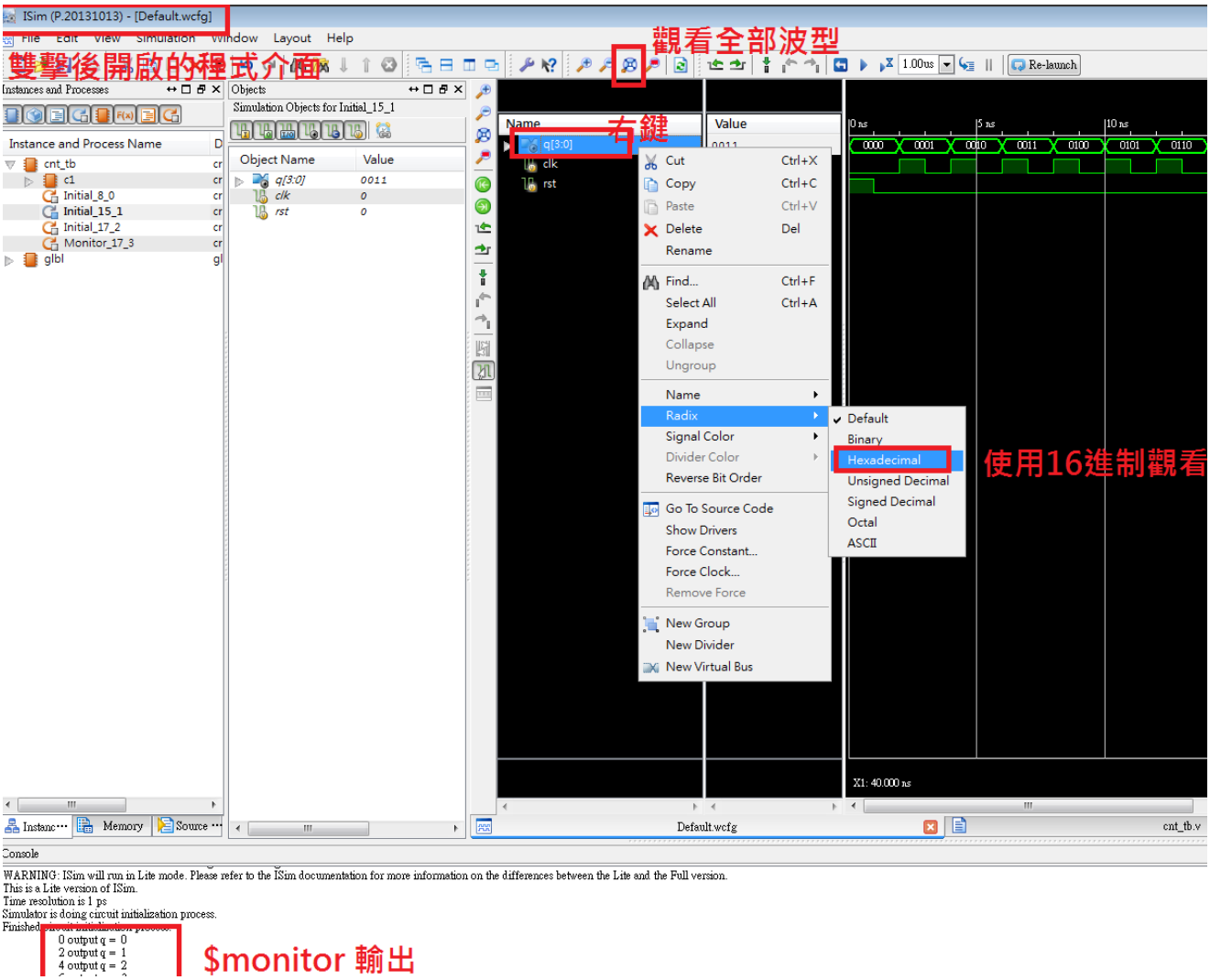



New Source Wizard
Select Source Type
Select source type, file name and its location.
BMM File
ChipScope Definition and Connection File
Implementation Constraints File
IP (CORE Generator & Architecture Wizard)
MEM File
Schematic
User Document
Verilog Module
Verilog Test Fixture
VHDL Module
VHDL Library
VHDL Package
VHDL Test Bench
Embedded Processor
File name:
cnt_tb.v
Location:
D:\code\verilog\first\first
Add to project
More Info
Next
Cancel


File Edit View Project Source Process Tools Window Layout Help
View: Implementation Simulation
Behavioral
Hierarchy
first
xc3s200an-4ftg256
cnt_tb (cnt_tb.v)
c1 - cnt (cnt.v)
No Processes Running
Processes: cnt_tb
ISim Simulator
Behavioral Check Syntax
Simulate Behavioral Model
Start
Libraries
Files
Design
Design Summary
`timescale 1ns / 1ps
module cnt_tb();
wire [3:0] q;
reg clk,rst;
cnt c1(q, clk, rst);
initial begin
clk=0;
rst=1;
#1 rst=0;
forever #1 clk=~clk;
end
initial #40 $finish;
initial $monitor($time," output q = %d", q);
endmodule
Analyzing Verilog file "D:/Xilinx/14.7/ISE_DS/ISE//verilog/src/glbl.v" into library isi
Process "Behavioral Check Syntax" completed successfully

(13) Test Bench Waveform Result：





Test Bench Waveform Result：