

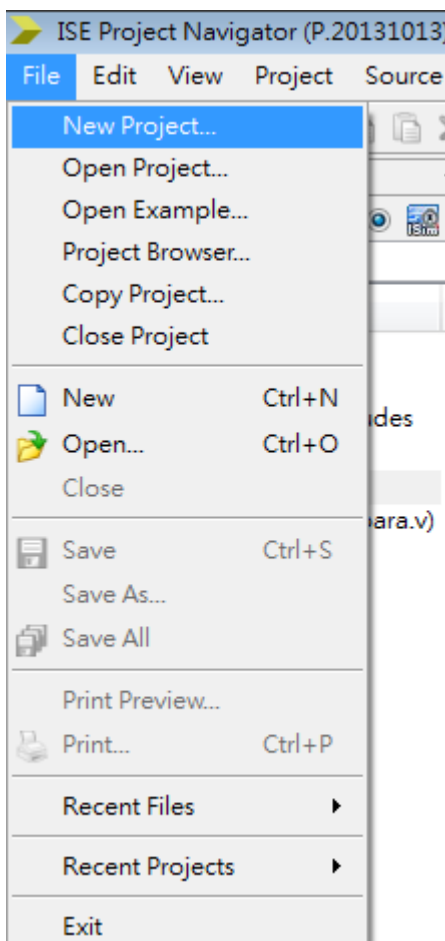
# Xilinx ISE 14.7 Training

## 1. 以 **Xilinx ISE** 做為驗證環境

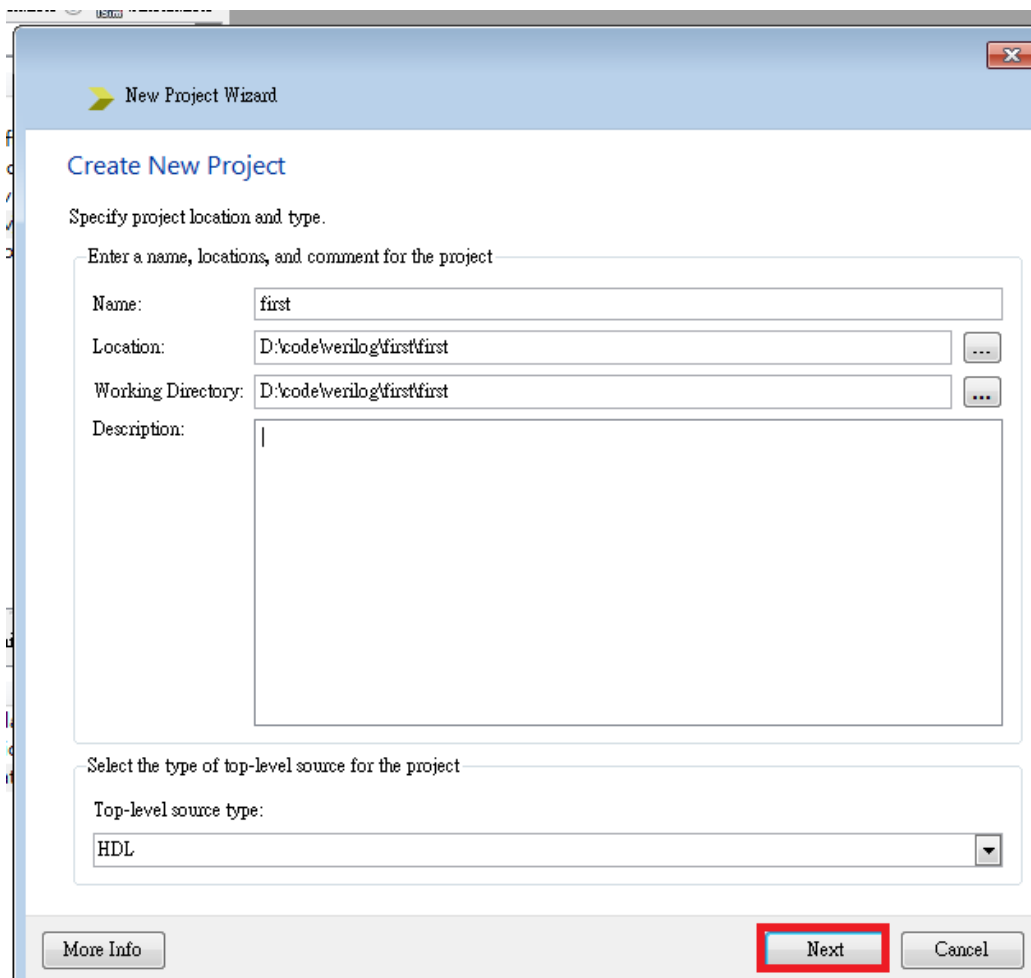
(配合 **cnt.v** , 及 **cnt\_tb.v** 為例)

### New project:

#### (1) File子New Project



## (2) Create New Project: Project Name, Project Location, Top-Level Source Type



The image shows a 'New Project Wizard' dialog box with a blue header bar containing a yellow arrow icon and the text 'New Project Wizard'. The main area is titled 'Create New Project' and contains the instruction 'Specify project location and type.' Below this, there are two sections. The first section, 'Enter a name, locations, and comment for the project', contains four fields: 'Name' with the value 'first', 'Location' with the value 'D:\code\verilog\first\first', 'Working Directory' with the value 'D:\code\verilog\first\first', and a large 'Description' text area. The second section, 'Select the type of top-level source for the project', contains a 'Top-level source type' dropdown menu with 'HDL' selected. At the bottom, there are three buttons: 'More Info', 'Next' (highlighted with a red rectangle), and 'Cancel'.

New Project Wizard

### Create New Project

Specify project location and type.

Enter a name, locations, and comment for the project

Name: first

Location: D:\code\verilog\first\first

Working Directory: D:\code\verilog\first\first

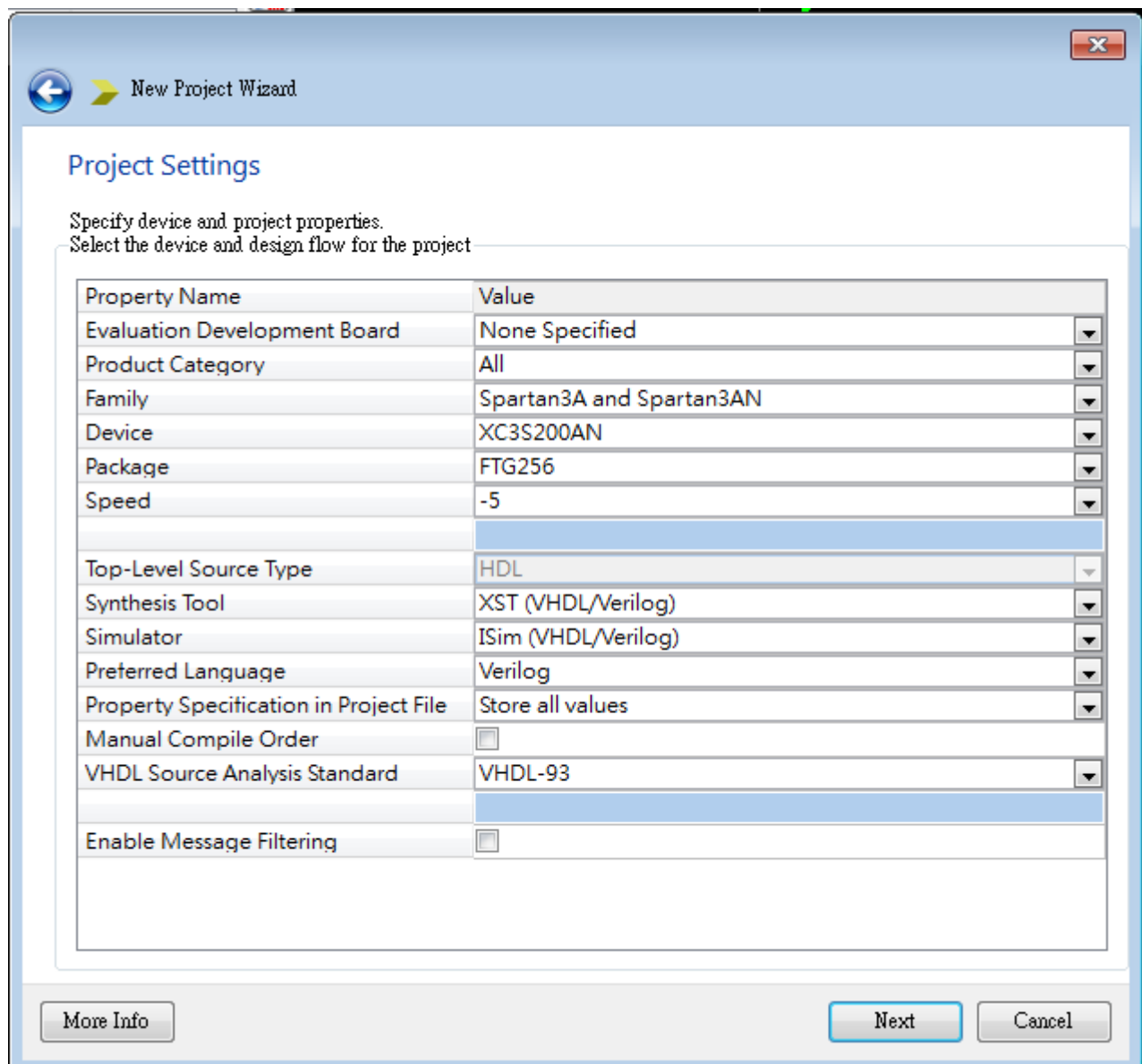
Description:

Select the type of top-level source for the project

Top-level source type: HDL

More Info Next Cancel

(3) **Device Properties:** Family, Device, Package, Speed 子看 FPGA board 上的 chip



The image shows the 'New Project Wizard' dialog box, specifically the 'Project Settings' step. The window has a title bar with a back arrow, a yellow arrow pointing right, and the text 'New Project Wizard'. The main area is titled 'Project Settings' and contains the instruction: 'Specify device and project properties. Select the device and design flow for the project'. Below this is a table with two columns: 'Property Name' and 'Value'. The table lists various project settings, including device information (Evaluation Development Board, Product Category, Family, Device, Package, Speed) and design flow settings (Top-Level Source Type, Synthesis Tool, Simulator, Preferred Language, Property Specification in Project File, Manual Compile Order, VHDL Source Analysis Standard, and Enable Message Filtering). At the bottom of the dialog are three buttons: 'More Info', 'Next', and 'Cancel'.

Property Name	Value
Evaluation Development Board	None Specified
Product Category	All
Family	Spartan3A and Spartan3AN
Device	XC3S200AN
Package	FTG256
Speed	-5
Top-Level Source Type	HDL
Synthesis Tool	XST (VHDL/Verilog)
Simulator	ISim (VHDL/Verilog)
Preferred Language	Verilog
Property Specification in Project File	Store all values
Manual Compile Order	<input type="checkbox"/>
VHDL Source Analysis Standard	VHDL-93
Enable Message Filtering	<input type="checkbox"/>



New Project Wizard



## Project Summary

Project Navigator will create a new project with the following specifications.

### Project:

Project Name: first  
Project Path: D:\code\verilog\first\first  
Working Directory: D:\code\verilog\first\first  
Description:  
Top Level Source Type: HDL

### Device:

Device Family: Spartan3A and Spartan3AN  
Device: xc3s200an  
Package: ftg256  
Speed: -5

Top-Level Source Type: HDL  
Synthesis Tool: XST (VHDL/Verilog)  
Simulator: ISim (VHDL/Verilog)  
Preferred Language: Verilog  
Property Specification in Project File: Store all values  
Manual Compile Order: false  
VHDL Source Analysis Standard: VHDL-93

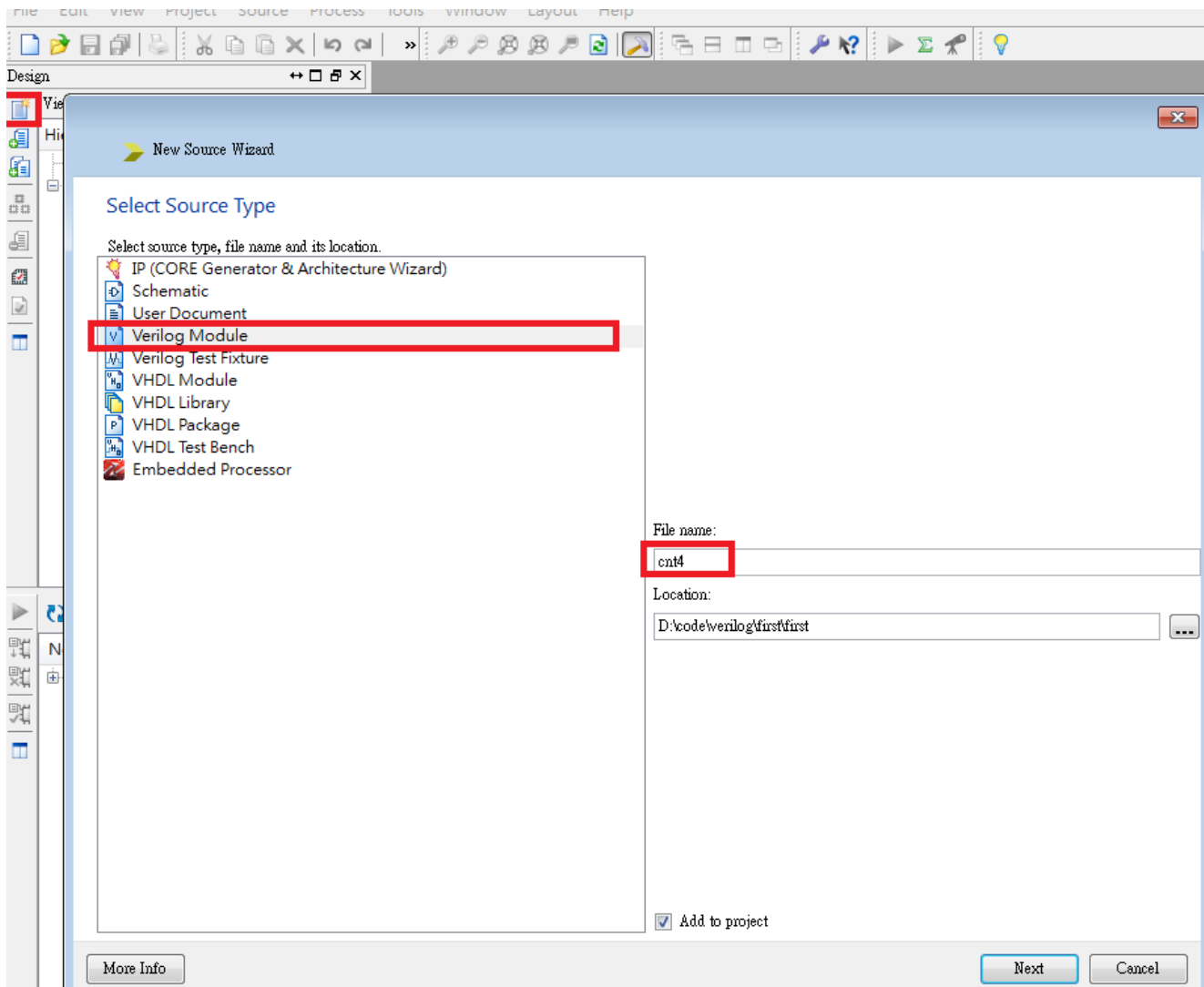
Message Filtering: disabled

More Info

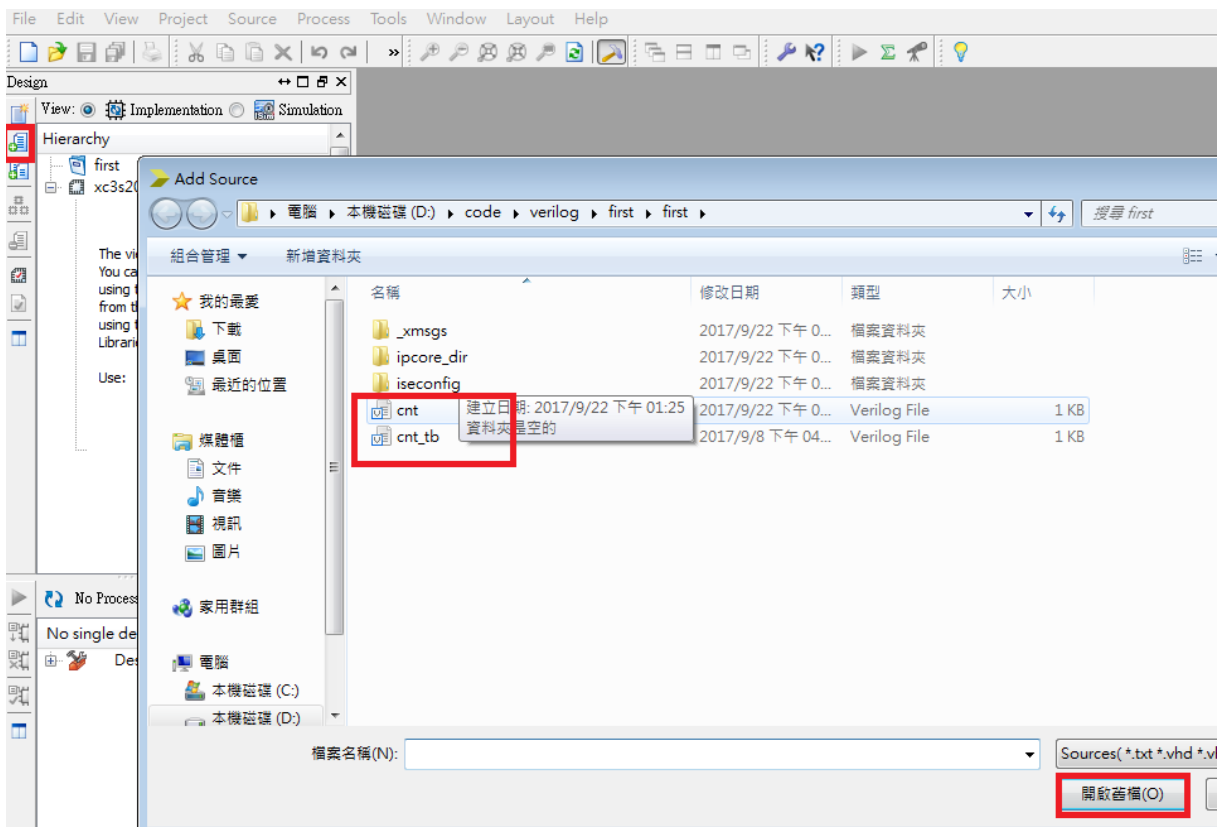
Finish

Cancel

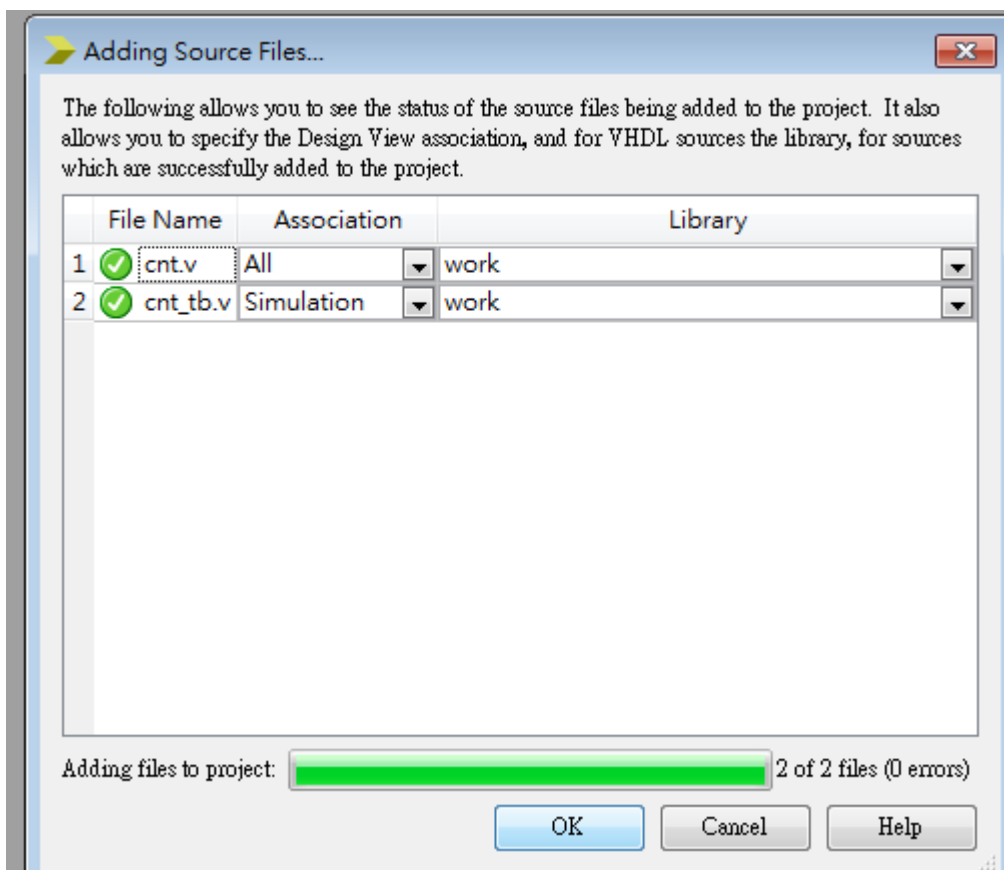
**(4) Create New Source:** 若需直接在 ISE 上寫程式，則使用此項。若程式已經寫好，則跳過此 選項。



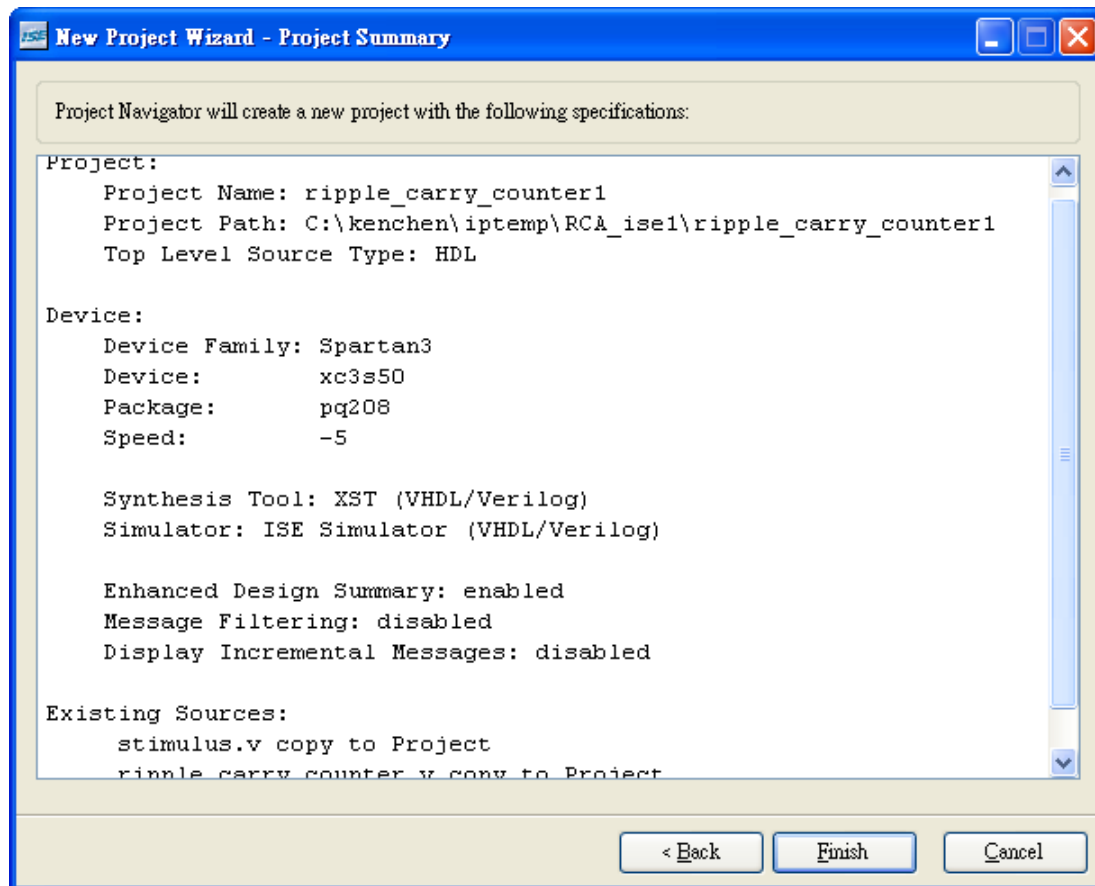
(5) Add Existing Sources: 選取 cnt4.v 及 cnt\_tb.v(測試檔)



兩隻程式已經被加入:

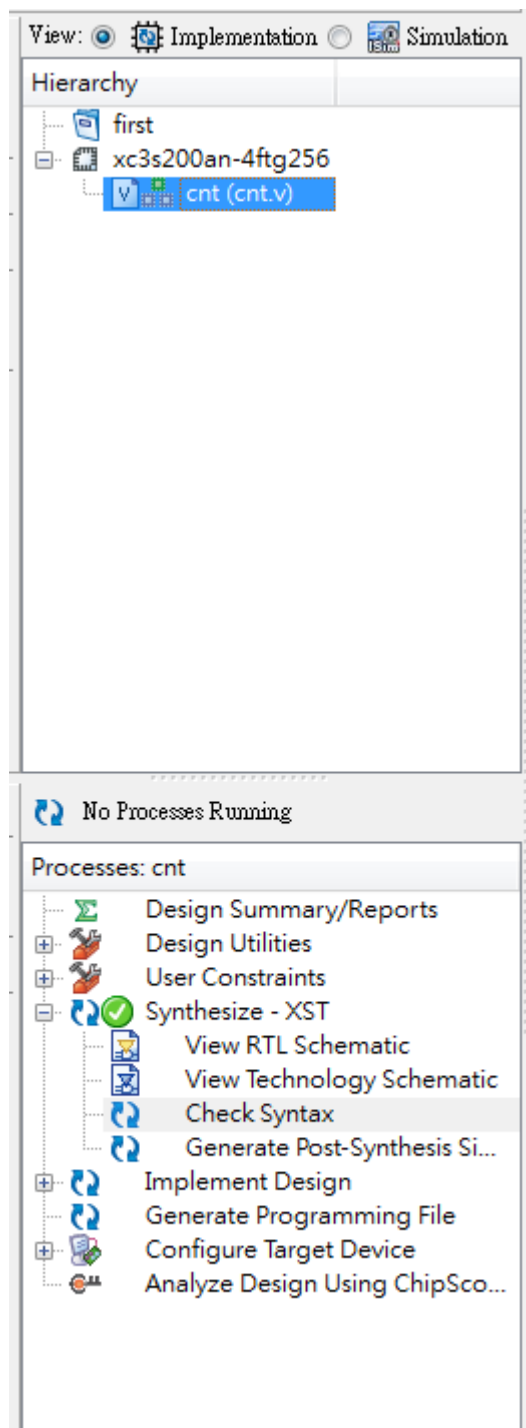


## (6) Project Summary:



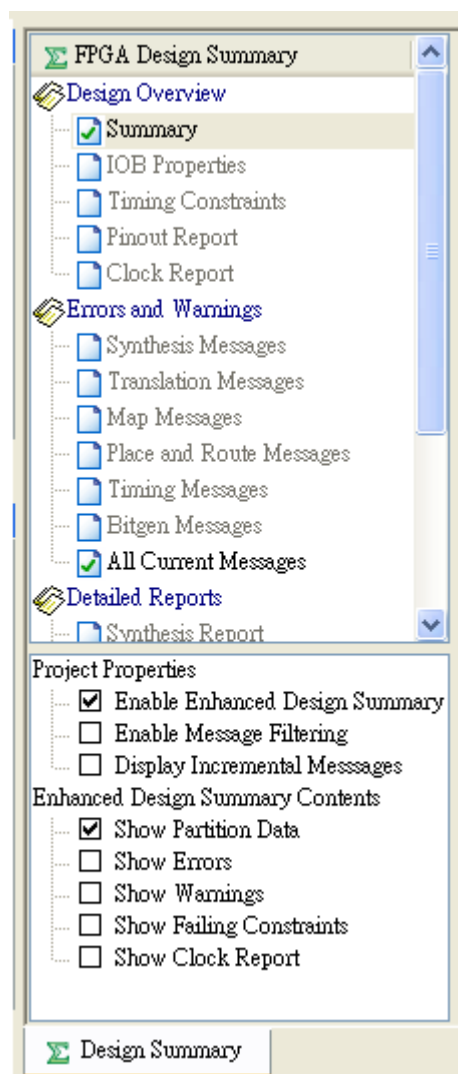
(7) 主畫面:

**Sources, Processes:**





## FPGA Design Summary:



# Report: 基本報告

## Libraries:

cnt Project Status (09/22/2017 - 14:14:29)					
<b>Project File:</b>	first.xise	<b>Parser Errors:</b>	No Errors		
<b>Module Name:</b>	cnt	<b>Implementation State:</b>	Synthesized		
<b>Target Device:</b>	xc3s200an-4ftg256	<b>• Errors:</b>	No Errors		
<b>Product Version:</b>	ISE 14.7	<b>• Warnings:</b>	No Warnings		
<b>Design Goal:</b>	Balanced	<b>• Routing Results:</b>			
<b>Design Strategy:</b>	<a href="#">Xilinx Default (unlocked)</a>	<b>• Timing Constraints:</b>			
<b>Environment:</b>	<a href="#">System Settings</a>	<b>• Final Timing Score:</b>			

Device Utilization Summary (estimated values)				
Logic Utilization	Used	Available	Utilization	
Number of Slices	2	1792	0%	
Number of Slice Flip Flops	4	3584	0%	
Number of 4 input LUTs	4	3584	0%	
Number of bonded IOBs	6	195	3%	
Number of GCLKs	1	24	4%	

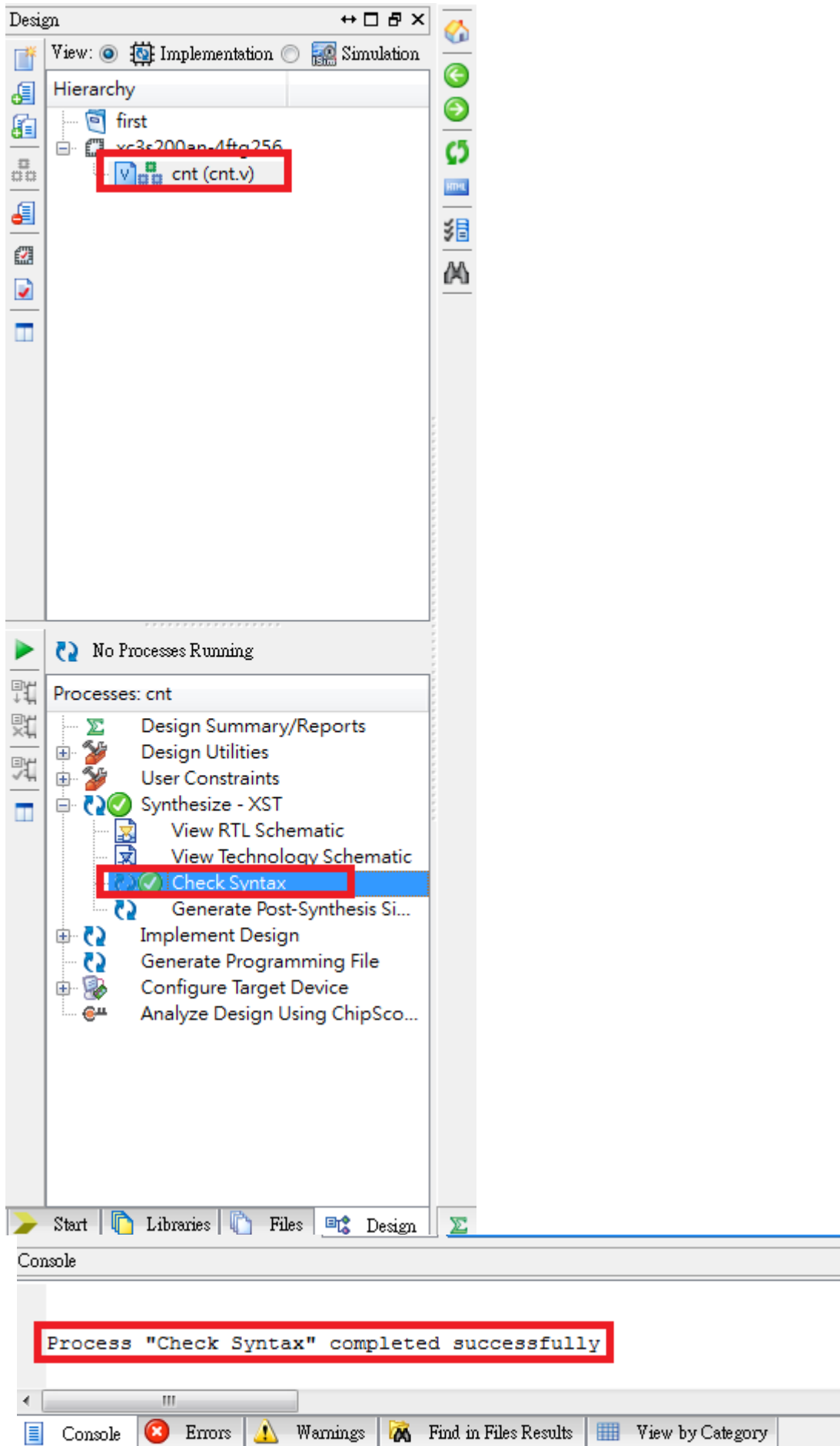
Detailed Reports						
Report Name	Status	Generated	Errors	Warnings	Infos	
<a href="#">Synthesis Report</a>	Current	週五 九月 22 14:14:28 2017	0	0	0	
Translation Report						
Map Report						
Place and Route Report						
Power Report						
Post-PAE Static Timing Report						
Bitgen Report						

Secondary Reports			
Report Name	Status	Generated	

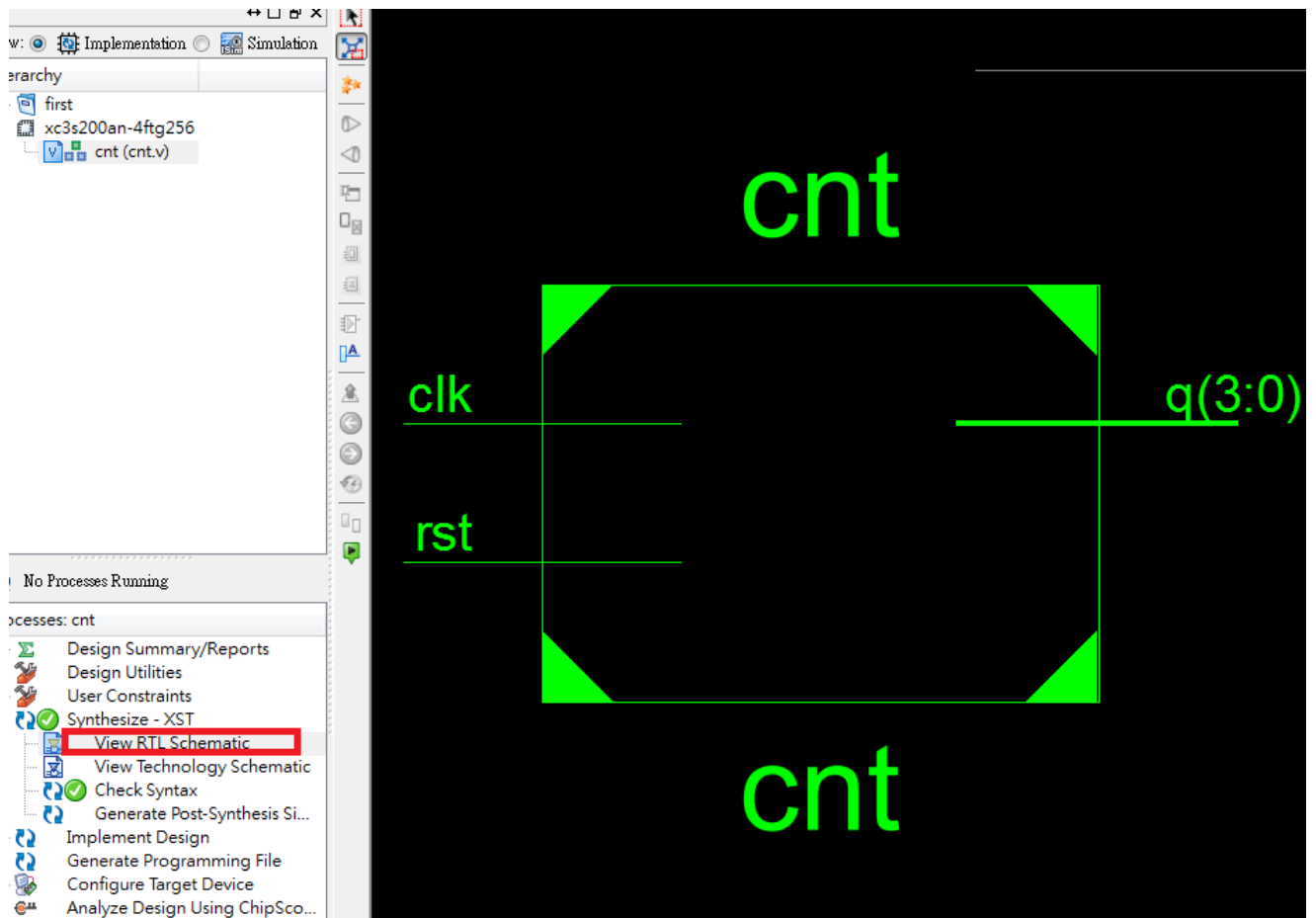
Source Libraries		
	work	
	cnt.v	
	cnt_tb.v	

(8)Check Syntax: 檢查 code 的語法是否有錯



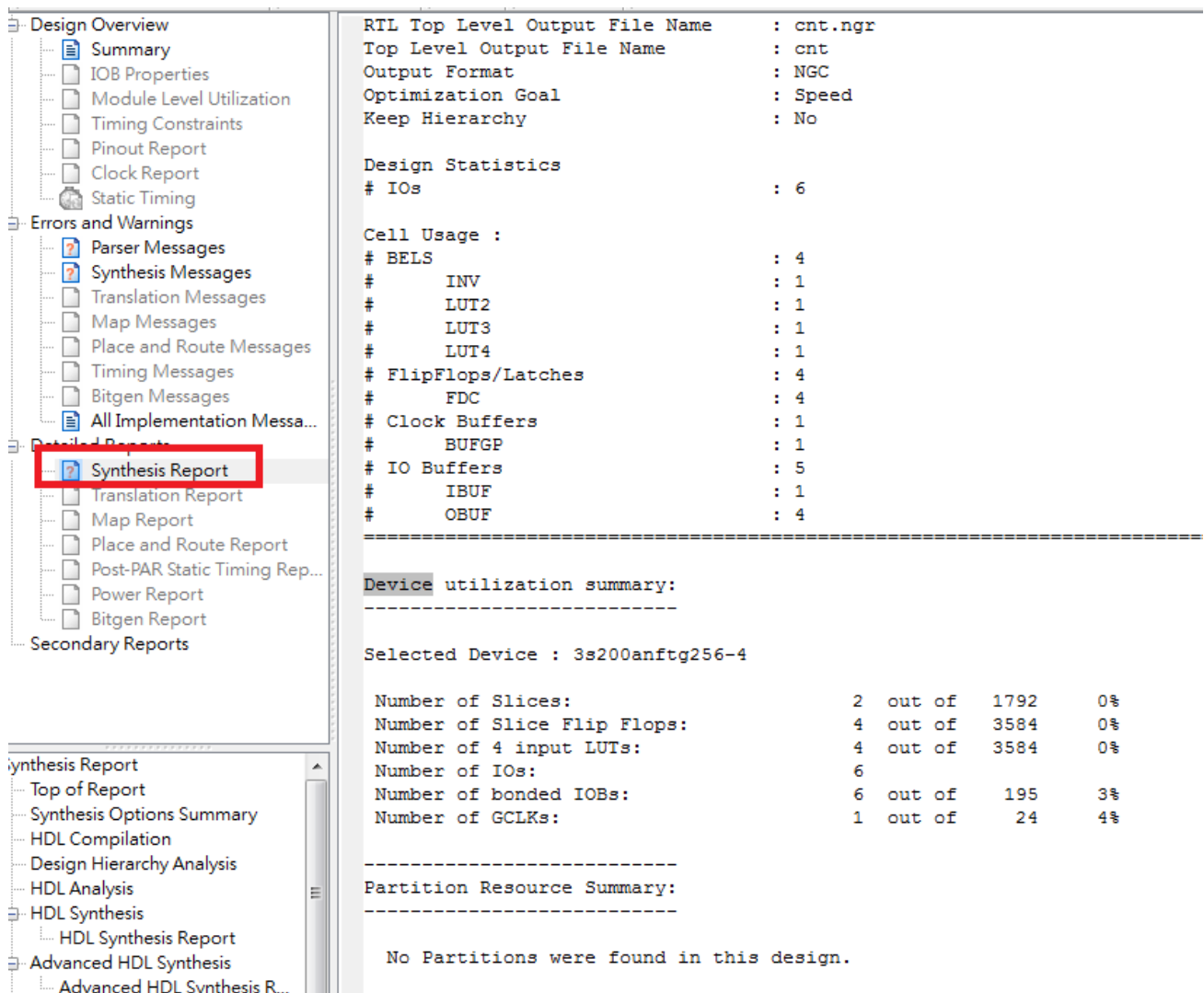
(9) **View RTL Schematic: RTL code** 的裴構圖

Sources子 Design: 內合主程式構成之 modules



## (10) View Synthesis Report: 合成結果

**Device utilization summary:** 使用 device 的資源有多少



The screenshot shows a software interface with a left-hand tree view and a right-hand content area. In the tree view, the 'Synthesis Report' is selected and highlighted with a red rectangle. The content area displays the following information:

```
RTL Top Level Output File Name : cnt.ngr
Top Level Output File Name : cnt
Output Format : NGC
Optimization Goal : Speed
Keep Hierarchy : No

Design Statistics
# IOs : 6

Cell Usage :
# BELS : 4
# INV : 1
# LUT2 : 1
# LUT3 : 1
# LUT4 : 1
# FlipFlops/Latches : 4
# FDC : 4
# Clock Buffers : 1
# BUFGP : 1
# IO Buffers : 5
# IBUF : 1
# OBUF : 4
```

---

**Device utilization summary:**

---

Selected Device : 3s200anftg256-4

Number of Slices:	2	out of	1792	0%
Number of Slice Flip Flops:	4	out of	3584	0%
Number of 4 input LUTs:	4	out of	3584	0%
Number of IOs:	6			
Number of bonded IOBs:	6	out of	195	3%
Number of GCLKs:	1	out of	24	4%

---

**Partition Resource Summary:**

---

No Partitions were found in this design.

**Timing Summary:** 最快頻率可以到多少

Timing Summary:

Speed Grade: -4

Minimum period: 2.544ns (Maximum Frequency: 393.082MHz)  
Minimum input arrival time before clock: No path found  
Maximum output required time after clock: 5.744ns  
Maximum combinational path delay: No path found

Timing Detail:

All values displayed in nanoseconds (ns)

最長路徑:

```
=====
Timing constraint: Default OFFSET OUT AFTER for Clock 'clk'
  Total number of paths / destination ports: 4 / 4
=====
Offset:                5.744ns (Levels of Logic = 1)
Source:                q_0 (FF)
Destination:          q<0> (PAD)
Source Clock:          clk rising

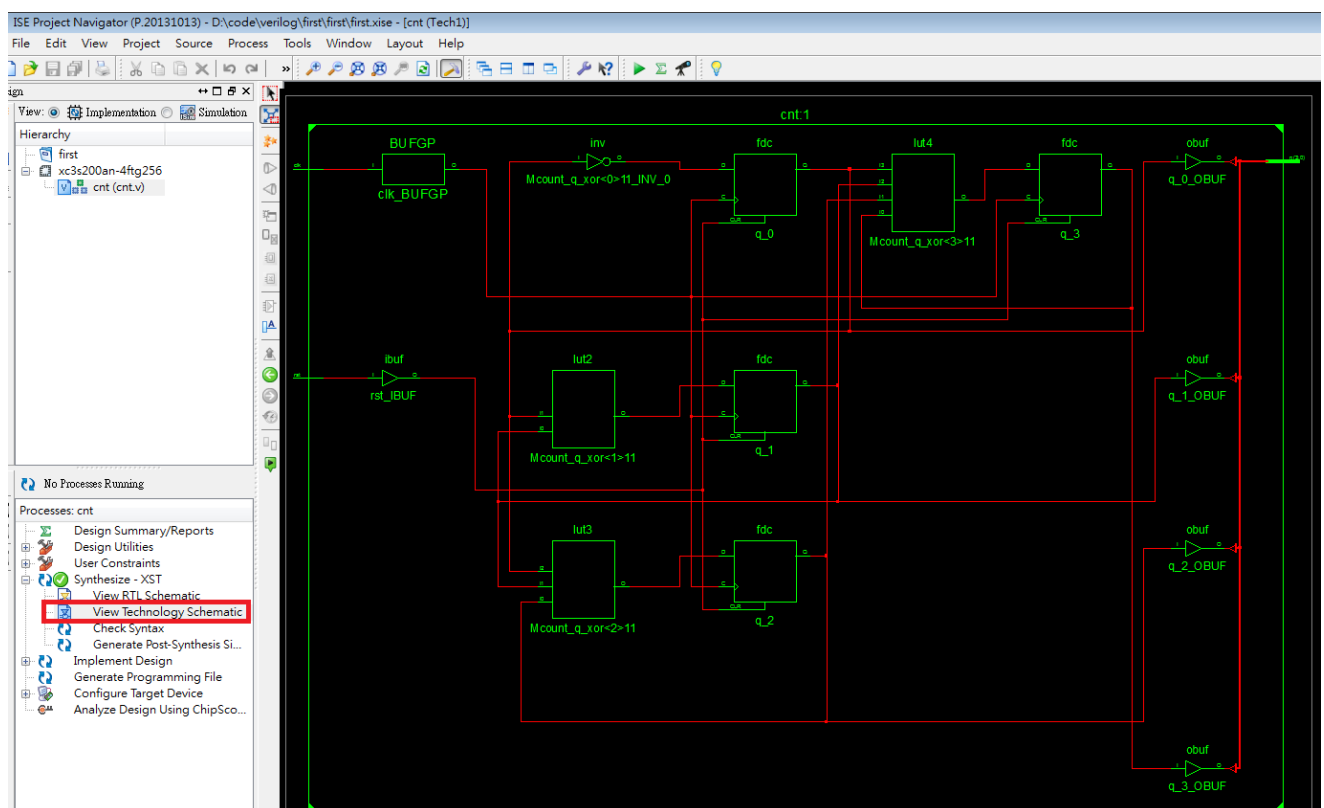
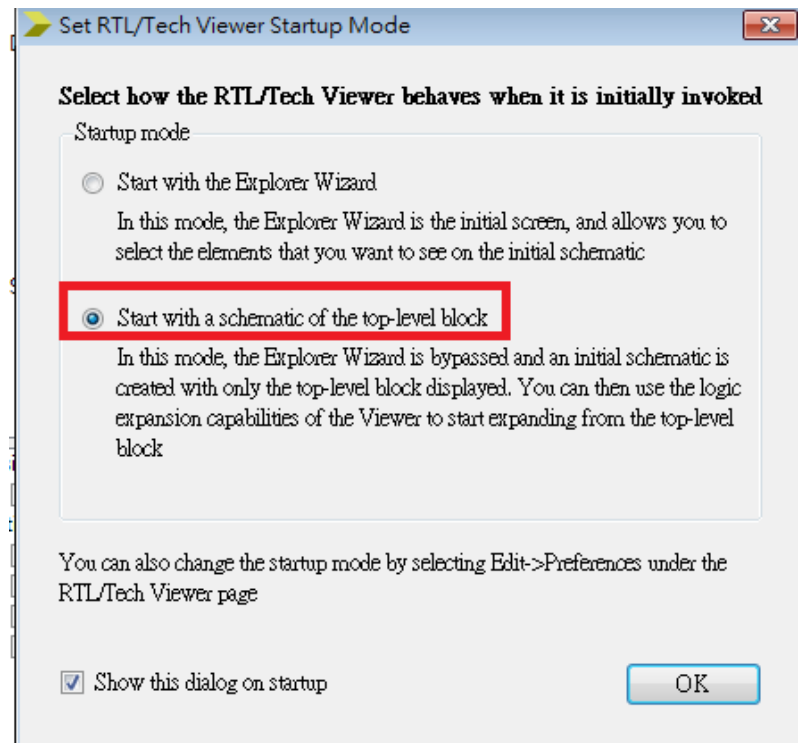
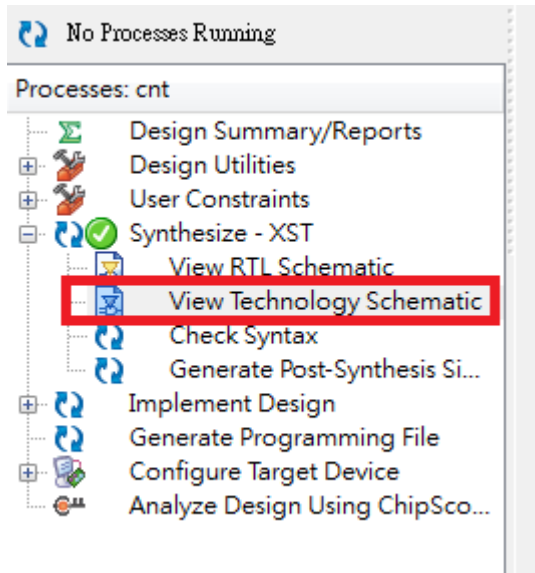
Data Path: q_0 to q<0>

   Cell:in->out      fanout   Gate      Net
                        Delay    Delay    Logical Name (Net Name)
-----
   FDC:C->Q           5        0.591    0.633    q_0 (q_0)
   OBUF:I->O           4.520          q_0_OBUF (q<0>)
-----
Total                5.744ns (5.111ns logic, 0.633ns route)
                        (89.0% logic, 11.0% route)
=====

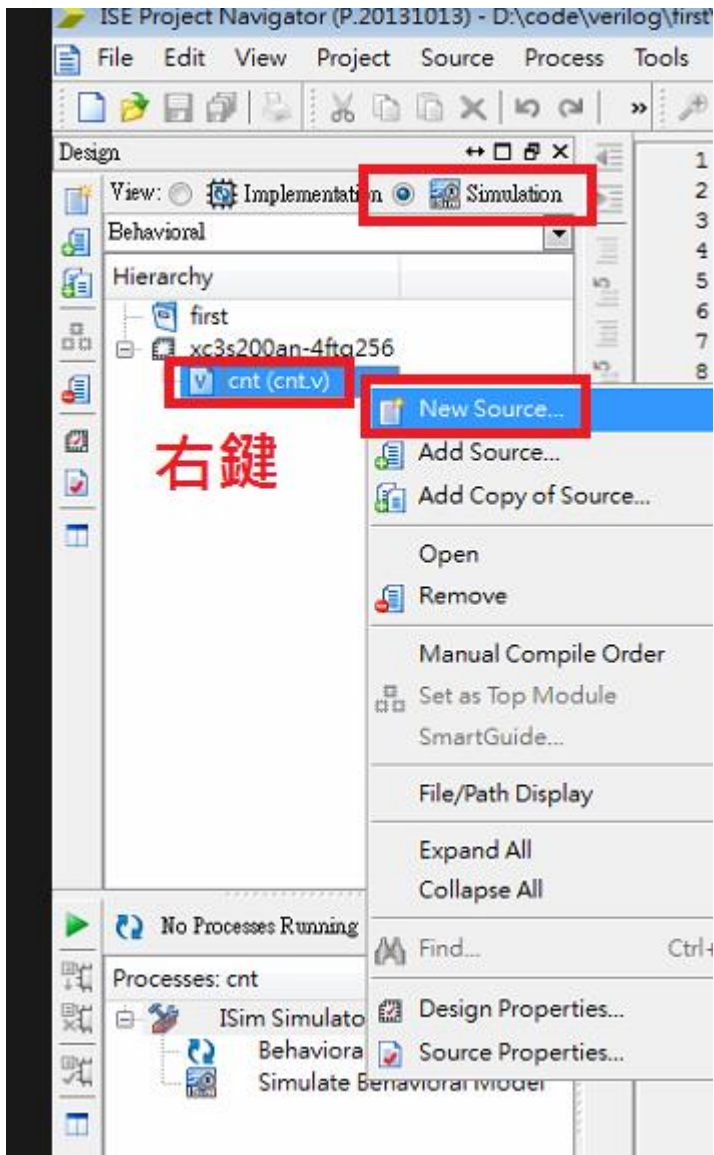
Total REAL time to Xst completion: 5.00 secs
Total CPU time to Xst completion: 5.10 secs

-->
```

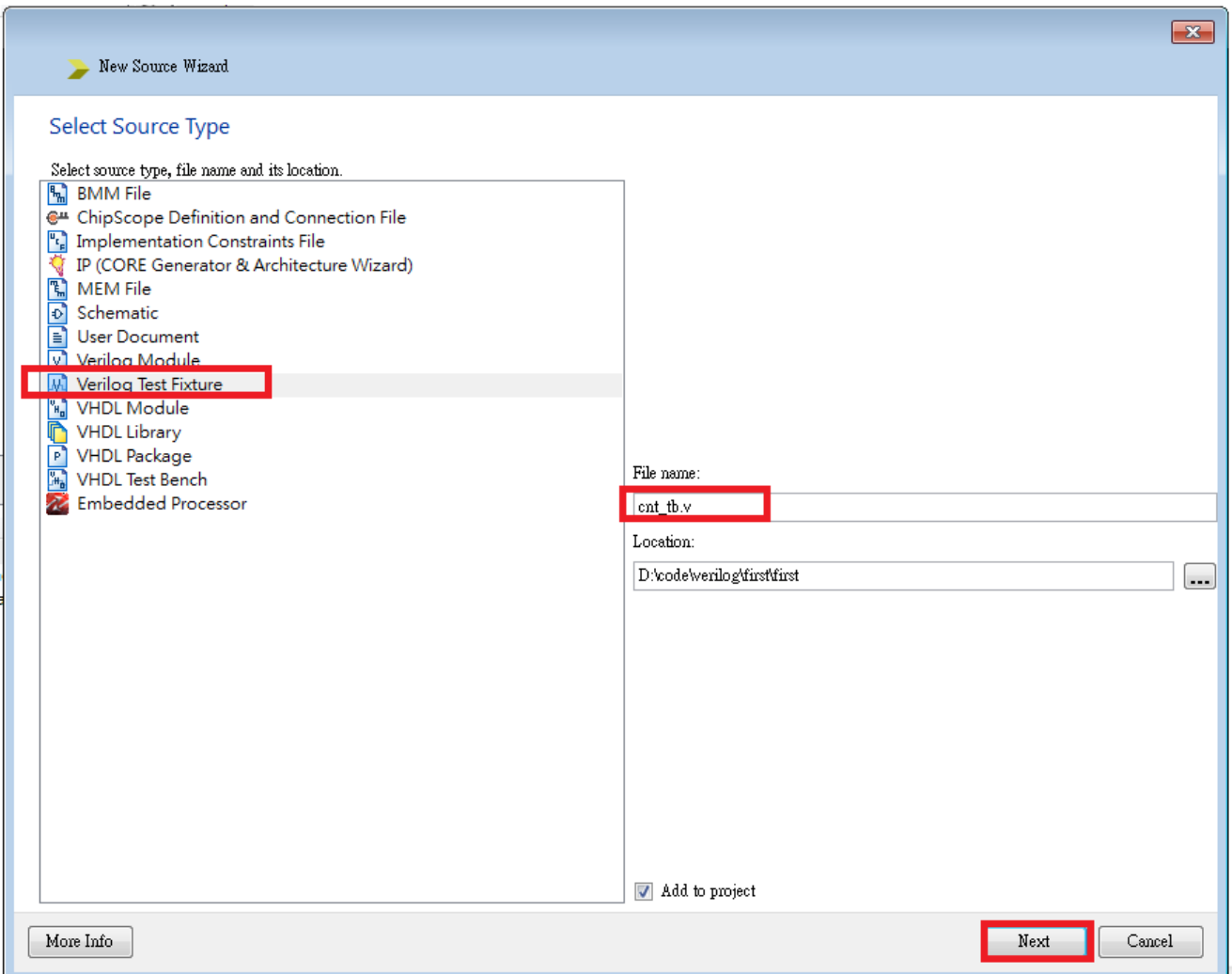
**(11) Processes子 View Technology Schematic: 經合成後的電路圖**



(12)Create New Test Fixture: 新增測試程式檔。







File Edit View Project Source Process Tools Window Layout Help

View: Implementation Simulation

Behavioral

Hierarchy

- first
  - xc3s200an-4ftg256
    - cnt\_tb (cnt\_tb.v)
    - c1 - cnt (cnt.v)

No Processes Running

Processes: cnt\_tb

- ISim Simulator
  - Behavioral Check Syntax
  - Simulate Behavioral Model

```
1 `timescale 1ns / 1ps
2
3 module cnt_tb();
4 wire [3:0] q;
5 reg clk,rst;
6 cnt c1(q, clk, rst);
7
8 initial begin
9     clk=0;
10    rst=1;
11    #1 rst=0;
12    forever #1 clk=~clk;
13 end
14
15 initial #40 $finish;
16
17 initial $monitor($time," output q = %d", q);
18
19
20
21 endmodule
22
23
24
25
```

Start Libraries Files Design

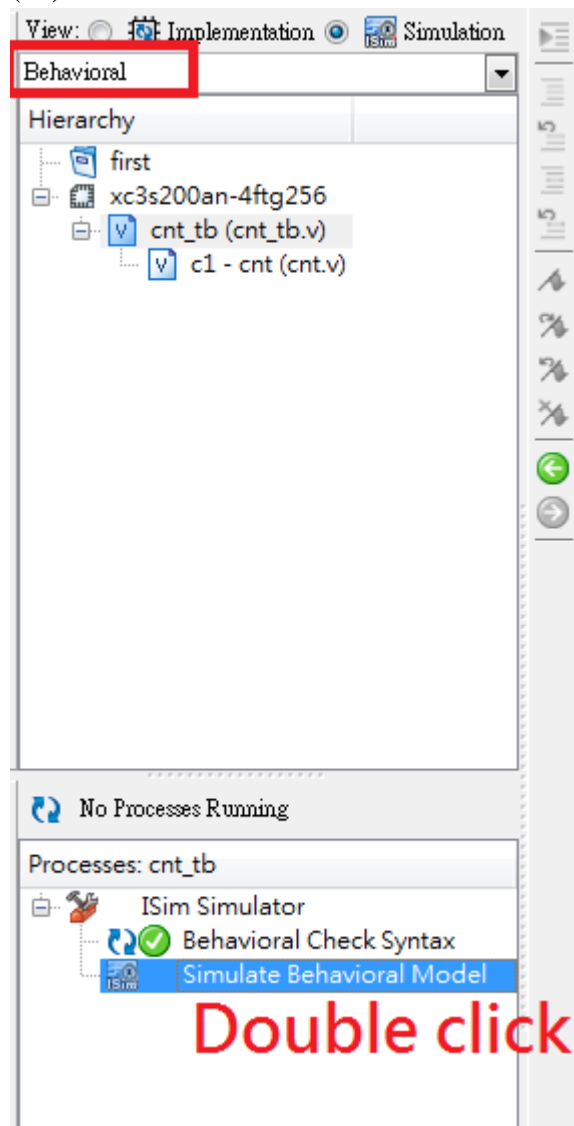
Design Summary

sole

Analyzing Verilog file "D:/Xilinx/14.7/ISE\_DS/ISE//verilog/src/glbl.v" into library isi

Process "Behavioral Check Syntax" completed successfully

(13)Test Bench Waveform Result :



ISim (P.20131013) - [Default.wcfg]

File Edit View Simulation Window Layout Help

雙擊後開啟的程式介面

觀看全部波型

右鍵

使用16進制觀看

Simulation Objects for Initial\_15\_1

Object Name	Value
q[3:0]	0011
clk	0
rst	0

Instance and Process Name

- cnt\_tb
- Initial\_8\_0
- Initial\_15\_1
- Initial\_17\_2
- Monitor\_17\_3
- glbl

Console

WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.  
This is a Lite version of ISim.  
Time resolution is 1 ps  
Simulator is doing circuit initialization process.  
Finished circuit initialization process.

0 output q = 0  
2 output q = 1  
4 output q = 2

\$monitor 輸出

Test Bench Waveform Result :

