Curriculum Vitae *last updated: 7/25/2022*

SURYA TEJA PARUCHURI

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EDUCATION

Johns Hopkins University, Baltimore, MD.
Graduate Certificate in Electrical and Computer Engineering GPA: 3.90/4.0 *Expected* May 2023
Coursework: Compressive Sensing and Sparse Recovery (A), Estimation and Detection Theory (A-), Advanced Digital Signal Processing (A+).

University of Maryland, College Park, MD.
Master of Science in Telecommunications GPA: 3.83/4.0 May 2017
*Scholarly Paper: "*Spectrum Efficiency: Using Full Duplex Techniques and Cognitive Radios."
Honors: Awarded Academic Excellence Scholarship, Nominated for Distinguished Student Award.

Vellore Institute of Technology, Vellore, India.
Bachelor of Technology in Electronics and Communication Engineering GPA: 8.35/10 May 2014
Senior Design Project: Radar Target Simulator.

CONTINUING EDUCATION

University of California, Irvine - Division of Continuing Education.
- FPGA Design Fundamentals (A+).
- Real Time Embedded Digital Signal Processing (A-).

RESEARCH INTERESTS

- Signal Processing and Communications.
- Applied Mathematics.
- Computer Engineering.

PUBLICATIONS

- E. E. Tsiropoulou, A. Thanou, **S.T. Paruchuri**, and S. Papavassiliou, "Self-organizing Museum Visitor Communities: A Participatory Action Research based Approach", *12th International Workshop on Semantic and Social Media Adaptation and Personalization (SMAP 2017)*, Bratislava, Slovakia, July, 2017.

- E.E.Tsiropoulou, S.T. Paruchuri and J.S. Baras, "Interest, Energy and Physical-Aware Coalitions Formation and Resource Allocation in Smart IoT Applications", *51st Conference on Information Sciences and Systems (CISS 2017),* Johns Hopkins University, Baltimore, MD, 2017.

- H. Dagale, S. V. R. Anand, M. Hegde, N. Purohit, M. K. Supreeth, G. S. Gill, V. Ramya, A. Shastry, S. Narasimman, Y. S. Lohith, and P. Surya, " CyPhyS+: A Reliable and Managed Cyber-Physical System for Old-Age Home Healthcare over a 6LoWPAN Using Wearable Motes, " in *2015 IEEE International Conference on Services Computing (SCC)*, 2015, pp. 309 - 316.

WORK EXPERIENCE

Senior System Design Engineer, NXP Inc Irvine CA — May 2022 – Present

- Design and Implement various modules for UWB Modem Design in MATLAB, C++, SystemC, Python and Simulink.

Engineer, Qualcomm Technologies Inc Boxborough MA — August 2020 – May 2022

- Designed and implemented Denali's (X65 Modem) bit-exact firmware for 5G NR W1 and W2 pre-coder selection modules on SILVER (Strongly Integrated Long Vector Extensions for Radio) accelerator in assembly, C and Python using SIMD, VLIW, modem specific composite instructions, hardware loops, and Out-of-Order (OOO) execution.
- Designed and implemented Denali (X65 Modem) EnTV's MRC (Maximal Ratio Combiner), demodulation (LUT based QPSK, 16-QAM & 64 QAM slicer) and various linear algebra modules such as 4D matrix multiplication etc., on SILVER (Strongly Integrated Long Vector Extensions for Radio) accelerator in assembly, C and Python using SIMD, VLIW, modem specific composite instructions, hardware loops, and Out-of-Order (OOO) execution.
- Designed & implemented RxFFT Circular FIFO buffer in firmware and it's API for 5G NR in C targeting IU, PDMEM (UMEM in Cayenne Modem) and task queues.
- Implemented FW logging modules for NR CSF firmware for easy debugging by Systems and Test Engineers.
- Contributed in firmware design & code reviews, train new employees, firmware design documentation etc.

Senior Engineer, Spirent Communications Inc Eatontown NJ — January – July 2020

- Implemented a multi-threaded dynamic rate convertor library (polyphase decimator & interpolators DSP blocks, thread manger, data sourcer, and sink) in C++ to resample large fading files (> 2 GB)
- Implemented closest interpolation rate searching algorithm within specified error specification in C++.
- Refactored Spirent's wireless channel models Intellectual Property library code written in MATLAB for modularity.

Embedded Engineer, Spirent Communications Inc Eatontown NJ — May 2018 – December 2019

- Improved Lognormal fading DSP firmware performance on TMS320C6678 by x3.84 (389,000 to 101,000 cycles) using processor intrinsics, reducing loop carried bound and software pipelining (out of order assembly execution).
- Designed, implemented and delivered 3GPP High Speed Train Channel model DSP firmware on TMS320C6678.
- Designed Vertex's dynamic rate-conversion sub-system to support arbitrary scaling of fading Doppler signals to an accuracy of 0.1 Hz using multi-rate filter banks in MATLAB. (Implementation in C++ is in progress).
- Lead a team of 2 Software Developers to deliver 2 major releases of Spirent's Live2Lab product – for 5G NR.
- Implemented new processing engine's routines for 5G NR Over-The-Air Testing of MIMO gNodeB in C#.
- Translated product manager's requirements to design specifications, project timeline, Test cases, and finally Product Documentation.
- Accelerated DSP firmware and Live2Lab build generation by setting Continuous Integration system using Ant Build, Jenkins and Perforce.
- Supported DSP command parsing performance improvement by bringing Core 7 on TMS320c6678 using sysBIOS.
- Accelerated delivery of Vertex's 4.50, 4.60 and 4.70 release by verifying statistical properties of fading Signal.

- Integrated dynamic phase shift and bulk delay firmware with software to generate frequency selective fading.

Wireless Engineering Intern, Skylark Wireless LLC. Houston TX November 2017 – May 2018

- Improved Iris's SFDR by 28.571% (9.52 dBc) by implementing self-calibration firmware to mitigate LO Feed Through, DC Offset and IQ impairments of LMS7002M --2X2 MIMO RFIC, using Python SWIG, SoapySDR and C++.
- Implemented a DOCSIS 3.1 to UHF Band Upstream Up conversion using LMS7002EVB and demoed to a client.
- Assisted in Iris software defined radio (SDR) Rx Sensitivity tests by setting up synchronized Iris SDR test-setup.
- Performed Quality Assurance-power sequence tests on 112 Iris-SDRs to characterize inrush current on Iris SDRs.
- Made a Rasberrypi image to remotely power cycle Base Station power boxes (inaccessible after installation).
- Recommended Microsoft Air Band Grant Initiative to raise a capital of $75000 for the start-up.

Web Developer, Institute for Systems Research, University of Maryland June 2016 – May 2017

- Developed Professor's website to organize over 750+ research papers, numerous honors and awards, courses, research project details etc., using Drupal CMS framework on a remote server.
- The website currently serves as a central digital repository, and eliminated need to maintain different spreadsheets.

Engineering Intern, Defense R&D Organization, India January 2014 – May 2014

- Designed Radar Target Simulator (RTS) using Digital Radio Frequency Memory & real time signal processing algorithms for hardware in the loop testing of Active Antenna Array Unit (AAAU) & Primary Radar (PR).
- RTS significantly reduces testing costs through ground based testing compared to mid-air testing process.
- Assisted in testing of modulation module based on Error Vector Magnitude (EVM) enhanced subject knowledge.

Engineering Training, Electronics Corporation of Indian Limited (ECIL), India June 2013

- Mastered instrument calibrations process through hands-on training on calibration of electronic radioactive detectors using Cesium (Cs) and Potassium (K-40) isotope samples.

RESEARCH AND TEACHING EXPERIENCE

Voluntary Research Assistant, University of Maryland November 2016 – May 2017

- Assisted Institute for Systems Research post-doctoral candidate, by implementing and numerically verifying against analytical solutions a "resource allocation algorithms for Internet of Things" and a "coalition formation algorithms for self-organizing museum visitors", in MATLAB.
- Co-authored two conference paper presented at ***51st Conference on Information Sciences and Systems,*** Baltimore, Maryland, 2017 and ***The 12th International Workshop on Semantic and Social Media Adaptation and Personalization (SMAP 2017),*** Bratislava, Slovakia, July, 2017.

Teaching Assistant, University of Maryland September 2016 – May 2017

- Assisted instructor on teaching multiple sessions of junior level course on Operations Research, by resolving students' questions, grading weekly homework, term exams and organizing make-up exams.
- Mentoring enhanced my teaching and knowledge transfer skills.

Project Assistant, ECE, Indian Institute of Science, India June 2014 – May 2015

- Developed a Fuzzy Logic based medical diagnosis algorithm for "*6LowPAN based Cyber Physical System for remote health monitoring"* - to assess patient's health.
- Implemented a simple statistical signal processing algorithm for QRS detection in ECG and improved heart anomalies detection and reduced complexity significantly compared to Pan Tompkins and Wavelet based beat classification algorithms.
- Expedited deployment and field testing of Wireless Sensor Network (WSN) by accelerating the debugging process of the server side socket code to prevent data misinterpretation.

- Co-authored a conference paper presented at ***12th IEEE International Conference on Services Computing,*** New York, 2015, and presented the project during Indian Institute of Science's Open Day 2015.

ACHIEVEMENTS & AWARDS

- Selected for final round for Data Science Fellowship by The Data Incubator/Cornell Tech. (<2% selectivity across US), November 2017.
- Telecommunication's Academic Scholarship, for excellence in academics, February 2017.
- Nominated for Telecommunication's Distinguished Student Award, December 2016.

SKILLS

- *Programming languages:* MATLAB, C, C++, C#, SystemC, Python, Bash, Assembly, VHDL, Javascript.
- *Libraries:* PyQt5, numpy, scipy, pandas, algorithmic C
- *Architectures:* Texas Instrument's c66xx & c320x DSP, Qualcomm's Hexagon (Q6 DSP)
- *RTOS & Tools:* Xilinx Vivado, TI CCStudio, SysBIOS SysBIOS, C66xx Compiler & assembler, Hexagon compiler & assembler, GNU Radio.
- *Lab Equipment:* Spectrum Analyzers, Network Analyzers, O'scopes, Signal Generators.
- *Typesetting & Productivity:* LaTeX, VIM, Git, SVN, Perfoce, GDB, SWIG, make, CMake, Jenkins, Ant Build.

SERVICE

Vice president, IEEE Electron Devices Society-VIT, VIT University, Vellore, India May 2012 – July 2013

- Supervised and budgeted guest lectures by renowned professors in Nano/Quantum electronics and National workshops to bolster awareness on Nano Sciences. Determined chapter's events and advertised to increase chapter's membership by 30%.