	original	openipc	
	muxctrl_reg0 0x200f0000 0x1 GPIO1_0 [SHUTTER_TRIG]	muxctrl_reg0 0x200f0000 0x1 GPIO1_0 [SHUTTER_TRIG]	TRUE
	muxctrl_reg1 0x200f0004 0x1 GPIO1_1 [SDIO_CCLK_OUT]	muxctrl_reg1 0x200f0004 0x1 GPIO1_1 [SDIO_CCLK_OUT]	TRUE
	muxctrl_reg2 0x200f0008 0x1 GPIO1_2 [SENSOR_CLK]	muxctrl_reg2 0x200f0008 0x1 GPIO1_2 [SENSOR_CLK]	TRUE
12	muxctrl_reg3 0x200f000c 0 [GPIO1_4] SPI0_SCLK	muxctrl_reg3 0x200f000c 0 [GPIO1_4] SPI0_SCLK	TRUE
13	muxctrl_reg4 0x200f0010 0 [GPIO1_5] SPI0_SDO	muxctrl_reg4 0x200f0010 0 [GPIO1_5] SPI0_SDO	TRUE
14	muxctrl_reg5 0x200f0014 0 [GPIO1_6] SPI0_SDI	muxctrl_reg5 0x200f0014 0 [GPIO1_6] SPI0_SDI	TRUE
	muxctrl_reg6 0x200f0018 0x1 GPIO2_0 [I2C_SDA]	muxctrl_reg6 0x200f0018 0x1 GPIO2_0 [I2C_SDA]	TRUE
	muxctrl_reg7 0x200f001c 0x1 GPIO2_1 [I2C_SCL]	muxctrl_reg7 0x200f001c 0x1 GPIO2_1 [I2C_SCL]	TRUE
18	muxctrl_reg8 0x200f0020 0 [GPIO2_2] UART1_RTSN	muxctrl_reg8 0x200f0020 0x1 GPIO2_2 [UART1_RTSN]	FALSE
	muxctrl_reg9 0x200f0024 0x1 GPIO2_3 [UART1_RXD]	muxctrl_reg9 0x200f0024 0x1 GPIO2_3 [UART1_RXD]	TRUE
	muxctrl_reg10 0x200f0028 0x1 GPIO2_4 [UART1_CTSN]	muxctrl_reg10 0x200f0028 0x1 GPIO2_4 [UART1_CTSN]	TRUE
	muxctrl_reg11 0x200f002c 0x1 GPIO2_5 [UART1_TXD]	muxctrl_reg11 0x200f002c 0x1 GPIO2_5 [UART1_TXD]	TRUE
24	muxctrl_reg12 0x200f0030 0 [GPIO3_0] MII_CRS VOU1120_DATA10	muxctrl_reg12 0x200f0030 0x1 GPIO3_0 [MII_CRS] VOU1120_DATA10	FALSE
25	muxctrl_reg13 0x200f0034 0 [GPIO3_1] MII_COL VOU1120_DATA9	muxctrl_reg13 0x200f0034 0x1 GPIO3_1 [MII_COL] VOU1120_DATA9	FALSE
	muxctrl_reg14 0x200f0038 0x1 GPIO4_3 [MII_RXD3] VOU1120_DATA15	muxctrl_reg14 0x200f0038 0x1 GPIO4_3 [MII_RXD3] VOU1120_DATA15	TRUE
	muxctrl_reg15 0x200f003c 0x1 GPIO4_2 [MII_RXD2] VOU1120_DATA11	muxctrl_reg15 0x200f003c 0x1 GPIO4_2 [MII_RXD2] VOU1120_DATA11	TRUE
	muxctrl_reg16 0x200f0040 0x1 GPIO4_1 [MII_RXD1] VOU1120_DATA8	muxctrl_reg16 0x200f0040 0x1 GPIO4_1 [MII_RXD1] VOU1120_DATA8	TRUE
	muxctrl_reg17 0x200f0044 0x1 GPIO4_0 [MII_RXD0] VOU1120_DATA12	muxctrl_reg17 0x200f0044 0x1 GPIO4_0 [MII_RXD0] VOU1120_DATA12	TRUE
	muxctrl_reg18 0x200f0048 0x1 GPIO4_7 [MII_TXD3] VOU1120_DATA3	muxctrl_reg18 0x200f0048 0x1 GPIO4_7 [MII_TXD3] VOU1120_DATA3	TRUE
	muxctrl_reg19 0x200f004c 0x1 GPIO4_6 [MII_TXD2] VOU1120_DATA13	muxctrl_reg19 0x200f004c 0x1 GPIO4_6 [MII_TXD2] VOU1120_DATA13	TRUE
	muxctrl_reg20 0x200f0050 0x1 GPIO4_5 [MII_TXD1] VOU1120_DATA0	muxctrl_reg20 0x200f0050 0x1 GPIO4_5 [MII_TXD1] VOU1120_DATA0	TRUE
	muxctrl_reg21 0x200f0054 0x1 GPIO4_4 [MII_TXD0] VOU1120_DATA4	muxctrl_reg21 0x200f0054 0x1 GPIO4_4 [MII_TXD0] VOU1120_DATA4	TRUE
	muxctrl_reg22 0x200f0058 0x1 GPIO3_2 [MII_RXCK] VOU1120_CLK	muxctrl_reg22 0x200f0058 0x1 GPIO3_2 [MII_RXCK] VOU1120_CLK	TRUE
	muxctrl_reg23 0x200f005c 0x3 GPIO3_3 MII_TXCK VOU1120_DATA7 [RMII_CLK]	muxctrl_reg23 0x200f005c 0x3 GPIO3_3 MII_TXCK VOU1120_DATA7 [RMII_CLK]	TRUE
	muxctrl_reg24 0x200f0060 0x1 GPIO3_4 [MII_RXDV] VOU1120_DATA1	muxctrl_reg24 0x200f0060 0x1 GPIO3_4 [MII_RXDV] VOU1120_DATA1	TRUE
	muxctrl_reg25 0x200f0064 0x1 GPIO3_5 [MII_TXEN] VOU1120_DATA5	muxctrl_reg25 0x200f0064 0x1 GPIO3_5 [MII_TXEN] VOU1120_DATA5	TRUE
	muxctrl_reg26 0x200f0068 0x1 GPIO2_6 [MII_TXER]	muxctrl_reg26 0x200f0068 0x1 GPIO2_6 [MII_TXER]	TRUE
	muxctrl_reg27 0x200f006c 0x1 GPIO2_7 [MII_RXER]	muxctrl_reg27 0x200f006c 0x1 GPIO2_7 [MII_RXER]	TRUE
	muxctrl_reg28 0x200f0070 0x1 GPIO1_3 [EPHY_CLK] VOU1120_DATA2	muxctrl_reg28 0x200f0070 0x1 GPIO1_3 [EPHY_CLK] VOU1120_DATA2	TRUE
	muxctrl_reg29 0x200f0074 0x1 GPIO3_6 [MDCK] VOU1120_DATA6 BOOT_SEL	muxctrl_reg29 0x200f0074 0x1 GPIO3_6 [MDCK] VOU1120_DATA6 BOOT_SEL	TRUE
	muxctrl_reg30 0x200f0078 0x1 GPIO3_7 [MDIO] VOU1120_DATA14	muxctrl_reg30 0x200f0078 0x1 GPIO3_7 [MDIO] VOU1120_DATA14	TRUE
	muxctrl_reg31 0x200f007c 0x1 GPIO1_7 [FLASH_TRIG]	muxctrl_reg31 0x200f007c 0x1 GPIO1_7 [FLASH_TRIG]	TRUE
	muxctrl_reg32 0x200f0080 0x1 GPIO6_0 [SDIO_CARD_DETECT]	muxctrl_reg32 0x200f0080 0x1 GPIO6_0 [SDIO_CARD_DETECT]	TRUE
	muxctrl_reg33 0x200f0084 0x1 GPIO6_1 [SDIO_CARD_POWER_EN]	muxctrl_reg33 0x200f0084 0x1 GPIO6_1 [SDIO_CARD_POWER_EN]	TRUE
	muxctrl_reg34 0x200f0088 0x1 GPIO6_2 [SDIO_CWPR]	muxctrl_reg34 0x200f0088 0x1 GPIO6_2 [SDIO_CWPR]	TRUE
	muxctrl_reg35 0x200f008c 0x1 GPIO6_3 [SDIO_CCMD]	muxctrl_reg35 0x200f008c 0x1 GPIO6_3 [SDIO_CCMD]	TRUE
	muxctrl_reg36 0x200f0090 0x1 GPIO6_4 [SDIO_CDATA0] CLK_TEST_OUT0 CLK_TEST_OUT1 CLK_TEST_OUT2 CLK_TEST_OUT3	muxctrl_reg36 0x200f0090 0x1 GPIO6_4 [SDIO_CDATA0] CLK_TEST_OUT0 CLK_TEST_OUT1 CLK_TEST_OUT2 CLK_TEST_OUT3	TRUE
	muxctrl_reg37 0x200f0094 0x1 PLL_TEST_OUT0 [SDIO_CDATA1] GPIO6_5 PLL_TEST_OUT1 PLL_TEST_OUT2 PLL_TEST_OUT3 RTC_TEST_CLK	muxctrl_reg37 0x200f0094 0x1 PLL_TEST_OUT0 [SDIO_CDATA1] GPIO6_5 PLL_TEST_OUT1 PLL_TEST_OUT2 PLL_TEST_OUT3 RTC_TEST_CLK	TRUE
	muxctrl_reg38 0x200f0098 0x1 GPIO6_6 [SDIO_CDATA2]	muxctrl_reg38 0x200f0098 0x1 GPIO6_6 [SDIO_CDATA2]	TRUE
	muxctrl_reg39 0x200f009c 0x1 GPIO6_7 [SDIO_CDATA3]	muxctrl_reg39 0x200f009c 0x1 GPIO6_7 [SDIO_CDATA3]	TRUE
	muxctrl_reg40 0x200f00a0 0 [SFC_DIO] GPIO7_0	muxctrl_reg40 0x200f00a0 0 [SFC_DIO] GPIO7_0	TRUE
	muxctrl_reg41 0x200f00a4 0 [SFC_WP_IO2] GPIO7_1	muxctrl_reg41 0x200f00a4 0 [SFC_WP_IO2] GPIO7_1	TRUE
	muxctrl_reg42 0x200f00a8 0 [SFC_CLK] GPIO7_2 SFC_ADDR_MODE	muxctrl_reg42 0x200f00a8 0 [SFC_CLK] GPIO7_2 SFC_ADDR_MODE	TRUE
	muxctrl_reg43 0x200f00ac 0 [SFC_DOI] GPIO7_3	muxctrl_reg43 0x200f00ac 0 [SFC_DOI] GPIO7_3	TRUE
	muxctrl_reg44 0x200f00b0 0 [SFC_HOLD_IO3] GPIO7_4	muxctrl_reg44 0x200f00b0 0 [SFC_HOLD_IO3] GPIO7_4	TRUE
	muxctrl_reg45 0x200f00b4 0x1 GPIO5_0 [USB_OVRCUR]	muxctrl_reg45 0x200f00b4 0x1 GPIO5_0 [USB_OVRCUR]	TRUE
41	muxctrl_reg46 0x200f00b8 0 [GPIO5_1] USB_PWREN	muxctrl_reg46 0x200f00b8 0x1 GPIO5_1 [USB_PWREN]	FALSE
	muxctrl_reg47 0x200f00bc 0x1 GPIO5_2 [PWM_OUT0]	muxctrl_reg47 0x200f00bc 0x1 GPIO5_2 [PWM_OUT0]	TRUE
43	muxctrl_reg48 0x200f00c0 0 [GPIO5_3] PWM_OUT1	muxctrl_reg48 0x200f00c0 0x1 GPIO5_3 [PWM_OUT1]	FALSE

61	muxctrl_reg49 0x200f00c4 0x1 IR_IN [GPIO7_5]	muxctrl_reg49 0x200f00c4 0x1 IR_IN [GPIO7_5]	TRUE
72	muxctrl_reg50 0x200f00c8 0x1 reserved [GPIO9_0]	muxctrl_reg50 0x200f00c8 0x1 reserved [GPIO9_0]	TRUE
73	muxctrl_reg51 0x200f00cc 0x1 reserved [GPIO9_1]	muxctrl_reg51 0x200f00cc 0x1 reserved [GPIO9_1]	TRUE
74	muxctrl_reg52 0x200f00d0 0x1 reserved [GPIO9_2]	muxctrl_reg52 0x200f00d0 0x1 reserved [GPIO9_2]	TRUE
75	muxctrl_reg53 0x200f00d4 0x1 reserved [GPIO9_3]	muxctrl_reg53 0x200f00d4 0x1 reserved [GPIO9_3]	TRUE
76	muxctrl_reg54 0x200f00d8 0x1 reserved [GPIO9_4]	muxctrl_reg54 0x200f00d8 0x1 reserved [GPIO9_4]	TRUE
77	muxctrl_reg55 0x200f00dc 0x1 reserved [GPIO9_5]	muxctrl_reg55 0x200f00dc 0x1 reserved [GPIO9_5]	TRUE
78	muxctrl_reg56 0x200f00e0 0x1 reserved [GPIO9_6]	muxctrl_reg56 0x200f00e0 0x1 reserved [GPIO9_6]	TRUE
79	muxctrl_reg57 0x200f00e4 0x1 reserved [GPIO9_7]	muxctrl_reg57 0x200f00e4 0x1 reserved [GPIO9_7]	TRUE
62	muxctrl_reg58 0x200f0108 0 [GPIO7_6] UART2_RXD	muxctrl_reg58 0x200f0108 0 [GPIO7_6] UART2_RXD	TRUE
63	muxctrl_reg59 0x200f010c 0 [GPIO7_7] UART2_TXD	muxctrl_reg59 0x200f010c 0 [GPIO7_7] UART2_TXD	TRUE
44	muxctrl_reg60 0x200f0110 0 [GPIO5_4] SPI1_SCLK	muxctrl_reg60 0x200f0110 0 [GPIO5_4] SPI1_SCLK	TRUE
45	muxctrl_reg61 0x200f0114 0 [GPIO5_5] SPI1_SDO	muxctrl_reg61 0x200f0114 0 [GPIO5_5] SPI1_SDO	TRUE
46	muxctrl_reg62 0x200f0118 0 [GPIO5_6] SPI1_SDI	muxctrl_reg62 0x200f0118 0 [GPIO5_6] SPI1_SDI	TRUE
47	muxctrl_reg63 0x200f011c 0 [GPIO5_7] SPI1_CSN	muxctrl_reg63 0x200f011c 0 [GPIO5_7] SPI1_CSN	TRUE
0	muxctrl_reg64 0x200f0120 0 [GPIO0_0] JTAG_TRSTN TEMPER_DQ	muxctrl_reg64 0x200f0120 0 [GPIO0_0] JTAG_TRSTN TEMPER_DQ	TRUE
1	muxctrl_reg65 0x200f0124 0 [GPIO0_1] JTAG_TCK TEMPER_DQ	muxctrl_reg65 0x200f0124 0 [GPIO0_1] JTAG_TCK TEMPER_DQ	TRUE
2	muxctrl_reg66 0x200f0128 0 [GPIO0_2] JTAG_TMS TEMPER_DQ	muxctrl_reg66 0x200f0128 0 [GPIO0_2] JTAG_TMS TEMPER_DQ	TRUE
3	muxctrl_reg67 0x200f012c 0 [GPIO0_3] JTAG_TDO TEMPER_DQ	muxctrl_reg67 0x200f012c 0 [GPIO0_3] JTAG_TDO TEMPER_DQ	TRUE
4	muxctrl_reg68 0x200f0130 0 [GPIO0_4] JTAG_TDI TEMPER_DQ	muxctrl_reg68 0x200f0130 0 [GPIO0_4] JTAG_TDI TEMPER_DQ	TRUE
5	muxctrl_reg69 0x200f0134 0x1 SVB_PWM [GPIO0_5] TEMPER_DQ	muxctrl_reg69 0x200f0134 0x1 SVB_PWM [GPIO0_5] TEMPER_DQ	TRUE
6	muxctrl_reg70 0x200f0138 0 [GPIO0_6] SVB_PWM TEMPER_DQ	muxctrl_reg70 0x200f0138 0x1 GPIO0_6 [SVB_PWM] TEMPER_DQ	FALSE
7	muxctrl_reg71 0x200f013c 0x1 SYS_RSTN_OUT [GPIO0_7] TEMPER_DQ	muxctrl_reg71 0x200f013c 0 [SYS_RSTN_OUT] GPIO0_7 TEMPER_DQ	FALSE
	muxctrl_reg72 0x200f0140 0 [VIU_CLK] GPIO11_6	muxctrl_reg72 0x200f0140 0 [VIU_CLK] GPIO11_6	TRUE
	muxctrl_reg73 0x200f0144 0 [VIU_VS] GPIO11_5	muxctrl_reg73 0x200f0144 0 [VIU_VS] GPIO11_5	TRUE
	muxctrl_reg74 0x200f0148 0 [VIU_HS] GPIO11_4	muxctrl_reg74 0x200f0148 0 [VIU_HS] GPIO11_4	TRUE
	muxctrl_reg75 0x200f014c 0 [VIU_DAT11] GPIO11_3	muxctrl_reg75 0x200f014c 0 [VIU_DAT11] GPIO11_3	TRUE
	muxctrl_reg76 0x200f0150 0 [VIU_DAT10] GPIO11_2	muxctrl_reg76 0x200f0150 0 [VIU_DAT10] GPIO11_2	TRUE
	muxctrl_reg77 0x200f0154 0 [VIU_DAT9] GPIO11_1	muxctrl_reg77 0x200f0154 0 [VIU_DAT9] GPIO11_1	TRUE
	muxctrl_reg78 0x200f0158 0 [VIU_DAT8] GPIO11_0	muxctrl_reg78 0x200f0158 0 [VIU_DAT8] GPIO11_0	TRUE
	muxctrl_reg79 0x200f015c 0 [VIU_DAT7] GPIO10_7	muxctrl_reg79 0x200f015c 0 [VIU_DAT7] GPIO10_7	TRUE
	muxctrl_reg80 0x200f0160 0 [VIU_DAT6] GPIO10_6	muxctrl_reg80 0x200f0160 0 [VIU_DAT6] GPIO10_6	TRUE
	muxctrl_reg81 0x200f0164 0 [VIU_DAT5] GPIO10_5	muxctrl_reg81 0x200f0164 0 [VIU_DAT5] GPIO10_5	TRUE
	muxctrl_reg82 0x200f0168 0 [VIU_DAT4] GPIO10_4	muxctrl_reg82 0x200f0168 0 [VIU_DAT4] GPIO10_4	TRUE
	muxctrl_reg83 0x200f016c 0 [VIU_DAT3] GPIO10_3	muxctrl_reg83 0x200f016c 0 [VIU_DAT3] GPIO10_3	TRUE
	muxctrl_reg84 0x200f0170 0 [VIU_DAT2] GPIO10_2	muxctrl_reg84 0x200f0170 0 [VIU_DAT2] GPIO10_2	TRUE
	muxctrl_reg85 0x200f0174 0 [VIU_DAT1] GPIO10_1	muxctrl_reg85 0x200f0174 0 [VIU_DAT1] GPIO10_1	TRUE
	muxctrl_reg86 0x200f0178 0 [VIU_DAT0] GPIO10_0	muxctrl_reg86 0x200f0178 0 [VIU_DAT0] GPIO10_0	TRUE