REPORT ON

DESIGN AND LAYOUT OF 8X8 BIT BAUGH WOOLEY MULTIPLIER USING CADENCE VIRTUOSO

DONE BY

SHASHI KUMAR JAKKA

MTECH (VLSI AND NANOELECTRONICS)

AIM: To design circuit and physical layout of a 8X8 Baugh Wooley Multiplier circuit using Cadence Virtuoso and verify its correctness through DRC and LVS checks.

Tools Used: Cadence Virtuoso

Theory:

Baugh Wooley Multiplier

The Baugh–Wooley algorithm is used for signed multiplication in two's complement form. It allows signed multiplication to be performed using the regular array multiplier structure by rearranging and complementing partial products so that only additions are required. For two signed 8-bit numbers in two's complement, the multiplicand and multiplier are written as

$$A = -A_7 \cdot 2^7 + \sum_{i=0}^{6} A_i \, 2^i, \ldots\ldots\ldots..(1)$$

$$B = -B_7 \cdot 2^7 + \sum_{j=0}^{6} B_j \, 2^j \ldots\ldots\ldots\ldots (2)$$

The product is given by $P = A * B$
Expanding this expression gives
$P = A_7 B_7 \cdot 2^{14} - A_7 \sum_{j=0}^{6} B_j \cdot 2^{7+j} - B_7 \sum_{i=0}^{6} A_i \cdot 2^{7+i} + \sum_{i=0}^{6} \sum_{j=0}^{6} A_i \, B_j \cdot 2^{i+j} \ldots\ldots\ldots..(3)$

The first term $A_7 B_7 \; 2^{14}$is positive. The middle two terms are negative partial products, while the last term is the unsigned multiplication of the lower 7 bits. In the Baugh–Wooley approach, each negative term -x is rewritten as ($\overline{x}$ + 1). Instead of subtracting a partial product, the complemented value is used, and a correction term is added in the appropriate column. In the 8-bit case, the negative terms appear in columns corresponding to weights 2^7 through 2^{13}.

The correction evaluates to

$$C = -2 \sum_{k=7}^{13} 2^k = -(2^{15} - 2^8) = -2^{15} + 2^8 \ldots\ldots\ldots (4)$$

This correction is implemented by inserting a fixed '1' at bit position 8 and a negative carry at bit position 15. The array structure of the Baugh–Wooley multiplier is built using two types of cells: white and gray cells.
A white cell is the standard multiplier cell. It generates the partial product $AiBj$ using an AND gate and combines it with the incoming sum and carry signals in a full adder. The sum is passed vertically downward, while the carry is passed diagonally to the next stage. A gray cell is introduced when the algorithm requires a complemented partial product. Instead of directly using $AiBj$, the gray cell inverts this term to produce $\overline{A_i B_j}$ and feeds it into the full adder. It also takes care of the correction '1' that is needed in that column to balance the complemented operation. Structurally, the gray cell has the same adder as the white cell but includes an inverter before the AND output. By arranging white cells for normal terms and gray cells for complemented sign-related terms, the Baugh–Wooley multiplier achieves signed multiplication with the same regular grid-like array used for unsigned multiplication. This uniformity makes the design simple,

modular, and well-suited for hardware implementation. The circuit with logic using white and gray cells are shown in figure 1.

The final form of the 8-bit product can be written as

$$P = \sum_{i=0}^{6}\sum_{j=0}^{6} A_i\, B_j 2^{i+j} + \sum_{j=0}^{6} \overline{A_7 B_j}\, 2^{7+j} + \sum_{j=0}^{6} \overline{B_7 A_j}\, 2^{7+j} + A_7 B_7 2^{14} + 2^8 - 2^{15} \ldots\ldots\ldots\ldots (5)$$

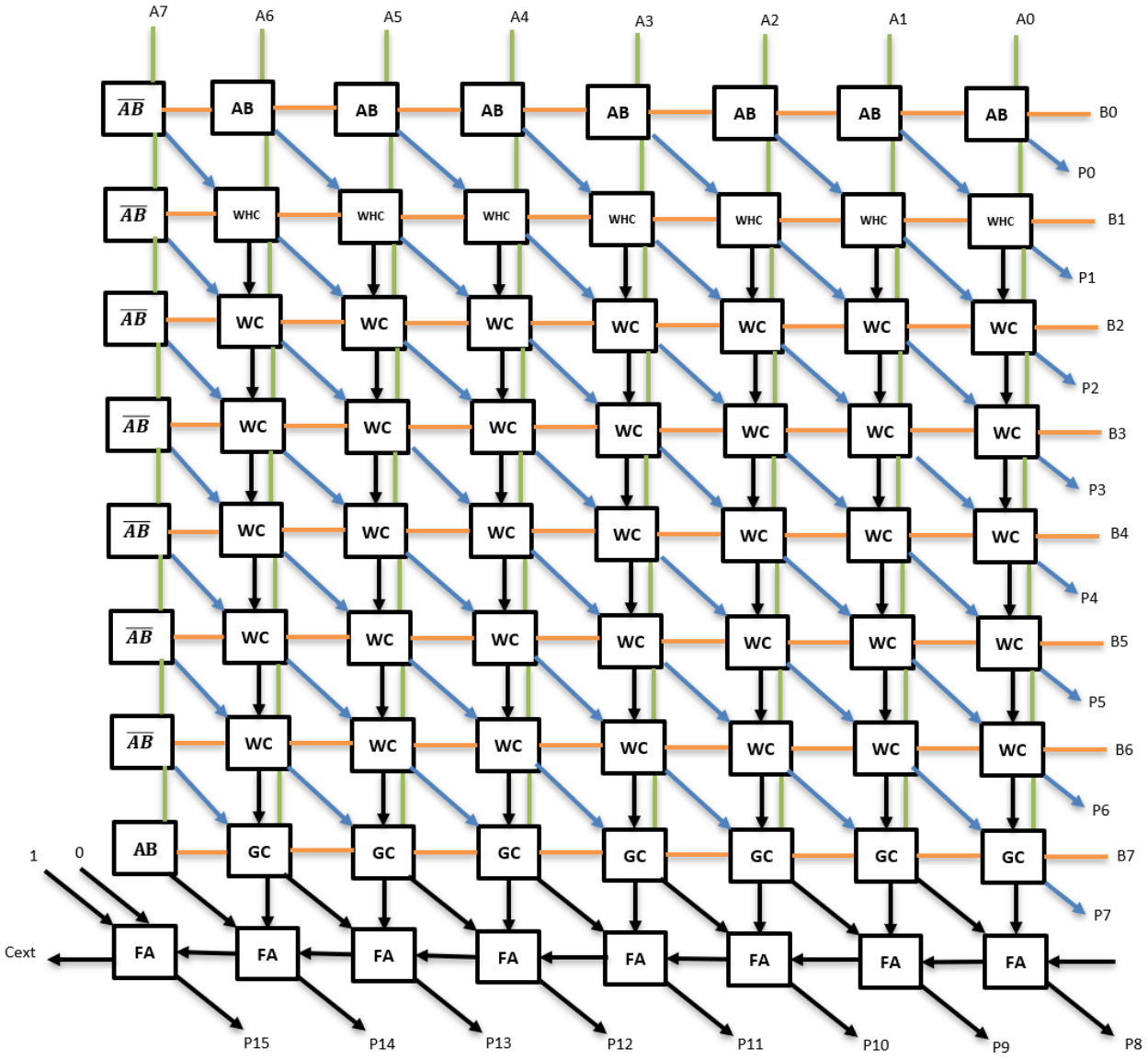

Fig: Circuit for 8x8 Baugh-Wooley Multiplier where $\overline{AB}$ is a NAND gate, **AB** is a AND gate, **WHC** is a White cell with half adder, **WC** White cell, **GC** is a Grey cell and **FA** is a Mirror full adder.

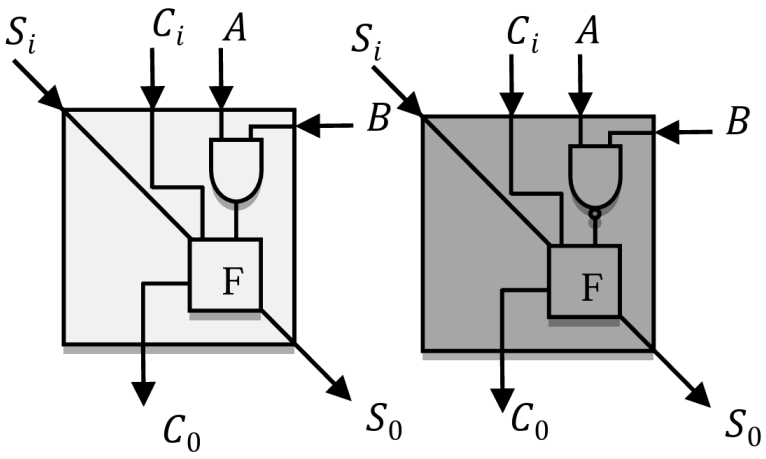

Figure 1(b): white and gray cell used in generic Baugh Wooley Multiplier

Layout

Layout design is the process of converting a circuit schematic into its physical geometric representation on silicon. It involves placing transistors, interconnections, and other components using layers like diffusion, polysilicon, and metal. In Cadence Virtuoso, the layout defines how the circuit will be fabricated, ensuring proper connectivity and minimal area while following design constraints. A good layout improves performance, reduces parasitic, and ensures manufacturability.

DRC (Design Rule Check)

Design Rule Check (DRC) ensures that the layout adheres to the fabrication process rules such as minimum width, spacing, overlap, and enclosure between layers. These rules are defined by the foundry to prevent defects during manufacturing. In Cadence Virtuoso, the DRC tool automatically scans the layout and highlights rule violations, which must be corrected before proceeding to fabrication to ensure a reliable and error-free chip.

LVS (Layout Versus Schematic)

Layout Versus Schematic (LVS) verification compares the extracted layout netlist with the schematic netlist to confirm that both represent the same electrical design. It checks the device types, connections, and hierarchy for consistency. In Cadence Virtuoso, the LVS tool ensures that no errors occurred during layout creation, such as missing or extra connections, guaranteeing that the fabricated chip will function as intended.

Multiplier Layout

A multiplier layout represents the physical realization of an arithmetic multiplication circuit on silicon. In the case of the 8×8 Baugh–Wooley Multiplier, the design uses the Baugh–Wooley algorithm, which efficiently handles signed number multiplication in two's complement form. This method simplifies partial product generation and summation, leading to a more regular and symmetrical layout structure. The layout involves placing and routing logic blocks such as AND gates, adders, and partial product arrays. Proper transistor sizing, metal routing, and layer optimization are essential to minimize propagation delay and power consumption. Using Cadence Virtuoso, the schematic of the 8×8 Baugh–Wooley Multiplier is converted into a layout view, ensuring correct connectivity and adherence to design rules for accurate and efficient VLSI implementation.

Schematics and Corresponding Layouts of 8×8 Baugh–Wooley Multiplier (from Basic Gates to Complete Multiplier):

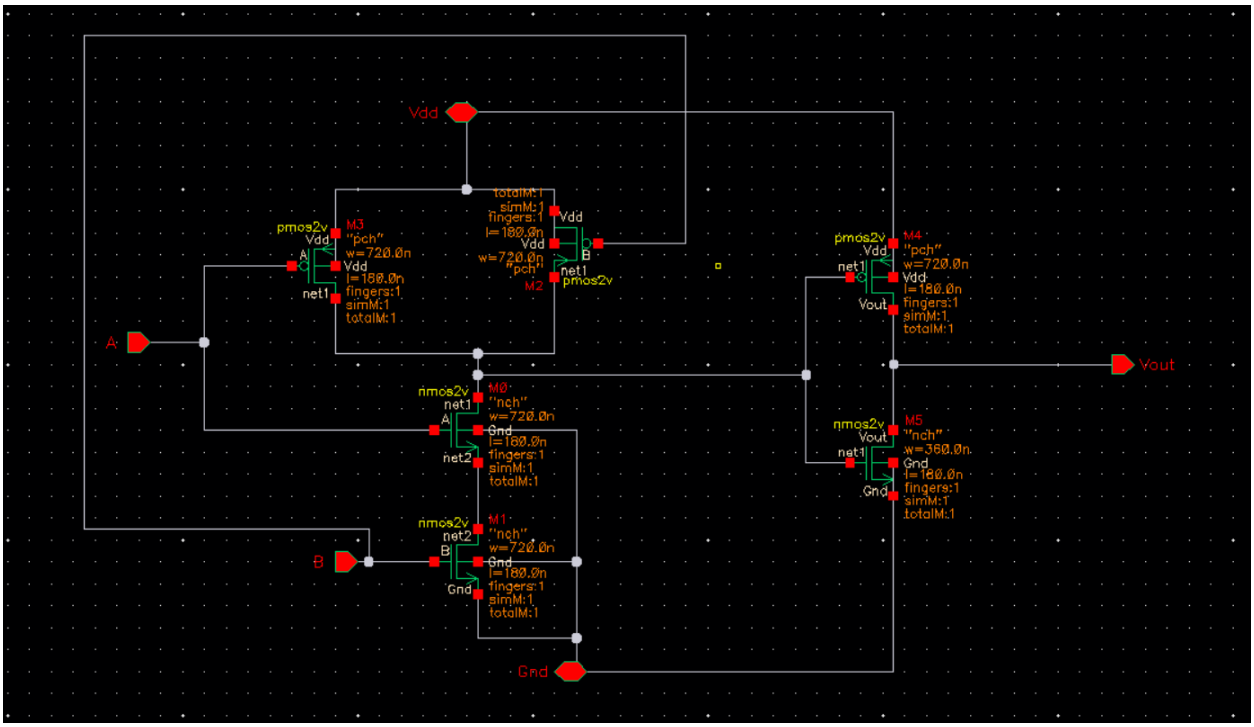

Fig: Schematic of AND gate

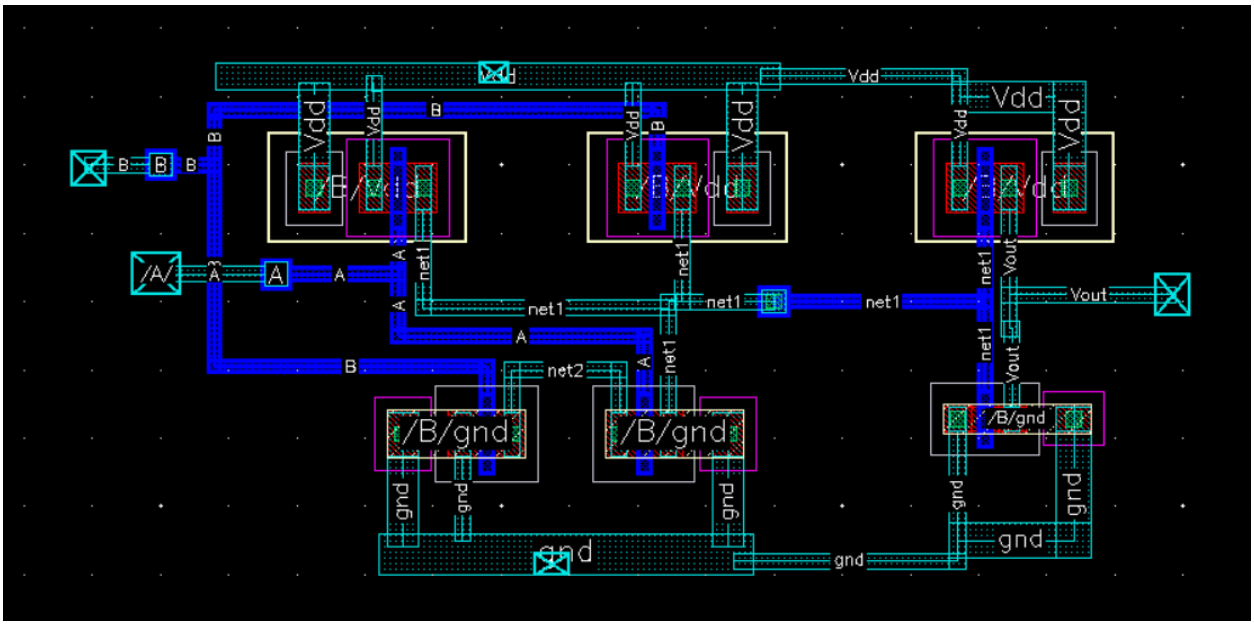

Fig: Layout of AND gate

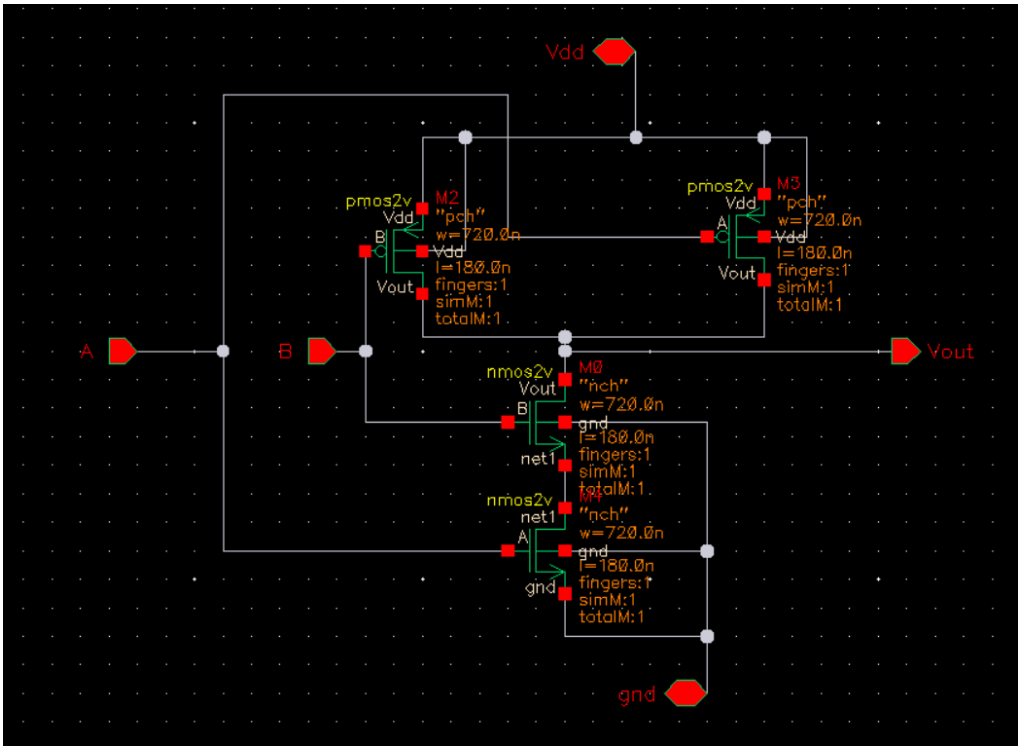

Fig: Schematic of NAND gate

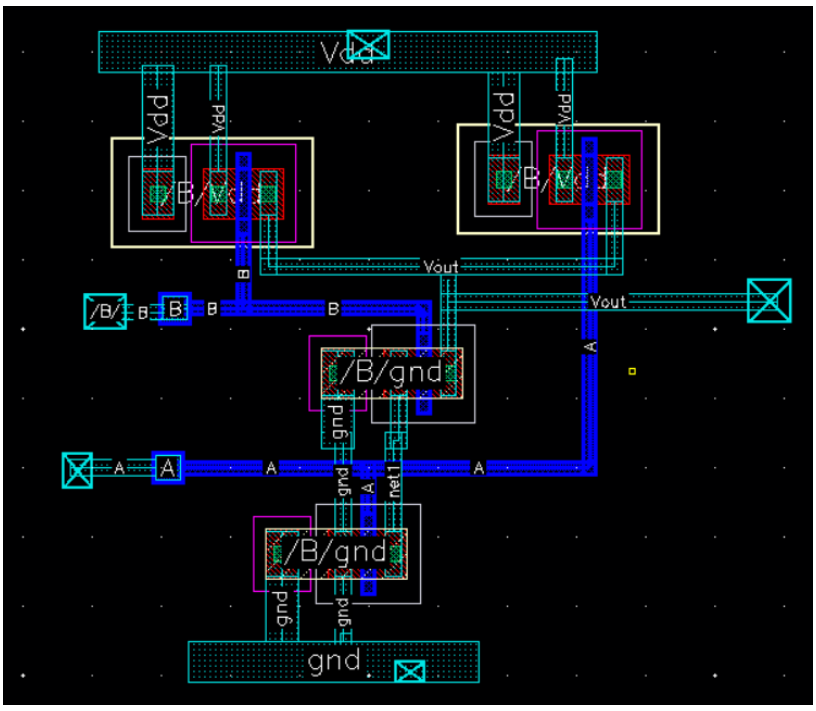

Fig: layout of NAND gate

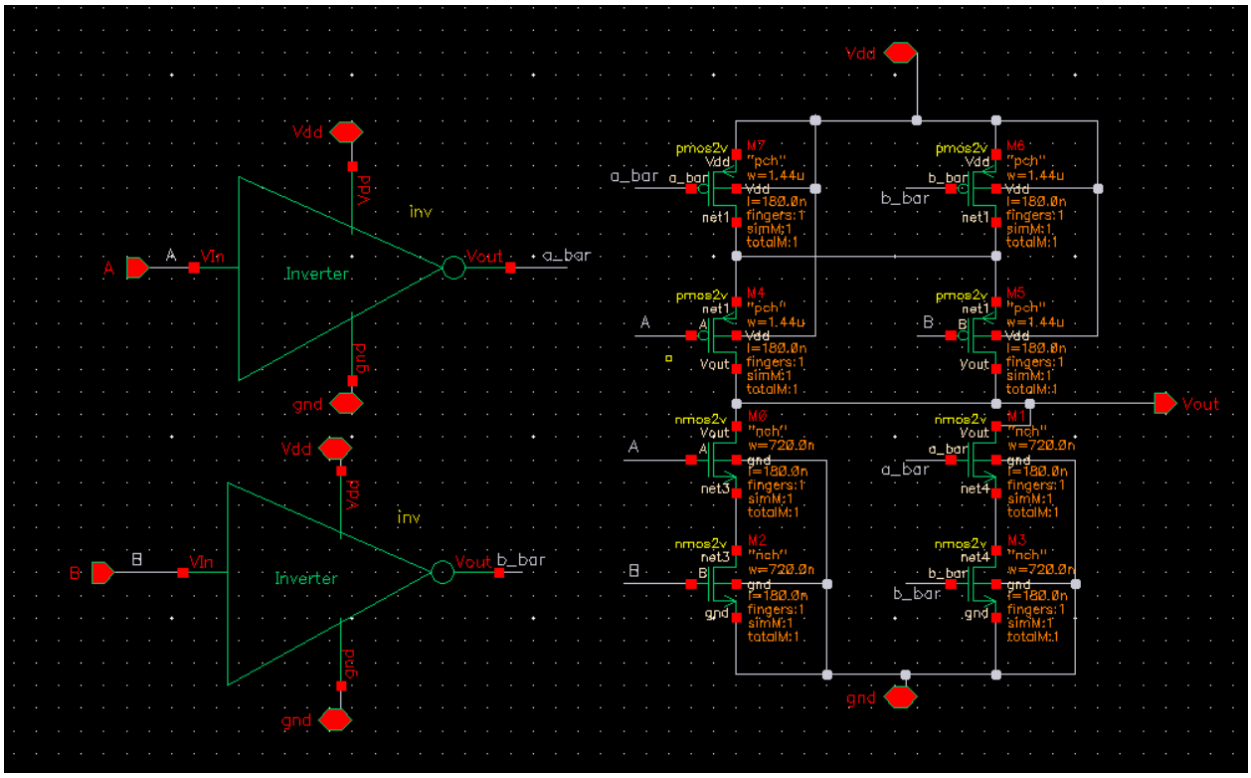

Fig: Schematic of XOR gate

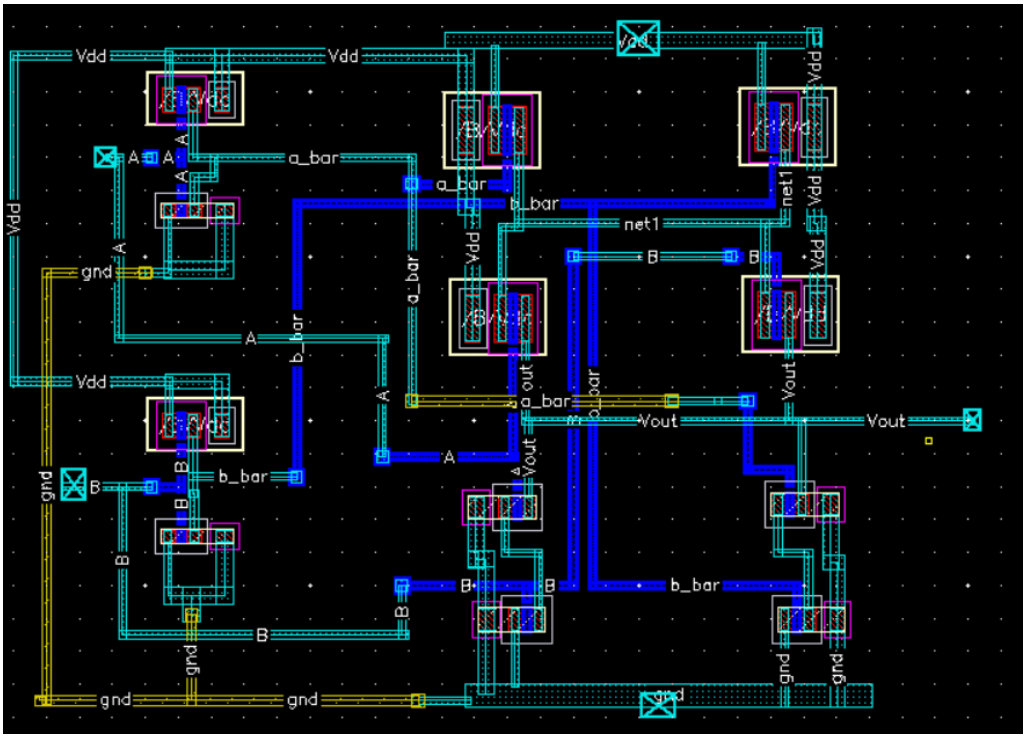

Fig: Layout of XOR gate

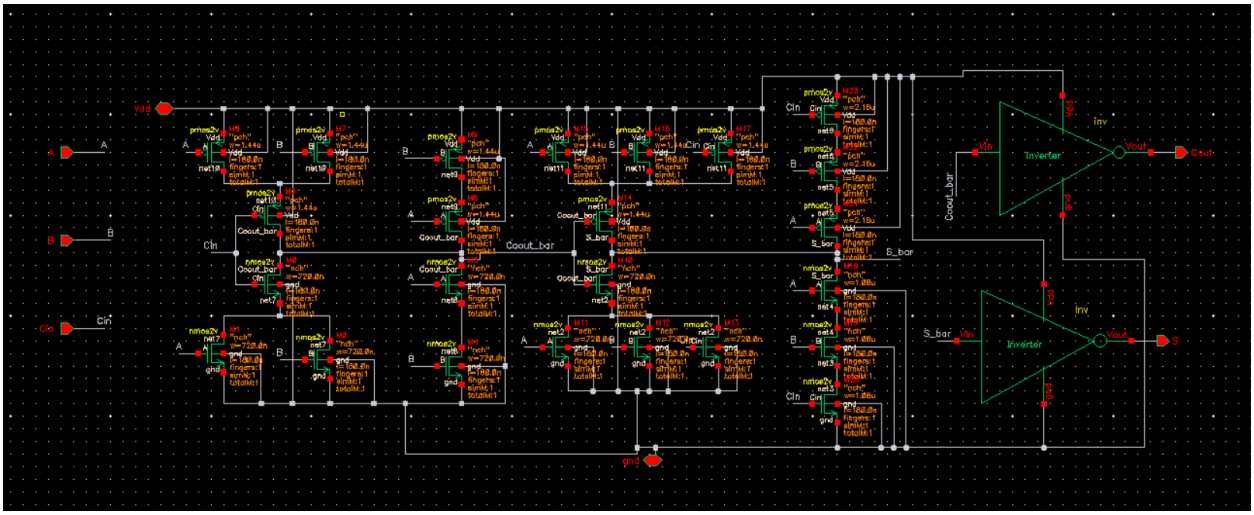

Fig: Schematic of Mirror Full Adder

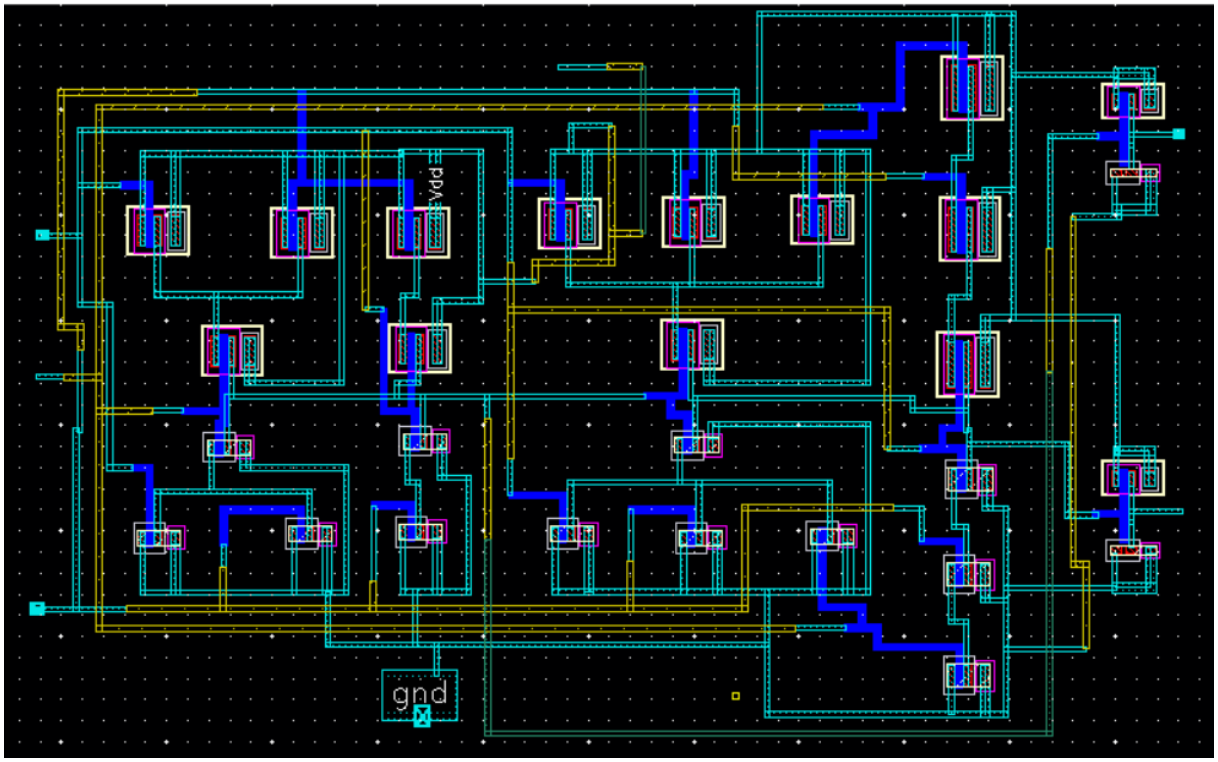

Fig: Layout of Mirror Full Adder

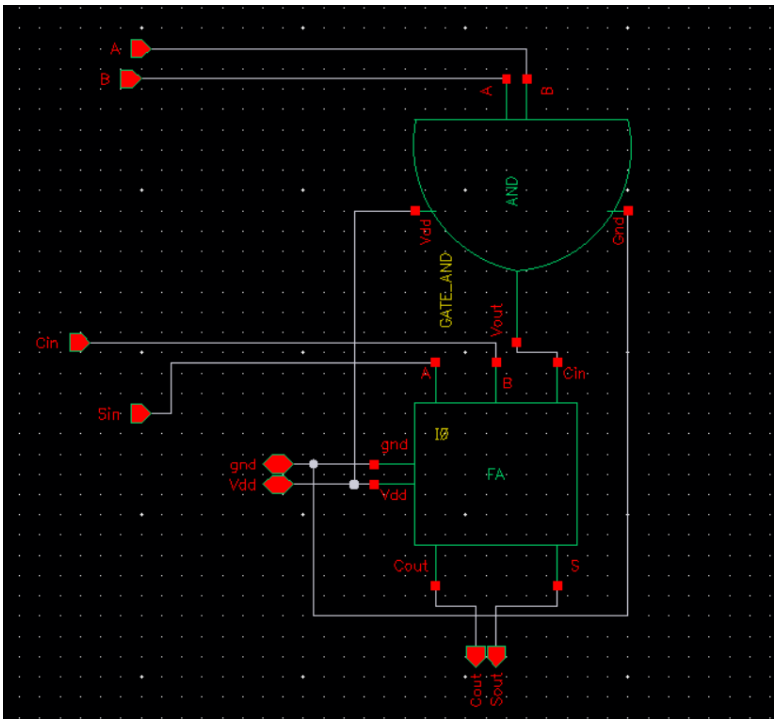

Fig: Schematic of white cell

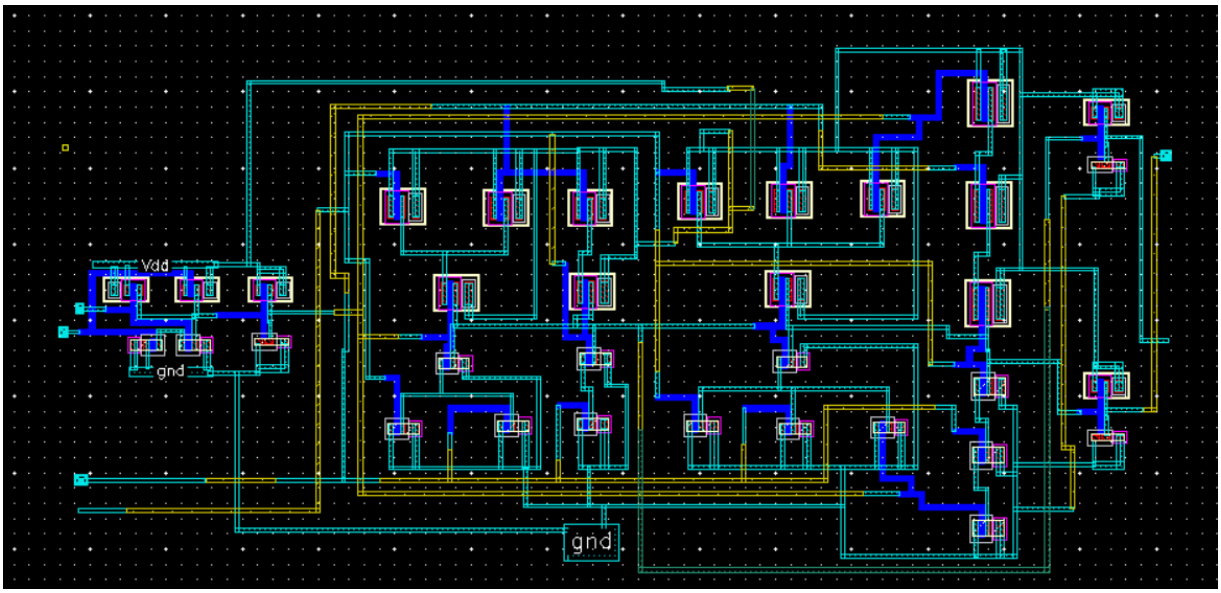

Fig: Layout of White cell

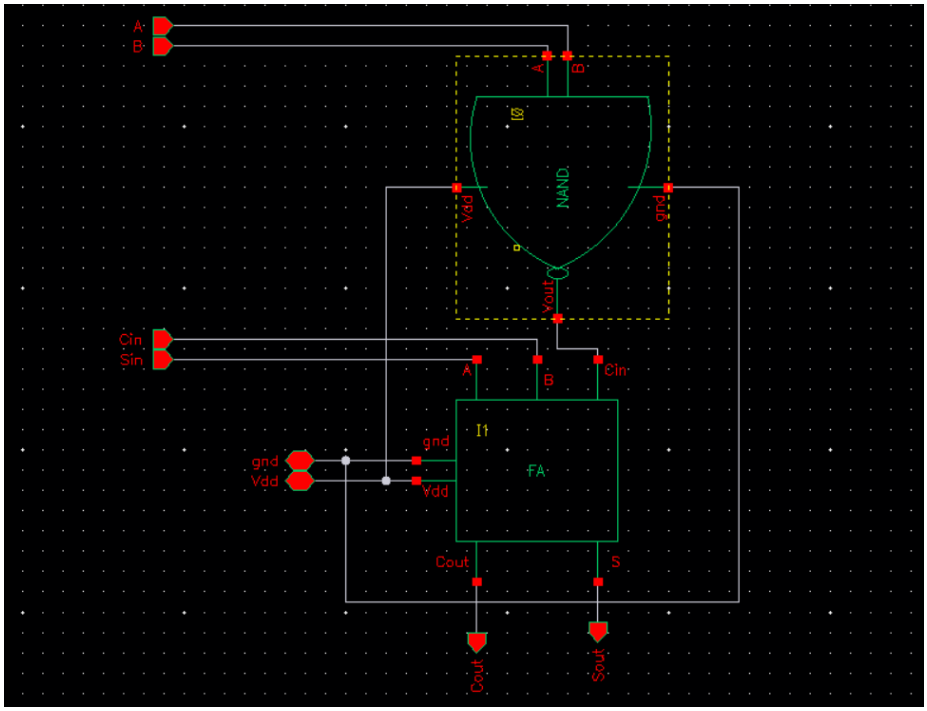

Fig: Schematic of Grey cell

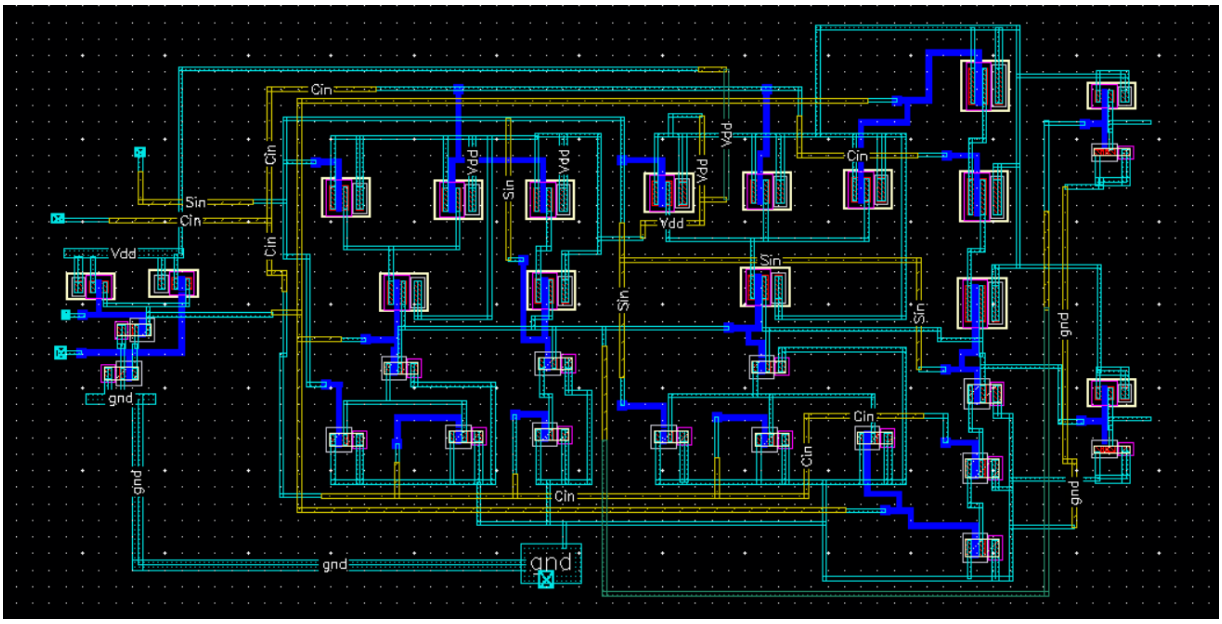

Fig: Layout of Grey cell

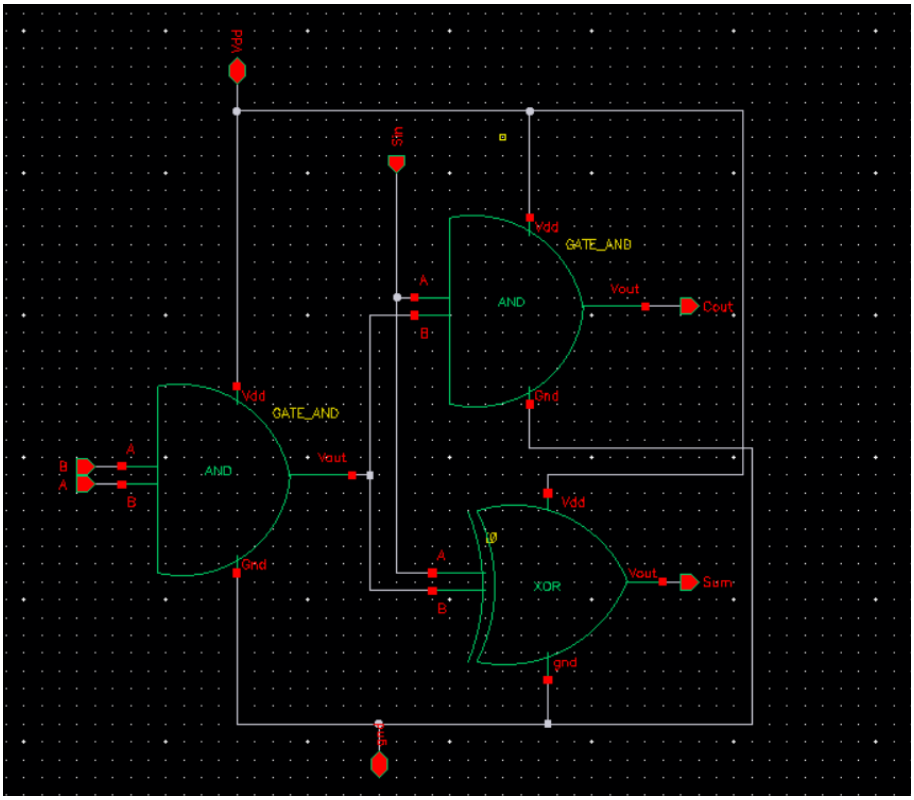

Fig: Schematic of white cell with half adder

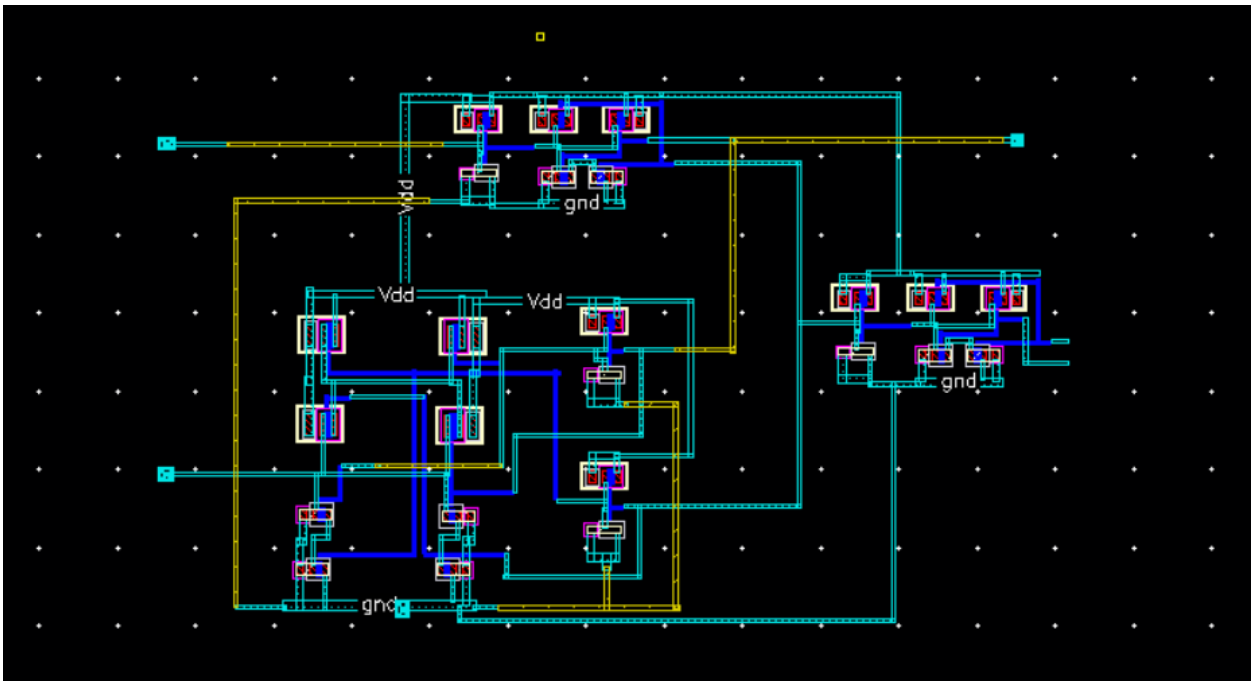

Fig: Layout of white cell with half adder

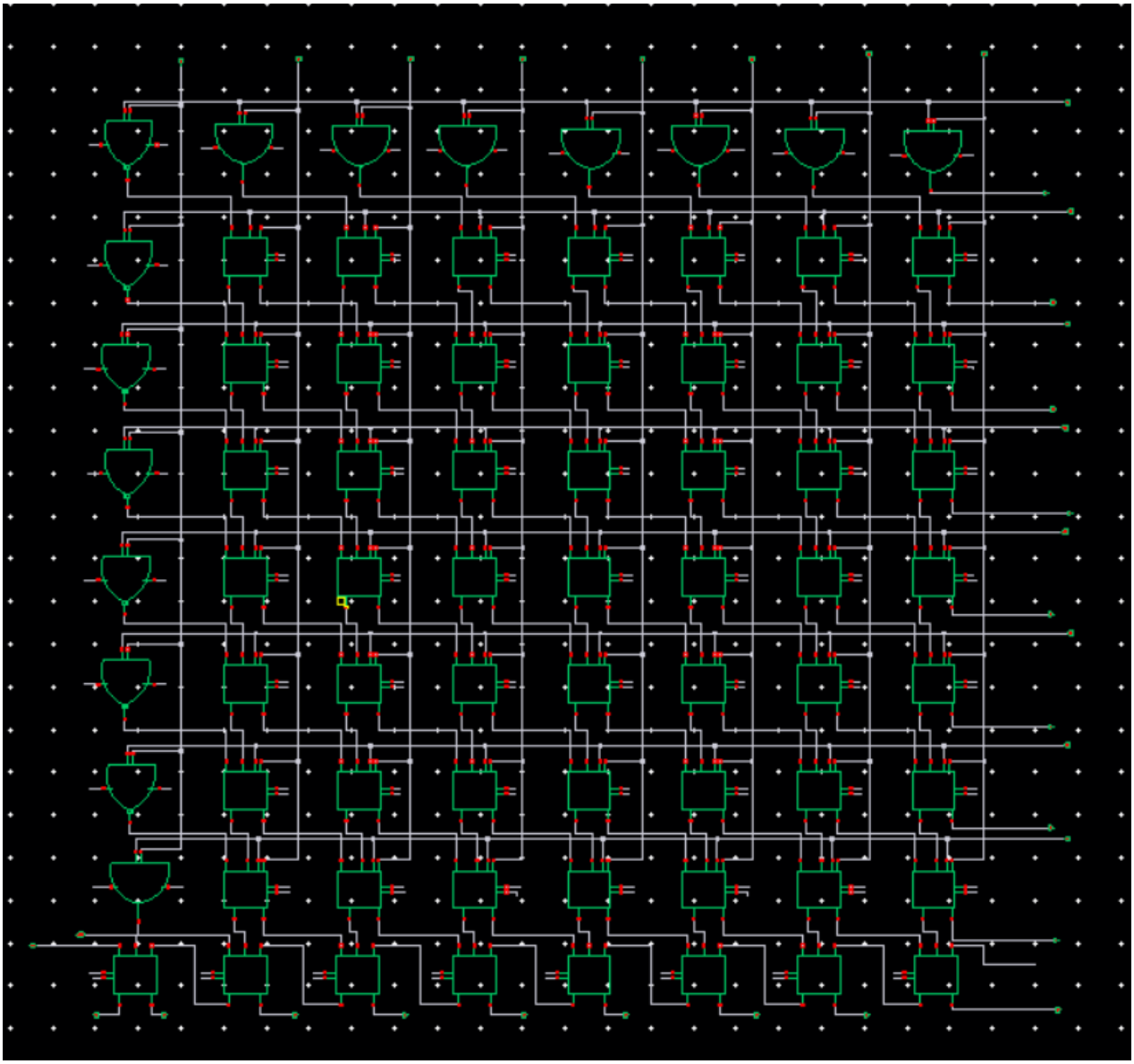

Fig: Schematic of 8x8 Baugh–Wooley Multiplier

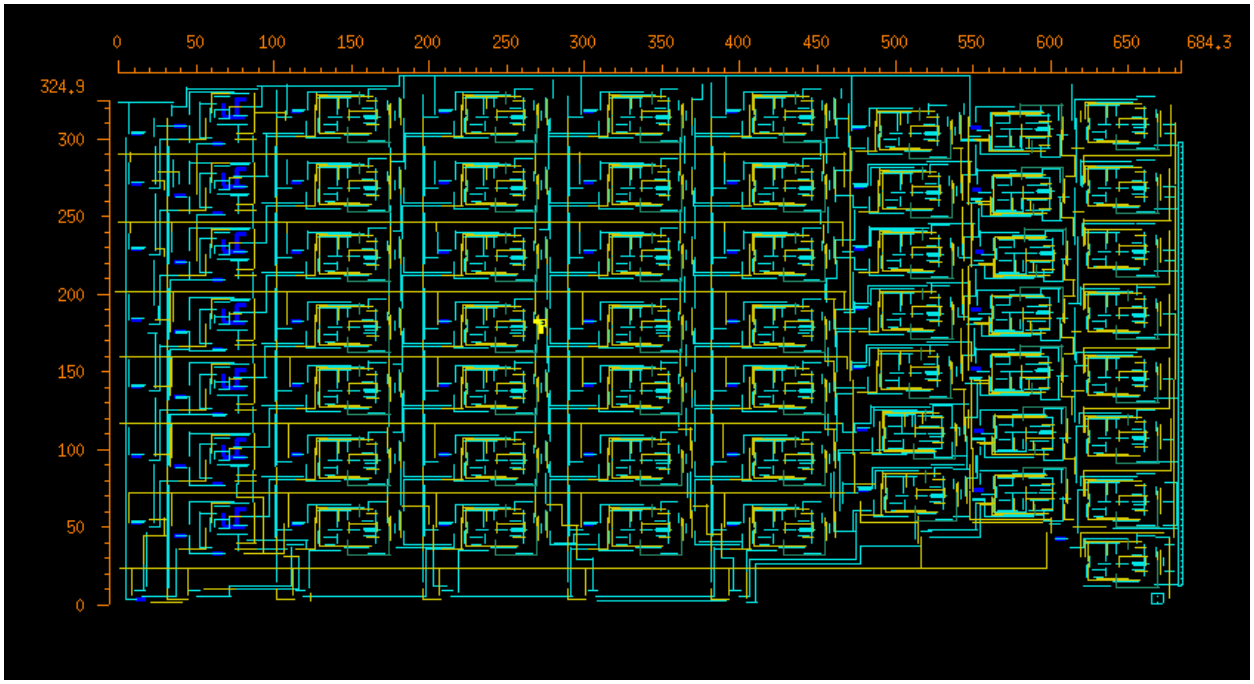

Fig: Layout of 8x8 Baugh–Wooley multiplier

Layout dimensions observed are approximately 325 µm x 685 µm.

Total number of transistors used in the circuit	1882
Area utilized for the layout	0.223 mm^2

Table: Hardware and area used for circuit

DRC Check:

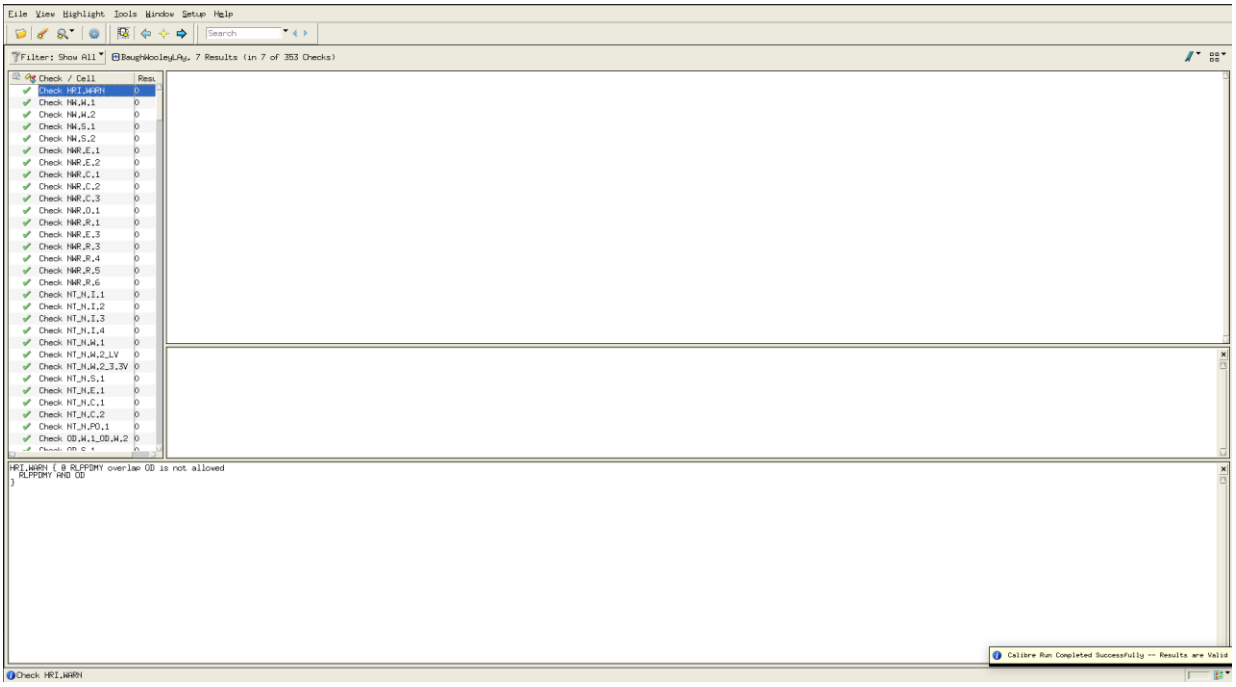

Fig: No Error in DRC check

LVS Check:

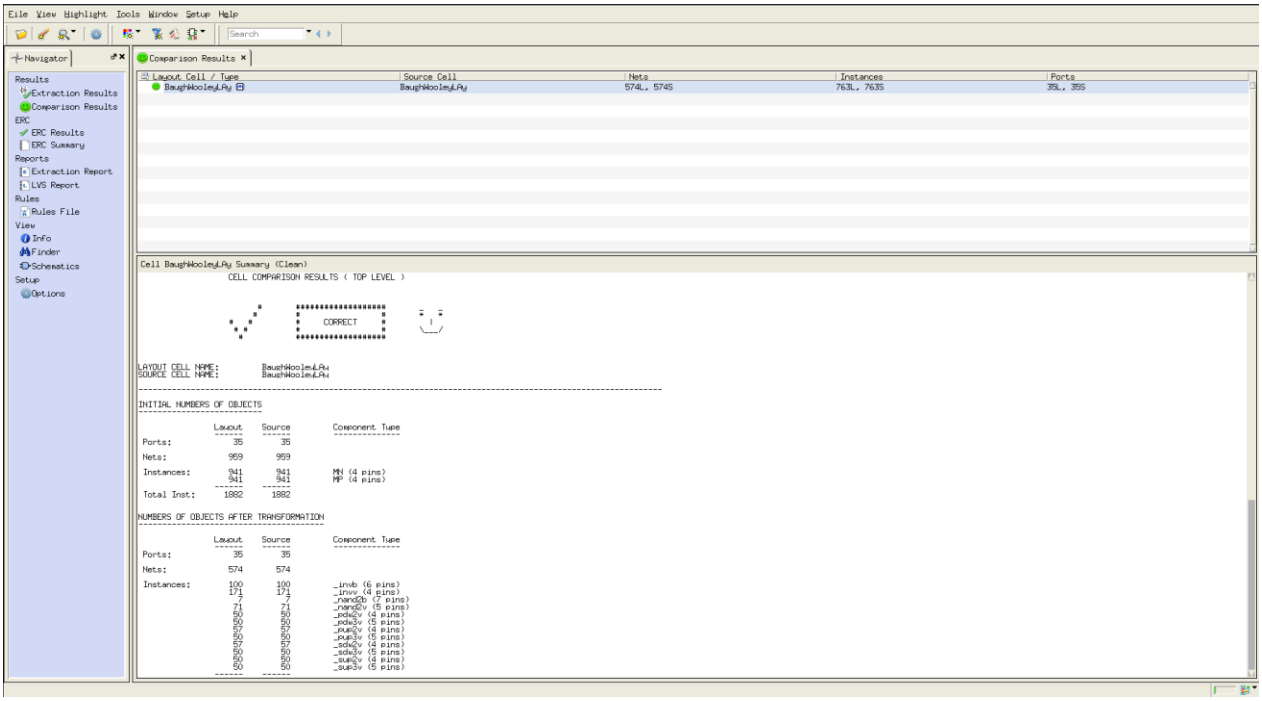

Fig: Successful LVS check

Conclusion:

The schematic and layout of the 8×8 Baugh–Wooley Multiplier were successfully designed and verified using Cadence Virtuoso. The design process began with the implementation of basic logic gates, followed by the development of partial product generation and adder arrays to construct the complete multiplier. The Baugh–Wooley algorithm enabled efficient signed multiplication with a regular layout structure, optimizing both speed and area. DRC and LVS checks confirmed that the layout is error-free and electrically consistent with the schematic.