

# RS-485 failsafe biasing: Old versus new transceivers

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It is incredible that an industrial interface standard such as RS-485, having been around for 30 years, still appears obscure to many industrial-network designers. While there should be plenty of literature available explaining the standard fundamentals, the Texas Instruments (TI) application team continues to receive basic questions on a weekly basis, such as how to apply failsafe biasing to an idle bus.

Failsafe biasing refers to the technique of providing a differential voltage to a terminated, idle bus in order to maintain the receiver output of a bus transceiver in a logic-high state. This technique is commonly required when legacy transceiver designs are used for designing bus networks.

Legacy designs such as transceiver X in Table 1 possess a wide input sensitivity of  $\pm 200$  mV. This means that small input signals between +200 mV and -200 mV can turn the receiver output either high or low, thus making the output state indeterminate.

During a data transmission, the differential line voltage of a fully loaded bus is required to be higher than  $\pm 1.5$  V, which is well above the transceiver's input sensitivity. However, during a handover of bus access from one node to another, or during a transmission pause, the bus idles. Then the low-impedance termination resistors, connecting the two conductors of the differential signal pair with each other, cause the differential bus voltage to be 0 V, right in the middle of the transceiver's input sensitivity, which produces an indeterminate output.

Therefore, to keep the receiver outputs at a logic high during bus idling, a positive, differential failsafe voltage higher than a receiver's positive input threshold ( $V_{IT+}$ ) must be applied to the bus.

Table 1 shows that the theoretically required failsafe levels decrease with the receiver's positive input threshold from one generation to the next. While transceiver X

requires a minimum of +200 mV of failsafe biasing, transceivers Y and Z can do without it as their positive input thresholds are below 0 V. Unfortunately, these values apply only in noise-free environments such as laboratories or the Earth's poles, and certainly not in the harsh environments of industrial factories where RS-485 networks are commonly installed.

Differential noise induced into the bus wires can falsely trigger a receiver input if the projected noise magnitude has not been included in the failsafe voltage calculation. Using a twisted-pair bus cable helps to convert noise induced along the cable run into common-mode noise. This noise is then rejected by the receiver's differential input. However, cable irregularities as well as noise induced at the bus node connectors might contribute to differential noise that cannot be rejected by a receiver.

Figure 1 on the next page shows that when a noise signal is superimposed onto the positive input threshold levels of transceivers X and Y, the minimum hysteresis voltage determines at which noise level the receiver output will assume the wrong logic state. Table 1, in which the receiver parameters have been extracted from different datasheets, gives a minimum hysteresis level only for transceiver Z. For the two older transceivers, X and Y, only typical hysteresis values are provided. In a situation such as determining the minimum failsafe value for a worst-case scenario, typical values are meaningless. In fact, the TI application team has measured minimum hysteresis voltages for both transceivers X and Y that were nearly half the specified typical values.

Furthermore, there is the possibility that for a given transceiver the hysteresis window might be located anywhere between the positive and negative input thresholds. Hence, for a worst-case calculation, one must assume that the hysteresis window is at the uppermost positive

**Table 1. Receiver input sensitivities of first-, second-, and third-generation (X, Y, and Z) transceivers**

TRANSCIVER	POSITIVE-GOING INPUT THRESHOLD VOLTAGE, $V_{IT+}$ (mV)			NEGATIVE-GOING INPUT THRESHOLD VOLTAGE, $V_{IT-}$ (mV)			INPUT HYSTERESIS VOLTAGE, $V_{Hys}$ (mV)			RECEIVER OUTPUT IS INDETERMINATE WHEN
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
X (SN65LBC176)			200	-200				50		$-0.2 \text{ V} < V_{AB} < 0.2 \text{ V}$
Y (SN65HVD12)			-10	-200				35		$-0.2 \text{ V} < V_{AB} < 0.01 \text{ V}$
Z (SN65HVD72)		-70	-20	-200	-150		50	80		$-0.2 \text{ V} < V_{AB} < 0.07 \text{ V}$

threshold limit. Therefore, to determine a sufficiently high failsafe-biasing voltage, the projected peak-to-peak noise level must be added to the positive input threshold voltage:  $V_{AB(min)} = V_{IT+} + V_{N(PP\_max)}$ .

For a well-balanced bus with a noise level of  $V_{N(PP\_max)} = 50$  mV, using transceiver X requires a differential failsafe voltage of  $V_{AB(min)} = 200$  mV + 50 mV = 250 mV (Figure 1).

Operating transceiver Y at the same noise level without external biasing could be risky, particularly when considering a significantly smaller minimum hysteresis than the nominal value. Again, adding the noise level to the positive input threshold provides a minimum failsafe voltage of  $V_{AB(min)} = -10$  mV + 50 mV = 40 mV.

The more modern third-generation transceiver Z can maintain a stable output without failsafe biasing. Its positive

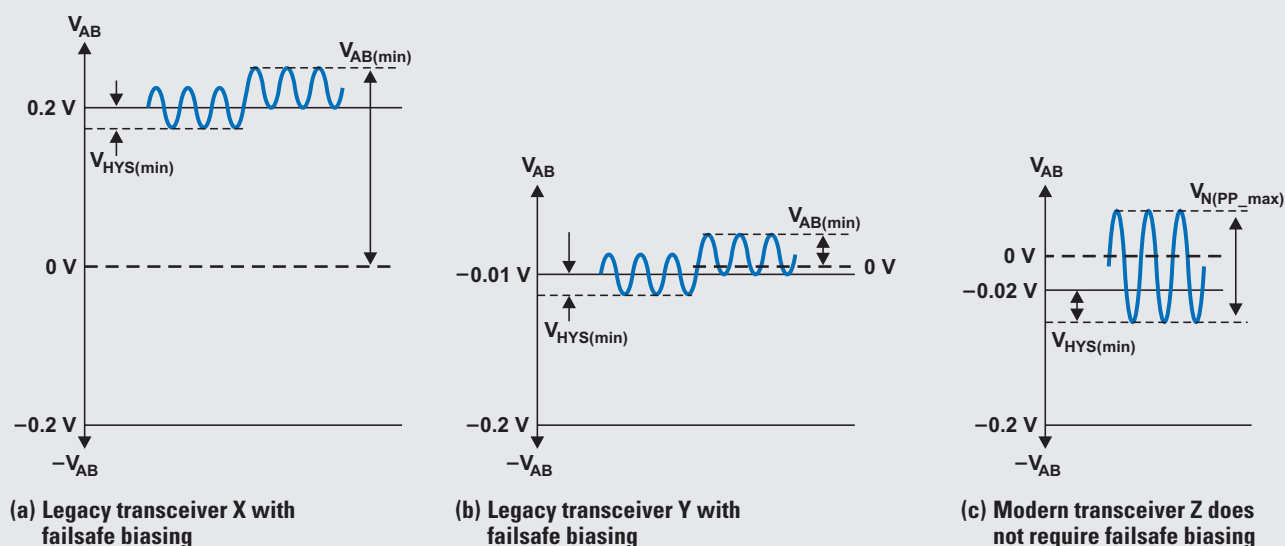
input threshold of -20 mV and the specified minimum hysteresis of 50 mV allow for a maximum peak-to-peak noise level of 140 mV, which is almost three times the noise immunity of legacy devices with external biasing.

If it is not possible to use modern transceivers, the calculation methods presented in the following section can be used to optimize the failsafe-biasing networks required by legacy transceivers.

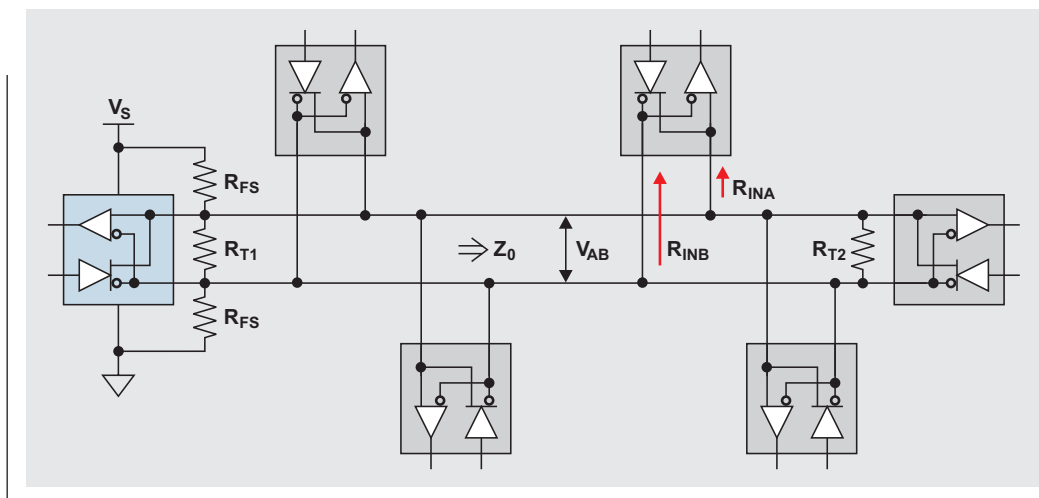
### Failsafe biasing for legacy transceivers

Figure 2 shows a terminated RS-485 bus with its distributed network nodes and a failsafe-biasing network consisting of two biasing resistors ( $R_{FS}$ ) and a termination resistor ( $R_{T1}$ ). With the majority of RS-485 applications being master/slave systems, the failsafe-biasing network is

**Figure 1. The need for failsafe biasing depends on the transceiver**



**Figure 2. RS-485 bus with failsafe-biasing network for legacy transceivers**



commonly installed at the master end of the bus, while the other cable end receives a termination resistor ( $R_{T2}$ ) matching the characteristic line impedance ( $Z_0$ ).

The major drawback of failsafe biasing is its common-mode loading. A common-mode load is the resistance between a signal conductor and the local transceiver ground. Transceivers have a high common-mode load, primarily because the receiver's input-voltage divider (Figure 3) reduces the input signal by a factor of 10 or more.

The internal resistor network, imposing a common-mode load on each of the A and B bus terminals, can be represented by a combined input resistance ( $R_{IN}$ ). The total common-mode resistance of an entire transceiver network then can be expressed through an equivalent input resistance ( $R_{INEQ}$ ) for both the A and the B line.

The RS-485 standard specifies a maximum common-mode load per bus line with  $375\ \Omega$ . Initially this value is allocated for only the bus transceivers. Implementing a failsafe-biasing network can consume a significant amount of this loading, therefore allowing only a reduced number of transceivers to be connected to the bus.

Figure 4 presents a lumped equivalent circuit of an RS-485 bus. This circuit allows the failsafe resistor values to be determined as a function of the required failsafe bus voltage ( $V_{AB}$ ), the supply voltage ( $V_S$ ), the common-mode loading caused by  $R_{FS}$  and  $R_{INEQ}$ , and the characteristic line impedance ( $Z_0$ ). Determining the currents into nodes A and B and solving for the respective line voltages ( $V_A$  and  $V_B$ ) yields

$$\frac{V_S - V_A}{R_{FS}} = \frac{V_A - V_B}{R_{T1}} + \frac{V_A - V_B}{R_{T2}} + \frac{V_A}{R_{INEQ}} \Rightarrow$$

$$V_A = R_{INEQ} \times \left[ \frac{V_S - V_A}{R_{FS}} - (V_A - V_B) \times \left( \frac{1}{R_{T1}} + \frac{1}{R_{T2}} \right) \right]$$

for Node A, and

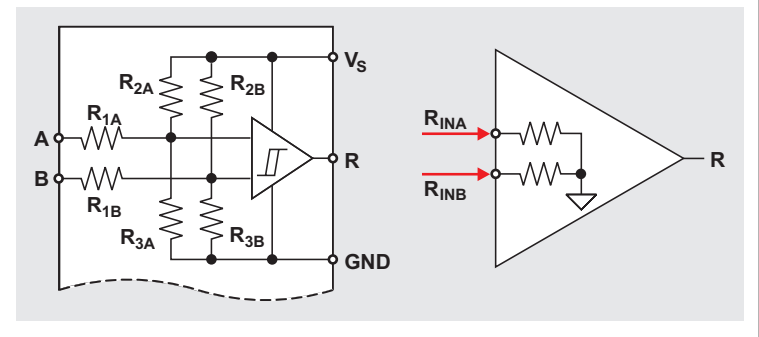
$$\frac{V_B}{R_{FS}} = \frac{V_A - V_B}{R_{T1}} + \frac{V_A - V_B}{R_{T2}} - \frac{V_B}{R_{INEQ}} \Rightarrow$$

$$V_B = R_{INEQ} \times \left[ (V_A - V_B) \times \left( \frac{1}{R_{T1}} + \frac{1}{R_{T2}} \right) - \frac{V_B}{R_{FS}} \right]$$

for Node B. Allowing for the difference between the two line voltages and assuring failsafe biasing under minimum supply conditions permits the required minimum failsafe bus voltage to be determined:

$$V_{AB(min)} = \frac{V_{S(min)}}{R_{FS}} \times \frac{1}{\frac{1}{R_{INEQ}} + \frac{1}{R_{FS}} + 2 \left( \frac{1}{R_{T1}} + \frac{1}{R_{T2}} \right)} \quad (1)$$

**Figure 3. Common-mode input resistance of the receiver section**



Because  $R_{FS}$  in combination with  $R_{INEQ}$  makes up the total common-mode load for a signal line, the parallel value of the two must not exceed the specified maximum of  $375\ \Omega$ , which is expressed through

$$R_{FS} \parallel R_{INEQ} = 375\ \Omega \text{ or } \frac{1}{R_{INEQ}} + \frac{1}{R_{FS}} = \frac{1}{375\ \Omega} \quad (2)$$

At the remote cable end, the termination resistor ( $R_{T2}$ ) must match the characteristic line impedance ( $Z_0$ ):

$$R_{T2} = Z_0 \text{ or } \frac{1}{R_{T2}} = \frac{1}{Z_0} \quad (3)$$

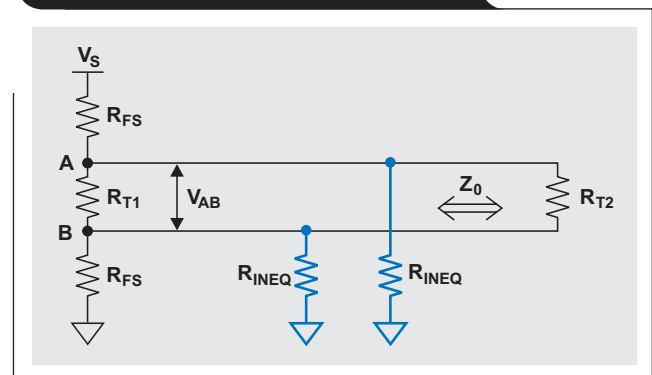
At the biasing network, the parallel combination of  $R_{T1}$  and the two failsafe resistors must also match  $Z_0$ :

$$R_{T1} \parallel 2R_{FS} = Z_0 \text{ or } \frac{1}{R_{T1}} = \frac{1}{Z_0} - \frac{1}{2R_{FS}} \quad (4)$$

Inserting Equations 2, 3, and 4 into Equation 1 then yields the bus failsafe voltage:

$$V_{AB(min)} = \frac{V_{S(min)}}{R_{FS} \left( \frac{1}{375\ \Omega} + \frac{4}{Z_0} \right) - 1} \quad (5)$$

**Figure 4. Lumped equivalent circuit**



Solving Equation 5 for  $R_{FS}$  provides the value of each failsafe-biasing resistor:

$$R_{FS} = \left( \frac{V_{S(min)}}{V_{AB(min)}} + 1 \right) \times \frac{1}{\frac{1}{375 \Omega} + \frac{4}{Z_0}} \quad (6)$$

After  $R_{FS}$  is known,  $R_{T1}$  can be derived from Equation 4. Once the failsafe network has been established, the maximum number of transceivers that can be connected to the bus can be determined through

$$n \leq \frac{12 \text{ k}\Omega}{UL_{XCVR}} \times \left( \frac{1}{375 \Omega} - \frac{1}{R_{FS}} \right), \quad (7)$$

where  $UL_{XCVR}$  is the unit-load (UL) rating of the transceiver. A typical design procedure would be to calculate  $R_{FS}$  via Equation 6 first, then determine  $R_{T1}$  via Equation 4 while making  $R_{T2} = Z_0$ . Finally, Equation 7 would be used to calculate the maximum number of bus transceivers possible.

The design examples in Table 2 show the typical design procedure. This table also highlights the differences in failsafe biasing between a network using 1-UL, 5-V transceivers (X) and one using 1/8-UL, 3.3-V transceivers (Y).

## Conclusion

Failsafe biasing with the high failsafe voltages required for first-generation transceivers causes heavy common-mode loading and necessitates a reduction in bus transceiver count. Using second-generation transceivers with less input sensitivity and lower unit loading improves the situation at low noise levels by allowing for a high transceiver count. The best of both worlds, however, can be accomplished only with modern third-generation transceivers, such as

TI's 3-V SN65HVD7x family and 5-V SN65HVD8x family. These new transceivers have the following advantages:

- They don't require an external bias resistor network that can impose heavy common-mode loading on the bus, reducing the number of transceivers that can be connected to the bus.
- Therefore they allow for up to 256 transceivers on a bus.
- They tolerate high noise levels.
- They are robust against 12-kV IEC ESD and 4-kV IEC burst transients.
- They are less expensive than legacy transceivers, and some come in much smaller packages that provide cost and space savings.
- The designer doesn't have to spend time going through a mathematical treatise like the one in this article.

## References

1. "Interface circuits for TIA/EIA-485 (RS-485)," Application Report. Available: [www.ti.com/slla036-aaj](http://www.ti.com/slla036-aaj)
2. "3.3V-supply RS-485 with IEC ESD protection," SN65HVD72/75/78 Datasheet. Available: [www.ti.com/sllse11-aaj](http://www.ti.com/sllse11-aaj)

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**Table 2. Examples of how failsafe biasing affects bus transceiver count**

TRANSCIVER X	TRANSCIVER Y
$V_{S(min)} = 4.75 \text{ V}$ , $V_{IT+} = 200 \text{ mV}$ , $UL_{XCVR} = 1 \text{ UL}$ $R_{T2} = 120 \Omega$ ( $R_{T2} = Z_0$ )	$V_{S(min)} = 3.05 \text{ V}$ , $V_{IT+} = -10 \text{ mV}$ , $UL_{XCVR} = 1/8 \text{ UL}$ $R_{T2} = 120 \Omega$ ( $R_{T2} = Z_0$ )
Assuming $V_{N(pp\_max)} = 50 \text{ mV}$ yields: $V_{AB(min)} = V_{IT+} + V_{N(pp\_max)} = 250 \text{ mV}$	Assuming $V_{N(pp\_max)} = 50 \text{ mV}$ yields: $V_{AB(min)} = V_{IT+} + V_{N(pp\_max)} = 40 \text{ mV}$
Applying Equation 6 yields: $R_{FS} = 555.5 \Omega$ . Choosing the closest E192 value makes $R_{FS} = 556 \Omega$ .	Applying Equation 6 yields: $R_{FS} = 2.11 \text{ k}\Omega$ . Choosing the closest E192 value makes $R_{FS} = 2.10 \text{ k}\Omega$ .
Applying Equation 4 yields: $R_{T1} = 134.5 \Omega$ . Choosing the closest E192 value makes $R_{T1} = 135 \Omega$ .	Applying Equation 4 yields: $R_{T1} = 123.5 \Omega$ . Choosing the closest E192 value makes $R_{T1} = 124 \Omega$ .
Applying Equation 7 yields: $n = 10 \text{ transceivers}$	Applying Equation 7 yields: $n = 210 \text{ transceivers}$

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