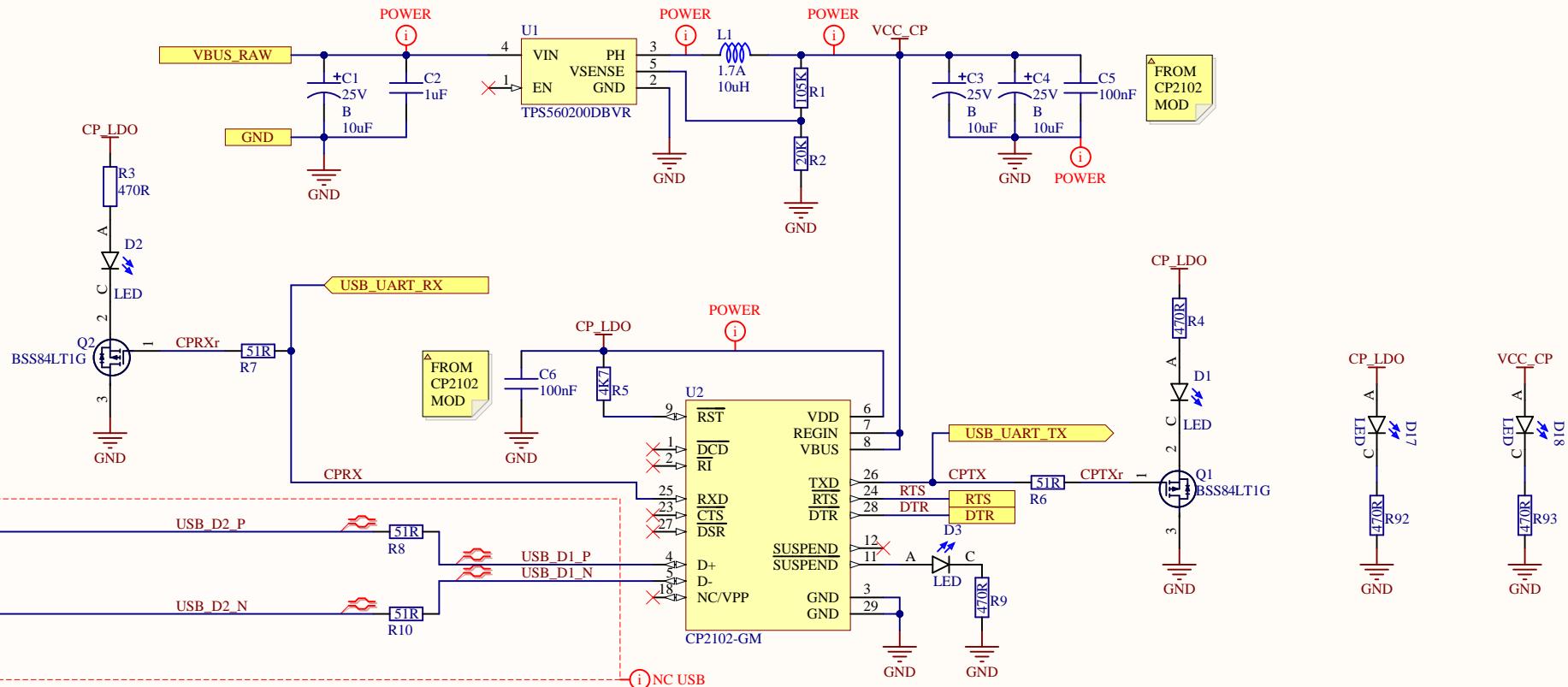


UART

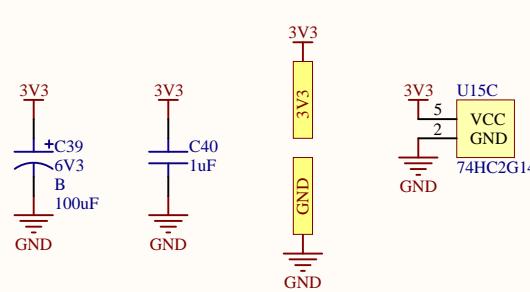


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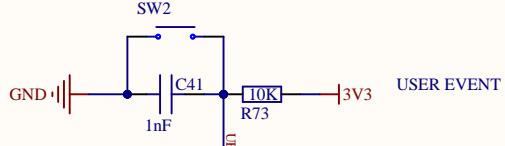
ESP32

1 2 3 4

A

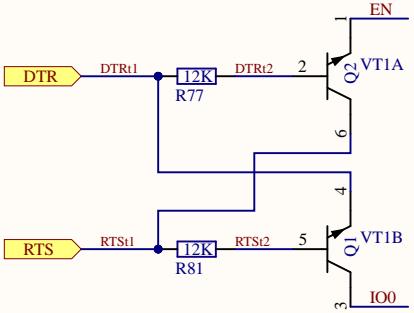


B

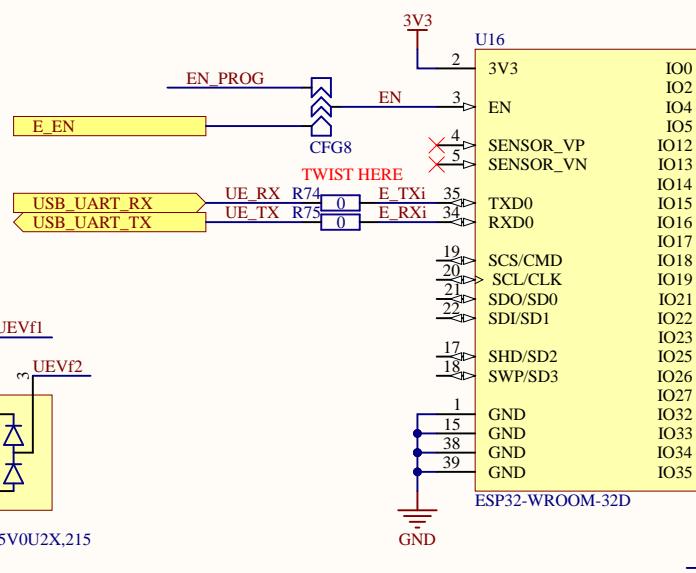


C

Auto Program
DTR RTS -> EN IO0
1 1 1 1
0 0 1 1
1 0 0 1
0 1 1 0



D



| Title | | |
|------------------------------------|-----------|----------|
| Size | Number | Revision |
| A4 | | |
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1 2 3 4

A

A B C D

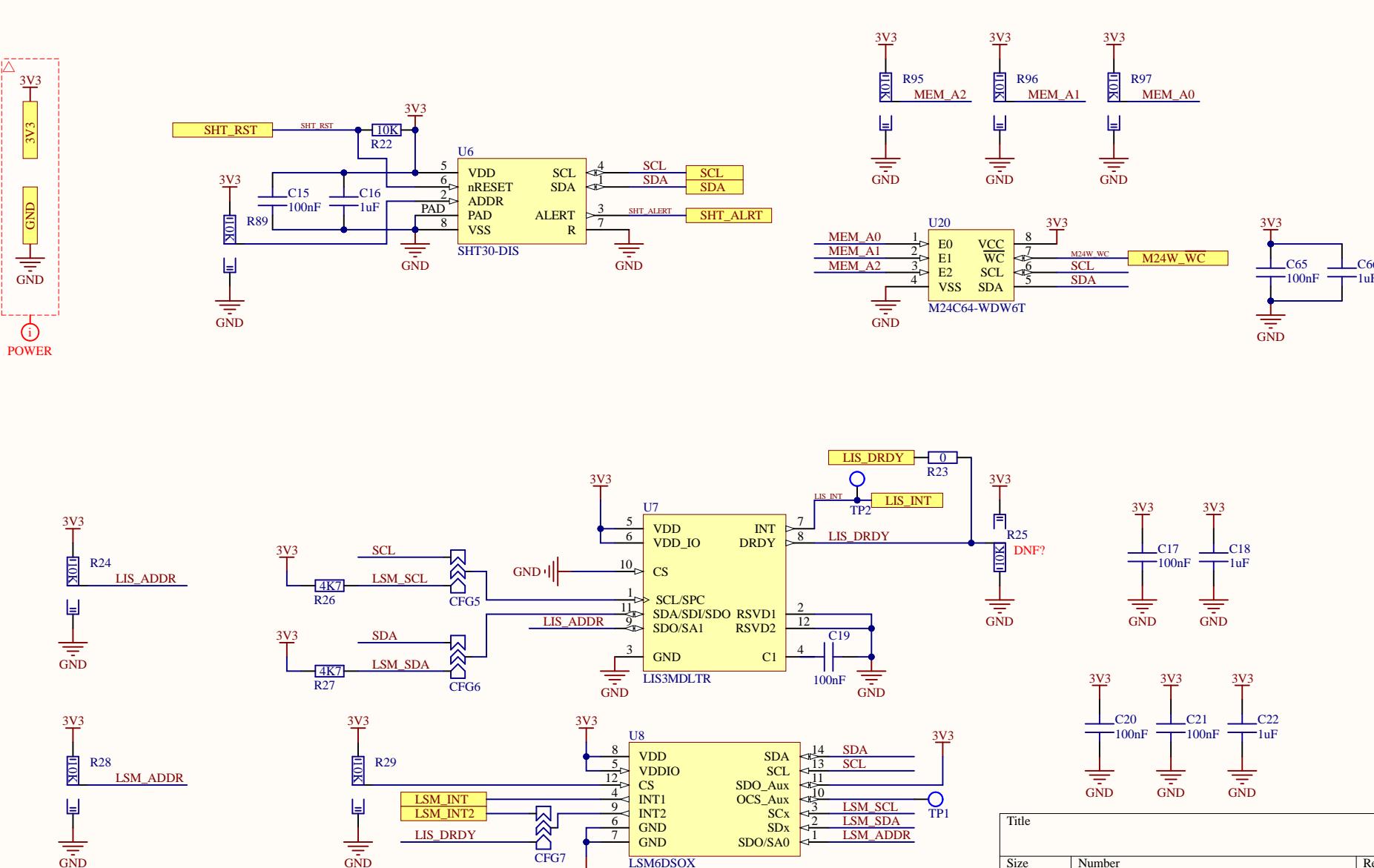
SENSORS

1

2

3

4

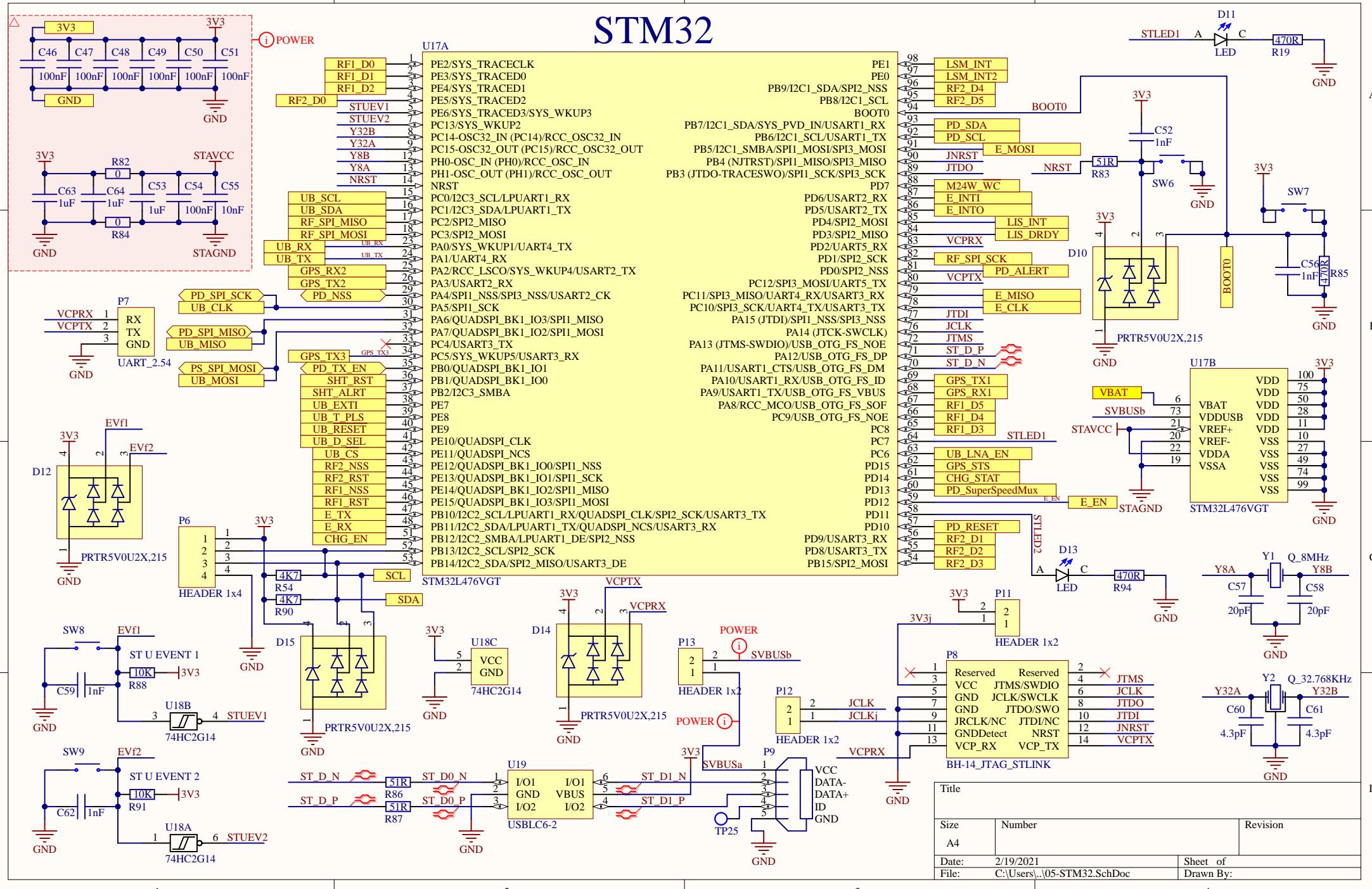


1

2

3

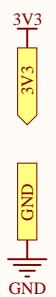
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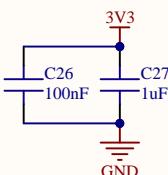
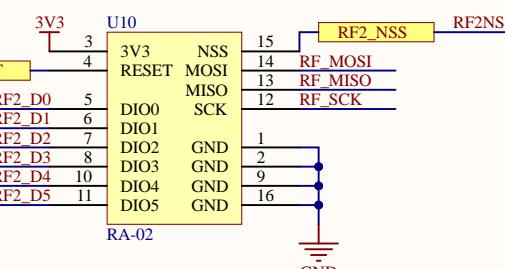
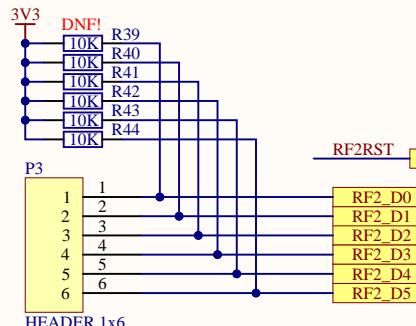
LORA

1 2 3 4

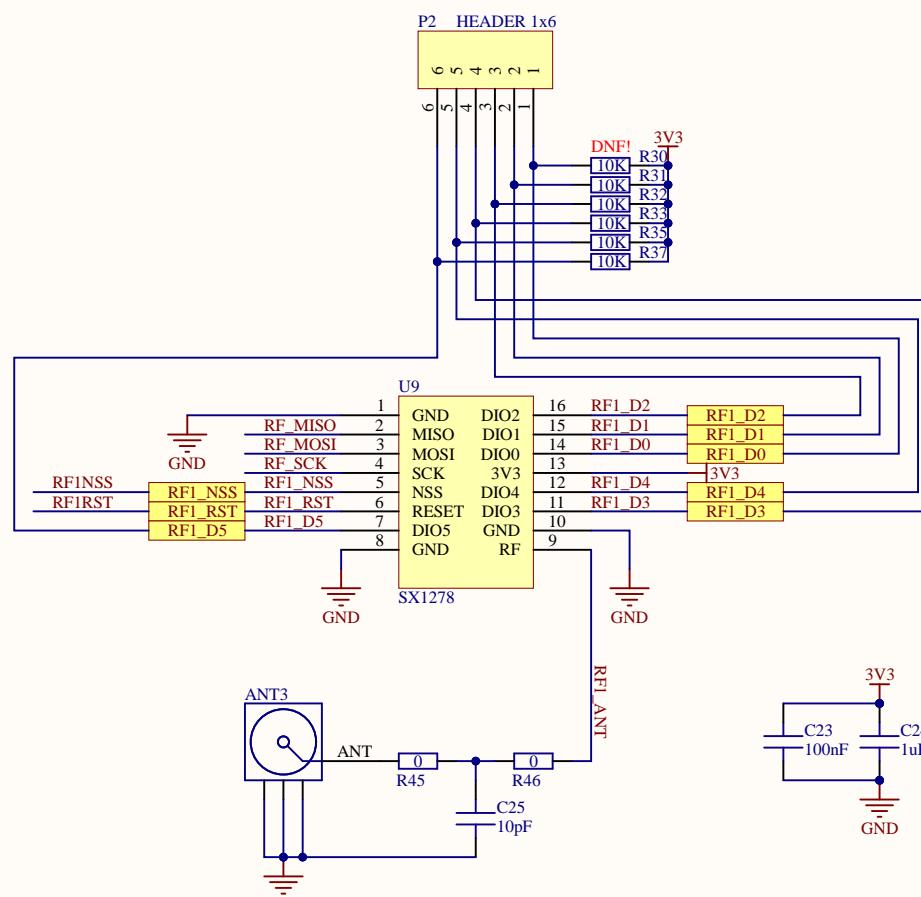
A



B



C

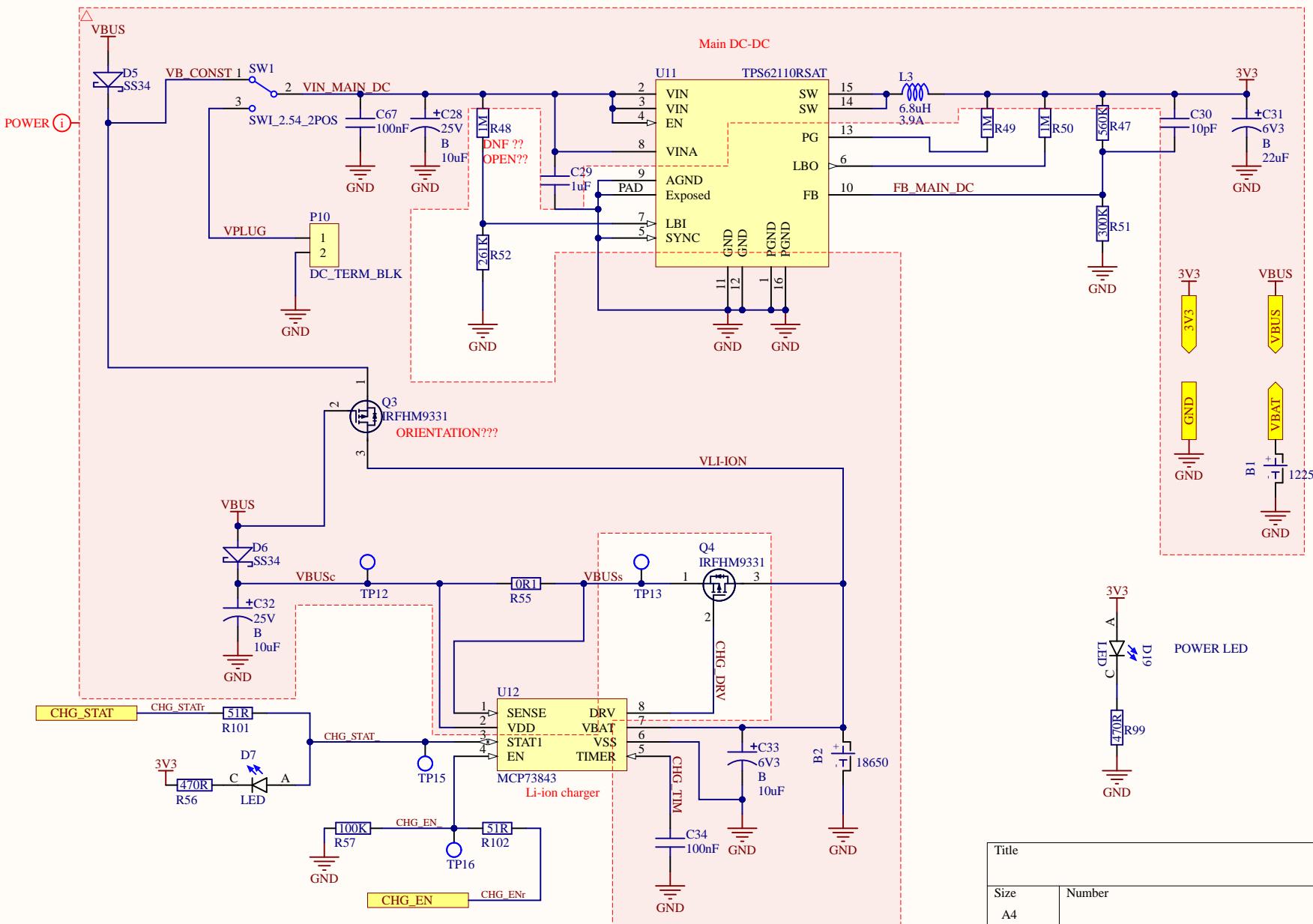


D



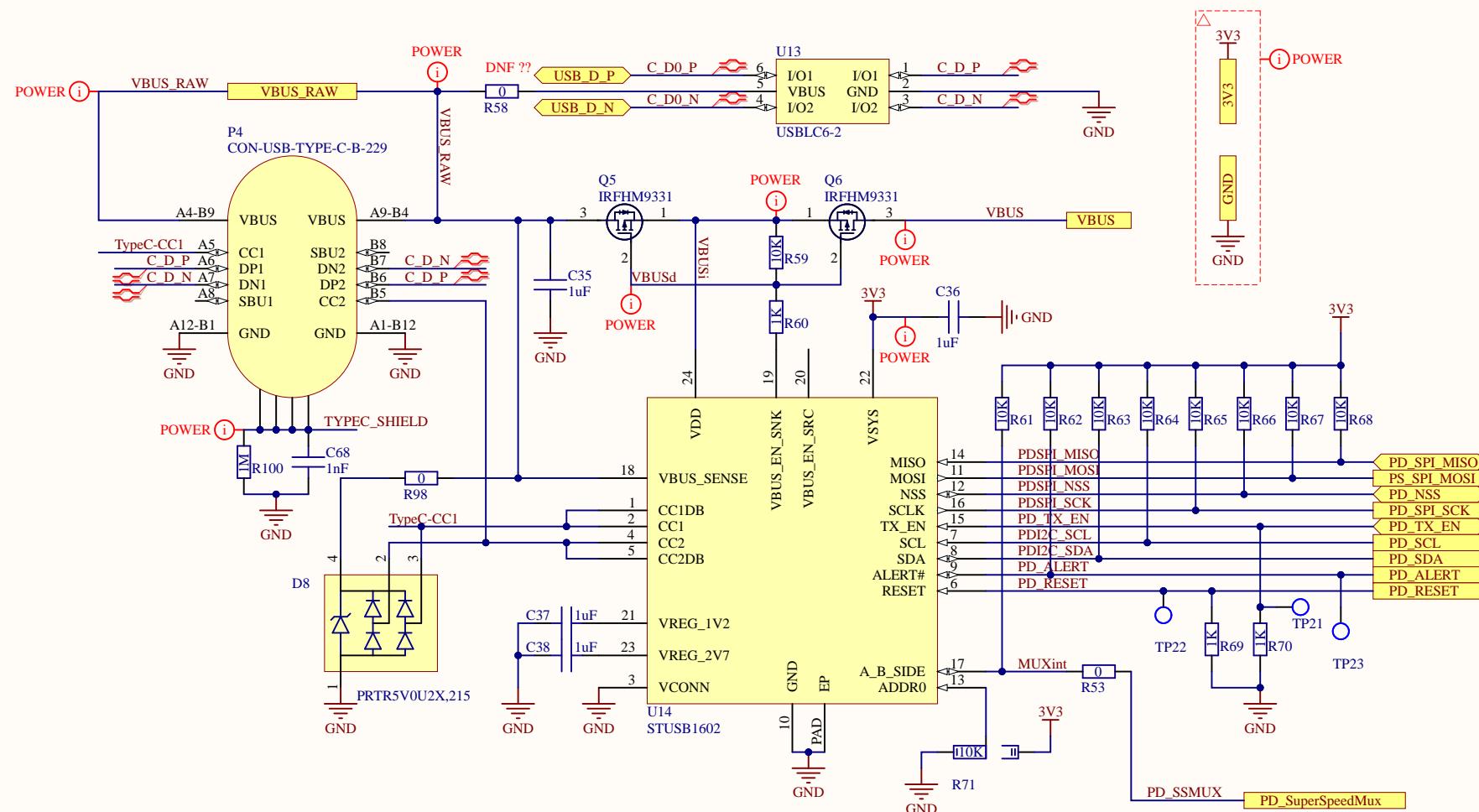
1 2 3 4

POWER



| | | |
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| Size A4 | Number | Revision |
| Date: | 2/19/2021 | Sheet of |
| File: | C:\Users\...\07-POWER.SchDoc | Drawn By: |

TYPE C PORT



| Title | | |
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| Size | Number | Revision |
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A

A

B

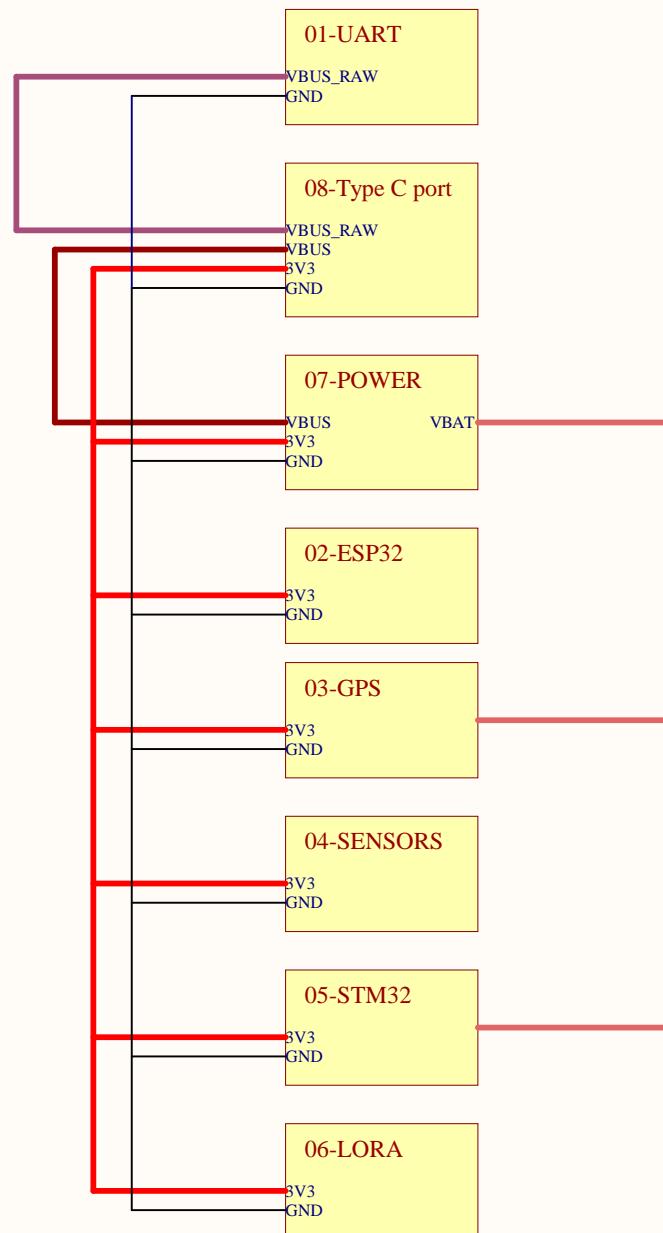
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C

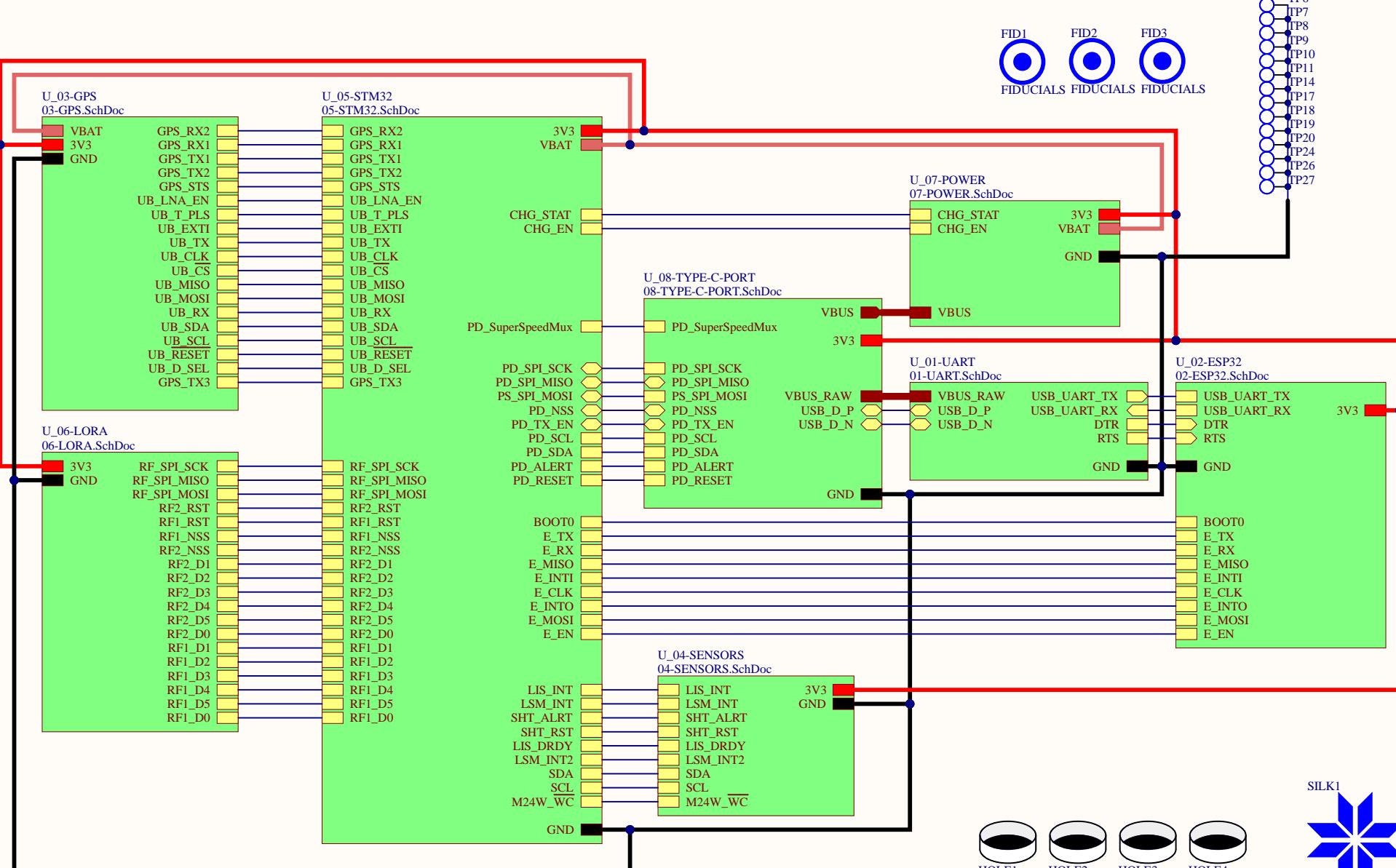
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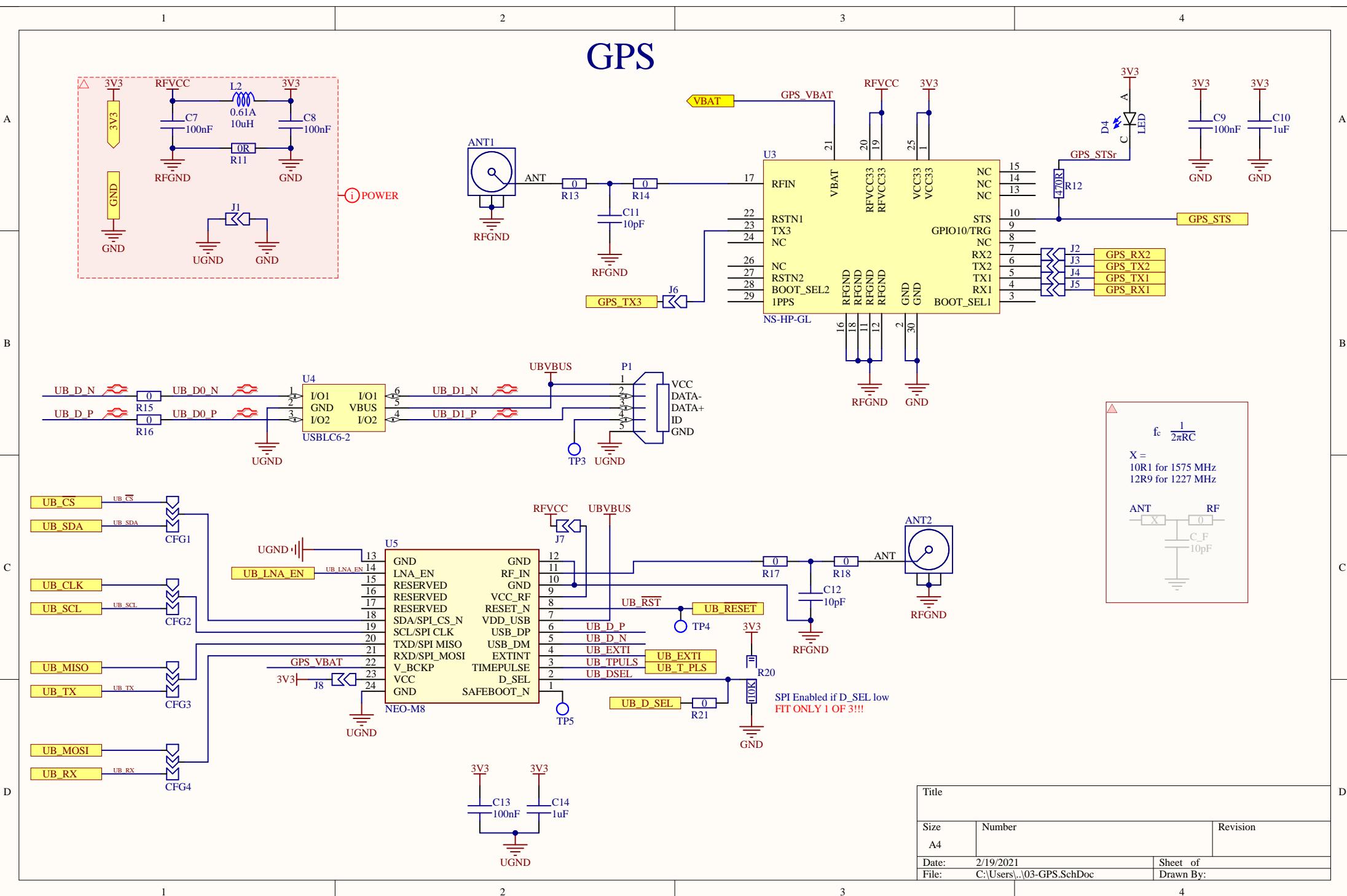
D



| Title | | |
|----------------|---|-----------------------|
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GPS



A

A

B

B

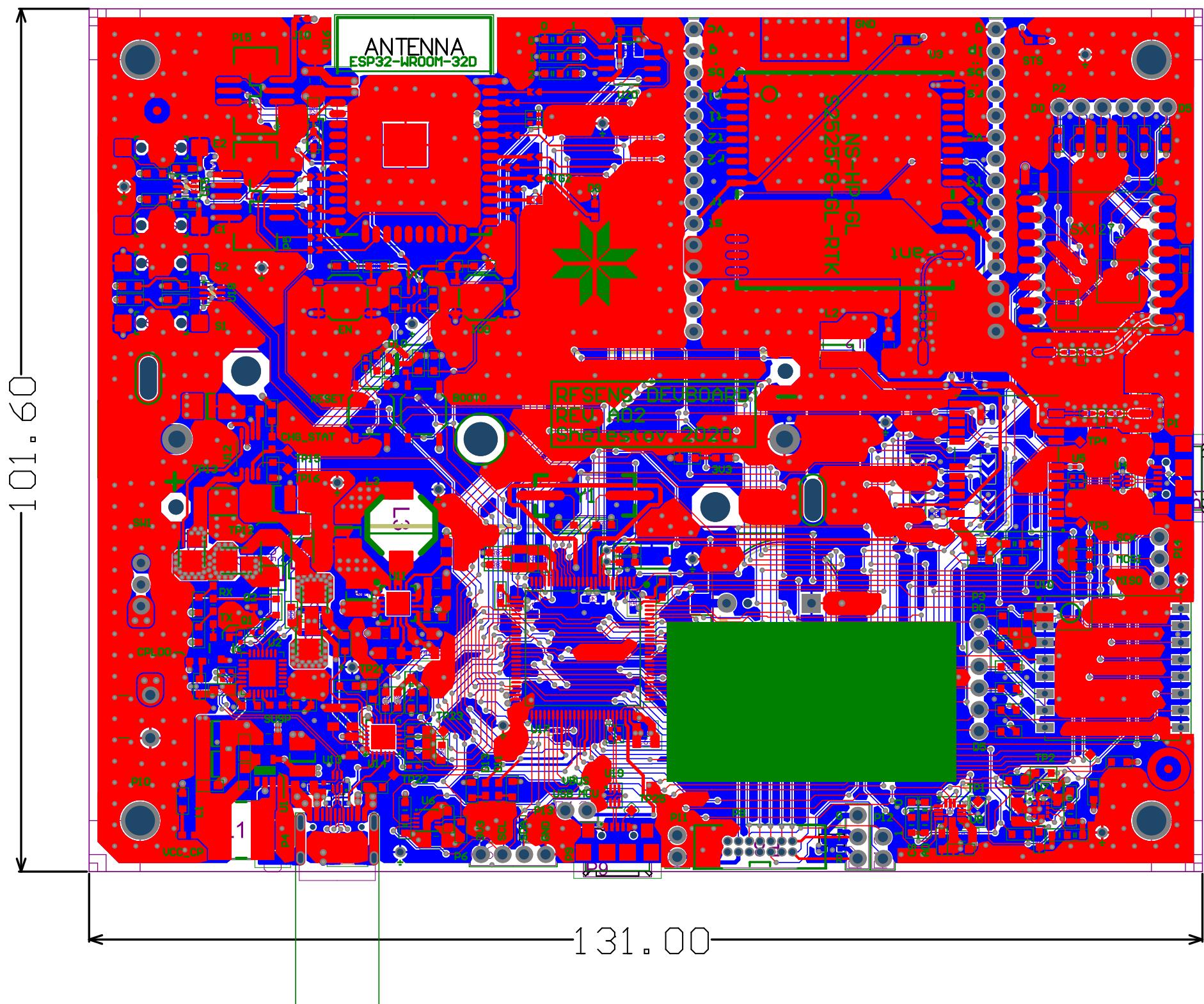
C

C

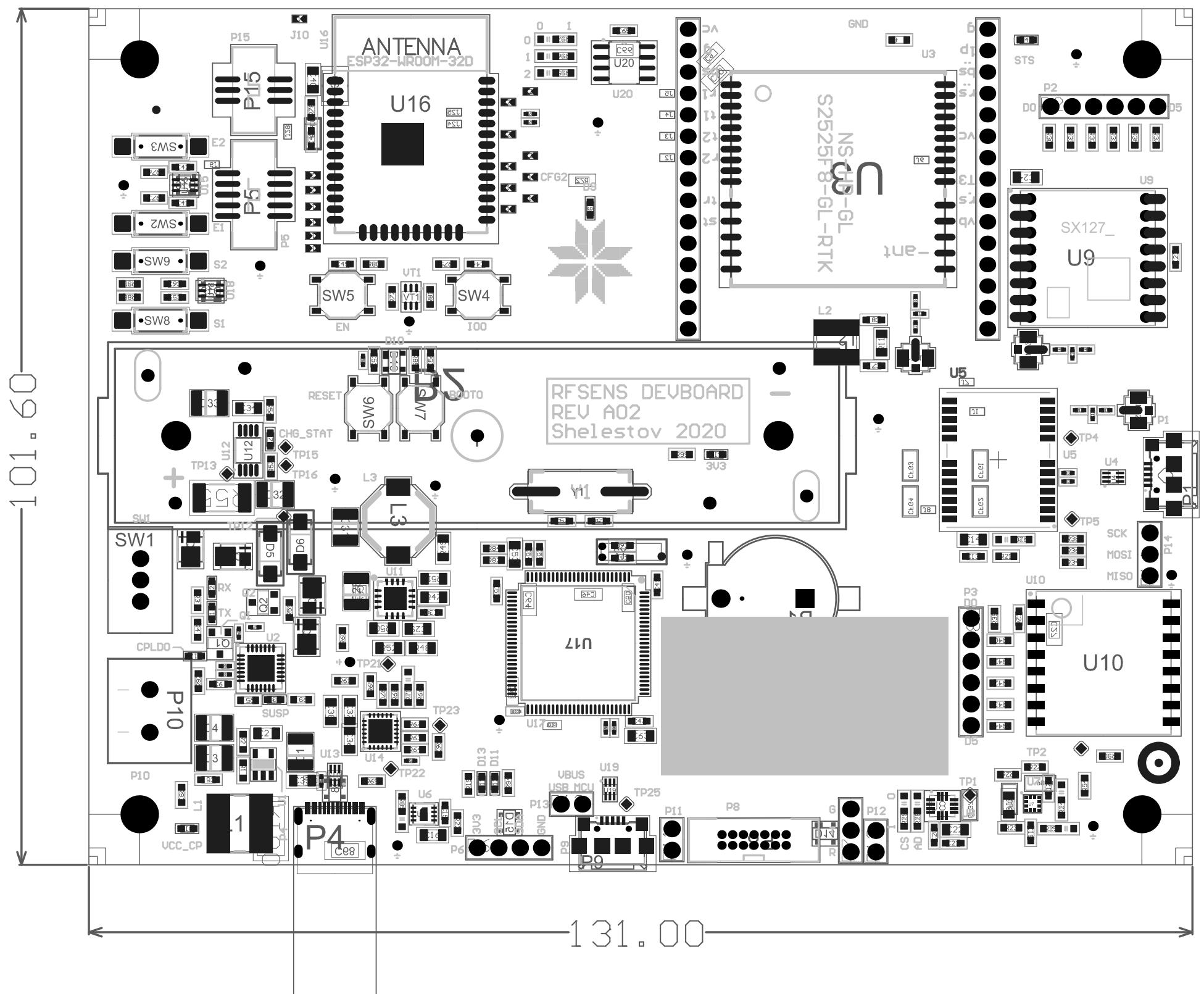
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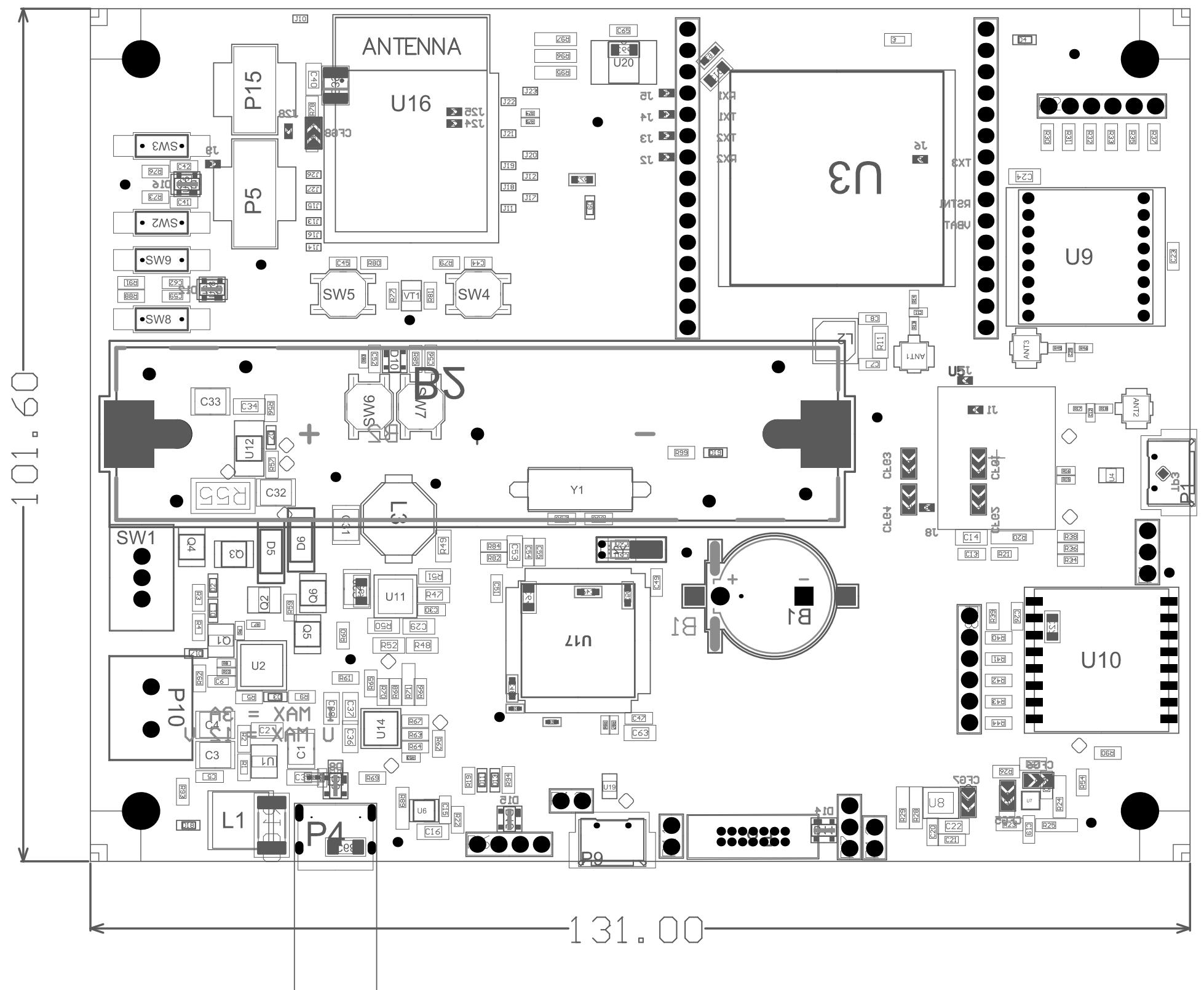
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| Title | | |
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| Size | Number | Revision |
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Board Stack Report





Board Stack Report

| Stack Up | | Layer Stack | | | |
|----------|---|----------------|---------------|-----------|----------|
| Layer | Board Layer Stack | Name | Material | Thickness | Constant |
| 1 | | Top Paste | | | |
| 2 | | Top Overlay | | | |
| 3 |  | Top Solder | Solder Resist | 0.40mil | 3.5 |
| 4 |  | TOP | Copper | 1.38mil | |
| 5 | | Dielectric 2 | PP-006 | 3.94mil | 4.2 |
| 6 |  | GND | Copper | 0.69mil | |
| 7 | | Dielectric 1 | Core-009 | 49.80mil | 4.5 |
| 8 |  | PWR | Copper | 0.69mil | |
| 9 | | Dielectric 3 | PP-006 | 3.94mil | 4.2 |
| 10 |  | BOT | Copper | 1.38mil | |
| 11 |  | Bottom Solder | Solder Resist | 0.40mil | 3.5 |
| 12 | | Bottom Overlay | | | |
| 13 | | Bottom Paste | | | |
| | Height : 62.61mil | | | | |

Design Rules Verification Report

Filename : C:\Users\strea\OneDrive\Documents\Altium\RFSENS_DEVBOARD\RFSENS-Altiu

Warnings 0
Rule Violations 0

| Warnings | |
|---|---|
| Total | 0 |
| Rule Violations | |
| Clearance Constraint (Gap=0.15mm) (All),(All) | 0 |
| Short-Circuit Constraint (Allowed=No) (All),(All) | 0 |
| Un-Routed Net Constraint (All) | 0 |
| Modified Polygon (Allow modified: No), (Allow shelved: No) | 0 |
| Width Constraint (Min=0.089mm) (Max=1.5mm) (Preferred=0.127mm) (All) | 0 |
| Width Constraint (Min=0.089mm) (Max=2.5mm) (Preferred=0.65mm) (InNetClass('POWER_NET_CLASS')) | 0 |
| Power Plane Connect Rule(Direct Connect)(Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm) | 0 |
| Hole Size Constraint (Min=0.025mm) (Max=5.08mm) (All) | 0 |
| Hole To Hole Clearance (Gap=0.254mm) (All),(All) | 0 |
| Minimum Solder Mask Sliver (Gap=0.1mm) (All),(All) | 0 |
| Silk To Solder Mask (Clearance=0.17mm) (IsPad),(All) | 0 |
| Silk to Silk (Clearance=0.254mm) (All),(All) | 0 |
| Net Antennae (Tolerance=0mm) (All) | 0 |
| Height Constraint (Min=0mm) (Max=25.4mm) (Preferred=12.7mm) (All) | 0 |
| Total | 0 |