IE University

Computer Science and Artificial Intelligence

TWO 2-BIT NUMBER ADDER

Discrete Mathematics

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Caterina Barbero, Javier Domínguez, Blanca Valdés
Juan Alonso-Allende and George Vashakidze

Contents

1 Truth table for the logical circuit

X_1	X_2	Y_1	Y_2	C	S_1	S_2
0	0	0	0	0	0	0
0	0	0	1	0	0	1
0	0	1	0	0	1	0
0	0	1	1	0	1	1
0	1	0	0	0	0	1
0	1	0	1	0	1	0
0	1	1	0	0	1	1
0	1	1	1	1	0	0
1	0	0	0	0	1	0
1	0	0	1	0	1	1
1	0	1	0	1	0	0
1	0	1	1	1	0	1
1	1	0	0	0	1	1
1	1	0	1	1	0	0
1	1	1	0	1	0	1
1	1	1	1	1	1	0

Based on the problem provided, we have four inputs that represent two two-bit numbers. Named consequently X1, X2, Y1, and Y2, where X1 and X2 represent the first two-bit number, and Y1 and Y2 the second two-bit number. The maximum possible output is 110 (because the maximum two two-bit number is 11, and 11+11 in a two-bit system is 110.) This is why we are using three two-bit numbers to describe the outcomes of the circuit. We have named C the first number of the three two-bit numbers. The remaining outputs are S1 and S2, which represent the two remaining two-bit numbers.

2 Disjunctive normal form using Boolean Algebra notation

$$C : X_1X_2Y_1Y_2 + X_1X_2Y_1\bar{Y_2} + X_1X_2\bar{Y_1}Y_2 + X_1\bar{X_2}Y_1Y_2 + X_1\bar{X_2}Y_1\bar{Y_2} + \bar{X_1}X_2Y_1Y_2$$

$$S_1 : \bar{X_1}\bar{X_2}Y_1\bar{Y_2} + \bar{X_1}\bar{X_2}Y_1Y_2 + \bar{X_1}X_2\bar{Y_1}Y_2 + \bar{X_1}X_2Y_1\bar{Y_2} + X_1\bar{X_2}\bar{Y_1}\bar{Y_2} + X_1\bar{X_2}\bar{Y_1}Y_2 + X_1X_2\bar{Y_1}\bar{Y_2} + X_1X_2Y_1Y_2$$

$$S_2 : \bar{X_1}\bar{X_2}\bar{Y_1}Y_2 + \bar{X_1}\bar{X_2}Y_1Y_2 + \bar{X_1}X_2\bar{Y_1}\bar{Y_2} + \bar{X_1}X_2Y_1\bar{Y_2} + X_1\bar{X_2}\bar{Y_1}Y_2 + X_1\bar{X_2}Y_1Y_2 + X_1X_2\bar{Y_1}\bar{Y_2} + X_1X_2Y_1\bar{Y_2}$$

3 Karnaugh maps for each output

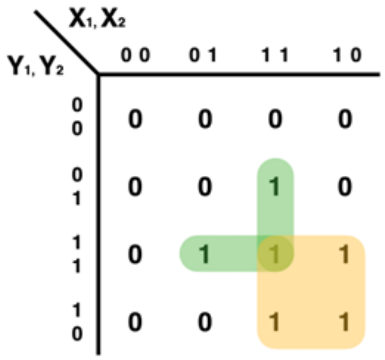


Figure 1: Output 1: Carry out (C)

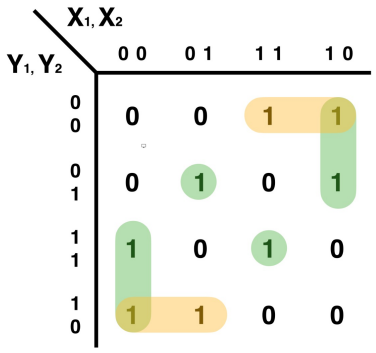


Figure 2: Output 2: Sum 1 (S_1)

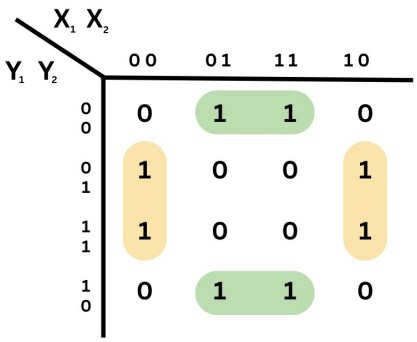


Figure 3: Output 3: Sum 2 (S_2)

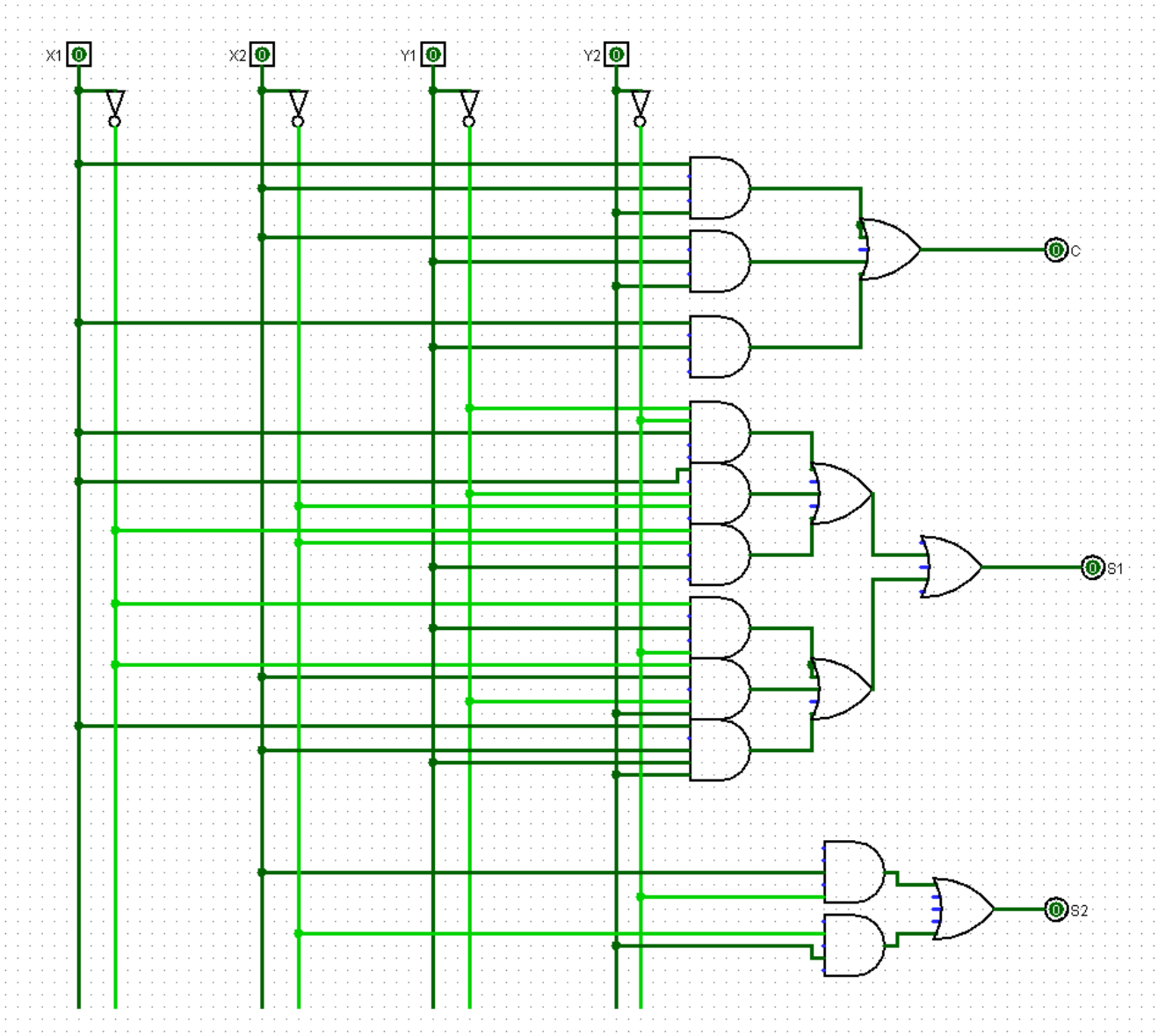
4 Minimal logical expression for each output

$$C : X_1X_2Y_2 + X_2Y_1Y_2 + X_1Y_1$$

$$S_1 : X_1\bar{Y}_1\bar{Y}_2 + X_1\bar{X}_2\bar{Y}_1 + \bar{X}_1\bar{X}_2Y_1 + \bar{X}_1Y_1\bar{Y}_2 + \bar{X}_1X_2\bar{Y}_1\bar{Y}_2 + X_1X_2Y_1Y_2$$

$$S_2 : X_2\bar{Y}_2 + \bar{X}_2Y_2$$

5 Image of the circuit



6 Truth table generated by Logisim

X1	X2	Y1	Y2	C	S1	S2
0	0	0	0	0	0	0
0	0	0	1	0	0	1
0	0	1	0	0	1	0
0	0	1	1	0	1	1
0	1	0	0	0	0	1
0	1	0	1	0	1	0
0	1	1	0	0	1	1
0	1	1	1	1	0	0
1	0	0	0	0	1	0
1	0	0	1	0	1	1
1	0	1	0	1	0	0
1	0	1	1	1	0	1
1	1	0	0	0	1	1
1	1	0	1	1	0	0
1	1	1	0	1	0	1
1	1	1	1	1	1	0

7 Karnaugh maps generated by logism

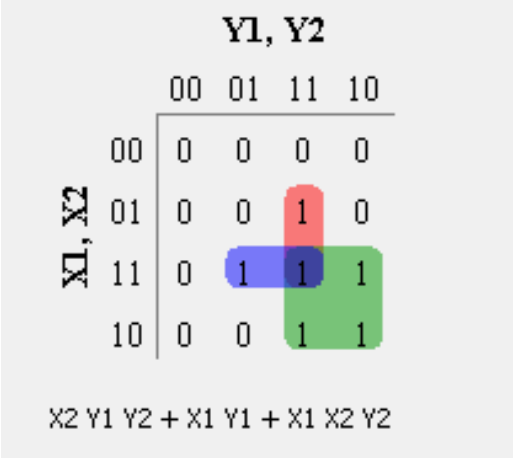


Figure 4: Output 1: Carry out (C)

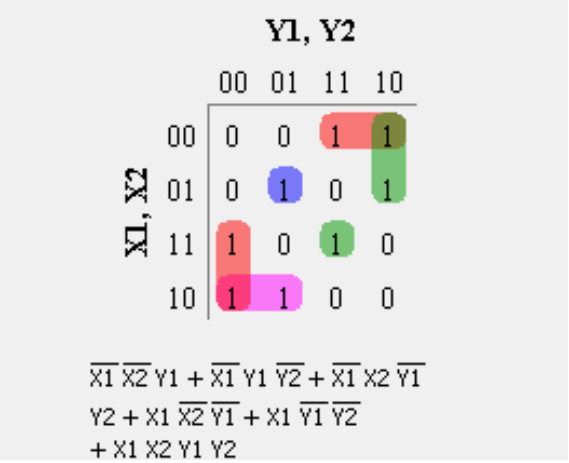


Figure 5: Output 2: Sum 1 (S_1)

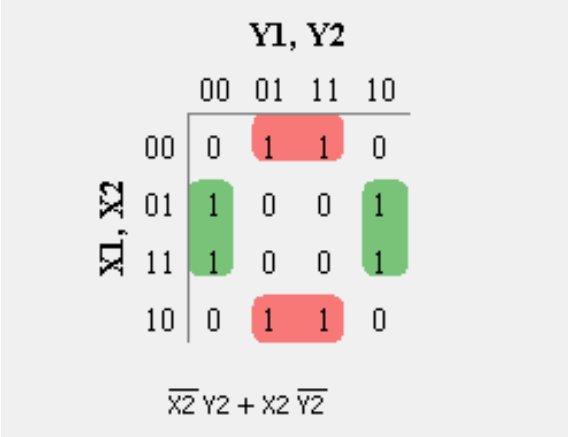


Figure 6: Output 3: Sum 2 (S_2)

Bibliography

[G] González, J. *Introduction to Karnaugh maps* (2019). The Organic Chemistry Tutor. [Video] YouTube. `https://www.youtube.com/watch?v=RO5alU6PpSU`

[R] Rosen, K. (2012) *Discrete mathematics and its applications*. New Delhi: McGraw-Hill. **p**p. 866-872.