# EDP/16

## Architecture

Educational Demonstration Processor is a simulated processor architecture designed for teaching the Computer Science specification in the UK. It is based on the BEP/16 as well as the x86 architecture, albeit modified to be more suitable.

The processor is 16 bit, with 10 general purpose registers as well as a collection of more particular registers.

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| --- | --- | --- |
| Register | Register Address | Purpose |
| R0-R9 | 0-9 | General purpose registers are used by the programmer in their application. |
| Program Counter PC | 13 | By the Execute part of the cycle, stores the address of the next instruction. A jump can be carried out by setting this value manually. |
| Flag Register FR | 14 | Stores various flags for use by the programmer. |
| Stack Pointer SP | 15 | Points to the current stack top |

Instructions are 16 bits long and follow the following format:

2 bits addressing mode (A)  
6 bits operation (O)  
4 bits register reference 1 (R)  
4 bits register reference 2 (r)  
8 bits operand (p)

AAOOOOOORRRRrrrrPPPP

## Assembly

### Instructions

|  |  |  |
| --- | --- | --- |
| Mnemonic | Operation | Format |
| ADD | Adds two integers, result is stored in the accumulator. | ADD reg1, reg2  ADD reg1, immed |
|  |  |  |