3T DRAM

➢ DRAM TECHNOLOGY

DRAM architectures describe how transistors and capacitors are arranged to store and access data bits.

The traditional **1T DRAM** cell uses a single transistor and capacitor, offering the smallest size but relying heavily on periodic refresh due to charge leakage.

The 3T DRAM cell adds extra transistors, which allows for:

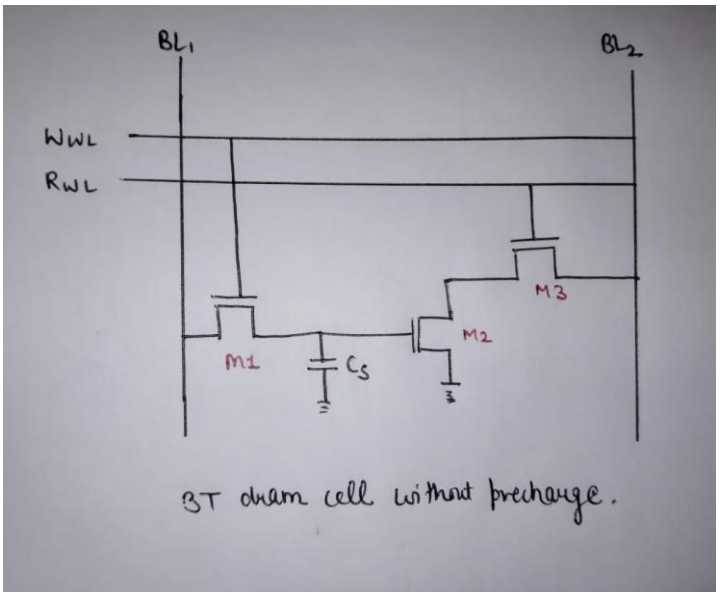
• **Higher noise margin** — the stored data is more resilient against voltage fluctuations or interference.

• **Better retention** — reduced leakage means the stored bit lasts longer without refreshing.

However, this comes at a cost: more transistors make the cell physically larger, which can reduce how many bits fit on a chip. Despite the size increase, in applications where stability and low power refresh matter more than maximum density, 3T DRAM still supports high-density integration, especially in embedded systems and specialized processors.

➢ 3T DRAM Cell Architecture

The 3T DRAM cell is composed of three transistors labelled M1, M2 (access transistors), and M3 (storage transistor).



• **Access Transistors (M1, M3):** These transistors act as switches controlled by word lines (WL) to enable reading from or writing to the storage node. When enabled, they connect the storage node to the bit lines (BL), allowing data transfer.

• **Storage Transistor (M2):** This transistor works as a gated diode, which holds the charge representing the stored bit in its gate capacitance rather than a separate capacitor.

• **Bit Lines (BL) and Word Lines (WL):** The bit lines carry data in and out, while the word lines select which cell to access by controlling the gate voltage of the access transistors.

• **Voltage References (Vdd) and Clock Signals**: These provide the necessary power and timing signals to coordinate read and write cycles precisely

➢ Working of 3T DRAM

The working of a 3T DRAM cell can be understood as follows:

• Data is stored as charge on the storage node (S node), represented by the voltage level on the gate capacitance of the storage transistor (M2).

• During a **write operation**, the word line (WL) connected to the write access transistor (M1) is activated, enabling a conduction path from the write bit line (BL) to the storage node.

• The voltage corresponding to the desired logic state (0 or 1) is transferred from the bit line to the storage node, charging or discharging it accordingly.

• In a **read operation**, the read word line activates the read access transistor (M3), which connects the storage node to the read bit line.

• The read bit line is precharged to a high voltage (typically Vdd) before the read; if the storage node holds a high charge (logic 1), it discharges the read bit line, causing the sense amplifier to detect a voltage drop.

• If the stored bit is logic 0, the read bit line stays near the precharged level, and the sense amplifier detects no significant change.

• The read operation is non-destructive, which means the stored charge at the storage node is not lost during reading, unlike in 1T1C DRAM cells.

• The stored charge leaks over time due to transistor leakage currents, so the cell retains data only for a finite retention period.

• To maintain data integrity, **periodic refresh cycles** are required, recharging the storage node to the correct voltage level.

• The timing and voltage pulses on the WL, BL, and clock signals control these write, read, and refresh operations for reliable memory access

➢ Explanation of circuit using Precharge

1. ***Precharge:***

   PC (precharge) is connected to two PMOS (M5,M6).

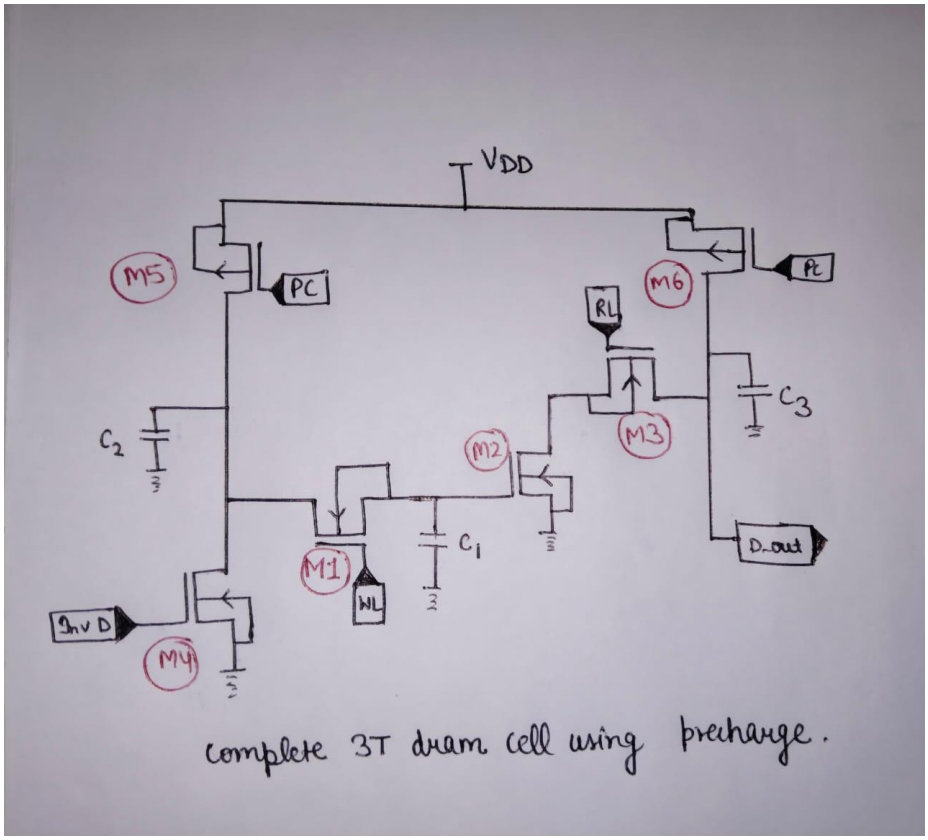
   When PC is LOW(0) -> PMOS ON

   PC is HIGH(3.3) -> PMOS OFF.

So when M5 & M6 turns ON ,they charges both bitlines to VDD.

M1 & M3 OFF -> No read or write access.

C2 & C3 charged to VDD(1.35V).



2. ***Working of M4:***

Inv_D (inverse_data) is applied to M4 which is the input for our circuit.

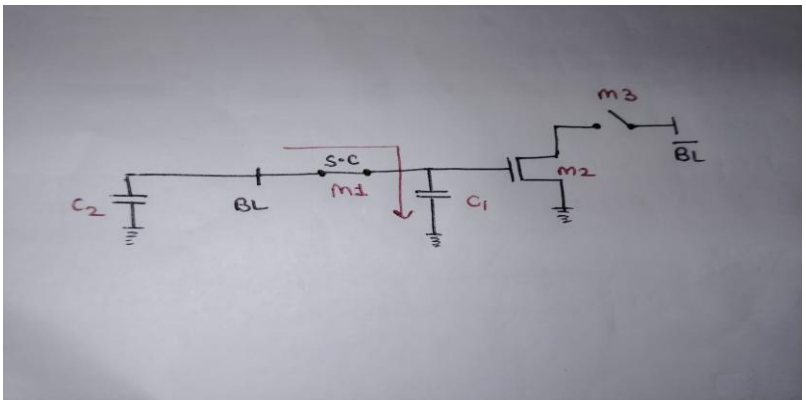
CASE I : When Inv_D = High(3.3V) -> M4 ON.
M4 conducts, pulls the storage node down to GND.
Allows us to write logic '0' to internal node.

CASE II : When Inv_D = LOW(0V) -> M4 OFF
M4 does not conduct, the internal node is not connected to GND.
Internal node can be charged via the bitline path. Allows us to write logic '1' to internal node.

3. ***Writing 1:***

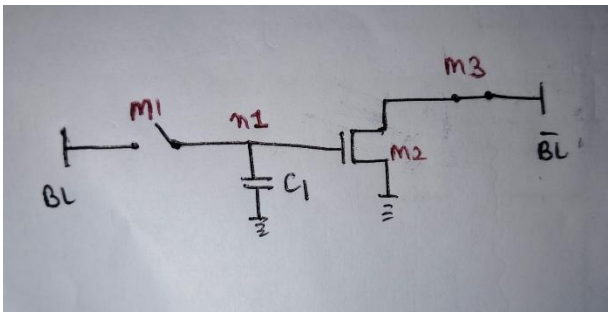
PC -> HIGH -> M5 & M6 OFF -> Precharge disabled
WL -> HIGH ->M1 ON -> Connects bitline to internal node.
Inv_D -> LOW -> M4 OFF -> Internal node is not pulled to GND.

Bitline was charged to 1.35V. This will charge up the internal node. Logic '1' is written.



4. ***Read :***

PC -> HIGH -> M5 & M6 OFF
WL -> LOW -> M1 OFF
RL -> HIGH -> M3 ON -> Connects storage node to C3.
Internal node either HIGH or LOW depending on what was written.



CASE 1: If n1 =1 then M2 turns ON and behave as short circuit. Then BL~ is connected to GND .

BL~ = 0 , therefore Dout =0.

CASE 2: If n1 = 0 then M2 turns OFF and behave as Open circuit. Then BL~ is equal to 1 because of precharge capacitor connected to BL~.

BL~ = VDD, therefore Dout = 1.

➢ Key features of the 3T DRAM cell:

• **Non-destructive Read:** The read operation in 3T DRAM does not destroy the stored data, unlike in classic 1T1C DRAM cells, improving reliability during access cycles.

• **Storage Using Transistor Gate Capacitance:** Instead of a separate capacitor, 3T DRAM uses the gate capacitance of the storage transistor as the storage node, simplifying fabrication and reducing cell size.

• **Retention Time**: Typical retention times are in the range of milliseconds, requiring periodic refresh but sufficient for many embedded and low-power use cases.

• **Fast Write and Read Speed:** Operations occur within nanoseconds, enabling high-speed access comparable to some SRAM designs**.**

• **Power Efficiency:** Lower power consumption due to absence of dedicated capacitors and efficient cell design.

• **Higher Density than SRAM:** 3T DRAM cells occupy less area than SRAM, allowing more memory cells per unit area, which is advantageous for embedded memory applications.

➢ Applications

3T DRAM is suited for:

• High-speed caches in processors

• Embedded systems

• Mobile devices requiring low refresh currents

• Low-cost memory in consumer electronics, optimizing price performance trade-offs

• Next-generation advanced integrated circuits using emerging technologies like FinFET to reduce leakage and improve scalability