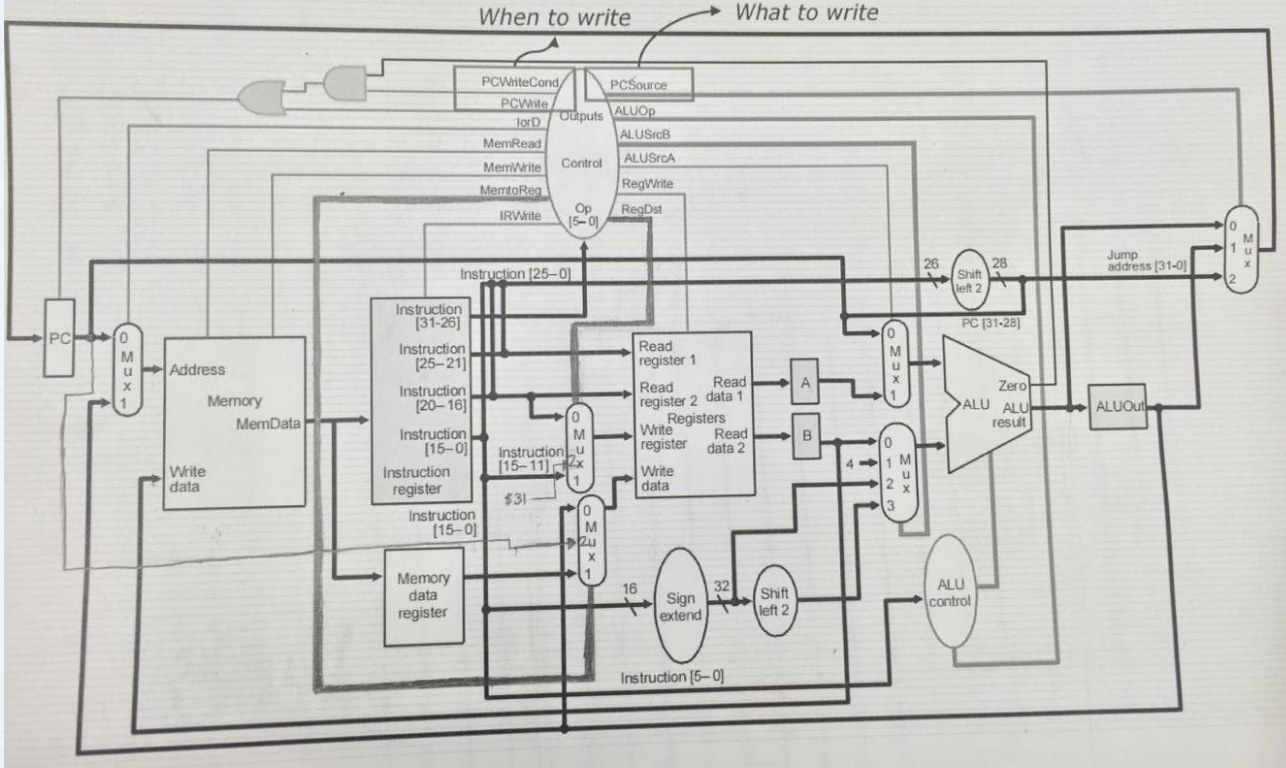
**Design: Modifications to the Data path**



For a jal instruction. RegDst is 10 and MemtoReg is 10, this enables $31 to be set to the PC+4 value. This results in the following changes:

* RegDst becomes a 2-bit signal. In turn, this means the RegDst mux becomes a 2-bit mux. Thus, the RegDst mux has three options: Rd, Rt, and $31.
* MemtoReg becomes a 2-bit signal. This is necessary because PC + 4 needs to be one of the possible write values (it is written into $31 for jal instructions). This signal comes from PC, because PC updates to PC+4 during the fetch state. In turn, the MemtoReg mux has PC+4 as an option.

**Verification: Results from a test program**

Test Program (from IFETCH.vhd):

X"00222020", -- add $4, $1, $2

X"0c000003", -- jal label1

X"00832820", -- add $5, $4, $3

X"00643020", -- label1: add $6, $3, $4

X"0c000006", -- jal label2

X"00c33820", -- add $7, $6, $3

X"00c34020", -- label2: add $8, $6, $3

X"0c000009", -- jal endlabel

X"01034820", -- add $9, $8, $3

X"01035020", -- endlabel: add $10, $8, $3

X"00000000",

X"00000000",

X"00000000",

X"00000000",

X"00000000",

X"00000000"

