DACSYS

Digital **A**nalog **C**onverter **Sys**tem

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Specification Sheet

Content

Introduction

The DACSYS operates as a standalone audio system, providing high resolution audio and minimalistic interface.

Audio can either be streamed via Bluetooth, WLAN (DLNA) or USB to the DACSYS and will then be converted to analog stereo audio.

The system is designed to offer the highest flexibility regarding further development to perfectly integrate the system in its environment while offering unexceptional high-quality hardware components.

Characteristics

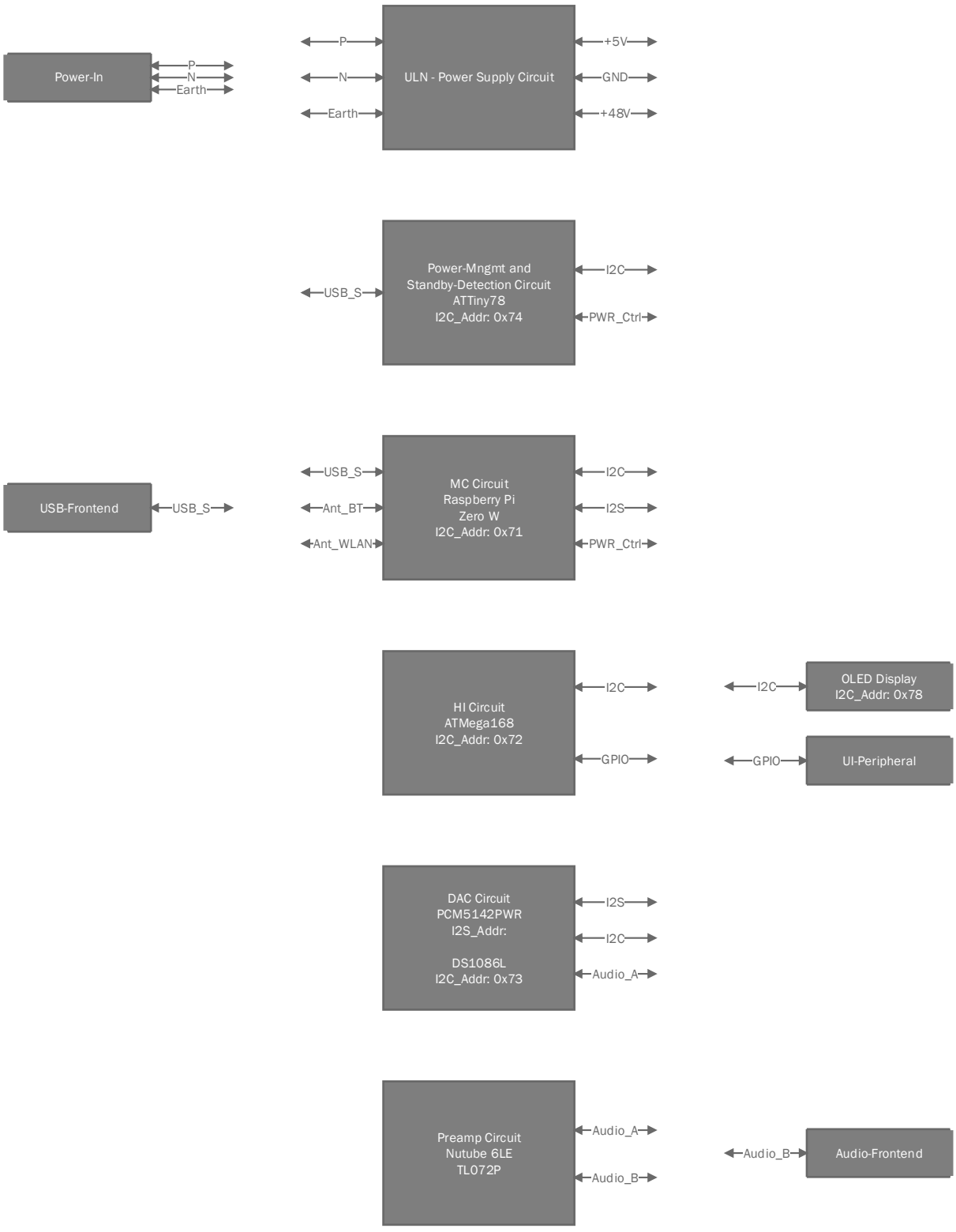
	Minimum	Average	Maximum
Bandwidth [Hz] (-3dB)	1		30k
Output voltage [mv] (RMS)	0		2100
Resolution [bit]	16		32
Sampling rate [kHz]	8		384
Dynamic Range [dB]		112	
Line Out Resistance [Ω]	1k		
Total Harmonic Distortion [dB]		-93	
Signal Noise Ratio [dB]		112	
Latency (WIFI)*			
Latency (Bluetooth)*			
Latency (USB)*			
Power Consumption			

*Values based on measurements, which may be influenced by individual setup

Table 0-1

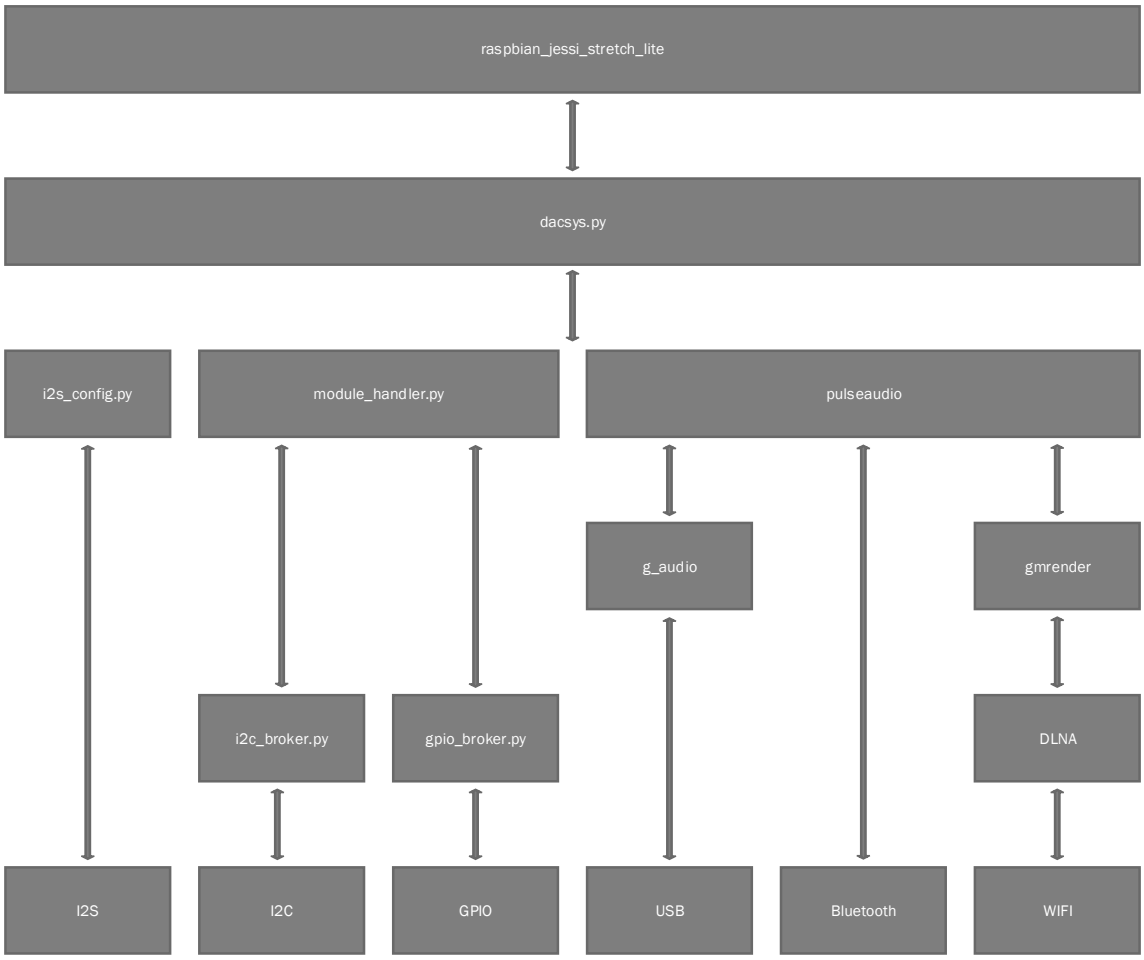
Overview

The following figure gives a general overview about the system modules.



Raspberry Pi Zero W

The following section describes the functionality and software architecture of the main control unit (MCU) and their interaction with other modules.



Technical Information

I2C Register Mapping

The DACSYS uses an I2C bus to communicate between the main control unit (MCU), the peripheral control unit (PCU) and other modules.

Addressing

The following table shows address and registers of the several devices.

Device	**Address**	**Register**
Raspberry PI Zero	0x71	[Master]
ATMega168-PU	0x72	0x00-0x3
DS1086L	0x73	
ATTiny28	0x74	

SS1780D	0x78	

Table 0-1

Register Summary

ATMega168-PU

The following table shows the register allocation for the human interface and peripheral control device ATMega168-PU.

Register	***Binary***								***Description***
0x00	X	X	X	X	X	X	X	X	SYSINF
0x01	P1	P2	P3	P4	P5	P6	P7	P8	PERIPHCTRL
0x02	b0	b1	b2	b3	b4	b5	b6	b7	RELENC
0x03	S1	S2	X	X	X	X	X	X	ABSSW
0x04	1b0	1b1	1b2	1b3	2b0	2b1	2b2	2b3	RELNUMSW

Table 0-2

DS1086L

The following table shows the register allocation for the clocking device DS1086L.

Register	***Binary***								***Description***
0x02	JS4	JS3	JS2	JS1	JS0	LO/HiZ	P3	P2	PRESCALER
	P1	P0	X_x	X_x	X_x	X_x	X_x	X_x	PRESCALER
0x08	b9	v8	b7	b6	b5	b4	b3	b2	DAC(MSB)
	b1	b0	X_0	X_0	X_0	X_0	X_0	X_0	DAC(LSB)
0x0E	X_1	X1	X1	b4	b3	b2	b1	b0	OFFSET
0x0D	X_1	X_1	X_1	X_1	WC	a2	a1	a0	ADDR
0x37	X_x	X_x	X_x	b4	b3	b2	b1	b0	RANGE
0x3F									WRITE EE

Table 0-3

ATTiny78

The following table shows the register allocation for the power supply control device ATTiny78.

SS1780D

(See datasheet for detailed description)

Schematics

Circuit