序号	指令	类型	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	功能	ALUOp
1	ADDIU	I	01001					rx			immediate								R[x] <= R[x] + SignExtend(immediate)	ALUOp_ADD
2	ADDIU3	I	01000					rx			ry			0	immediate				R[y] <= R[x] + SignExtend(immediate)	ALUOp_ADD
3	ADDSP	I	01100					011			immediate								SP <= SP + SignExtend(immediate)	ALUOp_ADD
4	ADDU	R	11100					rx			ry			rz			01		R[z] <= R[x] + R[y]	ALUOp_ADD
5	AND	R	11101					rx			ry			01100					R[x] <= R[x] & R[y]	ALUOp_AND
6	B	B	00010					immediate											PC <= PC + SignExtend(immediate)	ALUOp_BNOP
7	BEQZ	B	00100					rx			immediate								if (R[x] = 0) then PC <= PC+SignExtend(immediate)	ALUOp_BEQZ
8	BNEZ	B	00101					rx			immediate								if (R[x] != 0) then PC <= PC+SignExtend(immediate)	ALUOp_BNEZ
9	BTEQZ	B	01100					000			immediate								if (T = 0) then PC <= PC+SignExtend(immediate)	ALUOp_BEQZ
10	CMP	R	11101					rx			ry			01010					if (R[x] = R[y]) then T <= 0 else T <= 1	ALUOp_SNE
11	JR	J	11101					rx			00000000								PC <= R[x]	ALUOp_ADD
12	LI	I	01101					rx			immediate								R[x] <= ZeroExtend(immediate)	ALUOp_ADD
13	LW	I	10011					rx			ry			immediate					R[y] <= MEM[R[x] + SignExtend(immediate)]	ALUOp_ADD
14	LW_SP	I	10010					rx			immediate								R[x] <= MEM[SP + SignExtend(immediate)]	ALUOp_ADD
15	MFIH	R	11110					rx			00000000								R[x] <= IH	ALUOp_ADD
16	MFPC	R	11101					rx			01000000								R[x] <= PC	ALUOp_ADD
17	MTIH	R	11110					rx			00000001								IH <= R[x]	ALUOp_ADD
18	MTSP	R	01100					100			rx			00000					SP <= R[x]	ALUOp_ADD
19	NOP	N	00001					00000000000											空操作	ALUOp_ADD
20	OR	R	11101					rx			ry			01101					R[x] <= R[x] | R[y]	ALUOp_OR
21	SLL	R	00110					rx			ry			immediate			00		if (immediate = 0) then R[x] <= R[y] << 8 else R[x] <= R[y] << immediate(unsigned)	ALUOp_SLL
22	SRA	R	00110					rx			ry			immediate			11		(arithmetic) if (immediate = 0) then R[x] <= R[y] >> 8 else R[x] <= R[y] >> immediate(unsigned)	ALUOp_SRA
23	SUBU	R	11100					rx			ry			rz			11		R[z] <= R[x] - R[y]	ALUOp_SUB
24	SW	I	11011					rx			ry			immediate					MEM[R[x] + SignExtend(immediate)] <= R[y]	ALUOp_ADD
25	SW_SP	I	11010					rx			immediate								MEM[SP + SignExtend(immediate)] <= R[x]	ALUOp_ADD
26	MOVE	R	01111					rx			ry			00000					R[x] <= R[y]	ALUOp_ADD
27	SLT	R	11101					rx			ry			00010					if (R[x] < R[y]) then T <= 1 else T <= 0 (有符号比较)	ALUOp_SLT
28	SLLV	R	11101					rx			ry			00100					R[y] <= R[y] << R[x]	ALUOp_SLL
29	SLTU	R	11101					rx			ry			00011					if (R[x] < R[y]) then T <= 1 else T <= 0 (无符号比较)	ALUOp_SLTU
30	ADDSP3	I	00000					rx			immediate								R[x] <= SP + SignExtend(immediate)	ALUOp_ADD

序号	指令	ALUSrc	Mem-Read	Mem-Write	Pcto-Reg	Reg-Write	Memto-Reg	PC-Jump	Read-Register1	Read-Register2	Write-Register	Immediate	ImmediateOp
1	ADDIU	ALUSrc_IMMEDIATE	0	0	0	1	0	0	10, 8		10, 8	7, 0	SIGNEXTEND
2	ADDIU3	ALUSrc_IMMEDIATE	0	0	0	1	0	0	10, 8		7, 5	3, 0	SIGNEXTEND
3	ADDSP	ALUSrc_IMMEDIATE	0	0	0	1	0	0	REG_SP		REG_SP	7, 0	SIGNEXTEND
4	ADDU	ALUSrc_REG	0	0	0	1	0	0	10, 8	7, 5	4, 2		
5	AND	ALUSrc_REG	0	0	0	1	0	0	10, 8	7, 5	10, 8		
6	B		0	0	0	0	0	0				10, 0	SIGNEXTEND
7	BEQZ		0	0	0	0	0	0	10, 8			7, 0	SIGNEXTEND
8	BNEZ		0	0	0	0	0	0	10, 8			7, 0	SIGNEXTEND
9	BTEQZ		0	0	0	0	0	0	REG_T			7, 0	SIGNEXTEND
10	CMP	ALUSrc_REG	0	0	0	1	0	0	10, 8	7, 5	REG_T		
11	JR	ALUSrc_IMMEDIATE	0	0	0	0	0	1	10, 8				SETZERO
12	LI	ALUSrc_IMMEDIATE	0	0	0	1	0	0	REG_ZERO		10, 8	7, 0	ZEROEXTEND
13	LW	ALUSrc_IMMEDIATE	1	0	0	1	1	0	10, 8		7, 5	4, 0	SIGNEXTEND
14	LW_SP	ALUSrc_IMMEDIATE	1	0	0	1	1	0	REG_SP		10, 8	7, 0	SIGNEXTEND
15	MFIH	ALUSrc_IMMEDIATE	0	0	0	1	0	0	REG_IH		10, 8		SETZERO
16	MFPC	ALUSrc_IMMEDIATE	0	0	1	1	0	0			10, 8		SETZERO
17	MTIH	ALUSrc_IMMEDIATE	0	0	0	1	0	0	10, 8		REG_IH		SETZERO
18	MTSP	ALUSrc_IMMEDIATE	0	0	0	1	0	0	7, 5		REG_SP		SETZERO
19	NOP		0	0	0	0	0	0					
20	OR	ALUSrc_REG	0	0	0	1	0	0	10, 8	7, 5	10, 8		
21	SLL	ALUSrc_IMMEDIATE	0	0	0	1	0	0	7, 5		10, 8	4, 2	ZTE
22	SRA	ALUSrc_IMMEDIATE	0	0	0	1	0	0	7, 5		10, 8	4, 2	ZTE
23	SUBU	ALUSrc_REG	0	0	0	1	0	0	10, 8	7, 5	4, 2		
24	SW	ALUSrc_IMMEDIATE	0	1	0	0	0	0	10, 8	7, 5		4, 0	SIGNEXTEND
25	SW_SP	ALUSrc_IMMEDIATE	0	1	0	0	0	0	REG_SP	10, 8		7, 0	SIGNEXTEND
26	MOVE	ALUSrc_IMMEDIATE	0	0	0	1	0	0	7, 5		10, 8		SETZERO
27	SLT	ALUSrc_REG	0	0	0	1	0	0	10, 8	7, 5	REG_T		
28	SLLV	ALUSrc_REG	0	0	0	1	0	0	7, 5	10, 8	7, 5		
29	SLTU	ALUSrc_REG	0	0	0	1	0	0	10, 8	7, 5	REG_T		
30	ADDSP3	ALUSrc_IMMEDIATE	0	0	0	1	0	0	REG_SP		10, 8	7, 0	SIGNEXTEND