Report

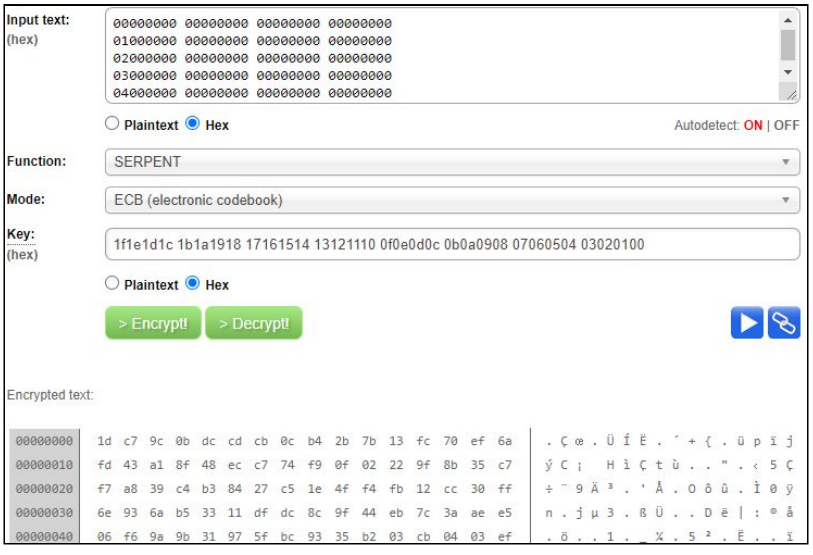
module structure

```
.
├── Report.pdf
├── tb_test.v                 // 測加密後解密
├── tb_practice.v             // 原本的testbench
└── Serpent
    ├── encrypt               // 加密用的
    │   ├── encryption.v      // 32 rounds
    │   ├── round.v           // Key mixing → S_box → Transformation
    │   └── S_box.v           // S box
    ├── decrypt               // 解密用的
    │   ├── decryption.v      // 32 rounds, 倒過來
    │   ├── round_inv.v       // Transformation_inv → S_box_inv → Key
mixing
    │   └── S_box_inv.v       // Inverse S box
    ├── keygen                // 生33個key用的
    │   └── key_gen.v         // 生33個key用的
    └── codegen.py            // 輔助用的
```

Test

```
iverilog tb_test.v
vvp a.out
iverilog tb_practice.v
vvp a.out
```

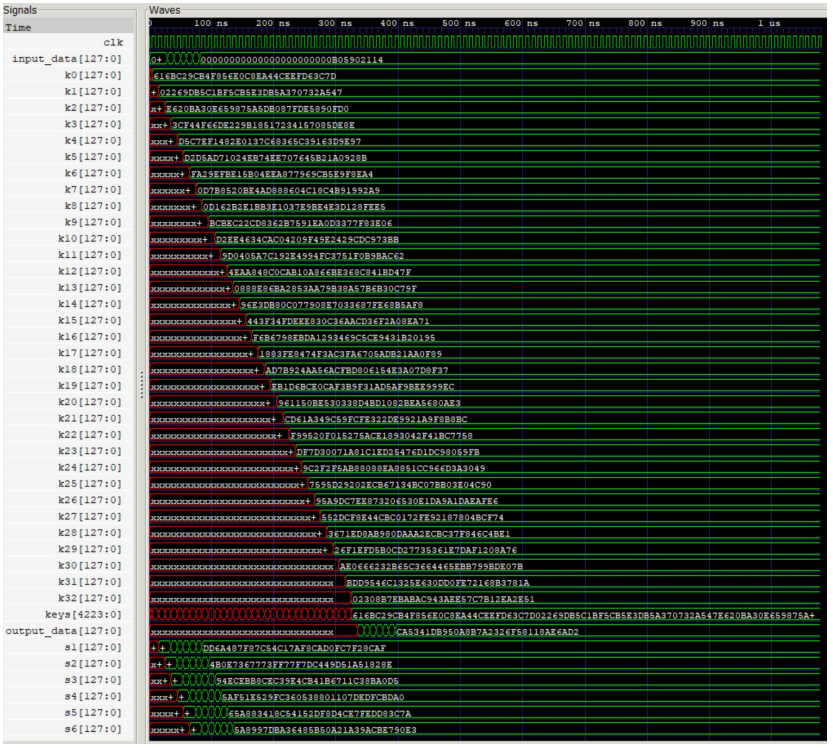
Result for tb_practice.v




```
PS C:\Users\sam\Downloads\Serpent> iverilog.exe .\tb_test.v
PS C:\Users\sam\Downloads\Serpent> iverilog.exe .\tb_practice.v
PS C:\Users\sam\Downloads\Serpent> vvp.exe .\a.out
VCD info: dumpfile top.vcd opened for output.
6aef70fc137b2bb40ccbcddc0b9cc71d
c7358b9f22020ff974c7ec488fa143fd
ff30cc12fbf44f1ec52784b3c439a8f7
e5ae3a7ceb449f8cdcdf1133b56a936e
ef0304cb03b23593bc5f97319b9af606
2f0459b824d85b312afaed864ce4fea9
```

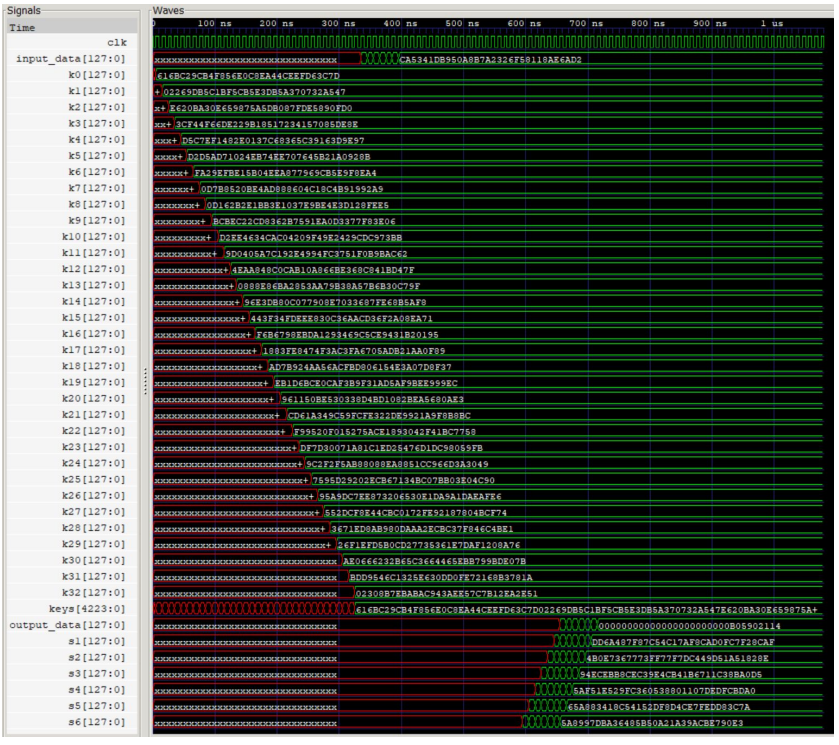
說明

Encryption:



每個cycle生4個omega，也就是一個key，總共33把key，要33個cycle；每個cycle生下一個state，pipeline做，第一把要等一個cycle，剩下的32個cycle，做32個round。故encryption要33個cycle，而input可以每個cycle都進來。

Decryption:



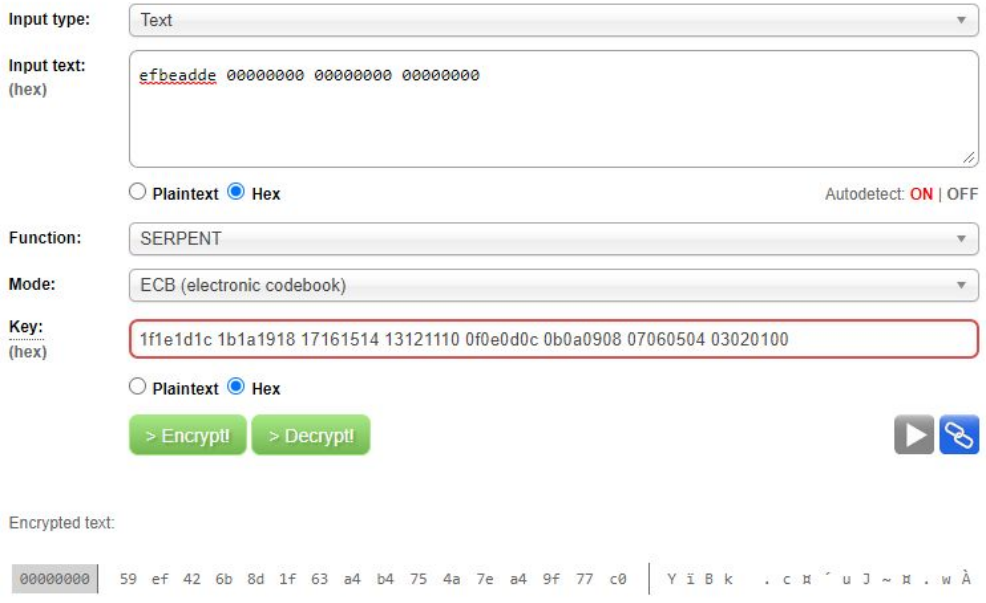
Decryption key要倒著xor，所以要先等key出來，故要33+32個cycle才能結束decryption。如果key先算好則可以只要32 cycle就結束。

Test on board

```
always @(*)
begin
      case ( axi_araddr[ADDR_LSB+OPT_MEM_ADDR_BITS:ADDR_LSB] )
        4'h0   : reg_data_out <= slv_reg0;
        4'h1   : reg_data_out <= slv_reg1;
        4'h2   : reg_data_out <= slv_reg2;
        4'h3   : reg_data_out <= slv_reg3;
        4'h4   : reg_data_out <= slv_reg4;
        4'h5   : reg_data_out <= slv_reg5;
        4'h6   : reg_data_out <= slv_reg6;
        4'h7   : reg_data_out <= slv_reg7;
        4'h8   : reg_data_out <= slv_reg8;
        4'h9   : reg_data_out <= slv_reg9;
        4'hA   : reg_data_out <= out_128[127:96];
        4'hB   : reg_data_out <= out_128[95:64];
        4'hC   : reg_data_out <= out_128[63:32];
        4'hD   : reg_data_out <= out_128[31:0];
        4'hE   : reg_data_out <= slv_reg14;
        4'hF   : reg_data_out <= out_32[31:0];
        default : reg_data_out <= 0;
      endcase
end
Serpent  dut(    .i_clk( S_AXI_ACLK ),
                 .i_resetn(  slv_reg14[0] ),
                 .i_dir( slv_reg14[1] ),
                 .i_key( {64'h0001020304050607, slv_reg9, slv_reg8, slv_reg7, slv_reg6, slv_reg5, slv_reg4} ),
                 .i_new_block( slv_reg14[2] ),
                 .i_data( {slv_reg3, slv_reg2, slv_reg1, slv_reg0} ),
                 .o_ready( out_32[0] ),
                 .o_output( out_128 ) );
```

Resource

Name	Slice LUTs (53200)	Slice Registers (106400)	F7 Muxes (26600)	F8 Muxes (13300)	Slice (13300)	LUT as Logic (53200)	LUT as Memory (17400)	Bonded IOPADs (130)	BUFGCTRL (32)
N my_ip_wrapper	22814	13279	64	32	5996	22754	60	130	1
my_ip_i (my_ip)	22814	13279	64	32	5996	22754	60	0	1
myip_0 (my_ip_myip_0_0)	22461	12822	64	32	5846	22461	0	0	0
inst (my_ip_myip_0_0_myip_v1_0)	22461	12822	64	32	5846	22461	0	0	0
myip_v1_0_S00_AXI_inst (my_ip_myip_0_	22461	12822	64	32	5846	22461	0	0	0
dut (my_ip_myip_0_0_Serpent)	22346	12424	32	32	5826	22346	0	0	0
d0 (my_ip_myip_0_0_decryption)	6734	4096	0	0	1990	6734	0	0	0
e0 (my_ip_myip_0_0_encryption)	128	4096	32	32	1655	128	0	0	0
kg (my_ip_myip_0_0_key_gen)	15512	4224	0	0	4332	15512	0	0	0
processing_system7_0 (my_ip_processing_syst	0	0	0	0	0	0	0	0	1
ps7_0_axi_periph (my_ip_ps7_0_axi_periph_0)	336	424	0	0	143	277	59	0	0
rst_ps7_0_100M (my_ip_rst_ps7_0_100M_0)	17	33	0	0	10	16	1	0	0



```
63      uint32_t current_state;
64
65      // 0~3 state
66      *((uint32_t *)BASE_IP + 0) = 0xdeadbeef;
67      *((uint32_t *)BASE_IP + 1) = 0x0;
68      *((uint32_t *)BASE_IP + 2) = 0x0;
69      *((uint32_t *)BASE_IP + 3) = 0x0;
70
71      // 4~9 key (upper 64 bits fixed 64'h0001020304050607)
72      *((uint32_t *)BASE_IP + 4) = 0x1c1d1e1f;
73      *((uint32_t *)BASE_IP + 5) = 0x18191a1b;
74      *((uint32_t *)BASE_IP + 6) = 0x14151617;
75      *((uint32_t *)BASE_IP + 7) = 0x10111213;
76      *((uint32_t *)BASE_IP + 8) = 0x0c0d0e0f;
77      *((uint32_t *)BASE_IP + 9) = 0x08090a0b;
78
79      // encrypt
80      current_state = (0*RESET) + (1*DIR) + (1*NEW_BLOCK);
81      *((uint32_t *)BASE_IP + 14) = current_state; // set current state
82      current_state = (1*RESET) + (1*DIR) + (1*NEW_BLOCK);
83      *((uint32_t *)BASE_IP + 14) = current_state; // set current state
84      current_state = (1*RESET) + (1*DIR) + (0*NEW_BLOCK);
85      *((uint32_t *)BASE_IP + 14) = current_state; // set current state
86
87      xil_printf("%8X \n\r", *((uint32_t *)BASE_IP + 10));
88      xil_printf("%8X \n\r", *((uint32_t *)BASE_IP + 11));
89      xil_printf("%8X \n\r", *((uint32_t *)BASE_IP + 12));
90      xil_printf("%8X \n\r", *((uint32_t *)BASE_IP + 13));
91
```

Console | Vitis Serial Terminal | Executables | Vitis Log | Problems | Debugger Console

Connected to: Serial (COM4, 115200, 0, 8)

```
C0779FA4

7E4A75B4

A4631F8D

6B42EF59
```