Module 5-7 Tutorial Questions

1. Design a 4-bit up-counter that has two control inputs: cnt enables counting up, while clear synchronously resets the counter to all 0s, using a parallel load register as a building block.

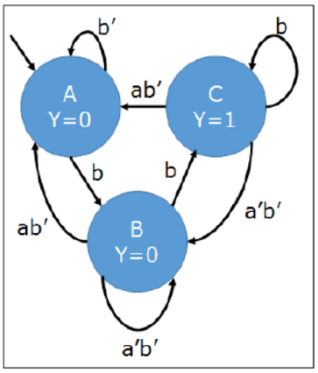
2. Draw the state transition diagram of sequence recogniser which could recognise input sequence 110. Assuming the left most bit arrives first.

3. Draw a state diagram for a FSM with no inputs and three outputs X, Y, and Z. The output sequence for {xyz} should be {000}, {001}, {010}, {100} repeated infinitely. {000} is the initial output.

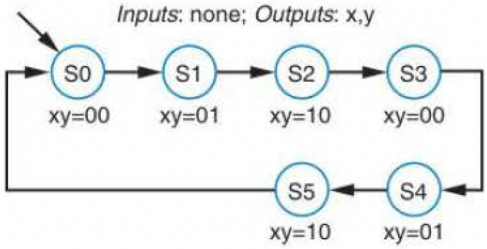
4. Design a 3-bit binary up counter following the FSM-based design approach. What is the maximum clock frequency this counter can operate at? You can assuming all registers are identical with Tsu = 0.5ns, Th = 0.5ns, TcQ = 0.5ns, and 2ns delay for any 2-input logic gate.

5. Design a sequence generator which generates a sequence of 0001, 0011, 1100, 1000?

6. Draw a state transition table for each of the FSMs shown below. Then, using multiplexers, registers, and/or logic gates, draw a circuit implementation. Is this a Moore or Mealy FSM?



7. Perform state minimisation for the following finite state machine.



8. Design a circuit to compute F = (A * B * C) + 3*D + 12. A, B, C, and D are 16-bit inputs, and F is a 16-bit output. Use 16-bit multiplier and adder components.

9. Based on question 8, assume inputs A, B, C, D and output F are now all stored in registers governed by the same clock signal, what is the maximum operating clock frequency for the circuit to work properly. Assume $TP_{multiplier}$ = 12.5ns, TP_{adder} = 5ns, TP_{su} = 0.5ns, TP_{h} = 0.3ns, and TP_{cQ} = 0.5ns.

10. Use the RTL design process to design a system that outputs the average of the most recent two data input samples. The system has an 8-bit unsigned data input I, and an 8-bit unsigned output avg. The system starts sampling data input when a single-bit input S changes from 0 to 1, otherwise stop and clear previous operations. Choose internal bit width that prevent overflow.

11. Use the RTL design process to create an alarm system that sets a single-bit output alarm to 1 when the average temperature of four consecutive samples meets or exceeds a user-defined threshold value. A 32-bit unsigned input CT indicates the current temperature, and a 32-bit unsigned input WT indicates the warning threshold. A single-bit input clr disables the alarm and the sampling process when it is 1.