Steven Frederiksen

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WORK EXPERIENCE

KFORCE | FPGA Design Engineer — Washington, D.C. | 2024 - present

- Supported the Tactical Electronic Warfare Division (TEWD) in NRL.
- Led design, implementation, and verification of upgraded RF environment real-time simulations using FPGAs.
- Utilized mixed-signal simulation and hardware-in-the-loop testbenches to verify design.
- Worked primarily as an individual; producing project timelines, goals, test plans, documentation, and technical status reports.

GRAF RESEARCH | Research Engineer — Blacksburg, VA | 2018 – 2024

- Led development of real-time, in-FPGA test bench platform for custom IP utilizing Vivado Model Composer and Vivado HLS for creation of generic interfaces, Simulink for simulation and test vector generation, and an Ethernet-based protocol for data transfer between test harness and user machine.
- Modeling, simulation, and implementation of DSP algorithms in FPGAs.
- Led development of Lattice-specific functionality for Graf Trace tool, which archives and verifies build artifacts throughout an FPGA build flow, enabling customers to meet new DoD guidance.
- Transitioned M.S. research to product prototype with Graf DELV software. DELV translates English specifications to System Verilog assertions for automatic verification of HDL.
- Led transition to Vue.js and deployment using Docker/Kubernetes for internal web-application product. Also performed full-stack development for the same project using Spring/Vue.
- Experience utilizing Python for internal tooling including: automated FPGA design instrumentation and testing, custom lab bench software, GUI and CLI application prototypes.
- Wrote and contributed to multiple winning Phase 1 and 2 SBIR proposals
- Kept up to date with state-of-the-art hardware trojan literature in service of SBIR contracts.

Publications: "DELV: Datasheet/English to Logic Verification," Edward Carlisle, Steven Frederikson, Jonathan Graf, Scott Harper, John Aromando, and Michael S. Hsiao, in *Government Microcircuit Applications & Critical Technology Conf.*, Mar. 2021.

PROJECTS

ESP32 ENVIRONMENTAL CONTROLLER — ESP32, FreeRTOS, IoT

Custom environemtal control and monitoring solution for fermentation projects.

- Live monitoring and control via MQTT
- I2C control and monitoring chain for sensors and relays.
- Uses ESP-IDF for FreeRTOS integration.

TTSA — Rust, EDA Algorithms, Optimzation, Simulated Annealing

Implementation of the TTSA algorithm using Rust.

SKILLS

Languages: Java, C/C++, Python, Rust, Bash, Javascript, Lisp, MATLAB
FPGA Development: Verilog, VHDL, Vivado HLS, Verilator, Symbiflow, ABV, Simulink/Model Composer, SystemVerilog/SVA
Technology: Microblaze, ESP-IDF, FreeRTOS, Arduino, HTML/CSS, Git, Docker, Kubernetes, XMIDAS, LaTeX
Communication: SBIR proposals, technical progress and final reports, journal article (link), Patent applications (link)

EDUCATION

B.S. Computer Engineering — Blacksburg, VA
Virginia Tech