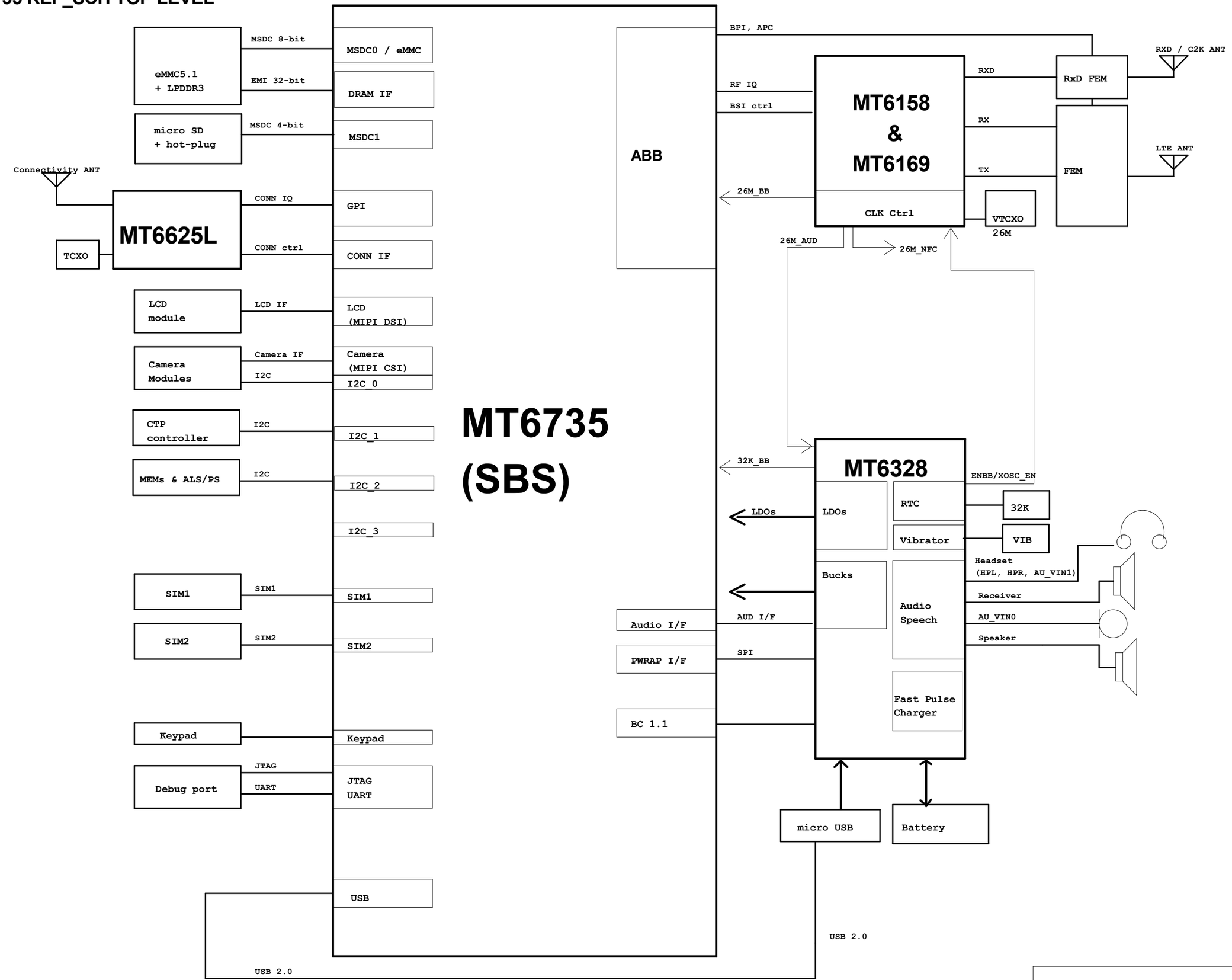
Project : MT6735 REF_SCH TOP LEVEL



Title	01_Block_Diagram		
Size E	MTK Confidential		
Date: Thursday, October 09, 2014		Sheet 1 of 26	

I2C	Function	I2C Spec.	Budget Timing	I2C Slave Address (7-bit mode)
I2C-0	Rear Camera - 13M	400 Kbps	Yes.	Rear camera (IMX135) I2C address: 0X10 (Write:0x20, Read:0x21) AF driver (DW9714A) I2C address: 0x0C (Write:0x18 , Read:0x19)
	Front Camera	400 Kbps	Yes.	Front camera (GC2355) I2C address: 0x3C (Write:0x78, Read:0x79)
I2C-1	CTP	400 Kbps	Yes.	GT1151 / CTP I2C address: 0X5D (Write:0xBA, Read:0xBB) or 0x14 (Write:0x28, Read:0x29)
I2C-2	M Sensor	2.5 Mbps		AK09911 / M-Sensor I2C Address: 0x0D (Write:0x1A, Read:0x1B)
	Gyro Sensor	400 Kbps	Yes.	ITG1010 / Gyro I2C Address: 0x68 (Write:0xD0, Read:0xD1)
	Accelerometer	400 Kbps		MC3410 / Accelerometer I2C address: 0x4C (Write:0x98, Read:0x99)
	RGB / PS Sensor	400 Kbps		CM36652 / RGB+PS I2C address: 0X60 (Write:0xC0, Read:0xC1)
	NFC	1.2 Mbps	Yes.	MT6605 / NFC I2C address: 0X28 (Write:0x50, Read:0x51)
	Flashlight Driver	400 Kbps		LM3642 / Flashlight Driver I2C address: 0X63 (Write:0xC6, Read:0xC7)
I2C-3				

Note : I2C Spec. : Standard mode (100 kbps) and Fast mode (400 kbps), Fast mode Plus (1 Mbps) and High-speed mode (3.4 Mbps)

V0.1 First Release (2014/09/05)

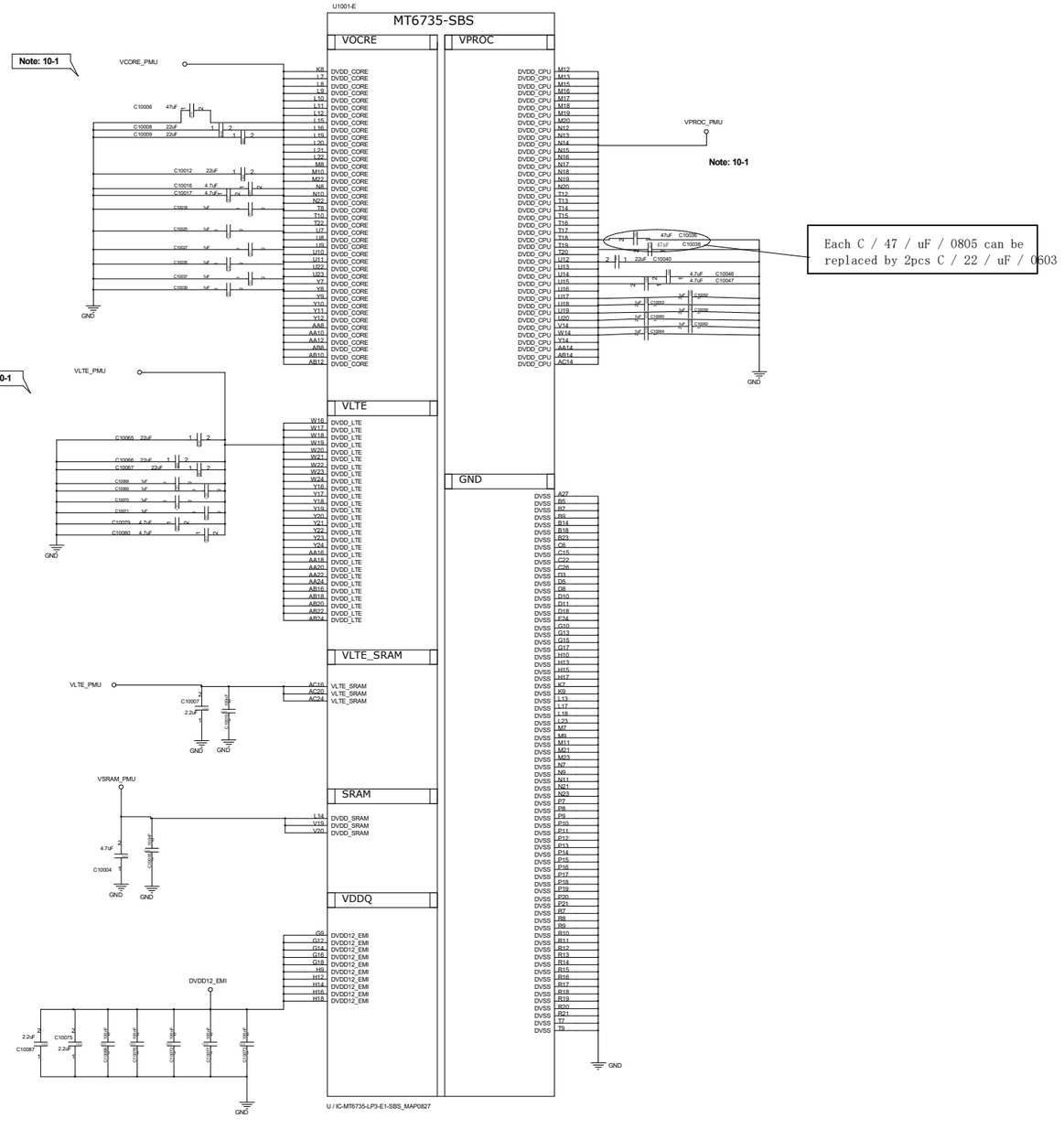
V0.2 Change Notice (2014/10/04)

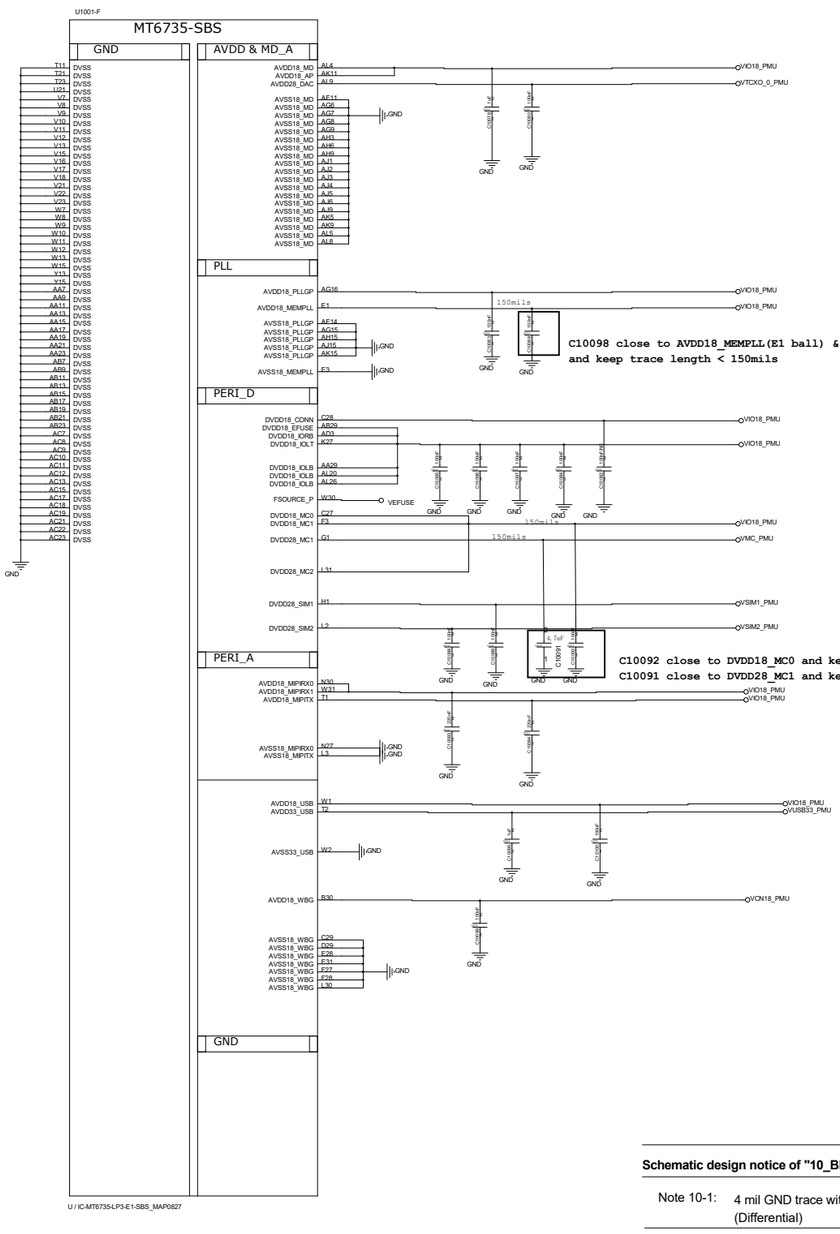
1. Modify Circuit and Cap of VPROC / VLTE / VCORE / DVDD12_EMI to sync with MMD Circuit [P10]
2. Modify VIO18 CAP
   -Change C10093 from 1uF to 220nF [P10]
   -Change C10094 from 1uF to 220nF [P10]
   -Change C10100 from 1uF to 100nF [P10]
   -Change C4101 from 2.2uF to 1uF [P41]
   -Change C5121 from 1uF to 100nF [P51]
   -Change C3706 from 2.2uF to 1uF [P37]
3. Add Notice for DVDD18_MC0/DVDD28_MC1 Cap [P10]
4. Delete UCTS0/URTS0 net [P12, 90]
5. Delete C2024 and connect AUXADC_VIN to D_GND directly [P20]
6. Rename R2004 to R2005 (sync with MMD circuit), and change from 200K to 1R [P20]
7. Delete SH2102 and connect CS_P to D_GND [P21]
8. Delete SH2101 [P21]
9. Change C4103 & C4104 from 10uF/C0603 to 2.2uF/C0402 [P41]
10. Delete Notice for Camera [P62]
11. Change U5003 from GPS SAW to GNSS SAW/B8313 [P50]
12. Change R1101 from 240R to 35R [P11]
13. Add Notice for Bypass CAP close to AVDD18_MEMPLL(E1 ball) & DVDD18_MC1(F3 ball) [P10]
14. Delete C2058~C2061 [P20]
15. Rename C2037 to C2040 (sync with MMD circuit) and add notice for C2040 [P20]
16. Rename SH2006~SH2010 to sync with MMD circuit [P20]
    -Rename SH2006 to SH2009
    -Rename SH2007 to SH2010
    -Rename SH2008 to SH2011
    -Rename SH2009 to SH2012
    -Rename SH2010 to SH2013 and modify description to NC/MMD/PMIC
17. Add SH2014 [P20]
18. Modify L2001/L2003/L2006/L2008/L2009 value description [P20]
19. Change net name VBAT_RF to VBAT [P32]
20. Change C3356 from NC to 47pF [P33]
21. Change R3802 from 0R to NC [P38]
22. Change LPF3801 from NC to LPF / FI-168L083523-T [P38]
23. Remove LPF3803/R3811/L3822/L3815 [P38]
24. Remove SH3126/SH3127/SH3128 [P31]
25. Remove SH3125 [P32]
26. SH3129 change to R3215 [P32]
27. SH3123 change to R3216 [P32]
28. SH3124 change to R3217 [P32]
29. Add notice for C3239: Put near PA Sky77621 side [P32]
30. Change SH4101 size from 0603 to 0201 (Sync with MMD) [P41]
31. Connect CON3301 pin3 & pin4 to GND [P33]
32. Modify notice for CON2101 pin1 (Bat connector-VBAT net) from 60mil to 125mil [P21]
33. Add notice for CON2101 pin3 (Bat connector-GND net), need 125mil [P21]
34. Rename bypass cap to sync with MMD circuit [P10]
    -Rename bypass cap for AVDD28_DAC from C10080 to C10090
    -Rename bypass cap for DVDD18_IOLT from C10086 to C10096
    -Rename bypass cap for DVDD18_IOLB from C10087 to C10097
35. Rename bypass cap for AVDD18_AUD from C2040 to C2058 [P20]
36. Mofidy notice for AVDD45_VSYS22 balls, change form 20mil to 30mil [P20]
37. Mofidy notice for AVDD45_VPA ball, change form 20mil to 30mil [P20]
38. Add trace width notice for Buck [P20]

V0.3 Change Notice (2014/10/24)

1. Delete CORESONIC_SWD/CORESONIC_SWCK net [P12, 90]
2. Modify R1105 & R1106 from 8K to 8.06K [P11]
3. Update U2402 complete part number: FAN53611AUC115X [P24]
4. Modify C10082 from 100nF to NC [P10]
5. Add Note12-1 & 12-2 for MT6735M [P12]
6. Connect GND_VLTE from SH2003 to SH2002 [P20]
7. Connect GND_VCORE1 from SH2002 to SH2003 [P20]
8. Change SH3903 to R3909 /0402/NC [P39]
9. Change SH3904 to R3910/0402/0R [P39]
10. Change PA3901 from RF7255 to SKY77765 [P39]
11. Change R3702 from 0R to 68R [P37]
12. Change R3701/3703 from NC to 100R [P37]
13. Modify R1101 from 35R to 36R [P11]
14. Modify R6510 Circuit [P65]
15. RF Phase2 first release [P31-34]

Title	05_Change_Notice
Size E	MTK Confidential
Date: Thursday, October 09, 2014	Sheet 3 of 26





Schematic design notice of "10_BB_POWER" page.

Note 10-1: 4 mil GND trace with good shielding to PMIC (Differential)

Note 10-3: FSOURCE_P(EFUSE)
(1)FSOURCE_P EFUSE power(VEFUSE) should be only for EFUSE usage(not share with other application)
(2)W/I EFUSE program, VEFUSE need 1uF bypass cap (pls refer to ¨LDO output voltage/current table〃)
(3)W/O EFUSE program, VEFUSE bypass cap should be NC.

Title	10_BB_POWER
Size	E
	MTK Confidential
Date:	Thursday, October 09, 2014
Sheet	4 of 28

U1001-A

MT6735-SBS

PMU_IF

SYSRSTB[8] AC2 SYSRSTB
WATCHDOG[8] U4 WATCHDOG
SRCLKENA0[8] V4 SRCLKENA0
SRCLKENA1[8] AC30 SRCLKENA1
RTC32K1V8[8] AC1 RTC32K_CK
PWRAP_SPI0_CSN[8] PWRAP_SPI0_CSN Y4 PWRAP_SPI0_CSN
PWRAP_SPI0_CK[8] Y3 PWRAP_SPI0_CK
PWRAP_SPI0_MO[8] AB2 PWRAP_SPI0_MO
PWRAP_SPI0_MI[8] AB1 PWRAP_SPI0_MI
AUD_CLK_MOS[8] Y1 AUD_CLK_MOSI
AUD_DAT_MOSI_1[8] AUD_DAT_MOSI_1 Y2 AUD_DAT_MOSI
AUD_DAT_MISO_1[8] W3 AUD_DAT_MISO
AA2 PWRAP_INT

PLLs Test Pin

JTAG

AJ31 JTMS
AJ30 JTCK
AJ29 JTDI
AK28 JTDO

Misc

AK30 TESTMODE
GND

NC

A1 NC
A2 NC
A30 NC
A31 NC
B1 NC
B31 NC
AK1 NC
AL1 NC
AL2 NC
AL30 NC
AL31 NC

DRAM_IF

REXTDN F2 EXTDN
R1101 2 2K 368
GND

VREF F16 EVREF[5,18] [41]

U / IC-MT6735-LP3-E1-SBS_MAP0827

R1109: 47K,Ext. Buck for LTE VSRAM: Enable
R1109: NC, Ext. Buck for LTE VSRAM: Disable

[41] EVREF[5,18]
DVDD12_EMI
R1105 2 8.2K
C1101 100nF
C1102 100nF
C1103 1uF
R1106 2 8.2K
GND GND GND

U1001-B

MT6735-SBS

SIM

[65] SIM1_SCLK[25] K4 SIM1_SCLK
[65] SIM1_SIO[25] J2 SIM1_SIO
[65] SIM1_SRST[25] J4 SIM1_SRST
[65] SIM2_SCLK[25] L4 SIM2_SCLK
[65] SIM2_SIO[25] K1 SIM2_SIO
[65] SIM2_SRST[25] K2 SIM2_SRST

BPI-L/C

AK20 BPI_BUS20
AH19 BPI_BUS19
AK21 BPI_BUS18
AL21 BPI_BUS17
AF20 BPI_BUS16
AG20 BPI_BUS15
AF21 BPI_BUS14
AG21 BPI_BUS13
AF22 BPI_BUS12
AH21 BPI_BUS11
[21] TP_EN AK22 BPI_BUS10
AG22 BPI_BUS9
AH22 BPI_BUS8
AJ22 BPI_BUS7
AK23 BPI_BUS6
AL23 BPI_BUS5

RFI_C

[11] LTE_RFIC0_BSI_EN AG17 RFIC0_BSI_EN
[11] LTE_RFIC0_BSI_CK AG18 RFIC0_BSI_CK
[11] LTE_RFIC0_BSI_D2 AK16 RFIC0_BSI_D2
[11] LTE_RFIC0_BSI_D1 AL17 RFIC0_BSI_D1
[11] LTE_RFIC0_BSI_D0 AK17 RFIC0_BSI_D0
AG19 C2K_TXBPI
AH18 RFIC1_BSI_EN
AJ19 RFIC1_BSI_CK
AL18 RFIC1_BSI_D0
AK19 RFIC1_TX_BSI_EN
AK18 RFIC1_TX_BSI_CK
AJ18 RFIC1_TX_BSI_D0

BPI - L

LTE_TXBP[11] AH1 LTE_TXBPI
VIO18_PMU 47KNC R1109 VLTE_SRAM_ID AD5 BPI_BUS27
47K R1110 GND
AG3 BPI_BUS26
AG4 BPI_BUS25
AE5 BPI_BUS24
[14] LTE_BPI_OUT23 AF5 BPI_BUS23
[13] LTE_BPI_OUT22 AG5 BPI_BUS22
[13] LTE_BPI_OUT21 AF2 BPI_BUS21
[14] LTE_BPI_OUT4 AF1 BPI_BUS4
[14] LTE_BPI_OUT3 AF2 BPI_BUS3
[14] LTE_BPI_OUT2 AG2 BPI_BUS2
AE1 BPI_BUS1
AH2 BPI_BUS0

U / IC-MT6735-LP3-E1-SBS_MAP0827

ABB_IF

C2KX26M_IN AE13
C2K_TX_BBIP AK14
C2K_TX_BBIN AK13
C2K_TX_BBQP AL12
C2K_TX_BBQN AK12
C2K_RX1_BBIP AJ13
C2K_RX1_BBIN AH13
C2K_RX1_BBQP AG13
C2K_RX1_BBQN AG14
C2K_RX2_BBIP AL15
C2K_RX2_BBIN AL14
C2K_RX2_BBQP AH14
C2K_RX2_BBQN AJ14
APC1 AH10 LTE_APC1 [37]
APC2 AJ10
LTEX26M_IN AE10 LTE_LTEX26M_IN[11]
LTE_TX_BBIP AK2 RF_TX_BBIP[11]
LTE_TX_BBIN AK3 RF_TX_BBIN[11]
LTE_TX_BBQP AL3 RF_TX_BBQP[11]
LTE_TX_BBQN AK4 RF_TX_BBQN[11]
LTE_RX1_BBIP AH7 RF_RX1_BBIP[11]
LTE_RX1_BBIN AJ7 RF_RX1_BBIN[11]
LTE_RX1_BBQP AK6 RF_RX1_BBQP[11]
LTE_RX1_BBQN AL6 RF_RX1_BBQN[11]
LTE_RX2_BBIP AK7 RF_RX2_BBIP[11]
LTE_RX2_BBIN AK8 RF_RX2_BBIN[11]
LTE_RX2_BBQP AJ8 RF_RX2_BBQP[11]
LTE_RX2_BBQN AH8 RF_RX2_BBQN[11]
RFIC_ET_P AH5
RFIC_ET_N AH4

MISC BSI

RFIC_MIPI0_SCLK AD2 MIPI0_SCLK[12]
RFIC_MIPI0_SDATA AB5 MIPI0_SDATA[12]
RFIC_MIPI1_SCLK AC3 MIPI1_SCLK[13]
RFIC_MIPI1_SDATA AB4 MIPI1_SDATA[13]
LTE_PAVM0 AD4
LTE_PAVM1 AC4

AUX IN

AUXIN2 AH11 VLTE_SRAM_ID
AUXIN1 AG12 AUX_IN1_NTC AUX_IN1_NTC[12] [32]
AUXIN0 AG11 AUX_IN0_NTC AUX_IN0_NTC[23] [63]

REF POWER

REFP AL10
AVSS_REFN AK10

GND
C1104 100nF
C1105/C1106 close to BB
C1106 100nF
C1105 100nF
GND
C1104 100nF
GND
Close to AP IC.

[37] [37] [37] [37] [37] [37]

U1001-C

MT6735-SBS

CSI

[62] RCP[22]	P28	RCP	
[62] RCN[22]	N28	RCN	
[62] RDP0[22]	N29	RDP0	
[62] RDN0[22]	P29	RDN0	
[62] RDP1[22]	P30	RDP1	
[62] RDN1[22]	P31	RDN1	
[62]	T30	RDP2	
[62]	R30	RDN2	
[62]	T31	RDP3	
[62]	U31	RDN3	
[62] RCP_A[22]	T28	RCP_A	
[62] RCN_A[22]	R28	RCN_A	
[62] RDP0_A[22]	T29	RDP0_A	
[62] RDN0_A[22]	R29	RDN0_A	
[62] RDP1_A[22]	V30	RDP1_A	
[62] RDN1_A[22]	U30	RDN1_A	
	V29	RDP2_A	
	U29	RDN2_A	
	V28	RDP3_A	
	U28	RDN3_A	

DSI

TCP	N2	MIPI_TCP[21]	[61]
TCN	N1	MIPI_TCN[21]	[61]
TDP0	R2	MIPI_TDP0[21]	[61]
TDN0	P2	MIPI_TDN0[21]	[61]
TDP1	R3	MIPI_TDP1	[61]
TDN1	P3	MIPI_TDN1	[61]
TDP2	N3		[61]
TDN2	M3		[61]
TDP3	M1		[61]
TDN3	M2		[61]

VRT R1 MIPI_VRT — R1227 1.5K — GND

DISP_PWM	AH31	DISP_PWM[10]	[23]
LCM_RST	W4	LCM_RST[21]	[61]
DSI_TE	AA5	DSI_TE[21]	[61]

[23] [23] [62] [25] KPCOL3 — R1296 1K

	W29	CMDAT0
	W28	CMDAT1
	Y31	CMPCLK
[22] CMMCLK	Y27	CMMCLK
[22] CMMCLK1	Y28	CMMCLK1

SPI

GPIO_CAMERA_RESET[22]	AH28	SPI_CS
GPIO_CTP_RSTB [21]	AH29	SPI_CK
[25] KPLED_EN	AG30	SPI_MO
[32] FLASH_LED_EN	AH30	SPI_MI

I2S

[9] GPIO_USB_DRVVBUS	AK26	I2S_BCK
[19] GPIO_GPS_LNA_EN	AL27	I2S_LRCK
[9] GPIO_CHG_EN	AK27	I2S_DATA_IN

U / IC-MT6735-LP3-E1-SBS_MAP0827

U1001-D

MT6735-SBS

USB

[64] USB_DP[24]	U2	USB_DP
[64] USB_DM[24]	V2	USB_DM
	V1	USB_VRT

USB_VRT_P0 — R1201 2.5K — GND

BC

[20] CHD_DP[8]	T3	CHD_DP
[20] CHD_DM[8]	T4	CHD_DM

KEYPAD

[25] KPROW2	AG23	KPROW2
[25] KPROW1	AJ23	KPROW1
[25] KPROW0	AH23	KPROW0
[22, 25] KPCOL2	AG24	KPCOL2
[25] KPCOL1	AK24	KPCOL1
[25] KPCOL0	AL24	KPCOL0

I2C

VCAM_IO_PMU		
[22] SCL0	AA30	SCL0
[22] SDA0	Y30	SDA0
VIO18_PMU		
[9,21] SCL1	AB31	SCL1
[9,21] SDA1	AB30	SDA1
VIO18_PMU		
[22,23] SCL2	AA28	SCL2
[22,23] SDA2	AB28	SDA2
	AB27	SCL3
	AC27	SDA3

UART

UTXD0	AJ28	UTXD0
URXD0	AJ27	URXD0
UTXD1	AG27	UTXD1
URXD1	AH27	URXD1
	AD30	UTXD2
	AF29	URXD2
	AE30	UTXD3
	AE31	URXD3

TP1201 TP50MIL TP1202 TP50MIL [22,25] KPROW5 — R1284 1K

WCN 6625

GPS_RX_IP	E30	GPS_RXIP
GPS_RX_IN	D30	GPS_RXIN
GPS_RX_QP	C30	GPS_RXQP
GPS_RX_QN	C31	GPS_RXQN
F2W_CLK	D28	F2W_CLK
F2W_DATA	D27	F2W_DATA
WB_RX_IP	K30	WB_RXIP
WB_RX_IN	J30	WB_RXIN
WB_RX_QP	J31	WB_RXQP
WB_RX_QN	H31	WB_RXQN
WB_TX_IP	H30	WB_TXIP
WB_TX_IN	G30	WB_TXIN
WB_TX_QP	F30	WB_TXQP
WB_TX_QN	F31	WB_TXQN

MSDCs

MSDC0_RSTB	D26	MSDC0_RSTB[18]	[41]
MSDC0_CMD	B24	MSDC0_CMD[18]	[41]
MSDC0_CLK	C23	MSDC0_CLK[18]	[41]
MSDC0_DSL	E25	MSDC0_DSL[18]	[41]
MSDC0_DAT7	D25	MSDC0_DAT7	[41]
MSDC0_DAT6	D23	MSDC0_DAT6	[41]
MSDC0_DAT5	A24	MSDC0_DAT5	[41]
MSDC0_DAT4	A23	MSDC0_DAT4	[41]
MSDC0_DAT3	E23	MSDC0_DAT3	[41]
MSDC0_DAT2	B25	MSDC0_DAT2	[41]
MSDC0_DAT1	B26	MSDC0_DAT1	[41]
MSDC0_DAT0	A26	MSDC0_DAT0	[41]
MSDC1_CLK	H3	MSDC1_CLK	MSDC1_CLK[25] [40]
MSDC1_CMD	F2	MSDC1_CMD	MSDC1_CMD[25] [40]
MSDC1_DAT3	G2	MSDC1_DAT3	
MSDC1_DAT2	H2	MSDC1_DAT2	
MSDC1_DAT1	H4	MSDC1_DAT1	
MSDC1_DAT0	G4	MSDC1_DAT0	
MSDC2_CLK	L29		
MSDC2_CMD	K28		
MSDC2_DAT3	M30		
MSDC2_DAT2	M31		
MSDC2_DAT1	L27		
MSDC2_DAT0	M27		

CONN_IF

WB_CTRL0	F29	WB_CTRL0
WB_CTRL1	G29	WB_CTRL1
WB_CTRL2	G28	WB_CTRL2
WB_CTRL3	H29	WB_CTRL3
WB_CTRL4	H28	WB_CTRL4
WB_CTRL5	J29	WB_CTRL5
WB_SCLK	B27	CONN_SCLK
WB_SDATA	B28	CONN_SDATA
WB_SEN	A29	CONN_SEN
XIN_WBG	E27	CONN_XO_IN
WB_RSTB	B29	CONN_RSTB
ANT_SEL0	J28	
ANT_SEL1	M28	
ANT_SEL2	L28	

PCM (ext MD)

PCM_CLK	AE27	R1285 1K	[25] KPROW4
PCM_SYNC	AD29	R1299 1K	[25] KPCOL7
PCM_TX	AD28	R1280 1K	[25] KPCOL5
PCM_RX	AD27	R1282 1K	[25] KPROW3

GPIO

SRCLKENAI	AC31		
EINT0	AE28	EINT0_IDDIG	[24]
EINT1	AE28	[22] VCAMA_EN	
EINT2	AE27	VCAMA1_EN	[22]
EINT3	AF30	EINT_ALPS	[23]
EINT4	AF31	EINT_ACC	[23]
EINT5	AL29	LOCK [22]	
EINT6	AK29	EINT_EAR	[20]
EINT7	AJ26	CAM_PDN0	[22]
EINT8	AH26	R1286 1K [25] KPCOL4	
EINT9	AG26	AUDIO_EN	[20]
EINT10	AH25	EINT_CTP	[21]
EINT11	AG25	CAM_RST1	[22]
EINT12	AK25	CAM_PDN1	[22]

U / IC-MT6735-LP3-E1-SBS_MAP0827

[50] WB_CTRL0[6,19] WB_CTRL0
[50] WB_CTRL1[6,19] WB_CTRL1
[50] WB_CTRL2[6,19] WB_CTRL2
[50] WB_CTRL3[6,19] WB_CTRL3
[50] WB_CTRL4[6,19] WB_CTRL4
[50] WB_CTRL5[6,19] WB_CTRL5
[50] CONN_SCLK[6,19] CONN_SCLK
[50] CONN_SDATA[6,19] CONN_SDATA
[50] CONN_SEN[6,19] CONN_SEN
[50] CONN_RSTB[6,19] CONN_RSTB

[50] GPS_RX_IP[6,19] GPS_RX_IP
[50] GPS_RX_IN[6,19] GPS_RX_IN
[50] GPS_RX_QP[6,19] GPS_RX_QP
[50] GPS_RX_QN[6,19] GPS_RX_QN
[50] F2W_CLK[6,19] F2W_CLK
[50] F2W_DATA[6,19] F2W_DATA
[50] WB_RX_IP[6,19] WB_RX_IP
[50] WB_RX_IN[6,19] WB_RX_IN
[50] WB_RX_QP[6,19] WB_RX_QP
[50] WB_RX_QN[6,19] WB_RX_QN
[50] WB_TX_IP[6,19] WB_TX_IP
[50] WB_TX_IN[6,19] WB_TX_IN
[50] WB_TX_QP[6,19] WB_TX_QP
[50] WB_TX_QN[6,19] WB_TX_QN
[50] CONN_XO_IN[6,19] CONN_XO_IN

Schematic design notice of "12_BB_2" page.

Note 12-1: MSDC2 Pin should be NC (No Connection) for MT6735M

Note 12-2: MT6735M does Not have CMMCLK1 function

Please refer to MT6735M Design Notice for details

MARK1 MARK2 MARK3 MARK4 MARK5 MARK6 MARK7

Title	12_BB_2
Size	E
	MTK Confidential
Date:	Thursday, October 09, 2014
Sheet	6 of 26

U1001-G

MT6735-SBS

EMI_IF

DQ0	A12	RDQ0	RCS_B	B4	CS0_N[18] [41]
DQ1	C10	RDQ1	RCS1_B	B3	CS1_N[18] [41]
DQ2	B12	RDQ2			
DQ3	C11	RDQ3	RCKE	D4	CKE[18] [41]
DQ4	B13	RDQ4			
DQ5	D12	RDQ5	RDQM0	D14	DQM0[18] [41]
DQ6	A14	RDQ6	RDQM1	C14	DQM1[18] [41]
DQ7	A15	RDQ7	RDQM2	D7	DQM2[18] [41]
DQ8	B15	RDQ8	RDQM3	C19	DQM3[18] [41]
DQ9	B16	RDQ9			
DQ10	D15	RDQ10	RDQS0	E15	DQS0_T[18] [41]
DQ11	B17	RDQ11	RDQS1	E17	DQS1_T[18] [41]
DQ12	D17	RDQ12	RDQS2	E12	DQS2_T[18] [41]
DQ13	C18	RDQ13	RDQS3	F20	DQS3_T[18] [41]
DQ14	A17	RDQ14			
DQ15	A18	RDQ15	RDQS0_B	F15	DQS0_C[18] [41]
DQ16	A9	RDQ16	RDQS1_B	F17	DQS1_C[18] [41]
DQ17	A8	RDQ17	RDQS2_B	F12	DQS2_C[18] [41]
DQ18	B8	RDQ18	RDQS3_B	E20	DQS3_C[18] [41]
DQ19	B11	RDQ19			
DQ20	B10	RDQ20	RCLK0	F9	CLK0_T[18] [41]
DQ21	C7	RDQ21	RCLK0_B	E9	CLK0_C[18] [41]
DQ22	A11	RDQ22			
DQ23	D9	RDQ23	RA0	D6	CA0
DQ24	D20	RDQ24	RA1	B6	CA1
DQ25	B19	RDQ25	RA2	A3	CA2
DQ26	D21	RDQ26	RA3	A6	CA3
DQ27	A20	RDQ27	RA4	A5	CA4
DQ28	B20	RDQ28	RA5	D2	CA5
DQ29	B22	RDQ29	RA6	C3	CA6
DQ30	B21	RDQ30	RA7	C2	CA7
DQ31	A21	RDQ31	RA8	B2	CA8
			RA9	D1	CA9

U / IC-MT6735-LP3-E1-SBS_MAP0827

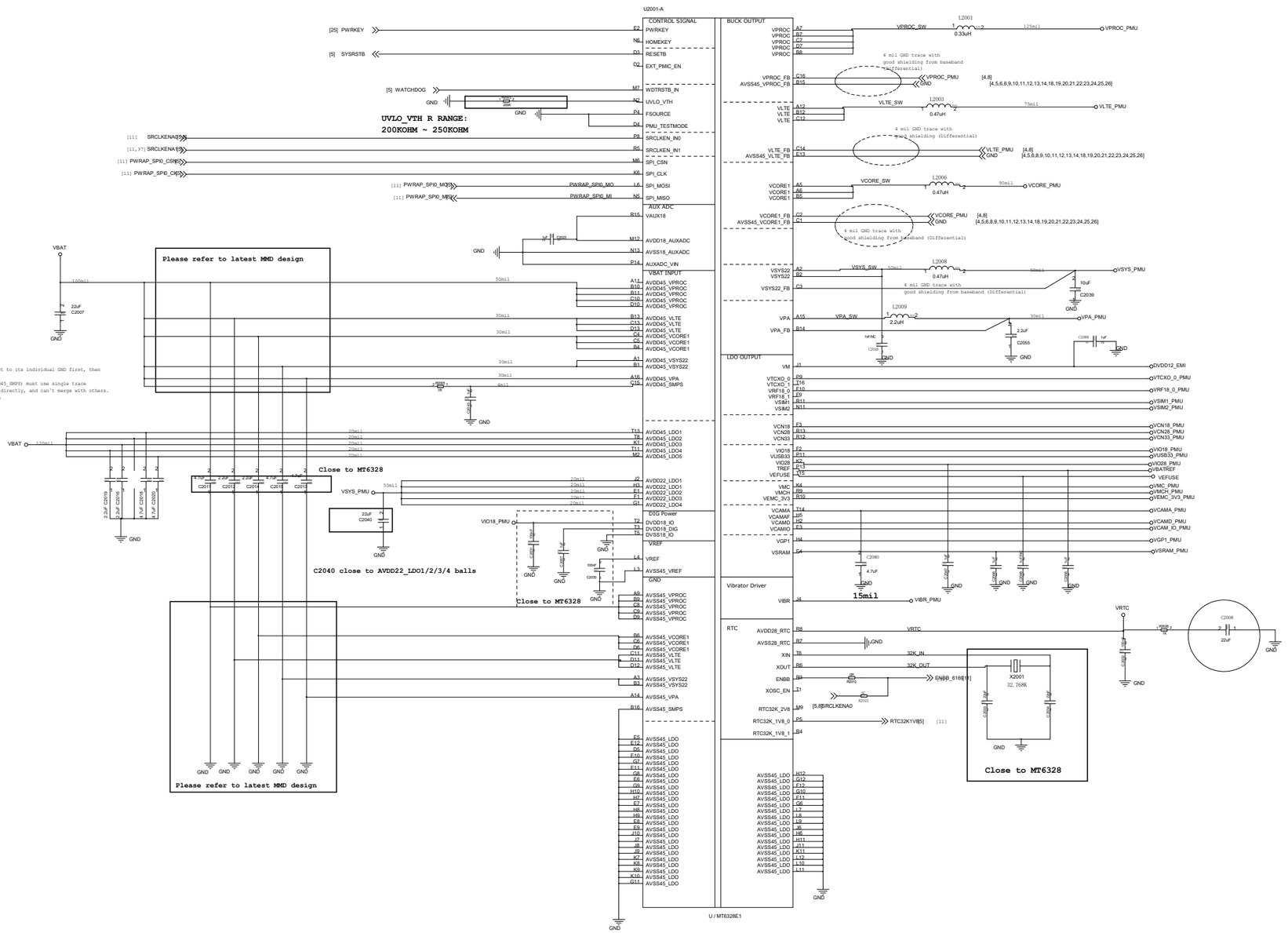
Title
13_BB_3

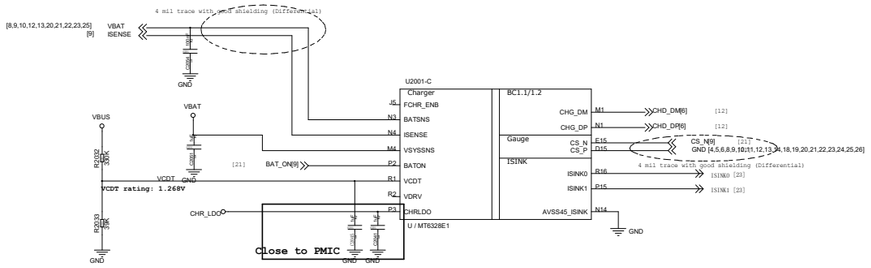
Size
E

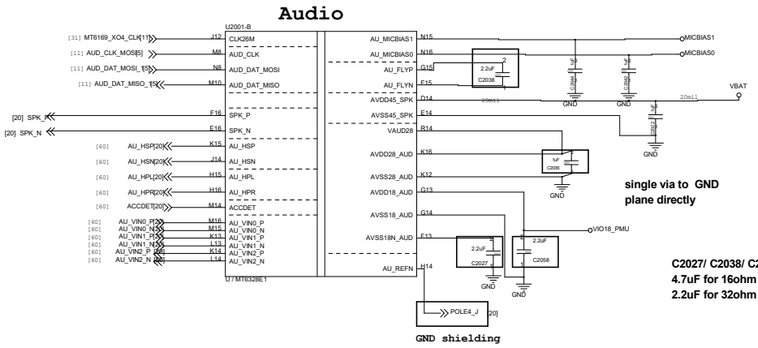
MTK Confidential

Date: Thursday, October 09, 2014 Sheet 7 of 26

Regulator	Output Voltage Range(V)	Output Current(mA)	Input Decoupling Cap	Output Decoupling	Note
VPROC	0.6~1.31	5000	>2.2uF	0.33uH+47uF*2+22uF	≧125mil
VCORE	0.6~1.31	3500	>2.2uF	0.47uH+47uF*2	≧88mil
VLTE	0.6~1.31	2800	>2.2uF	0.47uH+22uF*3	≧63mil
VSYS	2	1900	>2.2uF	0.47uH+22uF+10uF	≧48mil
VPA	0.5~3.4	600	>4.7uF	2.2uH+2.2uF+2.2uF	≧30mil
VM	1.24/1.39/1.54	1000		9.4uF~10uF	L/W=1500mil/25mil
VTCXO_0	2.8	40		1uF~3uF	L/W=2800mil/6mil
VTCXO_1	2.8	40		1uF~3uF	L/W=2800mil/6mil
VRF18_0	1.825	350		2.2~3.3uF	L/W=2800mil/10mil
VRF18_1	1.2/1.3/1.5/1.825	300		2.2~3.3uF	L/W=2800mil/10mil
VSIM1	1.7/1.8/1.86/2.76/3.0/3.1	50		1uF~3uF	L/W=2800mil/6mil
VSIM2	1.7/1.8/1.86/2.76/3.0/3.1	50		1uF~3uF	L/W=2800mil/6mil
VCN18	1.8	150		1uF~3uF	L/W=2800mil/10mil
VCN28	2.8	40		1uF~3uF	L/W=2800mil/6mil
VCN33	3.0/3.1/3.2/3.3/3.4/3.5/3.6	350		4.7uF~5uF	L/W=2800mil/12mil
VIO18	1.8	600		2.2~6.6uF	L/W=2800mil/20mil
VUSB33	3.3	20		1uF~3uF	L/W=2800mil/6mil
VIO28	2.8	200		2.2~6.6uF	L/W=2800mil/10mil
VEFUSE	1.8/1.9/2.0/2.1/2.2	200		1uF~3uF	L/W=2800mil/10mil
VMC	1.8/2.9/3.0/3.3	200		1uF~3uF	L/W=2800mil/10mil
VMCH	2.9/3.0/3.3	800		4.7uF~7uF	L/W=2800mil/20mil
VEMC_3V3	2.9/3.0/3.3	400		4.7uF~7uF	L/W=2800mil/12mil
VCAMA	1.5/1.8/2.5/2.8	200		2~3.3uF	L/W=2800mil/10mil
VCAMAF	1.2/1.3/1.5/1.8/2.0/2.8/3.0/3.3	200		2~3.3uF	L/W=2800mil/10mil
VCAMD	0.9/1.0/1.1/1.22/1.3/1.5	500		4.4uF~6.9uF	L/W=2800mil/16mil
VCAMIO	1.2/1.3/1.5/1.8	200		1uF~3uF	L/W=2800mil/10mil
VGP1	1.2/1.3/1.5/1.8/2.5/2.8/3.0/3.3	200		1uF~3uF	L/W=2800mil/10mil
VSRAM	0.6~1.31	400		4.7uF~7uF	L/W=2800mil/12mil
VIBR	1.2/1.3/1.5/1.8/2.0/2.8/3.0/3.3	100		1uF~3uF	L/W=2800mil/8mil
VAUX18	1.8	40		1uF~3uF	L/W=2800mil/6mil
VAUD28	2.8	40		1uF~3uF	L/W=2800mil/6mil
DVDD18_DIG	1.8	20		1uF	L/W=800mil/4mil
VRTC	2.8	2		0.1uF	L/W=800mil/4mil

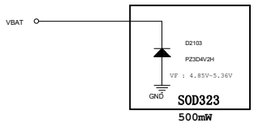


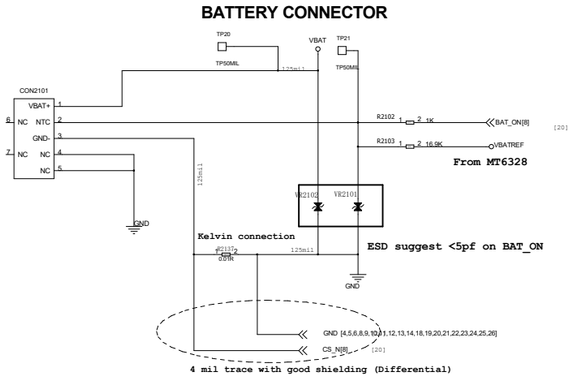




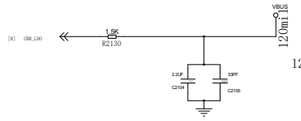
VIBR

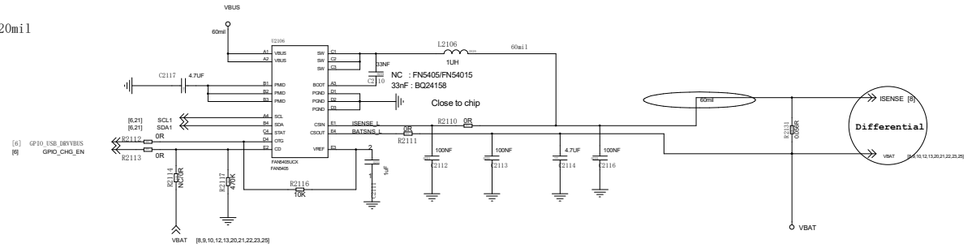
Title	20_POWER_MT6328
Size: E	MTK Confidential
Date: Thursday, October 09, 2014	Sheet 8 of 26





Charger





Cheap

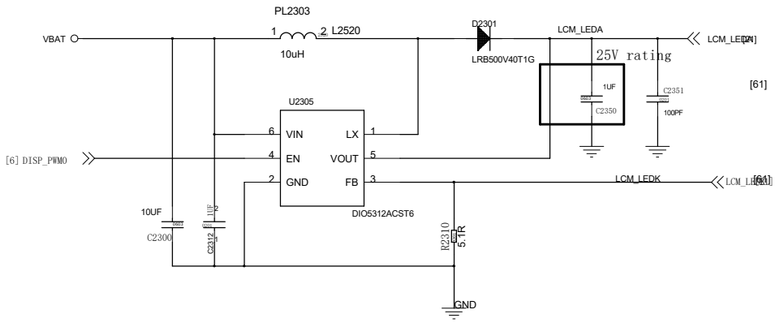
RESET CPU

Rest

If switching charger is used:
(1) R404~R412, C403~C408, L401, U402 are needed
(2) U303, U305 change to NC
(3) R328 change to 56m Ohm
(4) R409/R404 default use: FN5405/FN54015/BQ24158 (R411:NC)
R411: RT9450B (R409: NC)

Title	21_POWER_TBD	
Size E	MTK Confidential	
Date: Thursday, October 09, 2014	Sheet 9 of 26	

LCM Backlight LED Driver



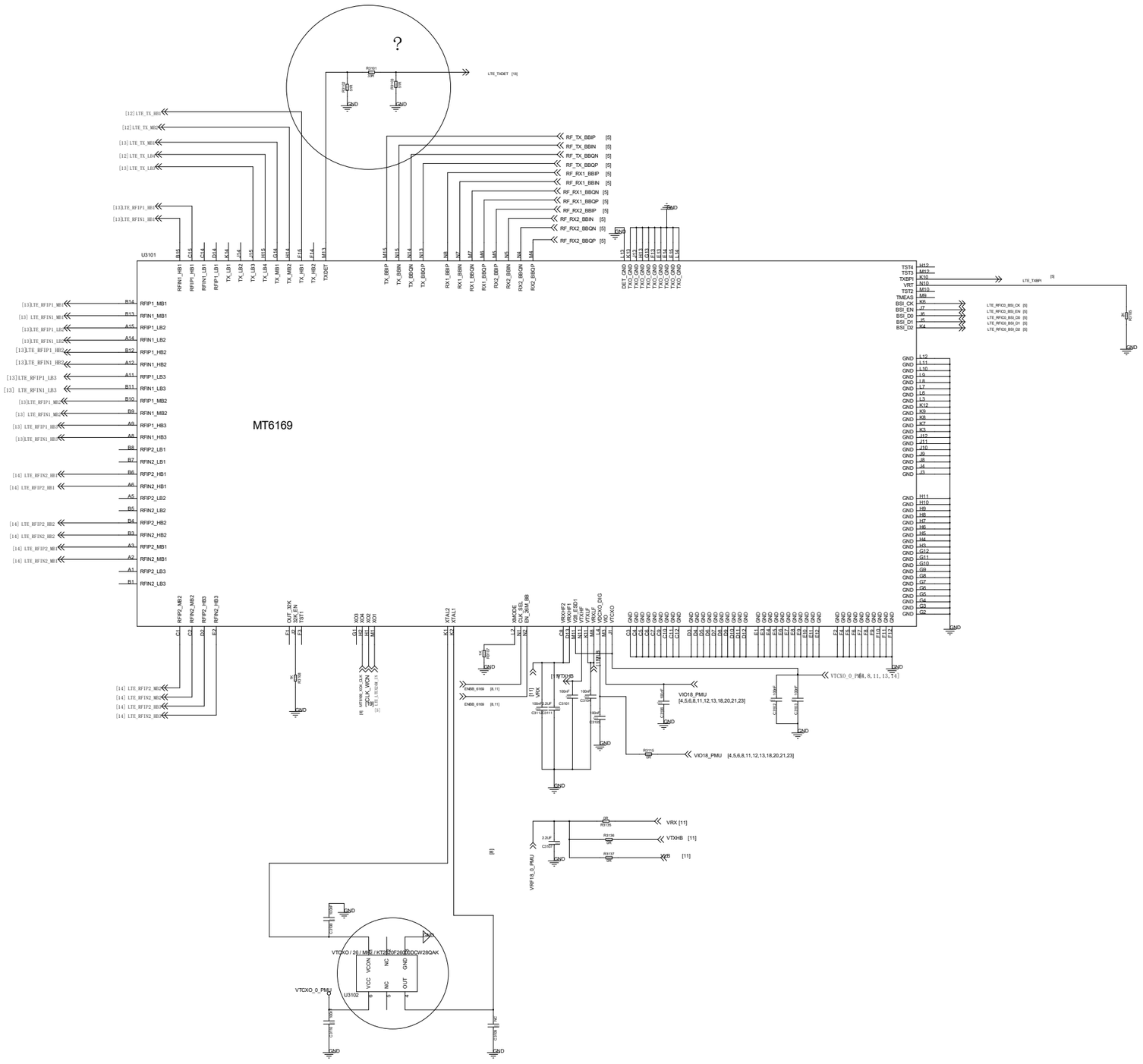
VOUT max. : 38V
Switch Frequency : 5KHz~100KHz
VFB : 200mV

Flash LED 5V Boost

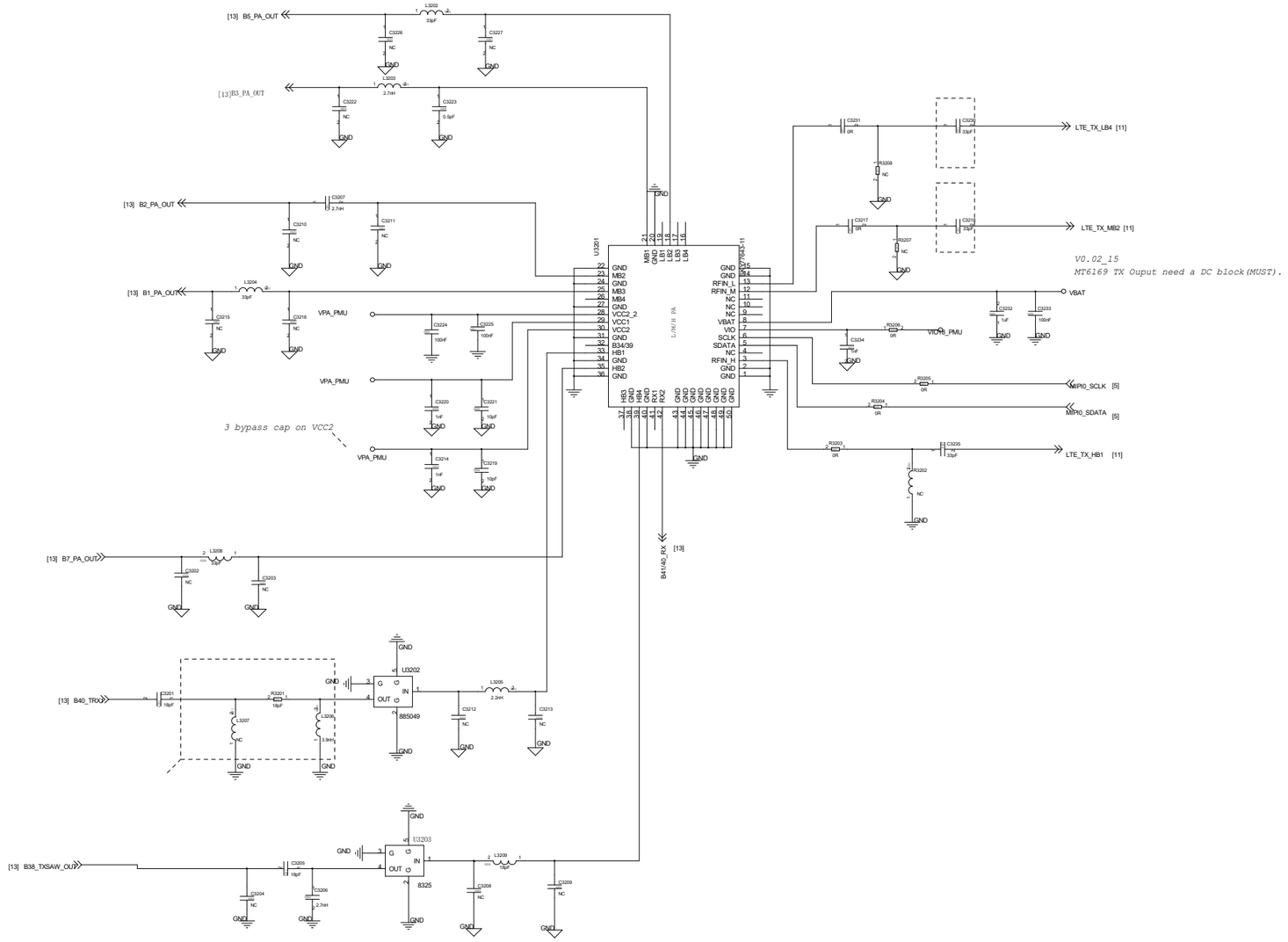
Flash LED I2C address: 0X63 (Write:0xC6, Read:0xC7)

Title	23_POWER_THIRD-PARTY		
Size E	MTK Confidential		
Date:	Thursday, October 09, 2014	Sheet 10	of 26

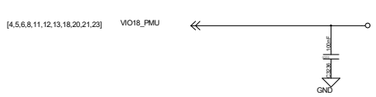
REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:



DRAWN:	DATED:	COMPANY:	
		TITLE:	
CHECKED:	DATED:		
QUALITY CONTROL:	DATED:	CODE: / SIZE: E / DRAWING NO: / REV:	
RELEASED:	DATED:	SCALE:	SHEET: 1 of 26



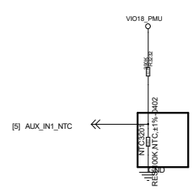
[4,5,6,8,11,12,13,18,20,21,23] VIO18_PMU

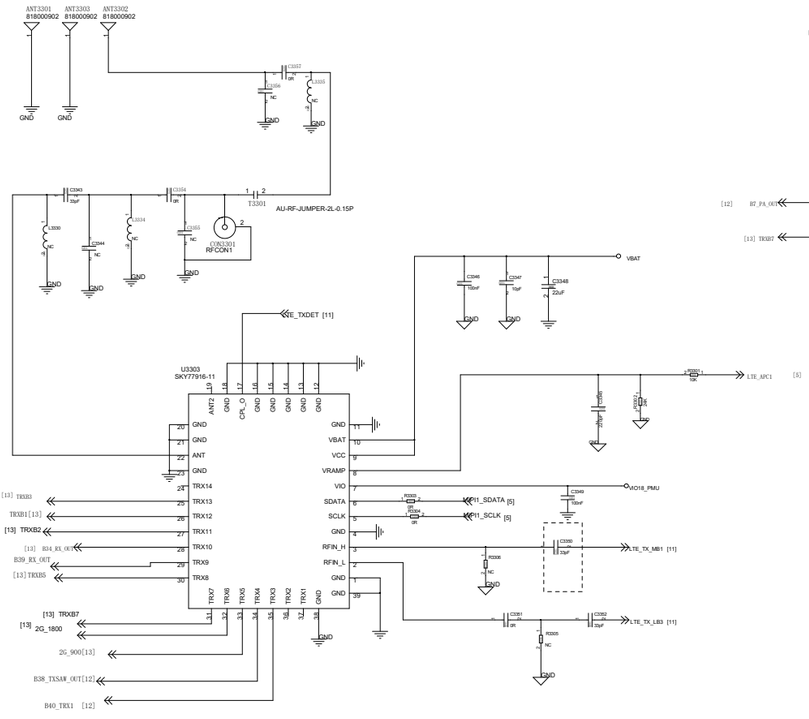


Power Net Connection

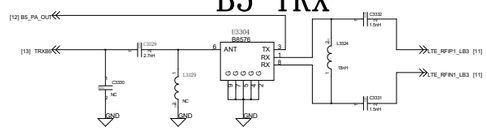
VPA_VCC1: 10mil
VPA_PMU,
VPA_VCC2,
VPA_VCC2_B7,

VBAT : 80mil

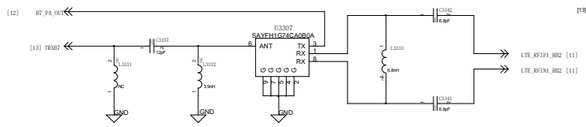




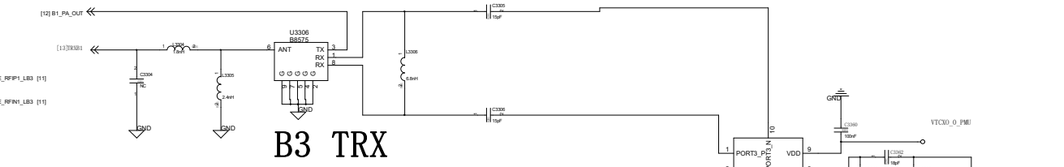
B5 TRX



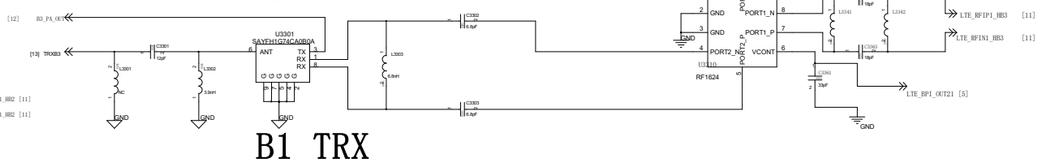
B7 TRX



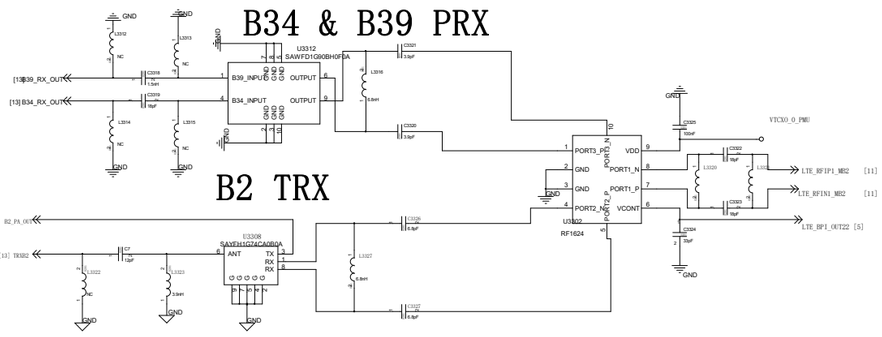
B3 TRX



B1 TRX

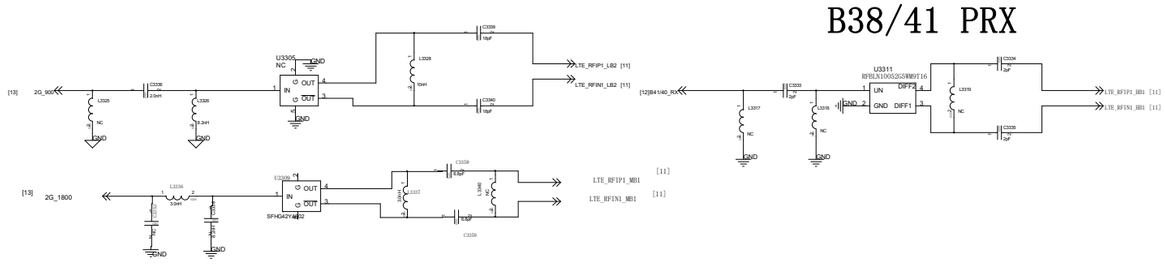


B34 & B39 PRX



B2 TRX

B38/41 PRX

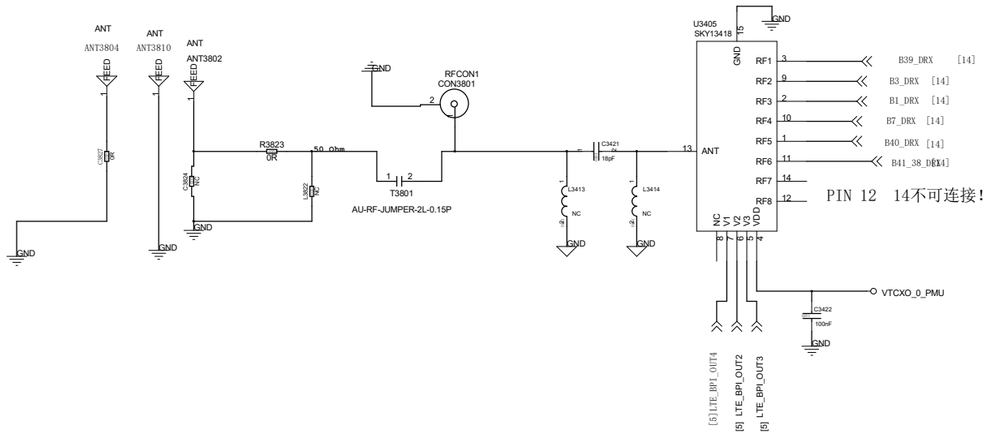


[31]

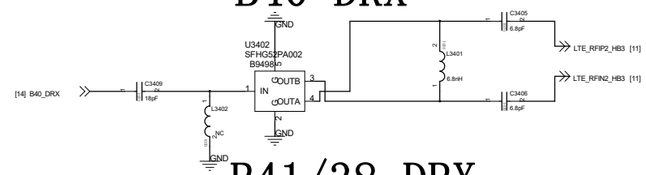
[31]

Title	33_RF_MT6169_RF_PRX
Size: E	MTK Confidential
Date: Monday, March 17, 2014	Sheet 15 of 26

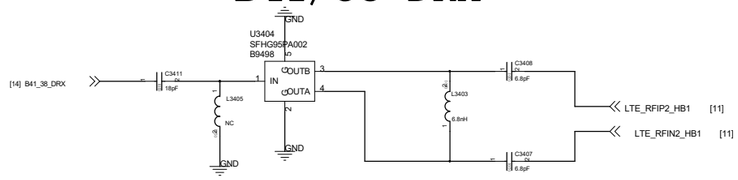
DRX ANT: 704~2690MHz



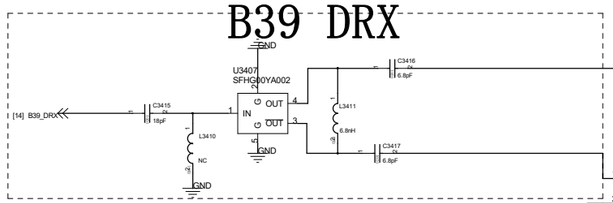
B40 DRX



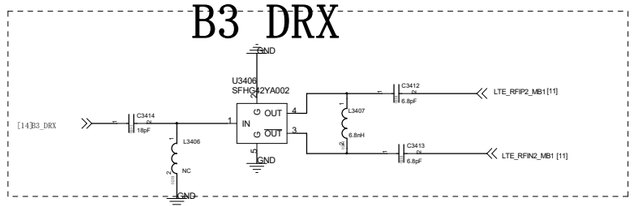
B41/38 DRX



B39 DRX

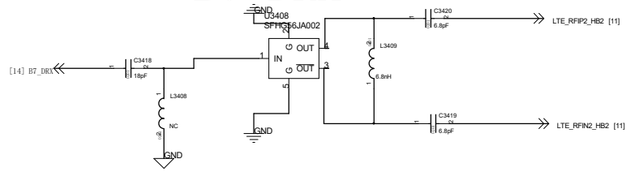


B3 DRX



B1 DRX

B7 DRX



Title	34_RF_MT6169_RF_DRX
Size E	MTK Confidential
Date: Monday, March 17, 2014	Sheet 14 of 26

5

4

3

2

1

eMMC+LPDDR3

221 Ball, 0.5mm pitch

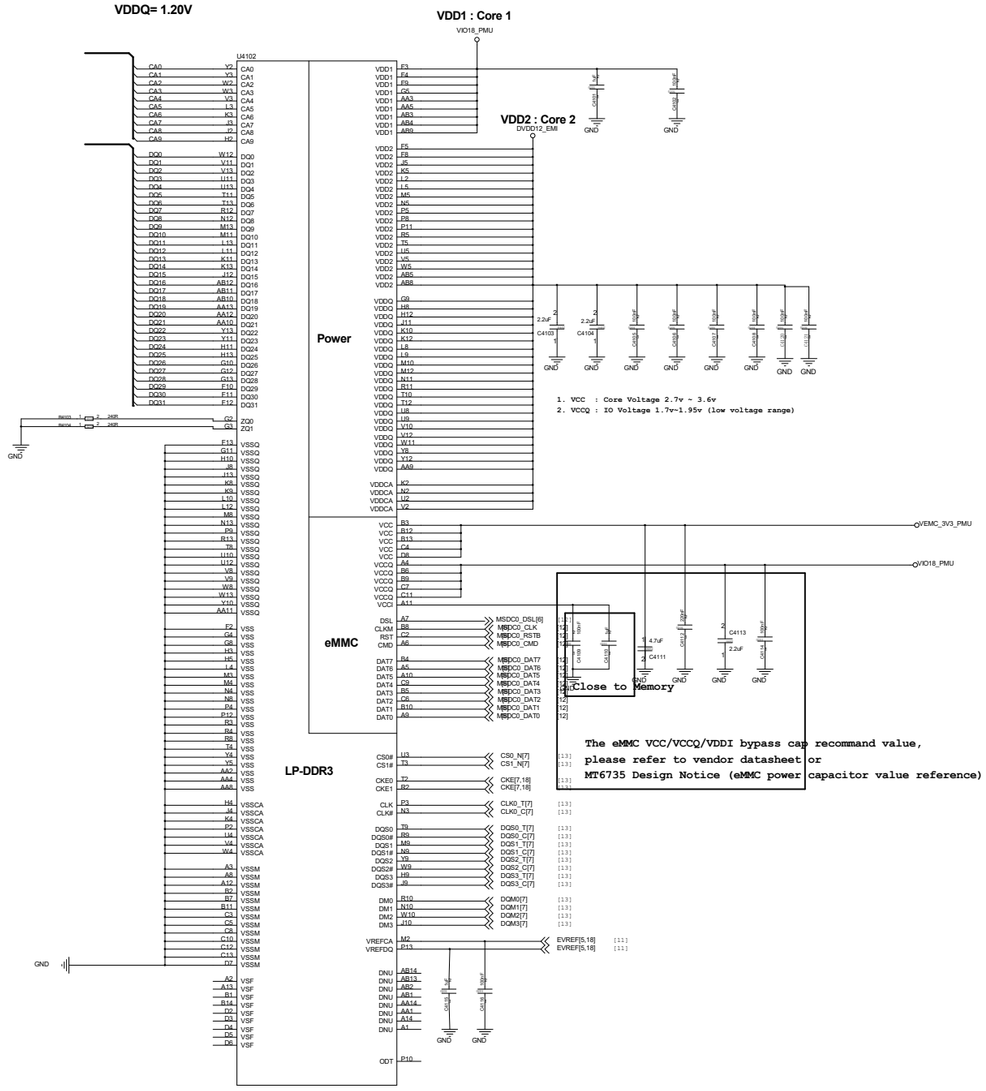
VDD1=1.8V
VDD2=1.20V
VDDCA=1.2V
VDDQ= 1.20V

8GB eMMC + 8Gb LPDDR3

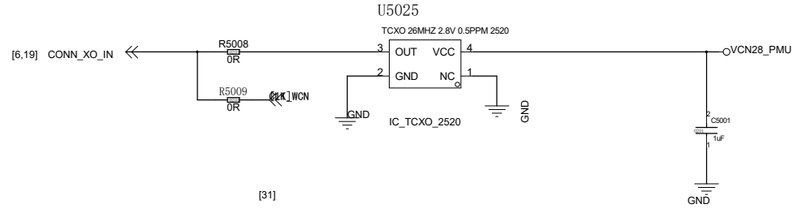
Hynix/H9TQ64A8GTMCUR-KUM

Connect to AP	
DQ[0..31]	DQ[0..31]
CA[0..9]	CA[0..9]
CS0_N	CS0_N
CS1_N	CS1_N
CKE	CKE
DQM0	DQM0
DQM1	DQM1
DQM2	DQM2
DQM3	DQM3
DQS0_C	DQS0_C
DQS1_C	DQS1_C
DQS2_C	DQS2_C
DQS3_C	DQS3_C
DQS0_T	DQS0_T
DQS1_T	DQS1_T
DQS2_T	DQS2_T
DQS3_T	DQS3_T
CLK0_T	CLK0_T
CLK0_C	CLK0_C
VREF_CA	VREF_CA
VREF_DQ	VREF_DQ
MSDC0_RSTB	MSDC0_RSTB
MSDC0_CMD	MSDC0_CMD
MSDC0_CLK	MSDC0_CLK
MSDC0_DSL	MSDC0_DSL
MSDC0_DAT0	MSDC0_DAT0
MSDC0_DAT1	MSDC0_DAT1
MSDC0_DAT2	MSDC0_DAT2
MSDC0_DAT3	MSDC0_DAT3
MSDC0_DAT4	MSDC0_DAT4
MSDC0_DAT5	MSDC0_DAT5
MSDC0_DAT6	MSDC0_DAT6
MSDC0_DAT7	MSDC0_DAT7

Power I/F	
VIO18_PMU	VIO18_PMU
VEMC_3V3_PMU	VEMC_3V3_PMU
DVDD12_EMI	DVDD12_EMI



Title	41_Memory_eMMC_LPDDR3
Size	E
	MTK Confidential
Date:	Thursday, October 09, 2014
Sheet	18 of 26

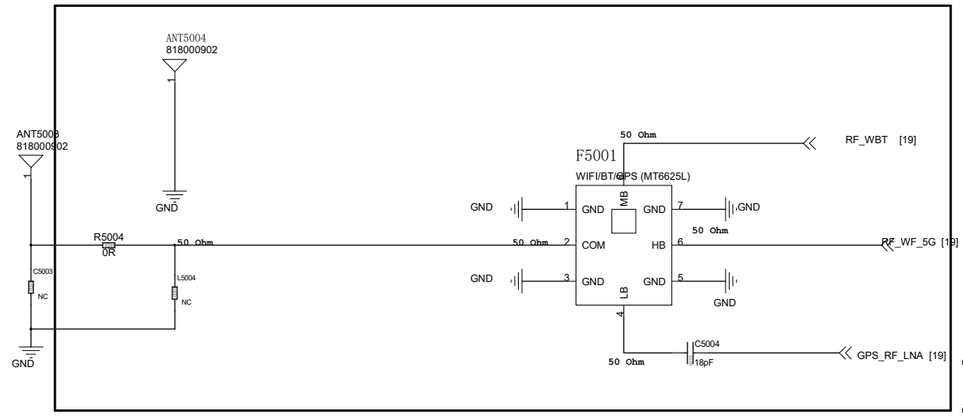


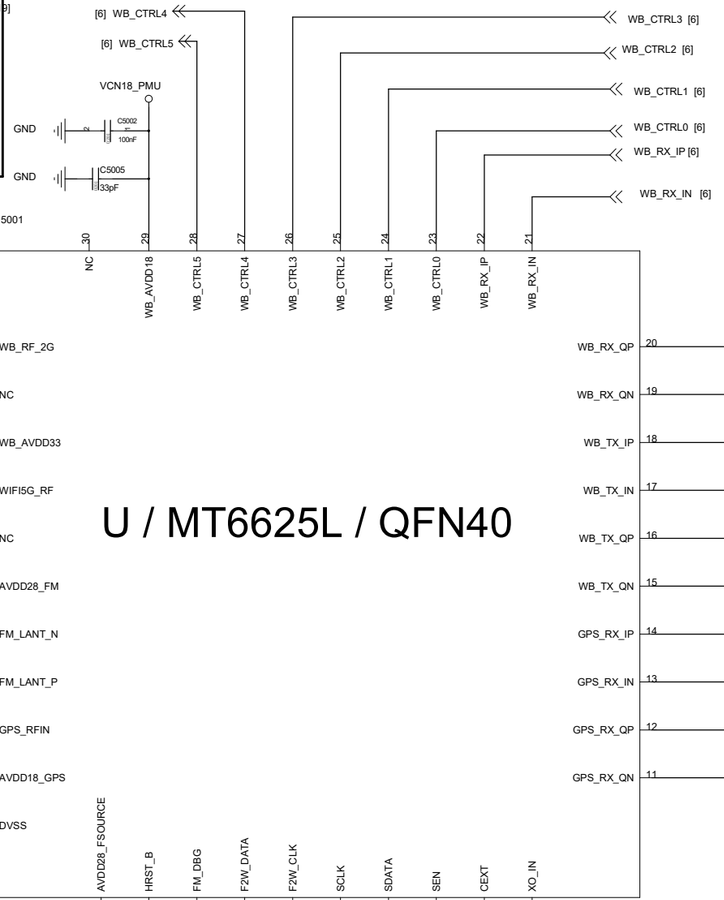
[31]

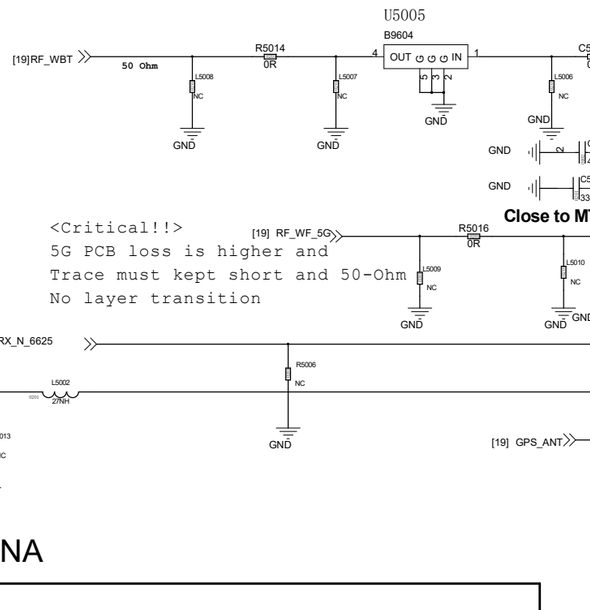
Close to Antenna

Same layer as Antenna, 50ohm trace reference to 3rd layer GND(2nd Layer clean)

Reserve Keep out region from L1 to Main GND layer





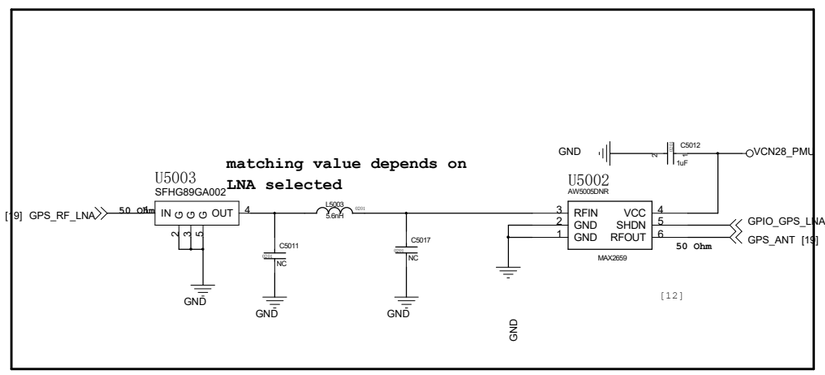


Close to MT6625

U / MT6625L / QFN40

GPS xLNA

Close to ANT



Same layer as Antenna, 50ohm trace reference to 3rd layer GND(2nd Layer clean)

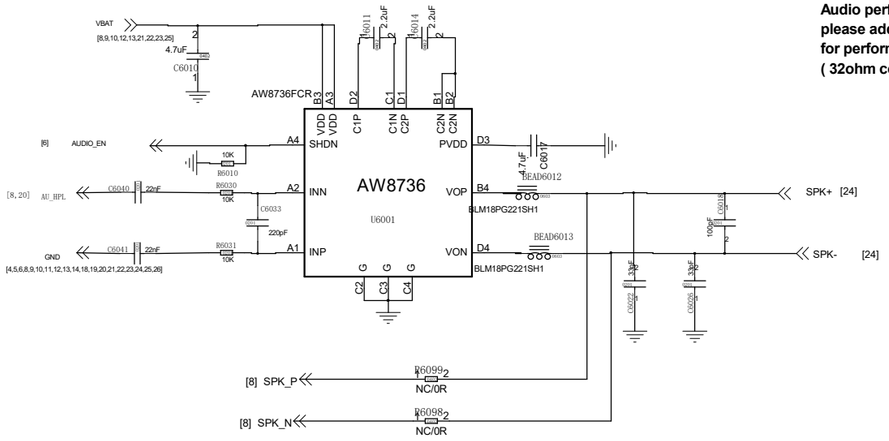
Title	50_CONNECTIVITY_MT6625	
Size E	MTK Confidential	
Date: Thursday, October 09, 2014	Sheet 19	of 26

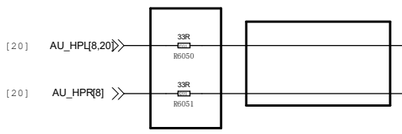
Earphone Audio

Based on your system level design , if better Audio performance is needed on your system, please add 32ohm to audio path for performance enhance proposal (32ohm condition pop noise can improve 6dB)

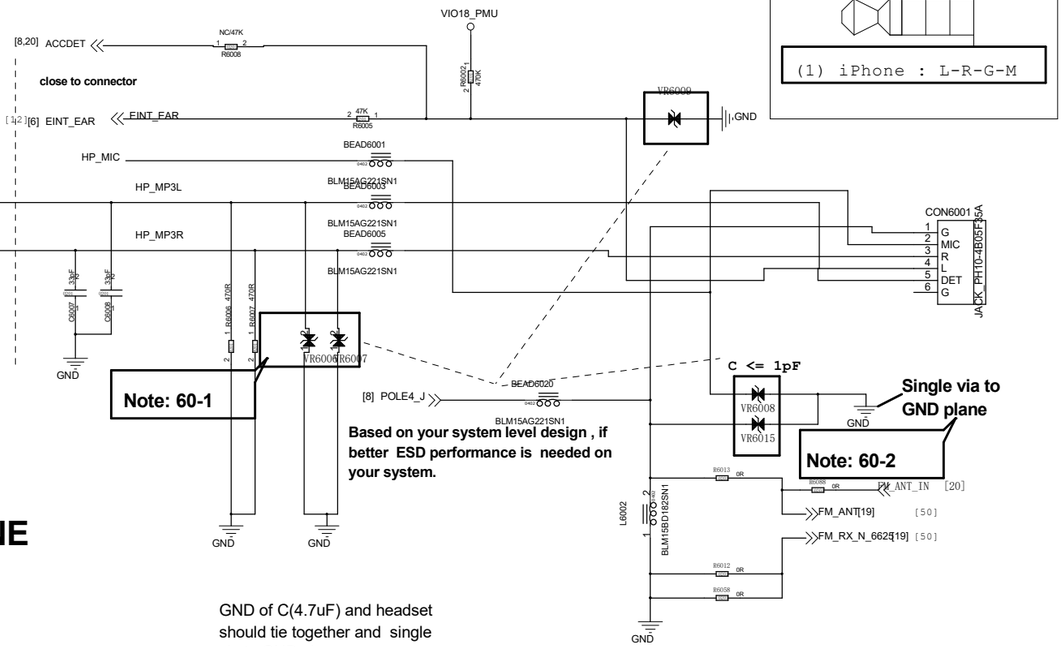
close to IC

close to connector

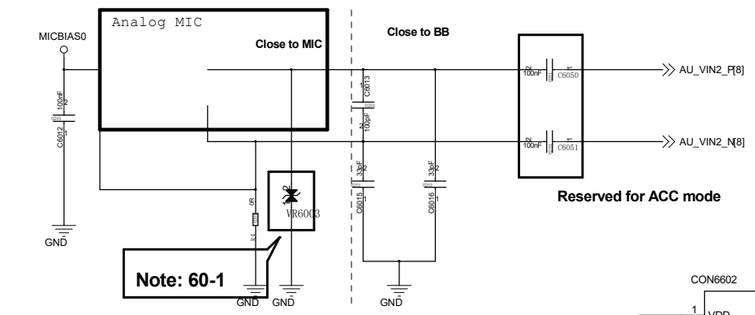




BEAD6002 / BEAD6004 are for FM-desense tuning proposal

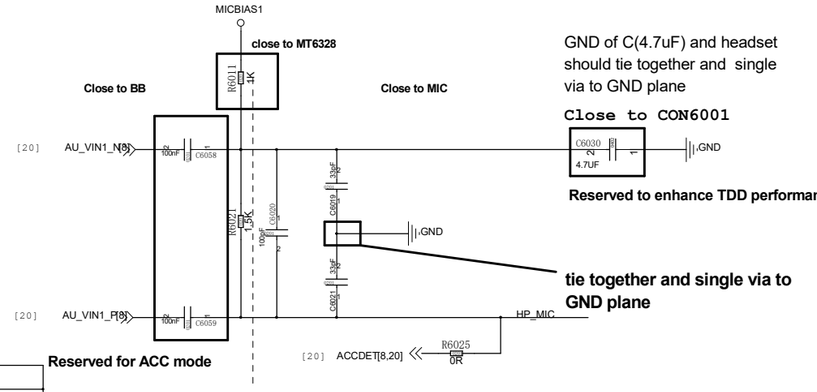


Handset Microphone 2



together then single via to main GND

Earphone MICPHONE

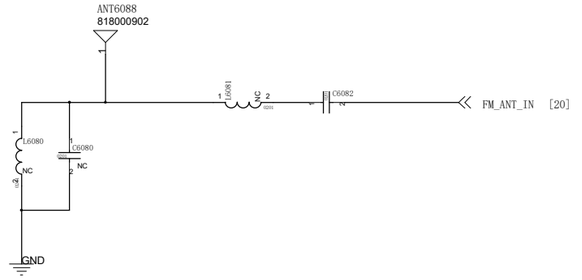


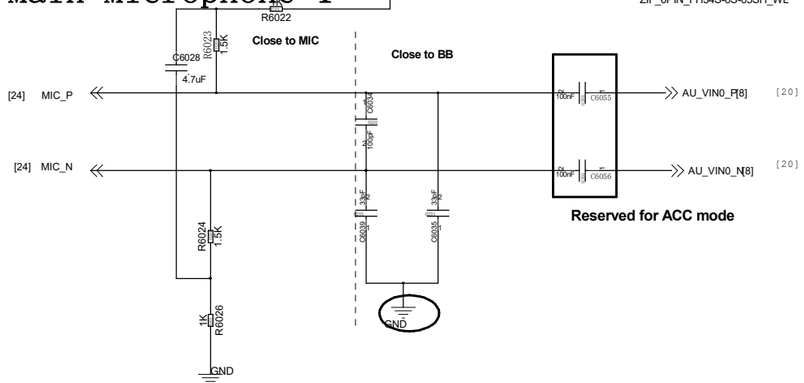
GND of C(4.7uF) and headset should tie together and single via to GND plane

Close to CON6001

Reserved to enhance TDD performance

tie together and single via to GND plane

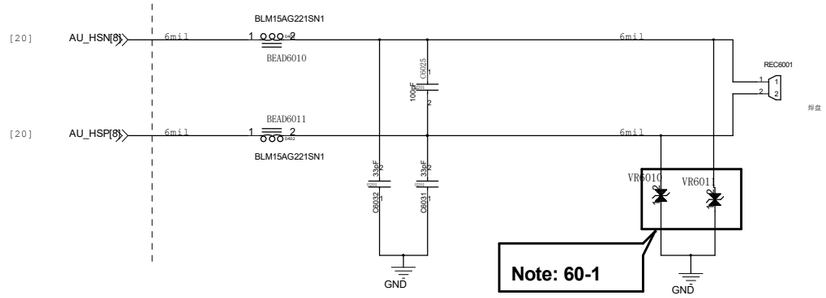




Receiver

close to IC

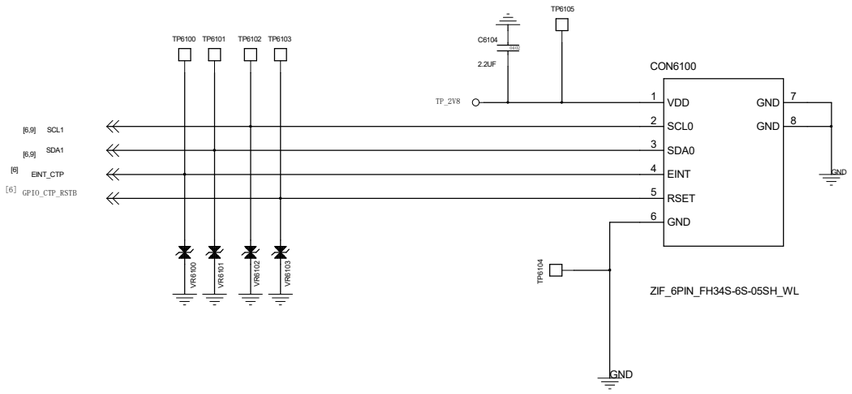
close to connector

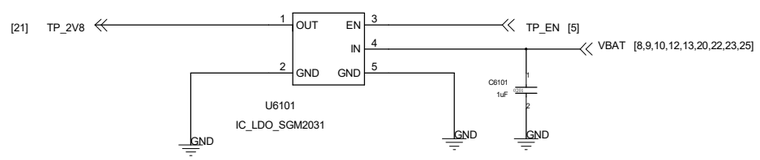


Based on your system level design , if better ESD performance is needed on your system.

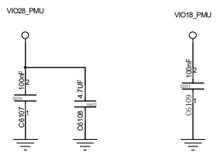
Title	60_PERI_AUDIO_IO
Size	E
	MTK Confidential
Date:	Thursday, October 09, 2014
Sheet	20 of 26

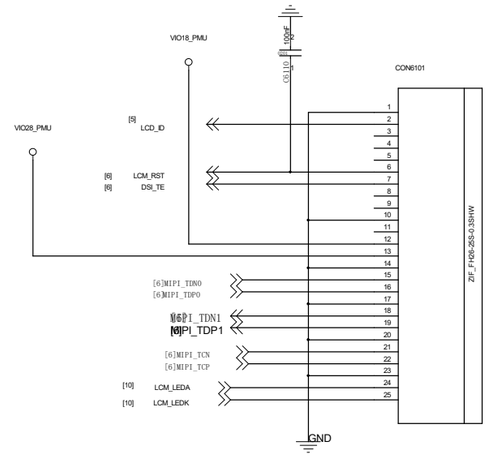
CTP Connector





Main LCM





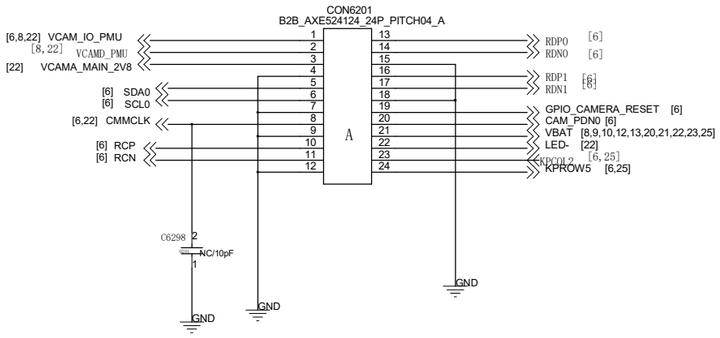
Schematic design notice of "61_PERI_LCD_CTP" page.

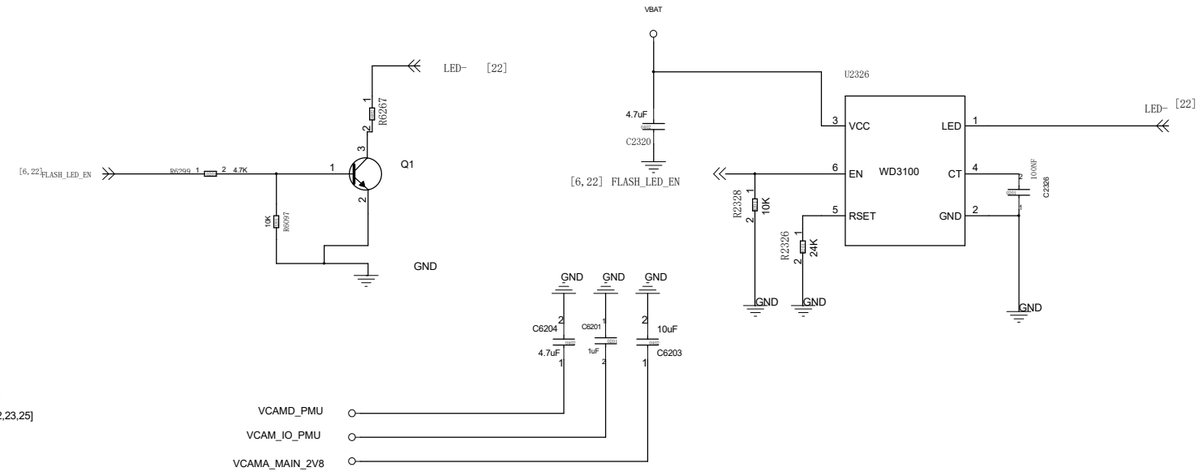
Note 61-1: GT1151 I2C address: 0X5D (Write:0xBA, Read:0xBB)
or 0x14 (Write:0x28, Read:0x29)

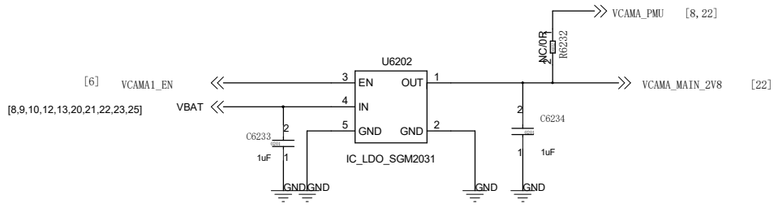
Title	61_PERI_LCD_CTP
Size E	MTK Confidential
Date: Thursday, October 09, 2014	Sheet 21 of 26

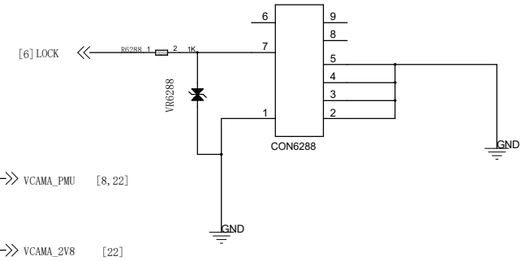
Rear Camera

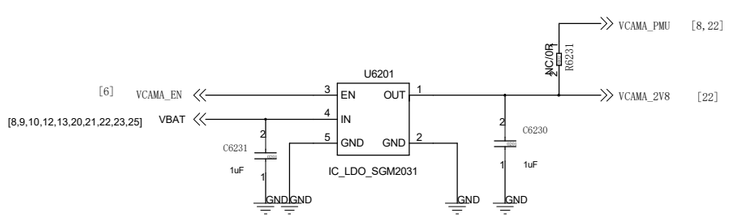
Rear camera (IMX135) I2C address: 0X10 (Write:0x20, Read:0x21)
AF driver (DW9714A) I2C address: 0x0C (Write:0x18 , Read:0x19)





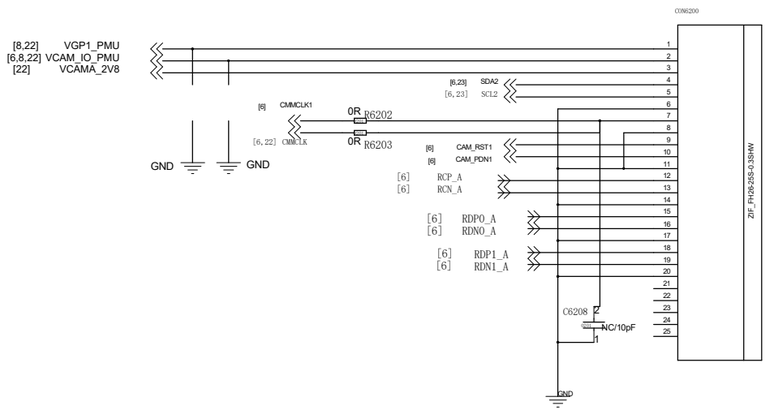


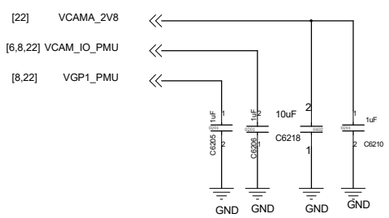


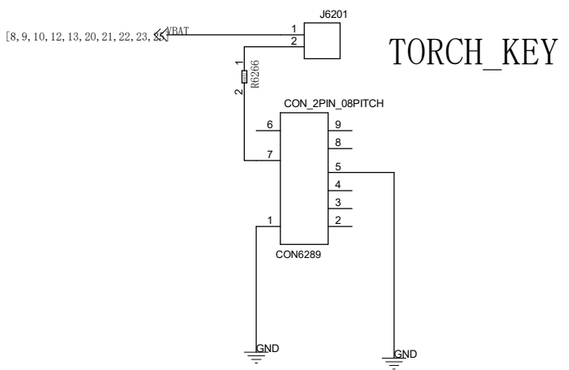


Front Camera

Front camera (GC2355) I2C address: 0x3C (Write:0x78, Read:0x79)





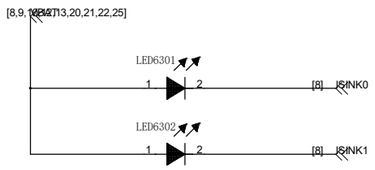


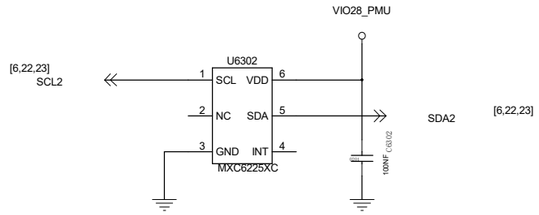
TORCH_KEY

Title	62_PERI_CAMERA	
Size E	MTK Confidential	
Date: Thursday, October 09, 2014	Sheet 22 of 26	

M-Sensor

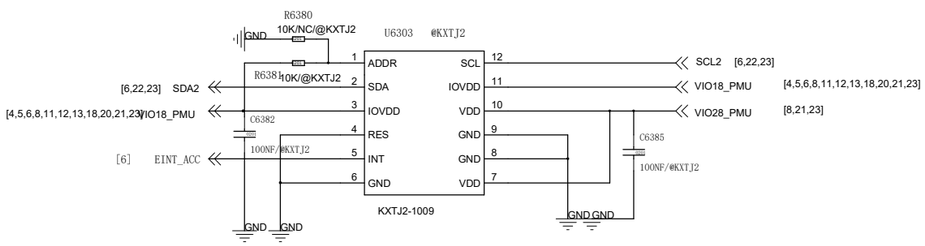
M-Sensor I2C Address: 0x0D (Write:0x1A, Read:0x1B)



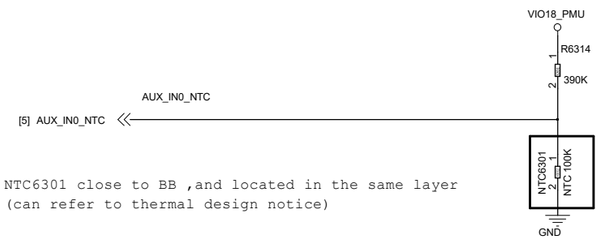


Accelerometer

MC3410 / Accelerometer I2C address: 0x4C (Write:0x98, Read:0x99)



Thermistor / To sense board level temperature



NTC6301 close to BB ,and located in the same layer
(can refer to thermal design notice)

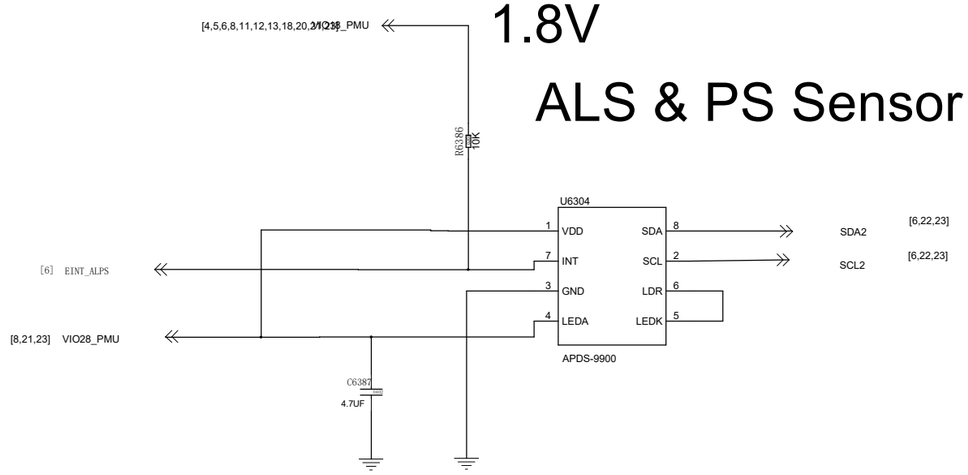
	PCB	Note
AUX_IN0_NTC	AP	Keep 5-8 mm to AP, and far to other heat source

ALS & PS Sensor

CM36652 / RGB + PS I2C address: 0X60 (Write:0xC0, Read:0xC1)

1.8V

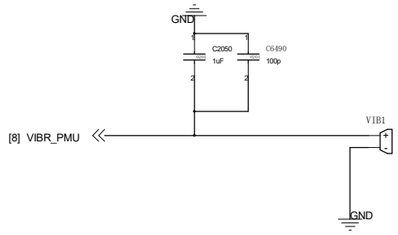
ALS & PS Sensor

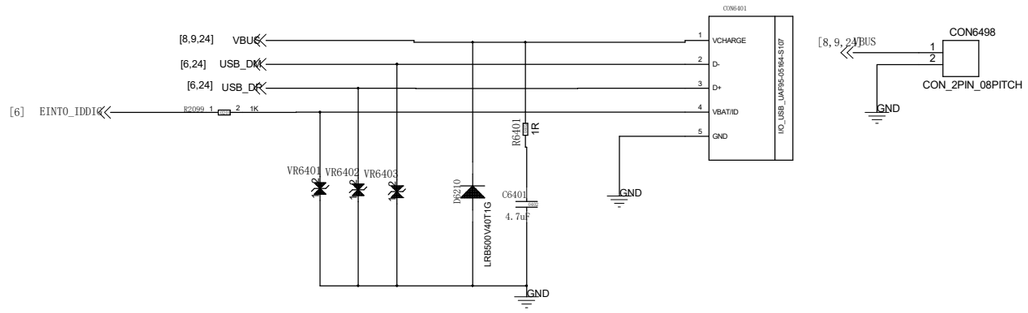


Title: 63_PERI_SENSORS
Size: E
MTK Confidential
Date: Thursday, October 09, 2014
Sheet 23 of 26

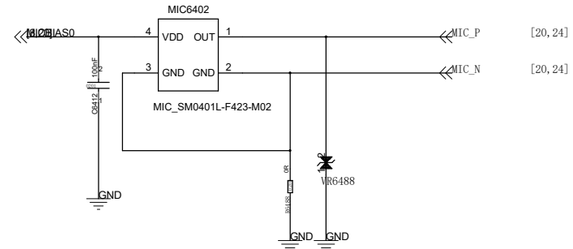
Sub Connector

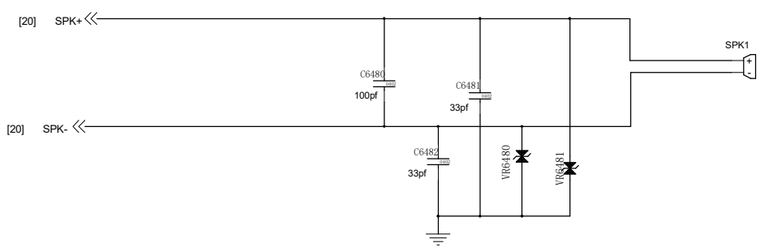
80mil

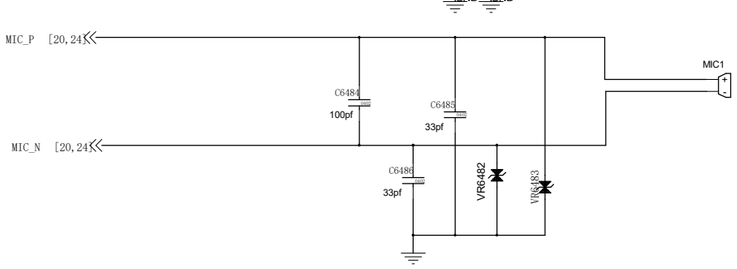


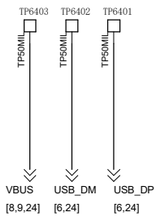


SUB need add ESD









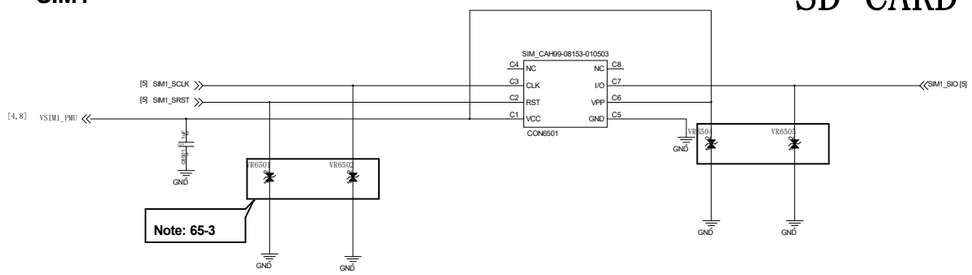
Schematic design notice of "64_PERI_USB_MHL" page.

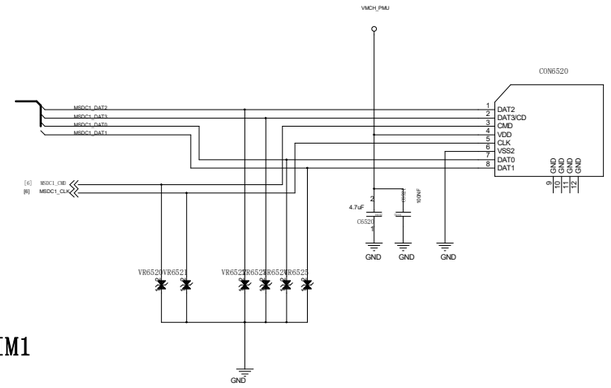
The equivalent capacitance of USB2.0 ESD protection device must be <=3pF.
For D+/D- 2-ch TVS device is also available for smaller layout area

Title	64_PERI_USB_MHL
Size E	MTK Confidential
Date: Thursday, October 09, 2014	Sheet 24 of 26

SD CARD

SIM1

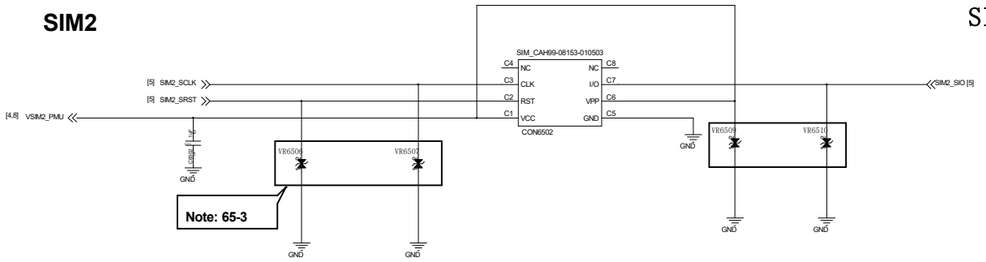




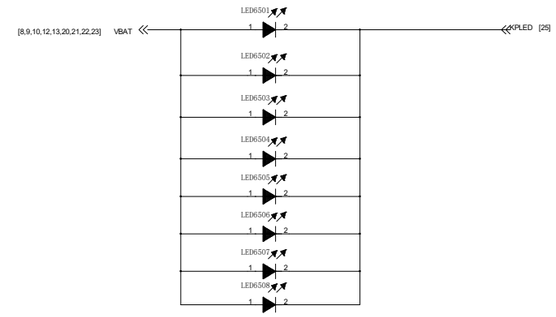
SIM1

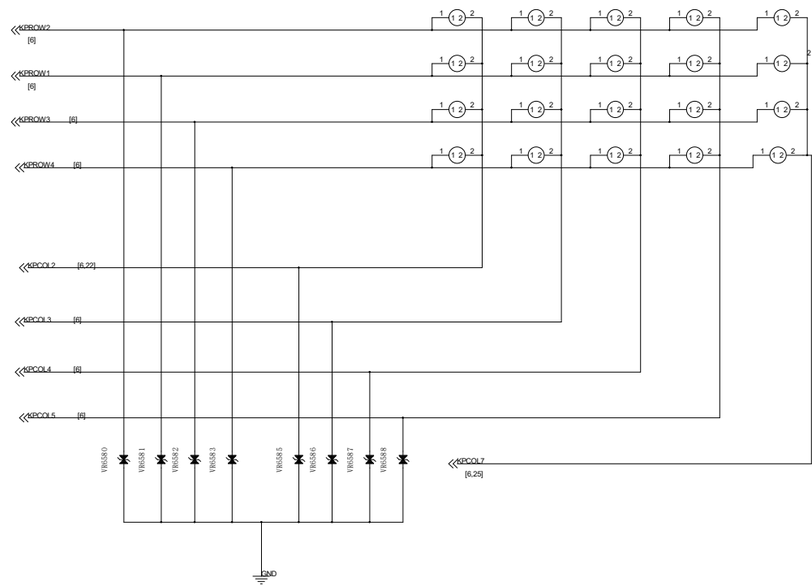
Based on your system level design , if better ESD performance is needed on your system.

SIM2

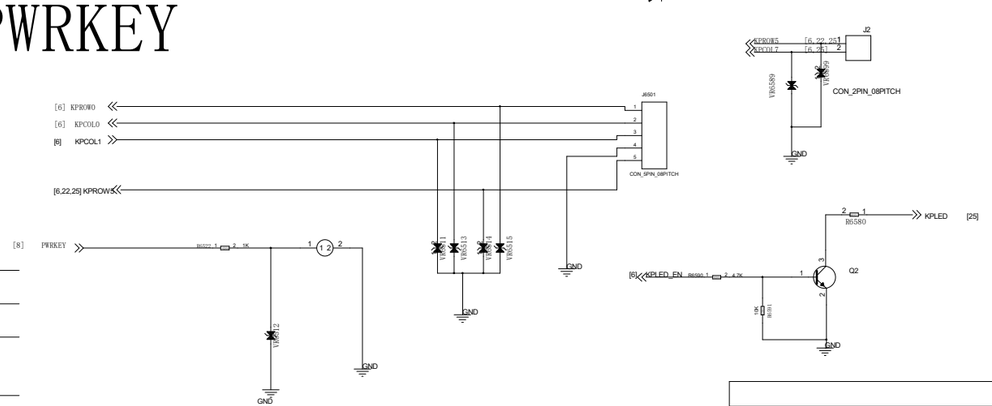


SIM2





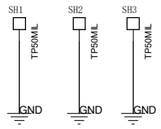
PWRKEY



Schematic design notice of "65_PERI_Dual_SIM_ICUSB_KEYPAD" page.

Note 65-1:	DO NOT put pull-up resistor on PWRKEY
Note 65-2:	Volume Up : HOME Key / GND Volume Down : KPROW0/KPCOL0
Note 65-3:	The equivalent capacitance of SIM ESD protection device must be <=22pF. But for NFC app. equivalent capacitance of NFC_SWP should <=0.5pF.

Title	65_PERI_Dual_SIM_KEYPAD
Size: E	MTK Confidential
Date: Thursday, October 09, 2014	Sheet 25 of 26



Title	66_PERI_VIBRATOR
Size: E	MTK Confidential
Date: Thursday, October 09, 2014	Sheet 26 of 26