Table of Contents

1. Features

- Low dark current
- Auto black level calibration
- Two wire serial interface, 16-bit address and 8-bit data
- Support output format: YCbCr (4:2:2), RGB565, RGB555, RGB444 and Raw
- Support image size: UXGA (1600 by 1200) and any size from scaling down
- Lens shading correction
- Automatic control functions: Auto-Exposure control(AE), Auto-White Balance(AWB)
- Including: Sharpness, noise reduction, defect correction, gamma, color saturation adjust.
- Specical effects included.
- Anti-Shake
- Embedded 1.5V regulator for core power
- Target module size: 6.5mm x 6.5mm

2. Key Performance

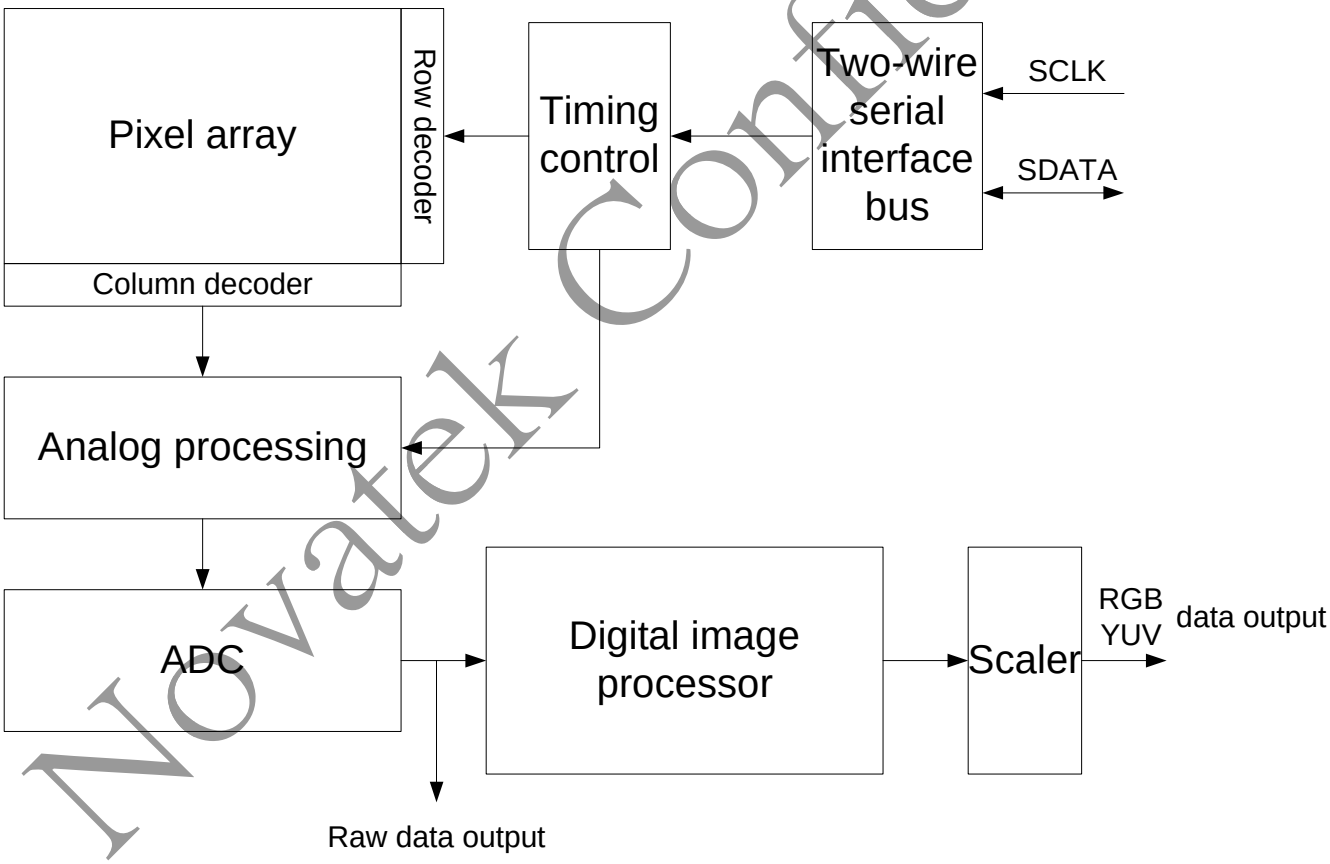
Parameter		Value
Array Size		1600 x 1200
Power Supply	Digital	1.5V ± 5%
	Analog	2.5V ~ 3.1V
	I/O	1.7V ~ 3.1V
Pixel Size		1.75 μm x 1.75 μm
Image Area		2814 μm x 2114 μm
SNR_{MAX}		35dB
Dynamic Range		56dB
Responsivity		1060 mV/Lux-sec
ADC Resolution		10 bits
Shutter		Electronic Rolling Shutter
Frame rate	SVGA	30 fps
	UXGA	10 fps
Color Filter Arrays		RGB Bayer pattern
Maximum Data Rate		24 Mp/s
Maximum Clock Rate		48 MHz
Power Consumption		112mW at 10fps, 48MHz, Full frame
		108mW at 30fps, 48MHz, SVGA
		Standby: 15uA

3. General Description

The NT99250 is a high performance image sensor. It incorporates a 1600 (H) x 1200 (V) image array, an on-chip PLL oscillator and an on-chip 10 bits ADC, and embedded image signal processor. All the required image signal processing functions, including sharpness, noise reduction, defect correction, gamma, and color saturation adjust are supported. User can easily control through two-wire serial interface bus.

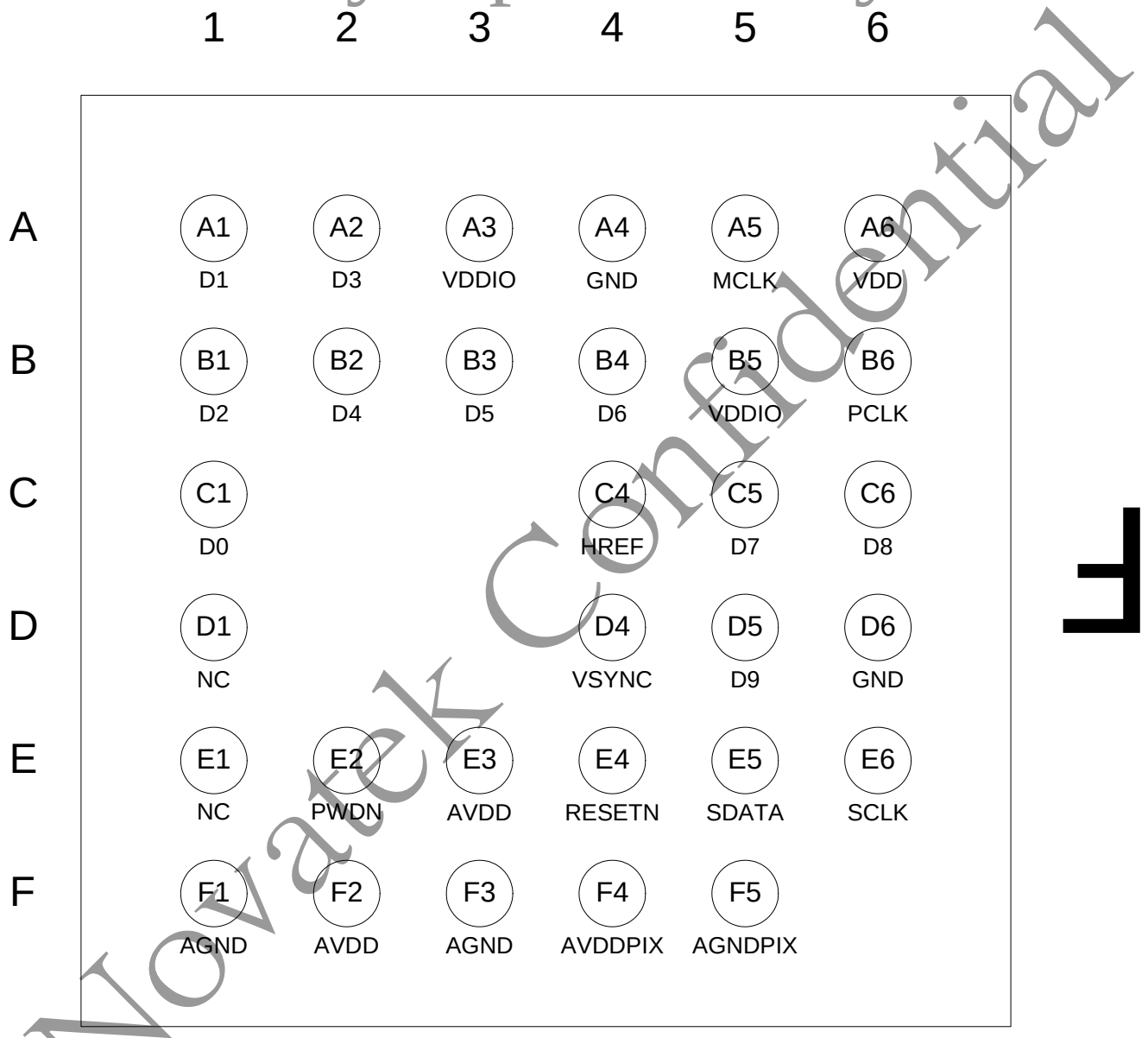
It is suitable for cellular phones and PC cameras applications.

4. Block Diagram



5. Pin Configuration

(Top view)



6. Pin Descriptions

I = input port

O = output port with normal driving/sinking

I/O = bi-directional port with normal driving/sinking

p/u = internal pull-up

p/d = internal pull-down

The Reset column below means the pin's default state after power on reset.

Pin No.	Name	Type	Reset	Descriptions
A1	D1	O	-	Data output 1
A2	D3	O	-	Data output 3
A3	VDDIO	Power	-	Digital power for I/O
A4	GND	Ground	-	Digital ground
A5	MCLK	I	-	System clock input
A6	VDD	Power	-	Digital power
B1	D2	O	-	Data output 2
B2	D4	O	-	Data output 4
B3	D5	O	-	Data output 5
B4	D6	O	-	Data output 6
B5	VDDIO	Power	-	Digital power for I/O
B6	PCLK	O	-	Pixel clock output
C1	D0	O	-	Data output 0
C4	HREF	O	-	Horizontal reference
C5	D7	O	-	Data output 7
C6	D8	O	-	Data output 8
D1	NC	-	-	NC
D4	VSYNC	O	-	Vertical synchronization
D5	D9	O	-	Data output 9
D6	GND	Ground	-	Digital ground
E1	NC	-	-	NC
E2	PWDN	I	-	Power down mode select, active high 0: normal mode 1: power down mode
E3	AVDD	Power	-	Analog power
E4	RESETN	I	-	Power on reset, active low 0: reset 1: normal
E5	SDATA	I/O	p/u	Two-wire serial interface bus data I/O
E6	SCLK	I	p/u	Two-wire serial interface bus clock input
F1	AGND	Ground	-	Analog ground
F2	AVDD	Power	-	Analog power
F3	AGND	Ground	-	Analog ground
F4	AVDDPIX	Power	-	Pixel power
F5	AGNDPIX	Ground	-	Pixel ground

7. Package Outline

	Symbol	Nominal	Min.	Max.
			µm	
Package Body Dimension X	A	4110	4085	4135
Package Body Dimension Y	B	4110	4085	4135
Package Height	C	780	720	840
Ball Height	C1	160	130	190
Package Body Thickness	C2	620	575	665
Thickness of Glass surface to wafer	C3	445	425	465
Ball Diameter	D	300	270	330
Total Pin Count	N	31(2NC)		
Pin Count X axis	N1	6		
Pin Count Y axis	N2	6		
Pins Pitch X axis	J1	600		
Pins Pitch Y axis	J2	600		
Edge to Pin Center Distance along X	S1	555	525	585
Edge to Pin Center Distance along Y	S2	555	525	585

∗ 1. The thickness of Bond-1 glass is 400 um(1pcs).

∗ 2. The material of solder ball is “Sn 96.5% / Ag 3 %/ Cu 0.5%”.

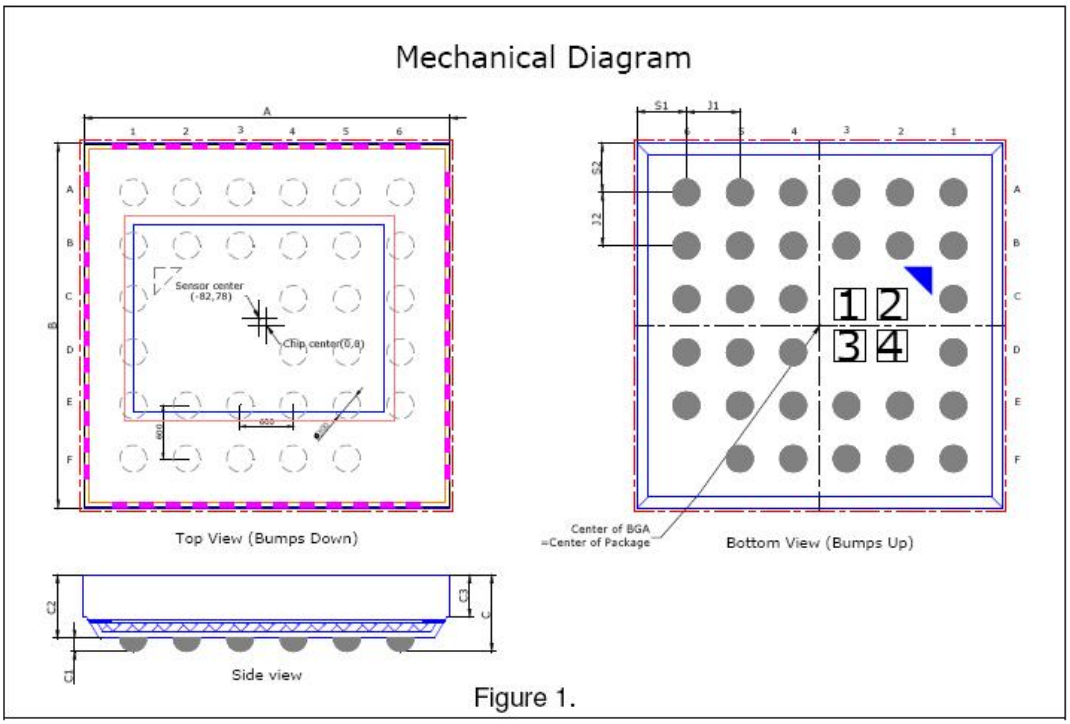
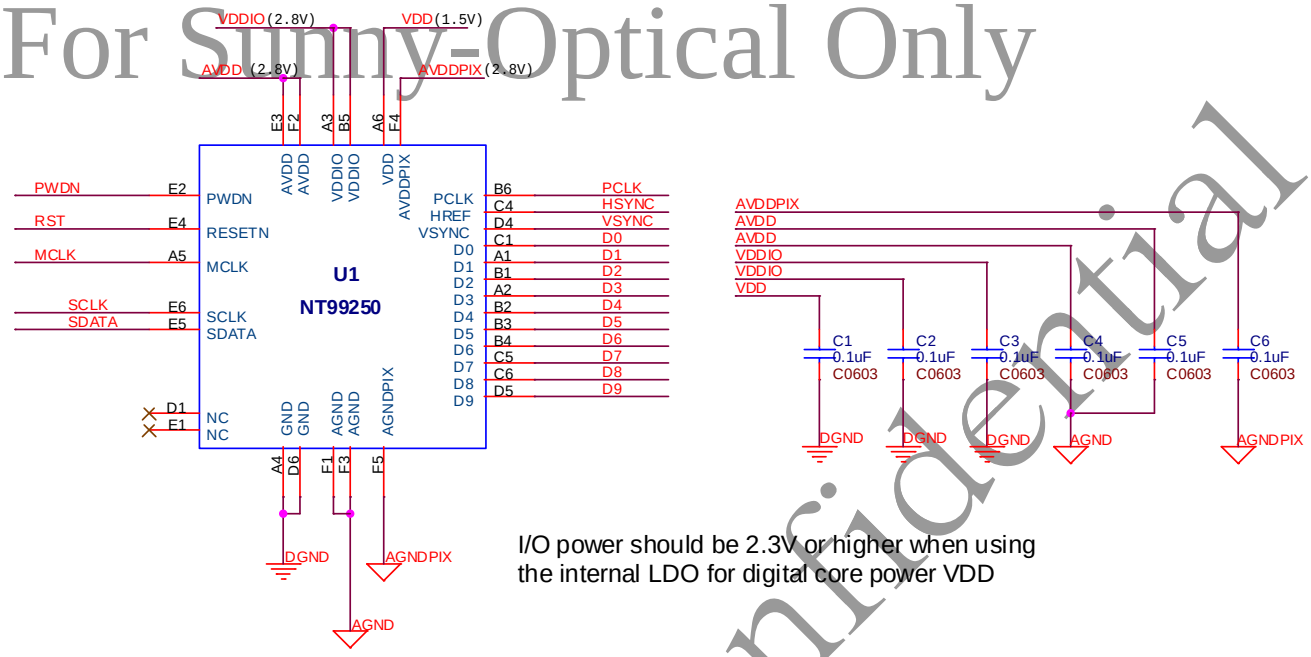


Figure 1.

8. Reference Circuit



I/O power should be 2.3V or higher when using the internal LDO for digital core power VDD

9. Function Description

9.1. Pixel Array

The NT99250 is a 1/5" CMOS image sensor. This sensor contains 1600 (H) x 1200 (V) pixels. CFA (Color Filter Arrays) are in a Bayer pattern. Fig. 1 shows the color filter array layout.

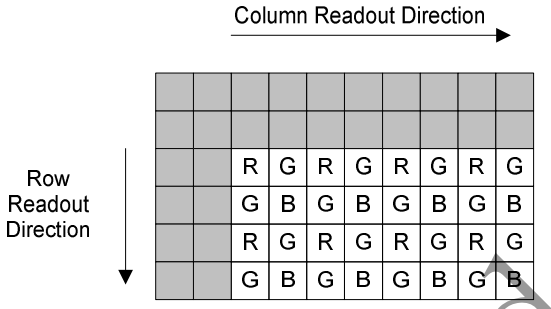


Fig. 1 Color filter array layout

9.2. Default Readout Order

When the sensor is operating in a system, the active surface of the sensor faces the scene as shown in Fig. 2. User can setting the register 0x3022 bit[1:0] to modify the image. By changing the readout direction the image can be mirrored in the horizontal and/or flipped in the vertical direction.

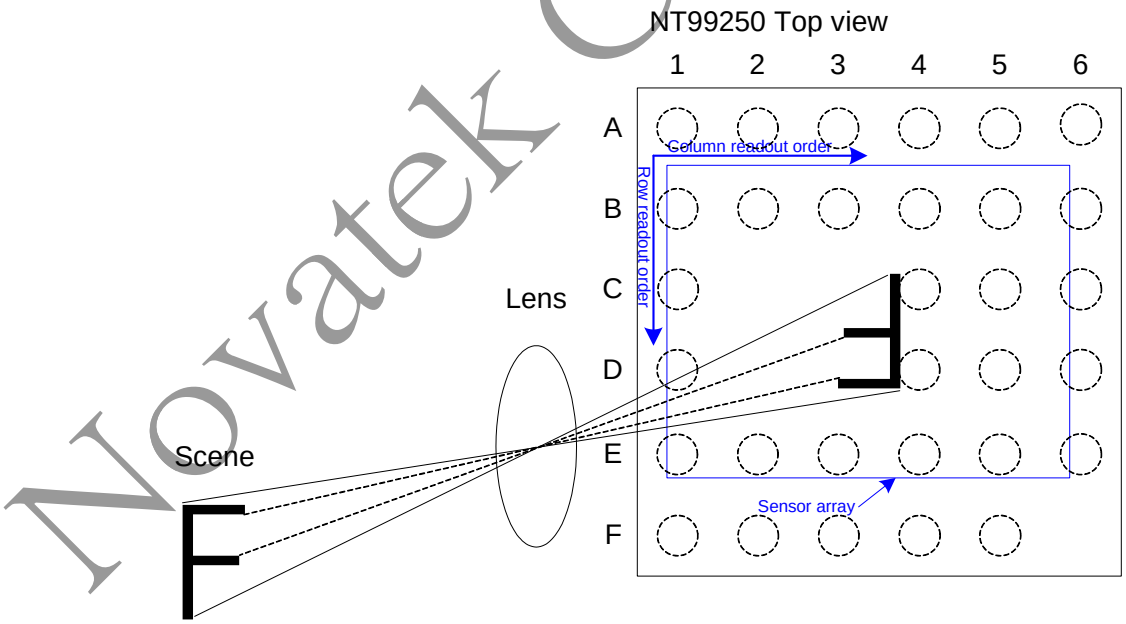


Fig. 2 Ddefault Readout Order

9.3. Analog Gain Control

The amplifier gain can be programmed by the two-wire serial interface.

9.4. 10-Bit ADC

The pixel output signal is digitized by the on-chip 10 bits ADC.

9.5. Image Windowing

User can program the window size by the two-wire serial interface bus. NT99250 output data is synchronized with the PCLK output. When HREF is HIGH, one pixel value is output on the 10-bit data bus (D0 ~ D9) every PCLK period. The pixel clock runs at the calculated frequency based on the sensor's master input clock (MCLK) and internal PLL configuration, and falling edges on the PCLK signal occur one-half of a pixel clock period after transitions on HREF, VSYNC, and DOUT. (see the below: pixel data timing example / row timing and HREF, VSYNC signals)

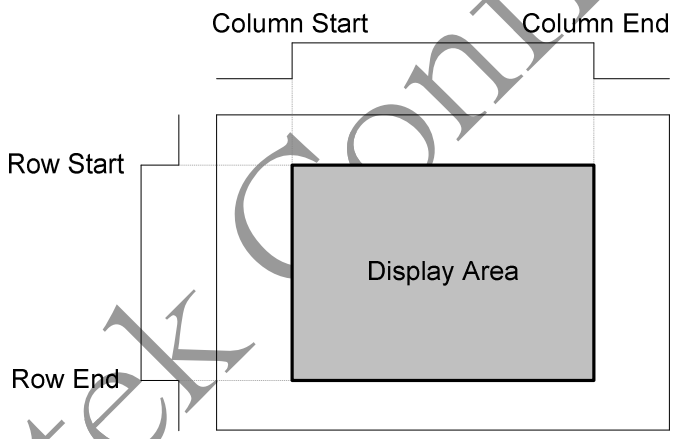
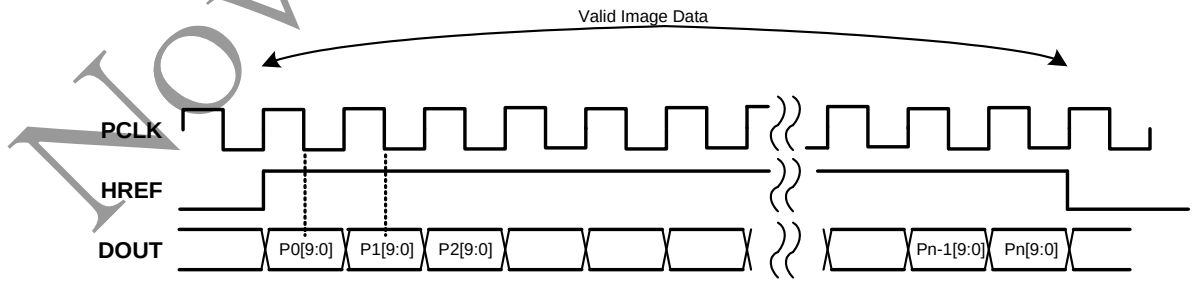
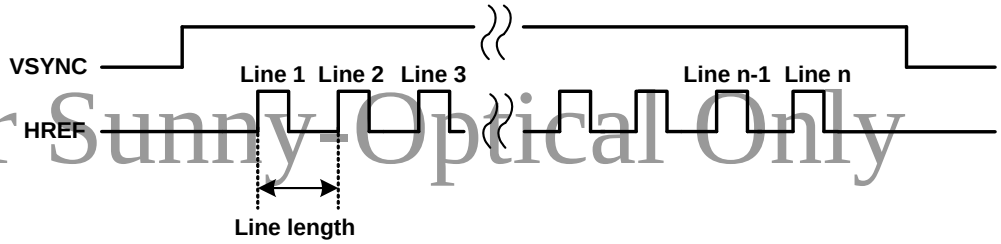


Fig. 3 Image Windowing

Pixel Data Timing Example: (HREF default setting: active high)



Row Timing and HREF / VSYNC signals: (VSYNC default setting: active high)



9.6. Output Format

- YCbCr

Mode	Byte	Byte	Byte	Byte
0x32F0[1] = 0 0x32F0[0] = 0	Cb_i	Y_i	Cr_i	Y_{i+1}
0x32F0[1] = 1 0x32F0[0] = 0	Cr_i	Y_i	Cb_i	Y_{i+1}
0x32F0[1] = 0 0x32F0[0] = 1	Y_i	Cb_i	Y_{i+1}	Cr_i
0x32F0[1] = 1 0x32F0[0] = 1	Y_i	Cr_i	Y_{i+1}	Cb_i

- RGB565

Mode	Byte	D9	D8	D7	D6	D5	D4	D3	D2
0x32F0[1] = 0 0x32F0[0] = 0	1st	R7	R6	R5	R4	R3	G7	G6	G5
	2nd	G4	G3	G2	B7	B6	B5	B4	B3
0x32F0[1] = 1 0x32F0[0] = 0	1st	B7	B6	B5	B4	B3	G7	G6	G5
	2nd	G4	G3	G2	R7	R6	R5	R4	R3
0x32F0[1] = 0 0x32F0[0] = 1	1st	G4	G3	G2	B7	B6	B5	B4	B3
	2nd	R7	R6	R5	R4	R3	G7	G6	G5
0x32F0[1] = 1 0x32F0[0] = 1	1st	G4	G3	G2	R7	R6	R5	R4	R3
	2nd	B7	B6	B5	B4	B3	G7	G6	G5

- RGB555

Mode	Byte	D9	D8	D7	D6	D5	D4	D3	D2
0x32F0[1] = 0 0x32F0[0] = 0	1st	0	R7	R6	R5	R4	R3	G7	G6
	2nd	G5	G4	G3	B7	B6	B5	B4	B3
0x32F0[1] = 1 0x32F0[0] = 0	1st	0	B7	B6	B5	B4	B3	G7	G6
	2nd	G5	G4	G3	R7	R6	R5	R4	R3

- RGB444x

Mode	Byte	D9	D8	D7	D6	D5	D4	D3	D2
0x32F0[1] = 0 0x32F0[0] = 0	1st	R7	R6	R5	R4	G7	G6	G5	G4
	2nd	B7	B6	B5	B4	0	0	0	0
0x32F0[1] = 1 0x32F0[0] = 0	1st	B7	B6	B5	B4	G7	G6	G5	G4
	2nd	R7	R6	R5	R4	0	0	0	0

- RGBx444

Mode	Byte	D9	D8	D7	D6	D5	D4	D3	D2
0x32F0[1] = 0 0x32F0[0] = 0	1st	0	0	0	0	R7	R6	R5	R4
	2nd	G7	G6	G5	G4	B7	B6	B5	B4
0x32F0[1] = 1 0x32F0[0] = 0	1st	G7	G6	G5	G4	B7	B6	B5	B4
	2nd	0	0	0	0	R7	R6	R5	R4

9.7. MSB/LSB Swap

The MSB and LSB can be swapped by setting the control register. Fig. 4 shows some examples of connections with external devices.

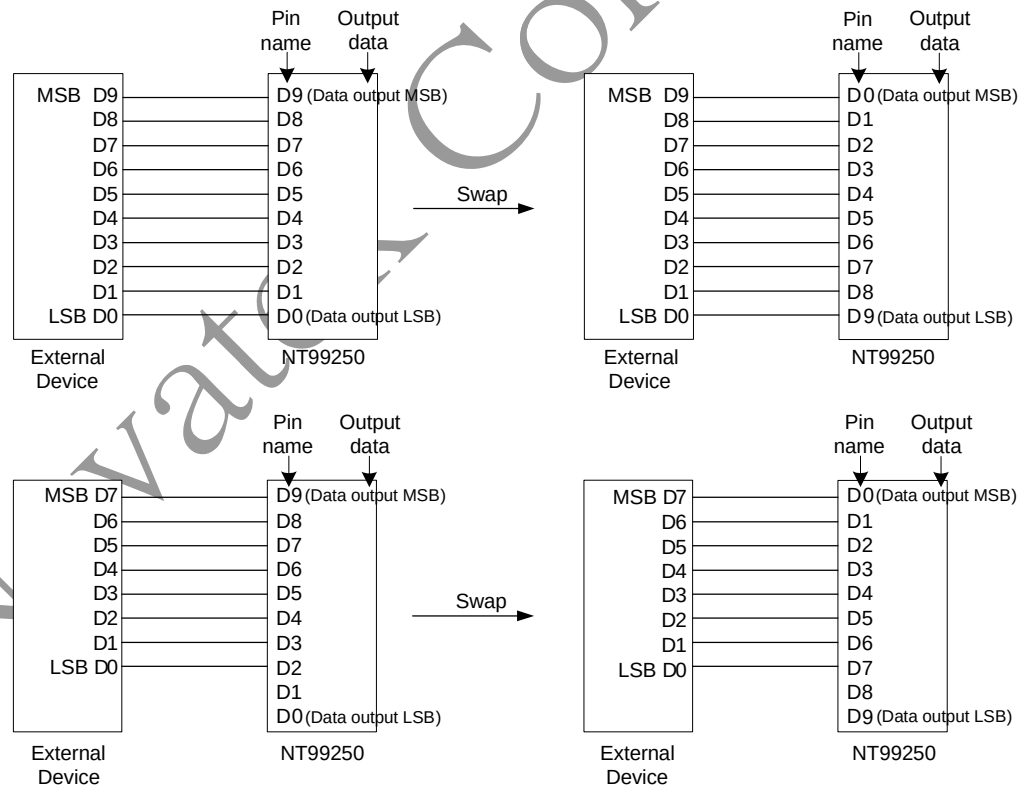


Fig. 4 examples of connections with external devices

9.8. Sepcial Effects

Normal

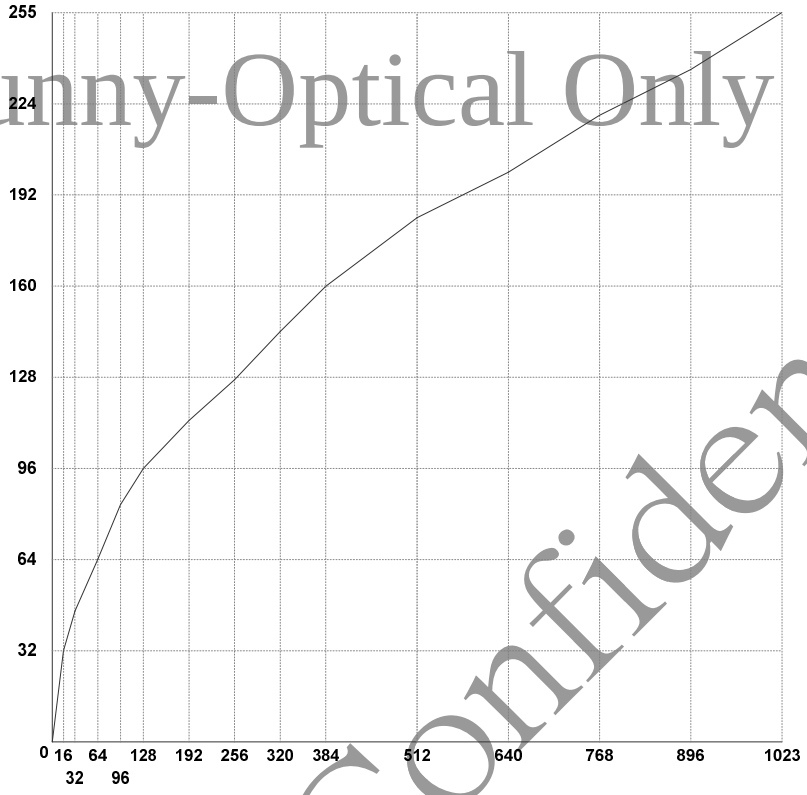
B/W

Sepia

Negative

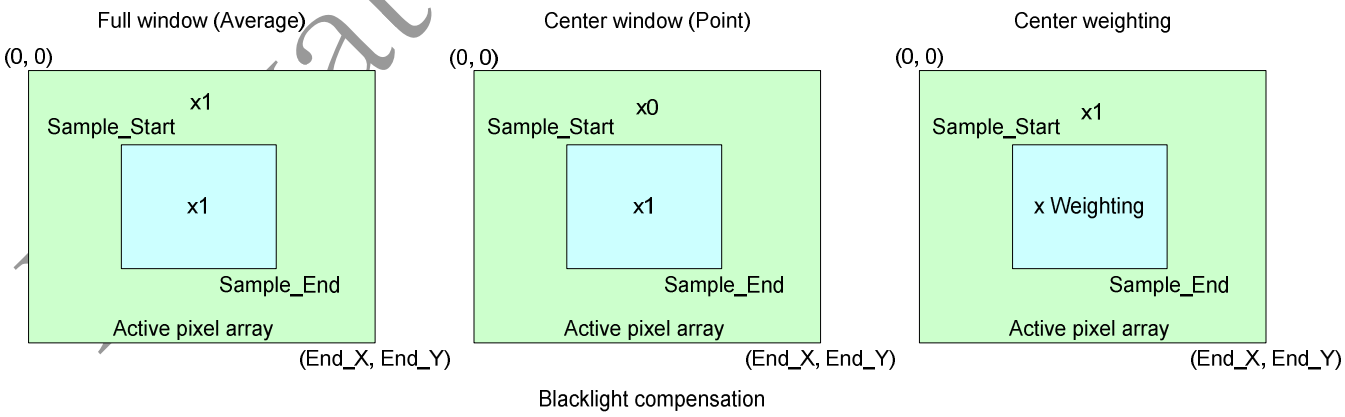
Solarization

9.9. Gamma Correction



9.10. Luminance Acculation Mode

The three modes can be used in AE algorithm. In difference condition, user can change the mode to get better exposure result. Example, in the backlight condition, the point meter can be chose.



10. Two-Wire Serial Interface Bus

User can control the register read/write through two-wire serial interface bus. The interface protocol uses a master/slave model in which a master controls one or more slave devices. The sensor acts as a slave device. The master device generates a clock MCLK that is an input to the sensor and used to synchronize data transfers. Data is transferred between master and slave on a bi-directional signal SDATA. SDATA must be pull up to VDDIO by a 1.5 k Ω resistor.

Data transfer on the two-wire serial interface bus are performed by a sequence of low level protocol elements:

- a (repeated) start condition
- a slave address / data direction byte
- an (a no) acknowledge bit
- a message byte
- a stop condition

The bus is idle when both SCLK and SDATA are “high”. Control of the bus is initiated with a start condition, and the bus is released with a stop condition. Only the master can generate the start and stop conditions.

- Start condition

  A start condition is defined as a high-to-low transition on SDATA while SCLK is “high”. At the end of a transfer, the master can generate a start condition without previously generating a stop condition; this is known as a “repeated start” or “restart” condition.

- Stop condition

  A stop condition is defined as a low-to-high transition on SDATA while SCLK is high.

- Data transfer

  Data is transferred serially, 8 bits at a time, with the MSB transmitted first. Each byte of data is followed by an acknowledge bit or a no-acknowledge bit. This data transfer mechanism is used for the slave address/data direction byte and for message bytes. One data bit is transferred during each SCLK clock period. SDATA can change when SCLK is “low” and must be stable while SCLK is “high”.

- Slave address / Data direction byte

  Bits [7:1] of this byte represent the device slave address and bit [0] indicates the data transfer direction. A “0” in bit [0] indicates a write, and a “1” indicates a read. The slave addresses used by the NT99250 are 0x6C (write address) and 0x6D (read address).

- Message byte

  Message bytes are used for sending register addresses and register write data to the slave device and for retrieving register read data. The protocol used is outside the scope of the I2C specification and is defined as part of the MIPI and CSI.

- Acknowledge bit

  Each 8-bit data transfer is followed by an acknowledge bit or a no-acknowledge bit in the SCLK clock period following the data transfer. The transmitter (which is the master when writing, or the slave when reading) releases SDATA. The receiver indicates an acknowledge bit by driving SDATA “low”. As for data transfers, SDATA can change when SCLK is “low” and must be stable while SCLK is “high”.

- No-acknowledge bit

  The no-acknowledge bit is generated when the receiver does not drive SDATA “low” during the SCLK clock period following a data transfer. A no-acknowledge bit is used to terminate a read sequence.

- Typical sequence

  A typical read or write sequence begins by the master generating a start condition on the bus. After the start condition, the master sends the 8-bit slave address/data direction byte. The last bit indicates whether the request is for a read or a write, where a “0” indicates a write and a “1” indicates a read. If the address matches the address of the slave device, the slave device acknowledges receipt of the address by generating an acknowledge bit on the bus.

  If the request was a write, the master then transfers the 16-bit register address to which the write should take place. This transfer takes place as two 8-bit sequences and the slave sends an acknowledge bit after each sequence to indicate that the byte has been received. The master then transfers the data as an 8-bit sequence; the slave sends an acknowledge bit at the end of the sequence. The master stops writing by generating a (re)start or stop condition.

If the request was a read, the master sends the 8-bit write slave address/data direction byte and 16-bit register address, the same way as with a write request. The master then generates a (re)start condition and the 8-bit read slave address/data direction byte, and clocks out the register data, eight bits at a time. The master generates an acknowledge bit after each 8-bit transfer. The slave's internal register address is auto-incremented after every 8 bits are transferred. The data transfer is stopped when the master sends a no-acknowledge bit.

10.1. Single Read from Random Location

This sequence (Fig. 5) starts with a dummy WRITE to the 16-bit address that is to be used for the READ. The master terminates the WRITE by generating a restart condition. The master then sends the 8-bit READ slave address/data direction byte and clocks out one byte of register data. The master terminates the READ by generating a noacknowledge bit followed by a stop condition. Fig. 5 shows how the internal register address maintained by the NT99250 is loaded and incremented as the sequence proceeds.

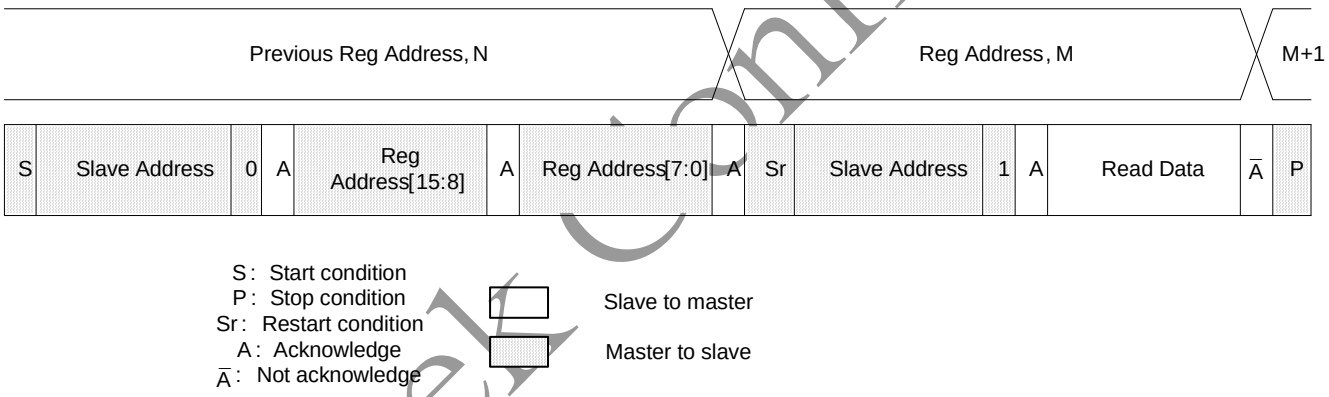


Fig. 5 Single read from random location

10.2. Single Read from Current Location

This sequence (see Fig. 6) performs a READ using the current value of the NT99250 internal register address. The master terminates the READ by generating a no-acknowledge bit followed by a stop condition. The figure shows two independent READ sequences.

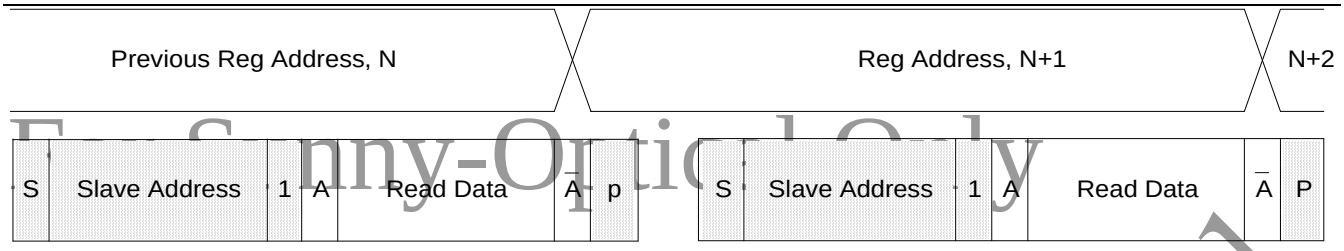


Fig. 6 Single read from current location

10.3. Sequential Read, Start from Random Location

This sequence (Fig. 7) starts in the same way as the single READ from random location (Fig. 5). Instead of generating a no-acknowledge bit after the first byte of data has been transferred, the master generates an acknowledge bit and continues to perform byte READs until "L" bytes have been read.

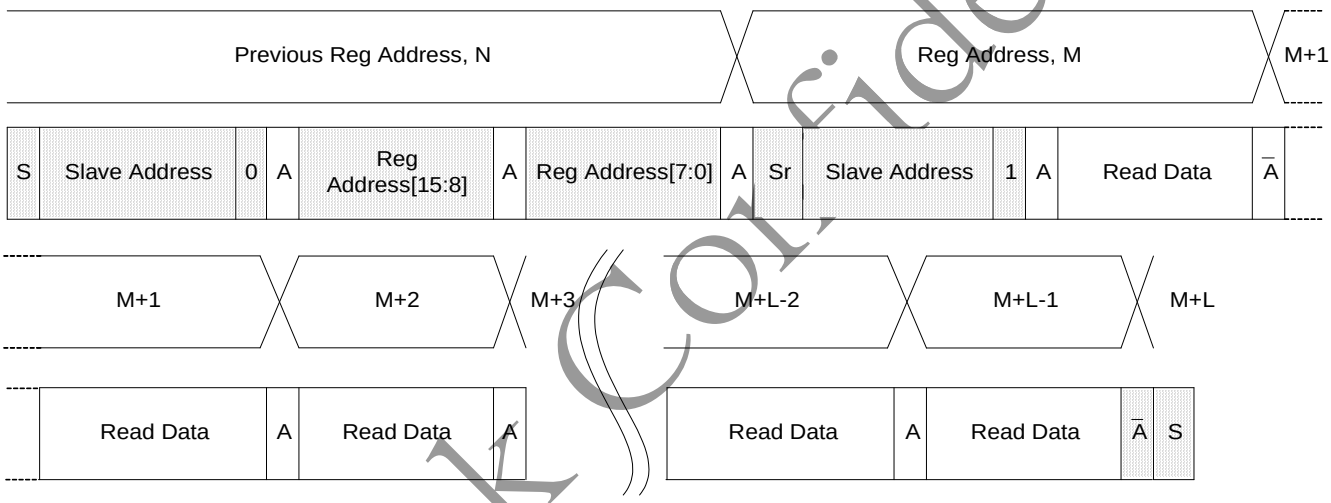


Fig. 7 Sequential read, start from random location

10.4. Sequential Read, Start from Current Location

This sequence (Fig. 8) starts in the same way as the single READ from current location (Fig. 6). Instead of generating a no-acknowledge bit after the first byte of data has been transferred, the master generates an acknowledge bit and continues to perform byte READs until "L" bytes have been read.

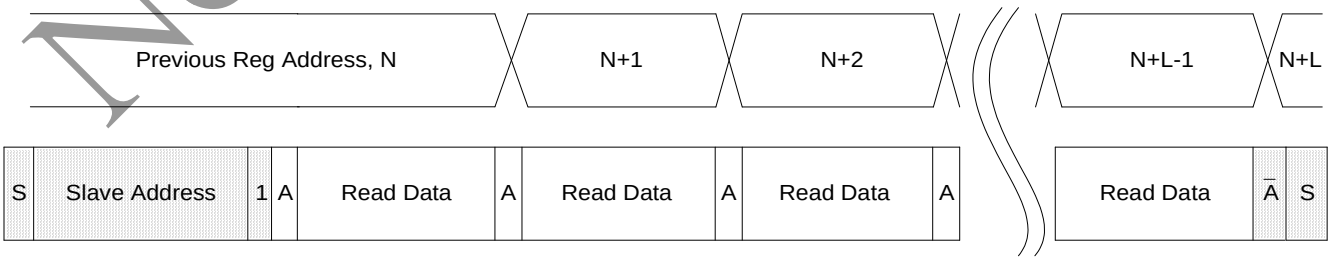


Fig. 8 Sequential read, start from current location

10.5. Single Write to Random Location

This sequence (Fig. 9) begins with the master generating a start condition. The slave address/data direction byte signals a WRITE and is followed by the HIGH then LOW bytes of the register address that is to be written. The master follows this with the byte of write data. The WRITE is terminated by the master generating a stop condition.

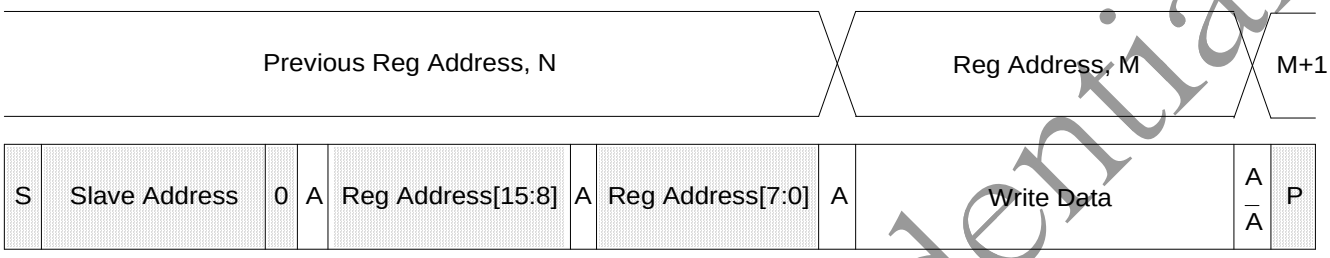


Fig. 9 Single write to random location

10.6. Sequential Write, Start at Random Location

This sequence (Fig. 10) starts in the same way as the single WRITE to random location (Fig. 9). Instead of generating a stop condition after the first byte of data has been transferred, the master continues to perform byte WRITEs until “L” bytes have been written. The WRITE is terminated by the master generating a stop condition.

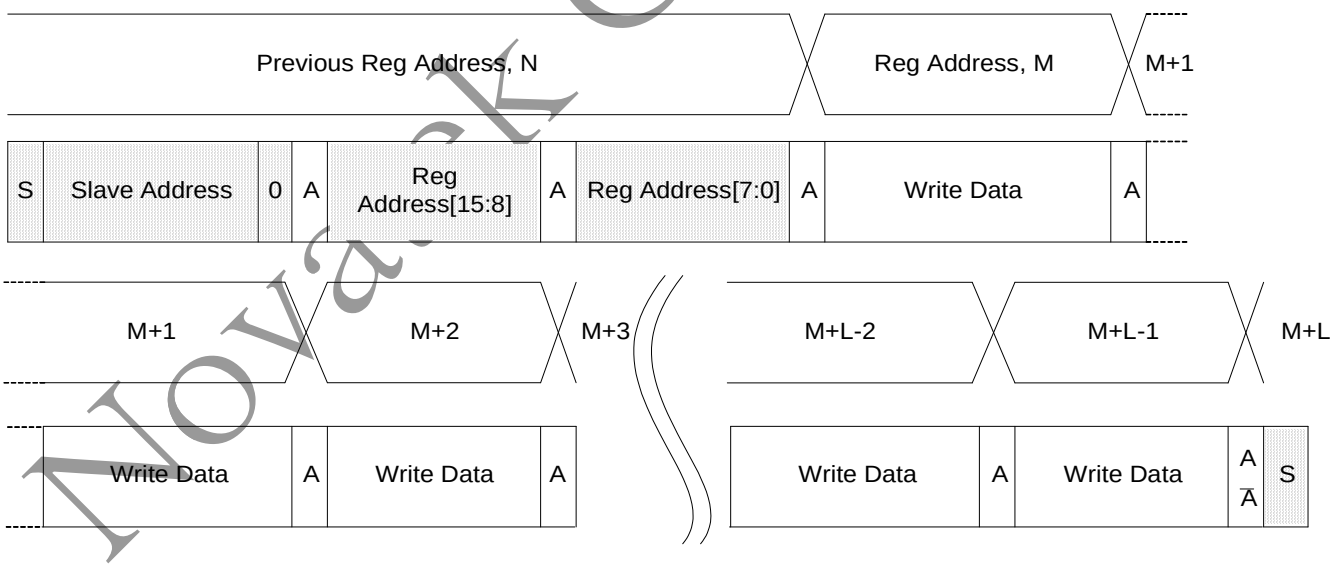


Fig. 10 Sequential write, start at random location

11. Control Registers

The device slave addresses are 0x6C for write and 0x6D for read. The detail control registers are listed as follow.

11.1. Sensor Control Registers (0x3000)

Address	Register Name	Bits	R/W	Reset Value	Descriptions
					Chip_Version [15:0]
0x3000	Chip_Version_H	7:0	R	0x25	bit [15:4] is chip number bit [3:0] is version
0x3001	Chip_Version_L	7:0	R	0x00	
					X_Addr_Start [10:0] †
0x3002	X_Addr_Start_H	2:0	R/W	0x00	The first column of visible pixels to be read out. Even only.
0x3003	X_Addr_Start_L	7:0	R/W	0x00	
					Y_Addr_Start [10:0] †
0x3004	Y_Addr_Start_H	2:0	R/W	0x00	The first row of visible pixels to be read out. Even only.
0x3005	Y_Addr_Start_L	7:0	R/W	0x00	
					X_Addr_End [10:0] †
0x3006	X_Addr_End_H	2:0	R/W	0x06	The last row of visible pixels to be read out. Odd only.
0x3007	X_Addr_End_L	7:0	R/W	0x3F	
					Y_Addr_End [10:0] †
0x3008	Y_Addr_End_H	2:0	R/W	0x04	The last row of visible pixels to be read out. Odd only.
0x3009	Y_Addr_End_L	7:0	R/W	0xAF	
					Line_Length_Pck [15:0] †
0x300A	Line_Length_Pck_H	7:0	R/W	0x08	The number of pixel clock periods in one line (row) time. This includes visible pixels and horizontal blanking time.
0x300B	Line_Length_Pck_L	7:0	R/W	0x24	
					Frame_Length_Line [15:0] †
0x300C	Frame_Length_Line_H	7:0	R/W	0x04	The number of complete lines (rows) in the output frame. This includes visible lines and vertical blanking lines.
0x300D	Frame_Length_Line_L	7:0	R/W	0xC0	
					X_Output_Size [10:0] †
0x300E	X_Output_Size_H	2:0	R/W	0x06	Set output size of x direction for display image. The maximum size is (X_Addr_End - X_Addr_Start + 1). If the Scaling down is disable, this size is final size.
0x300F	X_Output_Size_L	7:0	R/W	0x40	
					Y_Output_Size [10:0] †
0x3010	Y_Output_Size_H	2:0	R/W	0x04	Set output size of y direction for display image. The maximum size is (Y_Addr_End - Y_Addr_Start + 1) If the Scaling down is disable, this size is final size.
0x3011	Y_Output_Size_L	7:0	R/W	0xB0	
					Integration_Time [15:0] †
0x3012	Integration_Time_H	7:0	R/W	0x00	T_{ex} = (Exposure [15:0] + 1) * Row_time
0x3013	Integration_Time_L	7:0	R/W	0x01	

0x3014	DGain_R	1:0	R/W	0x00	Digital gain (bit [1] + 1) * (bit [0] + 1) * Analog gain.
0x3015	AGain_R	6:0	R/W	0x00	AGain = Gain1 * Gain2 Gain1 = (1 + bit [6]) *(1 + bit [5]) * (1 + bit [4]) Gain2 = (1 + (bit [3:0] + 1) / 16)
0x3016	DGain_Gr	1:0	R/W	0x00	Digital gain (bit [1] + 1) * (bit [0] + 1) * Analog gain.
0x3017	AGain_Gr	6:0	R/W	0x00	AGain = Gain1 * Gain2 Gain1 = (1 + bit [6]) *(1 + bit [5]) * (1 + bit [4]) Gain2 = (1 + (bit [3:0] + 1) / 16)
0x3018	DGain_Gb	1:0	R/W	0x00	Digital gain (bit [1] + 1) * (bit [0] + 1) * Analog gain.
0x3019	AGain_Gb	6:0	R/W	0x00	AGain = Gain1 * Gain2 Gain1 = (1 + bit [6]) *(1 + bit [5]) * (1 + bit [4]) Gain2 = (1 + (bit [3:0] + 1) / 16)
0x301A	DGain_B	1:0	R/W	0x00	Digital gain (bit [1] + 1) * (bit [0] + 1) * Analog gain.
0x301B	AGain_B	6:0	R/W	0x00	AGain = Gain1 * Gain2 Gain1 = (1 + bit [6]) *(1 + bit [5]) * (1 + bit [4]) Gain2 = (1 + (bit [3:0] + 1) / 16)
0x301C	Global_DGain	1:0	R/W	0x00	Digital gain (bit [1] + 1) * (bit [0] + 1) * Analog gain.
0x301D	Global_AGain	6:0	R/W	0x00	Writing a gain to this register is equivalent to writing code to each gain.
0x301E	PLL_Ctrl	6:0	R/W	0x54	
	PLL_Pwdn	6	R/W	1	When seting Output_Mode_Sel = 1 (stream out), then PLL_Pwdn = 0 0: Disable 1: Enable
	PLL_Bypass	5	R/W	0	0: Normal (Internal clock using PLL_PCLK) 1: Bypass (External clock using Ext_PCLK)
	PLL_M	4	R/W	1	0: PLL_M = 4 1: PLL_M = 8
	PLL_PCLK	3:2	R/W	1	Max. PCLK must be 52 MHz. If output format is Raw 10bits format by this setting, the PCLK is 26 MHz. The min. CLK_SRC must be over 13 MHz. 0: PCLK = (CLK_SRC * PLL_M) / 2 (at 13 MHz) 1: PCLK = (CLK_SRC * PLL_M) / 4 (at 26 MHz) 2: PCLK = (CLK_SRC * PLL_M) / 8 3: PCLK = (CLK_SRC * PLL_M) / 16
	Ext_PCLK	1:0	R/W	0	External clock setting 0: PCLK = (CLK_SRC) 1: PCLK = (CLK_SRC) / 2 2: PCLK = (CLK_SRC) / 4 3: PCLK = (CLK_SRC) / 8
0x301F	-	-	-	-	Reserved
0x3020	-	-	-	-	Reserved
0x3021	Reset_Register	7:0	R/W	0x60	
	Output_Bit_Swap	7	R/W	0	Output bit swap, swap MSB and LSB. 0: Disable 1: Enable.

	Clock_Output_TriState	6	R/W	1	Clock output Tri-state 0: Output clock pin will keep the last status before sensor standby mode. 1: Output clock pin will be tri-stated during standby mode.
	Data_Output_TriState	5	R/W	1	Data output Tri-state 0: Output data pins (VSYNC, HREF) will keep last status before sensor standby mode. 1: Output data pins will be tri-stated during standby mode.
	-	4	R	0	Reserved
	Show_Bad_Frame	2	R/W	0	Show bad frame 1: Output all frame (including bad frames) 0: Only output good frames (default)
	Output_Mode_Sel	1	R/W	0	Output mode select (Start) 1: Streaming. 0: Standby
	Reset	0	R/W	0	Reset Hardware clear. Setting this bit to initiates a reset sequence.
0x3022	Read_Mode_0	7:0	R/W	0x24	
	Y_Even_Inc	7:5	R/W	1	Increment applied to even addresses in Y (row) direction † 1: Normal readout
	X_Even_Inc	4:2	R/W	1	Increment applied to even addresses in X (column) direction † 1: Normal readout
	Mirror_Horizontal	1	R/W	0	Horizontal mirror 0: Normal readout 1: Mirror readout
	Flip_Vertical	0	R/W	0	Vertical flip 0: Normal readout 1: Flip readout
0x3023	Read_Mode_1	7:0	R/W	0x24	
	Y_Odd_Inc	7:5	R/W	1	Increment applied to odd addresses in Y (row) direction † 1: Normal readout 3: 1/2x 5: 1/3x 7: 1/4x
	X_Odd_Inc	4:2	R/W	1	Increment applied to odd addresses in X (column) direction † 1: Normal readout 3: 1/2x 5: 1/3x 7: 1/4x
	XY_Bin_En	1	R/W	0	Enable analog binning in X and Y directions. When set, X_Even_Inc and X_Odd_Inc must be set to 1 and 3. Y_Odd_Inc + Y_Even_Inc = 4.
	X_Bin_En	0	R/W	0	Enable analog binning in X directions.

					When set, X_Odd_Inc must be set to 3. X_Even_Inc = Y_Even_Inc = Y_Odd_Inc = 1.
0x3024	Read_Mode_2	7:0	R/W	0x00	
	-	7	R	0	Reserved
	Show_Dark_Pix	6	R/W	0	Show dark pixel 0: Don't show dark pixel. 1: Show dark pixel.
	-	5:4	R	0	Reserved
	Pclk_Edge_Sel	3	R/W	0	PCLK edge selection 0: Data valid on PCLK falling edge 1: Data valid on PCLK rising edge.
	Pclk_Output_Sel	2	R/W	0	PCLK output selection 0: PCLK always output 1: PCLK output qualified by HREF.
	VSync_Inverse	1	R/W	0	VSYNC inverse 0: Active high 1: Active low
	HREF_Inverse	0	R/W	0	HREF inverse 0: Active high 1: Active low
0x3025	Pattern_Mode	7:0	R/W	0x00	
	-	7:4	R	0	Reserved
	Pattern_Mode_Sel	3:0	R/W	0	Pattern select 0: Normal operation: no test pattern 1: Reserve 2: 100% Color bars 3: PN9 4: Reserve Pattern size depend on X_Output_Size and Y_Output_Size.
					PN9_Value [9:0]
0x3026	PN9_Value_H	1:0	R/W	0x00	When PN9 is enabled, this byte is random value.
0x3027	PN9_Value_L	7:0	R/W	0x00	
0x3028	-	-	-	-	Reserved
0x3029	-	-	-	-	Reserved
0x302A	-	-	-	-	Reserved
0x302B	-	-	-	-	Reserved
0x302C	-	-	-	-	Reserved
0x302D	-	-	-	-	Reserved
0x302E	-	-	-	-	Reserved
0x302F	-	-	-	-	Reserved
0x3030	-	-	-	-	Reserved
0x3031	-	-	-	-	Reserved
0x3032	-	-	-	-	Reserved

0x3033	-	-	-	-	Reserved
0x3034	-	-	-	-	Reserved
0x3035	-	-	-	-	Reserved
0x3036	-	-	-	-	Reserved
0x3037	-	-	-	-	Reserved
0x3038	-	-	-	-	Reserved
0x3039	-	-	-	-	Reserved
0x303A	-	-	-	-	Reserved
0x303B	-	-	-	-	Reserved
0x303C	-	-	-	-	Reserved
0x303D	-	-	-	-	Reserved
0x303E	-	-	-	-	Reserved
0x303F	Calibration_Control_1	7:0	R/W	0x00	
	ABLC_Base_Init_En	7	R/W	0	0: Disable 1: Enable
	ABLC_Recalcu_En	6	R/W	0	0: Disable 1: Enable
	ABLC_Avg_Gain_En	5	R/W	0	0: Disable 1: Enable
	ABLC_SameGreen	4	R/W	0	An equivalent green average value will be referenced. This register is effective when ABLC_Manual_En is 0
	Sen_DPC_En	3	R/W	0	Defect pixel correction enable 0: Disable 1: Enable
	BLC_Sampled_Pixel	2	R/W	0	The number of pixel to be sampled for ABLC and DBLC. The default value is 0
	DBLC_En	1	R/W	0	0: Disable 1: Enable
	ABLC_Manual_En	0	R/W	0	0: Auto calibration 1: Manual calibration
0x3040	ABLC_Thr_Top	7:0	R/W	0x50	Top threshold for black level
0x3041	ABLC_Thr_Bottom	7:0	R/W	0x14	Bottom threshold for black level
0x3042	-	-	-	-	Reserved
0x3043	-	-	-	-	Reserved
					ABLC_Ofs_R [9:0]
0x3044	ABLC_Ofs_R_H	1:0	R/W	0x02	DAC offset cancellation
0x3045	ABLC_Ofs_R_L	7:0	R/W	0x00	
					ABLC_Ofs_Gr [9:0]
0x3046	ABLC_Ofs_Gr_H	1:0	R/W	0x02	DAC offset cancellation
0x3047	ABLC_Ofs_Gr_L	7:0	R/W	0x00	
					ABLC_Ofs_Gb [9:0]

0x3048	ABLC_Ofs_Gb_H	1:0	R/W	0x02	DAC offset cancellation
0x3049	ABLC_Ofs_Gb_L	7:0	R/W	0x00	
					ABLC_Ofs_B [9:0]
0x304A	ABLC_Ofs_B_H	1:0	R/W	0x02	DAC offset cancellation
0x304B	ABLC_Ofs_B_L	7:0	R/W	0x00	
0x304C	ABLC_Avg_R	7:0	R	-	Black level average of R pixels
0x304D	ABLC_Avg_Gr	7:0	R	-	Black level average of Gr pixels
0x304E	ABLC_Avg_Gb	7:0	R	-	Black level average of Gb pixels
0x304F	ABLC_Avg_B	7:0	R	-	Black level average of B pixels
0x3050	OB_Thr	7:0	R/W	0xFF	Optical Black Threshold If (pixel value < OB_Thr), take this pixel into account.
0x3051	Optical_Black_Weight_0	7:0	R/W	0xF0	
	ABLC_GainW	7:4	R/W	0xF	Avg = Avg * (ABLC_GainW + 1) / 16
	-	3:0	R	0	Reserved
0x3052	Optical_Black_Weight_1	7:0	R/W	0x80	
	OB_MUL	7:2	R/W	0x20	The multiplier of optical black Pixel = pixel - OB_Avg * OB_MUL - OB_OFS
	-	1	R	0	Reserved
	OB_Ofs_H	0	R/W	0	OB_Ofs [8] MSB part of OB offset.
0x3053	OB_Ofs_L	7:0	R/W	0	OB_Ofs [7:0] LSB part of OB offset. Pixel = pixel - ob_ofs
0x3054	-	-	-	-	Reserved
0x3055	-	-	-	-	Reserved
0x3056	-	-	-	-	Reserved
0x3057	-	-	-	-	Reserved
0x3058	DPC_Gain_Thr	7:0	R/W	0xFF	
0x3059	DPC_Smooth_Thr1	7:0	R/W	0x05	
0x305A	DPC_Thr1	7:0	R/W	0x0A	
0x305B	DPC_Thr_Dark1	7:0	R/W	0x00	
0x305C	DPC_Smooth_Thr2	7:0	R/W	0x08	
0x305D	DPC_Thr2	7:0	R/W	0x0A	
0x305E	DPC_Thr_Dark2	7:0	R/W	0x00	
0x305F	-	-	-	-	Reserved
0x3060	Reg_Activate_Ctrl	0	R/W	0x00	Activate setting for specified registers. auto clear.
0x3068	Pad_Config_Serial_IO	7:0	R/W	0x2	
	-	7:1	R	0	Reserved
	Sio_Odrv	0	R/W	0	Output driving 0: 4 mA 1: 8 mA

0x3069	Pad_Config_Pix_Out	7:0	R/W	0x0	
	-	7:1	R	0	Reserved
	PixOut_Odrv	0	R/W	0	Output driving 0: 4 mA 1: 8 mA
0x306A	-	-	-	-	Reserved
0x306B	Pad_Config_Rstn	7:0	R/W	0x0	
	-	7:1	R	0	Reserved
	Rstn_Odrv	0	R/W	0	Output driving 0: 4 mA 1: 8 mA
0x306C	Pad_Config_Sync	7:0	R/W	0x0	
	-	7:1	R	0	Reserved
	Sync_Odrv	0	R/W	0	Output driving 0: 4 mA 1: 8 mA
0x306D	Pad_Config_Pclk	7:0	R/W	0x0	
	-	7:1	R	0	Reserved
	Pclk_Odrv	0	R/W	0	Output driving 0: 4 mA 1: 8 mA
0x306E	Pad_Config_Mclk	7:0	R/W	0x0	
	-	7:1	R	0	Reserved
	Mclk_Odrv	0	R/W	0	Output driving 0: 4 mA 1: 8 mA

† New register values are accepted by enabling LOAD bit in register 0x3060.

11.2. SOC Control Registers (0x3200)

Address	Register Name	Bits	R/W	Reset Value	Descriptions
0x3200	Mode_Control_0	5:0	R/W	0x10	
	LSC_En	5	R/W	0	Lens shading correction enable 0: Disable 1: Enable
	Gamma_En	4	R/W	1	Gamma correction enable 0: Disable 1: Enable
	Color_Gain_En	3	R/W	0	Color gain enable 0: Disable 1: Enable
	Color_Accmu_En	2	R/W	0	Color accumulation enable 0: Disable 1: Enable
	Lum_Accmu_En	1	R/W	0	Luminance accumulation enable 0: Disable 1: Enable
	-	0	R	0	Reserved
0x3201	Mode_Control_1	7:0	R/W	0x0F	
	-	7	R	0	Reserved
	Scaling_Down_En	6	R/W	0	Scaling down enable 0: Disable 1: Enable
	AE_En	5	R/W	0	Auto-exposure enable 0: Disable 1: Enable
	AWB_En	4	R/W	0	Auto-white balance enable 0: Disable 1: Enable
	Noise_Reduction_En	3	R/W	1	Noise reduction enable 0: Disable 1: Enable
	Edge_Enhance_En	2	R/W	1	Edge enhancement enable 0: Disable 1: Enable
	Color_Correct_En	1	R/W	1	Color correction and transform enable 0: Disable 1: Enable
	Special_Effect_En	0	R/W	1	Special effects enable 0: Disable 1: Enable

11.3. SOC Lens Shading Correction Registers (0x3210)

Address	Register Name	Bits	R/W	Reset Value	Descriptions
					LSC_Coef_R1 [15:0]
0x3210	LSC_Coef_R1_H	7:0	R/W	0x00	Coefficient
0x3211	LSC_Coef_R1_L	7:0	R/W	0x00	
					LSC_Coef_R2 [15:0]
0x3212	LSC_Coef_R2_H	7:0	R/W	0x00	Coefficient
0x3213	LSC_Coef_R2_L	7:0	R/W	0x00	
					LSC_Coef_R3 [15:0]
0x3214	LSC_Coef_R3_H	7:0	R/W	0x00	Coefficient
0x3215	LSC_Coef_R3_L	7:0	R/W	0x00	
					LSC_Coef_R4 [15:0]
0x3216	LSC_Coef_R4_H	7:0	R/W	0x00	Coefficient
0x3217	LSC_Coef_R4_L	7:0	R/W	0x00	
					LSC_Coef_Gr1 [15:0]
0x3218	LSC_Coef_Gr1_H	7:0	R/W	0x00	Coefficient
0x3219	LSC_Coef_Gr1_L	7:0	R/W	0x00	
					LSC_Coef_Gr2 [15:0]
0x321A	LSC_Coef_Gr2_H	7:0	R/W	0x00	Coefficient
0x321B	LSC_Coef_Gr2_L	7:0	R/W	0x00	
					LSC_Coef_Gr3 [15:0]
0x321C	LSC_Coef_Gr3_H	7:0	R/W	0x00	Coefficient
0x321D	LSC_Coef_Gr3_L	7:0	R/W	0x00	
					LSC_Coef_Gr4 [15:0]
0x321E	LSC_Coef_Gr4_H	7:0	R/W	0x00	Coefficient
0x321F	LSC_Coef_Gr4_L	7:0	R/W	0x00	
					LSC_Coef_Gb1 [15:0]
0x3220	LSC_Coef_Gb1_H	7:0	R/W	0x00	Coefficient
0x3221	LSC_Coef_Gb1_L	7:0	R/W	0x00	
					LSC_Coef_Gb2 [15:0]
0x3222	LSC_Coef_Gb2_H	7:0	R/W	0x00	Coefficient
0x3223	LSC_Coef_Gb2_L	7:0	R/W	0x00	
					LSC_Coef_Gb3 [15:0]
0x3224	LSC_Coef_Gb3_H	7:0	R/W	0x00	Coefficient
0x3225	LSC_Coef_Gb3_L	7:0	R/W	0x00	
					LSC_Coef_Gb4 [15:0]
0x3226	LSC_Coef_Gb4_H	7:0	R/W	0x00	Coefficient

0x3227	LSC_Coef_Gb4_L	7:0	R/W	0x00	
					LSC_Coef_B1 [15:0]
0x3228	LSC_Coef_B1_H	7:0	R/W	0x00	Coefficient
0x3229	LSC_Coef_B1_L	7:0	R/W	0x00	
					LSC_Coef_B2 [15:0]
0x322A	LSC_Coef_B2_H	7:0	R/W	0x00	Coefficient
0x322B	LSC_Coef_B2_L	7:0	R/W	0x00	
					LSC_Coef_B3 [15:0]
0x322C	LSC_Coef_B3_H	7:0	R/W	0x00	Coefficient
0x322D	LSC_Coef_B3_L	7:0	R/W	0x00	
					LSC_Coef_B4 [15:0]
0x322E	LSC_Coef_B4_H	7:0	R/W	0x00	Coefficient
0x322F	LSC_Coef_B4_L	7:0	R/W	0x00	
0x3230	-	-	-	-	Reserved
0x3231	-	-	-	-	Reserved
0x3232	-	-	-	-	Reserved
0x3233	-	-	-	-	Reserved
0x3234	-	-	-	-	Reserved
0x3235	-	-	-	-	Reserved
0x3236	-	-	-	-	Reserved
0x3237	-	-	-	-	Reserved
0x3238	Multiple_Width_Height	6:0	R/W	0x77	
	LSC_Mul_Height	6:4	R/W	7	Multiple height of sample height Height = (Mul_Height + 1) / 8
	LSC_Mul_Width	2:0	R/W	7	Multiple width of sample width Width = (Mul_Width + 1) / 8
					LSC_Max_R [9:0]
0x3239	LSC_Max_R_H	1:0	R/W	0x00	Coefficient
0x323A	LSC_Max_R_L	7:0	R/W	0x00	
0x323B	-	-	-	-	Reserved
					LSC_Max_Gr [9:0]
0x323C	LSC_Max_Gr_H	1:0	R/W	0x00	Coefficient
0x323D	LSC_Max_Gr_L	7:0	R/W	0x00	
0x323E	-	-	-	-	Reserved
					LSC_Max_Gb [9:0]
0x323F	LSC_Max_Gb_H	1:0	R/W	0x00	Coefficient
0x3240	LSC_Max_Gb_L	7:0	R/W	0x00	
0x3241	-	-	-	-	Reserved
					LSC_Max_B [9:0]

0x3242	LSC_Max_B_H	1:0	R/W	0x00	Coefficient
0x3243	LSC_Max_B_L	7:0	R/W	0x00	

11.4. SOC Gamma Registers (0x3270)

Address	Register Name	Bits	R/W	Reset Value	Descriptions
0x3270	Gamma_Tab_0	7:0	R/W	0x00	Gamma correction table register 0
0x3271	Gamma_Tab_1	7:0	R/W	0x1F	Gamma correction table register 1
0x3272	Gamma_Tab_2	7:0	R/W	0x2D	Gamma correction table register 2
0x3273	Gamma_Tab_3	7:0	R/W	0x3F	Gamma correction table register 3
0x3274	Gamma_Tab_4	7:0	R/W	0x4E	Gamma correction table register 4
0x3275	Gamma_Tab_5	7:0	R/W	0x5A	Gamma correction table register 5
0x3276	Gamma_Tab_6	7:0	R/W	0x6E	Gamma correction table register 6
0x3277	Gamma_Tab_7	7:0	R/W	0x7E	Gamma correction table register 7
0x3278	Gamma_Tab_8	7:0	R/W	0x8E	Gamma correction table register 8
0x3279	Gamma_Tab_9	7:0	R/W	0x9C	Gamma correction table register 9
0x327A	Gamma_Tab_10	7:0	R/W	0xB4	Gamma correction table register 10
0x327B	Gamma_Tab_11	7:0	R/W	0xC9	Gamma correction table register 11
0x327C	Gamma_Tab_12	7:0	R/W	0xDD	Gamma correction table register 12
0x327D	Gamma_Tab_13	7:0	R/W	0xEE	Gamma correction table register 13
0x327E	Gamma_Tab_14	7:0	R/W	0xFF	Gamma correction table register 14

11.5. SOC Auto-White Balance Registers (0x3290)

Address	Register Name	Bits	R/W	Reset Value	Descriptions
					WB_Gain_R [9:0]
0x3290	WB_Gain_R_H	1:0	R/W	0x01	AWB Gain R
0x3291	WB_Gain_R_L	7:0	R/W	0x00	
0x3292	-	-	-	-	Reserved
0x3293	-	-	-	-	Reserved
0x3294	-	-	-	-	Reserved
0x3295	-	-	-	-	Reserved
					WB_Gain_B [9:0]
0x3296	WB_Gain_B_H	1:0	R/W	0x01	AWB Gain B
0x3297	WB_Gain_B_L	7:0	R/W	0x00	
0x3298	CA_Result_R	7:0	R	-	Color accumulation result R
0x3299	CA_Result_G	7:0	R	-	Color accumulation result G
0x329A	CA_Result_B	7:0	R	-	Color accumulation result B
0x329B	AWB_Control_0	7:0	R/W	0x00	
	AWB_Conve_Range	7:4	R/W	0	AWB convergence range
	-	3:0	R	0	Reserved
0x329C	AWB_Control_1	7:0	R/W	0x4A	
	AWB_Fine_Tune_Thr	7:3	R/W	9	If difference less than this register, into fine tune mode.
	AWB_Fine_Tune_Step	2:0	R/W	2	AWB fine tune adjustment step 0: No effect. 1: Slowly. 7: Quickly.
0x329D	AWB_Fast_Tune_thr1	6:0	R/W	0x23	Fast speed
0x329E	AWB_Fast_Tune_thr2	6:0	R/W	0x19	Middle speed
0x329F	AWB_Fast_Tune_thr3	6:0	R/W	0x0F	Slow speed
0x32A0	AWB_Fast_Tune_Step	7:0	R/W	0x78	

11.6. SOC Auto-Exposure Registers (0x32B0)

Address	Register Name	Bits	R/W	Reset Value	Descriptions
0x32B0	Statistics_Mode	1:0	R/W	0x00	Luminance accumulation mode 00: Average 01: Pointer 1x: Center Weighting
0x32B1	LA_Weighting	7:0	R/W	0x11	
					LA_X0 [9:0]
0x32B2	LA_X0_H	1:0	R/W	0x01	Left-top X
0x32B3	LA_X0_L	7:0	R/W	0x0B	
					LA_Y0 [9:0]
0x32B4	LA_Y0_H	1:0	R/W	0x00	Left-top Y
0x32B5	LA_Y0_L	7:0	R/W	0xC8	
					LA_X1 [9:0]
0x32B6	LA_X1_H	1:0	R/W	0x02	Right-bottom X
0x32B7	LA_X1_L	7:0	R/W	0x12	
					LA_Y1 [9:0]
0x32B8	LA_Y1_H	1:0	R/W	0x01	Right-bottom Y
0x32B9	LA_Y1_L	7:0	R/W	0x90	
0x32BA	LA_Result	7:0	R	-	Luminance accumulation result [7:0]
0x32BB	AE_Control_0	5:0	R/W	0x0D	
	Anti_Shake_En	5	R/W	0	Anti-Shake enable 0: Disable 1: Enable
	-	-	R	0	Reserved
	Manual_Set_Flicker	3	R/W	1	Manual set flicker frequency. 0: 60Hz 1: 50Hz
	-	-	R	0	Reserved
	AE_Anti_Flicker_En	1	R/W	0	Anti-flicker enable 0: Disable 1: Enable
	AE_AGC_En	0	R/W	1	AGC enable 0: Disable 1: Enable
0x32BC	AE_Target_Lum	7:0	R/W	0x40	AE target luminance
0x32BD	AE_ConvRange_Upper	6:0	R/W	0x00	AE convergence range upper
0x32BE	AE_ConvRange_Lower	6:0	R/W	0x07	AE convergence range lower
0x32BF	AE_Control_1	7:0	R/W	0x4A	
	AE_Fast_Tune_Thr_2	7:5	R/W	2	Thr_2 always > thr_1.
	AE_Fast_Tune_Thr_1	4:3	R/W	1	0: No effect 1: Fast

					3: Slow
	AE_Adjustment_Speed	2:0	R/W	2	0: no effect 1: Quickly 7: smoothly
0x32C0	AE_Control_2	7:0	R/W	0x22	
	AEC_Adjust_Step_3	7:4	R/W	2	Fast speed for AEC
	AEC_Adjust_Step_2	3:1	R/W	1	Middle speed for AEC
	AEC_Adjust_Step_1	0	R/W	0	Slow speed for AEC
0x32C1	AE_Control_3	7:0	R/W	0x45	
	AEC_Min_ExpLine	7:4	R/W	4	Minimum exposure line limit for AEC
	AEC_Max_ExpLine_H	3:0	R/W	5	AE_Max_ExpLine [11:8] Maximum exposure line limit for AEC.
0x32C2	AEC_MaxExpLine_L	7:0	R/W	0	AE_Max_ExpLine [7:0]
0x32C3	AGC_Min_Limit	7:0	R/W	0	Minimum gain limit for AGC
0x32C4	-	-	-	-	Reserved
0x32C5	AGC_Max_Limit	7:0	R/W	0x5F	AE_AGC_Max_Limit [7:0]
0x32C6	AGC_Adjust_Step_3	5:0	R/W	0x18	Fast speed for AGC
0x32C7	AE_Control_5	7:0	R/W	0x64	
	AGC_Adjust_Step_2	7:3	R/W	0xC	Middle speed for AGC
	AGC_Adjust_Step_1	2:0	R/W	0x4	Slow speed for AGC
0x32C8	AE_Flicker_50Hz	7:0	R/W	0x3C	AE flicker exposure line 50 Hz Set 1/200 Sec into this register.
0x32C9	AE_Flicker_60Hz	7:0	R/W	0x32	AE flicker exposure line 60 Hz Set 1/240 Sec into this register.

11.7. SOC Scaler Registers (0x32E0)

Address	Register Name	Bits	R/W	Reset Value	Descriptions
					Scaler_Out_Size_X [10:0] †
0x32E0	Scaler_Out_Size_X_H	2:0	R/W	0x06	Output horizontal size (Even size only) Minimun width is 56.
0x32E1	Scaler_Out_Size_X_L	7:0	R/W	0x40	
					Scaler_Out_Size_Y [10:0] †
0x32E2	Scaler_Out_Size_Y_H	2:0	R/W	0x04	Output vertical size (Even size only) Minimun height is 42.
0x32E3	Scaler_Out_Size_Y_L	7:0	R/W	0xB0	
0x32E4	HSC_SCF_I	4:0	R/W	0x00	Integer part of horizontal scaling factor †
0x32E5	HSC_SCF	7:0	R/W	0x00	Fraction part of horizontal scaling factor †
0x32E6	VSC_SCF_I	4:0	R/W	0x00	Integer part of vertical scaling factor †
0x32E7	VSC_SCF	7:0	R/W	0x00	Fraction part of vertical scaling factor †
0x32E8	Scaling_Mode_Sel	0	R/W	0x01	Horizontal and vertical scaling methods † 0: Zero-order 1: BiLinear

† New register values are accepted by enabling LOAD bit in register 0x3060.

11.8. SOC Output Format and Specical Effects Registers (0x32F0)

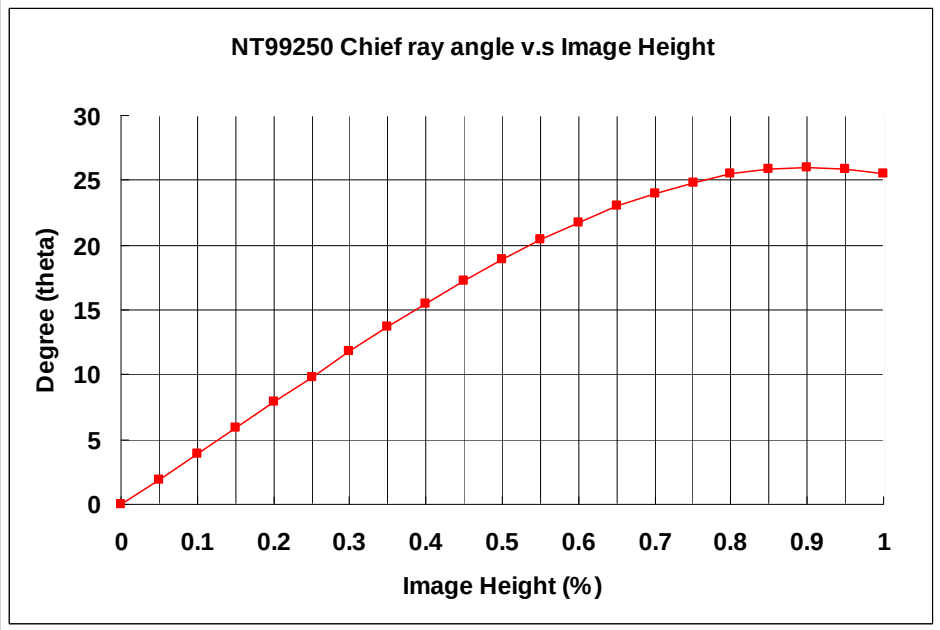
Address	Register Name	Bits	R/W	Reset Value	Descriptions
0x32F0	Output_Format	7:0	R/W	0x00	
	YCbCr_To_RGB_En	7	R/W	0	YCbCr to RGB 0: Disable 1: Enable
	Output_Format_Sel	6:4	R/W	0	Output format 0: YCbCr 1: RGB565 2: RGB555 3: RGB444x 4: RGBx444 5: Raw-10 bits
	Raw_Output_Ch_Sel	3:2	R/W	0	Raw-10 bits mode only 0: R start 1: Gr start 2: Gb start 3: B start
	RB_Swap	1	R/W	0	R and B swap 0: Disable 1: In YCbCr mode, swap Cb and Cr. In RGB mode, swap Red and Blue.
	Output_Byte_Swap	0	R/W	0	Output byte swap 0: Disable 1: In YCbCr mode, swap chroma and luminance byte. In RGB mode, swap odd and even byte.
0x32F1	Special_Effect_0	4:0	R/W	0x00	
	Output_Limit	4:3	R/W	0	00: Data value from 0 to 255. 01: Data value from 1 to 254. 10: Y data from 16 to 235; C value form 16 to 240. 11: Reserved.
	Effect_Option	2:0	R/W	0	000: Normal 001: Black and White 010: Sepia 011: Negative 100: Solarization 101: User define 110: Reserved 111: Reserved
0x32F2	Y_Component	7:0	R/W	0x80	Y component.
0x32F3	Chroma_Component	7:0	R/W	0x80	Cb/Cr components. For special effect.
0x32F4	Cb_Ofs	7:0	R/W	0x80	Cb offset. For special effect.
0x32F5	Cr_Ofs	7:0	R/W	0x80	Cr offset. For special effect.
0x32F6	Special_Effect_1	5:0	R/W	0x00	
	Half_Invert	5	R/W	0	Special effect: Solarization.
	Invert	4	R/W	0	Special effect. Negative.
	Se_C_Component_En	3	R/W	0	Cb/Cr component enable in color component adjustment 0: Disable

				1: Enable
Se_Y_Component_En	2	R/W	0	Y component enable in color component adjustment 0: Disable 1: Enable
-	1:0	R	0	Reserved

11.9. Image Quality Control Registers (0x3300)

Address	Register Name	Bits	R/W	Reset Value	Descriptions
0x3300	Noise_Enh_Param	7:0	R/W	0x12	
	Edge_Enhancement_H	7:6	R/W	0	Edge_Enhancement [9:8]
	Noise_Reduction_Val	5:0	R/W	0x12	Noise reduction Set rbw and gw in the same time
0x3301	Edge_Enhancement_L	7:0	R/W	0x80	Edge_Enhancement [7:0]
					Matrix_RR [10:0]
0x3302	Matrix_RR_H	2:0	R/W	0x00	Color correction and transform matrix
0x3303	Matrix_RR_L	7:0	R/W	0x4D	
					Matrix_RG [10:0]
0x3304	Matrix_RG_H	2:0	R/W	0x00	Color correction and transform matrix
0x3305	Matrix_RG_L	7:0	R/W	0x96	
					Matrix_RB [10:0]
0x3306	Matrix_RB_H	2:0	R/W	0x00	Color correction and transform matrix
0x3307	Matrix_RB_L	7:0	R/W	0x1D	
					Matrix_GR [10:0]
0x3308	Matrix_GR_H	2:0	R/W	0x07	Color correction and transform matrix
0x3309	Matrix_GR_L	7:0	R/W	0xD5	
					Matrix_GG [10:0]
0x330A	Matrix_GG_H	2:0	R/W	0x07	Color correction anmd transform matrix
0x330B	Matrix_GG_L	7:0	R/W	0xAB	
					Matrix_GB [10:0]
0x330C	Matrix_GB_H	2:0	R/W	0x00	Color correction and transform matrix
0x330D	Matrix_GB_L	7:0	R/W	0x80	
					Matrix_BR [10:0]
0x330E	Matrix_BR_H	2:0	R/W	0x00	Color correction and transform matrix
0x330F	Matrix_BR_L	7:0	R/W	0x80	
					Matrix_BG [10:0]
0x3310	Matrix_BG_H	2:0	R/W	0x07	Color correction and transform matrix
0x3311	Matrix_BG_L	7:0	R/W	0x95	
					Matrix_BB [10:0]
0x3312	Matrix_BB_H	2:0	R/W	0x07	Color correction and transform matrix
0x3313	Matrix_BB_L	7:0	R/W	0xEB	

12. Chief Ray Angle



13. Electrical Characteristics

13.1. Absoulte Maximum Ratings

VDD Supply Voltage	-0.3	to	+2.0V
VDDIO / AVDD Supply Voltage	-0.3	to	+3.3V
Operating Ambient Temperature	-20^0C	to	$+70^0$C
Storage Temperature	-40^0C	to	$+85^0$C

Comment

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

13.2. DC Characteristics

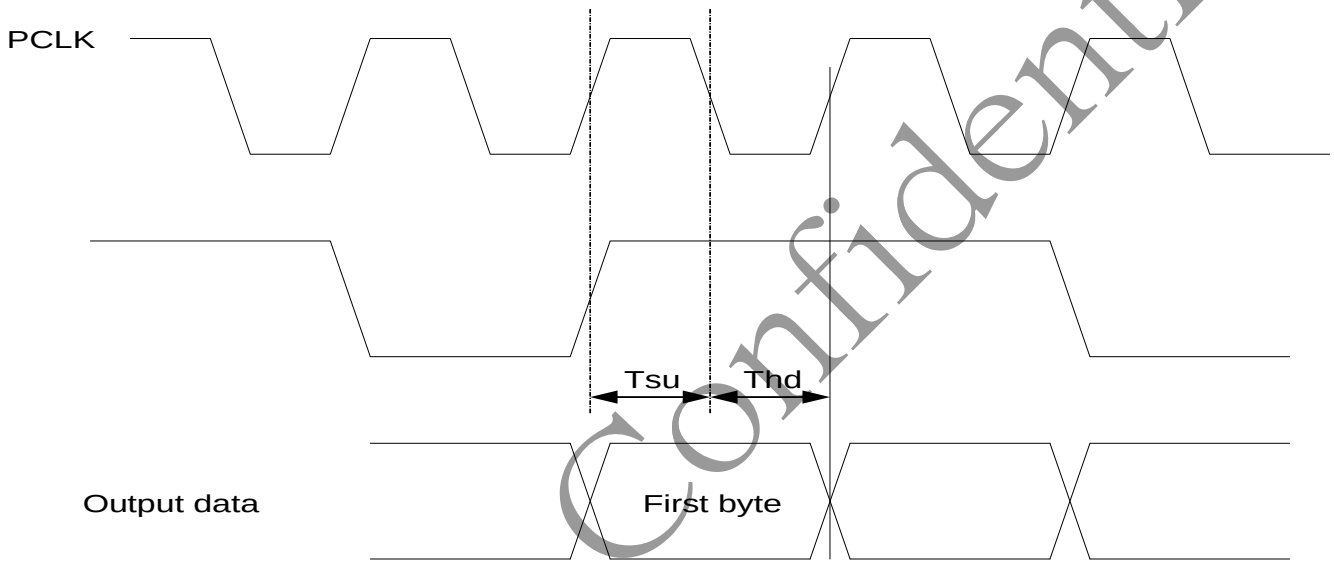
Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
VDD	Digital Logic Supply Voltage	1.425	1.5	1.575	V	
VDDIO	I/O Interface Supply Voltage	1.7	2.8	3.1	V	
AVDD	Analog Supply Voltage	2.5	2.8	3.1	V	
AVDDPIX	Pixel Supply Voltage	2.5	2.8	3.1	V	
P_{RUN}	Operating Power Consumption	-	123	-	mW	10fps @ full resolution
I_{VDD}	Digital Logic Operating Current	-	24	-	mW	10fps @ full resolution (external 1.5V)
I_{VDDIO}	I/O Operating Current	-	65.8	-	mW	10fps @ full resolution (internal LDO)
I_{AVDD}	AVDD Operating Current	-	56	-	mW	10fps @ full resolution
V_{IH}	Input High Voltage	0.7 x VDDIO	-	-	V	
V_{IL}	Input Low Voltage	-	-	0.3 x VDDIO	V	
I_{OH}	Output Driving Current VDDIO = 2.8V	-	5	-		V_{OH}=VDDIO-0.3V, 4mA setting
I_{OL}	Output Sinking Current VDDIO = 2.8V	-	6.5	-		V_{OL}=GND+0.3V, 4mA setting
I_{OH}	Output Driving Current VDDIO = 1.8V	-	3.6	-		V_{OH}=VDDIO-0.3V, 4mA setting
I_{OL}	Output Sinking Current VDDIO = 1.8V	-	4	-		V_{OL}=GND+0.3V, 4mA setting
I_{OZ}	Tri-state Output Leakage Current	-	-	±1	μA	
R_{PU}	Internal Pull-up Resistor	40	75	190	KΩ	

13.3. AC Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
F_{OSC}	Frequency MCLK	6	26	27	MHz	
	Duty cycle	45	-	55	%	

Horizontal Timing

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
Tsu	Output data setup time	-	10	-	ns	VDDIO=2.8V
Thd	Output data hold time	-	10	-	ns	PCLK=48MHz



Two-wire Serial Interface Timing

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
Tsclk	Serial Interface Input Clock Frequency	-	-	400	KHz	
T_{high}	High Period of The SCLK Clock	0.6	-	-	µs	
T_{low}	Low Period of The SCLK Clock	1.3	-	-	µs	
$T_{STR:SU}$	Start Setup Time	0.6	-	-	µs	
$T_{STR:HD}$	Start Hold Time	0.6	-	-	µs	
$T_{STP:SU}$	Stop Setup Time	0.6	-	-	µs	
$T_{DAT:SU}$	DATA Setup Time	0.1	-	-	µs	
$T_{DAT:HD}$	DATA Hold Time	0	-	-	µs	
T_{BUF}	Bus Free Time between a STOP and START Condition	1.3	-	-	µs