理解mipi协议 - 与时俱进的专栏 - 博客频道

分类：

LCD驱动（3）

完成mipi信号通道分配后，需要生成与物理层对接的时序、同步信号：

MIPI规定，传输过程中，包内是200mV、包间以及包启动和包结束时是1.2V，两种不同的电压摆幅，需要两组不同的LVDS驱动电路在轮流切换工作；为了传输过程中各数据包之间的安全可靠过渡，从启动到数据开始传输，MIPI定义了比较长的可靠过渡时间，加起来最少也有600多ns；而且规定各个时间参数是可调的，所以需要一定等待时间，需要缓存，我们用寄存器代替FIFO，每通道128Byte。

串行时钟与数据差分传输的过渡时间关系如下：

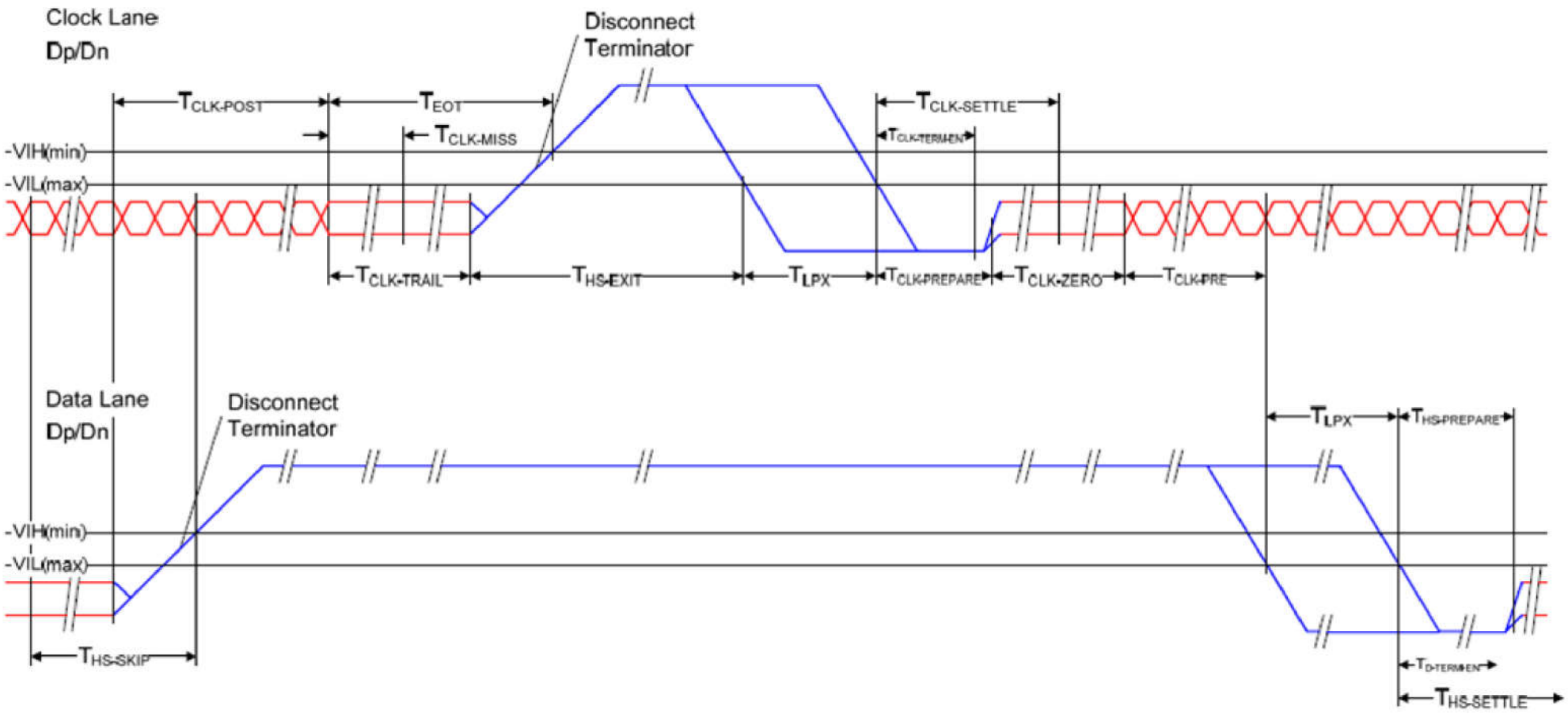


Figure 21 Switching the Clock Lane between Clock Transmission and Low-Power Mode

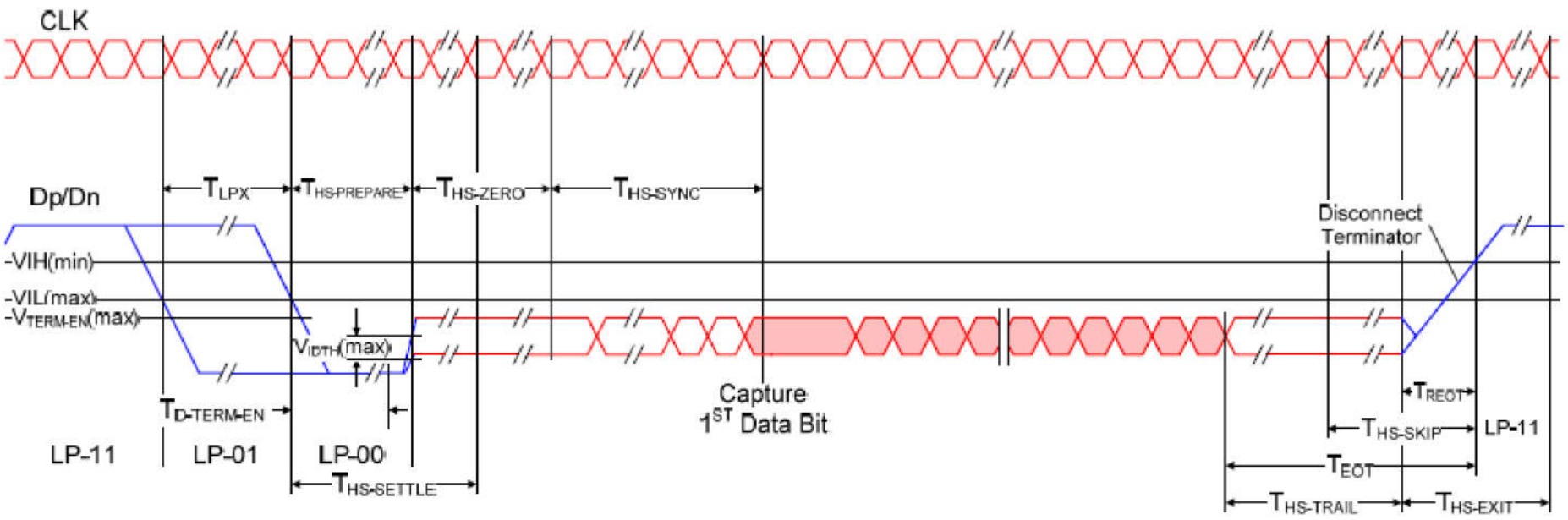
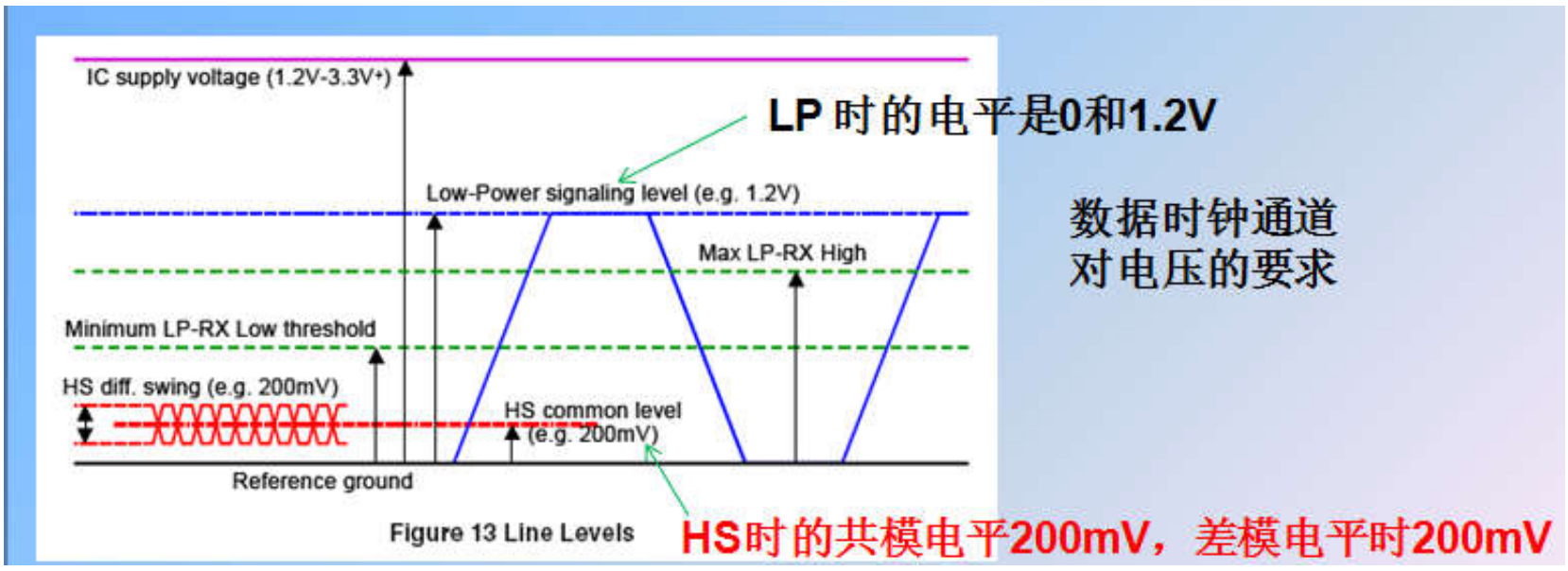


Figure 14 High-Speed Data Transmission in Bursts



各个时间参数需要满足以下的要求：

Table 14 Global Operation Timing Parameters

Parameter	Description	Min	Typ	Max	Unit	Notes
$T_{CLK-MISS}$	Timeout for receiver to detect absence of Clock transitions and disable the Clock Lane HS-RX.			60	ns	1, 6
$T_{CLK-POST}$	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of $T_{HS-TRAIL}$ to the beginning of $T_{CLK-TRAIL}$.	60 ns + 52*UI			ns	5
$T_{CLK-PRE}$	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8			UI	5
$T_{CLK-PREPARE}$	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	38		95	ns	5
$T_{CLK-SETTLE}$	Time interval during which the HS receiver shall ignore any Clock Lane HS transitions, starting from the beginning of $T_{CLK-PREPARE}$.	95		300	ns	6
$T_{CLK-TERM-EN}$	Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$.	Time for Dn to reach $V_{TERM-EN}$		38	ns	6
$T_{CLK-TRAIL}$	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst.	60			ns	5
$T_{CLK-PREPARE} + T_{CLK-ZERO}$	$T_{CLK-PREPARE}$ + time that the transmitter drives the HS-0 state prior to starting the Clock.	300			ns	5
$T_{D-TERM-EN}$	Time for the Data Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$.	Time for Dn to reach $V_{TERM-EN}$		35 ns + 4*UI		6
T_{EOT}	Transmitted time interval from the start of $T_{HS-TRAIL}$ or $T_{CLK-TRAIL}$, to the start of the LP-11 state following a HS burst.			105 ns + n*12*UI		3, 5
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst.	100			ns	5

Parameter	Description	Min	Typ	Max	Unit	Notes
$T_{HS-PREPARE}$	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission	40 ns + 4*UI		85 ns + 6*UI	ns	5
$T_{HS-PREPARE} + T_{HS-ZERO}$	$T_{HS-PREPARE}$ + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.	145 ns + 10*UI			ns	5
$T_{HS-SETTLE}$	Time interval during which the HS receiver shall ignore any Data Lane HS transitions, starting from the beginning of $T_{HS-PREPARE}$.	85 ns + 6*UI		145 ns + 10*UI	ns	6
$T_{HS-SKIP}$	Time interval during which the HS-RX should ignore any transitions on the Data Lane, following a HS burst. The end point of the interval is defined as the beginning of the LP-11 state following the HS burst.	40		55 ns + 4*UI	ns	6
$T_{HS-TRAIL}$	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst	max(n*8*UI, 60 ns + n*4*UI)			ns	2, 3, 5
T_{INIT}	See section 5.11.	100			µs	5
T_{LPX}	Transmitted length of any Low-Power state period	50			ns	4, 5
Ratio T_{LPX}	Ratio of $T_{LPX(MASTER)}/T_{LPX(SLAVE)}$ between Master and Slave side	2/3		3/2		
T_{TA-GET}	Time that the new transmitter drives the Bridge state (LP-00) after accepting control during a Link Turnaround.	5*T_{LPX}			ns	5
T_{TA-GO}	Time that the transmitter drives the Bridge state (LP-00) before releasing control during a Link Turnaround.	4*T_{LPX}			ns	5
$T_{TA-SURE}$	Time that the new transmitter waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	T_{LPX}		2*T_{LPX}	ns	5
T_{WAKEUP}	Time that a transmitter drives a Mark-1 state prior to a Stop state in order to initiate an exit from ULPS.	1			ms	5

Notes

1. The minimum value depends on the bit rate. Implementations should ensure proper operation for all the supported bit rates.
2. If a > b then max(a, b) = a otherwise max(a, b) = b
3. Where n = 1 for Forward-direction HS mode and n = 4 for Reverse-direction HS mode
4. T_{LPX} is an internal state machine timing reference. Externally measured values may differ slightly from the specified values due to asymmetrical rise and fall times.
5. Transmitter-specific parameter
6. Receiver-specific parameter

UI 的值：

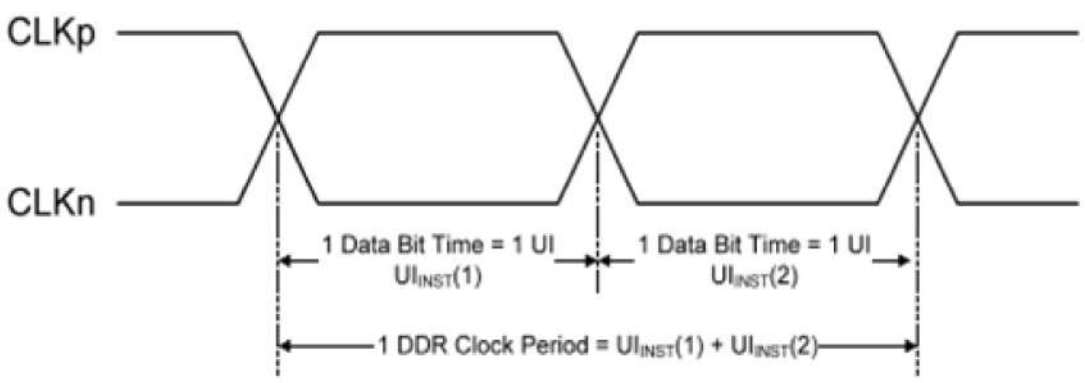


Figure 50 DDR Clock Definition

Table 26 Clock Signal Specification

Clock Parameter	Symbol	Min	Typ	Max	Units	Notes
UI instantaneous	UI_{INST}			12.5	ns	1,2

Notes:

时钟通道的最小值是40MHz

1. This value corresponds to a minimum 80 Mbps data rate.
2. The minimum UI shall not be violated for any single bit period, i.e., any DDR half cycle within a data burst.

数据与时钟的相位关系：

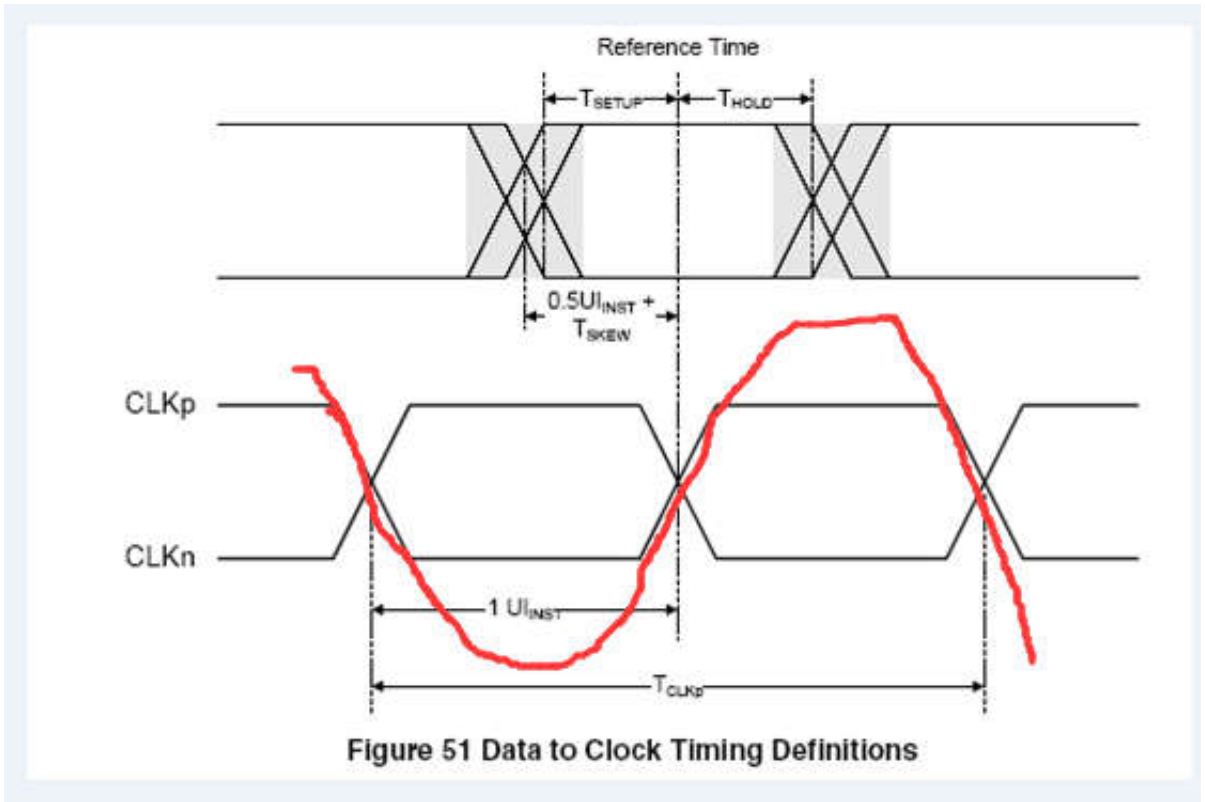


Figure 51 Data to Clock Timing Definitions

根据前面文章:[mipi差分信号原理]() 介绍。

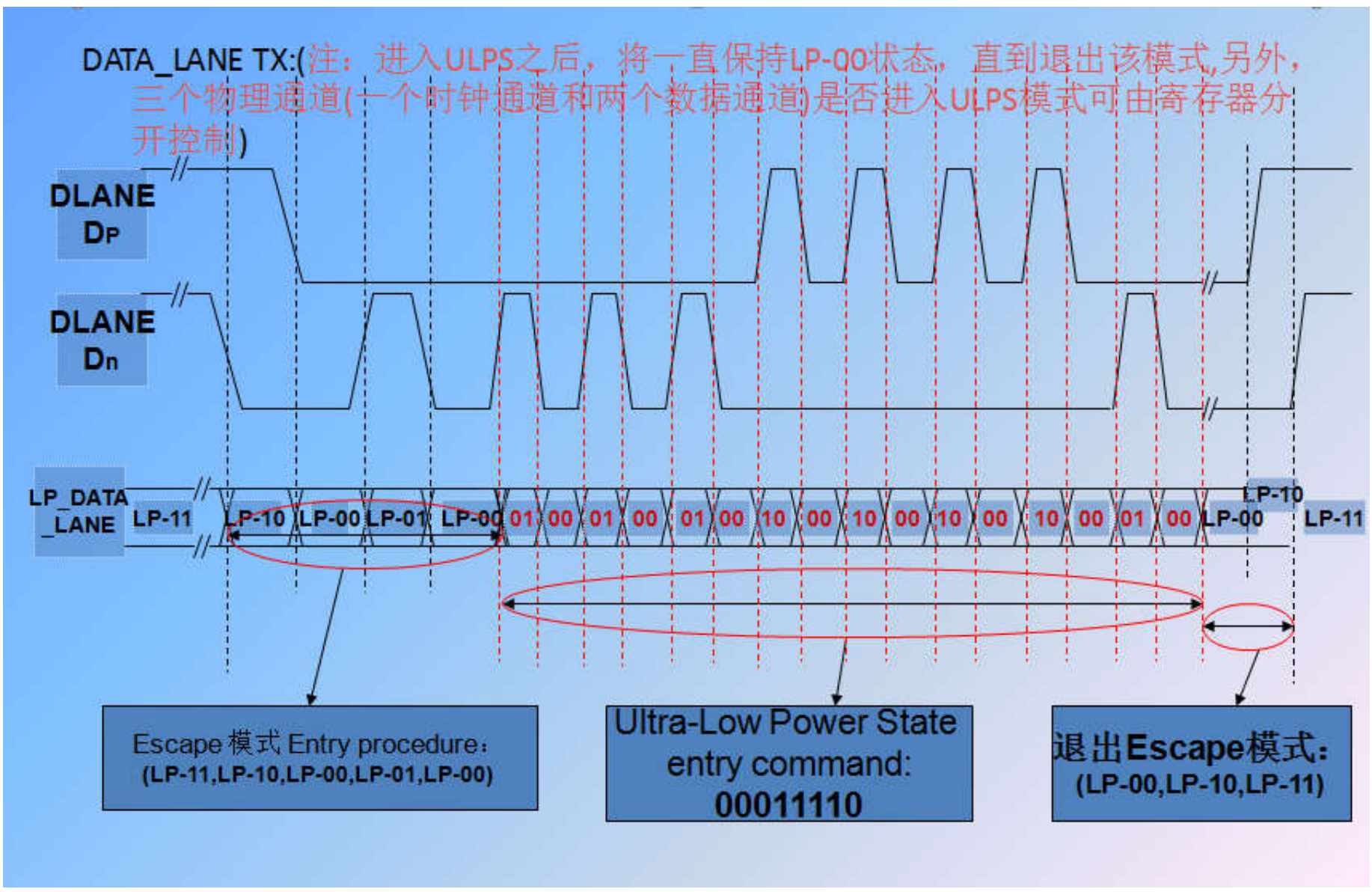
CLKp是高电平，CLKn是低电平的时候，差分信号表现为高电平。

CLKn是高电平，CLKp是低电平的时候，差分信号表现为低电平。

所以结果就可以等效成红线描述的正弦。

从正弦可以看出，data在clk的高电平和低电平都有传输数据。

数据通道进入和退出SLM(即睡眠模式)的控制：



mipi信号传输分为单端和差分传输。例如：

LP-00, LP-01, LP-10, LP-11 (单端)

HS-0, HS-1 (差分)

Ultra-Low Power State entry command: 00011110 是差分传输，读取方法和上面提到的clk是一样的，需要注意的是Dp和Dn如果同时是高电平或同时是低电平的时候是无效数据，这个时候大概对应的是clk正弦的峰值，只有其中一个是高一个是低才是有效的差分数据。

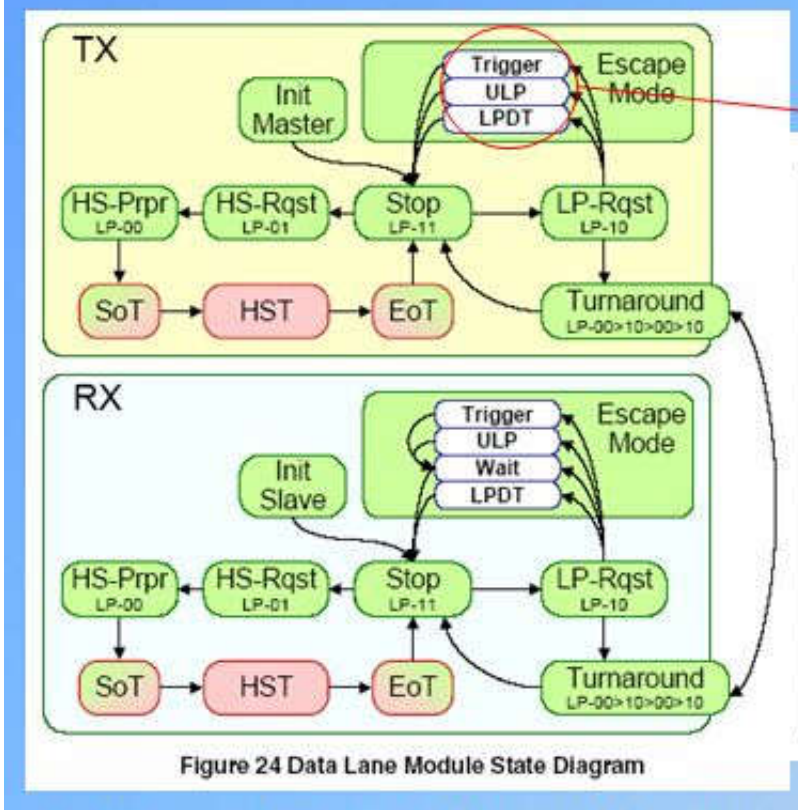


Figure 24 Data Lane Module State Diagram

数据通道中各种模式转换的状态图

Table 8 Escape Entry Codes

Escape Mode Action	Command Type	Entry Command Pattern (first bit transmitted to last bit transmitted)
Low-Power Data Transmission	mode	11100001
Ultra-Low Power State	mode	00011110
Undefined-1	mode	10011111
Undefined-2	mode	11011110
Reset-Trigger [Remote Application]	Trigger	01100010
Unknown-3	Trigger	01011101
Unknown-4	Trigger	00100001
Unknown-5	Trigger	10100000

进入各种状态数据通道需要发送的命令

总结：

对应于同步信号完成并串转换；

*HS 状态为高速低压差分信号，传输高速连续串行数据；

*LP 状态为低速低功耗信号，传输控制信号和状态信号；

*MIPI要求HS 工作在1GHz 的频率下，完成共模信号为0.2v 差模信号为0.2v 的差分信号的传输；

*LP 传递控制信号，要求高电平为1.2v 低电平为0的电平信号输出；

*HS 及LP 状态下，输出信号的电学特性要求非常苛刻，具体电学性能的要求可见附带文档表格。

*MIPI是双向可选的，可以高速发送，也可以进行高速接收，或收发功能同时具备，我们目前根据需求仅做了发送功能；

*MIPI的HS模式（0.2V），传送图像数据，速度为80Mbps ~ 1000Mbps；

*MIPI的LP模式（1.2V），可以用于传送控制命令，最高速度为10Mbps；

*MIPI规定，任一个MIPI设备必须Escape Mode，此为Low Power Data Trabsmission Mode，LP模式中的一种，此模式下可低速传输图像或其他数据。

*MIPI规定了Low Power Mode、 Ultra Low Power Mode的电压范围、以及它们之间、它们与HS模式之间的相互切换方式或相关要求；

*MIPI D-PHY是各个MIPI工作组共用的物理层规范；

最后，需要注意一点：

BTA：bus turn around，用来host接受外设发送命令或应答信号用的，如果host DPHY设置了这个，但是lcd不支持的话，就有可能有问题。

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