1/5’’ UXGA CMOS Image Sensor

GC2015

DataSheet

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GalaxyCore Inc.

Content

GALAXYCORE CONFIDENTIAL

Sensor Overview

1.1 General Description

The GC2015 features 1600V x 1200H resolution with 1/5-inch optical format, and 4-transistor pixel structure for high image quality and low noise variations.

The full scale integration of high-performance and low-power functions makes the GC2015 best fit the design, reduce implementation process, and extend the battery life of cell phones, PDAs, and a wide variety of mobile applications.

The on-chip ISP provides a very smooth AE (Auto Exposure) and accurate AWB(Auto White Balance) control. It provides various data formats, such as Bayer RGB, RGB565,YCbCr 4:2:2. It has a commonly used two-wire serial interface for host to control the operation of the whole sensor.

1.2 Features

- Standard optical format of 1/5 inch
- Various output formats: YCbCr4:2:2, RGB565, Raw Bayer
- Windowing support
- Horizontal /Vertical mirror
- Image processing module
- Package: CSP

1.3 Application

- Cellular Phone Cameras
- Notebook and desktop PC cameras
- PDAs
- Toys

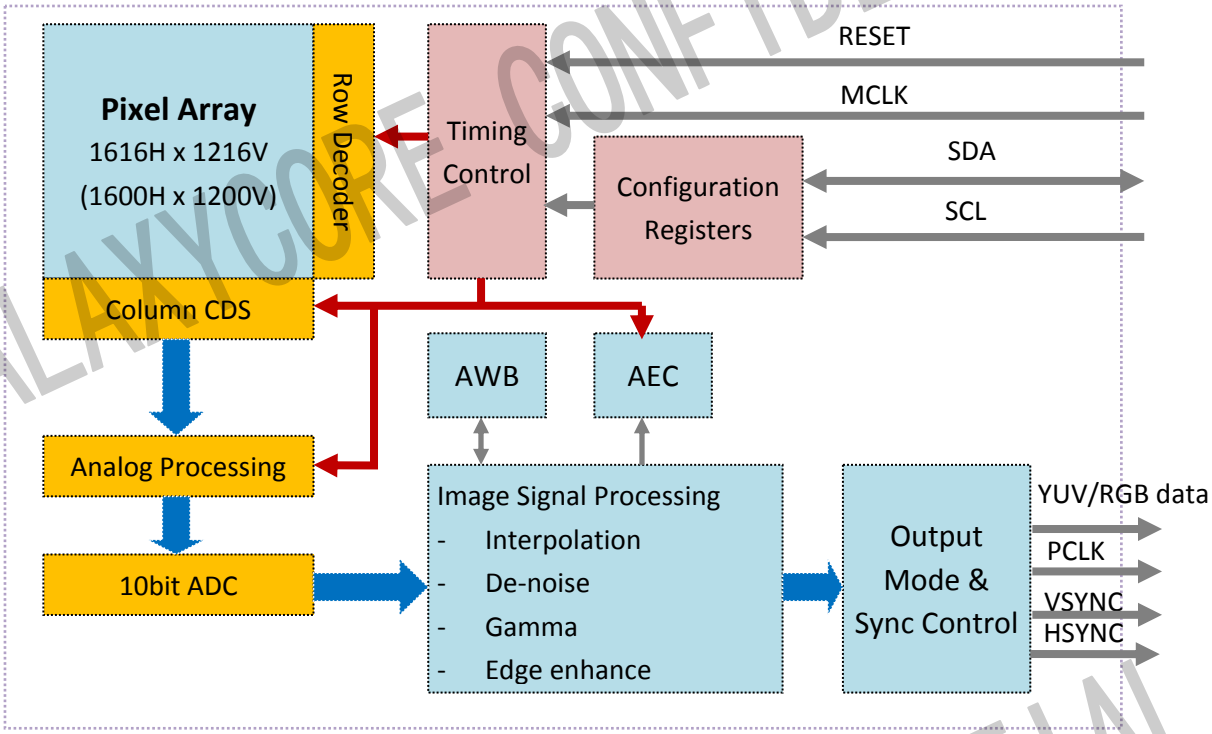
- Digital still cameras and camcorders
- Video telephony and conferencing equipments
- Security systems
- Industrial and environmental systems

1.4 Technical Specifications

Parameter	Typical value
Optical Format	1/5 inch
Pixel Size	1.75um x 1.75um
Active pixel array	1616 x 1216
ADC resolution	10-bit ADC
Max Frame rate	Preview mode(SVGA):25fps@48M MCLK
	Capture mode(UXGA):12fps@48M MCLK
Power Supply	DVDD28: 2.7 ~ 3.3V DVDD15: 1.4~1.9V IOVDD: 1.7~3.3V
Power Consumption	120mW
SNR	TBD
Dark Current	TBD
Sensitivity	TBD
Operating temperature:	-20~70℃
Stable Image temperature	0~50℃
Optimal lens chief ray angle(CRA)	25 degree(see figure of Chief Ray angle)
Package type	CSP

2. Block level description

2.1 Block diagram



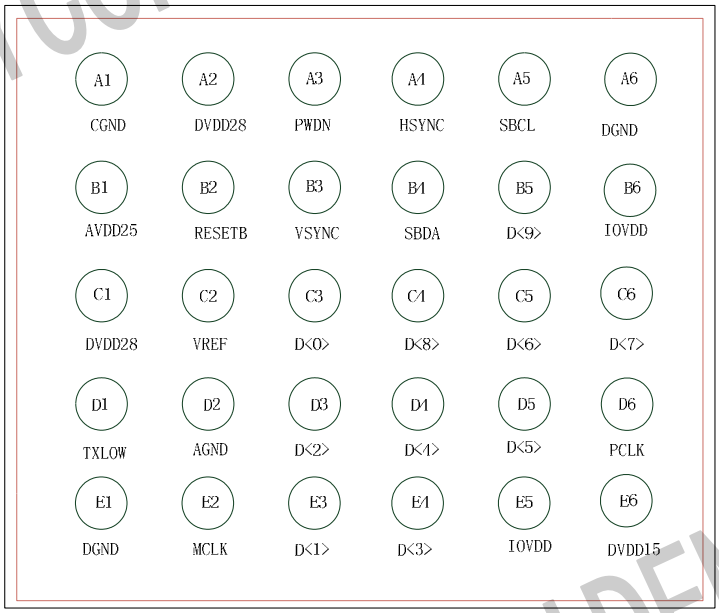
GC2015 has an active image array of 1616x1216 pixels. The active pixels are read out progressively through column/row driver circuits. In order to reduce fixed pattern noise, CDS circuits are adopted. The analog signal is transferred to digital signal by 10 bit A/D converter. The digital signals are processed in the ISP Block, including Bayer interpolation, denoise, color correction, gamma correction, data format conversion and so on. Users can easily control these functions via two-wire serial interface bus.

2.2 Signal descriptions

	Name	Pin type	Description
A1	**CGND**	Ground	Ground for sensor analog
A2	**DVDD28**	POWER	Power for analog circuit/sensor array
A3	**PWDN**	Input	power down (active high)
A4	**HSYNC**	Output	Horizontal reference output
A5	**SBCL**	Input	SCCB input clock
A6	**DGND**	Ground	Ground for digital
B1	**AVDD25**	POWER	Internal analog power
B2	**RESETB**	Input	reset (active high)
B3	**VSYNC**	Output	Vertical sync output
B4	**SBDA**	I/O	SCCB data
B5	**D<9>**	Output	YUV/RGB video port bit [7]
B6	**IOVDD**	POWER	Power Supply for I/O circuits，1.7~3.3V
C1	**DVDD28**	POWER	Power for analog circuit/sensor array
C2	**VREF**	Power	internal analog reference
C3	**D<0>**	Output	Raw RGB bit[0]
C4	**D<8>**	Output	YUV/RGB video port bit[6]
C5	**D<6>**	Output	YUV/RGB video port bit [4]
C6	**D<7>**	Output	YUV/RGB video port bit [5]
D1	**TXLOW**	Power	internal analog reference
D2	**AGND**	Ground	Ground for analog circuit/sensor array
D3	**D<2>**	Output	YUV/RGB video port bit [0]
D4	**D<4>**	Output	YUV/RGB video port bit [2]
D5	**D<5>**	Output	YUV/RGB video port bit [3]
D6	**PCLK**	Output	Pixel clock output
E1	**DGND**	Ground	Ground for digital circuit
E2	**INCLK**	Input	sensor input clock
E3	**D<1>**	Output	Raw RGB bit[1]

E4	**D<3>**	Output	YUV/RGB video port bit [1]
E5	**IOVDD**	POWER	Power Supply for I/O circuits，1.7~3.3V
E6	**DVDD15**	POWER	Power for digital core

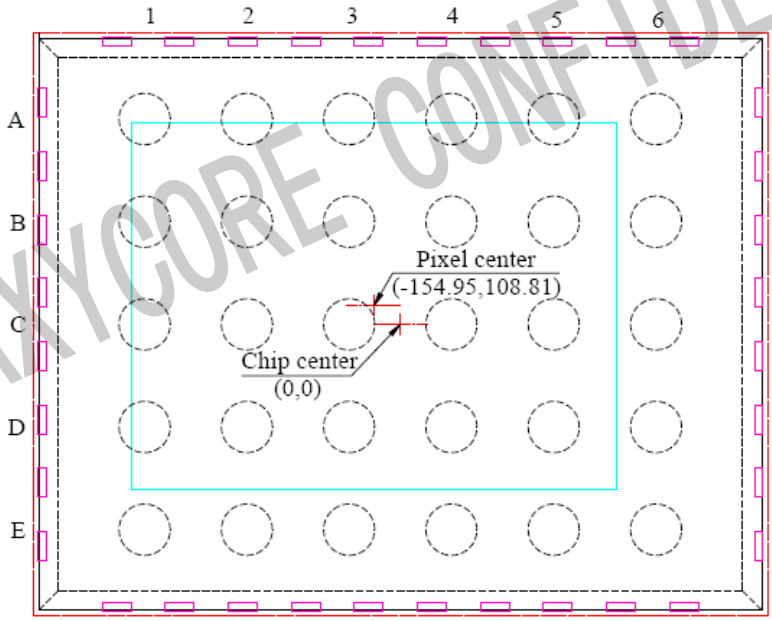
2.3 Pin Diagram



Top view

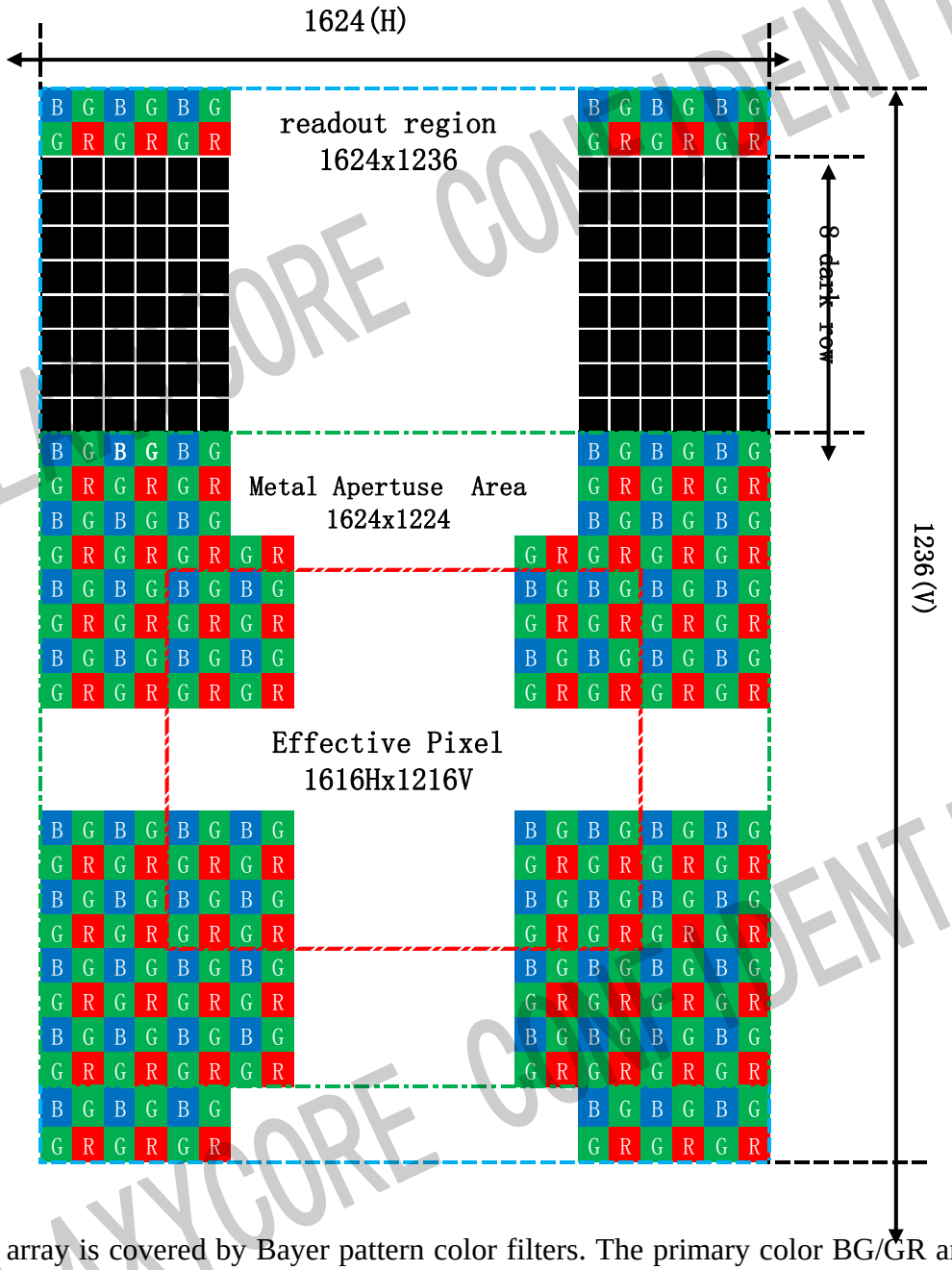
3. Optical specifications

3.1 Sensor array center



Top View

3.2 Pixel Array Structure



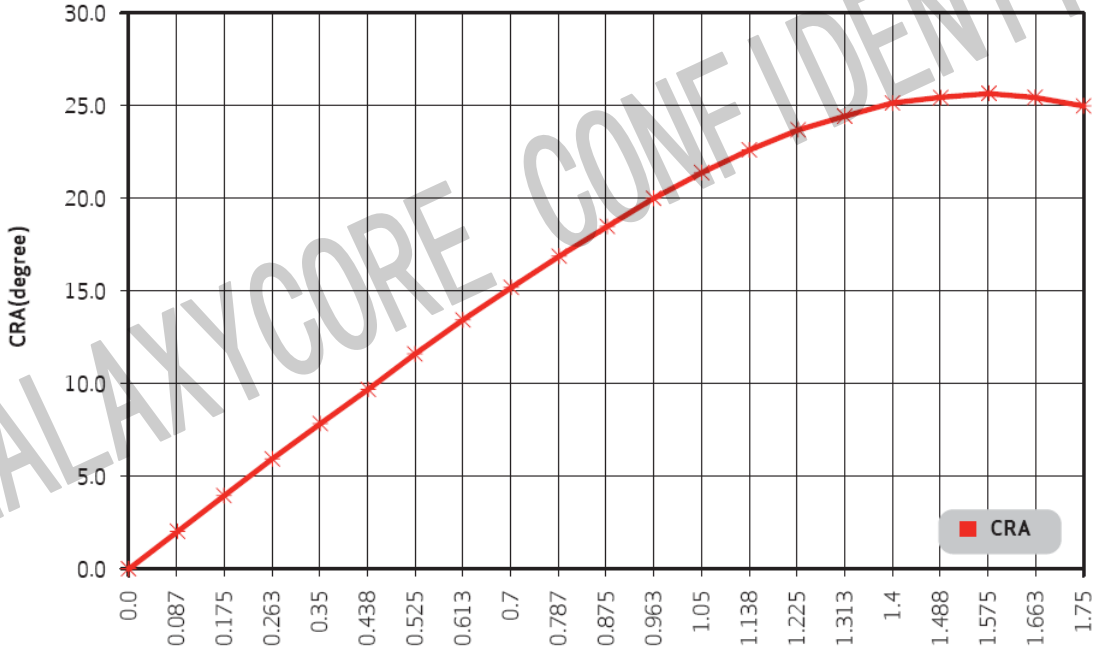
Pixel array is covered by Bayer pattern color filters. The primary color BG/GR array is arranged in line-alternating way.

If no flip in column, column is read out from 0 to 1615. If flip in column, column is read out from 1615 to 0.

If no flip in row, row is read out from 0 to 1215. If flip in row, row is read out from 1215 to 0.

3.3 Lens Chief Ray Angle(CRA)

Chief Ray angle (CRA)

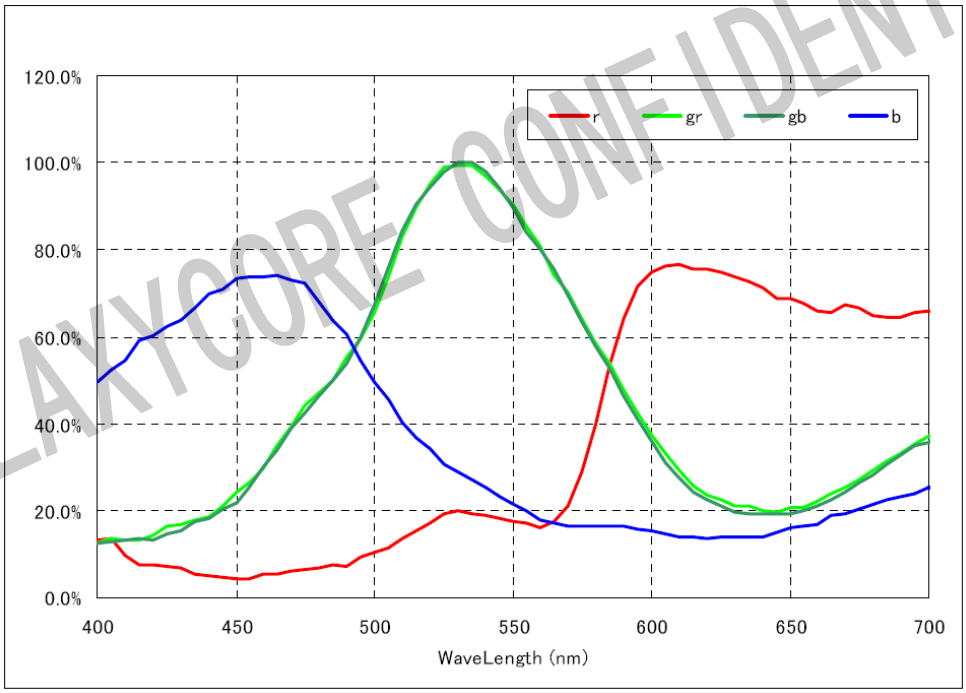


CRA versus image height plot

Field(%)	Image height(mm)	CRA(degrees)
0	0	0
10	0.177	4.15
20	0.354	8.25
30	0.531	12.2
40	0.708	15.83
50	0.885	18.98
60	1.062	21.61
70	1.239	23.62
80	1.416	24.82
90	1.593	25.39
100	1.77	25.78
110	1.895	25.89

3.4 Color Filter Spectral Characteristics

The optical spectrum of color filters is shown below



4. Two-wire Serial Bus Communication

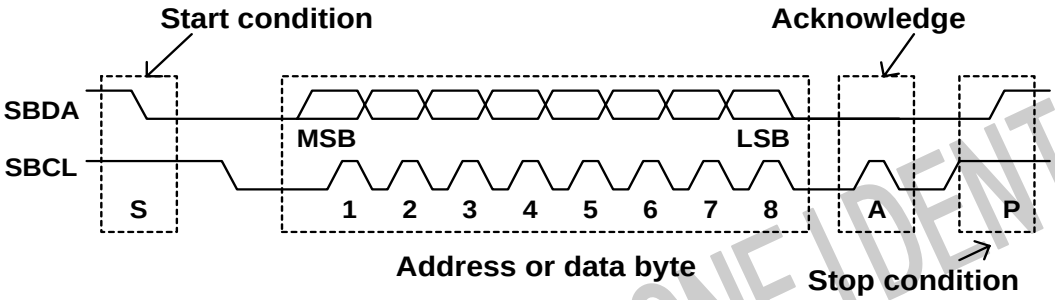
GC2015 Device Address:

serial bus write address = 0x60, serial bus read address = 0x61

4.1 Protocol

The host must perform the role of a communications master and GC2015 acts as either a slave receiver or transmitter. The master must do

- Generate the **Start(S)/Stop(P)** condition
- Provide the serial clock on **SBCL**.



Single Register Writing:

S	60H	A	Register Address	A	Data	A	P

Incremental Register Writing:

S	60H	A	Register Address	A	Data(1)	A	……	Data(N)	A	P

Single Register Reading:

S	60H	A	Register Address	A	S	61H	A	Data	NA	P

Incremental Register Reading:

S	60H	A	Register Address	A	S	61H	A	Data(1)	A	……	Data(N)	NA	P

Notes:

From master to slave

From slave to master

S: Start condition

P: Stop condition

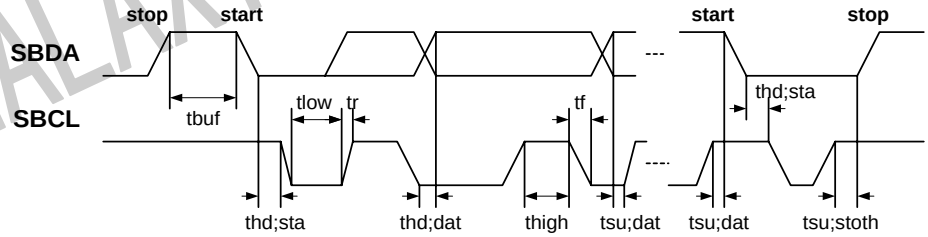
A: Acknowledge bit

NA: No acknowledge

Register Address: Sensor register address

Data: Sensor registers value

4.2 Serial Bus Timing

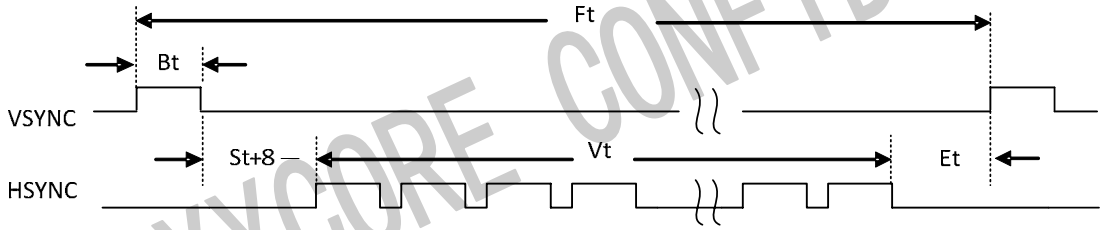


Parameter	Symbol	Min.	Max.	Unit
SBCL clock frequency	fscl	0	400	KHz
Bus free time between a stop and a start	tbuf	1.2	*	μs
Hold time for a repeated start	thd;sta	1.0	*	μs
LOW period of SBCL	tlow	1.2	*	μs
HIGH period of SBCL	thigh	1.0	*	μs
Set-up time for a repeated start	tsu;sta	1.2	*	ns
Data hold time	thd;dat	1.3	*	ns
Data Set-up time	tsu;dat	250	*	ns
Rise time of SBCL, SBDA	tr	*	250	ns
Fall time of SBCL, SBDA	tf	*	300	ns
Set-up time for a stop	tsu;sto	1.2	*	μs
Capacitive load of bus line (SBCL, SBDA)	Cb	*	*	pf

5. Applications

5.1 Timing

Preview mode is for preview size output (800x600),capture mode is for full size output(1600x1200), Suppose Vsync is low active and Hsync is high active, and ouput format is YCbCr/RGB565, then the timing of vsync and hsync is bellowing(preview mode is the same as capture mode , take capture mode for example):



Ft =VB+ Vt +8 （unit is row_time）

VB = Bt + St + Et， Vblank/Dummy line，setting by register 0x14 and 0x15.

Ft -> Frame time，one frame time

Bt -> Blank time，Vsync no active time.

St -> Start time，setting by register 0x20.

Et –> End time，setting by register 0x21.

Vt -> valid line time. UXGA is 1216，Vt=win_height-8，win_height is setting by register 0x1a 和 0x1b(capture mode)（1216）.

When exp_time <= win_height+VB，Bt=VB-St-Et。Frame rate is controlled by window_height+VB。

When exp_time > win_height+VB，Bt=exp_time-win_height-St-Et。Frame rate is controlled by exp_time。

The following is row_time calculate:

row_time = Hb + Sh_delay + win_width + 4.

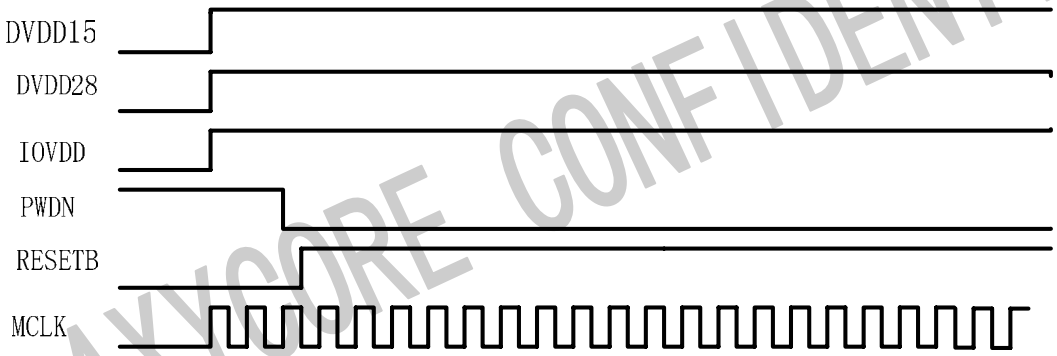
Hb –> HBlank or dummy pixel，Setting by register 0x12 and 0x13.

Sh_delay -> Setting by register 0x1e.

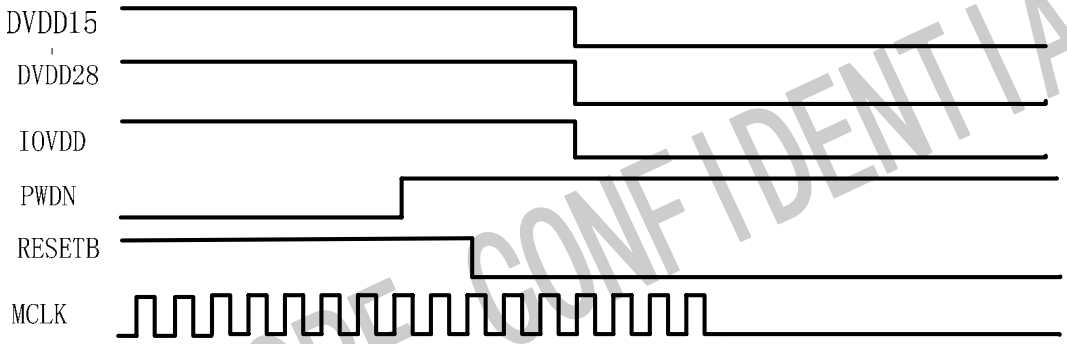
win_width -> Setting by register 0x0b and 0x0c, win_width = 1600, final_output_width +16(Preview mode, column binning is open). So for UXGA, we should set win_width as 1616.

5.2 Power on/off sequence

5.2.1 Power On Sequence



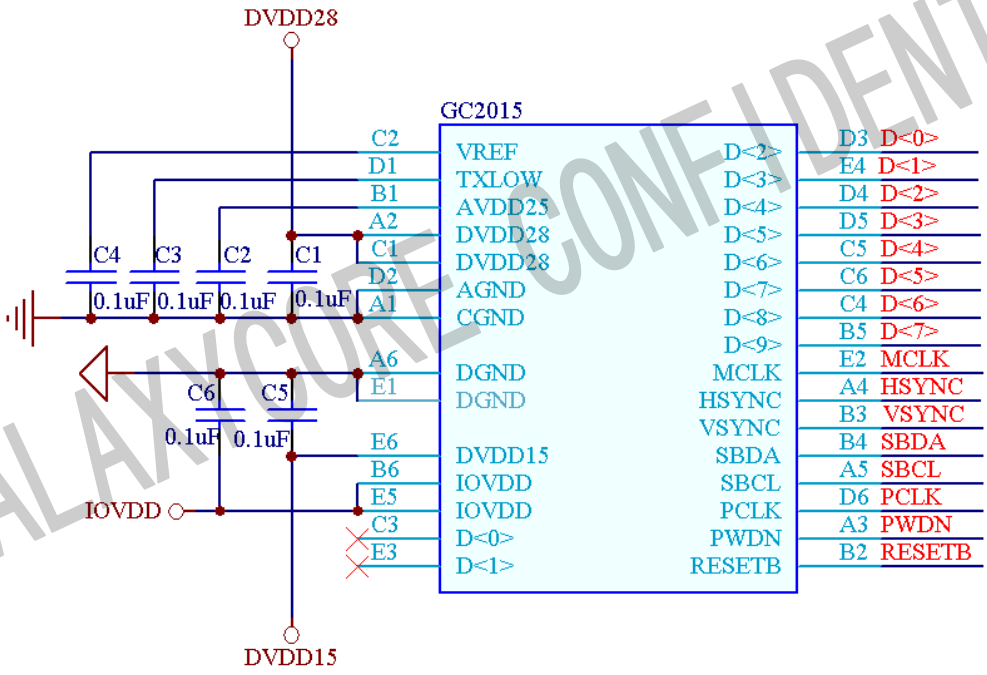
5.2.2 Power Off Sequence



5.3 DC characteristics (-20 ^{O}C < T_A <70^{O}C)

Symbol		Parameter	Min	Typ	Max	Unit
Supply						
V_{DVDD28}		Power supply	2.7	2.8	3.3	V
V_{DVDD15}		Supply voltage(digital core)	1.4	1.5	1.9	V
V_{IOVDD}		Supply voltage(digital I/O)	1.7	2.8	3.3	V
I_{DVDD28}		Active(operating) current		8	20	mA
I_{DVDD15}				12	20	mA
I_{IOVDD}	1.8V			4	10	mA
	2.8V			6	10	mA
I_{DDS_PWD}		Standby Current	10	20	60	uA
Digital Input(Typical conditions: DVDD = 2.8V,， DVDD = 1.5V ， IOVDD = 1.8V)						
V_{IH}		Input voltage HIGH	1.4			V
V_{IL}		Input voltage LOW			0.6	V
Digital Output(DVDD28 = 2.8V，standard Loading 25PF ， IOVDD = 1.8V)						
V_{OH}		Output voltage HIGH	1.6			V
V_{OL}		Output voltage LOW			0.2	V

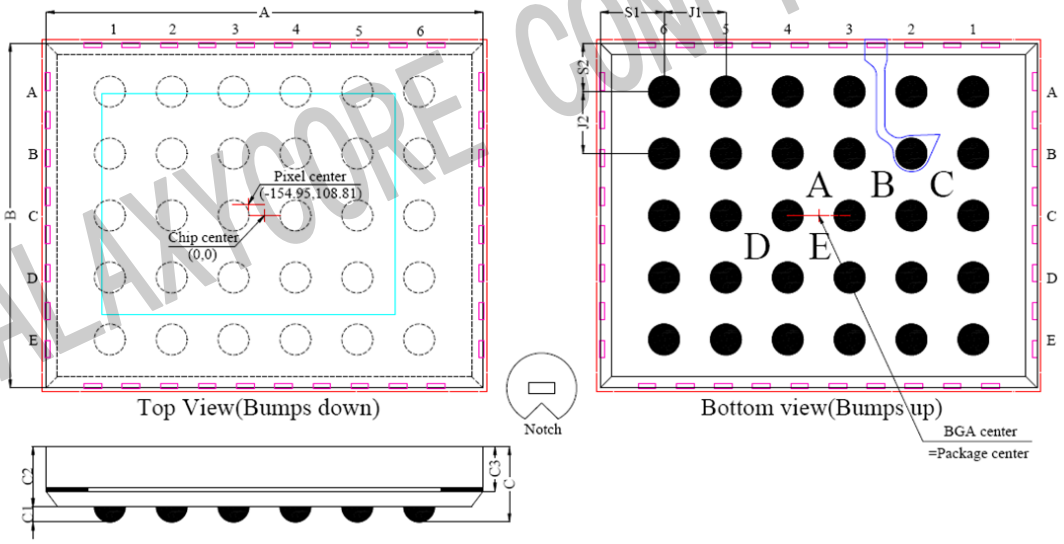
5.4 Reference of Application Circuit



*Recommended location of capacitor on PCB:

The capacitor of power supply should be wired to power supply PAD as short as possible.

6. Package specifications



Package dimensions

Description	Symbol	Nominal	Min.	Max.
		Millimeters		
Package Body Dimension X	A	4.240	4.215	4.265
Package Body Dimension Y	B	3.340	3.315	3.365
Package Height	C	0.800	0.740	0.860
Ball Height	C1	0.160	0.130	0.190
Package Body Thickness	C2	0.640	0.605	0.675
Thickness from top glass surface to wafer	C3	0.435	0.415	0.455
Ball Diameter	D	0.300	0.270	0.330
Total Ball Count	N	30		
Ball Count X axis	N1	6		
Ball Count Y axis	N2	5		
Pins Pitch X axis	J1	0.600		
Pins Pitch Y axis	J2	0.600		
Edge to Pin Center Distance along X	S1	0.620	0.590	0.650
Edge to Pin Center Distance along Y	S2	0.470	0.440	0.500

7. Register List

Analog & CISCTL

Address	Name	Width	Default Value	R/W	Description
P0:0x00	**Chip_ID_high**	**8**	**0x20**	**RO**	**Chip ID high**
P0:0x01	**Chip_ID_low**	**4**	**0x05**	**RO**	**Chip ID low**
P0:0x02	Preview_capture_mode	1	0x01	RW	[7:1] NA [0] preview or capture mode 1: Preview Mode(SVGA) 0: Capture Mode(UXGA)
P0:0x03	Exposure time high	4	0x01	RW	[7:5] NA [4:0] exposure time[12:8]，use line processing time as the unit.
P0:0x04	Exposure time low	8	0x00	RW	Exposure time [7:0], controlled by AEC if AEC is on
P0:0x05	Preview mode HB[11:8]	4	0x01	RW	[7:3] NA [3:0] Preview mode HB[11:8]
P0:0x06	Preview mode HB[7:0]	8	0xc1	RW	Preview mode HB[7:0]
P0:0x07	Preview mode	5	0x00	RW	Preview mode VB[12:8] , if current exposure

	VB[12:8]				< (Vb + window Height) , frame rate will be (Vb + window Height); otherwise frame rate will be determined by exposure time. [7:5] NA [4:0]Preview mode V-blank high bit [12:8]
P0:0x08	Preview mode VB[7:0]	8	0x40	RW	Preview mode VB[7:0]
P0:0x09	Pre_Row_start[10:8]	3	0x00	RW	[7:3] NA [2:0] Preview mode Row Start[10:8]
P0:0x0a	Pre_Row_start[7:0]	8	0x05	RW	Preview mode Row Start[7:0]
P0:0x0b	Pre_Col_start[10:8]	3	0x00	RW	[7:3] NA [2:0] Preview mode Column start[10:8]
P0:0x0c	Pre_Col_start[7:0]	8	0x08	RW	Preview mode Column start[7:0]
P0:0x0d	prev_win_height[10:8]	3	0x04	RW	[7:3] NA [2:0] preview Window height[10:8]
P0:0x0e	prev_win_height[7:0]	8	0xc0	RW	Preview Window height[7:0]
P0:0x0f	Pre_win_width[10:8]	2	0x06	RW	[7:2] NA [1:0] Preview Window width[10:8]
P0:0x10	Pre_win_width[7:0]	8	0x50	RW	Preview window width[7:0]
P0:0x11	Pre_sh_delay	8	0x52	RW	Preview mode sh_delay
P0:0x12	Capt_Hb[11:8]	4	0x01	RW	[7:4] NA [3:0] Capture Mode HB[11:8]
P0:0x13	Capt_Hb[7:0]	8	0x2a	RW	Capture Mode HB[7:0]
P0:0x14	Capt_VB[12:8]	5	0x00	RW	[7:5] NA [4:0] Capture Mode VB[12:8]
P0:0x15	Capt_VB[7:0]	8	0x68	RW	Capture Mode VB[7:0]
P0:0x16	Capt_Row_Start[10:8]	3	0x00	RW	[7:3] NA [2:0] Capture Mode Row Start[10:8]
P0:0x17	Capt_Row_Start[7:0]	8	0x05	RW	Capture Mode Row Start[7:0]
P0:0x18	Capt_Col_start[10:8]	3	0x00	RW	[7:3] NA [2:0] Capture Mode Column Start[10:8]
P0:0x19	Capt_Col_start[7:0]	8	0x0c	RW	Capture Mode Column Start[7:0]
P0:0x1a	Capt_Win_Height [10:8]	3	0x04	RW	[7:3] NA [2:0] Capture Mode Window Height[10:8]

P0:0x1b	Capt_Win_Height [7:0]	8	0xc0	RW	Capture Mode Window Height[7:0]
P0:0x1c	Capt_Win_Width[10:8]	3	0x06	RW	[7:3] NA [2:0] Capture Mode Window Width[10:8]
P0:0x1d	Capt_Win_Width[7:0]	8	0x50	RW	Capture Mode Window Width[7:0]
P0:0x1e	Capt_Sh_Delay	8	0x52	RW	Capture mode Sh_delay
P0:0x1f	NA	NA	NA	NA	NA
P0:0x20	Vs_st	8	0x08	RW	Vsync start time
P0:0x21	Vs_et	8	0x08	RW	Vsync end time
P0:0x22	Row_tail_width	4	0x00	RW	Row tail width
P0:0x23~0x27 NA					
P0:0x28	Db_row_en	8	0x00	RO	Controlled by AEC, when Low light disable ,user can write them [7:1] NA [0] db_row_en
P0:0x29	CISCTL_mode1	8	0X20	RW	[7] HSYNC always [6] Close 2 frame dbrow [5:4] CFA sequence [3:2] dark CFA sequence [1] Updown image [0] mirror image
P0:0x2a	CISCTL_mode2	8	0xca	RW	[7] Column Bin (default Preview) [6] Row evenskip (default Preview) [5] restg 1: on 0: off [4] reserved [3:2] sdark mode 00 sdark off, 01 every row sdark, 10 sdark 4 row in even frame, 11 sdark 4 row in each frame [1:0] exposure mode [1] new exposure/normal badframe [0] badframe enable
P0:0x2b	CISCTL_mode3	8	0x05	RW	[7:5] NA [4] Capture AD data edge [3:0] AD pipe number
P0:0x2c	CISCTL_mode4	8	0x00	RW	[7:6] Tx_mode [5] Coltest_en

					[4] ADtest_en [3:0] rowset_num
0x2d~0x2f NA					
P0:0x30	Rsh_width	4 4	0x22	RW	[7:4] restg_width, X2 [3:0] sh_width X2
P0:0x31	Tsp_width	5 2	0x0d	RW	[7:2] tx_width [1:0] space_width X2
P0:0x32	Analog_mode1	8	0x17	RW	[7:6]rsv1,rsv0 [5:4] Column bias 0 0: 3u 0 1: 5u(default) 1 0: 7u 1 1: 9u [3:2] comv_r 0 0: 0.52 0 1: 0.52 1 0: 0.9 1 1: 1.07 [1] clk_delay [0] apwd, 1 mean close analog circuit
P0:0x33	Analog_mode2	8	0x00	RW	[7]NA, [6]pgain [5:4]Output pad pull up/down mode 1 1: pull up 0 0: pull down 0 1： none 1 0： forbidden [3]txlow_en [2:0]txlow voltage 000 : -1.76V 001: -1.58V 010: -1.4V 011: -1.22V 100: -1.04V 101: -0.86V 110: -0.68V 111: -0.5V
P0:0x34	Hrst_rsg	8	0x48	RW	[7] hrst [6:4] da_rsg 0 0 0: 0.24 0 0 1: 0.38 0 1 0: 0.54

					0 1 1: 0.71 1 0 0: 0.88 1 0 1: 1.05 1 1 0: 1.22 1 1 1: 1.37 [3]txhigh_en [2:0]NA
P0:0x35	Vref A25	4 4	0xba	RW	[7] vref_en [6:4] da_vref 0 0 0: 3.06 0 0 1: 3.24 0 1 0: 3.41 0 1 1: 3.59 1 0 0: 3.77 1 0 1: 3.94 1 1 0: 4.12 1 1 1: 4.3 [3] da25_en [2]NA [1:0]da25_r 0 0: 2.6V 0 1: 2.44V 1 0: 2.52V 1 1: 2.36V
P0:0x36	ADC_r	8	0x01	RW	[7]NA [6:5]opa_r 0 0: 24uA 0 1: 21uA 1 0: 16uA 1 1: 14uA [4:2]NA [1:0]sRef 0 0: 1.36 0 1: 1.26 1 0: 1.16 1 1: 1.06
P0:0x37	PAD_drv	8	0x15	RW	[7:6] NA, [5:4] hsync/vsync driving current 0 0: 4mA 0 1: 8mA 1 0: 12mA 1 1: 16mA

					[3:2] data pins driving current 0 0: 2mA 0 1: 4mA 1 0: 8mA 1 1: 10mA [1:0] pclk pin driving current 0 0: 2mA 0 1: 4mA 1 0: 8mA 1 1: 10mA
P0:0x38	Analog_mode3	8	0x00	RW	[7:2] NA [1] rowclk_mode [0] adclk_mode
P0:0xfa	clk_div_mode	3	0x00	RW	[6:4]+1 represent the frequency division number [2:0] represent the high level in one pulse after frequency division Mclk by Div duty 0x11 2 1:1 0x21 3 1:2 0x22 3 2:1 0x31 4 1:3 0x32 4 2:2 0x33 4 3:1 … 0x76 8 6:2 0x77 8 7:1
P0:0xfe	Reset related	8	0x00	RW	[7] soft_reset [6:5] NA [4] CISCTL_restart_n, restart CISCTL, effective low [3:1] NA [0] page_select 0: registers in page0 1: registers in page1

ISP Related

Address	Name	Width	Default Value	R/W	Description
P0:0x40	Block_enable_1	8	0xff	RW	[7] BKS_en [6] gamma enable [5] CC enable [4] Edge enhancement enable [3] Interpolation enable [2] Noise removal enable [1] Defect removal enable [0] Lens-shading correction enable
P0:0x41	Block_enable_2	8	0xff	RW	[7] NA [6] NA [5] skin correction enable [4] CbCr_HUE_en [3] Y_as_en [2] autogray_en [1] Y_gamma_en [0] HSP_en
P0:0x42	AAAA_enable	8	0x00	RW	[7] Auto_SA_en [6] auto_EE [5] auto_DNDD [4] auto_LSC [3] NA [2] ABS enable [1] AWB enable [0] NA
P0:0x43	special_effect	8	0x00	RW	[7:3] NA [2] edge_map [1] CbCr fixed enable [0] Inverse color
P0:0x44	Output_format	8	0xa2	RW	[7] ISP high 8 or low 8 [6] shake mode, RGB565 dither [5] NA [4:0]output data mode 5'h00 Cb Y Cr Y 5'h01 Cr Y Cb Y 5'h02 Y Cb Y Cr 5'h03 Y Cr Y Cb 5'h06 RGB 565 5'h07 RGB x555 5'h08 RGB 555x

					5'h09 RGB x444 5'h0a RGB 444x 5'h0f bypass 10bits 5'h11 only Y 5'h12 only Cb 5'h13 only Cr 5'h14 only R 5'h15 only G 5'h16 only B 5'h17 switch odd/even column /row to controls output bayer pattern P1:0x53[6:5]: 0 0 RGBG 0 1 RGGB 10 BGGR 11 GBRG 5'h18 DNDD_out_mode, high 8 5'h19 LSC_out_mode, high 8
P0:0x45	output_en	4	0x00	RW	[3]data output enable [2]pclk output enable [1]hsync output enable [0]vsync output enable
P0:0x46	sync_mode	8	0x3f	RW	Synchronize signal output mode [7] data delay half [6] hsync delay half [5] allow pclk around hsync [4] allow pclk around vsync [3] opclk gated in HB 0: not gated 1: gated [2] opclk polarity 0: invert of isp_2pclk(isp_pclk) 1: same as isp_2pclk(isp_pclk) [1] hsync polarity 0: low valid 1: high valid [0] vsync polarity 0: low valid 1: high valid
P0:0x48	global_gain	8	0x48	RW	
P0:0x49	bypass_mode	8	0x83	RW	[7] allow_hsync_in_row_tail [6] single_2_double_mode

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					[5] first_second_switch [4] NA [3] is_8bit_bypass [2] is_10bit_bypass [1:0] bypass which 8bits from 11bit, in is_8bit_bypass mode 11: [10:3]----default 10: [9:2] 01: [8:1] 00: [7:0]
P0:0x4a	Clock_gating_en	8	0x81	RW	[7] ISP quiet mode， in SH time, clock ISP's AAA clock [6] NA [5] BCR_close_others [4] NA [3] NA [2] Divide gated clock enable [1] NA [0]NA
P0:0x4b	debug_mode1	8	0xe8	RW	[7:6] BFF gate mode [5] NA [4] hide 2 clk mode [3:2] pipe gate mode [1] AWB_gain_mode, 1: at PREGAIN 0: at POSTGAIN [0] more boundary mode
P0:0x4c	debug_mode2	8	0x00	RW	[7:5] NA [4] skin map [3] test image when in VGA, UXGA 1: UXGA 0: VGA [2] input test image [1] LSC test image [0] test image after EEINP
P0:0x4d	Debug_mode3	8	0x01	RW	[7:2] NA [1] INBF enable [0] update gain mode
P0:0x4e	Bayer_mode	8	0x89	RW	[7] hold after quiet mode [6] odd even row switch [5] odd even column switch [4:0] out count limit

P0:0x4f	AEC_EN	1	0x00	RW	[7:1] NA [0] AEC_en
P0:0x50	Crop_win_mode	1	0x00	RW	[7:1] NA [0] Crop out Window mode
P0:0x51	Crop_win_y1[11:8]	4	0x00	RW	[7:4] NA [3]: 0-> forward, 1-> backward 1: [3:0] is valid 0: [10:0] is valid [2:0]Crop _win_y1[10:8]
P0:0x52	Crop_win_y1[7:0]	8	0x00	RW	Crop _win_y1[7:0]
P0:0x53	Crop_win_x1[11:8]	4	0x00	RW	[7:4] NA [3]: 0-> forward, 1-> backward 1: [5:0] is valid 0: [10:0] is valid [2:0]Crop _win_y1[10:8]
P0:0x54	Crop_win_x1[7:0]	8	0x00	RW	Crop _win_x1[7:0]
P0:0x55	out_win_height[10:8]	3	0x02	RW	[7:3] NA [2:0]Out window height[10:8]
P0:0x56	out_win_height[7:0]	8	0x80	RW	Out window height[7:0]
P0:0x57	out_win_width[10:8]	3	0x01	RW	[7:3] NA [2:0]Out window width[10:8]
P0:0x58	out_win_width[7:0]	8	0xe0	RW	Out window width[7:0]
P0:0x59	subsample	8	0x11	RW	[7:4]subsample row ratio [3:0]subsample col ratio
P0:0x5a	sub_mode	6	0x07	RW	[5] use_or_cut_row [4] use_or_cut_col [3] smooth Y [2] smooth chroma [1] neighbor vag mode [0] subsample_extend_opclk
P0:0x5b	sub_row_N1	8	0x02	RW	[7:4] sub_row_num1 [3:0] sub_row_num2
P0:0x5c	sub_row_N2	8	0x04	RW	[7:4] sub_row_num3 [3:0] sub_row_num4
P0:0x5d	sub_row_N3	8	0x00	RW	[7:4] sub_row_num5 [3:0] sub_row_num6
P0:0x5e	sub_row_N4	8	0x00	RW	[7:4] sub_row_num7 [3:0] sub_row_num8
P0:0x5f	sub_col_N1	8	0x02	RW	[7:4] sub_col_num1 [3:0] sub_col_num2

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P0:0x60	sub_col_N2	8	0x04	RW	[7:4] sub_col_num3 [3:0] sub_col_num4
P0:0x61	sub_col_N3	8	0x00	RW	[7:4] sub_col_num5 [3:0] sub_col_num6
P0:0x62	sub_col_N4	8	0x00	RW	[7:4] sub_col_num7 [3:0] sub_col_num8

BLK

Address	Name	Width	Default Value	R/W	Description
P0:0x63	Blk_mode1	8	0x27	RW	[7] NA [6:4] BLK_smooth_speed, [3] NA [2] dark_current_mode 1 use exp_rated_darkc 0 use ndark_row calculated [1] dark_current_en [0] offset_en
P0:0x64	BLK_mode2	8	0x09	RW	[7:4] NA [3:0] BLK_row_select_mode
P0:0x65	BLK_limit_value	7	0x40	RW	low align 10bits
P0:0x66	global_offset	7	0x01	RW	low align 10bits
P0:0x67	current_R_offset	6	0x00	RO	[7:6] NA [5:0] Current_R_offset
P0:0x68	current_G_offset	6	0x00	RO	[7:6] NA [5:0] Current_G_offset
P0:0x69	current_B_offset	6	0x00	RO	[7:6] NA [5:0] current_B_offset
P0:0x6a	current_R_dark_current	6	0x00	RO	[7:6] NA [5:0] Current_R_dark_current
P0:0x6b	Current_G_dark_current	6	0x00	RO	[7:6] NA [5:0] Current_G_dark_current
P0:0x6c	current_B_dark_current	6	0x00	RW	[7:6] NA [5:0] Current_B_dark_current
P0:0x6d	Exp_rate_darkc	8	0x04	RW	Low 8 bits of 0.12, 4 means when exp =1024, dark current portion is 4
P0:0x6e	offset_submode offset_ratio_G	2 6	0x20	RW	[7:6]offset submode 00: channel will be adjusted respectively 01: adjusted by average of 4 channels 10: G and RB channel be adjusted separately

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					11: switch RB and G channel [5:0] offset ratio of G channel ,1.5 bits
P0:0x6f	darkc_submode dark_current_ratio_G	6	0x10	RW	[7:6] darkc submode 00: channel will be adjusted respectively 01: adjusted by average of 4 channels 10: G and RB channel be adjusted separately 11: switch RB and G channel [5:0] dark current ratio of G channel
P0:0x70	offset_ratio_RB	6	0x18	RW	[5:0] offset ratio of RB channel, 1.5bits
P0:0x71	dark_current_ratio_RB	6	0x18	RW	[5:0] dark current ratio of RB channel ,1.5 bits
P0:0x72	manual_G_offset	6	0x00	RW	S5, aligned to lower 8 of 11 bits data
P0:0x73	manual_R_offset	6	0x00	RW	S5, aligned to lower 8 of 11 bits data
P0:0x74	manual_B_offset	6	0x00	RW	S5, aligned to lower 8 of 11 bits data

PREGAIN

Address	Name	Width	Default Value	R/W	Description
P0:0x75	Auto_pregain	8	0x40	RO	Controlled by AEC , can be manually controlled when disable AEC
P0:0x76	Auto_postgain	8	0x40	RO	Controlled by AEC , can be manually controlled when disable AEC
P0:0x77	Channel_gain_R	8	0x80	RW	1.7 bits, G channel pre gain
P0:0x78	Channel_gain_G	8	0x80	RW	1.7 bits, R channel pre gain
P0:0x79	Channel_gain_B	8	0x90	RW	1.7 bits, B channel pre gain (for AWB's lgiht temperature mode, set slightly B_gain a little)
P0:0x7a	AWB_R_gain	8	0x50	RO	2.6 bits, red channel gain from auto white balancing
P0:0x7b	AWB_G_gain	8	0x40	RO	2.6 bits, green channel gain from auto white balancing
P0:0x7c	AWB_B_gain	8	0x80	RO	2.6 bits, blue channel gain from auto white balancing
P0:0x7d	R_ratio	8	0x80	RW	1.7 bits, R_ratio
P0:0x7e	G_ratio	8	0x80	RW	1.7 bits, G_ratio
P0:0x7f	B_ratio	8	0x80	RW	1.7 bits, B_ratio

LSC

Address	Name	Width	Default Value	R/W	Description

P1:0xb0	P_LSC_YCP_EN P_LSC_compens ate P_LSC_Sign_b4 C_LSC_pixel_arra y_select	 1 1 1 2	0x13	RW	[7:5] NA [4] P_LSC_YCP_EN [3]P_LSC_compensate [2] P_LSC_signed_b4 [1:0] P_LSC_pixel_array_select 00: center column and row range :0-512 ---------1600*1200 01: center column range: 200-712 Center row range :100-612 ----------800*600 10: center column range: 350-862 Center row range :200-712 ----------1280*800 11: center column range: 544-1056 Center row range :344-856 ----------1600*1200
P1:0xb1	P_LSC_red_b2	8	0x20	RW	Preview mode Square coefficient for R,G,B channel
P1:0xb2	P_LSC_green_b2	8	0x20	RW	
P1:0xb3	P_LSC_blue_b2	8	0x20	RW	
P1:0xb4	P_LSC_red_b4	8	0x20	RW	Preview mode Quadra coefficient for R,G,B channel
P1:0xb5	P_LSC_green_b4	8	0x20	RW	
P1:0xb6	P_LSC_blue_b4	8	0x20	RW	
P1:0xb7	P_LSC_compens ate_b2	8	0x20	RW	Preview mode compensate
P1:0xb8	P_LSC_row_cent er	8	0x80	RW	Preview mode LSC row center
P1:0xb9	P_LSC_col_cente r	8	0x80	RW	Preview mode LSC column center
P1:0xba	C_LSC_YCP_en C_LSC_compens ate C_LSC_signed_b 4 C_LSC_pixel_arra y_select	1 1 1 2	0x13	RW	[7:5] NA [4] C_LSC_YCP_EN [3]C_LSC_compensate [2] C_LSC_signed_b4 [1:0] C_LSC_pixel_array_select 00: center column and row range :0-512 ---------1600*1200 01: center column range: 200-712 Center row range :100-612 ----------800*600 10: center column range: 350-862 Center row range :200-712 ----------1280*800 11: center column range: 544-1056

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					Center row range :344-856 ----------1600*1200
P1:0xbb	C_LSC_red_b2	8	0x20	RW	Capture mode Square coefficient for R,G,B channel
P1:0xbc	C_LSC_green_b2	8	0x20	RW	
P1:0xbd	C_LSC_blue_b2	8	0x20	RW	
P1:0xbe	C_LSC_red_b4	8	0x20	RW	Capture mode Quadra coefficient for R,G,B channel
P1:0xbf	C_LSC_green_b4	8	0x20	RW	
P1:0xc0	C_LSC_blue_b4	8	0x20	RW	
P1:0xc1	C_LSC_compensate_b2	8	0x20	RW	Capture mode compensate
P1:0xc2	C_LSC_row_center	8	0x80	RW	Capture mode LSC row center
P1:0xc3	C_LSC_col_center	8	0x80	RW	Capture mode LSC column center
P1:0xc4	NA				

ASDE (auto saturation de-noise and edge enhancement)

Address	Name	Width	Default Value	R/W	Description
P0:0x98	ASDE_gain_high_th	8	0x20	RW	The gain threshold of auto_funtion for dark light.
P0:0x99	ASDE_gain_mode ASDE_DN_b_slope	4 4	0xf6	RW	[7:4]: ASDE_gain_mode [3]1: use_post_gain [2]1:use_pre_gain [1]1:use_global_gain [0]1:use_col_gain [3:0] ASDE_DN_b_slope
P0:0x9a	ASDE_DN_bilat_b	5	0x0c	RO	ASDE_DN_bilat_b
P0:0x9b	ASDE_DN_n_slope ASDE_DN_c_slope	4 4	0xea	RW	[7:4] ASDE_DN_n_slope [3:0] ASDE_DN_c_slope
P0:0x9c	ASDE_DN_bilat_n ASDE_DN_C_coeff[4:1]	4 4	0x08	RO	[7:4] ASDE_DN_bilat_n [3:0] ASDE_DN_C_coeff[4:1]
P0:0x9d	ASDE_DD_bright_th_slope ASDE_DD_limit_slope	4 4	0x5f	RW	[7:4] ASDE_DD_bright_th_slope [3:0] ASDE_DD_limit_slope

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P0:0x9e	ASDE_DD_bright_th ASDE_DD_limit	4 4	0x5f	RO	[7:4] ASDE_DD_bright_th [3:0] ASDE_DD_limit
P0:0x9f	ASDE_EE1_effect_slope ASDE_EE2_effect_slope	4 4	0x12	RW	[7:4] ASDE_EE1_effect_slope [3:0] ASDE_EE2_effect_slope
P0:0xa0	ASDE_edge1_effect ASDE_edge2_effect	4 4	0x48	RO	[7:4] ASDE_edge1_effect [3:0] ASDE_edge2_effect
P0:0xa1	ASDE_auto_saturation_dec_slope	8	0x10	RW	ASDE_auto_saturation_dec_slope
P0:0xa2	ASDE_auto_saturation_low_limit ASDE_sub_saturation_slope	4 4	0x31	RW	[7:4] ASDE_auto_saturation_low_limit [3:0] ASDE_sub_saturation_slope
P1:0xc5	T_ASDE_low_luma_value_th	8	0x20	RW	for decrease lsc's gain
P1:0xc6	T_ASDE_LSC_b2_slope	8	0x20	RW	T_ASDE_LSC_b2_slope
P1:0xc7	T_ASDE_LSC_b4_slope	8	0x20	RW	T_ASDE_LSC_b4_slope
P1:0xc8	T_ASDE_LSC_c2_slope	8	0x20	RW	T_ASDE_LSC_c2_slope
P1:0xc9	LSC_red_b2	8	0xd8	RO	LSC_red_b2
P1:0xca	LSC_red_b4	8	0xe3	RO	LSC_red_b4
P1:0xcb	LSC_compensate_b2	8	0xeb	RO	LSC_compensate_b2
P1:0xcc	AEC_luma_value[11:4]	8	0xf0	RO	AEC_luma_value[11:4]
P1:0xcd~cf		NA			

DNDD

Address	Name	Width	Default Value	R/W	Description
P0:0x80	DN_mode_en	8	0x07	RW	[7] DN_inc_or_dec [6:5] NA [4] zero_weight_mode [3] share mode

					1: R, G, B input matrix share the same pattern 0: RB uses rectangle pattern while G uses diamond pattern [2] c_weight_adap_mode 1: center weight changee dynamically according to noise 0: use fixed center weight [1] dn_lsc_mode 1: decrease noise removal extent according to LSC 0: use the same denoise strategy for the whole image [0] dn_b_mode 1: use adaptive b value in bilateral filter, max 63 0: use fixed b value in bilateral filter
P0:0x81	DN_mode_ratio	8	0x22	RW	[7:6] NA [5:4] C_weight_adaptive_ratio, decide the max distance between the center point and its neighbor points 0 0 uses [3:0]of the difference between max and min, or clamp to f 0 1 uses [4:1] of the difference between max and min, or clamp to f 0 1 uses [5:2] of the difference between max and min, or clamp to f 1 1 uses [6:3] of the difference between max and min [3:2] dn_lsc_ratio 0 0 use [5:3] of LSC gain or clamp to7 0 1 use [6:4] of LSC gain or clamp to 7 1 0 use [7: 5] of LSC gain or clamp to 7 1 1 use [8:6] of LSC gain [1:0] dn_b_mode_ratio controls the bilateral_b according to max distance. 0 0 use [5:0] as the max distance or clamp to 0x3f 0 1 use [6:1] as the max distance or clamp to 0x3f 1 0 use [7:2] as the max distance 1 1 use {1'b0, [7:3]} as the max distance

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P0:0x82	DN_bilat_b_base	5	0x0c	RW	[7:5] NA Fixed bilateral b value
P0:0x83	DN_bilat_n_base , DN_C_weight	4 4	0x05	RW	[7:4] Base noise level of each frame; in low light case, will add DN_n_incr as noise level of each frame [3:0] base center pixel weight, When in low light case, the weight will be modified as (C_base+pixel_plannar)*DN_Ccoeff
P0:0x84	DD_dark_bright_ TH	8	0xe5	RW	DD_dark_bright_TH
P0:0x85	DD_flat_TH	8	0x86	RW	//max-min/dd_ratio smaller DD_flat_TH [7:4] dd_th subtract one //max-min/dd_ratio smaller DD_flat_TH [3:0] dd_th subtract two
P0:0x86	DD_limit DD_ratio	4 2	0xf2	RW	[7:4] DD_limit, threshold of a defect pixel [3:2] NA [1:0] DD_ratio, controls the difference between bright and dark pixel 0 0 defect threshold use [3:0] of (max-min) or clamp to f 0 1 defect threshold use [4:1] of (max-min) or clamp to f 1 0 defect threshold use [5:2] of (max-min) or clamp to f 1 1 defect threshold use [6:3] of (max-min) or clamp to f
P0:0x87-89 NA					

INTPEE （Interpolation and Edge Enhancement）

Address	Name	Width	Default Value	R/W	Description
P0:0x8a	EEINTP mode 1	8	0x6c	RW	[7] NA [6] new edge mode (HP3 mode) [5] edge2 mode 1: use direct template in 3x3 high pass filter [4] HP mode [3] LP interpolation enable：enable low pass filter of the center pixel by the direction for interpolation [2] LP edge enable: enable low pass filter of

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					the center pixel before edge enhancement [1:0] LP edge mode 0 0 the least LP(1&8) 0 1 3&8 1 0 7&8 1 1 1&0
P0:0x8b	EEINTP mode 2	8	0x00	RW	[7] NA [6]NA [5] only 2 direction [4] fixed direction threshold [3] only defect map: show defect [2] map_dir: show current edge direction [1] anti shake mode [0] NA
P0:0x8c	Direction TH1	6	0x05	RW	[7:6]NA Lower Criteria for direction detection
P0:0x8d	Direction TH2	6	0x3f	RW	[7:6] NA Upper Criteria for direction detection
P0:0x8e	Diff_HV_TI_TH Direction diff TH	4 4	0x05	RW	[7:4] Diff_HV_TI_TH [3:0] Direction diff TH
P0:0x8f	Edge1 effect Edge2 effect	4 4	0x48	RW	[7:4] edge effect use 5x5 template, float 0.5 [3:0] edge effect use 3x3 template Controlled by user or ASDE
P0:0x90	Edge_pos_ratio Edge_neg_ratio	4 4	0x88	RW	[7:4] pos edge ratio , 1.3Bits [3:0] neg edge ratio , 1.3Bits
P0:0x91	Edge1_max Edge1_min	4 4	0x81	RW	[7:4] edge1 max [3:0] edge1 min
P0:0x92	Edge2_max Edge2_min	4 4	0x81	RW	[7:4] edge2 max [3:0] edge2 min
P0:0x93	Edge1_th Edge2_th	4 4	0x22	RW	[7:4] edge1 threshold [3:0] edge2 threshold
P0:0x94	Edge_pos_max Edge_neg_max	4 4	0xf8	RW	[7:4] Pos_edge_max [3:0] Neg_edge_max

ABB

Address	Name	Bit	default	R/W	Description
P0:0xa5	ABB mode	8	0x31	RW	[6:4] row_select, [0] ABB_en
P0:0xa6	ABB target average	8	0x05	RW	S7, black stretch target average, allow negative target value

P0:0xa7	ABB range	8	0x33	RW	[7:4] big range, x4, for points that are far from target [3:0] small range, for points that are close to target
P0:0xa8	ABB limit value	7	0x20	RW	[7] NA [6:0] black point criteria that neither blooming points nor defect points will be counted.
P0:0xa9	ABB speed	8	0x22	RW	[7] NA [6:4] fast speed [3] NA [2:0] IIR smooth speed
P0:0xaa	Current R black level	7	0x04	RO	[7] NA [6:0] channel black level aligns to lower 7 bit of 10 bit input data, controlled by ABB or user
P0:0xab	Current G black level	7	0x04	RO	
P0:0xac	Current B black level	7	0x04	RO	
P0:0xad	Current R black factor	8	0x04	RO	Used to fine tune R black value,Lower 8 of 10,controlled by ABB or user
P0:0xae	Current G black factor	8	0x04	RO	
P0:0xaf	Current G black factor	8	0x04	RO	

CC

Address	Name	Width	Default Value	R/W	Description
P0:0xb0	CC Matrix C11	8	0x44	RW	R channel coefficient 1, S1.6
P0:0xb1	CC Matrix C12	8	0xfe	RW	R channel coefficient 2, S1.6
P0:0xb2	CC Matrix C13	8	0xfe	RW	R channel coefficient 3, S1.6
P0:0xb3	CC Matrix C21	8	0xfe	RW	G channel coefficient 1, S1.6
P0:0xb4	CC Matrix C22	8	0x44	RW	G channel coefficient 2, S1.6
P0:0xb5	CC Matrix C23	8	0xfe	RW	G channel coefficient 3, S1.6
P0:0xb6	CC Matrix C41	5	0x00	RW	R channel offset coefficient, S4
P0:0xb7	CC Matrix C42	5	0x00	RW	G channel offset coefficient, S4
P0:0xb8	CC Matrix C43	5	0x00	RW	B channel offset coefficient, S4

GAMMA

Address	Name	Width	Default Value	R/W	Description
P0:0xbf	Gamma_out0	8	0x10	RO	Each out value of knee_i.

					Knee0=0
P0:0xc0	Gamma_out1	8	0x20	RO	Knee1=8
P0:0xc1	Gamma_out2	8	0x38	RO	Knee2=16
P0:0xc2	Gamma_out3	8	0x4E	RO	Knee3=24
P0:0xc3	Gamma_out4	8	0x63	RO	Knee4=32
P0:0xc4	Gamma_out5	8	0x76	RO	Knee5=40
P0:0xc5	Gamma_out6	8	0x87	RO	Knee6=48
P0:0xc6	Gamma_out7	8	0xa2	RO	Knee7=64
P0:0xc7	Gamma_out8	8	0xb8	RO	Knee8=80
P0:0xc8	Gamma_out9	8	0xca	RO	Knee9=96
P0:0xc9	Gamma_out10	8	0xd8	RO	Knee10=112
P0:0xca	Gamma_out11	8	0xe3	RO	Knee11=128
P0:0xcb	Gamma_out12	8	0xe9b	RO	Knee12=144
P0:0xcc	Gamma_out13	8	0xf0	RO	Knee13 =160
P0:0xcd	Gamma_out14	8	0xf8	RO	Knee14 = 192
P0:0xce	Gamma_out15	8	0xfd	RO	Knee15 = 224
P0:0xcf	Gamma_out16	8	0xff	RO	Knee16 = 256

YCP

Address	Name	Width	Default Value	R/W	Description
P0:0xd0	Global saturation	8	0x40	RW	Global saturation, controlled by auto_saturation
P0:0xd1	saturation_Cb	8	0x30	RW	Cb saturation 3.5bits, 0x20=1.0
P0:0xd2	saturation_Cr	8	0x30	RW	Cr saturation 3.5bits, 0x20=1.0
P0:0xd3	luma_contrast	8	0x40	RW	Luma_contrast, can be adjusted via contrast center 2.6bits, 0x40=1.0
P0:0xd4	Contrast center	8	0x80	RW	Contrast center value
P0:0xd5	Luma_offset	8	0x00	RW	Add offset on luma value. S7.
P0:0xd6	skin_Cb_center	8	0xe8	RW	Cb criteria for skin detection.
P0:0xd7	skin_Cr_center	4	0x18	RW	Cr criteria for skin detection.
P0:0xd8	Skin radius square	8	0x28	RW	Defines skin range
P0:0xd9	Skin brightness high Skin brightness low	4 4	0xe3	RW	[7:4] skin brightness high threshold [3:0] skin brightness low threshold
P0:0xda	Fixed_Cb	8	0x00	RW	S7, if fixed CbCr function is enabled, current image Cb value will be replace by this value

					to achieve special effect
P0:0xdb	Fixed_Cr	8	0x00	RW	S7, if fixed CbCr function is enabled, current image Cr value will be replace by this value to achieve special effect
P0:0xdc	NA				
P0:0xdd	Edge_dec_sa_en Edge_dec_sa_slope	3 4	0x38	RW	[7] NA [6:4] edge_dec_sa_en [3:0] edge_dec_sa_slope
P0:0xde	auto-gray mode Sa_autogray	2 4	0x36		[7:6] NA [5:4] provide 4 modes to decrease saturation, (corner1, corner2) 0 0 (4,8) 0 1 (4, 12) 1 0 (4, 20) 1 1 (8, 16) [3:0] sa_autogray, proposed gray slope in Cb, Cr domain
P0:0xdf	Saturation_sub_strength	8	0x00	RO	Chroma offset in low light
P0:0xe0	Y_Gamma_out0	8	0x00	RW	Knee0=0
P0:0xe1	Y_Gamma_out1	8	0x10	RW	Knee1=8
P0:0xe2	Y_Gamma_out2	8	0x1c	RW	Knee2=16
P0:0xe3	Y_Gamma_out3	8	0x30	RW	Knee3=32
P0:0xe4	Y_Gamma_out4	8	0x43	RW	Knee4=48
P0:0xe5	Y_Gamma_out5	8	0x54	RW	Knee5=64
P0:0xe6	Y_Gamma_out6	8	0x65	RW	Knee6=80
P0:0xe7	Y_Gamma_out7	8	0x75	RW	Knee7=96
P0:0xe8	Y_Gamma_out8	8	0x93	RW	Knee8=128
P0:0xe9	Y_Gamma_out9	8	0xb0	RW	Knee9=160
P0:0xea	Y_Gamma_out10	8	0xcb	RW	Knee10=192
P0:0xeb	Y_Gamma_out11	8	0xe6	RW	Knee11=224
P0:0xec	Y_Gamma_out12	8	0xff	RW	Knee12=255

AEC

Address	Name	Width	Default Value	R/W	Description
P1:0x10	AEC_mode1	8	0xca	RW	[7] low_light_mode [6] measure_point [5] exp_mode, [4:2] gain_mode [1:0] skip_mode

					0:2X2 1:4x4 10 4x8 11 8x8
P1:0x11	AEC_mode2	8	0x21	RW	[7] fix target [6:4] AEC take action every N frame [3:2] close frame number to eliminate bad frame [1] change exp_gain_mode: only effect when exp change 2 steps(up or down) [0] dead_zone_mode: 1: AEC sto*p margin* use smaller margin 0: AEC converging mode use two criteria
P1:0x12	AEC_mode3	8	0x00	RW	[7] AEC_enable [6] map measure point [5] color Y mode [4] skin weight mode [3] NA [2] color select [1:0] column max gain select 00: column gain maximum can use 4 levels 01: column gain maximum can use 5 levels 10: column gain maximum can use 6 levels 11: column gain maximum can use 7 levels
P1:0x13	AEC_target_Y	8	0x50	RW	expected luminance value
P1:0x14	Y_average	8	0x00	RO	Current frame luma average
P1:0x15	AEC_high_low_range	8	0xf2	RW	[7:4] x16, count limit for high luminance pixels [3:0] x4, count limit for low luminance pixels
P1:0x16	AEC_number_limit_high_range	5	0x35	RW	AEC number limit high range
P1:0x17	AEC_ignore	8	0x18		[4] AEC_ignore_enable [3:0] AEC ignore number
P1:0x18	AEC_skin_offset AEC_R_offset	4 4	0x88	RW	[7:4] AEC_skin_offset [3:0] AEC_R_offset
P1:0x19	AEC_G_offset AEC_B_offset	4 4	0x88	RW	[7:4] AEC_G_offset [3:0] AEC_B_offset

P1:0x1a	AEC_slow_margin AEC_slow_speed	4 3	0x91	RW	[7:4] AEC slow margin, X4 [3] NA [2:0] AEC slow speed
P1:0x1b	AEC_fast_margin AEC_fast_speed	4 3	0x96	RW	[7:4] AEC fast margin, X4 [3] NA [2:0] AEC fast speed
P1:0x1c	AEC_exp_change_gain_ratio	8	0x96	RW	Gain change criteria, float 1.7, default use 1.2x
P1:0x1d	AEC_step2_sunlight	8	0x02	RW	AEC_step2_sunlight
P1:0x1e	AEC_I_frames AEC_D_ratio	2 4	0x33	RW	[7:6] NA [5:4] mode for Y difference selection 0 0 / 0 1 use last two frame difference 1 0 use last three frame difference 1 1 use last 4 frame difference [3:0] differential coefficient in AEC control algorithm
P1:0x1f	AEC_I_stop_L_margin	7	0x07	RW	[7] NA [6:0] x2, Will be used as AEC convergence margin when P0:0xd1[0]=0
P1:0x20	AEC_I_stop_margin AEC_I_ratio	4 4	0x61	RW	[7:4] AEC adjust stop margin [3:0] integration coefficient
P1:0x21	AEC_max_pose_dg_gain	8	0xc0	RW	Digital post gain limit, float 2.6 ,X3
P1:0x22	AEC_max_pre_dg_gain	8	0x60	RW	Digital pre gain limit, float 2.6, X1.5
P1:0x23	AEC_low_light_exp_THD_max[12:8]	5	0x0a	RW	AEC Low light mode exposure threshold maximum
P1:0x24	AEC_low_light_exp_THD_max[7:0]	8	0x50	RW	
P1:0x25	AEC_low_light_exp_THD_min[12:8]	5	0x09	RW	AEC Low light mode exposure threshold minimum
P1:0x26	AEC_low_light_exp_THD_min[7:0]	8	0x60	RW	
P1:0x27	AEC_low_light_gain_High	8	0x40	RW	3.5bits

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P1:0x28	AEC_low_light_gain_Low	8	0x20	RW	3.5bits
P1:0x29	P_N_AEC_anti_flicker_step[12:8]	5	0x01	RW	Preview,normal mode flicker step
P1:0x2a	P_N_AEC_anti_flicker_step[7:0]	8	0x00	RW	
P1:0x2b	P_N_AEC_exp_level_1[12:8]	5	0x05	RW	Preview,normal mode Exposure level 1
P1:0x2c	P_N_AEC_exp_level_1[7:0]	8	0x00	RW	
P1:0x2d	P_N_AEC_exp_level_2[12:8]	5	0x08	RW	Preview,normal mode Exposure level 2
P1:0x2e	P_N_AEC_exp_level_2[7:0]	8	0x00	RW	
P1:0x2f	P_AEC_exp_level_3[12:8]	5	0x09	RW	Preview,normal mode Exposure level 3
P1:0x30	P_AEC_exp_level_3[7:0]	8	0x00	RW	
P1:0x31	P_AEC_exp_level_4[12:8]	5	0x16	RW	Preview,normal mode Exposure level 4
P1:0x32	P_AEC_exp_level_4[7:0]	8	0x00	RW	
P1:0x33	P_N_AEC_max_exp_level AEC_exp_min_l[12:8]	8	0x60	RW	Preview,normal mode [6:5]max exposure levels can be applied by AEC [4:0]minimum exposure level high 5 bits
P1:0x34	AEC_exp_min_l[7:0]	8	0x04	RW	Preview,normal mode minimum exposure level low 8 bits
P1:0x35	P_L_AEC_anti_flicker_step[12:8]	5	0x00	RW	Preview,low light mode Anti flicker step
P1:0x36	P_L_AEC_anti_flicker_step[7:0]	8	0x80	RW	
P1:0x37	P_L_AEC_exp_level_1[12:8]	5	0x05	RW	Preview,low light mode Exposure level 1
P1:0x38	P_L_AEC_exp_level_1[7:0]	8	0x00	RW	
P1:0x39	P_L_AEC_exp_level_2[12:8]	5	0x0a	RW	Preview,low light mode Exposure level 2
P1:0x3a	P_L_AEC_exp_level_2[7:0]	8	0x00	RW	
P1:0x3b	P_L_AEC_max_exp_level	8	0x01	RW	Preview,low light mode

P1:0x3c	C_N_AEC_anti_flicker_step[12:8]	5	0x00	RW	Capture,normal mode Anti flicker step
P1:0x3d	C_N_AEC_anti_flicker_step[7:0]	8	0x78	RW	
P1:0x3e	C_N_AEC_exp_level_1[12:8]	5	0x05	RW	Capture,normal mode Exposure level 1
P1:0x3f	C_N_AEC_exp_level_1[7:0]	8	0x28	RW	
P1:0x40	C_N_AEC_exp_level_2[12:8]	5	0x06	RW	Capture,normal mode Exposure level 2
P1:0x41	C_N_AEC_exp_level_2[7:0]	8	0x90	RW	
P1:0x42	C_AEC_exp_level_3[12:8]	5	0x09	RW	Capture,normal mode Exposure level 3
P1:0x43	C_AEC_exp_level_3[7:0]	8	0x60	RW	
P1:0x44	C_AEC_exp_level_4[12:8]	5	0x0b	RW	Capture,normal mode Exposure level 1
P1:0x45	C_AEC_exp_level_4[7:0]	8	0xb8	RW	
P1:0x46	C_N_AEC_max_exp_level	8	0x03	RW	Capture,normal mode
P1:0x47	C_L_AEC_anti_flicker_step[12:8]	5	0x00	RW	Capture,low light mode Anti flicker step
P1:0x48	C_L_AEC_anti_flicker_step[7:0]	8	0x3c	RW	
P1:0x49	C_L_AEC_exp_level_1[12:8]	5	0x05	RW	Capture,low light mode Exposure level 1
P1:0x4a	C_L_AEC_exp_level_1[7:0]	8	0x28	RW	
P1:0x4b	C_L_AEC_exp_level_2[12:8]	5	0x07	RW	Capture,low light mode Exposure level 2
P1:0x4c	C_L_AEC_exp_level_2[7:0]	8	0x80	RW	
P1:0x4d	C_L_AEC_max_exp_level	8	0x01	RW	Capture,low light mode max exposure levels can be applied by AEC
P1:0x4e	Y_accelerate_th	8	0x20	RW	Parameter for AEC.

ABS

Address	Name	Width	Default	R/W	Description

			Value		
P1:0x80	ABS_range_compesate ABS_skip_frame	4 3	0xf 0x3	RW	[7:4] X4+3, add "more range" to enlarge more stretch [3] NA [2:0] Set number of frames to be skipped in ABS adjustment
P1:0x81	ABS_stop_margin	4	0x2	RW	[7:4] NA [3:0] margin for ABS to stop adjustment
P1:0x82	Y_S_compesate ABS_manual_K	4 4	0x00	RW	[7:4] Y_S_compesate [3:0] manual ABS slope adjustment, default 0
P1:0x83	Y_stretch_limit	8	0x20	RW	[7:0] Y_stretch limit
P1:0x84	Y_tilt	8	0xc0	RO	[7:0] the corner point, stretch Y if less than it
P1:0x85	Y_stretch_K	8	0x40	RO	[7:0] the slope ABS calculated for Y less than Y_tilt, 2.6bits

Measure Window

Address	Name	Width	Default Value	R/W	Description
P1:0x06	P_big_win_x0	8	0x04	RW	Used in preview frame
P1:0x07	P_big_win_y0	8	0x02	RW	
P1:0x08	P_big_win_x1	8	0x65	RW	
P1:0x09	P_big_win_y1	8	0x4b	RW	
P1:0x0a	C_big_win_x0	8	0x04	RW	Used in capture frame
P1:0x0b	C_big_win_y0	8	0x02	RW	
P1:0x0c	C_big_win_x1	8	0xca	RW	
P1:0x0d	C_big_win_y1	8	0x9	RW	

OUT Module

Address	Name	Width	Default Value	R/W	Description
P1:0x00	Close_frame_en Close_frame_num	1 4	0x00	RW	[7:5] NA [4] close frame function enable, close output Vsync to control frame rate [3:0] frames to be closed should be selected from this pool
P1:0x01	Close_frame_num1	8	0x00	RW	These two registers is a combi of four 4bit registers, they defines up to any 4 frames to be closed
P1:0x02	Close_frame_nu	8	0x00	RW	

	m2				
P1:0x03	Pad_test_valid[11:8] Pad_test_data[11:8]	4 4	0x00	RW	To test pad driver current When the bit of pad_test_valid is set, the corresponding pad is set as the the corresponding bit of pad_test_data Note: {vsync, hsync, data[9:0]} -> pad_test_valid
P1:0x04	Pad_test_valid[7:0]	8	0x00	RW	
P1:0x05	Pad_test_data[7:0]	8	0x00	RW	
P0:0x4e	Bayer_mode	8	0x89	RW	[7] opclk gated enable in subsample [6] odd even row switch [5] odd even column switch [4:0] pixel count limit to extend row in tail, do NOT less than 2
P1:0x86	EEINTP_HP_acc_height	1	0x03	RW	EEINTP_HP_acc_height high bit[8]
P1:0x87	EEINTP_HP_acc_height	8	0x40	RW	EEINTP_HP_acc_height high bit[7:0]
P1:0x88	EEINTP_HP_acc_sum [31:24]	8	0x00	RO	EEINTP_HP_acc_sum [31:24]
P1:0x89	EEINTP_HP_acc_sum[23:16]	8	0x00	RO	EEINTP_HP_acc_sum[23:16]
P1:0x8a	EEINTP_HP_acc_sum[15:8]	8	0x00	RO	EEINTP_HP_acc_sum[15:8]
P1:0x8b	EEINTP_HP_acc_sum[7:0]	8	0x00	RO	EEINTP_HP_acc_sum[7:0]

AWB

Address	Name	Width	Default Value	R/W	Description
P1:0x50	AWB_RGB_high_low	8	0xf5	RW	Defines the RGB range of gray pixel to be selected
P1:0x51	AWB_Y_to_C_diff2	8	0x18	RW	Gray pixel criteria
P1:0x52	AWB_C_max	8	0x10	RW	Chroma limit
P1:0x53	AWB_C_inter	8	0x22	RW	Slope of interested zone upper bond
P1:0x54	AWB_C_inter2	8	0x40	RW	Slope of interested zone lower bond
P1:0x55	AWB_C_max_big	8	0x60	RW	Chroma limit when big_c mode enable

P1:0x56	AWB_Y_high	8	0x40	RW	Give high luminance point more weight
P1:0x57	AWB_number_limit	8	0x90	RW	Number limit
P1:0x58	Kwin_ratio Sel_point AWB_auto_window Skip_mode	3 1 1 2	0x6 0 0 0	RW	[7] NA Kwin_ratio, criteria to validate small blocks to be used in AWB calculation [6] block threshold selection 1: use maximum threshold 0: use threshold defined by [5:4], default [5:4] small blocks validation criteria 0 0: threshold level 1, 1.5x, default 0 1: threshold level 2, 2.0x 1 0: threshold level 3, 2.5x 1 1: threshold level 4, 3.0x [3] NA [2] AWB sample location 0 : before gamma 1: after gamma [1:0]AWB skip mode 00: 2x2 01: 4x4 10: 4x8 11: 8x8
P1:0x59	Kwin_thd	5	0x6	RW	[7:5]NA [4:0]Low limit of block's min distance diff from last one each
P1:0x5a	Light_gain_range	8	0x30	RW	Defines gain range in R/B gain domain
P1:0x5b	move_TH move_number_limit	4 4	0x4 0x2	RW	Parameter for AWB.
P1:0x5c	show_and_mode	8	0x0f	RW	
P1:0x5d	adjust_speed adjust_margin	4 4	0x42	RW	[7:4] adjust speed [3:0] adjust margin
P1:0x5e	every_N light_temp_mode	2 4	0x21	RW	[7:6] NA [5:4] Number of frames for AEC operation [3] FIR filter enable [2] filter mode 1: 4 filter mode 2: 2 filter mode

					[1] NA [0] Light temp mode enable
P1:0x5f	R_5k_gain	8	0x40	RW	Parameter for AWB.
P1:0x60	B_5k_gain	8	0x40	RW	Parameter for AWB.
P1:0x61	AWB_sinT	8	0xc2	RW	Parameter for AWB.
P1:0x62	AWB_cosT	8	0xa6	RW	Parameter for AWB.
P1:0x63	AWB_X1_cut	8	0x20	RW	Parameter for AWB.
P1:0x64	AWB_X2_cut	8	0x4b	RW	Parameter for AWB.
P1:0x65	AWB_Y1_cut	8	0xb0	RW	Parameter for AWB.
P1:0x66	AWB_Y2_cut	8	0xea	RW	Parameter for AWB.
P1:0x67	AWB_R_gain_limit	8	0x70	RW	AWB_R_gain_limit
P1:0x68	AWB_G_gain_limit	8	0x58	RW	AWB_G_gain_limit
P1:0x69	AWB_B_gain_limit	8	0x78	RW	AWB_B_gain_limit
P1:0x6a	AWB_small_win_width_step	8	0x61	RO	AWB_small_win_width_step
P1:0x6b	AWB_small_win_height_step	8	0x48	RO	AWB_small_win_height_step
P1:0x6c	AWB_A_R2G_set_L	8	0x45	RW	Parameter for AWB.
P1:0x6d	AWB_A_R2G_set_H	8	0x58	RW	Parameter for AWB.
P1:0x6e	AWB_A_B2G_set_L	8	0x30	RW	Parameter for AWB.
P1:0x6f	AWB_A_B2G_set_H	8	0x3d	RW	Parameter for AWB.
P1:0x70	AWB_A_G_set_L	8	0x20	RW	Parameter for AWB.
P1:0x71	AWB_A_G_set_H	8	0x50	RW	Parameter for AWB.
P1:0x72	AWB_Yellow_R2G_set	8	0x60	RW	Parameter for AWB.
P1:0x73	AWB_Yellow_B2G_set	8	0x20	RW	Parameter for AWB.
P1:0x74	AWB_Yellow_G_set	8	0x30	RW	Parameter for AWB.
P1:0x75	AWB_CT_change_THD	7	0x20	RW	Parameter for AWB.
P1:0x76	R_avg_use	8	0x40	RO	Current R gain

P1:0x77	G_avg_use	8	0x40	RO	Current G gain
P1:0x78	B_avg_use	8	0x40	RO	Current B gain
P1:0x79	R_light_gain	8	0x60	RO	R_light_gain
P1:0x7a	B_light_gain	8	0x60	RO	B_light_gain

8. Revision history

Version1.0 2011.01.26

- Document release

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