SAMSUNG ELECTRONICS

DATA SHEET

S5K5BAF

1/5” 2MP CMOS Image Sensor SoC with an Embedded Image Processor

March 2009

Revision 0.07

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S5K5BAF 1/5” 2MP CMOS Image Sensor
SoC with an Embedded Image Processor

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Samsung Electronics Co., Ltd.
San #24 Nongseo-Dong, Giheung-Gu
Yongin-City, Gyeonggi-Do, Korea
C.P.O. Box #37, Suwon 446-711

TEL: (82)-(31)-209-8763
FAX: (82)-(31)-209-5324
E-mail: junghee@samsung.com

Home Page: http://www.samsungsemi.com
Printed in the Republic of Korea

Revision History

Revision	Date	Amendment
R0.00	19-Aug-08	Initial draft
R0.01	13-Oct-08	Function description modify.
R0.02	05-Dec-08	Pin description modify.
R0.03	08-Jan-09	TBD item modify.
R0.04	20-Feb-09	Typo error modify.
R0.05	18-Mar-09	Register map modify.
R0.06	18-June-09	Typo error modify.
R0.07	10-Aug-09	Typo error modify

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1 OVERVIEW

The S5K5BAF is a highly integrated 2-megapixel camera chip that includes CMOS image sensor, image processor and both 8-bit ITU-R 656/601 parallel interface and MIPI CSI2 compliant serial interface. It is fabricated using SAMSUNG 0.13μm CMOS image sensor process developed for imaging application to realize high-efficiency and low-power photo sensor.

The CMOS image sensor consists of 1616x1216 Active Pixel Sensor (APS) array which has 1/5 inch optical format, on-chip 10-bit ADC array to digitize the analog pixel output, and on-chip Correlated Double Sampling (CDS) to reduce Fixed Pattern Noise (FPN) drastically.

The image processor performs sophisticated image processing functions including color recovery and correction, false color suppression, lens shading correction, noise removal, edge enhancesment, programmable gamma correction, image down scaling, auto defect correction, auto dark level compensation, auto flicker correction (50/60Hz), auto exposure (AE), auto white balance (AWB). The F/W performs auto functions on embedded RISC processor. The host controller is able to access and control this device via general IIC bus.

2 KEY FEATURES

2.1 IMAGE SENSOR

- Optical format: 1/5 inch
- Unit pixel size: 1.75um
- Effective resolution: 1600 (H) x 1200 (V)
- Active resolurion: 1616 (H) x 1216 (V)
- Color filter: RGB Bayer pattern
- Shutter type: Electronic rolling shutter
- Max. capture frame rate: 15fps @full resolution
- Max. video frame rate: 30fps @VGA
- Max. pixel clock Frequency: 70MHz
- Max. pixel rate: 35Mp/s
- ADC accuracy: 10-bit
- Progressive scan readout
- Window panning & cropping
- Vertical flip and horizontal mirror mode
- Continuous and single frame capture mode
- Frame rate control
- LED and flash strobe mode
- Parallel output format: ITU-R. 656/ 601 YUV422, RGB888/ RGB565, RAW10
- Serial output format: MIPI CSI2 (single lane) YUV422, RGB888/ RGB565, RAW10

2.2 IMAGE PROCESSOR

- Color recovery and correction
- False color suppression
- Lens shading correction
- Noise removal
- Edge enhancement
- SXGA or any size smaller than SXGA down scaling
- Programmable gamma correction
- Auto defect correction
- Auto dark level compensation
- Auto flicker correction (50/60Hz)
- Auto exposure (AE)
- Auto white balance (AWB)
- Built-in test image generation

2.3 DEVICE

- Host control interface: I^2C bus
- Internal PLL (6MHz to 27MHz input frequency)
- Stand-by mode for power saving
- Operating temperature: -20°C to +60°C
- Supply voltage: 2.8V for analog, 1.5V for digital core (with internal regulator off), 1.8V - 2.8V for I/O
- 1.8V to 1.5V internal regulator

3 LOGICAL SYMBOL DIAGRAM

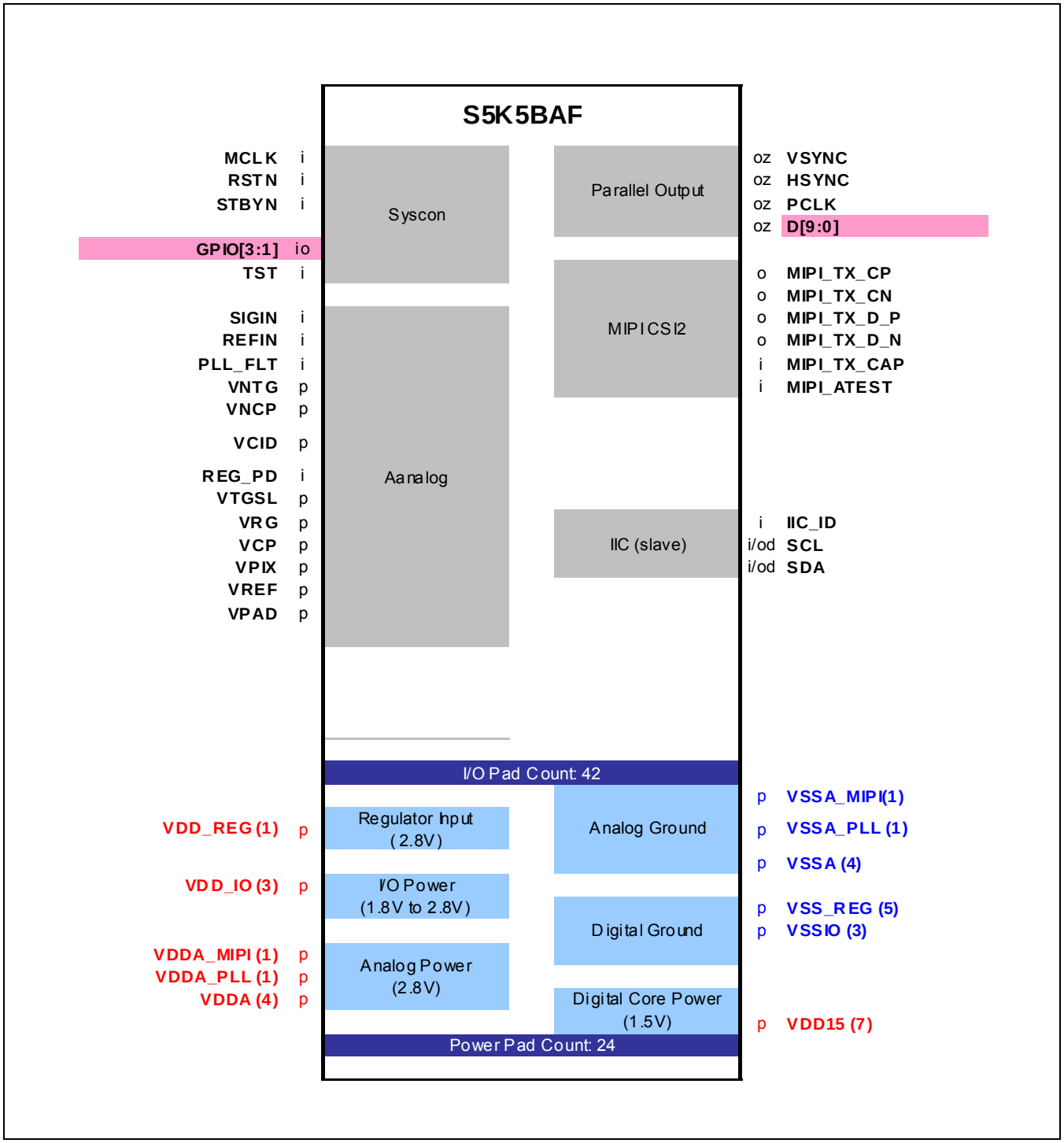


Figure 1. Logical Symbol Diagram

4 PAD CONFIGURATION

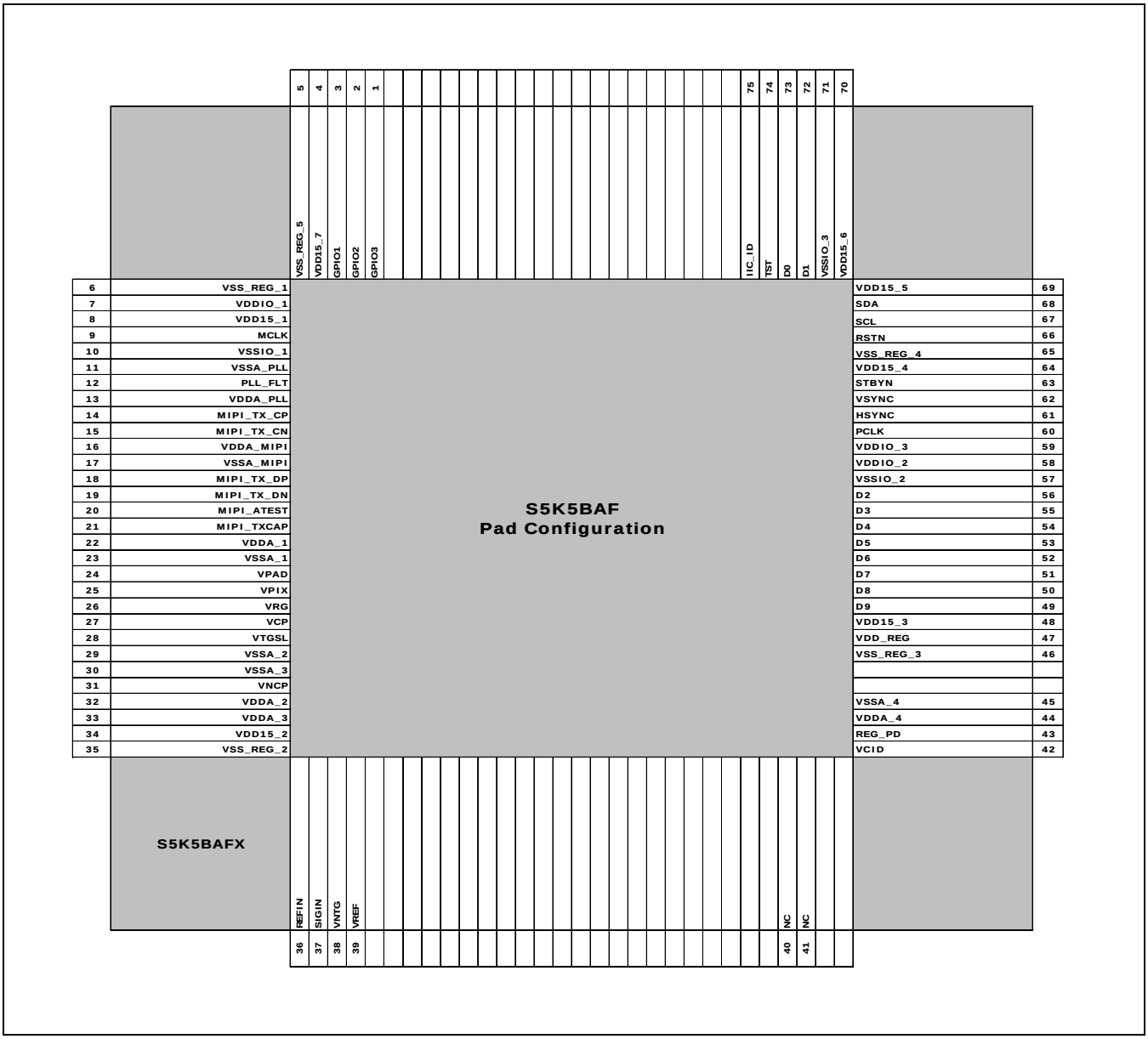


Figure 2. Pad Configuration

5 PAD DESCRIPTION

Table 1. Pad Description

Pad No	Pad Name	I/O	Description
9	MCLK	I	Master clock. 6M to 27MHz. 27MHz is default. Change the PLL register settings if lower frequencies are used.
66	RSTN	I	Master reset (Active low)
63	STBYN	I	Hardware standby mode (Active low). Set to '1' if not used. All parallel outputs go to Hi-Z state during STBYN is asserted.
74	TST	I	Test mode. Set to '0' in normal mode
43	REG_PD	A	Internal regulator power-down 0:operation, 1:power-down
24	VPAD	A	Analog test. Open in normal mode
36	REFIN	A	Analog test. Open in normal mode
39	VREF	A	Analog test pad.
28	VTGSL	A	Analog test pad.
38	VNTG	A	Analog test pad.
42	VCID	A	Analog test. Connect to 2.8V
12	PLL_FLT	A	PLL test. Open in normal
25	VPIX	A	Analog test. 0.1uF external capacitor between pin and ground.
26	VRG	A	Analog test.
27	VCP	A	Analog test. 0.1uF external capacitor between pin and ground.
31	VNCP	A	Analog test.
37	SIGIN	A	Analog test.
75	IIC_ID	I	IIC slave address selection IIC_ID= 0: 0111_1000b, 1: 0101_1010b
67	SCL	IOD	IIC slave clock for host control.
68	SDA	IOD	IIC slave data for host control
3	GPIO_1	IOZ	General purpose I/Os [NOTE] GPIO_1: flash strobe output GPIO_2: flash strobe input
2	GPIO_2	IOZ	
1	GPIO_3	IOZ	
62	VSYNC	OZ	Vertical sync output for parallel interface
61	HSYNC	OZ	Horizontal sync output for parallel interface
60	PCLK	OZ	Pixel clock output for parallel interface
73	D0	OZ	Pixel data output for parallel interface. D9: MSB, D0: LSB
72	D1	OZ	

Pad No	Pad Name	I/O	Description
56	D2	OZ	D[9:0] for 10-bit data D[9:2] for 8-bit data
55	D3	OZ	
54	D4	OZ	
53	D5	OZ	
52	D6	OZ	
51	D7	OZ	
50	D8	OZ	
49	D9	OZ	
14	MIPI_TX_CP	O	CSI-2 Tx clock positive. Open if not used.
15	MIPI_TX_CN	O	CSI-2 Tx clock negative. Open if not used.
18	MIPI_TX_DP	O	CSI-2 Tx data positive. Open if not used.
19	MIPI_TX_DN	O	CSI-2 Tx data negative. Open if not used.
20	MIPI_TX_ATEST	A	Analog test. Open in normal mode or if not used.
21	MIPI_TX_CAP	A	CSI-2 Tx capacitor. 0.1uF external capacitor between pin and ground. Open if not used.
8 34 48 65 69 70 5	VDD15_1 VDD15_2 VDD15_3 VDD15_4 VDD15_5 VDD15_6 VDD15_7	P	Digital Core Power 1.5V (1.4V to 1.6V) [NOTE] a) Regulator on (REG_PD=0): 0.4uF capacitor between VDD15 and ground b) Regulator off (REG_PD=1): 1.5V with 0.4uF power capacitor
47	VDD_REG	P	Regulator input power 1.8V (1.7V to 1.9) [NOTE] a) Regulator on (REG_PD=0): 1.8V b) Regulator off (REG_PD=1): 1.5V
7 58 59	VDDIO_1 VDDIO_2 VDDIO_3	P	I/O power 1.8V (1.7V to 1.9V) or 2.8V (2.6V to 3.0V) with 0.1uF power capacitor
4 6 35 46 64	VSS_REG_5 VSS_REG_1 VSS_REG_2 VSS_REG_3 VSS_REG_4	P	Digital ground
10 57 71	VSSIO_1 VSSIO_2 VSSIO_3		
16	VDDA_MIPI	P	Analog power

Pad No	Pad Name	I/O	Description
13	VDDA_PLL		2.8V (2.6V to 3.0V) with 0.1uF power capacitor
22 32 33 44	VDDA_1 VDDA_2 VDDA_3 VDDA_4		
17	VSSA_MIPI		
11	VSSA_PLL		
23 29 30 45	VSSA_1 VSSA_2 VSSA_3 VSSA_4	P	Analog ground

6 PIXEL ARRAY INFORMATION

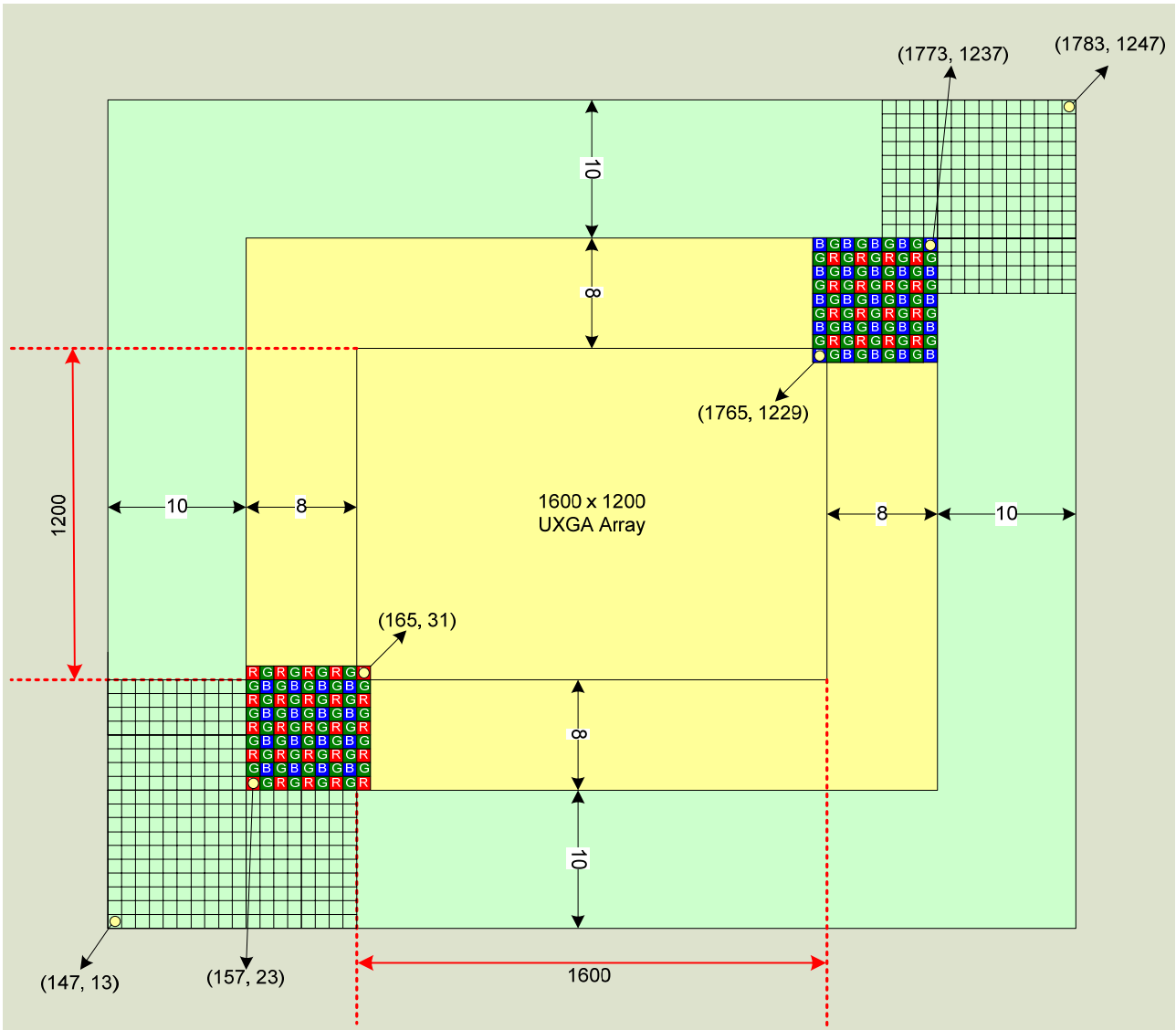


Figure 3. Pixel Arrary Information

7 VIDEO OUTPUT INTERFACE DESCRIPTION

7.1 PARALLEL OUTPUT INTERFACE

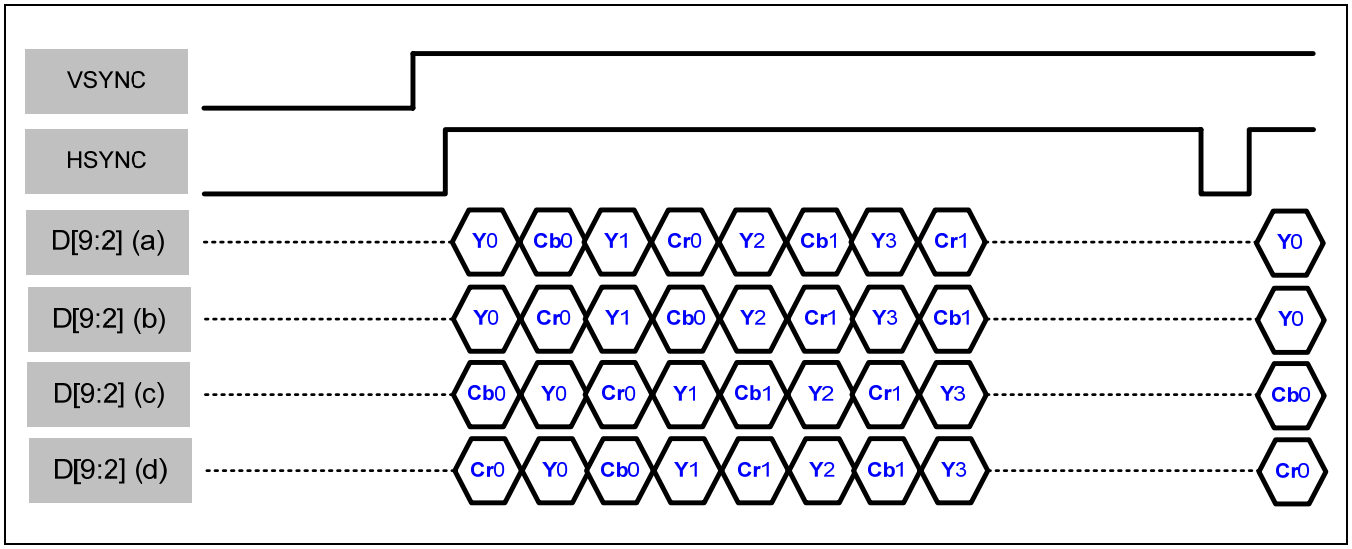


Figure 4. ITU-R.601 YCbCr Data Output Timing

NOTE: Set the related register to select the data output sequence, (a) to (d).

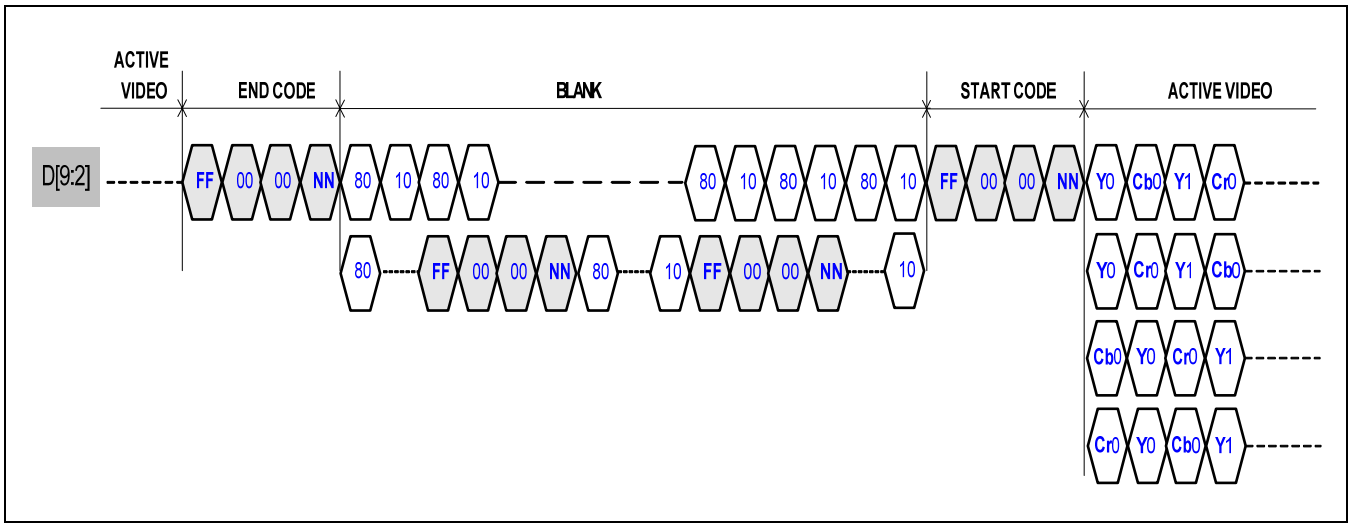


Figure 5. ITU-R.656 YCbCr Data Output Timing

NOTE:

1. The video data is in compliance with Recommendation 656.
2. The data words 0 and 255 (00 and FF in hex notation) are reserved for data identification purposes and consequently only 254 of the possible 256 words may be used to express a signal value.
3. Each timing reference code consists of a four word sequence in the following format: FF 00 00 NN.
4. The fourth word (NN) contains information, the state of field blanking, and the state of line blanking
5. NN consist of 1(MSB, fixed), F, V, H, P3, P2, P1, P0(LSB) bits (F = 0 during field 1, 1 during field 2, V = 0 elsewhere, 1 during field blanking, H = 0 in SAV(Start of Active Video), 1 in EAV(End of Active Video), P3,P2,P1,P0 : protection bits)

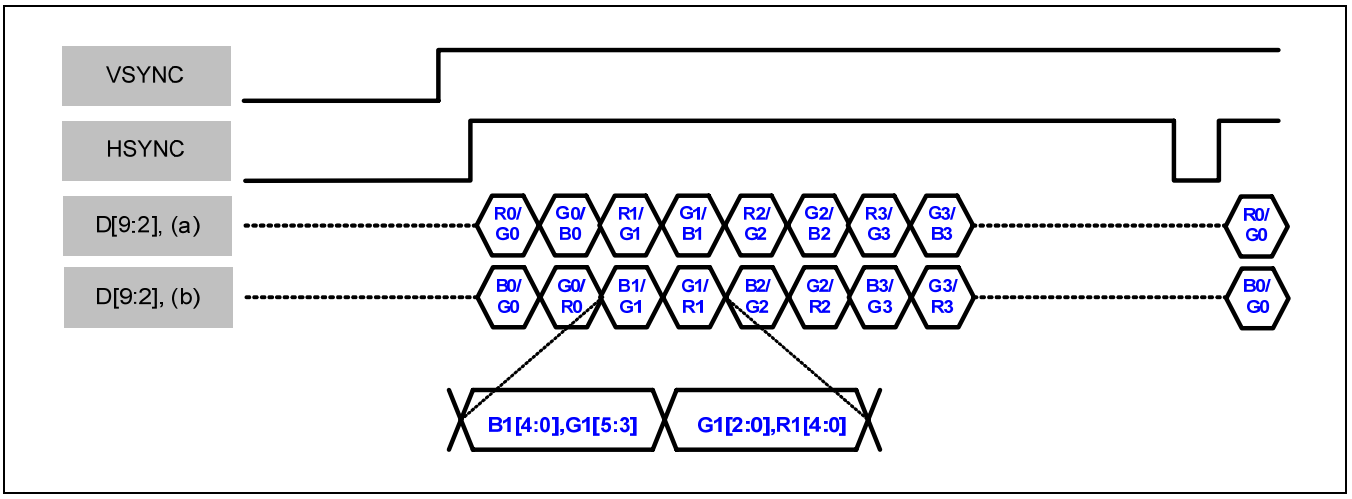


Figure 6. RGB565 Data Output Timing

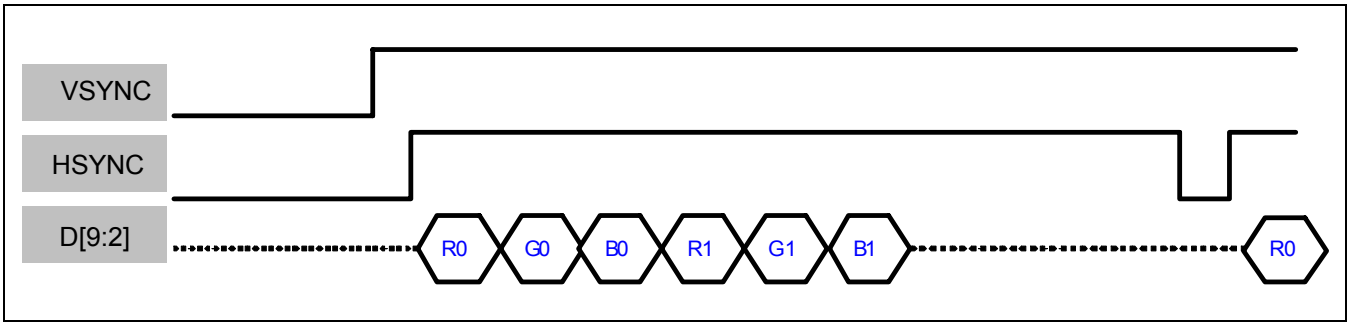


Figure 7. RGB888 Data Output Timing

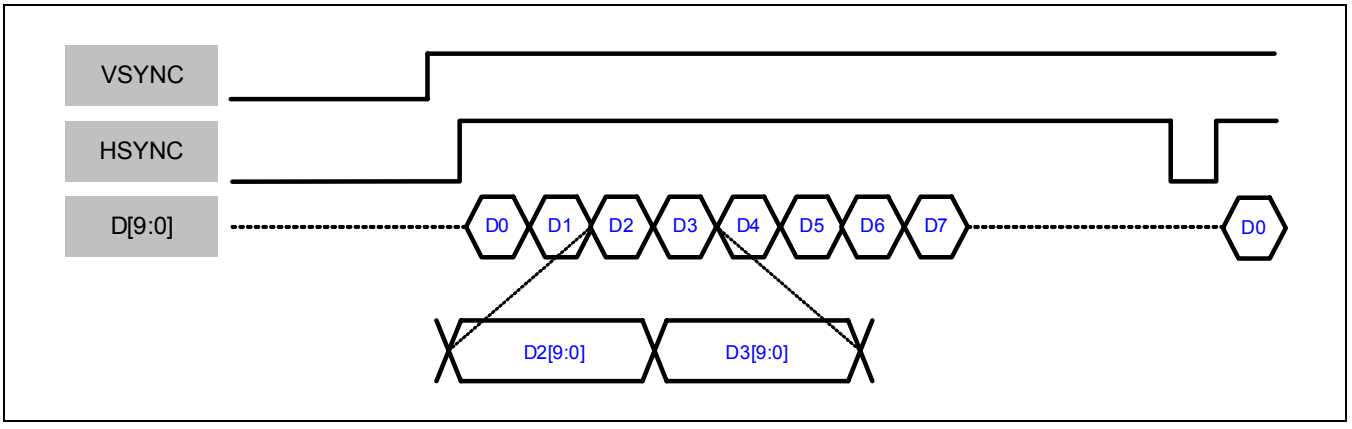


Figure 8. CIS Raw Data Output Timing – RAW10

NOTE: 10-bit parallel data pads should be bonded for RAW10 interface.

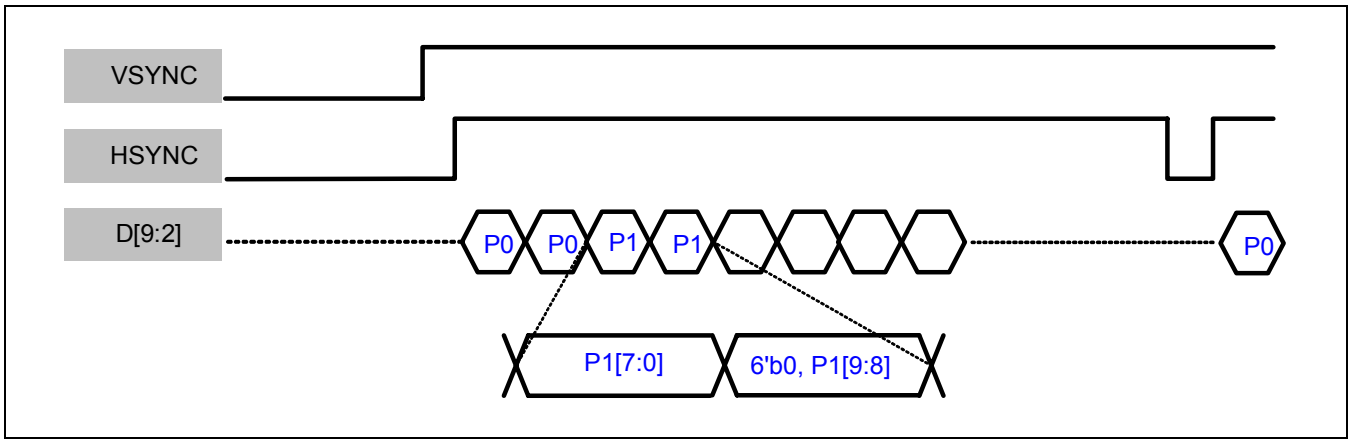


Figure 9. CIS Raw Data Output Timing – RAW10(8+2)

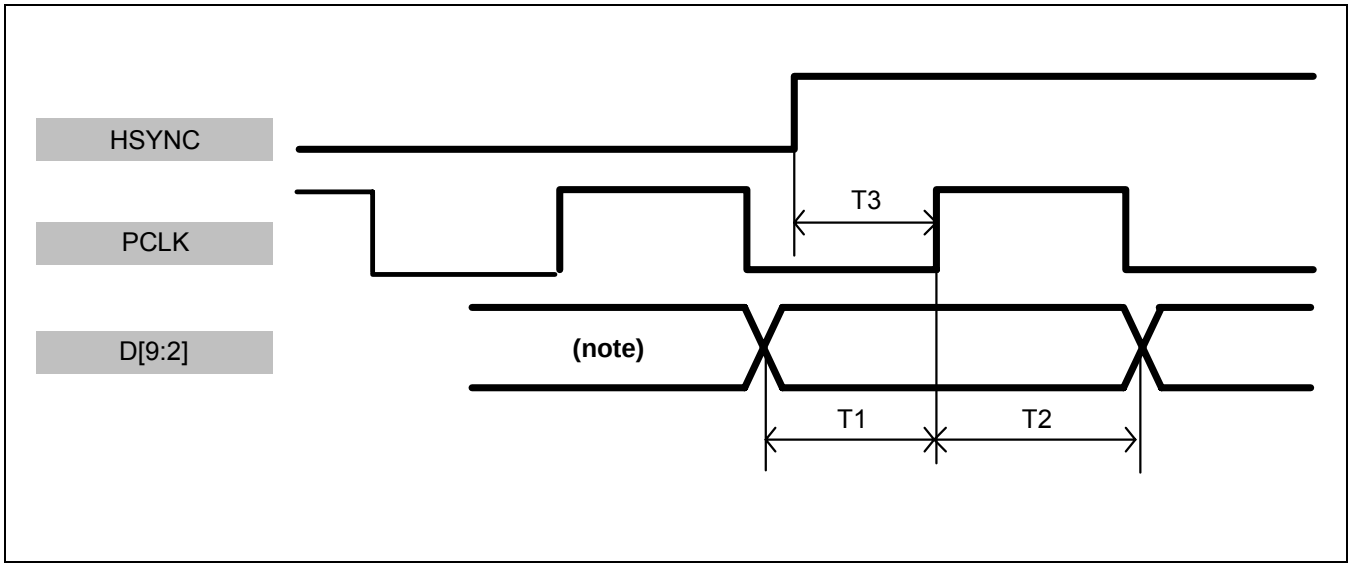


Figure 10. Output Data and Pixel Clock Timing

NOTE: Blank & start code, otherwise ‘0’ for ITU-R.656 output format:

Symbol	Parameter	Min	Max	Unit
T1	Data Setup Time to PCLK	4	-	ns
T2	Data Hold Time to PCLK	4	-	ns
T3	HSYNC↑ to PCLK↑ delay	4	-	ns

7.2 SERIAL OUTPUT INTERFACE (MIPI CSI-2)

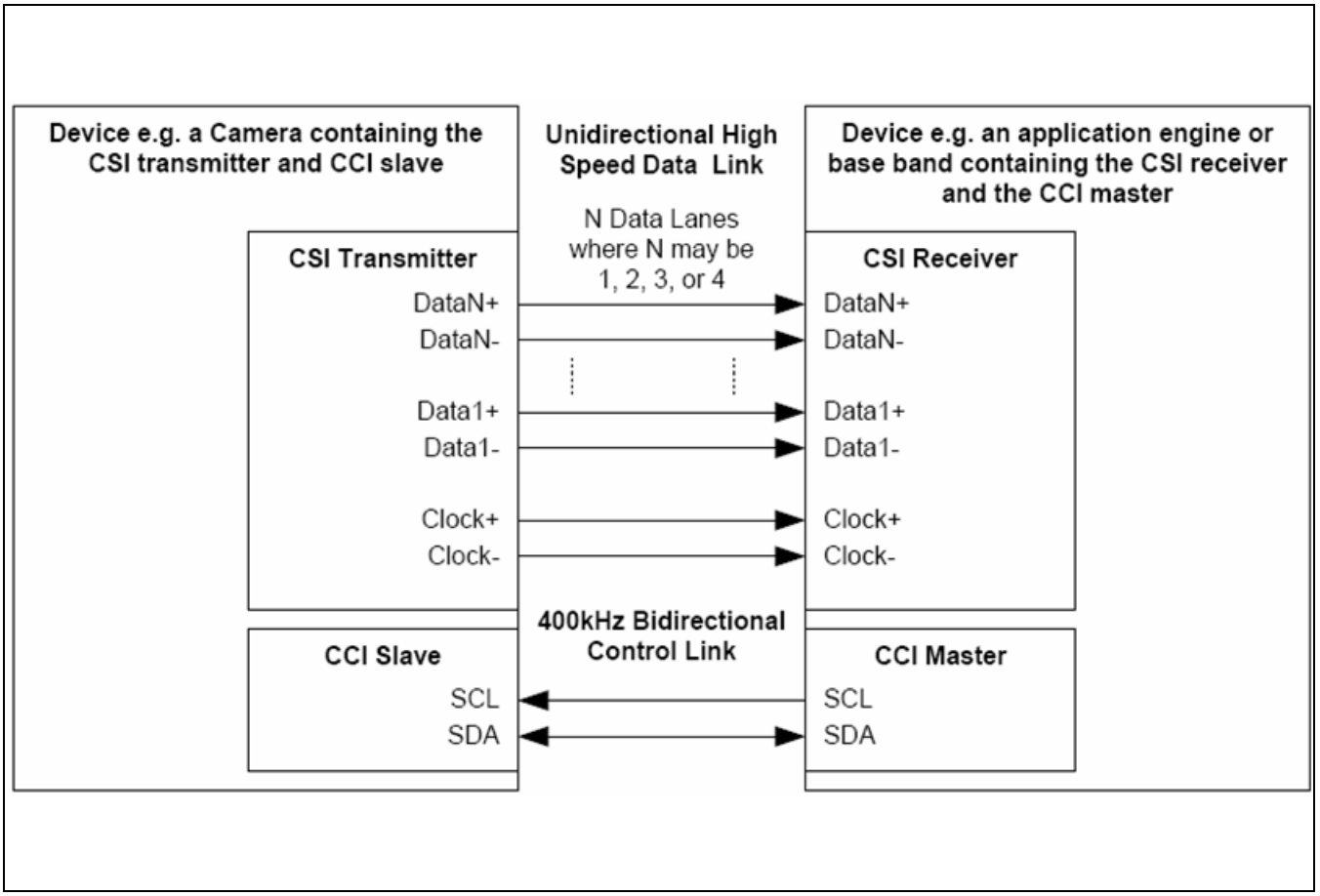


Figure 11. CSI-2 and CCI Transmitter and Receiver Interface

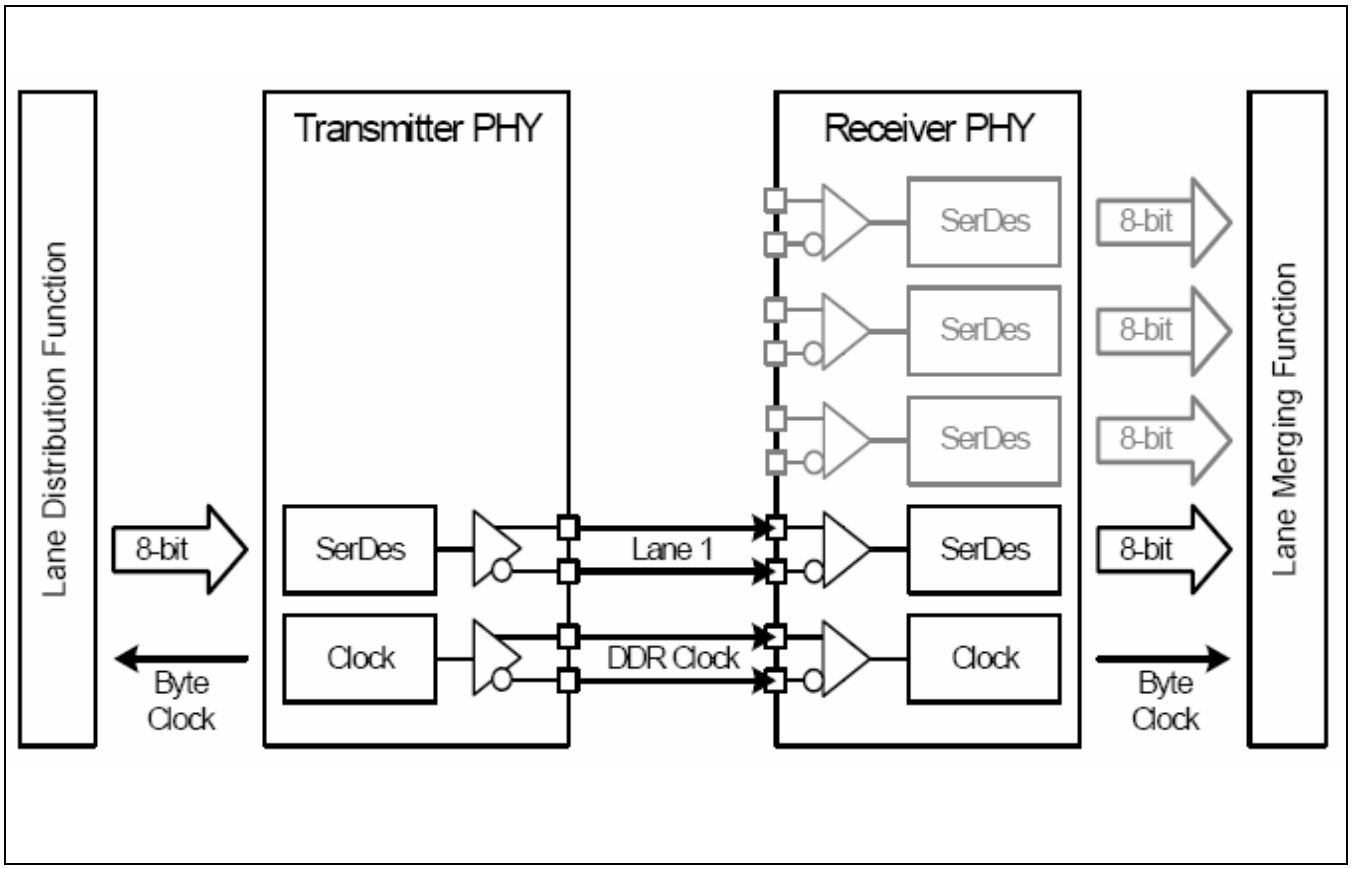


Figure 12. One Lane Transmitter and Four Lane Receiver Example

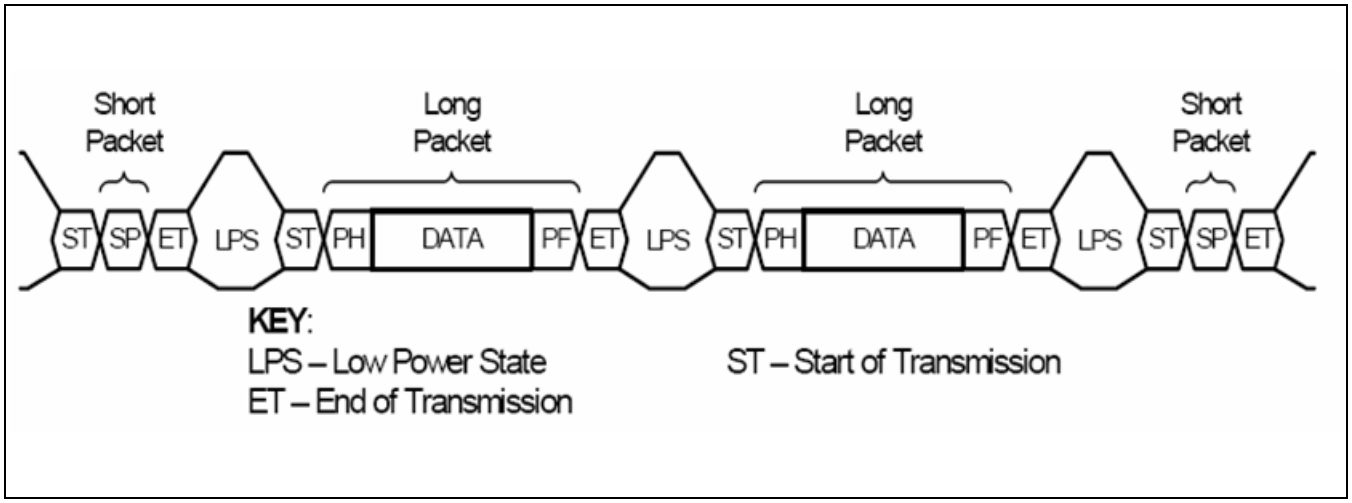


Figure 13. Low Level Protocol Packet Overview

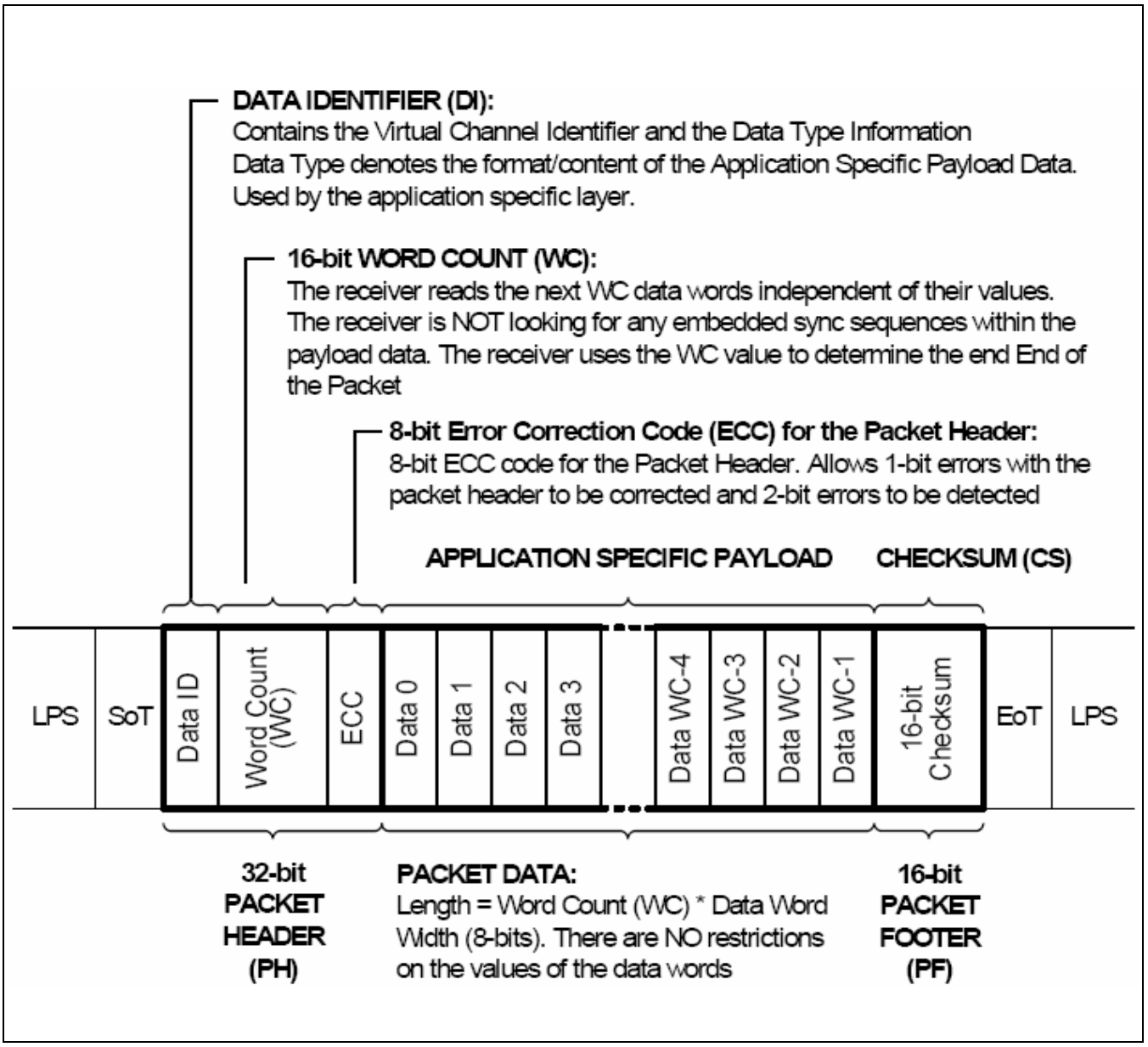


Figure 14. Long Packet Structure

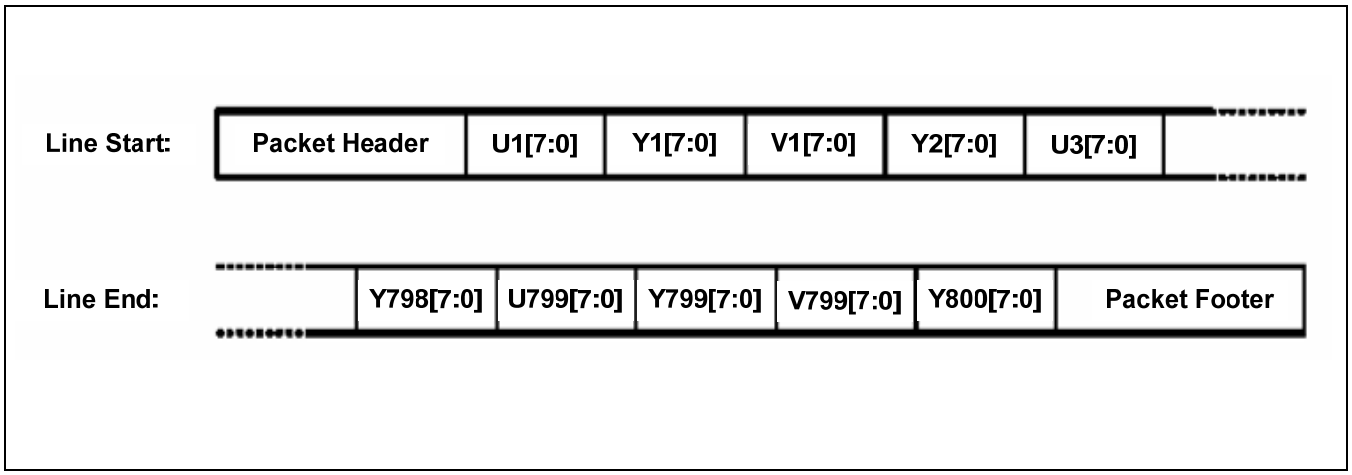


Figure 15. YUV422 Transmission

NOTE: Byte values transmitted LSB first.

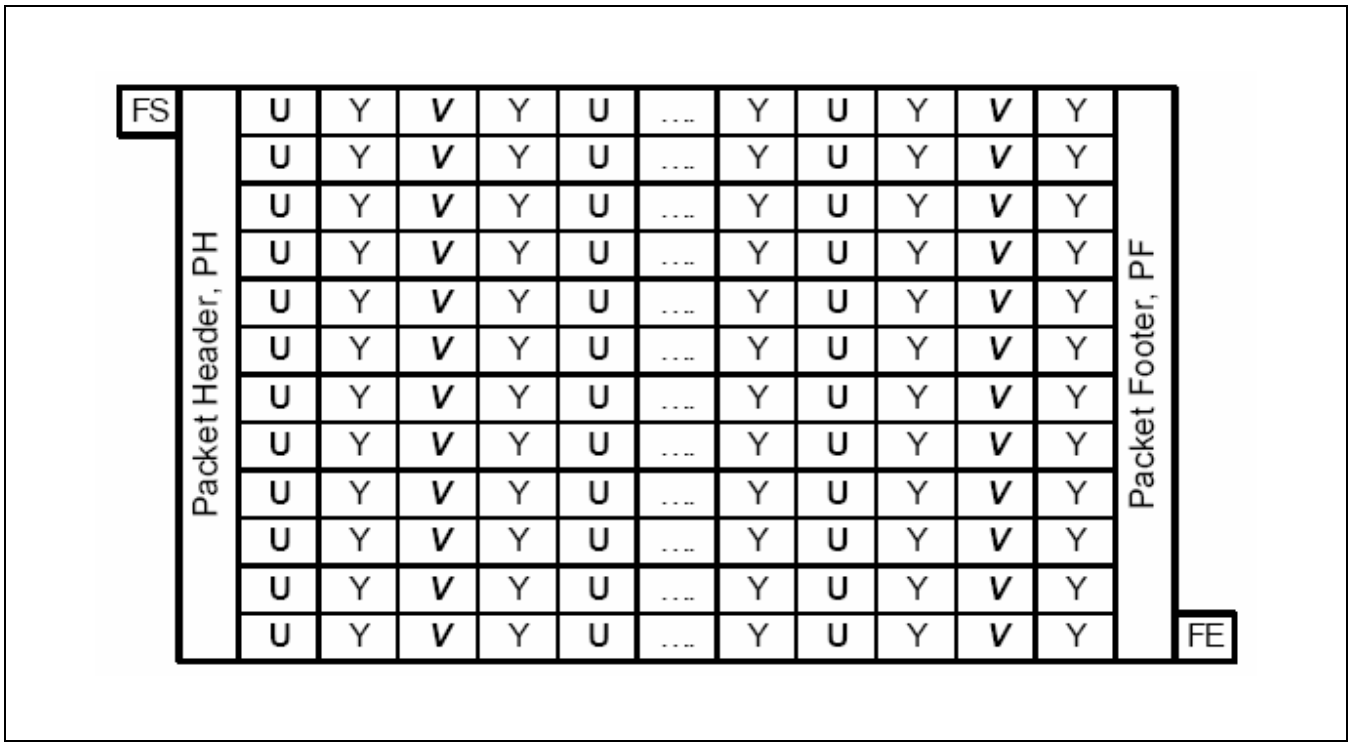


Figure 16. YUV422 Frame Format

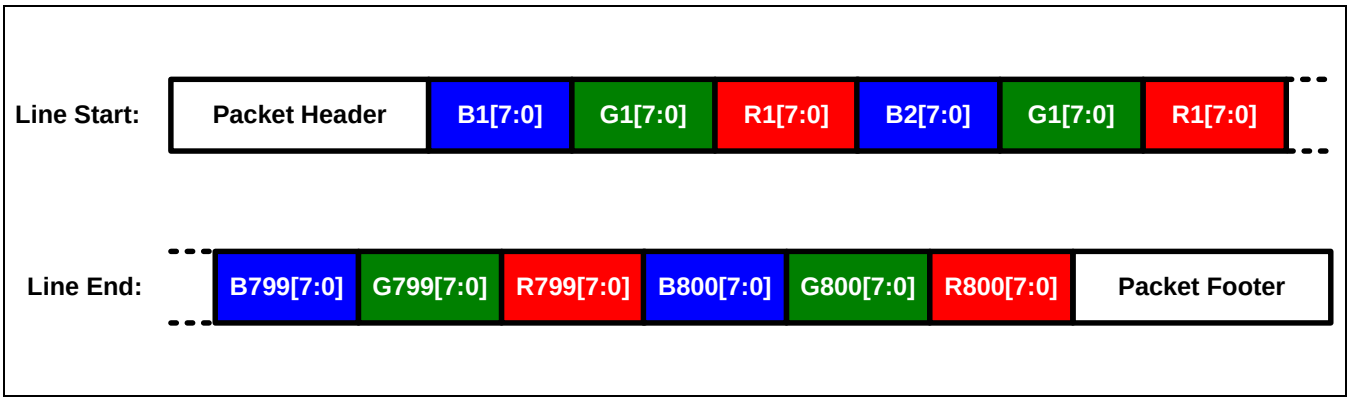


Figure 17. RGB888 Transmission

NOTE: Byte values transmitted LSB first.

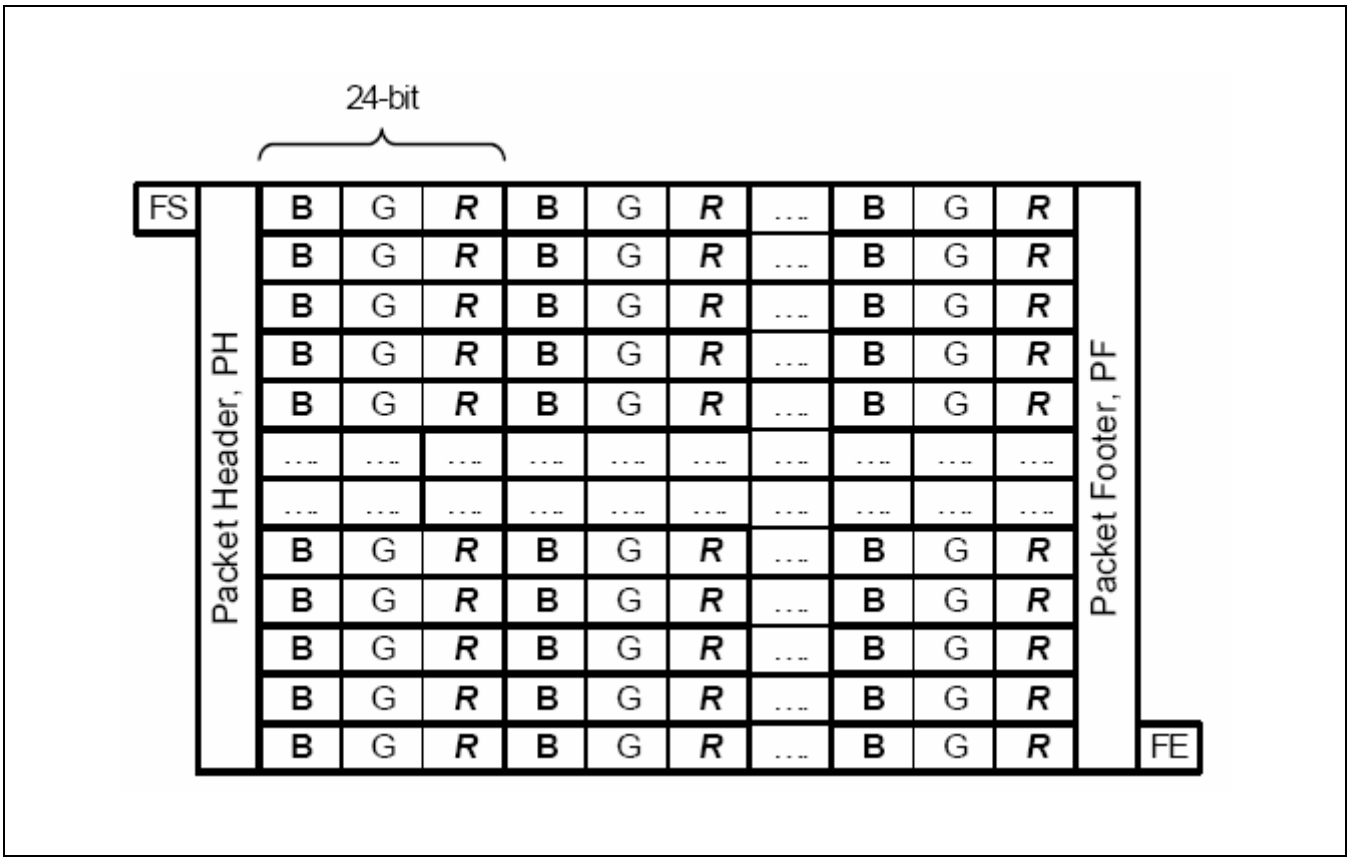


Figure 18. RGB888 Frame Format

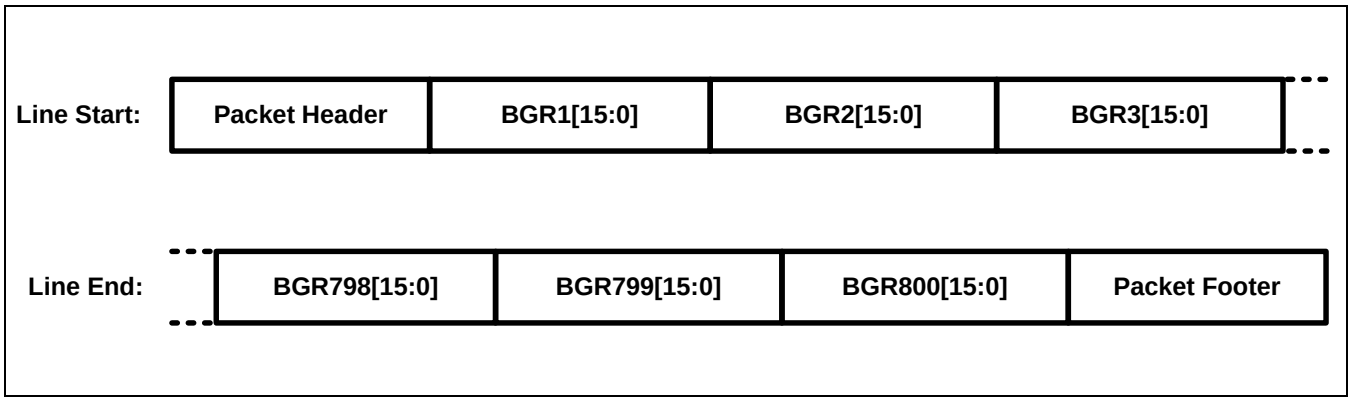


Figure 19. RGB565 Transmission

NOTE: Byte values transmitted LSB first.

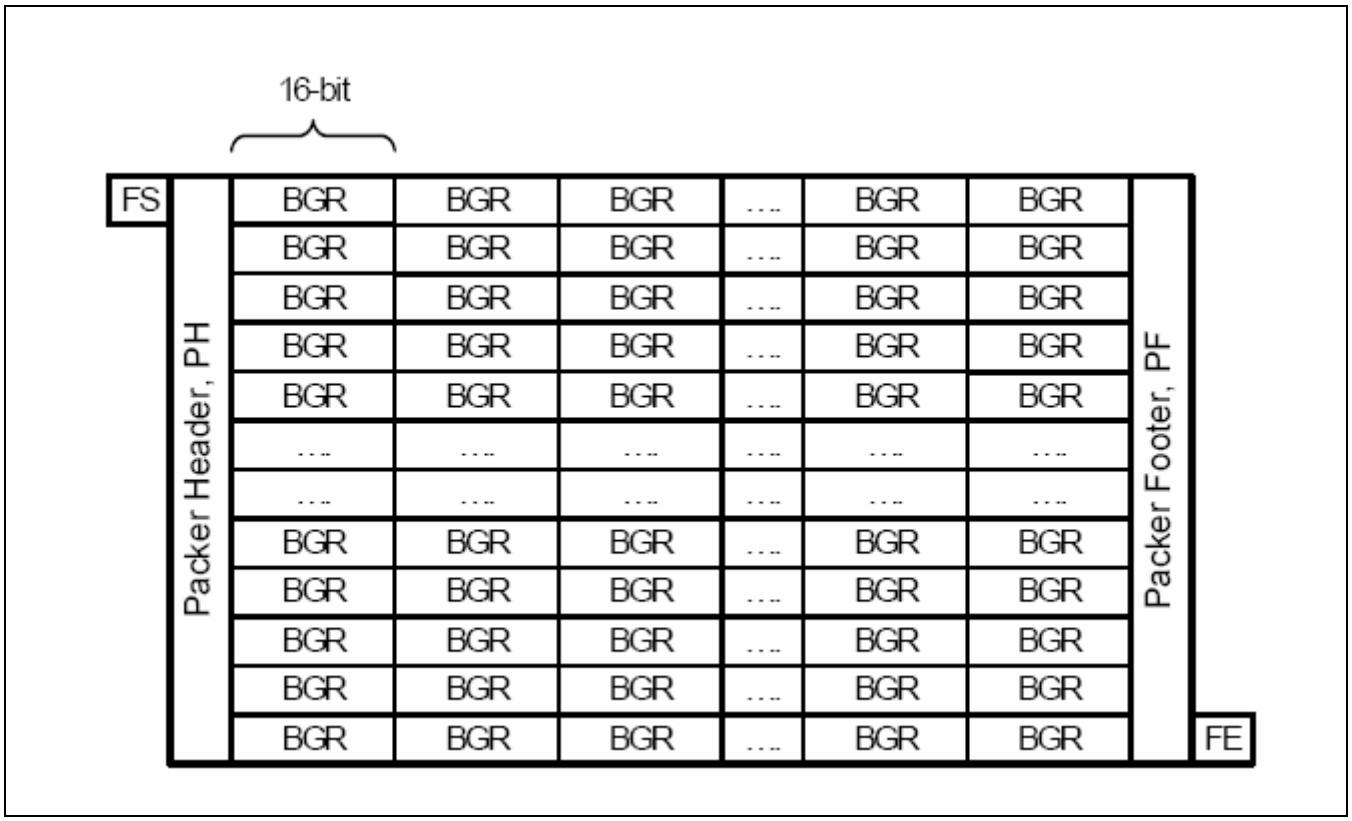


Figure 20. RGB565 Frame Format

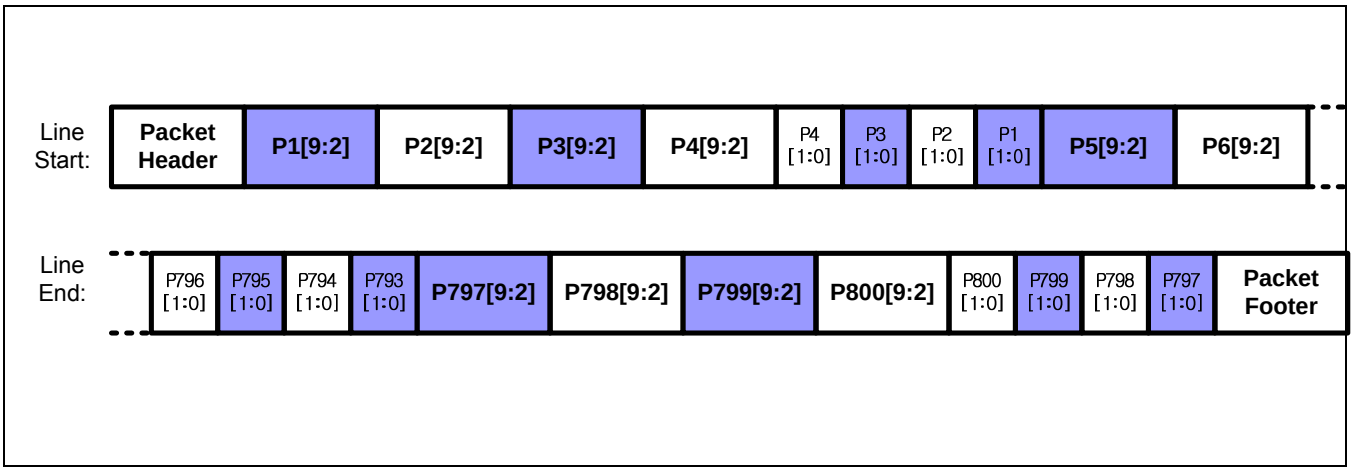


Figure 21. RAW10 Transmission

NOTE: Byte values transmitted LSB first.

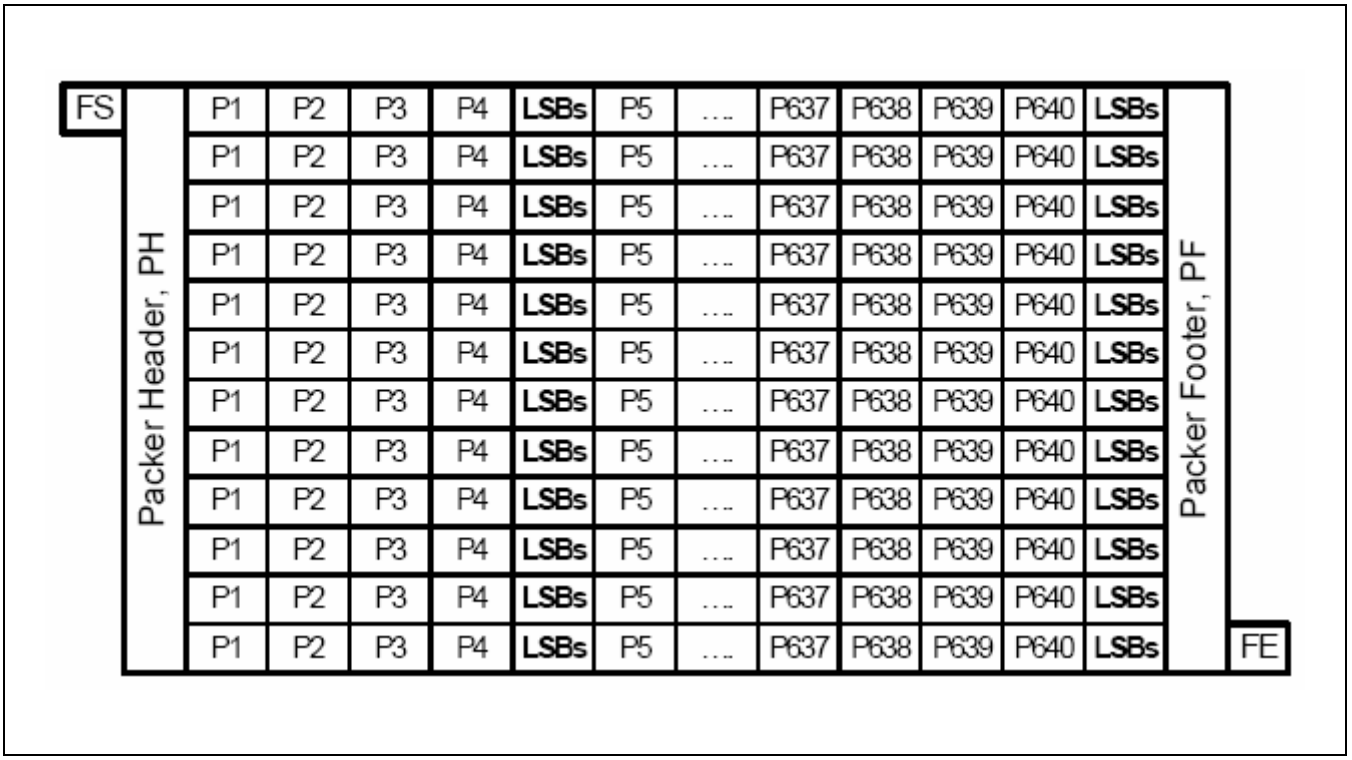


Figure 22. RAW10 Frame Format

7.2.1 Control Interface Description

The I^{2}C interface is a two-wire bi-directional serial bus. Both wires (Serial Clock Line -SCL and Serial Data Line - SDA) are connected to a positive supply via a pull-up resistor, and when the bus is free both lines are high. The output stage of the device must have an open-drain or open collector type IO cell to perform a wired-AND function between all devices that are connected on the bus.

The two-wire serial interface defines several different transmission stages, namely:

- A start bit
- The slave device 7-bit address
- An (No) acknowledge bit coming from slave.
- An 8-bit or 16-bit message (address and/or data).
- A stop bit (or another 8-bit or 16-bit message in multiple Read/Write access)

The data on the SDA pin must be stable during the high period of the clock (SCL) as shown in the Figure 23. Only the master may change the data while SCL is high. A high-to-low transition marks a START condition, and a low-to-high a STOP condition.

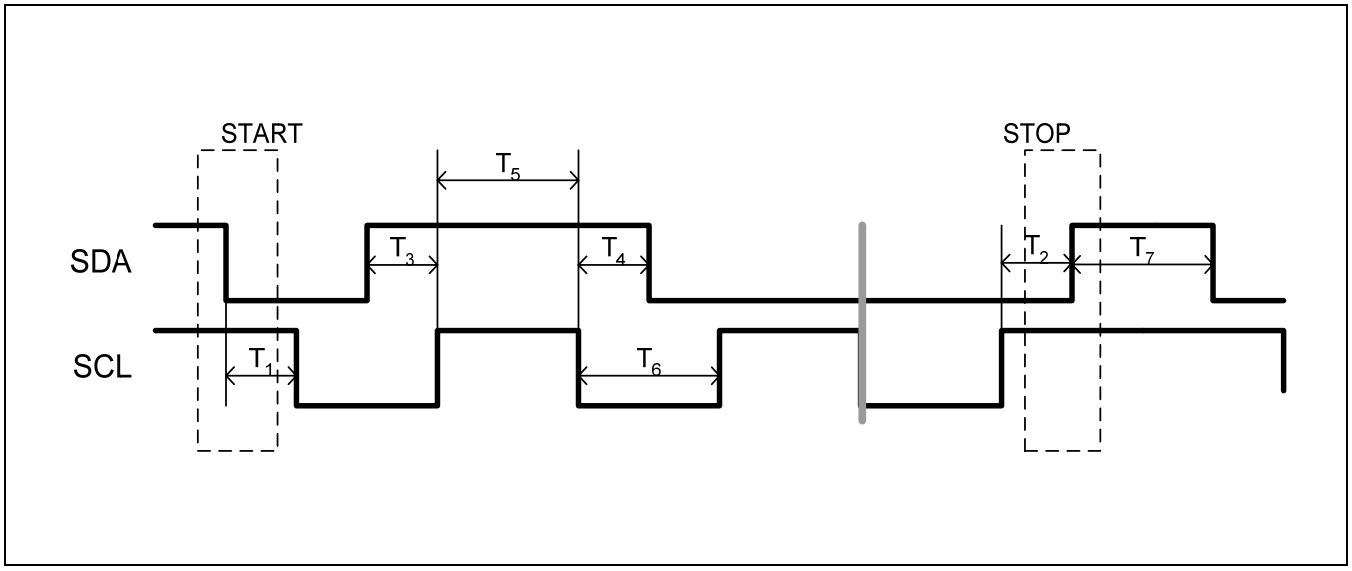


Figure 23. I^{2}C **General Timing Specification**

(a) Standard Mode

Symbol	Parameter	Min	Max	Unit
	SCL clock frequency	0	100	kHz
T1	Hold time for START condition	0.4	-	us
T2	Setup time for STOP condition	4.0	-	us
T3	Data setup time	250	-	ns
T4	Data hold time	0	3.45	us
T5	High period of the SCL clock	4.0	-	us
T6	Low period of the SCL clock	4.7	-	us
T7	Bus free time between STOP and START condition	4.7	-	us
	Rise time for both SDA and SCL signals		1000	ns
	Fall time for both SDA and SCL signals		300	ns
C_B	Capacitive load for each bus line		400	pF

(b) Fast Mode

Symbol	Parameter	Min	Max	Unit
	SCL clock frequency	0	400	kHz
T1	Hold time for START condition	0.6	-	us
T2	Setup time for STOP condition	0.6	-	us
T3	Data setup time	100	-	ns
T4	Data hold time	0	0.9	us
T5	High period of the SCL clock	0.6	-	us
T6	Low period of the SCL clock	1.3	-	us
T7	Bus free time between STOP and START condition	1.3	-	us
	Rise time for both SDA and SCL signals		300	ns
	Fall time for both SDA and SCL signals		300	ns
C_B	Capacitive load for each bus line		400	pF

NOTE: Fast mode can be supported with above 14MHz external clock (MCLK).

The master device activates a START condition, and sends the first byte of data that contains the 7-bit address, and a direction bit (R/W#, 1 for read, 0 for write). The addressed device pulls down the SDA line as an acknowledge procedure.

Figure 24 illustrates the steps to read and write data transfers.

- The colored boxes represent master-to-slave data transfer.
- The clear boxes represent slave-to-master data transfer.

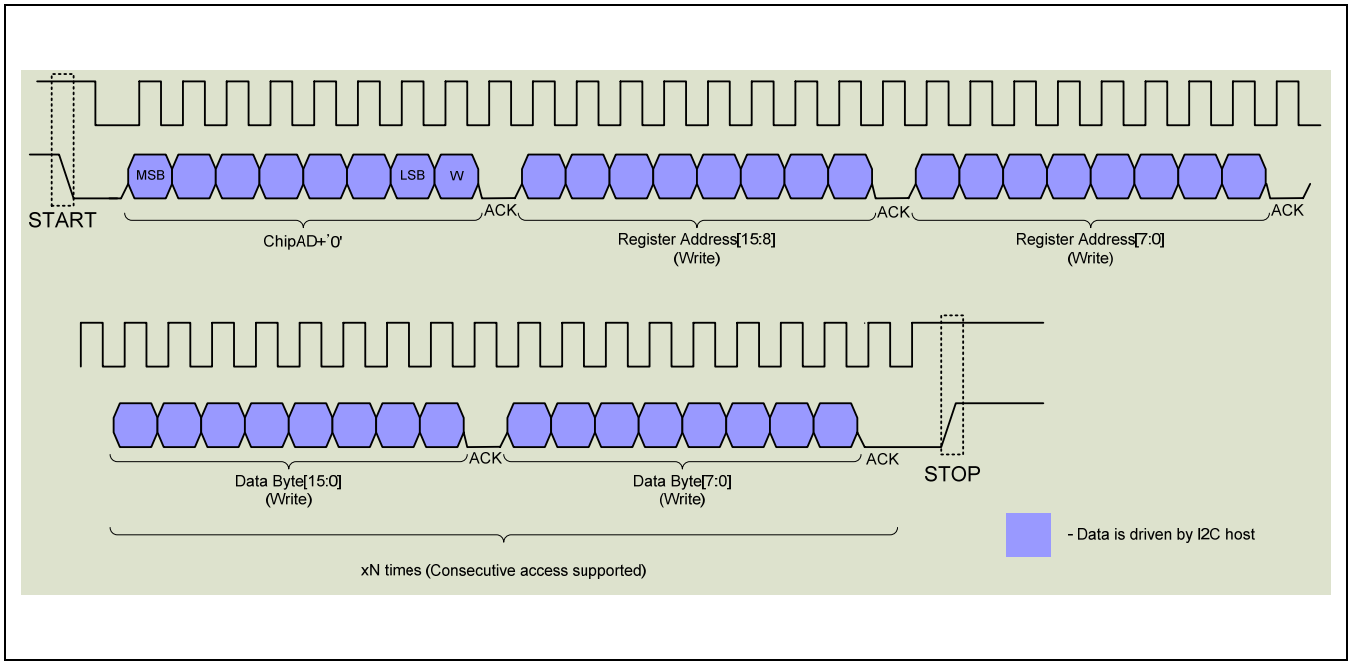


Figure 24. I^2C **Write Timing Example(16 Address, 2 data bytes)**

NOTE: Use pin configuration of IIC_ID to change the device address, which is described in pad description.

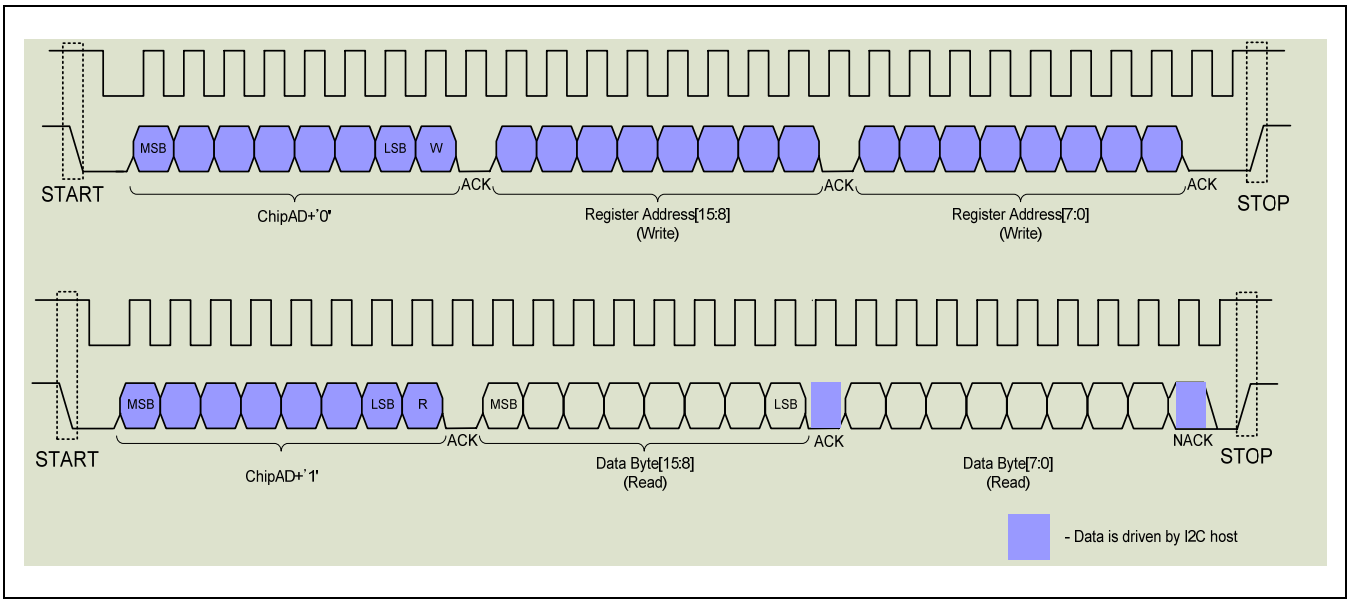


Figure 25. I²C Single Read Timing Example(16 Address, 2 data bytes)

NOTE: Use pin configuration of IIC_ID to change the device address, which is described in pad description.

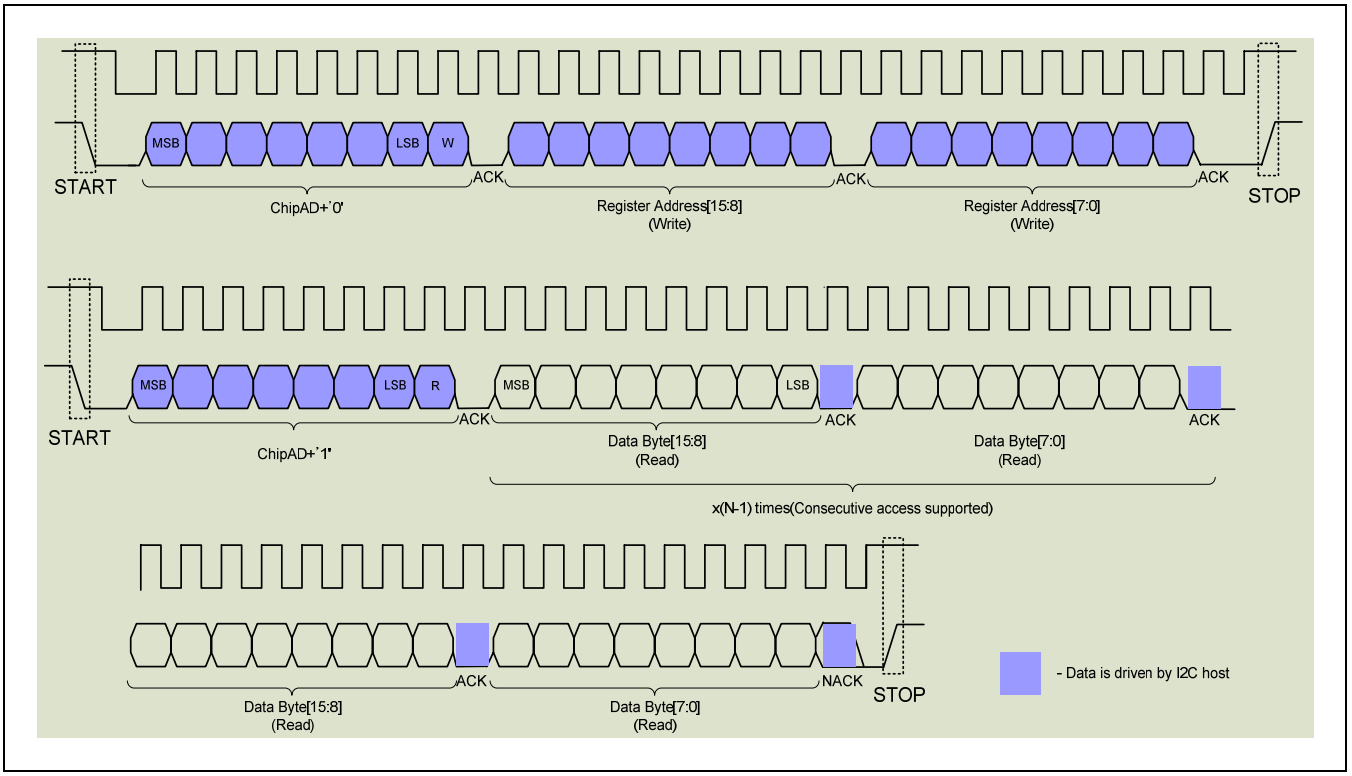


Figure 26. I²C multiple(N) Read Timing Example(16 Address, 2 data bytes)

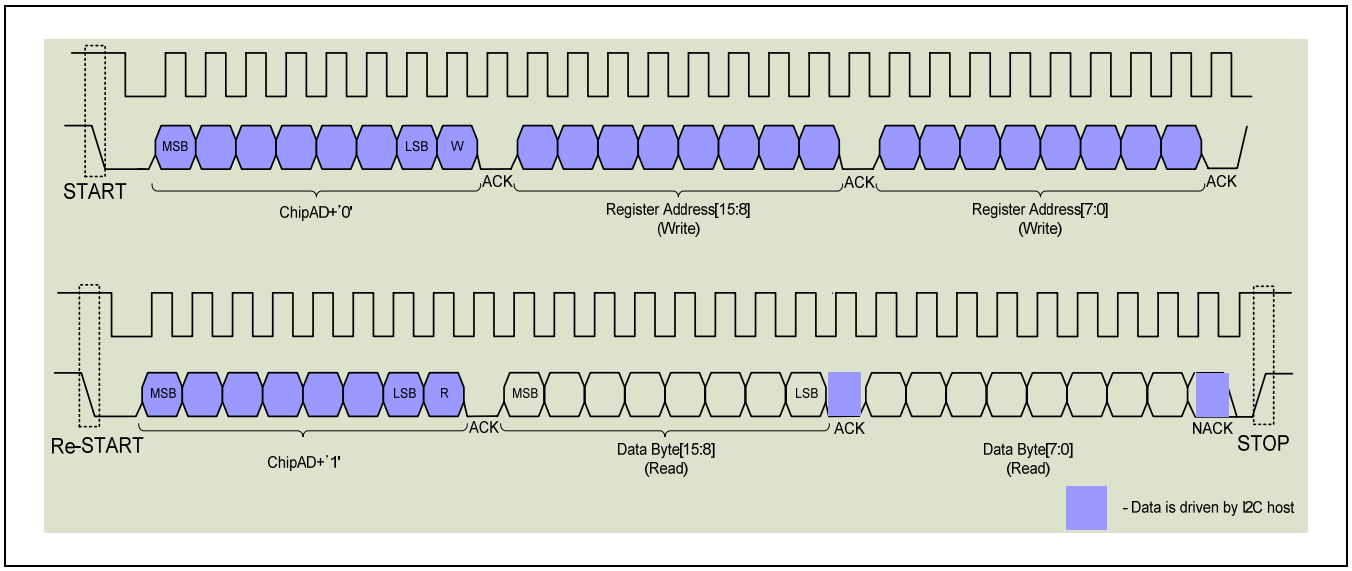
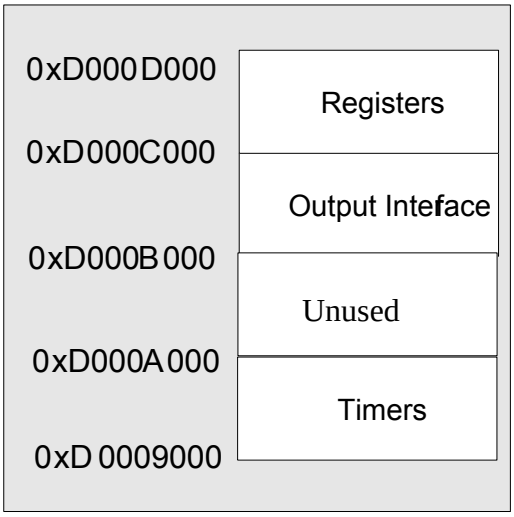


Figure 27. I²C Single Read acess with Repeated Start Example(16 Address, 2 data bytes)

IIC Writing Example

IIC_ID	Device Address
0	0111_1000b/78h
1	0101_1010b/5Ah

Configure IIC_ID=0, for device address, 0111_1000cab.



When accessing one of GTG Registers, its page address is C0. You can access it in 8-bit access mode or 16-bit access mode.

For example: When writing data(AAh) to register (04h) of page C0 in 8-bit access mode;

write(78h, FEh, C0h) // set page C0

write(78h, 04h, 00h) // upper byte

write(78h, 05h, AAh) // lower byte

NOTE: Write (device address & R/W bit, register address, data, ...)
NOTE: All data are regarded as 16-bits.

For example: When writing a series of data to continuous registers of page (C0h) in 8-bit access mode;

data(AAh) -> register(04h)

data(BBh) -> register(06h)

data(CCh) -> register(08h)

data(DDh) -> register(0Ah)

write(78h, FEh, C0h) // set page C0

write(78h, 04h, 00h, AAh, 00h, BBh, 00h, CCh, 00h, DDh)

For example: When writing a series of data to continuous registers of page (C0h) in 16-bit access mode;

write (78h, C0h, 04h, 00h, AAh, 00h, BBh, 00h, CCh, 00h, DDh)

8 FUNCTIONAL DESCRIPTION

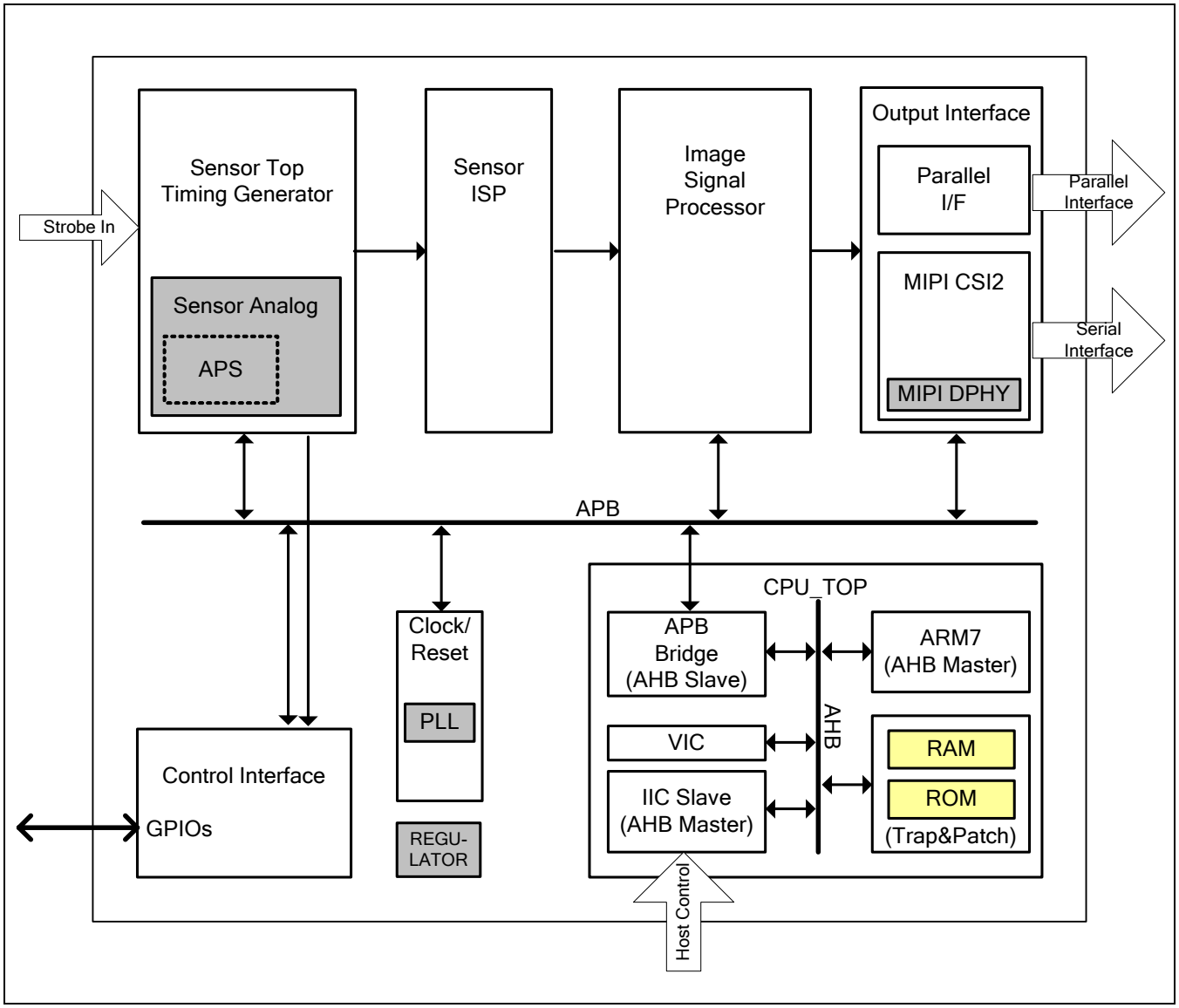


Figure 28. Functional Block Diagram

8.1 ANALOG TO DIGITAL CONVERTER (ADC)

The image sensor has an on-chip ADC. Column parallel ADC scheme is used for low power analog processing.

8.1.1 Correlated Double Sampling (CDS)

The analog output signal of each pixel includes some temporal random noise caused by the pixel reset action and some fixed pattern noise by the in-pixel amplifier offset deviation. To eliminate those noise components, a correlated double sampling (CDS) circuit is used before converting to digital code.

8.1.2 Programmable Gain

Use Gain Control Register to control the gain of pixel signal. As increasing the signal gain control register, the ADC conversion range slope decreases and its output code value increases. The gain increased as following equation:

Analog Gain
register gain[7:0]
$(\text{Analogue gain}) = 2^{GAIN[7:5]} \times \left(1 + \frac{GAIN[4:0]}{32}\right)$

Figure 29. Relative Channel Gain

8.2 TIMING GENERATOR FUNCTIONS

8.2.1 CIS Raw Data Output

GTG supports configurable-bit CIS raw data.

8.2.2 Pixel Array Addresses

An addressable pixel array is defined as the pixel address range to be read. The addressable pixel array can be assigned anywhere on the pixel array. ***x_addr_start***, y_***addr_start***, ***x_addr_end*** and y_***addr_end*** register controls the addressed region of the pixel array.

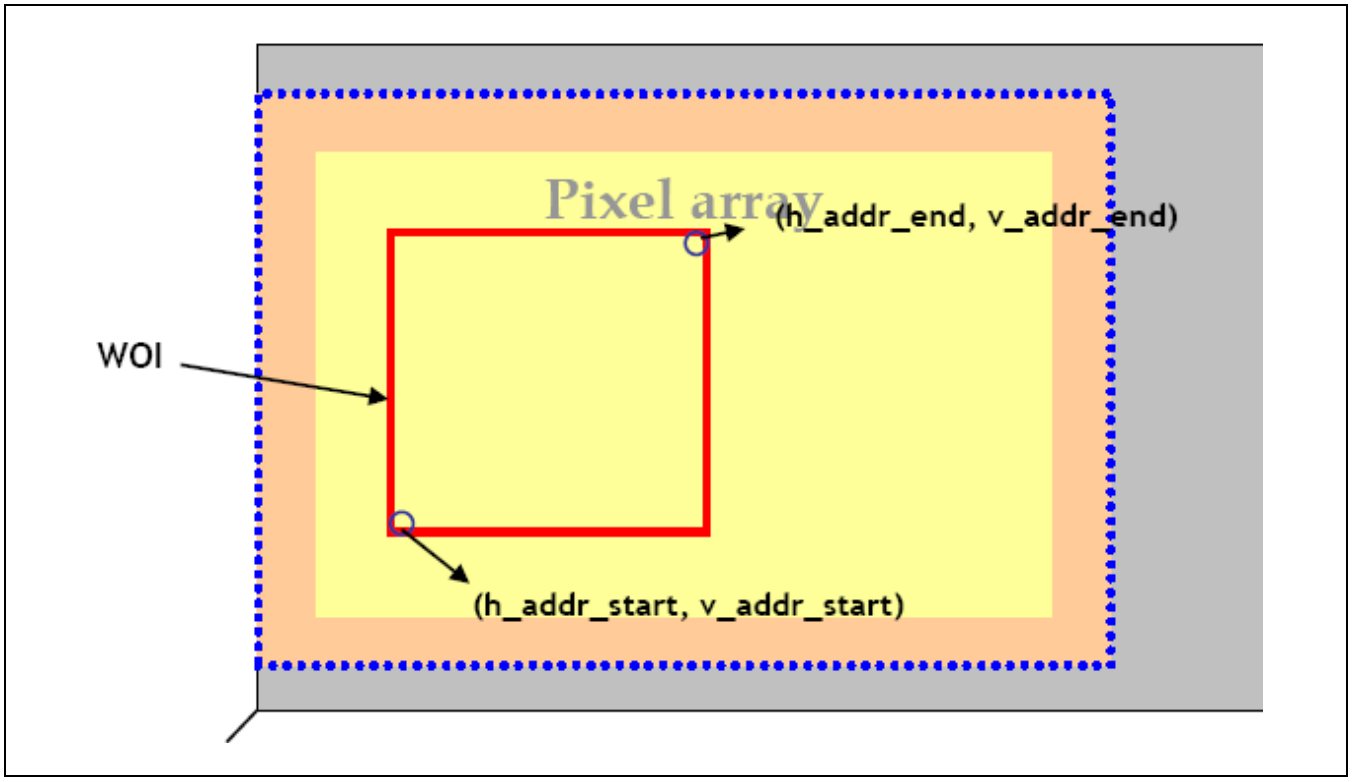


Figure 30. Window of interest of Pixel Array

8.2.3 Mirror/ Flip

The pixel data is normally read out from left to right in the horizontal direction and from top to bottom in the vertical direction. Change the ***mirror/flip*** mode to reverse the read-out sequence, and the resulting image can be flipped like a mirror image. Pixel data is then read out from right to left in horizontal mirror mode and from bottom to top in vertical flip mode. The horizontal mirror and the vertical flip mode can be programmed by the image orientation register.

The sensor module supports four possible pixel readout orders, as described in the sections below.

8.2.4 Standard Readout

x_addr_start, x_addr_end register controls the addressed region of the horizontal pixel data output, and the ***y_addr_start, y_addr_end*** register controls the addressed region of the vertical pixel data output.

8.2.5 Horizontally Mirrored and Vertically Flipped Readout

x_addr_end, x_add_start register controls the addressed region of the horizontal pixel data output, and ***y_addr_end, y_add_start*** register controls the addresses region of the vertical pixel data output.

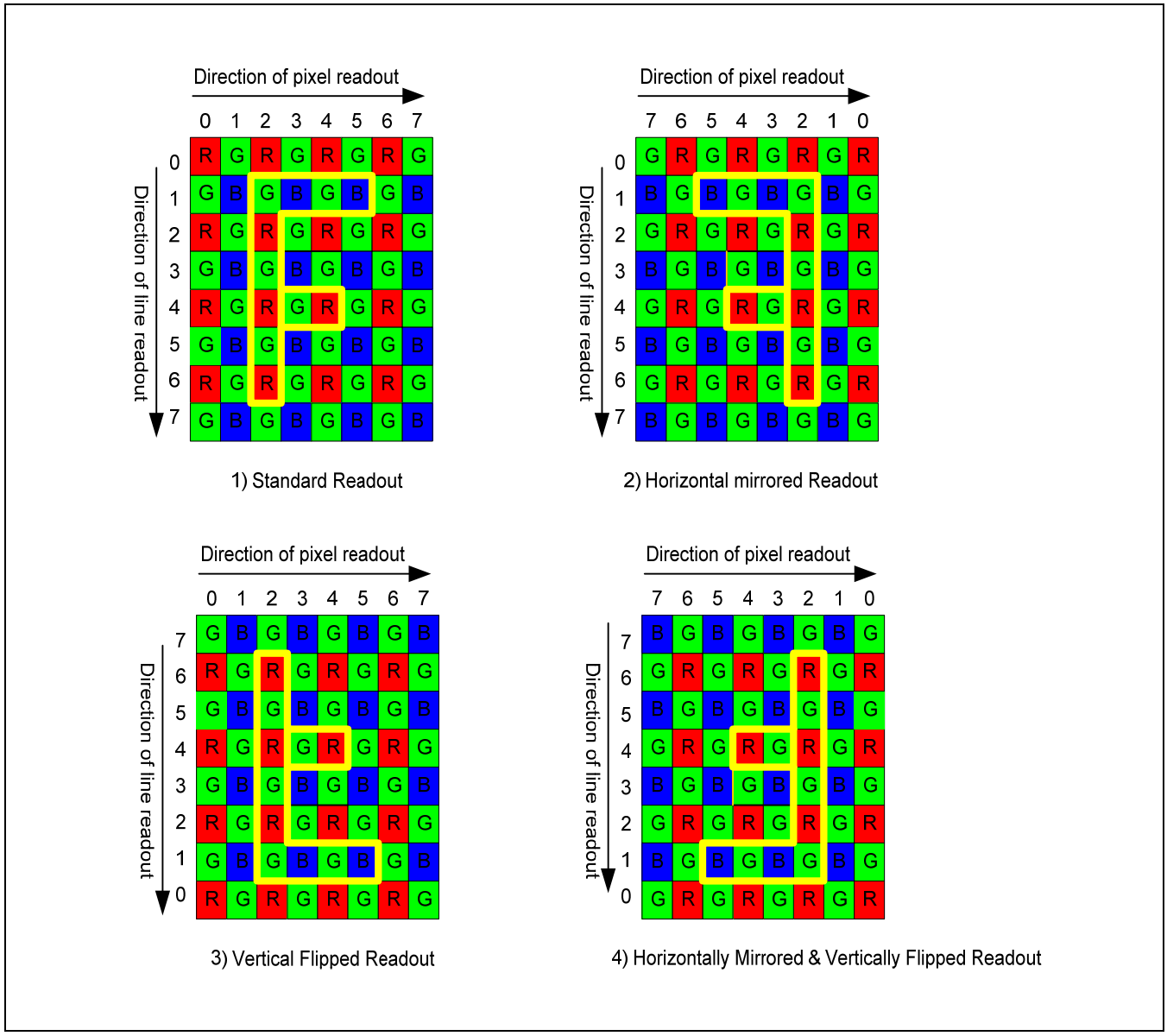


Figure 31. Horizontal Mirror and Vertical Flip

8.2.6 Frame Rate Control (Virtual Frame)

Vary the size of the virtual frame to change the line rate and the frame rate. line_length_pck and frame_length_lines register controls the virtual frame's width and depth. The horizontal and vertical blanking times (horizontal blanking time: **line_length_pck** – ***x_output_size***, vertical blanking time: **frame_length_lines** – ***y_output_size***) should meet system requirements.

Frame rate = TGCLK / (frame_length_lines * line_length_pck)

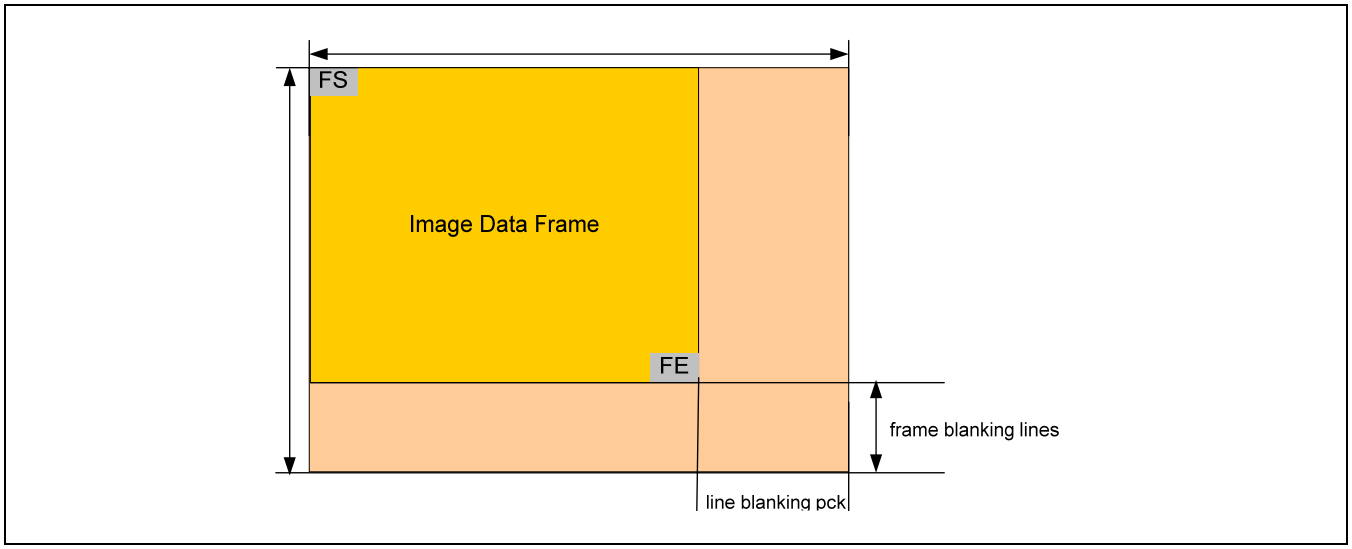


Figure 32. Virtual Frame Timing

8.2.7 Integration Time Control (Electronic Shutter Control)

Shutter operation controls pixel integration time. During the shutter operation, the amount of time – integration time – is determined by the column Step Integration Time Control Register (fine_integration_time) and the line Step Integration Time Control Register (coarse_integration_time). The total integration time of the sensor module can be calculated using the following formula:

Total_integration_time = {(coarse_integration_time * line_length_pck) + fine_integration_time + const} * pclk period [sec]

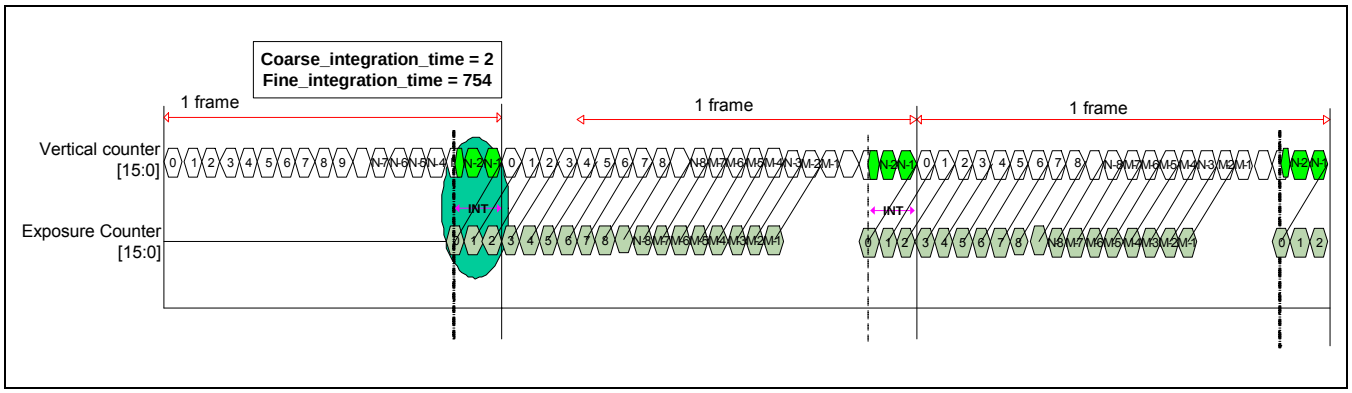


Figure 33. Integration Time Counter Diagram

8.2.8 LED Flash Control

Both devices are controlled by the firmware and activated directly by the sensor.

Register-Based Host Interface

The following registers control the flash status and functionality:

REG_TC_FLS_Mode	Sets flash mode according to TC_FlashSt_type enum
REG_TC_FLS_Threshold	Sets flash activation threshold in normalized brightness units
REG_TC_FLS_Polarity	Sets flash device polarity. 1: active high, 0: active low

NOTE:

1. There is no guarantee for the quality of AE or any other algorithm convergence before the flash capture. There is typically only one frame for convergence. This time frame is too short, and the results may not be perfect.
2. Using an extra frame for AE or AWB convergence extends the preview to capture time. Typically, it doubles this period.

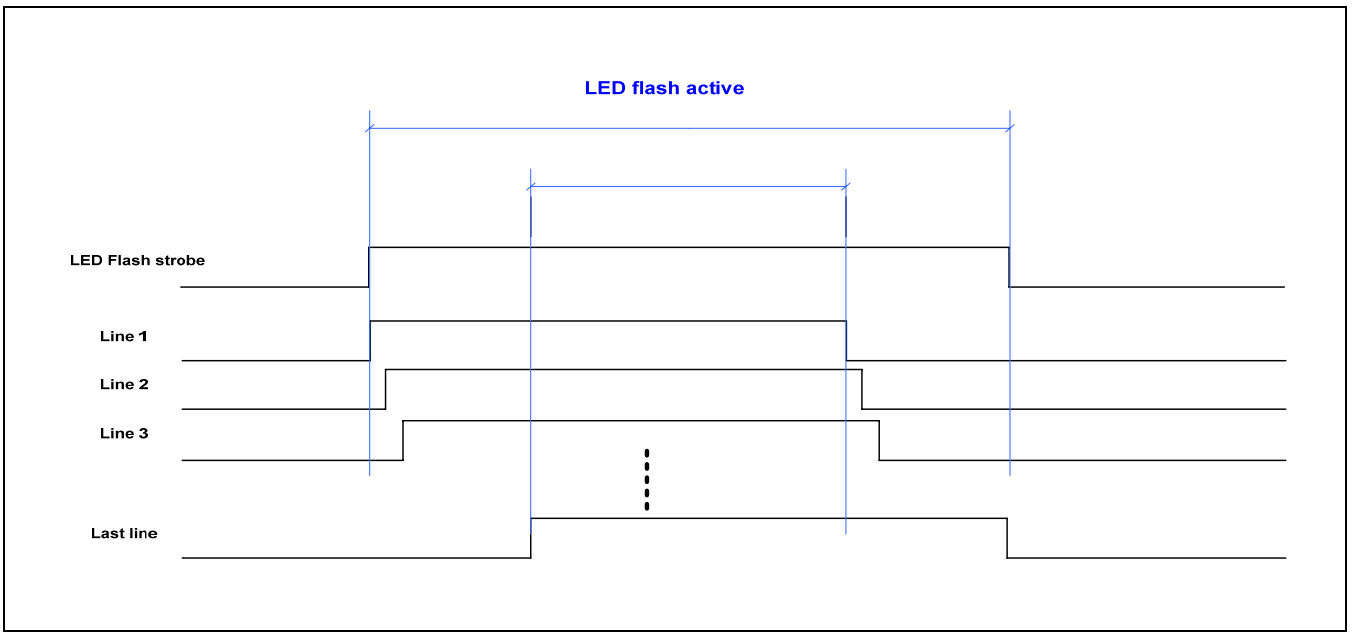


Figure 34. Flash Timing Diagram

Following are application examples for each flash device type. Please note that when LED is used, the host is responsible for algorithm convergence prior to capture, the FW is responsible for algorithm convergence. Dedicated flash algorithms convergence code can be added to the FW using a special SW hook function that is loaded to the FW during initialization.

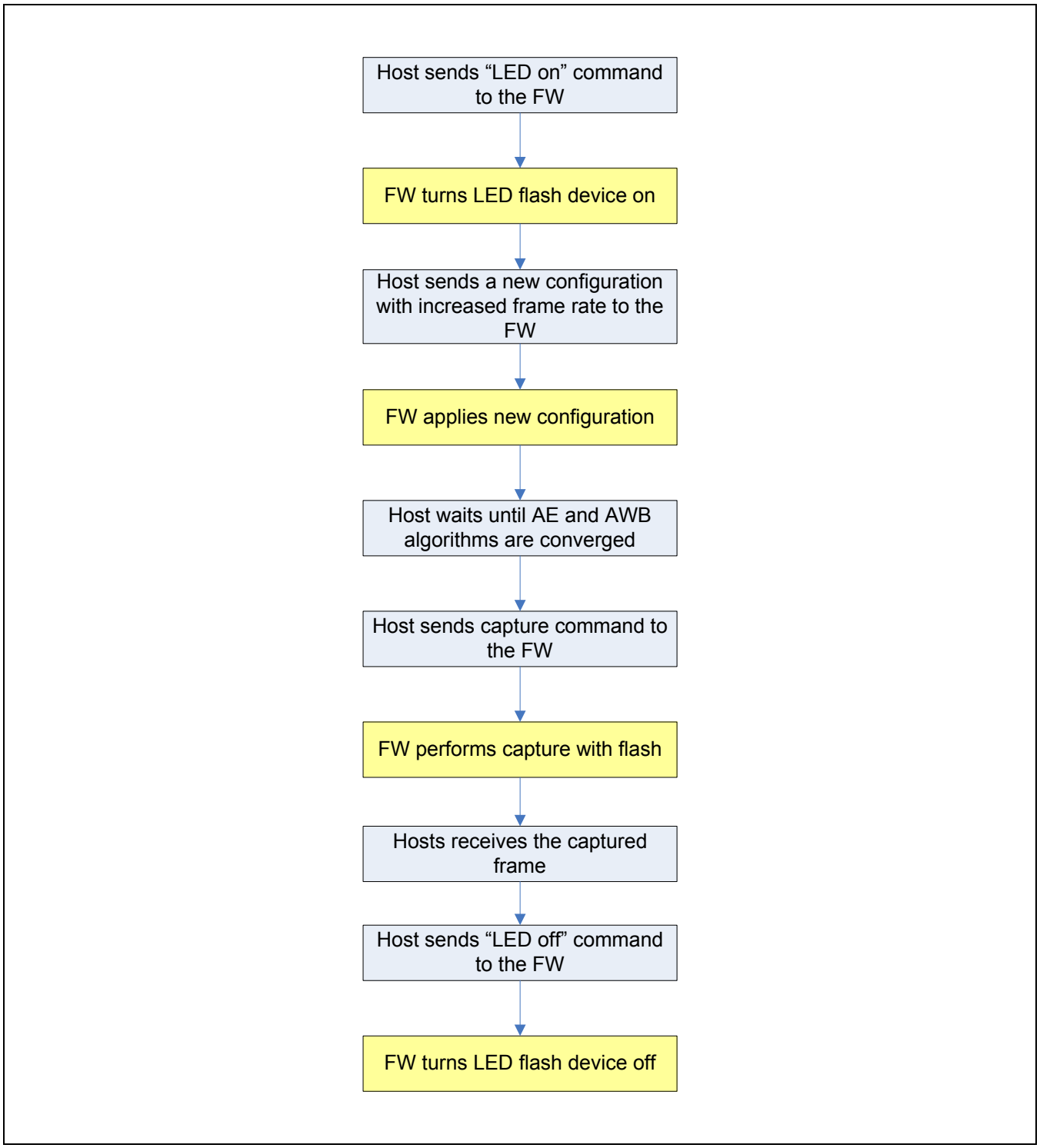


Figure 35. LED Flash Capture Sequence

8.3 IMAGE SIGNAL PROCESSOR

8.3.1 Auto Exposure

The embedded AE control algorithm tracks the change of the luminance in selected windows, and then compares it to the AE target value. The target value varies according to the scene type. The image brightness is adjusted by controlling analog and digital gains and image sensor integration time. The AE algorithm is designed for fast convergence and may adapt very quickly to dynamic illumination changes.

8.3.2 Auto White Balance

The AWB algorithm alters the color components of the image in order to ensure that the white color appears white under all illumination types. The algorithm uses three different statistics channels – one per illumination group (warm, outdoor and general). Each channel filters the image pixels based on R-gain / B-gain plane polygon.

The algorithm includes a scene type detector (six scene types).

8.3.3 Auto Flicker Correction

Flicker may occur when the sensor integration time is not an integer multiple of the frequency of electrical network, for example under a 50Hz or 60Hz fluorescent lamp. The flicker is detected using a dynamic algorithm and adjust the integration time to some limited values to correct the flicker.. If the exposure value is smaller than 1/100 of a second (or 1/120, depending on the lighting frequency), flicker band noise may be seen in an office environment.

8.3.4 Lens Shading Correction

Two different methods of shading correction are used– one uses parabolic shading compensation, and another removes residual effects and is based on grid model. Shading correction dynamically changes based on illumination type.

8.3.5 Color Demosaicking

Each Bayer color pixel from the image sensor is converted into an RGB pixel and the missing color information of a Bayer pixel is derived from the value of adjacent pixels. The algorithm uses several special-purpose approaches such as text and natural modes. Separate decisions are made for each pixel in the image.

8.3.6 Color Correction

Variable color profiles are used for color representation improvement. The decision about the profile is taken based on scene brightness and illumination type. Color correction is done using non-linear transformation, parameterized by 18 coefficients, based on ICC device-link technology.

8.3.7 Despeckle

This algorithm detects and replaces isolated bad pixels and pixel pairs on the raw image data based on their neighbors’ pattern and average.

8.3.8 Denoising

The denoising algorithm implements the "edge-preserving smoothing" algorithm. It averages pixels that are close in value to the central pixel. Neighboring pixels are equalized before averaging.

8.3.9 Gamma Correction

Five Gamma correction tables are used for the following color components:

R, G and B - Contrast and device correction

Y - Luminance correction

UV - For color saturation correction

8.3.10 Image Downscaling

The image from the sensor can be downscaled to an arbitrary size with even X and Y dimensions. The downscaling accuracy ensures any output size up to a 3-5 pixel variance. More precise output sizes can be achieved by cropping.

Among other resolutions, SXGA, SVGA, VGA, QVGA, QQVGA, CIF, and QCIF resolutions are supported.

8.3.11 Special Effects

The special effects may be used to create a Sepia (warm tone), Aqua (cool tone), Monochrome or Negative effect on Image.

8.3.12 Output Formatting

The ISP outputs 8-bit processed video data in the form of standard YUV ITU-R.656/601 or RGB data. Raw sensor data in Bayer format may also be outputted with 8-10 bit accuracy.

8.3.13 Image Properties Controls

The user may dynamically control the following image properties independently - Brightness, Contrast, Saturation, Sharpness, Glamour.

8.3.14 OTP Memory

The S5K5BAF supports a maximum of 48bits OTP memory to store chip identification (36bits) and manufacturing information (12bits). Contact your local SEC FAE for more details.

9 SYSTEM STATE DIAGRAM

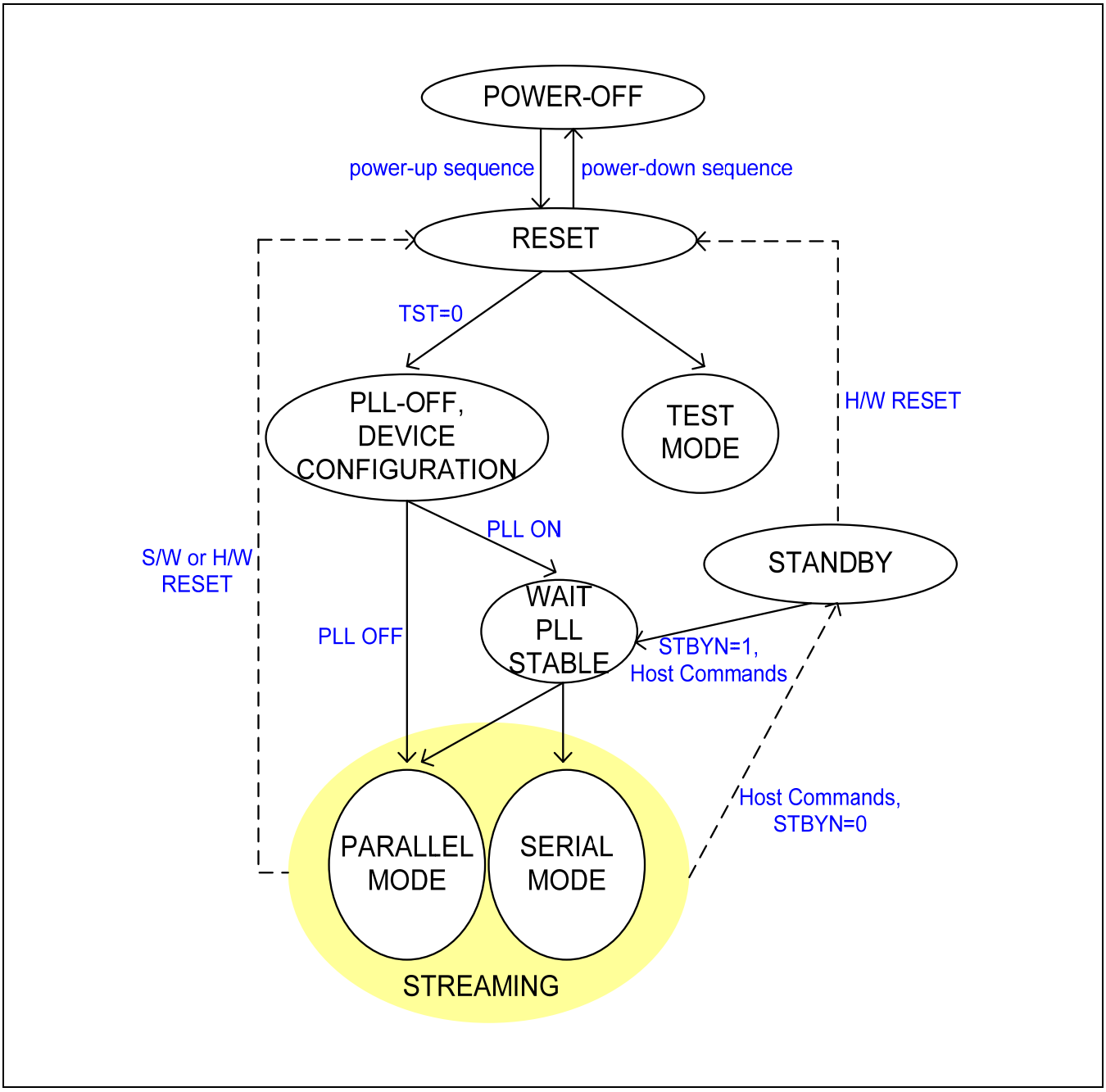


Figure 36. System State Diagram

10 POWER-UP/DOWN SEQUENCE

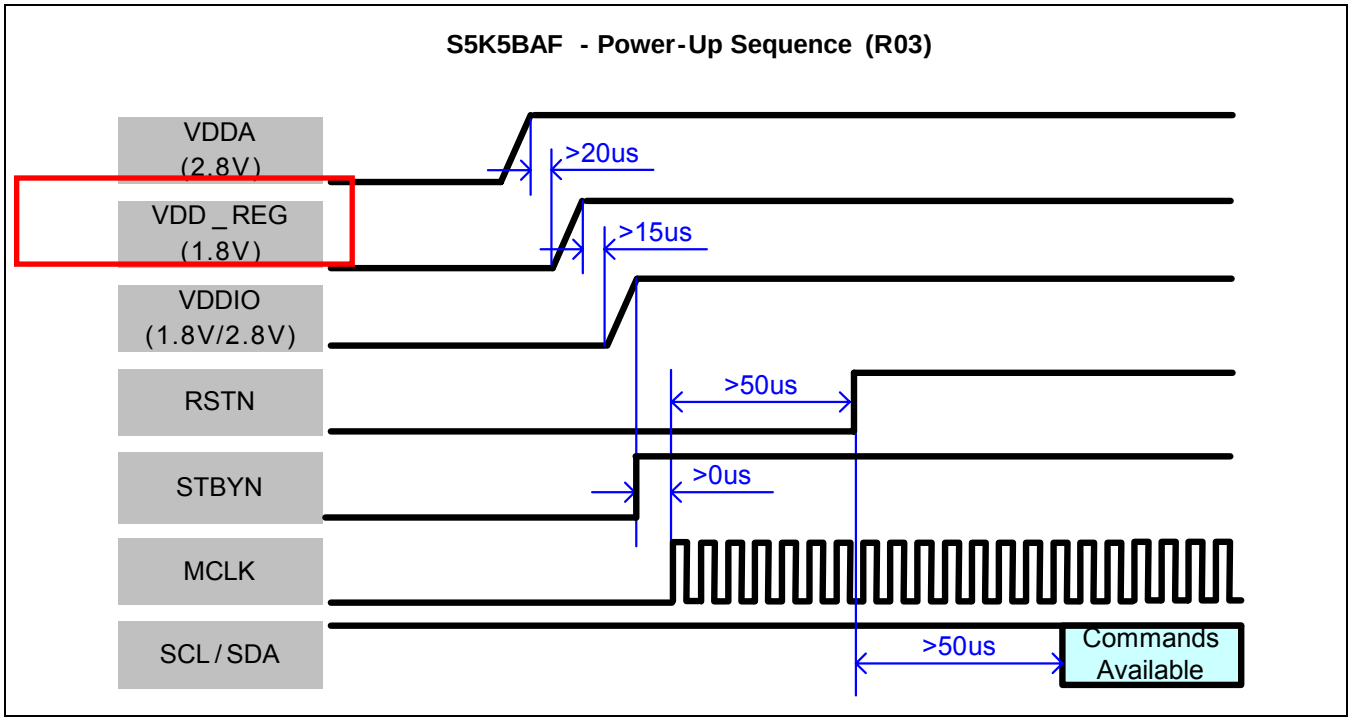


Figure 37. Power-Up Sequence

NOTE: If internal regulator is not used, open VDD_REG and apply VDD15, of which power-up sequence is same to VDD_REG.

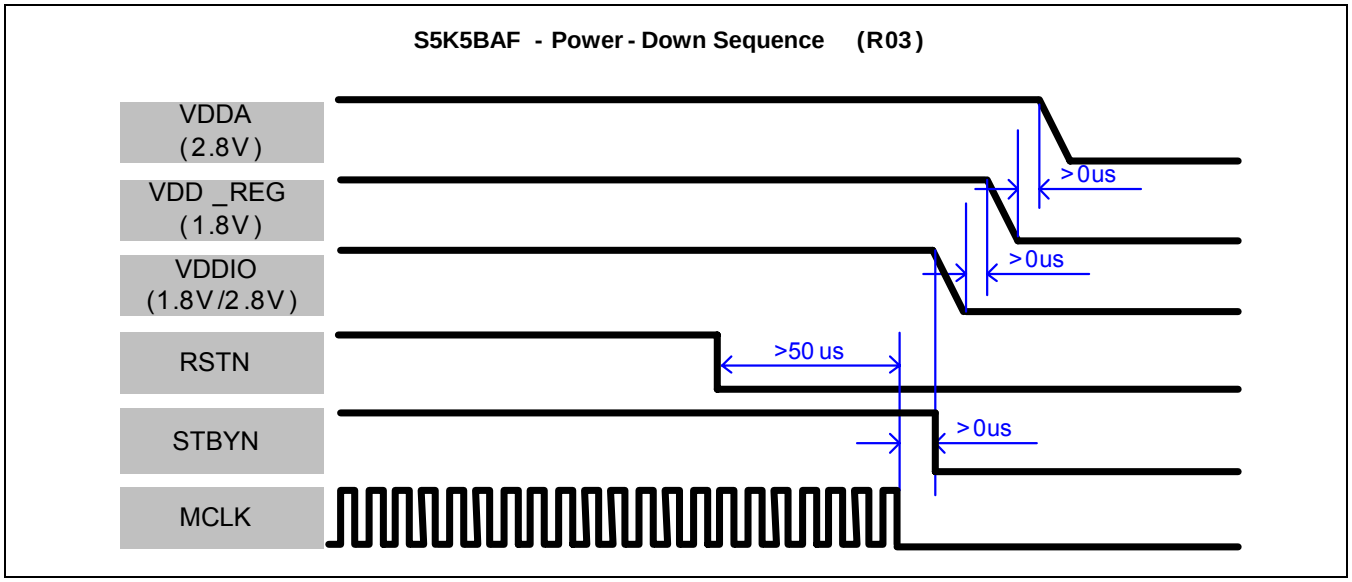


Figure 38. Power-Down Sequence

NOTE: If internal regulator is not used, open VDD_REG and apply VDD15, of which power-down sequence is same to VDD_REG.

11 STANDBY SEQUENCE

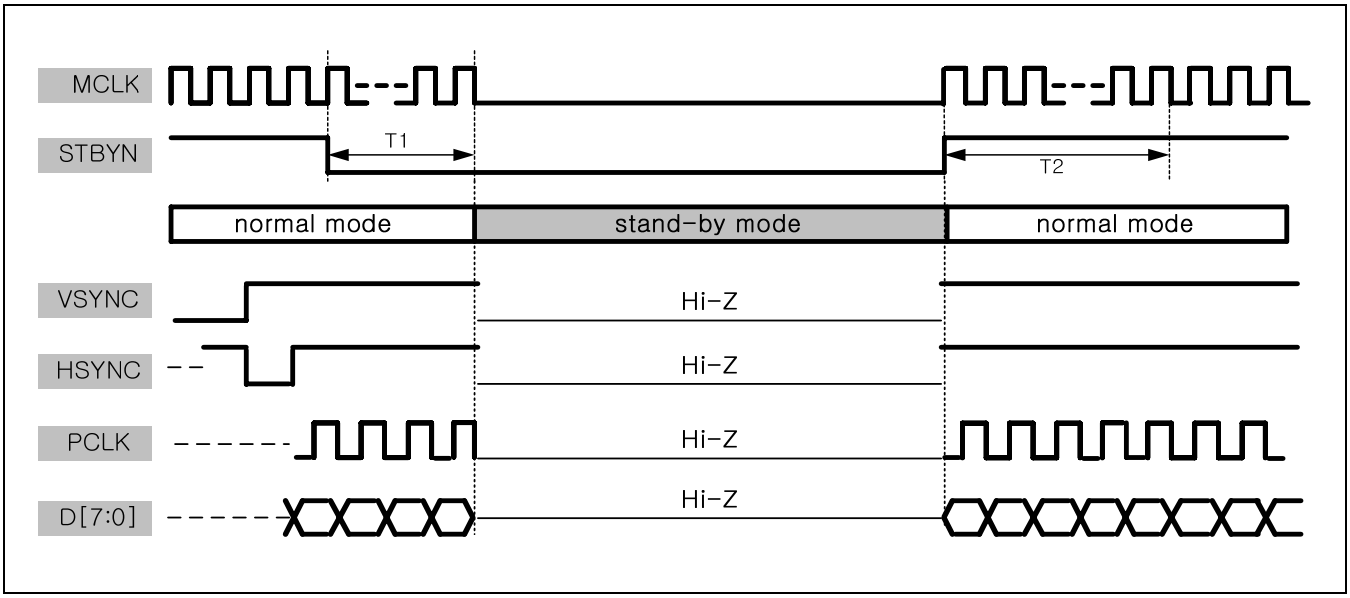


Figure 39. Standby/Wakeup - Sequences

Symbol	Parameter	Min	Max	Unit
T1	STBYN ↓ to Output Tri-state Delay	10000	-	cycle
T2	STBYN ↑ to Valid Output Delay	28000	-	cycle

NOTE:
1. Cycle: MCLK.
2. PLL lock time of 28000 MCLK cycles is required after STBYN goes high.

12 ELECTRICAL CHARACTERISTICS

Table 2. Absolute Maximum Rating

Parameter	Symbol	Value	Unit
I/O Digital Power (2.8V or 1.8V)	V_{DDIO}	-0.3 to 3.8	V
Analog Power (2.8V)	V_{DDA}	-0.3 to 3.8	
Core Digital Power (1.5V)	V_{DDD}	-0.3 to 2.0	
Input Voltage	V_I	-0.3 to 3.8	
Ambient Temperature	T_A	-20 to +60	°C
Storage Temperature	T_S	-40 to +85	

Table 3. DC Characteristics

(V_{DDIO1} = 2.8V ± 0.2V, V_{DDIO2} = 1.8V ± 0.10V , V_{DDD} = 1.5V ± 0.1V, Ta = -20 to + 60 °C)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage	V_{DDA}		2.6	2.8	3.0	V
	V_{DDD}		1.4	1.5	1.6	
	V_{DDIO1}		2.6	2.8	3.0	
	V_{DDIO2}		1.7	1.8	1.9	
High-Level Input Voltage	V_{IH}		0.7* V_{DDIO}	-	-	
Low-Level Input Voltage	V_{IL}		-	-	0.2* V_{DDIO}	
High Level Output Voltage	V_{OH}	Output High Voltage(@Ioh=-100uA)	V_{DDIO}-0.2	-	-	
Low-Level Output Voltage	V_{OL}	Output Low Voltage(@Iol=100uA)	-	-	0.2	
High-Level Input Current	I_{IH}	$V_I = V_{DDIO}$	-10	-	10	uA
		$V_I = V_{DDIO}$ (with Pull-Down)	-	-	72	
Low-Level Input Current	I_{IL}	$V_I = V_{SS}$	-10	-	10	
		$V_I = V_{SS}$ (with Pull-Up)	-72	-	-	
Standby Current	I_{STBY}	STBYN = Low, MCLK = Low (0 lux Illumination)	-	200	250	
Supply Current	I_{DD}	Serial Output Mode @15fps	81	160	180	mA
		Parallel Output Mode @15fps	81	150	180	
Power Consumption	P_{DD}	Serial Output Mode @15fps	120	-	400	mW

Parameter	Symbol	Condition	Min	Typ	Max	Unit
		Parallel Output Mode @15fps	120	-	400	
Input Capacitance	C_{IN}		-	4	8	pF

13 REGISTER DESCRIPTION

Address	Initialization Parameters	Default	Size	Attribute	Description
0x70000130	REG_FWrevision	0x09	1	R	FW revision
0x70000152	REG_FWsenId	0x25BA	2	R	FW sensor ID support
0x700001B8	REG_TC_IPRM_InClockLSBs	0x7D00	2	R/W	Input clock in KHz (lower 16 bit)
0x700001BA	REG_TC_IPRM_InClockMSBs	0x0000	2	R/W	Input clock in KHz (upper 16 bit)
0x700001BC	REG_TC_IPRM_PllFreqDiv4	0x1F40	2	R/W	Reserved
0x700001BE	REG_TC_IPRM_AddHeader	0x0000	2	R/W	Reserved
0x700001C0	REG_TC_IPRM_ValidVActiveLow	0x0000	2	R/W	Reserved
0x700001C2	REG_TC_IPRM_SenI2CAdr	0x0011	2	R/W	Reserved
0x700001C4	REG_TC_IPRM_MI2CDrSclMan	0x0001	2	R/W	Reserved
0x700001C6	REG_TC_IPRM_UseNPviClocks	0x0001	2	R/W	Number of PLL configurations to be computed (0-2)
0x700001C8	REG_TC_IPRM_UseNMipiClocks	0x0000	2	R/W	Number of MIPI configurations to be computed (0-2) Total sum of UseNPviClocks and UseNMipiClocks cannot be greater than 3 UseNPviClocks and UseNMipiClocks are also indexes which determin what is used among following clock sets.
0x700001CA	REG_TC_IPRM_bBlockInternalPllCalc	0x0000	2	R/W	Use external PLL settings rather than internal FW calculation. That is, If this is set, then PLL calculation of FW is prohibited.
0x700001CC	REG_TC_IPRM_OpClk4KHz_0	0x0000	1FBD	R/W	First system clock frequency in KHz divided by 4
0x700001CE	REG_TC_IPRM_MinOutRate4KHz_0	0x1770	0FDF	R/W	Minimal output rate of first clock in KHz divided by 4
0x700001D0	REG_TC_IPRM_MaxOutRate4KHz_0	0x1F40	1FBD	R/W	Maximal output rate of first clock in KHz divided by 4
0x700001D2	REG_TC_IPRM_OpClk4KHz_1	0x1770	2	R/W	Second system clock frequency in KHz divided by 4
0x700001D4	REG_TC_IPRM_MinOutRate4KHz_1	0x1770	2	R/W	Minimal output rate of second clock in KHz divided by 4
0x700001D6	REG_TC_IPRM_MaxOutRate4KHz_1	0x2328	2	R/W	Maximal output rate of second clock in KHz divided by 4
0x700001D8	REG_TC_IPRM_OpClk4KHz_2	0x0BB8	2	R/W	Third system clock frequency in KHz divided by 4
0x700001DA	REG_TC_IPRM_MinOutRate4KHz_2	0x05DC	2	R/W	Minimal output rate of third clock in KHz divided by 4
0x700001DC	REG_TC_IPRM_MaxOutRate4KHz_2	0x1770	2	R/W	Maximal output rate of third clock in KHz divided by 4

Address	Initialization Parameters	Default	Size	Attribute	Description
0x700001DE	REG_TC_IPRM_UseRegsAPI	0x0001	2	R/W	1: Use Register I/F
0x700001E0	REG_TC_IPRM_InitParamsUpdated	0x0000	2	R/W	Update values in FW and invoke FW initialization
0x700001E2	REG_TC_IPRM_ErrorInfo	0x0000	2	R	Error code received from FW (0: no error) This Error occurs when F/W failed to find PLL setting for input value.
0x700001E4	REG_TC_UserBrightness	0x0000	2	R/W	Control brightness value
0x700001E6	REG_TC_UserContrast	0x0000	2	R/W	Control contrast value
0x700001E8	REG_TC_UserSaturation	0x0000	2	R/W	Control saturation value
0x700001EA	REG_TC_UserSharpBlur	0x0000	2	R/W	Control sharpness value
0x700001EC	REG_TC_UserGlamour	0x0000	2	R/W	Control glamour value
0x700001EE	REG_TC_GP_SpecialEffects	0x0000	2	R/W	Special effects selection
0x700001F0	REG_TC_GP_EnablePreview	0x0000	2	R/W	Enable/ disable preview output
0x700001F2	REG_TC_GP_EnablePreviewChanged	0x0000	2	R/W	Synchronize FW with Enable preview request
0x700001F4	REG_TC_GP_EnableCapture	0x0000	2	R/W	Invoke capture request
0x700001F6	REG_TC_GP_EnableCaptureChanged	0x0000	2	R/W	Synchronize FW with capture request
0x700001F8	REG_TC_GP_NewConfigSync	0x0000	2	R/W	Set this flag when sending a new configuration. The FW clears the flag after a configuration is applied.
0x700001FA	REG_TC_GP_PrevReqInputWidth	0x0640	2	R/W	Preview sensor input window width: Equal or greater than output width and up to 1600
0x700001FC	REG_TC_GP_PrevReqInputHeight	0x04B0	2	R/W	Preview sensor input window height: Equal or greater than output height and up to 1200
0x700001FE	REG_TC_GP_PrevInputWidthOfs	0x0000	2	R/W	Preview sensor input window X offset
0x70000200	REG_TC_GP_PrevInputHeightOfs	0x0000	2	R/W	Preview sensor input window Y offset
0x70000202	REG_TC_GP_CapReqInputWidth	0x0640	2	R/W	Capture sensor input window width: Equal or greater than output width and up to 1600
0x70000204	REG_TC_GP_CapReqInputHeight	0x04B0	2	R/W	Capture sensor input window height: Equal or greater than output height and up to 1200
0x70000206	REG_TC_GP_CapInputWidthOfs	0x0000	2	R/W	Capture sensor input window X offset
0x70000208	REG_TC_GP_CapInputHeightOfs	0x0000	2	R/W	Capture sensor input window Y offset
0x7000020A	REG_TC_GP_PrevZoomReqInputWidth	0x0640	2	R/W	Preview output crop window width: Equal or greater than output width and up to 1600
0x7000020C	REG_TC_GP_PrevZoomReqInput	0x04B0	2	R/W	Preview output crop window height:

Address	Initialization Parameters	Default	Size	Attribute	Description
	Height				Equal or greater than output height and up to 1200
0x7000020E	REG_TC_GP_PrevZoomReqInputWidthOfs	0x0000	2	R/W	Preview output crop window X offset
0x70000210	REG_TC_GP_PrevZoomReqInputHeightOfs	0x0000	2	R/W	Preview output crop window Y offset
0x70000212	REG_TC_GP_CapZoomReqInputWidth	0x0640	2	R/W	Capture output crop window width: Equal or greater than output width and up to 1600
0x70000214	REG_TC_GP_CapZoomReqInputHeight	0x04B0	2	R/W	Capture output crop window height: Equal or greater than output height and up to 1200
0x70000216	REG_TC_GP_CapZoomReqInputWidthOfs	0x0000	2	R/W	Capture output crop window X offset
0x70000218	REG_TC_GP_CapZoomReqInputHeightOfs	0x0000	2	R/W	Capture output crop window Y offset
0x7000021A	REG_TC_GP_InputsChangeRequest	0x0000	2	R/W	Synchronize FW with input values
0x7000021C	REG_TC_GP_ActivePrevConfig	0x0000	2	R/W	Index number of active preview configuration
0x7000021E	REG_TC_GP_PrevConfigChanged	0x0000	2	R/W	Synchronize FW with new preview configuration
0x70000220	REG_TC_GP_PrevOpenAfterChange	0x0001	2	R/W	A flag that signals whether, after the configuration change, the output should be enabled or not
0x70000222	REG_TC_GP_ErrorPrevConfig	0x0000	2	R	Error code received from FW for preview calculation (0: no error)
0x70000224	REG_TC_GP_ActiveCapConfig	0x0000	2	R/W	Index number of active capture configuration
0x70000226	REG_TC_GP_CapConfigChanged	0x0000	2	R/W	Synchronize FW with new capture configuration
0x70000228	REG_TC_GP_ErrorCapConfig	0x0000	2	R	Error code received from FW for capture calculation (0: no error)
0x7000022A	REG_TC_GP_PrevConfigBypassChanged	0x0000	2	R/W	Synchronize FW with preview configuration bypass/ usage request
0x7000022C	REG_TC_GP_CapConfigBypassChanged	0x0000	2	R/W	Synchronize FW with capture configuration bypass/ usage request
0x7000022E	REG_TC_GP_SleepMode	0x0000	2	R/W	Set sleep mode (1: sleep, 0: wake-up)
0x70000230	REG_TC_GP_SleepModeChanged	0x0000	2	R/W	Synchronize FW with sleep mode change
0x70000232	REG_TC_GP_SRA_AddLow	0x0000	2	R/W	Reserved
0x70000234	REG_TC_GP_SRA_AddHigh	0x0000	2	R/W	Reserved
0x70000236	REG_TC_GP_SRA_AccessType	0x0000	2	R/W	Reserved

Address	Initialization Parameters	Default	Size	Attribute	Description
0x70000238	REG_TC_GP_SRA_Changed	0x0000	2	R/W	Reserved
0x7000023A	REG_TC_GP_PrevMinFrTimeMsecMult10	0x0000	2	R	Get actual maximal preview frame rate in 0.1 mSec units
0x7000023C	REG_TC_GP_PrevOutKHzRate	0x0000	2	R	Get actual preview output rate in KHz
0x7000023E	REG_TC_GP_CapMinFrTimeMsecMult10	0x0000	2	R	Get actual maximal capture frame rate in 0.1 mSec units
0x70000240	REG_TC_GP_CapOutKHzRate	0x0000	2	R	Get actual capture output rate in KHz
0x70000242	REG_0TC_PCFG_usWidth	0x0640	2	R/W	Output width (Up to 1600 in increments of 2)
0x70000244	REG_0TC_PCFG_usHeight	0x04B0	2	R/W	Output height (Up to 1200 in increments of 2)

0x70000246	REG_0TC_PCFG_Format	0x0005	2	R/W	Output format:
					TC_FORMAT_RGB565 = 0,
					TC_FORMAT_RGB888 = 1,
					TC_FORMAT_FULL_YUV = 5, // YUV422 0-255
					TC_FORMAT_CROPPED_YUV = 6, // YUV422 16-240
					TC_FORMAT_BAYER = 7, // Bayer format, before ISP chain

0x70000248	REG_0TC_PCFG_usMaxOut4KHzRate	0x1770	2	R/W	Maximal output rate in KHz
0x7000024A	REG_0TC_PCFG_usMinOut4KHzRate	0x05DC	2	R/W	Minimal output rate in KHz
0x7000024C	REG_0TC_PCFG_PVIMask	0x0042	2	R/W	PVI configuration flags
0x7000024E	REG_0TC_PCFG_uClockInd	0x0000	2	R/W	System clock index (1-3)
0x70000250	REG_0TC_PCFG_usFrTimeType	0x0000	2	R/W	Frame rate type: TC_FR_TIME_DYNAMIC = 0, TC_FR_TIME_FIXED_NOT_ACCURATE = 1, TC_FR_TIME_FIXED_ACCURATE = 2
0x70000252	REG_0TC_PCFG_FrRateQualityType	0x0000	2	R/W	Frame rate quality: TC_FRVSQ_DYNAMIC = 0, TC_FRVSQ_BEST_FRRATE = 1, TC_FRVSQ_BEST_QUALITY = 2
0x70000254	REG_0TC_PCFG_usMaxFrTimeMsecMult10	0x1964	2	R/W	Required frame time for fixed FR / maximal frame time for dynamic FR [333 – 6500] (Units are in 0.1 ms) (For example, 333 for 33.3 ms)
0x70000256	REG_0TC_PCFG_usMinFrTimeMsecMult10	0x0000	2	R/W	Minimal frame time for dynamic FR. Not valid for fixed FR [333 – 6500] (Units are in 0.1 ms)
0x70000258	REG_0TC_PCFG_sSaturation	0x0000	2	R/W	Device correction saturation control
0x7000025A	REG_0TC_PCFG_sSharpBlur	0x0000	2	R/W	Device correction sharpness control

Address	Initialization Parameters	Default	Size	Attribute	Description
0x7000025C	REG_0TC_PCFG_sGlamour	0x0000	2	R/W	Device correction glamour control
0x7000025E	REG_0TC_PCFG_sColorTemp	0x0000	2	R/W	Device correction color temperature control
0x70000260	REG_0TC_PCFG_uDeviceGammaIndex	0x0000	2	R/W	Device correction Gamma table index
0x70000262	REG_0TC_PCFG_uPrevMirror	0x0000	2	R/W	Preview mirror mode (X/Y) - Bit mask
0x70000264	REG_0TC_PCFG_uCaptureMirror	0x0000	2	R/W	Capture mirror mode (X/Y) - Bit mask
0x70000266	REG_0TC_PCFG_uRotation	0x0000	2	R/W	Capture rotation mode
0x70000268	REG_1TC_PCFG_usWidth	0x0400	2	R/W	Output width (Up to 1600 in increments of 2)
0x7000026A	REG_1TC_PCFG_usHeight	0x0300	2	R/W	Output height (Up to 1200 in increments of 2)

0x7000026C	REG_1TC_PCFG_Format	0x0005	2	R/W	Output format:
					TC_FORMAT_RGB565 = 0,
					TC_FORMAT_RGB888 = 1,
					TC_FORMAT_FULL_YUV = 5, // YUV422 0-255
					TC_FORMAT_CROPPED_YUV = 6, // YUV422 16-240
					TC_FORMAT_BAYER = 7, // Bayer format, before ISP chain

0x7000026E	REG_1TC_PCFG_usMaxOut4KHzRate	0x1770	2	R/W	Maximal output rate in KHz
0x70000270	REG_1TC_PCFG_usMinOut4KHzRate	0x05DC	2	R/W	Minimal output rate in KHz
0x70000272	REG_1TC_PCFG_PVIMask	0x0042	2	R/W	PVI configuration flags
0x70000274	REG_1TC_PCFG_uClockInd	0x0000	2	R/W	System clock index (1-3)
0x70000276	REG_1TC_PCFG_usFrTimeType	0x0000	2	R/W	Frame rate type: TC_FR_TIME_DYNAMIC = 0, TC_FR_TIME_FIXED_NOT_ACCURATE = 1, TC_FR_TIME_FIXED_ACCURATE = 2
0x70000278	REG_1TC_PCFG_FrRateQualityType	0x0000	2	R/W	Frame rate quality: TC_FRVSQ_DYNAMIC = 0, TC_FRVSQ_BEST_FRRATE = 1, TC_FRVSQ_BEST_QUALITY = 2
0x7000027A	REG_1TC_PCFG_usMaxFrTimeMsecMult10	0x1964	2	R/W	Required frame time for fixed FR / maximal frame time for dynamic FR [333 – 6500] (Units are in 0.1 ms) (For example, 333 for 33.3 ms)
0x7000027C	REG_1TC_PCFG_usMinFrTimeMsecMult10	0x0000	2	R/W	Minimal frame time for dynamic FR. Not valid for fixed FR [333 – 6500] (Units are in 0.1 ms)
0x7000027E	REG_1TC_PCFG_sSaturation	0x0000	2	R/W	Device correction saturation control

Address	Initialization Parameters	Default	Size	Attribute	Description
0x70000280	REG_1TC_PCFG_sSharpBlur	0x0000	2	R/W	Device correction sharpness control
0x70000282	REG_1TC_PCFG_sGlamour	0x0000	2	R/W	Device correction glamour control
0x70000284	REG_1TC_PCFG_sColorTemp	0x0000	2	R/W	Device correction color temperature control
0x70000286	REG_1TC_PCFG_uDeviceGammaIndex	0x0000	2	R/W	Device correction Gamma table index
0x70000288	REG_1TC_PCFG_uPrevMirror	0x0000	2	R/W	Preview mirror mode (X/Y) - Bit mask
0x7000028A	REG_1TC_PCFG_uCaptureMirror	0x0000	2	R/W	Capture mirror mode (X/Y) - Bit mask
0x7000028C	REG_1TC_PCFG_uRotation	0x0000	2	R/W	Capture rotation mode
0x7000028E	REG_2TC_PCFG_usWidth	0x0320	2	R/W	Output width (Up to 1600 in increments of 2)
0x70000290	REG_2TC_PCFG_usHeight	0x0258	2	R/W	Output height (Up to 1200 in increments of 2)

0x70000292	REG_2TC_PCFG_Format	0x0005	2	R/W	Output format:
					TC_FORMAT_RGB565 = 0,
					TC_FORMAT_RGB888 = 1,
					TC_FORMAT_FULL_YUV = 5, // YUV422 0-255
					TC_FORMAT_CROPPED_YUV = 6, // YUV422 16-240
					TC_FORMAT_BAYER = 7, // Bayer format, before ISP chain

0x70000294	REG_2TC_PCFG_usMaxOut4KHzRate	0x1770	2	R/W	Maximal output rate in KHz
0x70000296	REG_2TC_PCFG_usMinOut4KHzRate	0x05DC	2	R/W	Minimal output rate in KHz
0x70000298	REG_2TC_PCFG_PVIMask	0x0042	2	R/W	PVI configuration flags
0x7000029A	REG_2TC_PCFG_uClockInd	0x0000	2	R/W	System clock index (1-3)
0x7000029C	REG_2TC_PCFG_usFrTimeType	0x0000	2	R/W	Frame rate type: TC_FR_TIME_DYNAMIC = 0, TC_FR_TIME_FIXED_NOT_ACCURATE = 1, TC_FR_TIME_FIXED_ACCURATE = 2
0x7000029E	REG_2TC_PCFG_FrRateQualityType	0x0000	2	R/W	Frame rate quality: TC_FRVSQ_DYNAMIC = 0, TC_FRVSQ_BEST_FRRATE = 1, TC_FRVSQ_BEST_QUALITY = 2
0x700002A0	REG_2TC_PCFG_usMaxFrTimeMsecMult10	0x1964	2	R/W	Required frame time for fixed FR / maximal frame time for dynamic FR [333 – 6500] (Units are in 0.1 ms) (For example, 333 for 33.3 ms)
0x700002A2	REG_2TC_PCFG_usMinFrTimeMsecMult10	0x0000	2	R/W	Minimal frame time for dynamic FR. Not valid for fixed FR [333 – 6500] (Units are in 0.1 ms)

Address	Initialization Parameters	Default	Size	Attribute	Description
0x700002A4	REG_2TC_PCFG_sSaturation	0x0000	2	R/W	Device correction saturation control
0x700002A6	REG_2TC_PCFG_sSharpBlur	0x0000	2	R/W	Device correction sharpness control
0x700002A8	REG_2TC_PCFG_sGlamour	0x0000	2	R/W	Device correction glamour control
0x700002AA	REG_2TC_PCFG_sColorTemp	0x0000	2	R/W	Device correction color temperature control
0x700002AC	REG_2TC_PCFG_uDeviceGammaIndex	0x0000	2	R/W	Device correction Gamma table index
0x700002AE	REG_2TC_PCFG_uPrevMirror	0x0000	2	R/W	Preview mirror mode (X/Y) - Bit mask
0x700002B0	REG_2TC_PCFG_uCaptureMirror	0x0000	2	R/W	Capture mirror mode (X/Y) - Bit mask
0x700002B2	REG_2TC_PCFG_uRotation	0x0000	2	R/W	Capture rotation mode
0x700002B4	REG_3TC_PCFG_usWidth	0x0280	2	R/W	Output width (Up to 1600 in increments of 2)
0x700002B6	REG_3TC_PCFG_usHeight	0x01E0	2	R/W	Output height (Up to 1200 in increments of 2)

0x700002B8	REG_3TC_PCFG_Format	0x0005	2	R/W	Output format:
					TC_FORMAT_RGB565 = 0,
					TC_FORMAT_RGB888 = 1,
					TC_FORMAT_FULL_YUV = 5, // YUV422 0-255
					TC_FORMAT_CROPPED_YUV = 6, // YUV422 16-240
					TC_FORMAT_BAYER = 7, // Bayer format, before ISP chain

0x700002BA	REG_3TC_PCFG_usMaxOut4KHzRate	0x1770	2	R/W	Maximal output rate in KHz
0x700002BC	REG_3TC_PCFG_usMinOut4KHzRate	0x05DC	2	R/W	Minimal output rate in KHz
0x700002BE	REG_3TC_PCFG_PVIMask	0x0042	2	R/W	PVI configuration flags
0x700002C0	REG_3TC_PCFG_uClockInd	0x0000	2	R/W	System clock index (1-3)
0x700002C2	REG_3TC_PCFG_usFrTimeType	0x0000	2	R/W	Frame rate type: TC_FR_TIME_DYNAMIC = 0, TC_FR_TIME_FIXED_NOT_ACCURATE = 1, TC_FR_TIME_FIXED_ACCURATE = 2
0x700002C4	REG_3TC_PCFG_FrRateQualityType	0x0000	2	R/W	Frame rate quality: TC_FRVSQ_DYNAMIC = 0, TC_FRVSQ_BEST_FRRATE = 1, TC_FRVSQ_BEST_QUALITY = 2
0x700002C6	REG_3TC_PCFG_usMaxFrTimeMsecMult10	0x1964	2	R/W	Required frame time for fixed FR / maximal frame time for dynamic FR [333 – 6500] (Units are in 0.1 ms) (For example, 333 for 33.3 ms)

Address	Initialization Parameters	Default	Size	Attribute	Description
0x700002C8	REG_3TC_PCFG_usMinFrTimeMsecMult10	0x0000	2	R/W	Minimal frame time for dynamic FR. Not valid for fixed FR [333 – 6500] (Units are in 0.1 ms)
0x700002CA	REG_3TC_PCFG_sSaturation	0x0000	2	R/W	Device correction saturation control
0x700002CC	REG_3TC_PCFG_sSharpBlur	0x0000	2	R/W	Device correction sharpness control
0x700002CE	REG_3TC_PCFG_sGlamour	0x0000	2	R/W	Device correction glamour control
0x700002D0	REG_3TC_PCFG_sColorTemp	0x0000	2	R/W	Device correction color temperature control
0x700002D2	REG_3TC_PCFG_uDeviceGammaIndex	0x0000	2	R/W	Device correction Gamma table index
0x700002D4	REG_3TC_PCFG_uPrevMirror	0x0000	2	R/W	Preview mirror mode (X/Y) - Bit mask
0x700002D6	REG_3TC_PCFG_uCaptureMirror	0x0000	2	R/W	Capture mirror mode (X/Y) - Bit mask
0x700002D8	REG_3TC_PCFG_uRotation	0x0000	2	R/W	Capture rotation mode
0x700002DA	REG_4TC_PCFG_usWidth	0x0140	2	R/W	Output width (Up to 1600 in increments of 2)
0x700002DC	REG_4TC_PCFG_usHeight	0x00F0	2	R/W	Output height (Up to 1200 in increments of 2)

0x700002DE	REG_4TC_PCFG_Format	0x0005	2	R/W	Output format:
					TC_FORMAT_RGB565 = 0,
					TC_FORMAT_RGB888 = 1,
					TC_FORMAT_FULL_YUV = 5, // YUV422 0-255
					TC_FORMAT_CROPPED_YUV = 6, // YUV422 16-240
					TC_FORMAT_BAYER = 7, // Bayer format, before ISP chain

0x700002E0	REG_4TC_PCFG_usMaxOut4KHzRate	0x1770	2	R/W	Maximal output rate in KHz
0x700002E2	REG_4TC_PCFG_usMinOut4KHzRate	0x05DC	2	R/W	Minimal output rate in KHz
0x700002E4	REG_4TC_PCFG_PVIMask	0x0042	2	R/W	PVI configuration flags
0x700002E6	REG_4TC_PCFG_uClockInd	0x0000	2	R/W	System clock index (1-3)
0x700002E8	REG_4TC_PCFG_usFrTimeType	0x0000	2	R/W	Frame rate type: TC_FR_TIME_DYNAMIC = 0, TC_FR_TIME_FIXED_NOT_ACCURATE = 1, TC_FR_TIME_FIXED_ACCURATE = 2
0x700002EA	REG_4TC_PCFG_FrRateQualityType	0x0000	2	R/W	Frame rate quality: TC_FRVSQ_DYNAMIC = 0, TC_FRVSQ_BEST_FRRATE = 1, TC_FRVSQ_BEST_QUALITY = 2

Address	Initialization Parameters	Default	Size	Attribute	Description
0x700002EC	REG_4TC_PCFG_usMaxFrTimeMsecMult10	0x1964	2	R/W	Required frame time for fixed FR / maximal frame time for dynamic FR [333 – 6500] (Units are in 0.1 ms) (For example, 333 for 33.3 ms)
0x700002EE	REG_4TC_PCFG_usMinFrTimeMsecMult10	0x0000	2	R/W	Minimal frame time for dynamic FR. Not valid for fixed FR [333 – 6500] (Units are in 0.1 ms)
0x700002F0	REG_4TC_PCFG_sSaturation	0x0000	2	R/W	Device correction saturation control
0x700002F2	REG_4TC_PCFG_sSharpBlur	0x0000	2	R/W	Device correction sharpness control
0x700002F4	REG_4TC_PCFG_sGlamour	0x0000	2	R/W	Device correction glamour control
0x700002F6	REG_4TC_PCFG_sColorTemp	0x0000	2	R/W	Device correction color temperature control
0x700002F8	REG_4TC_PCFG_uDeviceGammaIndex	0x0000	2	R/W	Device correction Gamma table index
0x700002FA	REG_4TC_PCFG_uPrevMirror	0x0000	2	R/W	Preview mirror mode (X/Y) - Bit mask
0x700002FC	REG_4TC_PCFG_uCaptureMirror	0x0000	2	R/W	Capture mirror mode (X/Y) - Bit mask
0x700002FE	REG_4TC_PCFG_uRotation	0x0000	2	R/W	Capture rotation mode
0x70000300	REG_TC_TCFG_P_ClkCfgMinTimeMilliMult100	0x0000	2		
0x70000302	REG_0TC_CCFG_uCaptureMode	0x0000	2	R/W	Capture type: 0 - Regular
0x70000304	REG_0TC_CCFG_usWidth	0x0640	2	R/W	Capture width (Up to 1600 in increments of 2)
0x70000306	REG_0TC_CCFG_usHeight	0x04B0	2	R/W	Capture height (Up to 1200 in increments of 2)
0x70000308	REG_0TC_CCFG_Format	0x0009	2	R/W	Capture format
0x7000030A	REG_0TC_CCFG_usMaxOut4KHzRate	0x1770	2	R/W	Maximal output rate in KHz
0x7000030C	REG_0TC_CCFG_usMinOut4KHzRate	0x05DC	2	R/W	Minimal output rate in KHz
0x7000030E	REG_0TC_CCFG_PVIMask	0x0042	2	R/W	PVI configuration flags
0x70000310	REG_0TC_CCFG_uClockInd	0x0000	2	R/W	System clock index (1-3)
0x70000312	REG_0TC_CCFG_usFrTimeType	0x0000	2	R/W	Frame rate type: TC_FR_TIME_DYNAMIC = 0, TC_FR_TIME_FIXED_NOT_ACCURATE = 1, TC_FR_TIME_FIXED_ACCURATE = 2
0x70000314	REG_0TC_CCFG_FrRateQualityType	0x0002	2	R/W	Frame rate quality: TC_FRVSQ_DYNAMIC = 0, TC_FRVSQ_BEST_FRRATE = 1, TC_FRVSQ_BEST_QUALITY = 2

Address	Initialization Parameters	Default	Size	Attribute	Description
0x70000316	REG_0TC_CCFG_usMaxFrTimeMsecMult10	0x1964	2	R/W	Required frame time for fixed FR / maximal frame time for dynamic FR [333 – 6500] (Units are in 0.1 ms) (For example, 333 for 33.3 ms)
0x70000318	REG_0TC_CCFG_usMinFrTimeMsecMult10	0x0000	2	R/W	Minimal frame time for dynamic FR. Not valid for fixed FR [333 – 6500] (Units are in 0.1 ms)
0x7000031A	REG_0TC_CCFG_sSaturation	0x0000	2	R/W	Device correction saturation control
0x7000031C	REG_0TC_CCFG_sSharpBlur	0x0000	2	R/W	Device correction sharpness control
0x7000031E	REG_0TC_CCFG_sGlamour	0x0000	2	R/W	Device correction glamour control
0x70000320	REG_0TC_CCFG_sColorTemp	0x0000	2	R/W	Device correction color temperature control
0x70000322	REG_0TC_CCFG_uDeviceGammaIndex	0x0000	2	R/W	Device correction Gamma table index
0x70000324	REG_1TC_CCFG_uCaptureMode	0x0000	2	R/W	Capture type: 0 - Regular
0x70000326	REG_1TC_CCFG_usWidth	0x0500	2	R/W	Capture width (Up to 1600 in increments of 2)
0x70000328	REG_1TC_CCFG_usHeight	0x03C0	2	R/W	Capture height (Up to 1200 in increments of 2)
0x7000032A	REG_1TC_CCFG_Format	0x0009	2	R/W	Capture format
0x7000032C	REG_1TC_CCFG_usMaxOut4KHzRate	0x1770	2	R/W	Maximal output rate in KHz
0x7000032E	REG_1TC_CCFG_usMinOut4KHzRate	0x05DC	2	R/W	Minimal output rate in KHz
0x70000330	REG_1TC_CCFG_PVIMask	0x0042	2	R/W	PVI configuration flags
0x70000332	REG_1TC_CCFG_uClockInd	0x0000	2	R/W	System clock index (1-3)
0x70000334	REG_1TC_CCFG_usFrTimeType	0x0000	2	R/W	Frame rate type: TC_FR_TIME_DYNAMIC = 0, TC_FR_TIME_FIXED_NOT_ACCURATE = 1, TC_FR_TIME_FIXED_ACCURATE = 2
0x70000336	REG_1TC_CCFG_FrRateQualityType	0x0002	2	R/W	Frame rate quality: TC_FRVSQ_DYNAMIC = 0, TC_FRVSQ_BEST_FRRATE = 1, TC_FRVSQ_BEST_QUALITY = 2
0x70000338	REG_1TC_CCFG_usMaxFrTimeMsecMult10	0x1964	2	R/W	Required frame time for fixed FR / maximal frame time for dynamic FR [333 – 6500] (Units are in 0.1 ms) (For example, 333 for 33.3 ms)
0x7000033A	REG_1TC_CCFG_usMinFrTimeMsecMult10	0x0000	2	R/W	Minimal frame time for dynamic FR. Not valid for fixed FR [333 – 6500] (Units are in 0.1 ms)
0x7000033C	REG_1TC_CCFG_sSaturation	0x0000	2	R/W	Device correction saturation control

Address	Initialization Parameters	Default	Size	Attribute	Description
0x7000033E	REG_1TC_CCFG_sSharpBlur	0x0000	2	R/W	Device correction sharpness control
0x70000340	REG_1TC_CCFG_sGlamour	0x0000	2	R/W	Device correction glamour control
0x70000342	REG_1TC_CCFG_sColorTemp	0x0000	2	R/W	Device correction color temperature control
0x70000344	REG_1TC_CCFG_uDeviceGammaIndex	0x0000	2	R/W	Device correction Gamma table index
0x70000346	REG_2TC_CCFG_uCaptureMode	0x0000	2	R/W	Capture type: 0 - Regular
0x70000348	REG_2TC_CCFG_usWidth	0x0320	2	R/W	Capture width (Up to 1600 in increments of 2)
0x7000034A	REG_2TC_CCFG_usHeight	0x0258	2	R/W	Capture height (Up to 1200 in increments of 2)
0x7000034C	REG_2TC_CCFG_Format	0x0009	2	R/W	Capture format
0x7000034E	REG_2TC_CCFG_usMaxOut4KHzRate	0x1770	2	R/W	Maximal output rate in KHz
0x70000350	REG_2TC_CCFG_usMinOut4KHzRate	0x05DC	2	R/W	Minimal output rate in KHz
0x70000352	REG_2TC_CCFG_PVIMask	0x0042	2	R/W	PVI configuration flags
0x70000354	REG_2TC_CCFG_uClockInd	0x0000	2	R/W	System clock index (1-3)
0x70000356	REG_2TC_CCFG_usFrTimeType	0x0000	2	R/W	Frame rate type: TC_FR_TIME_DYNAMIC = 0, TC_FR_TIME_FIXED_NOT_ACCURATE = 1, TC_FR_TIME_FIXED_ACCURATE = 2
0x70000358	REG_2TC_CCFG_FrRateQualityType	0x0002	2	R/W	Frame rate quality: TC_FRVSQ_DYNAMIC = 0, TC_FRVSQ_BEST_FRRATE = 1, TC_FRVSQ_BEST_QUALITY = 2
0x7000035A	REG_2TC_CCFG_usMaxFrTimeMsecMult10	0x1964	2	R/W	Required frame time for fixed FR / maximal frame time for dynamic FR [333 – 6500] (Units are in 0.1 ms) (For example, 333 for 33.3 ms)
0x7000035C	REG_2TC_CCFG_usMinFrTimeMsecMult10	0x0000	2	R/W	Minimal frame time for dynamic FR. Not valid for fixed FR [333 – 6500] (Units are in 0.1 ms)
0x7000035E	REG_2TC_CCFG_sSaturation	0x0000	2	R/W	Device correction saturation control
0x70000360	REG_2TC_CCFG_sSharpBlur	0x0000	2	R/W	Device correction sharpness control
0x70000362	REG_2TC_CCFG_sGlamour	0x0000	2	R/W	Device correction glamour control
0x70000364	REG_2TC_CCFG_sColorTemp	0x0000	2	R/W	Device correction color temperature control
0x70000366	REG_2TC_CCFG_uDeviceGammaIndex	0x0000	2	R/W	Device correction Gamma table index
0x70000368	REG_3TC_CCFG_uCaptureMode	0x0000	2	R/W	Capture type: 0 - Regular

Address	Initialization Parameters	Default	Size	Attribute	Description
0x7000036A	REG_3TC_CCFG_usWidth	0x0280	2	R/W	Capture width (Up to 1600 in increments of 2)
0x7000036C	REG_3TC_CCFG_usHeight	0x01E0	2	R/W	Capture height (Up to 1200 in increments of 2)
0x7000036E	REG_3TC_CCFG_Format	0x0009	2	R/W	Capture format
0x70000370	REG_3TC_CCFG_usMaxOut4KHzRate	0x1770	2	R/W	Maximal output rate in KHz
0x70000372	REG_3TC_CCFG_usMinOut4KHzRate	0x05DC	2	R/W	Minimal output rate in KHz
0x70000374	REG_3TC_CCFG_PVIMask	0x0042	2	R/W	PVI configuration flags
0x70000376	REG_3TC_CCFG_uClockInd	0x0000	2	R/W	System clock index (1-3)
0x70000378	REG_3TC_CCFG_usFrTimeType	0x0000	2	R/W	Frame rate type: TC_FR_TIME_DYNAMIC = 0, TC_FR_TIME_FIXED_NOT_ACCURATE = 1, TC_FR_TIME_FIXED_ACCURATE = 2
0x7000037A	REG_3TC_CCFG_FrRateQualityType	0x0002	2	R/W	Frame rate quality: TC_FRVSQ_DYNAMIC = 0, TC_FRVSQ_BEST_FRRATE = 1, TC_FRVSQ_BEST_QUALITY = 2
0x7000037C	REG_3TC_CCFG_usMaxFrTimeMsecMult10	0x1964	2	R/W	Required frame time for fixed FR / maximal frame time for dynamic FR [333 – 6500] (Units are in 0.1 ms) (For example, 333 for 33.3 ms)
0x7000037E	REG_3TC_CCFG_usMinFrTimeMsecMult10	0x0000	2	R/W	Minimal frame time for dynamic FR. Not valid for fixed FR [333 – 6500] (Units are in 0.1 ms)
0x70000380	REG_3TC_CCFG_sSaturation	0x0000	2	R/W	Device correction saturation control
0x70000382	REG_3TC_CCFG_sSharpBlur	0x0000	2	R/W	Device correction sharpness control
0x70000384	REG_3TC_CCFG_sGlamour	0x0000	2	R/W	Device correction glamour control
0x70000386	REG_3TC_CCFG_sColorTemp	0x0000	2	R/W	Device correction color temperature control
0x70000388	REG_3TC_CCFG_uDeviceGammaIndex	0x0000	2	R/W	Device correction Gamma table index
0x7000038A	REG_4TC_CCFG_uCaptureMode	0x0000	2	R/W	Capture type: 0 - Regular
0x7000038C	REG_4TC_CCFG_usWidth	0x0140	2	R/W	Capture width (Up to 1600 in increments of 2)
0x7000038E	REG_4TC_CCFG_usHeight	0x00F0	2	R/W	Capture height (Up to 1200 in increments of 2)
0x70000390	REG_4TC_CCFG_Format	0x0009	2	R/W	Capture format
0x70000392	REG_4TC_CCFG_usMaxOut4KHzRate	0x1770	2	R/W	Maximal output rate in KHz

Address	Initialization Parameters	Default	Size	Attribute	Description
0x70000394	REG_4TC_CCFG_usMinOut4KHzRate	0x05DC	2	R/W	Minimal output rate in KHz
0x70000396	REG_4TC_CCFG_PVIMask	0x0042	2	R/W	PVI configuration flags
0x70000398	REG_4TC_CCFG_uClockInd	0x0000	2	R/W	System clock index (1-3)
0x7000039A	REG_4TC_CCFG_usFrTimeType	0x0000	2	R/W	Frame rate type: TC_FR_TIME_DYNAMIC = 0, TC_FR_TIME_FIXED_NOT_ACCURATE = 1, TC_FR_TIME_FIXED_ACCURATE = 2
0x7000039C	REG_4TC_CCFG_FrRateQualityType	0x0002	2	R/W	Frame rate quality: TC_FRVSQ_DYNAMIC = 0, TC_FRVSQ_BEST_FRRATE = 1, TC_FRVSQ_BEST_QUALITY = 2
0x7000039E	REG_4TC_CCFG_usMaxFrTimeMsecMult10	0x1964	2	R/W	Required frame time for fixed FR / maximal frame time for dynamic FR [333 – 6500] (Units are in 0.1 ms) (For example, 333 for 33.3 ms)
0x700003A0	REG_4TC_CCFG_usMinFrTimeMsecMult10	0x0000	2	R/W	Minimal frame time for dynamic FR. Not valid for fixed FR [333 – 6500] (Units are in 0.1 ms)
0x700003A2	REG_4TC_CCFG_sSaturation	0x0000	2	R/W	Device correction saturation control
0x700003A4	REG_4TC_CCFG_sSharpBlur	0x0000	2	R/W	Device correction sharpness control
0x700003A6	REG_4TC_CCFG_sGlamour	0x0000	2	R/W	Device correction glamour control
0x700003A8	REG_4TC_CCFG_sColorTemp	0x0000	2	R/W	Device correction color temperature control
0x700003AA	REG_4TC_CCFG_uDeviceGammaIndex	0x0000	2	R/W	Device correction Gamma table index
0x700003AC	REG_TC_FLS_Mode	0x0000	2	R/W	Set flash mode: 0: TC_FLASH_DISABLE, 1: TC_FLASH_CONT_ENABLE, // Always on 2: TC_FLASH_PULSE_ENABLE, // Use burst pulse on every capture 3: TC_FLASH_PULSE_AUTO // Sensor controls the Flash status (burst mode)
0x700003AE	REG_TC_FLS_Threshold	0x0050	2	R/W	Set flash activation threshold in normalized brightness units
0x700003B0	REG_TC_FLS_Polarity	0x0001	2	R/W	Set flash device polarity. 1: active high, 0: active low
0x700003B2	REG_TC_FLS_XenonMode	0x0000	2	R/W	Set Xenon flash mode: 0: TC_XENON_DISABLE, 1: TC_XENON_ONE_STROBE, // Use one strobe

Address	Initialization Parameters	Default	Size	Attribute	Description
					2: TC_XENON_PRE_FLASH // Use n strobes for pre-flash and another one, full
0x700003B4	REG_TC_FLS_XenonPreFlashCnt	0x0001	2	R/W	Number of Xenon pre-flash strobes
0x700003B6	REG_SF_USER_LeiLow	0x0000	2	R/W	Set LEI low limit
0x700003B8	REG_SF_USER_LeiHigh	0x0000	2	R/W	Set LEI high limit
0x700003BA	REG_SF_USER_LeiChanged	0x0000	2	R/W	Synchronize FW with LEI limits change
0x700003BC	REG_SF_USER_Exposure	0x0000	2	R/W	Set manual exposure value to low
0x700003BE	REG_SF_USER_ExposureHigh	0x0000	2	R/W	Set manual exposure value to high
0x700003C0	REG_SF_USER_ExposureChanged	0x0000	2	R/W	Synchronize FW with exposure settings change
0x700003C2	REG_SF_USER_TotalGain	0x0000	2	R/W	Set total gain value
0x700003C4	REG_SF_USER_TotalGainChanged	0x0000	2	R/W	Synchronize FW with total gain change
0x700003C6	REG_SF_USER_Rgain	0x0000	2	R/W	Set red gain value
0x700003C8	REG_SF_USER_RgainChanged	0x0000	2	R/W	Synchronize FW with red gain change
0x700003CA	REG_SF_USER_Ggain	0x0000	2	R/W	Set green gain value
0x700003CC	REG_SF_USER_GgainChanged	0x0000	2	R/W	Synchronize FW with green gain change
0x700003CE	REG_SF_USER_Bgain	0x0000	2	R/W	Set blue gain value
0x700003D0	REG_SF_USER_BgainChanged	0x0000	2	R/W	Synchronize FW with blue gain change
0x700003D2	REG_SF_USER_WBgainChanged	0x0000	2	R/W	Synchronize FW with gain change
0x700003D4	REG_SF_USER_FlickerQuant	0x0000	2	R/W	Set flicker quantization: 0: no AFC, 1: 50 Hz, 2: 60 Hz
0x700003D6	REG_SF_USER_FlickerQuantChanged	0x0000	2	R/W	Synchronize FW with flicker quantization change
0x700003D8	REG_SF_USER_GASRAlphaVal	0x0000	2		
0x700003DA	REG_SF_USER_GASRAlphaChanged	0x0000	2		
0x700003DC	REG_SF_USER_GASGAlphaVal	0x0000	2		
0x700003DE	REG_SF_USER_GASGAlphaChanged	0x0000	2		
0x700003E0	REG_SF_USER_GASBAlphaVal	0x0000	2		
0x700003E2	REG_SF_USER_GASBAlphaChanged	0x0000	2		
0x700003EA	REG_SF_USER_aGain	0x0000	2	R/W	Set analog gain value
0x700003EC	REG_SF_USER_aGainChanged	0x0000	2	R/W	Synchronize FW with analog gain change
0x700003EE	REG_SF_USER_dGain	0x0000	2	R/W	Set digital gain value

Address	Initialization Parameters	Default	Size	Attribute	Description
0x700003F0	REG_SF_USER_dGainChanged	0x0000	2	R/W	Synchronize FW with digital gain change
0x700003F2	REG_TC_OIF_EnMipiLanes	0x0000	2	R/W	Number of MIPI lanes (0: PVI, 1: 1 lane MIPI, 2: 2 lane MIPI)
0x700003F4	REG_TC_OIF_EnPackets	0x0000	2	R/W	MIPI configuration bit mask
0x700003F6	REG_TC_OIF_CfgChanged	0x0000	2	R/W	Synchronize FW with output interface configuration change
0x700003F8	REG_TC_DBG_AutoAlgEnBits	0x007F	2	R/W	Auto-algorithms enable/disable: SF_AA_ALL = 0, SF_AA_AE_ACTIVE = 1, SF_AA_DIV_LEI = 2, SF_AA_WB_ACTIVE = 3, SF_AA_USE_WB_FOR_ISP = 4, SF_AA_FLICKER = 5, SF_AA_FIT = 6, SF_AA_WR_HW = 7
0x700003FA	REG_TC_DBG_IspBypass	0x0000	2	R/W	Bypass FW operation
0x700003FC	REG_TC_DBG_ReInitCmd	0x0000	2	R/W	Invoke FW "soft reset"
0x70000468	ConfigChTune_pStTune	0x00000000	4		
0x7000046C	ConfigChTune_usTuneNum	0x0000	2		
0x70000478	lt_uLimitHigh	0x0121	2	R/W	Boundary high
0x7000047A	lt_uLimitLow	0x00DF	2	R/W	Boundary low
0x70000484	lt_uMaxExp1	0x00009C40	4	R/W	Maximal exposure 1 for Capture mode
0x70000488	lt_uMaxExp2	0x0000E848	4	R/W	Maximal exposure 2 for Capture mode
0x7000048C	lt_uCapMaxExp1	0x00009C40	4	R/W	Maximal exposure 1 for Preview mode
0x70000490	lt_uCapMaxExp2	0x0000E848	4	R/W	Maximal exposure 2 for Preview mode
0x70000494	lt_uMaxAnGain1	0x0200	2	R/W	Maximal analog gain1
0x70000496	lt_uMaxAnGain2	0x0500	2	R/W	Maximal analog gain2
0x70000498	lt_uMaxDigGain	0x0200	2	R/W	TBD
0x7000049A	lt_uMinExp	0x000A	2	R/W	Min LEI Value
0x7000049C	lt_uISO	0x0100	2	R/W	Gainoffset value.
0x700004A0	lt_uLeiInit	0x000005DC	4	R/W	Initial value of LEI.
0x700004A4	lt_bUseOptLeiForCapture	0x0000	2	R/W	Flag Register of OptiamlLEI and TargetLEI.
0x700004A6	lt_uCaptureFactor88	0x0100	2	R/W	Capture Weight.

Address	Initialization Parameters	Default	Size	Attribute	Description
0x700004AA	lt_bExactGainComp	0x0001	2		
0x700006CA	seti_uContrastCenter	0x0200	2	R/W	Contrast Center for manual contrast.
0x700006CC	seti_OldStyleBrightness	0x0000	2		
0x700006CE	seti_OldStyleSaturation	0x0000	2		
0x70000B2E	AFC_Default60Hz	0x0001	2	R/W	Default frequency: 1 – 60Hz, 0 – 50Hz.
0x70000B36	AFC_ManualQuant	0x0000	2		
0x70000B38	AFC_AeManual50FlickerTable[0]	0x0301	2		
0x70000B3A	AFC_AeManual50FlickerTable[1]	0x0705	2		
0x70000B3C	AFC_AeManual50FlickerTable[2]	0x0B09	2		
0x70000B3E	AFC_AeManual50FlickerTable[3]	0x0F0D	2		
0x70000B40	AFC_AeManual50FlickerTable[4]	0x1310	2		
0x70000B42	AFC_AeManual50FlickerTable[5]	0x1A16	2		
0x70000B44	AFC_AeManual50FlickerTable[6]	0x2820	2		
0x70000B46	AFC_AeManual50FlickerTable[7]	0x0030	2		
0x70000B48	AFC_AeManual60FlickerTable[0]	0x0201	2		
0x70000B4A	AFC_AeManual60FlickerTable[1]	0x0604	2		
0x70000B4C	AFC_AeManual60FlickerTable[2]	0x0A08	2		
0x70000B4E	AFC_AeManual60FlickerTable[3]	0x0F0C	2		
0x70000B50	AFC_AeManual60FlickerTable[4]	0x1310	2		
0x70000B52	AFC_AeManual60FlickerTable[5]	0x1A16	2		
0x70000B54	AFC_AeManual60FlickerTable[6]	0x2820	2		
0x70000B56	AFC_AeManual60FlickerTable[7]	0x0030	2		
0x70000B94	awbb_GainsInit[0]	0x053C	2		
0x70000B96	awbb_GainsInit[1]	0x0400	2		
0x70000B98	awbb_GainsInit[2]	0x055C	2		
0x70000B9C	awbb_IndoorGrZones_m_BGrid[0]_m_left	0x03CC	2		
0x70000B9E	awbb_IndoorGrZones_m_BGrid[0]_m_right	0x03F9	2		
0x70000BA0	awbb_IndoorGrZones_m_BGrid[1]_m_left	0x03B7	2		
0x70000BA2	awbb_IndoorGrZones_m_BGrid[1]_m_right	0x03F9	2		
0x70000BA4	awbb_IndoorGrZones_m_BGrid[2]_m_left	0x03A0	2		
0x70000BA6	awbb_IndoorGrZones_m_BGrid[2]_m_right	0x03F9	2		
0x70000BA8	awbb_IndoorGrZones_m_BGrid[3]_m_left	0x0389	2		

Address	Initialization Parameters	Default	Size	Attribute	Description
0x70000BAA	awbb_IndoorGrZones_m_BGrid[3]_m_right	0x03EC	2		
0x70000BAC	awbb_IndoorGrZones_m_BGrid[4]_m_left	0x036C	2		
0x70000BAE	awbb_IndoorGrZones_m_BGrid[4]_m_right	0x03DB	2		
0x70000BB0	awbb_IndoorGrZones_m_BGrid[5]_m_left	0x034E	2		
0x70000BB2	awbb_IndoorGrZones_m_BGrid[5]_m_right	0x03C6	2		
0x70000BB4	awbb_IndoorGrZones_m_BGrid[6]_m_left	0x0334	2		
0x70000BB6	awbb_IndoorGrZones_m_BGrid[6]_m_right	0x03AF	2		
0x70000BB8	awbb_IndoorGrZones_m_BGrid[7]_m_left	0x0318	2		
0x70000BBA	awbb_IndoorGrZones_m_BGrid[7]_m_right	0x0394	2		
0x70000BBC	awbb_IndoorGrZones_m_BGrid[8]_m_left	0x02FE	2		
0x70000BBE	awbb_IndoorGrZones_m_BGrid[8]_m_right	0x037B	2		
0x70000BC0	awbb_IndoorGrZones_m_BGrid[9]_m_left	0x02EA	2		
0x70000BC2	awbb_IndoorGrZones_m_BGrid[9]_m_right	0x0362	2		
0x70000BC4	awbb_IndoorGrZones_m_BGrid[10]_m_left	0x02D5	2		
0x70000BC6	awbb_IndoorGrZones_m_BGrid[10]_m_right	0x034D	2		
0x70000BC8	awbb_IndoorGrZones_m_BGrid[11]_m_left	0x02C5	2		
0x70000BCA	awbb_IndoorGrZones_m_BGrid[11]_m_right	0x0336	2		
0x70000BCC	awbb_IndoorGrZones_m_BGrid[12]_m_left	0x02B4	2		
0x70000BCE	awbb_IndoorGrZones_m_BGrid[12]_m_right	0x031F	2		
0x70000BD0	awbb_IndoorGrZones_m_BGrid[13]_m_left	0x02A4	2		
0x70000BD2	awbb_IndoorGrZones_m_BGrid[13]_m_right	0x030B	2		
0x70000BD4	awbb_IndoorGrZones_m_BGrid[1	0x0297	2		

Address	Initialization Parameters	Default	Size	Attribute	Description
	4]_m_left				
0x70000BD6	awbb_IndoorGrZones_m_BGrid[14]_m_right	0x02F9	2		
0x70000BD8	awbb_IndoorGrZones_m_BGrid[15]_m_left	0x028A	2		
0x70000BDA	awbb_IndoorGrZones_m_BGrid[15]_m_right	0x02EB	2		
0x70000BDC	awbb_IndoorGrZones_m_BGrid[16]_m_left	0x027C	2		
0x70000BDE	awbb_IndoorGrZones_m_BGrid[16]_m_right	0x02DD	2		
0x70000BE0	awbb_IndoorGrZones_m_BGrid[17]_m_left	0x0270	2		
0x70000BE2	awbb_IndoorGrZones_m_BGrid[17]_m_right	0x02D0	2		
0x70000BE4	awbb_IndoorGrZones_m_BGrid[18]_m_left	0x0267	2		
0x70000BE6	awbb_IndoorGrZones_m_BGrid[18]_m_right	0x02C5	2		
0x70000BE8	awbb_IndoorGrZones_m_BGrid[19]_m_left	0x0259	2		
0x70000BEA	awbb_IndoorGrZones_m_BGrid[19]_m_right	0x02B9	2		
0x70000BEC	awbb_IndoorGrZones_m_BGrid[20]_m_left	0x024F	2		
0x70000BEE	awbb_IndoorGrZones_m_BGrid[20]_m_right	0x02AB	2		
0x70000BF0	awbb_IndoorGrZones_m_BGrid[21]_m_left	0x0245	2		
0x70000BF2	awbb_IndoorGrZones_m_BGrid[21]_m_right	0x029F	2		
0x70000BF4	awbb_IndoorGrZones_m_BGrid[22]_m_left	0x023B	2		
0x70000BF6	awbb_IndoorGrZones_m_BGrid[22]_m_right	0x0295	2		
0x70000BF8	awbb_IndoorGrZones_m_BGrid[23]_m_left	0x0234	2		
0x70000BFA	awbb_IndoorGrZones_m_BGrid[23]_m_right	0x028C	2		
0x70000BFC	awbb_IndoorGrZones_m_BGrid[24]_m_left	0x022E	2		
0x70000BFE	awbb_IndoorGrZones_m_BGrid[24]_m_right	0x0284	2		

Address	Initialization Parameters	Default	Size	Attribute	Description
0x70000C00	awbb_IndoorGrZones_m_BGrid[25]_m_left	0x0227	2		
0x70000C02	awbb_IndoorGrZones_m_BGrid[25]_m_right	0x027B	2		
0x70000C04	awbb_IndoorGrZones_m_BGrid[26]_m_left	0x0221	2		
0x70000C06	awbb_IndoorGrZones_m_BGrid[26]_m_right	0x0270	2		
0x70000C08	awbb_IndoorGrZones_m_BGrid[27]_m_left	0x021D	2		
0x70000C0A	awbb_IndoorGrZones_m_BGrid[27]_m_right	0x0265	2		
0x70000C0C	awbb_IndoorGrZones_m_BGrid[28]_m_left	0x0217	2		
0x70000C0E	awbb_IndoorGrZones_m_BGrid[28]_m_right	0x0257	2		
0x70000C10	awbb_IndoorGrZones_m_BGrid[29]_m_left	0x0217	2		
0x70000C12	awbb_IndoorGrZones_m_BGrid[29]_m_right	0x0243	2		
0x70000C14	awbb_IndoorGrZones_m_BGrid[30]_m_left	0x0000	2		
0x70000C16	awbb_IndoorGrZones_m_BGrid[30]_m_right	0x0000	2		
0x70000C18	awbb_IndoorGrZones_m_BGrid[31]_m_left	0x0000	2		
0x70000C1A	awbb_IndoorGrZones_m_BGrid[31]_m_right	0x0000	2		
0x70000C1C	awbb_IndoorGrZones_m_BGrid[32]_m_left	0x0000	2		
0x70000C1E	awbb_IndoorGrZones_m_BGrid[32]_m_right	0x0000	2		
0x70000C20	awbb_IndoorGrZones_m_BGrid[33]_m_left	0x0000	2		
0x70000C22	awbb_IndoorGrZones_m_BGrid[33]_m_right	0x0000	2		
0x70000C24	awbb_IndoorGrZones_m_BGrid[34]_m_left	0x0000	2		
0x70000C26	awbb_IndoorGrZones_m_BGrid[34]_m_right	0x0000	2		
0x70000C28	awbb_IndoorGrZones_m_BGrid[35]_m_left	0x0000	2		
0x70000C2A	awbb_IndoorGrZones_m_BGrid[3	0x0000	2		

Address	Initialization Parameters	Default	Size	Attribute	Description
	5]_m_right				
0x70000C2C	awbb_IndoorGrZones_m_BGrid[36]_m_left	0x0000	2		
0x70000C2E	awbb_IndoorGrZones_m_BGrid[36]_m_right	0x0000	2		
0x70000C30	awbb_IndoorGrZones_m_BGrid[37]_m_left	0x0000	2		
0x70000C32	awbb_IndoorGrZones_m_BGrid[37]_m_right	0x0000	2		
0x70000C34	awbb_IndoorGrZones_m_BGrid[38]_m_left	0x0000	2		
0x70000C36	awbb_IndoorGrZones_m_BGrid[38]_m_right	0x0000	2		
0x70000C38	awbb_IndoorGrZones_m_BGrid[39]_m_left	0x0000	2		
0x70000C3A	awbb_IndoorGrZones_m_BGrid[39]_m_right	0x0000	2		
0x70000C3C	awbb_IndoorGrZones_m_GridStep	0x00000004	4		
0x70000C40	awbb_IndoorGrZones_m_GridSz	0x0000001E	4		
0x70000C44	awbb_IndoorGrZones_m_Boffs	0x000000DE	4		
0x70000C48	awbb_IndoorGrZones_y_low	0x0000000A	4		
0x70000C50	awbb_IndoorGrZones_y_high	0x000000E0	4		
0x70000C54	awbb_OutdoorGrZones_m_BGrid[0]_m_left	0x0290	2		
0x70000C56	awbb_OutdoorGrZones_m_BGrid[0]_m_right	0x02C0	2		
0x70000C58	awbb_OutdoorGrZones_m_BGrid[1]_m_left	0x027E	2		
0x70000C5A	awbb_OutdoorGrZones_m_BGrid[1]_m_right	0x02C0	2		
0x70000C5C	awbb_OutdoorGrZones_m_BGrid[2]_m_left	0x0270	2		
0x70000C5E	awbb_OutdoorGrZones_m_BGrid[2]_m_right	0x02B6	2		
0x70000C60	awbb_OutdoorGrZones_m_BGrid[3]_m_left	0x0263	2		
0x70000C62	awbb_OutdoorGrZones_m_BGrid[3]_m_right	0x02A9	2		

Address	Initialization Parameters	Default	Size	Attribute	Description
0x70000C64	awbb_OutdoorGrZones_m_BGrid[4]_m_left	0x0259	2		
0x70000C66	awbb_OutdoorGrZones_m_BGrid[4]_m_right	0x029C	2		
0x70000C68	awbb_OutdoorGrZones_m_BGrid[5]_m_left	0x0250	2		
0x70000C6A	awbb_OutdoorGrZones_m_BGrid[5]_m_right	0x028F	2		
0x70000C6C	awbb_OutdoorGrZones_m_BGrid[6]_m_left	0x0248	2		
0x70000C6E	awbb_OutdoorGrZones_m_BGrid[6]_m_right	0x0283	2		
0x70000C70	awbb_OutdoorGrZones_m_BGrid[7]_m_left	0x0248	2		
0x70000C72	awbb_OutdoorGrZones_m_BGrid[7]_m_right	0x0277	2		
0x70000C74	awbb_OutdoorGrZones_m_BGrid[8]_m_left	0x0000	2		
0x70000C76	awbb_OutdoorGrZones_m_BGrid[8]_m_right	0x0000	2		
0x70000C78	awbb_OutdoorGrZones_m_BGrid[9]_m_left	0x0000	2		
0x70000C7A	awbb_OutdoorGrZones_m_BGrid[9]_m_right	0x0000	2		
0x70000C7C	awbb_OutdoorGrZones_m_BGrid[10]_m_left	0x0000	2		
0x70000C7E	awbb_OutdoorGrZones_m_BGrid[10]_m_right	0x0000	2		
0x70000C80	awbb_OutdoorGrZones_m_BGrid[11]_m_left	0x0000	2		
0x70000C82	awbb_OutdoorGrZones_m_BGrid[11]_m_right	0x0000	2		
0x70000C84	awbb_OutdoorGrZones_m_BGrid[12]_m_left	0x0000	2		
0x70000C86	awbb_OutdoorGrZones_m_BGrid[12]_m_right	0x0000	2		
0x70000C88	awbb_OutdoorGrZones_m_BGrid[13]_m_left	0x0000	2		
0x70000C8A	awbb_OutdoorGrZones_m_BGrid[13]_m_right	0x0000	2		
0x70000C8C	awbb_OutdoorGrZones_m_BGrid[14]_m_left	0x0000	2		
0x70000C8E	awbb_OutdoorGrZones_m_BGrid[	0x0000	2		

Address	Initialization Parameters	Default	Size	Attribute	Description
	14]_m_right				
0x70000C90	awbb_OutdoorGrZones_m_BGrid[15]_m_left	0x0000	2		
0x70000C92	awbb_OutdoorGrZones_m_BGrid[15]_m_right	0x0000	2		
0x70000C94	awbb_OutdoorGrZones_m_BGrid[16]_m_left	0x0000	2		
0x70000C96	awbb_OutdoorGrZones_m_BGrid[16]_m_right	0x0000	2		
0x70000C98	awbb_OutdoorGrZones_m_BGrid[17]_m_left	0x0000	2		
0x70000C9A	awbb_OutdoorGrZones_m_BGrid[17]_m_right	0x0000	2		
0x70000C9C	awbb_OutdoorGrZones_m_BGrid[18]_m_left	0x0000	2		
0x70000C9E	awbb_OutdoorGrZones_m_BGrid[18]_m_right	0x0000	2		
0x70000CA0	awbb_OutdoorGrZones_m_BGrid[19]_m_left	0x0000	2		
0x70000CA2	awbb_OutdoorGrZones_m_BGrid[19]_m_right	0x0000	2		
0x70000CA4	awbb_OutdoorGrZones_m_BGrid[20]_m_left	0x0000	2		
0x70000CA6	awbb_OutdoorGrZones_m_BGrid[20]_m_right	0x0000	2		
0x70000CA8	awbb_OutdoorGrZones_m_BGrid[21]_m_left	0x0000	2		
0x70000CAA	awbb_OutdoorGrZones_m_BGrid[21]_m_right	0x0000	2		
0x70000CAC	awbb_OutdoorGrZones_m_BGrid[22]_m_left	0x0000	2		
0x70000CAE	awbb_OutdoorGrZones_m_BGrid[22]_m_right	0x0000	2		
0x70000CB0	awbb_OutdoorGrZones_m_BGrid[23]_m_left	0x0000	2		
0x70000CB2	awbb_OutdoorGrZones_m_BGrid[23]_m_right	0x0000	2		
0x70000CB4	awbb_OutdoorGrZones_m_BGrid[24]_m_left	0x0000	2		
0x70000CB6	awbb_OutdoorGrZones_m_BGrid[24]_m_right	0x0000	2		
0x70000CB8	awbb_OutdoorGrZones_m_GridStep	0x00000004	4		

Address	Initialization Parameters	Default	Size	Attribute	Description
0x70000CBC	awbb_OutdoorGrZones_m_GridSz	0x00000008	4		
0x70000CC0	awbb_OutdoorGrZones_m_Boffs	0x000001F8	4		
0x70000CC4	awbb_OutdoorGrZones_y_low	0x0000000A	4		
0x70000CCC	awbb_OutdoorGrZones_y_high	0x000000E0	4		
0x70000CD0	awbb_LowBrGrZones_m_BGrid[0]_m_left	0x03B9	2		
0x70000CD2	awbb_LowBrGrZones_m_BGrid[0]_m_right	0x0434	2		
0x70000CD4	awbb_LowBrGrZones_m_BGrid[1]_m_left	0x0373	2		
0x70000CD6	awbb_LowBrGrZones_m_BGrid[1]_m_right	0x0434	2		
0x70000CD8	awbb_LowBrGrZones_m_BGrid[2]_m_left	0x0335	2		
0x70000CDA	awbb_LowBrGrZones_m_BGrid[2]_m_right	0x0434	2		
0x70000CDC	awbb_LowBrGrZones_m_BGrid[3]_m_left	0x0302	2		
0x70000CDE	awbb_LowBrGrZones_m_BGrid[3]_m_right	0x0424	2		
0x70000CE0	awbb_LowBrGrZones_m_BGrid[4]_m_left	0x02D0	2		
0x70000CE2	awbb_LowBrGrZones_m_BGrid[4]_m_right	0x0403	2		
0x70000CE4	awbb_LowBrGrZones_m_BGrid[5]_m_left	0x02AB	2		
0x70000CE6	awbb_LowBrGrZones_m_BGrid[5]_m_right	0x03DF	2		
0x70000CE8	awbb_LowBrGrZones_m_BGrid[6]_m_left	0x028A	2		
0x70000CEA	awbb_LowBrGrZones_m_BGrid[6]_m_right	0x03B5	2		
0x70000CEC	awbb_LowBrGrZones_m_BGrid[7]_m_left	0x0270	2		
0x70000CEE	awbb_LowBrGrZones_m_BGrid[7]_m_right	0x0386	2		
0x70000CF0	awbb_LowBrGrZones_m_BGrid[8]_m_left	0x0258	2		
0x70000CF2	awbb_LowBrGrZones_m_BGrid[8]	0x0365	2		

Address	Initialization Parameters	Default	Size	Attribute	Description
	_m_right				
0x70000CF4	awbb_LowBrGrZones_m_BGrid[9]_m_left	0x0243	2		
0x70000CF6	awbb_LowBrGrZones_m_BGrid[9]_m_right	0x0342	2		
0x70000CF8	awbb_LowBrGrZones_m_BGrid[10]_m_left	0x022E	2		
0x70000CFA	awbb_LowBrGrZones_m_BGrid[10]_m_right	0x0328	2		
0x70000CFC	awbb_LowBrGrZones_m_BGrid[11]_m_left	0x021A	2		
0x70000CFE	awbb_LowBrGrZones_m_BGrid[11]_m_right	0x0304	2		
0x70000D00	awbb_LowBrGrZones_m_BGrid[12]_m_left	0x0208	2		
0x70000D02	awbb_LowBrGrZones_m_BGrid[12]_m_right	0x02EC	2		
0x70000D04	awbb_LowBrGrZones_m_BGrid[13]_m_left	0x01FC	2		
0x70000D06	awbb_LowBrGrZones_m_BGrid[13]_m_right	0x02D2	2		
0x70000D08	awbb_LowBrGrZones_m_BGrid[14]_m_left	0x01F0	2		
0x70000D0A	awbb_LowBrGrZones_m_BGrid[14]_m_right	0x02B4	2		
0x70000D0C	awbb_LowBrGrZones_m_BGrid[15]_m_left	0x01E9	2		
0x70000D0E	awbb_LowBrGrZones_m_BGrid[15]_m_right	0x029C	2		
0x70000D10	awbb_LowBrGrZones_m_BGrid[16]_m_left	0x01E3	2		
0x70000D12	awbb_LowBrGrZones_m_BGrid[16]_m_right	0x0280	2		
0x70000D14	awbb_LowBrGrZones_m_BGrid[17]_m_left	0x01E3	2		
0x70000D16	awbb_LowBrGrZones_m_BGrid[17]_m_right	0x0268	2		
0x70000D18	awbb_LowBrGrZones_m_BGrid[18]_m_left	0x0000	2		
0x70000D1A	awbb_LowBrGrZones_m_BGrid[18]_m_right	0x0000	2		
0x70000D1C	awbb_LowBrGrZones_m_BGrid[19]_m_left	0x0000	2		

Address	Initialization Parameters	Default	Size	Attribute	Description
0x70000D1E	awbb_LowBrGrZones_m_BGrid[19]_m_right	0x0000	2		
0x70000D20	awbb_LowBrGrZones_m_BGrid[20]_m_left	0x0000	2		
0x70000D22	awbb_LowBrGrZones_m_BGrid[20]_m_right	0x0000	2		
0x70000D24	awbb_LowBrGrZones_m_BGrid[21]_m_left	0x0000	2		
0x70000D26	awbb_LowBrGrZones_m_BGrid[21]_m_right	0x0000	2		
0x70000D28	awbb_LowBrGrZones_m_BGrid[22]_m_left	0x0000	2		
0x70000D2A	awbb_LowBrGrZones_m_BGrid[22]_m_right	0x0000	2		
0x70000D2C	awbb_LowBrGrZones_m_BGrid[23]_m_left	0x0000	2		
0x70000D2E	awbb_LowBrGrZones_m_BGrid[23]_m_right	0x0000	2		
0x70000D30	awbb_LowBrGrZones_m_BGrid[24]_m_left	0x0000	2		
0x70000D32	awbb_LowBrGrZones_m_BGrid[24]_m_right	0x0000	2		
0x70000D34	awbb_LowBrGrZones_m_GridStep	0x00000005	4		
0x70000D38	awbb_LowBrGrZones_m_GridSz	0x00000012	4		
0x70000D3C	awbb_LowBrGrZones_m_Boffs	0x000000AE	4		
0x70000D40	awbb_LowBrGrZones_y_low	0x0000000A	4		
0x70000D48	awbb_LowBrGrZones_y_high	0x000000E0	4		
0x70000D4C	awbb_CrclLowT_R_c	0x000003CF	4		
0x70000D50	awbb_CrclLowT_B_c	0x0000012E	4		
0x70000D54	awbb_CrclLowT_Rad_c	0x0000DF21	4		
0x70000D58	awbb_CrclLowT_y_low	0x0000000A	4		
0x70000D60	awbb_CrclLowT_y_high	0x000000E0	4		
0x70000D64	awbb_DarkBr	0x0032	2		

Address	Initialization Parameters	Default	Size	Attribute	Description
0x70000D66	awbb_IntcR	0x0135	2		
0x70000D68	awbb_IntcB	0x0120	2		
0x70000D6E	awbb_MinNumOfInitialPatches	0x0023	2		
0x70000D70	awbb_MinNumOfLowBrInitialPatches	0x0023	2		
0x70000D72	awbb_AvMoveToGamutDist	0x0040	2		
0x70000D7C	awbb_ScDetect_Overwrite	0x0000	2		
0x70000D7E	awbb_ScDetect_Select	0x0000	2		
0x70000D80	awbb_ByPass_OutdoorMode	0x0000	2		
0x70000D82	awbb_ByPass_LowTempMode	0x0000	2		
0x70000D88	awbb_Use_InvalidOutDoor	0x0000	2		
0x70000D8C	awbb_Use_Filters	0x0065	2		
0x70000D8E	awbb_GridEnable	0x0000	2		
0x70000D90	awbb_UseAvAsIllum	0x0000	2		
0x70000D92	awbb_SunnyBr	0x274C	2		
0x70000D94	awbb_Sunny_NBzone	0x03E8	2		
0x70000D96	awbb_CloudyBr	0x07D0	2		
0x70000D98	awbb_Cloudy_NBzone	0x0078	2		
0x70000D9A	awbb_Cloudy_BdivRzone	0x000F	2		
0x70000D9C	awbb_MacbethGamut_WidthZone	0x006C	2		
0x70000D9E	awbb_MacbethGamut_HeightZone	0x0038	2		
0x70000DA0	awbb_MacbethGamut_WidthZone2	0x0040	2		
0x70000DA2	awbb_MacbethGamut_HeightZone2	0x0010	2		
0x70000DA4	awbb_LowTemp_RBzone	0x0078	2		
0x70000DA6	awbb_LowBr_NBzone	0x000A	2		
0x70000DA8	awbb_LowBr0_NBzone	0x0019	2		
0x70000DAA	awbb_GamutWidthThr1	0x05F0	2		
0x70000DAC	awbb_GamutHeightThr1	0x01F4	2		
0x70000DAE	awbb_GamutWidthThr2	0x006C	2		
0x70000DB0	awbb_GamutHeightThr2	0x0038	2		
0x70000DB2	awbb_CloudyRB	0x00E5	2		
0x70000DB4	awbb_LowTempRB	0x05B0	2		
0x70000DB6	awbb_MinNumOfFinalPatches	0x0023	2		
0x70000DB8	awbb_MinNumOfOutdoorPatches	0x0023	2		
0x70000DBC	awbb_MinNumOfLowBrFinalPatches	0x0023	2		

Address	Initialization Parameters	Default	Size	Attribute	Description
0x70000DBE	awbb_MinNumOfLowBr0_FinalPatches	0x0046	2		
0x70000DC2	awbb_GnCurPntImmunity	0x000F	2		
0x70000DC4	awbb_GnFarPntImmunity	0x001E	2		
0x70000DC6	awbb_GnCurPntLongJump	0x000A	2		
0x70000DC8	awbb_GainsMaxMove	0x0258	2		
0x70000DCA	awbb_GnMinMatchToJump	0x0001	2		
0x70000DCC	awbb_GainsRCcoef	0x00C8	2		
0x70000DCE	awbb_GridCorr_R[0][0]	0xFFFE	2		
0x70000DD0	awbb_GridCorr_R[0][1]	0xFFFE	2		
0x70000DD2	awbb_GridCorr_R[0][2]	0x0000	2		
0x70000DD4	awbb_GridCorr_R[0][3]	0x0000	2		
0x70000DD6	awbb_GridCorr_R[0][4]	0x0000	2		
0x70000DD8	awbb_GridCorr_R[0][5]	0x0000	2		
0x70000DDA	awbb_GridCorr_R[1][0]	0xFFDD	2		
0x70000DDC	awbb_GridCorr_R[1][1]	0xFFFB	2		
0x70000DDE	awbb_GridCorr_R[1][2]	0xFFE2	2		
0x70000DE0	awbb_GridCorr_R[1][3]	0x0000	2		
0x70000DE2	awbb_GridCorr_R[1][4]	0xFFF1	2		
0x70000DE4	awbb_GridCorr_R[1][5]	0x0000	2		
0x70000DE6	awbb_GridCorr_R[2][0]	0x0000	2		
0x70000DE8	awbb_GridCorr_R[2][1]	0xFFFC	2		
0x70000DEA	awbb_GridCorr_R[2][2]	0x0000	2		
0x70000DEC	awbb_GridCorr_R[2][3]	0x0000	2		
0x70000DEE	awbb_GridCorr_R[2][4]	0x0000	2		
0x70000DF0	awbb_GridCorr_R[2][5]	0x0000	2		
0x70000DF2	awbb_GridCorr_B[0][0]	0x000C	2		
0x70000DF4	awbb_GridCorr_B[0][1]	0x0006	2		
0x70000DF6	awbb_GridCorr_B[0][2]	0x0000	2		
0x70000DF8	awbb_GridCorr_B[0][3]	0x0000	2		
0x70000DFA	awbb_GridCorr_B[0][4]	0x0000	2		
0x70000DFC	awbb_GridCorr_B[0][5]	0x0000	2		
0x70000DFE	awbb_GridCorr_B[1][0]	0x0017	2		
0x70000E00	awbb_GridCorr_B[1][1]	0x0015	2		
0x70000E02	awbb_GridCorr_B[1][2]	0x002D	2		
0x70000E04	awbb_GridCorr_B[1][3]	0x0037	2		
0x70000E06	awbb_GridCorr_B[1][4]	0x000C	2		

Address	Initialization Parameters	Default	Size	Attribute	Description
0x70000E08	awbb_GridCorr_B[1][5]	0x0000	2		
0x70000E0A	awbb_GridCorr_B[2][0]	0x000C	2		
0x70000E0C	awbb_GridCorr_B[2][1]	0x0006	2		
0x70000E0E	awbb_GridCorr_B[2][2]	0x0000	2		
0x70000E10	awbb_GridCorr_B[2][3]	0x0000	2		
0x70000E12	awbb_GridCorr_B[2][4]	0x000C	2		
0x70000E14	awbb_GridCorr_B[2][5]	0x0000	2		
0x70000E16	awbb_GridConst_1[0]	0x030C	2		
0x70000E18	awbb_GridConst_1[1]	0x0348	2		
0x70000E1A	awbb_GridConst_1[2]	0x0384	2		
0x70000E1C	awbb_GridConst_2[0]	0x0FA6	2		
0x70000E1E	awbb_GridConst_2[1]	0x1000	2		
0x70000E20	awbb_GridConst_2[2]	0x1064	2		
0x70000E22	awbb_GridConst_2[3]	0x10C8	2		
0x70000E24	awbb_GridConst_2[4]	0x115E	2		
0x70000E26	awbb_GridConst_2[5]	0x1208	2		
0x70000E28	awbb_GridCoeff_R_1	0x00BE	2		
0x70000E2A	awbb_GridCoeff_B_1	0x00AB	2		
0x70000E2C	awbb_GridCoeff_R_2	0x00B5	2		
0x70000E2E	awbb_GridCoeff_B_2	0x00B5	2		
0x70000E30	awbb_OutdoorFltrSz	0x0008	2		
0x70000E32	awbb_RGainOff	0x0000	2		
0x70000E34	awbb_BGainOff	0x0000	2		
0x70000E36	awbb_GGainOff	0x0000	2		
0x70000E56	awbb_GamMinOff	0x0640	2		
0x70000E58	awbb_GamMinRatio1	0x00C8	2		
0x70000E5A	awbb_GamMinRatio2	0x0080	2		
0x70000E5C	awbb_GamOffMinCos2_10	0x02BC	2		
0x70000E5E	awbb_GLocusR	0x0297	2		
0x70000E60	awbb_GLocusB	0x036A	2		
0x70000E62	awbb_LowTSubstrPnt[0]	0x0127	2		
0x70000E64	awbb_LowTSubstrPnt[1]	0x0140	2		
0x70000E66	awbb_LowTSubstrPnt[2]	0x016E	2		
0x70000E68	awbb_LowTSubstrPnt[3]	0x019B	2		
0x70000E6A	awbb_LowTSubstrPnt[4]	0x01B3	2		
0x70000E6C	awbb_LowTSubstrPnt[5]	0x01BD	2		
0x70000E6E	awbb_LowTSubstrPnt[6]	0x01C3	2		

Address	Initialization Parameters	Default	Size	Attribute	Description
0x70000E70	awbb_LowTSubstrWeight[0]	0x0000	2		
0x70000E72	awbb_LowTSubstrWeight[1]	0x0028	2		
0x70000E74	awbb_LowTSubstrWeight[2]	0x00AA	2		
0x70000E76	awbb_LowTSubstrWeight[3]	0x00C8	2		
0x70000E78	awbb_LowTSubstrWeight[4]	0x00F0	2		
0x70000E7A	awbb_LowTSubstrWeight[5]	0x0100	2		
0x70000E7C	awbb_LowTSubstrWeight[6]	0x0114	2		
0x70000E80	awbb_ChMoveToNearR	0x00B3	2		
0x70000E84	awbb_UseFixedOutDoor	0x0001	2		
0x70000E86	awbb_OutdoorWP_r	0x0202	2		
0x70000E88	awbb_OutdoorWP_b	0x02F9	2		
0x70000E8A	awbb_BorderSize	0x0010	2		
0x70000E8C	awbb_LowBr0_PatchNumZone	0x0019	2		
0x70000F5A	ae_WeightTbl_16[0]	0x0101	2		
0x70000F5C	ae_WeightTbl_16[1]	0x0101	2		
0x70000F5E	ae_WeightTbl_16[2]	0x0101	2		
0x70000F60	ae_WeightTbl_16[3]	0x0101	2		
0x70000F62	ae_WeightTbl_16[4]	0x0101	2		
0x70000F64	ae_WeightTbl_16[5]	0x0201	2		
0x70000F66	ae_WeightTbl_16[6]	0x0102	2		
0x70000F68	ae_WeightTbl_16[7]	0x0101	2		
0x70000F6A	ae_WeightTbl_16[8]	0x0101	2		
0x70000F6C	ae_WeightTbl_16[9]	0x0202	2		
0x70000F6E	ae_WeightTbl_16[10]	0x0202	2		
0x70000F70	ae_WeightTbl_16[11]	0x0101	2		
0x70000F72	ae_WeightTbl_16[12]	0x0101	2		
0x70000F74	ae_WeightTbl_16[13]	0x0402	2		
0x70000F76	ae_WeightTbl_16[14]	0x0204	2		
0x70000F78	ae_WeightTbl_16[15]	0x0101	2		
0x70000F7A	ae_WeightTbl_16[16]	0x0201	2		
0x70000F7C	ae_WeightTbl_16[17]	0x0504	2		
0x70000F7E	ae_WeightTbl_16[18]	0x0405	2		
0x70000F80	ae_WeightTbl_16[19]	0x0102	2		
0x70000F82	ae_WeightTbl_16[20]	0x0501	2		
0x70000F84	ae_WeightTbl_16[21]	0x0505	2		
0x70000F86	ae_WeightTbl_16[22]	0x0505	2		
0x70000F88	ae_WeightTbl_16[23]	0x0105	2		

Address	Initialization Parameters	Default	Size	Attribute	Description
0x70000F8A	ae_WeightTbl_16[24]	0x0503	2		
0x70000F8C	ae_WeightTbl_16[25]	0x0505	2		
0x70000F8E	ae_WeightTbl_16[26]	0x0505	2		
0x70000F90	ae_WeightTbl_16[27]	0x0305	2		
0x70000F92	ae_WeightTbl_16[28]	0x0303	2		
0x70000F94	ae_WeightTbl_16[29]	0x0303	2		
0x70000F96	ae_WeightTbl_16[30]	0x0303	2		
0x70000F98	ae_WeightTbl_16[31]	0x0303	2		
0x70001186	pll_uMinRefFreq	0x07D0	2		
0x70001188	pll_uMaxRefFreq	0x2EE0	2		
0x7000118A	pll_uMinVcoFreqKhz	0x0145	2		
0x7000118C	pll_uMaxVcoFreqKhz	0x028B	2		
0x7000118E	pll_bBypassEnaRD	0x0001	2		
0x700014A0	Mon_LT_ulActualLei	0x00000000	4		
0x700014A4	Mon_LT_uStableCntr	0x0000	2		
0x700014AC	Mon_LT_ulCrntTargetLei	0x00000000	4		
0x700014B8	Mon_LT_usNextActualExp	0x00000000	4		
0x700014C0	Mon_LT_uSenMinExp	0x0000	2		
0x700014C2	Mon_LT_usActualDGainMax	0x0000	2		
0x700014C4	Mon_LT_ActualGain_Digital88	0x0000	2		Actual max digital gain.
0x700014C6	Mon_LT_ActualGain_RequestedAnalog88	0x0000	2		
0x700014C8	Mon_LT_ActualGain_AccurateAnalog88	0x0000	2		
0x700014CA	Mon_LT_NextGain_Digital88	0x0000	2		
0x700014CC	Mon_LT_NextGain_RequestedAnalog88	0x0000	2		
0x700014CE	Mon_LT_NextGain_AccurateAnalog88	0x0000	2		
0x700014D4	Mon_LT_HwFrTime	0x00000000	4		
0x700014DE	Mon_LT_usActualTotGain	0x0000	2		
0x700014E0	Mon_LT_usActualDigGain	0x0000	2		
0x700014EC	Mon_LT_Exp_uLines	0x0000	2		
0x700014EE	Mon_LT_Exp_uSamples	0x0000	2		
0x700019AC	Mon_AWB_m_IndoorStat_AvE_Po	0x0000	2		

Address	Initialization Parameters	Default	Size	Attribute	Description
	int_r				
0x700019AE	Mon_AWB_m_IndoorStat_AvE_Point_b	0x0000	2		
0x700019B0	Mon_AWB_m_IndoorStat_AvE_No	0x0000	2		
0x700019B4	Mon_AWB_m_IndoorStat_y_Stat_y_sum	0x00000000	4		
0x700019B8	Mon_AWB_m_IndoorStat_y_Stat_y_min	0x0000	2		
0x700019BA	Mon_AWB_m_IndoorStat_y_Stat_y_max	0x0000	2		
0x700019BC	Mon_AWB_m_IndoorStat_y_Stat_y_No	0x0000	2		
0x700019C0	Mon_AWB_m_LowTStat_YLvl[0]_Point_r	0x0000	2		
0x700019C2	Mon_AWB_m_LowTStat_YLvl[0]_Point_b	0x0000	2		
0x700019C4	Mon_AWB_m_LowTStat_YLvl[0]_No	0x0000	2		
0x700019C6	Mon_AWB_m_LowTStat_YLvl[1]_Point_r	0x0000	2		
0x700019C8	Mon_AWB_m_LowTStat_YLvl[1]_Point_b	0x0000	2		
0x700019CA	Mon_AWB_m_LowTStat_YLvl[1]_No	0x0000	2		
0x700019CC	Mon_AWB_m_LowTStat_AvE_Point_r	0x0000	2		
0x700019CE	Mon_AWB_m_LowTStat_AvE_Point_b	0x0000	2		
0x700019D0	Mon_AWB_m_LowTStat_AvE_No	0x0000	2		
0x700019D2	Mon_AWB_m_LowBrStat_YLvl[0]_Point_r	0x0000	2		
0x700019D4	Mon_AWB_m_LowBrStat_YLvl[0]_Point_b	0x0000	2		
0x700019D6	Mon_AWB_m_LowBrStat_YLvl[0]_No	0x0000	2		
0x700019D8	Mon_AWB_m_LowBrStat_YLvl[1]_Point_r	0x0000	2		
0x700019DA	Mon_AWB_m_LowBrStat_YLvl[1]_Point_b	0x0000	2		
0x700019DC	Mon_AWB_m_LowBrStat_YLvl[1]_No	0x0000	2		

Address	Initialization Parameters	Default	Size	Attribute	Description
0x700019DE	Mon_AWB_m_LowBrStat_AvE_Point_r	0x0000	2		
0x700019E0	Mon_AWB_m_LowBrStat_AvE_Point_b	0x0000	2		
0x700019E2	Mon_AWB_m_LowBrStat_AvE_No	0x0000	2		
0x700019E4	Mon_AWB_m_OutDStat_YLvl[0]_Point_r	0x0000	2		
0x700019E6	Mon_AWB_m_OutDStat_YLvl[0]_Point_b	0x0000	2		
0x700019E8	Mon_AWB_m_OutDStat_YLvl[0]_No	0x0000	2		
0x700019EA	Mon_AWB_m_OutDStat_YLvl[1]_Point_r	0x0000	2		
0x700019EC	Mon_AWB_m_OutDStat_YLvl[1]_Point_b	0x0000	2		
0x700019EE	Mon_AWB_m_OutDStat_YLvl[1]_No	0x0000	2		
0x700019F0	Mon_AWB_m_OutDStat_AvE_Point_r	0x0000	2		
0x700019F2	Mon_AWB_m_OutDStat_AvE_Point_b	0x0000	2		
0x700019F4	Mon_AWB_m_OutDStat_AvE_No	0x0000	2		
0x70001A3A	Mon_AWB_IllumPt_r	0x0000	2		
0x70001A3C	Mon_AWB_IllumPt_b	0x0000	2		
0x70001A3E	Mon_AWB_FinalPt_r	0x0000	2		
0x70001A40	Mon_AWB_FinalPt_b	0x0000	2		
0x70001A42	Mon_AWB_uGamutWidth	0x0000	2		
0x70001A44	Mon_AWB_uGamutHeight	0x0000	2		
0x70001A4A	Mon_AWB_uFrameStatus	0x0000	2		
0x70001A72	Mon_AWB_FinalWP_wpLowBr_r	0x0000	2		
0x70001A74	Mon_AWB_FinalWP_wpLowBr_b	0x0000	2		
0x70001A76	Mon_AWB_FinalWP_wpLowBr0_r	0x0000	2		
0x70001A78	Mon_AWB_FinalWP_wpLowBr0_b	0x0000	2		
0x70001A7A	Mon_AWB_FinalWP_wpLowBrS_r	0x0000	2		
0x70001A7C	Mon_AWB_FinalWP_wpLowBrS_b	0x0000	2		
0x70001A7E	Mon_AWB_FinalWP_wpOutdoor_r	0x0000	2		
0x70001A80	Mon_AWB_FinalWP_wpOutdoor_b	0x0000	2		

Address	Initialization Parameters	Default	Size	Attribute	Description
0x70001A82	Mon_AWB_FinalWP_wpLowTemp_r	0x0000	2		
0x70001A84	Mon_AWB_FinalWP_wpLowTemp_b	0x0000	2		
0x70001A86	Mon_AWB_FinalWP_wpGeneral_r	0x0000	2		
0x70001A88	Mon_AWB_FinalWP_wpGeneral_b	0x0000	2		
0x70001A8A	Mon_AWB_FinalWP_wpPrimOutdoorWP_r	0x0000	2		
0x70001A8C	Mon_AWB_FinalWP_wpPrimOutdoorWP_b	0x0000	2		
0x70001A8E	Mon_AWB_Weights_wLowBr	0x0000	2		
0x70001A90	Mon_AWB_Weights_wSunny	0x0000	2		
0x70001A92	Mon_AWB_Weights_wCloudy	0x0000	2		
0x70001A94	Mon_AWB_Weights_wHighTemp	0x0000	2		
0x70001A96	Mon_AWB_Weights_wOutdoor	0x0000	2		
0x70001A98	Mon_AWB_Weights_wLowTemp	0x0000	2		
0x70001A9A	Mon_AWB_Weights_wGeneral	0x0000	2		
0x70001A9C	Mon_AWB_Weights_wDummy	0x0000	2		
0x70001AE0	Mon_AWB_Match2Jump	0x0000	2		
0x70001AF4	Mon_AWB_NearR_r	0x0000	2		
0x70001AF6	Mon_AWB_NearR_b	0x0000	2		
0x70001AF8	Mon_AWB_NearB_r	0x0000	2		
0x70001AFA	Mon_AWB_NearB_b	0x0000	2		
0x70001AFC	Mon_AWB_PrevNearR_r	0x0000	2		
0x70001AFE	Mon_AWB_PrevNearR_b	0x0000	2		
0x70001B00	Mon_AWB_PrevNearB_r	0x0000	2		
0x70001B02	Mon_AWB_PrevNearB_b	0x0000	2		
0x70001B5A	Mon_AAIO_bLEIRefresh	0x0000	2		
0x70001B5C	Mon_AAIO_bAE	0x0000	2		
0x70001B64	Mon_AAIO_bAFC	0x0000	2		
0x70001B66	Mon_AAIO_bAWB	0x0000	2		
0x70001B68	MVAR_AAIO_bFIT	0x0000	2		
0x70001B78	Mon_AAIO_ulOptimalLei	0x00000000	4		
0x70001CF8	Mon_AE_CrntAvBr	0x0000	2		
0x70001D0A	Mon_AE_FinalGain	0x0000	2		
0x70001D18	Mon_AE_WeightTbl_16[0]	0x0000	2		
0x70001D1A	Mon_AE_WeightTbl_16[1]	0x0000	2		

Address	Initialization Parameters	Default	Size	Attribute	Description
0x70001D1C	Mon_AE_WeightTbl_16[2]	0x0000	2		
0x70001D1E	Mon_AE_WeightTbl_16[3]	0x0000	2		
0x70001D20	Mon_AE_WeightTbl_16[4]	0x0000	2		
0x70001D22	Mon_AE_WeightTbl_16[5]	0x0000	2		
0x70001D24	Mon_AE_WeightTbl_16[6]	0x0000	2		
0x70001D26	Mon_AE_WeightTbl_16[7]	0x0000	2		
0x70001D28	Mon_AE_WeightTbl_16[8]	0x0000	2		
0x70001D2A	Mon_AE_WeightTbl_16[9]	0x0000	2		
0x70001D2C	Mon_AE_WeightTbl_16[10]	0x0000	2		
0x70001D2E	Mon_AE_WeightTbl_16[11]	0x0000	2		
0x70001D30	Mon_AE_WeightTbl_16[12]	0x0000	2		
0x70001D32	Mon_AE_WeightTbl_16[13]	0x0000	2		
0x70001D34	Mon_AE_WeightTbl_16[14]	0x0000	2		
0x70001D36	Mon_AE_WeightTbl_16[15]	0x0000	2		
0x70001D38	Mon_AE_WeightTbl_16[16]	0x0000	2		
0x70001D3A	Mon_AE_WeightTbl_16[17]	0x0000	2		
0x70001D3C	Mon_AE_WeightTbl_16[18]	0x0000	2		
0x70001D3E	Mon_AE_WeightTbl_16[19]	0x0000	2		
0x70001D40	Mon_AE_WeightTbl_16[20]	0x0000	2		
0x70001D42	Mon_AE_WeightTbl_16[21]	0x0000	2		
0x70001D44	Mon_AE_WeightTbl_16[22]	0x0000	2		
0x70001D46	Mon_AE_WeightTbl_16[23]	0x0000	2		
0x70001D48	Mon_AE_WeightTbl_16[24]	0x0000	2		
0x70001D4A	Mon_AE_WeightTbl_16[25]	0x0000	2		
0x70001D4C	Mon_AE_WeightTbl_16[26]	0x0000	2		
0x70001D4E	Mon_AE_WeightTbl_16[27]	0x0000	2		
0x70001D50	Mon_AE_WeightTbl_16[28]	0x0000	2		
0x70001D52	Mon_AE_WeightTbl_16[29]	0x0000	2		
0x70001D54	Mon_AE_WeightTbl_16[30]	0x0000	2		
0x70001D56	Mon_AE_WeightTbl_16[31]	0x0000	2		