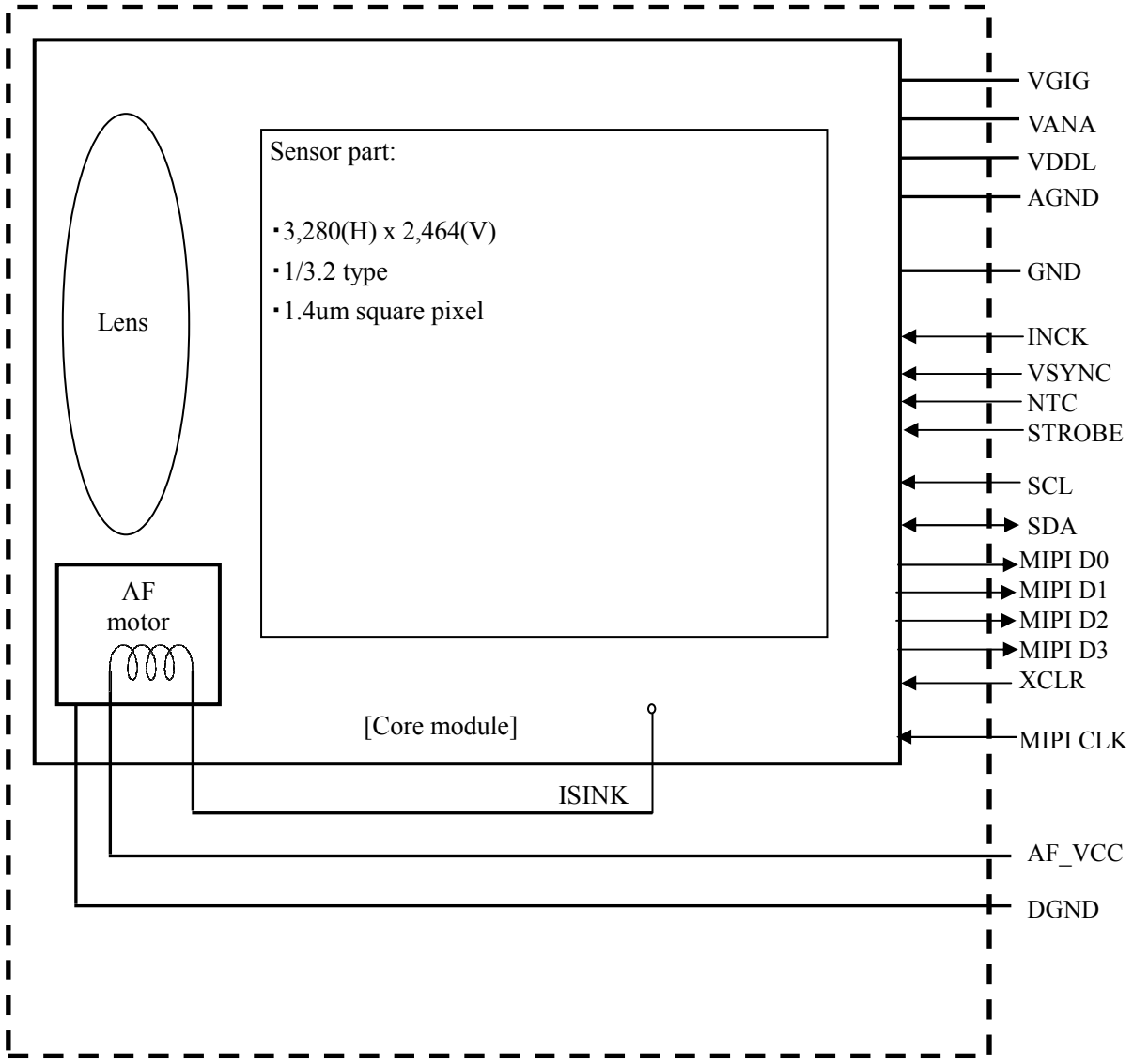
1. Block diagram

1-1.Camera module block diagram



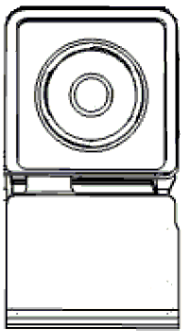
[Module with FPC]

2. Pin assignment

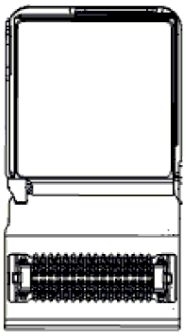
Pin #	Name	I/O	Pin Type
1	GND	-	Ground
2	INCK	-	Master clock
3	MIPI D3 N		Outputs 1
4	I2C_C		I2C
5	MIPI D3 P		Outputs 2
6	I2C_D		I2C
7	GND	-	Ground
8	VSYNC		
9	MIPI D1 N		Outputs 3
10	NTC	-	Thermistor
11	MIPI D1 P		Outputs 4
12	GND_AF		
13	GND	-	Ground
14	AVDD_AF	-	
15	MIPI CLK N		
16	VDDL	-	
17	MIPI CLK P		
18	VDDL	-	
19	GND	-	Ground
20	VGIG	-	
21	MIPI D0 N		Outputs 5
22	VGIG	-	
23	MIPI D0 P		Outputs 6
24	XCLR		
25	GND	-	Ground
26	Strobe		
27	MIPI D2 N		Outputs 7
28	NC	-	No contact
29	MIPI D2 P		Outputs 8
30	VANA	-	
31	GND	-	Ground
32	AGND	-	Ground
33	LED (-)	-	
34	LED (-)	-	
35	LED (+)	-	
36	LED (+)	-	Ground for AF motor 1)

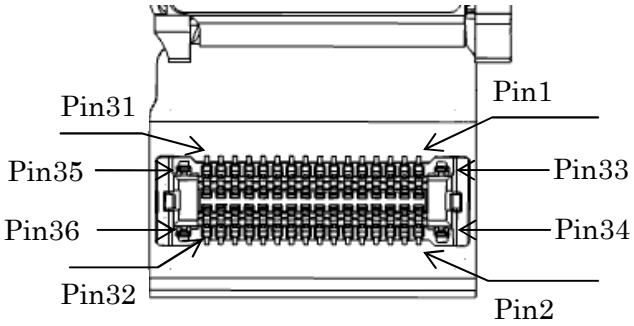
1) Please be careful not to inflict outside noise on the power supplies terminal (DVDD_CORE, DVDD_IO, AVDD).

[Top View]

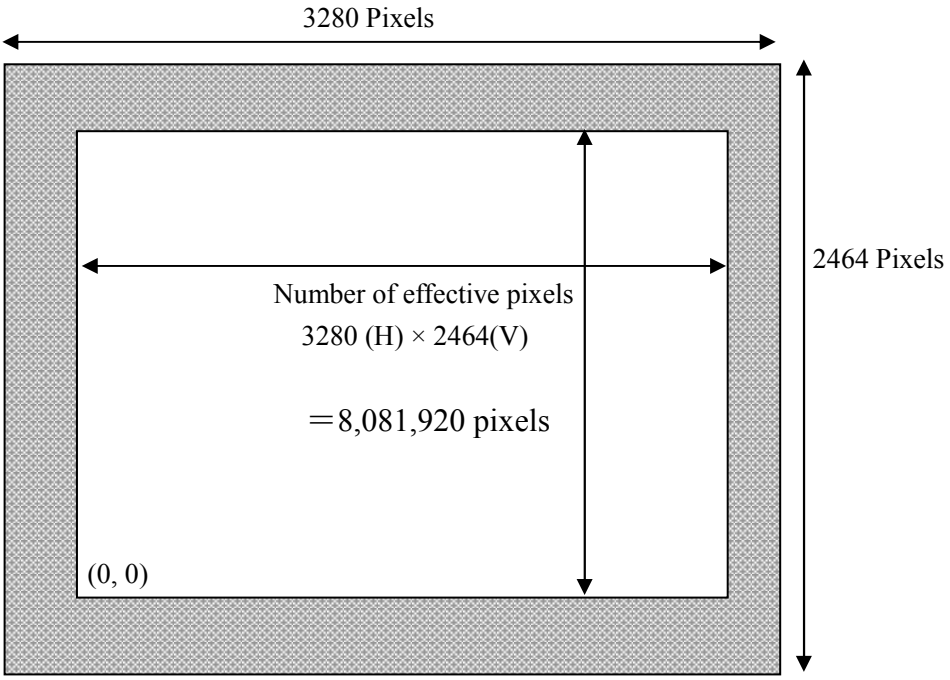


[Bottom View]





3. Arrangement of pixel



(0, 2464) (3280, 2464)

R	G	R	G	R		G	R	G	R	G
G	B	G	B	G		B	G	B	G	B
R	G	R	G	R		G	R	G	R	G
G	B	G	B	G		B	G	B	G	B
R	G	R	G	R		G	R	G	R	G
G	B	G	B	G		B	G	B	G	B
R	G	R	G	R		G	R	G	R	G
G	B	G	B	G		B	G	B	G	B
R	G	R	G	R		G	R	G	R	G
G	B	G	B	G		B	G	B	G	B
R	G	R	G	R		G	R	G	R	G
G	B	G	B	G		B	G	B	G	B

(0, 0) (3280, 0)

4. Camera specification

4-1. CMOS image sensor specification

Subject	Description
Optical lens	1/3.2 type
Scanning Method	Progressive Scan, RGB primary color filter
Number of effective Pixels	3,280(H) x 2,464(V)
Number of output Pixels	-(H) x -(V)
Pixel Pitch	1.4μm (H) x 1.4μm(V)

4-2. Camera part package specification

Items	characteristics
Material	Plastic / Glass epoxy substrate
Size	Core module: 8.5mm x 8.5mm x (h)6.4mm

4-3.Lens specification

Subject	Description	Note
Lens Configuration	5 pieces of plastic lens	
Focal Length	4.3mm	
F number	F2.4	
Viewing Angle (Inf)	(H)55.1 deg, (H)42.7 deg , (D):66 deg	
TV Distortion (Inf)	±1.0% max	(A)
Focus Range	10 cm to infinity	

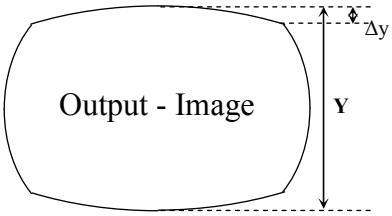
[Note(A)]

When it takes a rectangle pattern (4:3).

The height of the image center of the monitor screen : Y

The difference with the height of the penumbra part : Δy

(Δy / Y) × 100%



Monitor type

- Cask type :Δy is negative value
- Spool type : Δy is positive value

5. Electrical characteristics

5-1.Absolute maximum rating

Item	Symbol	Specification	Unit	Note
Power Supply Voltage	VANA	-0.3～3.2	V	IO Power
	VDDL	-0.3～2.0	V	Analog Power
	VGIG	-0.3～3.2	V	Internal Core digital power
Current Consumption(AF)	AVDD_AF	80	mA	
Storage Temperature	T_{STG}	-40～+85	℃	

5-2.Recommended operating condition

(Ta=+25℃)

Items	Symbol	MIN.	TYP.	MAX.	Unit	Remarks
Power Supply Voltage	VANA	2.6	2.7	2.9	V	Analog Voltage
	VDDL	1.1	1.2	1.3	V	Digital Voltage
	VGIG	1.65	1.8	1.92	V	IO Voltage
Current Consumption	I_{ANA}			100	mA	Analog current
	I_{CORE}			1		Digital current
				10	uA	Motor driver start current
	I_{IO}			165	mA	Input current
Standby Current	I_{SB}			10	μA	
Operating Temperature	T_A	-15		65	℃	

6. Communication protocol

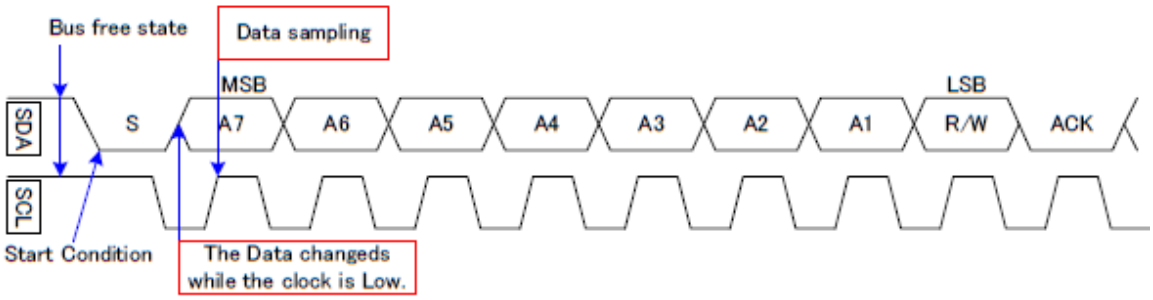


Fig. 7 Start Condition

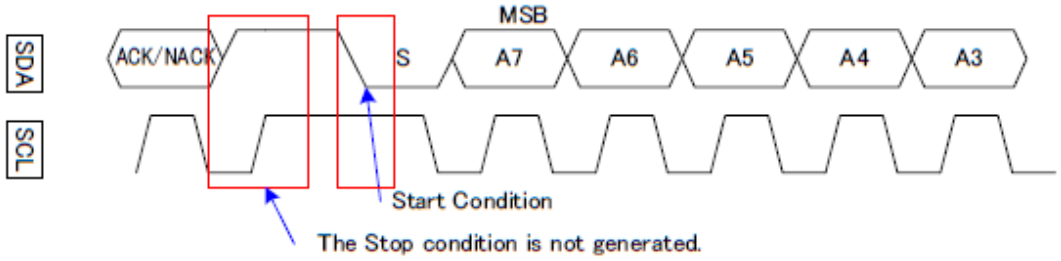


Fig. 8 Repeated Start Condition

The Stop condition is defined by SDA changing from Low to High while SCL is High.

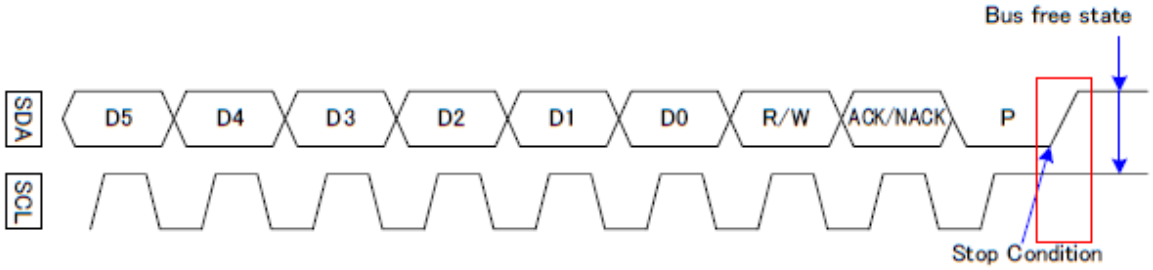


Fig. 9 Stop Condition

The slave address is as follows.

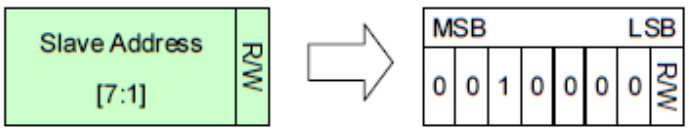


Fig. 10 Slave Address (Default)

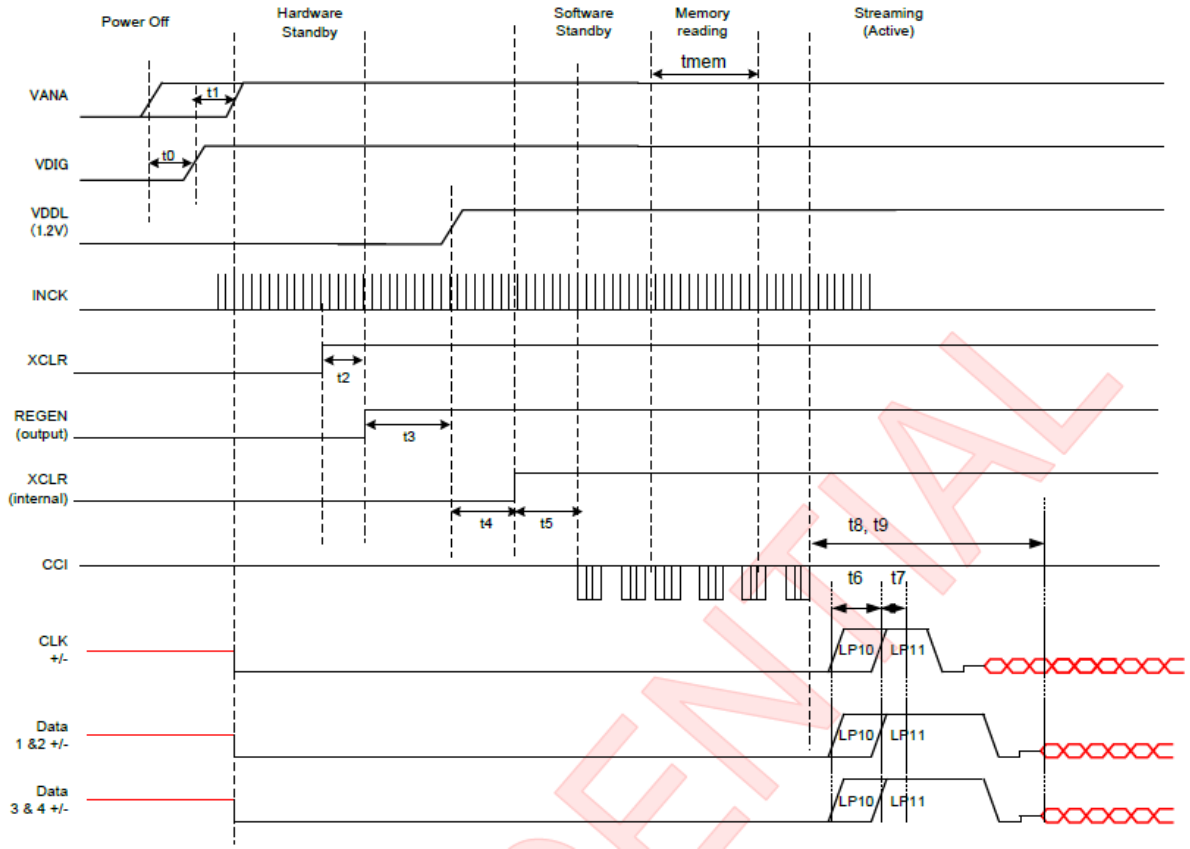
The R/W bit indicates the data transfer direction.

Table 6 R/W Bit

R/W bit	Transfer direction
0	Write(Master →Sensor)
1	Read(Sensor → Master)

Startup Sequence in 2-wire Serial Communication Mode

Perform power-on according to the following sequence.



Constraint	Label	Min	Max	Units	Comment
Sequence free of VANA rising and VDIG rising	t0, t1	VANA and VDIG may rise in any order.		ns	
Time to REGEN Low to High after XCLR Low to High	t2		0.5	us	
Time to VDDL is supplied to sensor after REGEN high	t3			us	Depending on Device
Internal XCLR is Low to High after VDDL is supplied	t4	100	600	us	Waking up time and init settings
Initializing time of silicon	t5		8825	clocks	
D-PHY power-up	t6	1	1.1	ms	
D-PHY init	t7	100	110	us	
After releasing software standby to data streaming time	t8	1.5ms + exposure time			
Quick launch up time	t9		1	frame	stable time until optimal image quality

7. VCM Driver Interface

- Address : 0001110
- Write command : 00011100
- Read command : 00011101

REGISTER DESCRIPTIONS

In this section, for registers that use less than eight bits, the unused bits are read back as 0s. The unused bits are 0 for write operations. Registers are right justified; 0 for unused bits are on the MSB side.

Table 9. Register Descriptions

Addr (Hex)	Addr (Dec)	Name	Description	R/W Bits	Reset
0x00	0	IC_INFO	IC information	8 R	0x24
0x01	1	IC_VERSION	IC version	3 R	0x04
0x02	2	Control	Configure the AD5816E modes of operation	5 R/W	0x00
0x03	3	VCM_CODE_MSB	DAC MSB register	2 R/W	0x00
0x04	4	VCM_CODE_LSB	DAC LSB register	8 R/W	0x00
0x05	5	Status	Indicates an overcurrent or undervoltage condition	2 R	0x00
0x06	6	Mode	Driver frequency, drive mode, and ARC mode	8 R/W	0x01
0x07	7	VCM_FREQ	VCM frequency	8 R/W	0x80
0x08	8	VCM_THRESHOLD	VCM threshold value	8 R/W	0x08

REGISTER BIT DEFINITIONS

Table 10. IC_INFO Register, Address = 0x00, Reset = 0x24, Type = R

Bits	Bit Name	Reset	Description
[7:4]	MAN_ID[3:0]	0010	Manufacturer ID.
[3:0]	DEV_ID[3:0]	0100	Device ID.

Table 11. IC_VERSION Register, Address = 0x01, Reset = 0x04, Type = R

Bits	Bit Name	Reset	Description
[7:3]	Reserved	00000	Must be set to 00000.
[2:0]	VERSION[2:0]	100	Version.

Table 12. Control Register, Address = 0x02, Reset = 0x00, Type = R/W

Bits	Name	Reset	Description
[7:5]	Reserved	0	Must be set to 0.
4	SWTOLIN_EN	0	0 = drive mode is defined by the DRV_MODE bit in the mode register. 1 = moves in switched mode and stays in linear mode (this bit has priority over the DRV_MODE bit).
3	LOW_VBAT_DIS	0	0 = low supply shutdown circuitry enabled. 1 = low supply shutdown circuitry disabled.
2	OVER_CURR_DIS	0	0 = overcurrent circuitry enabled. 1 = overcurrent circuitry disabled.
1	RING_CTRL	0	0 = direct drive. 1 = ARC enabled.
0	SW_RESET	0	1 = an immediate reset of all registers to their default values. This bit is reset to 0 automatically. This bit is fully asynchronous to all bits in this register. Any active sequence is interrupted, and then all registers are reset. This bit has the highest priority of all the bits in the register.

Table 13. VCM_CODE_MSB Register, Address = 0x03, Reset = 0x00, Type = R/W

Bits	Name	Reset	Description
[7:2]	Reserved	000000	Must be set to 000000.
[1:0]	D[9:8]	00	DAC output MSB.

Table 14. VCM_CODE_LSB Register, Address = 0x04, Reset = 0x00, Type = R/W

Bits	Name	Reset	Description
[7:0]	D[7:0]	0	DAC output LSB. The move is initiated (either in linear or switched fashion) after both registers, VCM_CODE_MSB and VCM_CODE_LSB, are written to.

Table 15. Status Register, Address = 0x05, Reset = 0x00, Type = R

Bits	Name	Reset	Description
[7:2]	Reserved	000000	Must be set to 000000.
1	LOW_VBAT	0	Must be disabled ('1')when VDD≤2.3V before writing to a code different to 0x000 to the VCM_CODE registers. 1 = undervoltage lockout. If LOW_VBAT drops below 2.27 V (typical), the VCM_CODE_MSB and VCM_CODE_LSB registers are reset to their default values (0x00) and the part enters power-down mode. This bit is automatically cleared the next time the user writes to the VCM_CODE_MSB and VCM_CODE_LSB registers and VDD is above 2.31 V (typical).
0	OVER_CURR	0	1 = overcurrent lockout. If the current at ISOURCE exceeds 200 mA ± 20%, the VCM_CODE_MSB and VCM_CODE_LSB registers are reset to their default values (0x00) and the part enters power-down mode. This bit is automatically cleared the next time the user writes to the VCM_CODE_MSB and VCM_CODE_LSB registers and ISOURCE is below 200 mA ± 20%.

Table 16. Mode Register, Address = 0x06, Reset = 0x01, Type = R/W

Bits	Name	Reset	Description		
7	EMI	0	0 = EMI reduction on. 1 = EMI reduction off.		
6	ARC-RES1.5	0	0 = ARC-RES1.5 disabled. 1 = ARC-RES1.5 enabled (Bit ARC_MODE is ignored).		
5	CLK_RANGE	0	0 = Clock Range 1 (1.11 MHz to 5 MHz). 1 = Clock Range 2 (555 kHz to 1 MHz).		
[4:2]	CLK_DIV[2:0]	000	These bits set the clock frequency of the switched driver.		
			CLK_DIV	**CLK_RANGE = 0**	**CLK_RANGE = 1**
			111	5.00 MHz	
			110	3.33 MHz	
			101	2.50 MHz	
			100	2.00 MHz	1.00 MHz
			011	1.66 MHz	830 kHz
			010	1.42 MHz	710 kHz
			001	1.25 MHz	625 kHz
			000	1.11 MHz	555 kHz
1	DRV_MODE	0	0 = switched. 1 = linear.		
0	ARC_MODE	1	0 = ARC-RES1 1 = ARC-RES2 Ignored when ARC-RES1.5 = 1.		

Table 17. VCM_FREQ Register, Address = 0x07, Reset = 0x80, Type = R/W

Bits	Bit Name	Reset	Description
[7:0]	VCM_FREQ[7:0]	10000000	In direct load mode, VCM_FREQ is ignored. The VCM resonance frequency is f_{RES} = 1/(51.2 µs × (VCM_FREQ + 128)). VCM_FREQ = 0x00 → f_{RES} = 152.6 Hz. VCM_FREQ = 0xFF → f_{RES} = 51.0 Hz.

Table 18. VCM_THRESHOLD Register, Address = 0x08, Reset 0x08, Type = R/W

Bits	Bit Name	Reset	Description
[7:0]	VCM_THRESHOLD[7:0]	00001000	The VCM threshold is programmed using eight bits. The real threshold is nine bits wide and is obtained from the register value: register value (8 bits) = D7 to D0 → threshold value (9 bits) = {D7 to D0, 0}; therefore, the real threshold is double the value contained in this register.