S5K4BAFB

(EVT1)

Implemented Auto Focus Algorithm with internal ROM

1/4” UXGA CMOS Image Sensor with an Embedded Image Signal Processor

Data Sheet
(Rev. 003)

DOCUMENT REVISION HISTORY

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0.01	07-03-20	Y.B.Kim G.E.Sung	-Modified IIC_ID description (Page9) -Reg. Map AF Page 0Eh, 13h added, <7.97h> <20.01h> <22.D7h> descriptions modified. -Package Informations removed.
0.02	07-05-07	Y.B.Kim J.C.Hong	-Modified E-Fuse Spec & Reg. Map (Page 52, 53, 87) -Modified DC Characteristics (Page60, 61 V_{DDIO1} Min/Max Value and Note) -Added Package Pin Configuration (Page11) -Modified Power Up Sequence (Page53~55) -Modified AC Characteristics (Page62) -Modified DC Characteristics (Page60)
0.03	07-07-26	Y.B.Kim	-Modified AC Characteristics (Page62) -Modified Pad Drive Strength Control (Page85,86 2.4Eh, 2.4Fh)

Contents

DOCUMENT REVISION HISTORY 2
FEATURES 6
GENERAL DESCRIPTION 6
LOGICAL SYMBOL DIAGRAM 7
I/O DESCRIPTION 8
CHIP PAD CONFIGURATION 10
PACKAGE PIN CONFIGURATION 11
PIXEL ARRAY INFORMATION 12
I/O TIMING DESCRIPTION 13
PLL DESCRIPTION (CLKSEL SET TO “1”) 20
FUNCTIONAL DESCRIPTION 22
AUTO FOCUS 40
PWM TIMER 42
PWM OVERVIEW 48
E-FUSE CELL ARRARY STRUCTURE 50
E-FUSE WRITE TIMING 51
E-FUSE READ TIMING 52
POWER UP/DOWN SEQUENCE 53
STAND-BY SEQUENCE 57
IMAGING CHARACTERISTICS 58
ELECTRICAL CHARACTERISTICS 59
PACKAGE INFORMATION (320-CLCC) 63
REGISTER DESCRIPTION 64
1. ARM COMMAND REGISTER MAP (PAGE 00H) 66
2. ISP REGISTER MAP (PAGE 01H) 74
3. CIS REGISTER MAP (PAGE 02H) 83
4. IMAGE FORMAT(1) (PAGE 03H) 87
5. IMAGE FORMAT(2) (PAGE 04H) 89
6. ISP REGISTER MAP (PAGE 05H) 91
7. ODM ZONE REGISTER MAP (PAGE 06H) 98
8. PROGRAM CONSTANT REGISTER MAP (PAGE 07H) 99
9. R SHADE COEFFICIENT REGISTER MAP((PAGE 09H) 103
10. SUPPRESS (PAGE 0BH) 110
11. AF REGISTER MAP(1) (PAGE 0EH) 118
12. AF REGISTER MAP(2) (PAGE 13H) 120
13. IMAGE FORMAT(3) (PAGE 14H) 133
14. BOUNDARY REGISTER MAP (PAGE 15H) 135
15. ISP REGISTER MAP (PAGE 1BH) 136
16. SHADING REGISTER MAP (PAGE 1CH) 147
17. GAMMA & EDGE REGISTER MAP (PAGE 1DH) 149
18. SUPPRESS2 REGISTER MAP (PAGE 1EH) 156
19. AE CONTROL REGISTER MAP (PAGE 20H) 158
20. AWB2 REGISTER MAP (PAGE 22H) 165
21. DIGITAL ZOOM REGISTER MAP (PAGE 28H) 172

List of Figures

Figure 1: Logical Symbol Diagram 7
Figure 2: Chip Pad Configuration 10
Figure 3: Package Pin Configuration 11
Figure 4: Pixel Array Information 12
Figure 5: ITU-R.601 YCbCr Data Output Timing 13
Figure 6: ITU-R.656 YCbCr Data Output Timing 13
Figure 7: RGB565 Data Out Timing 14
Figure 8: CIS Raw Data Output Timing 14
Figure 9: IIC General Timing 15
Figure 10: IIC Write Timing 16
Figure 11: IIC Multi-byte Write Timing 17
Figure 12 : IIC Read Timing 18
Figure 13: IIC Multi-byte Read Timing 19
Figure 14: PLL Block Diagram 20
Figure 15: MCLK Timing 21
Figure 16: Functional Block Diagram 22
Figure 17: Relative Channel Gain 23
Figure 18: Physical Pixel Array 24
Figure 19: Horizontal Mirror and Vertical Flip 26
Figure 20: Sub-Sampled readout 27
Figure 21: Rolling Shutter Operation (ERS/No Bulb, FSM) 29
Figure 22: Rolling Shutter Operation (ERS/No Bulb, Timing) 30
Figure 23: Rolling Shutter Operation (ERS Bulb, FSM) 31
Figure 24: Rolling Shutter Operation (ERS Bulb, Timing) 32
Figure 25: Mechanical Shutter Operation (GRS/No Bulb, FSM) 33
Figure 26: Mechanical Shutter Operation (GRS/No Bulb, Timing) 34
Figure 27: Mechanical Shutter Operation (GRS Bulb, FSM) 35
Figure 28: Mechanical Shutter Operation (GRR/Bulb, Timing) 36
Figure 29: AF Interface 40
Figure 30: Functional Block Diagram For AF 41
Figure 31: A simple example of a PWM cycle 42
Figure 32: Basic PWM Timer Operation 43
Figure 33: Example of a timer operation 44
Figure 34: Example of double buffering feature (Fixed TCMPBn) 45
Figure 35: Example of double buffering feature (Fixed TCNTBn) 45
Figure 36: Prescaler & Divider 46
Figure 37: Inverter on/off 47
Figure 38: The Waveform when a deadzone feature is enabled 47
Figure 39: PWM 1 CYCLE TIMING 48
Figure 40: E-Fuse Array 50
Figure 41: E-Fuse Program Mode 51
Figure 42: E-Fuse Read Mode 52
Figure 43: Power Up Sequence for External Clock Using Internal Reaulator 53
Figure 44: Power Up Sequence for External Clock Not-Using Internal Regulator 53
Figure 45: Power Up Sequence for PLL Clock Using Internal Regulator 54
Figure 46: Power Up Sequence for PLL Clock Not-Using Internal Regulator 54
Figure 47: Power Up Sequence for only one slave operation Using Internal Regulator 55
Figure 48: Power Up Sequence for only one slave operation Not-using Internal Regulator 55

Figure 49: Power Down Sequence Using Internal Regulator 56
Figure 50: Power Down Sequence Not-using Internal Regulator 56
Figure 51: Stand-By Sequence 57
Figure 52: Output Timing 62
Figure 53: Package Information (320 CLCC) 63

List of Tables

Table 1: I/O Description 8
Table 2: Imaging Characteristics 58
Table 3: Absolute Maximum Rating 59
Table 4: DC Characteristics 59
Table 5: Electrostatic Characteristics 61
Table 6: AC Characteristics 62

FEATURES

- Optical size: 1/4 inch
- Pixel size: 2.25 um
- Effective resolution: 1600 (H) x 1200 (V), UXGA
- Line progressive read out
- Panning and cropping
- Vertical and horizontal flip mode
- Continuous and single frame capture mode
- Averaging sub-sampling (x2) and digital sub-sampling (x2, x4)
- Output format: 8-Bit ITU-R.656/601 (4:2:2 YCbCr), 565RGB, CIS Raw Data
- Max. frame rate: 15fps @ UXGA
- Color correction
- Edge enhancement
- Lens shading correction
- Programmable gamma correction
- Image scaling down (SXGA, VGA, QVGA, QQVGA, CIF, QCIF)
- Auto focus (AF)
- Auto exposure (AE)
- Auto white balance (AWB)
- Auto flicker correction
- Auto defect correction
- Auto dark level compensation
- Built-in test pattern generation
- Xenon and LED type flash support
- Standby mode for power saving
- I^2C bus control interface
- Operating temperature: -20°C to +60°C
- Supply voltage: 2.8V for analog and 2.8V ~ 1.8V for I/O, 1.8V/1.5V for digital

GENERAL DESCRIPTION

The S5K4BAFB is a highly integrated UXGA camera chip which includes CMOS image sensor (CIS) and Image Signal Processor (ISP). It is fabricated by SAMSUNG 0.13μm CMOS image sensor process developed for imaging application to realize high-efficiency and low-power photo sensor. The sensor consists of 1600 x 1200 effective pixels which meet with 1/4 inch optical format. The CIS has on-chip 10-bit ADC arrays to digitize the pixel output and also on-chip Correlated Double Sampling (CDS) to reduce Fixed Pattern Noise (FPN) drastically. The ISP performs sophisticated image processing functions including color recovery and correction, edge enhancement, lens shading correction, programmable gamma correction, auto defect correction, auto flicker correction, auto focus (AF), auto exposure (AE), auto white balance (AWB), and image scaling. The AF, AE and AWB functions are preformed by an embedded RISC processor. The host controller is able to access and control this device via I^2C bus. The S5K4BAFB is suitable for low power camera module with 2.8V/1.5V power supply.

LOGICAL SYMBOL DIAGRAM

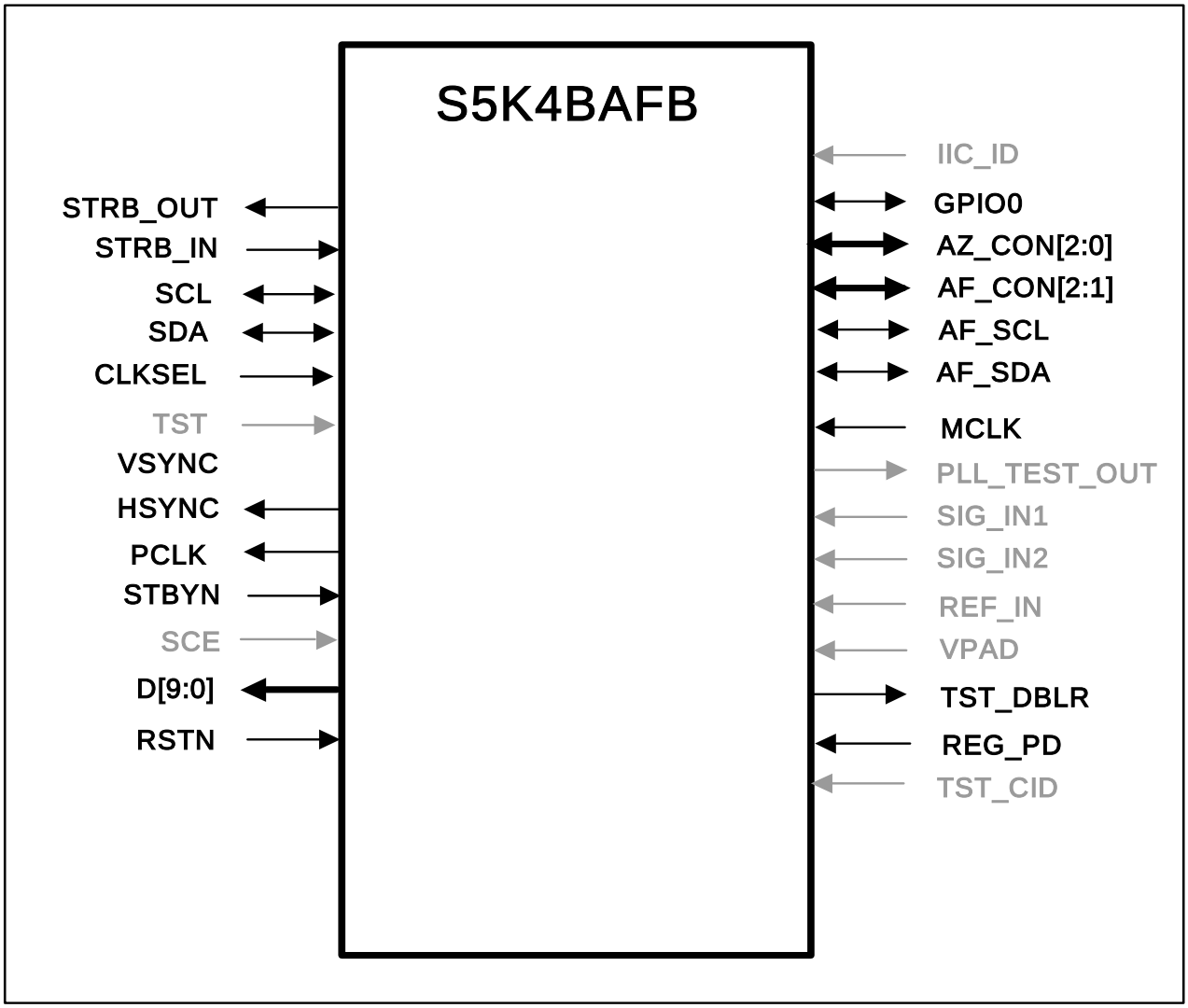


Figure 1: Logical Symbol Diagram

I/O DESCRIPTION

Table 1: I/O Description

Pad No	Pad Name	I/O	Description
3	**STRB_OUT**	O	Flash Strobe Output
4	**STRB_IN**	I	Flash Strobe Input (Active high, Set to '0' or open if not used)
5	**SCL**	B	I2C Clock/Data for Backend Processor
6	**SDA**	B	
7	**CLKSEL**	I	Set to '1' in normal mode("1" : PLL use, "0" : External MCLK use)
10	**TST**	I	Test Mode Selection (Set to '0' in normal mode, Set to '1' in CIS raw data output mode)
11	**HSYNC**	Oz	Horizontal Sync Output
12	**VSYNC**	Oz	Vertical Sync Output
13	**PCLK**	Oz	Pixel Clock Output
14	**D0**	Oz	Pixel Data Output (D0: LSB, D7: MSB)
15	**STBYN**	I	Stand-By Mode (Active low, Set to '1' if not used)
16	**SCE**	I	Used for test (Set to '0' or open in normal mode)
21	**D1**	Oz	Pixel Data Output (D0: LSB, D7: MSB)
22	**D2**	Oz	
23	**D3**	Oz	
24	**D4**	Oz	
25	**D5**	Oz	
26	**D6**	Oz	
27	**D7**	Oz	
28	**D8**	Oz	Open in normal operation mode (factory use only)
29	**D9**	Oz	Connected in CIS only raw data output mode (D0: LSB, D9: MSB)
31	**RSTN**	I	Master Reset (Active low)
36	**TST_CID**	I	Chip ID Test
37	**REG_PD**	I	Regulator Power Down (Set to '0' in Internal Regulator mode, Set to '1' in Regulator Power Down mode)
38	**TST_DBLR**	I	Analog Voltage Pad 2
44	**VPAD**	I	Analog Voltage Pad 1
45	**REF_IN**	I	ADC Teg Reference Input
48	**SIG_IN1**	I	ADC Teg Signal Input1
49	**SIG_IN2**	I	ADC Teg Signal Input2
53	**PLL_TEST_OUT**	O	PLL Pump Out
54	**MCLK**	I	Master Clock (Default: 27MHz, if lower frequencies are used, change PLL register settings)
55	**AF_SCL**	B	I2C Clock/Data for Actuator Driver Control as master At CIS only raw data mode I2C Clock/Data for Backend Processor
56	**AF_SDA**	B	
57	**AF_CON1**	B	Actuator Driver Control Output (PWM Channel – 1,2) or GPIO
58	**AF_CON2**	B	

59	**AZ_CON0**	B	Actuator Driver Control Output (PWM Channel – 3,4,5) or GPIO
60	**AZ_CON1**	B	
61	**AZ_CON2**	B	
64	**GPIO0**	B	General Purpose I/O
65	**IIC_ID**	I	IIC ID Selection, Set to “0” IIC ID is 5Ah, Set to “1” IIC ID is 52h

34,69	**VDD_REG**	P	Regulator Power for Core Digital (1.8V)
2,9,35, 62,68	**VDD15**	P	Power for Core Digital (1.5V) or Capacitor
1,8,33, 63,70	**VSS_REG**	P	Digital Ground
30	**VDD_FS**	P	Power for Fail Safe I/O (2.8V ~ 1.8V)
32	**VSS_FS**	P	Ground for Fail Safe I/O
17,18, 67	**VDDIO**	P	I/O Digital Power (2.8V ~ 1.8V)
19,20, 66	**VSSIO**	P	I/O Digital Ground
39,42, 43,50, 52	**VDDA**	P	Analog Power (2.8V)
40,41, 46,47 51	**VSSA**	P	Analog Ground

[NOTE]
Oz : Tri-state Output

CHIP PAD CONFIGURATION

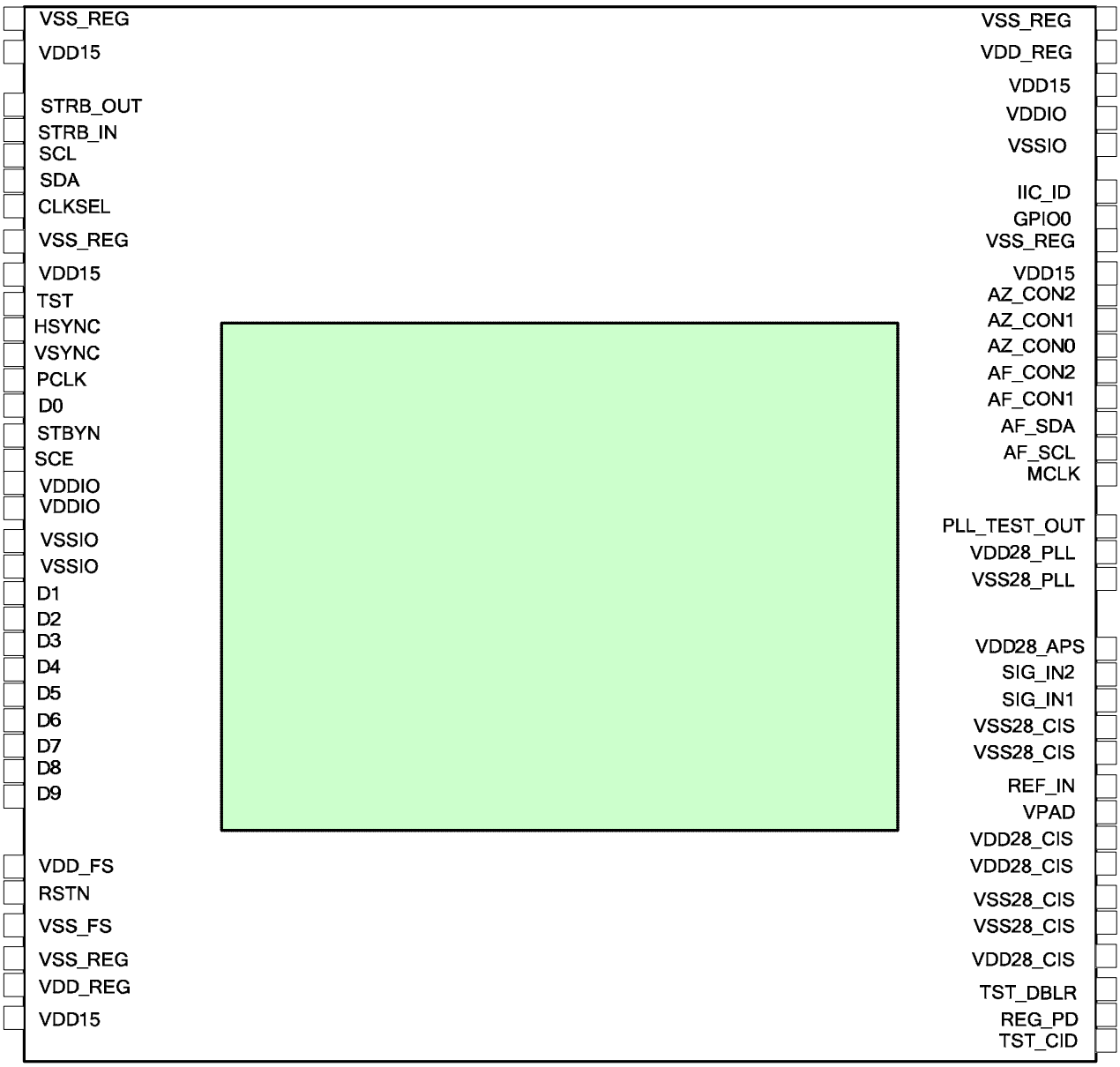


Figure 2: Chip Pad Configuration

PACKAGE PIN CONFIGURATION

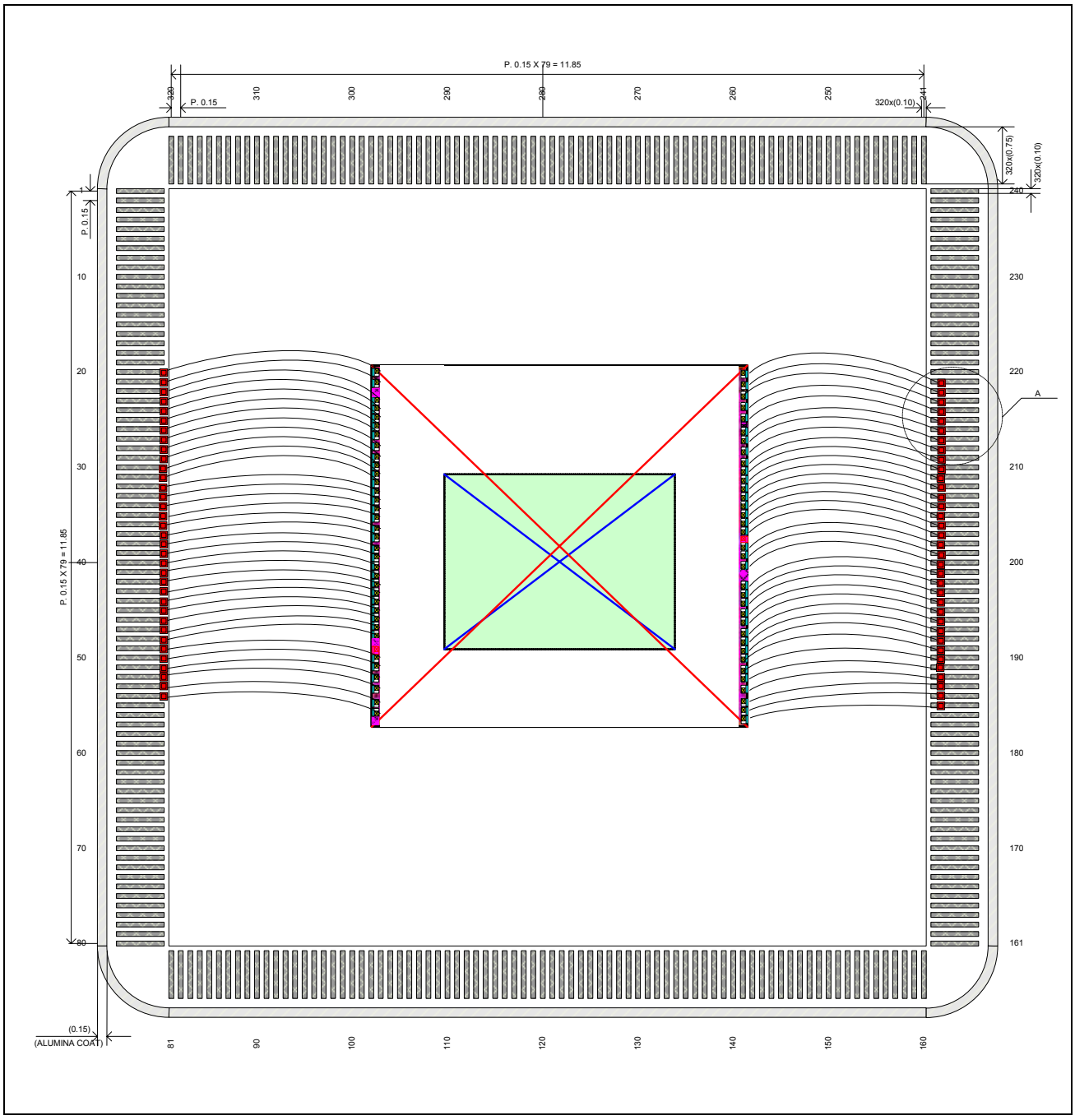


Figure 3: Package Pin Configuration

PIXEL ARRAY INFORMATION

(TOP VIEW ON CHIP DISPLAYED IMAGE WILL BE FLIPPED.)

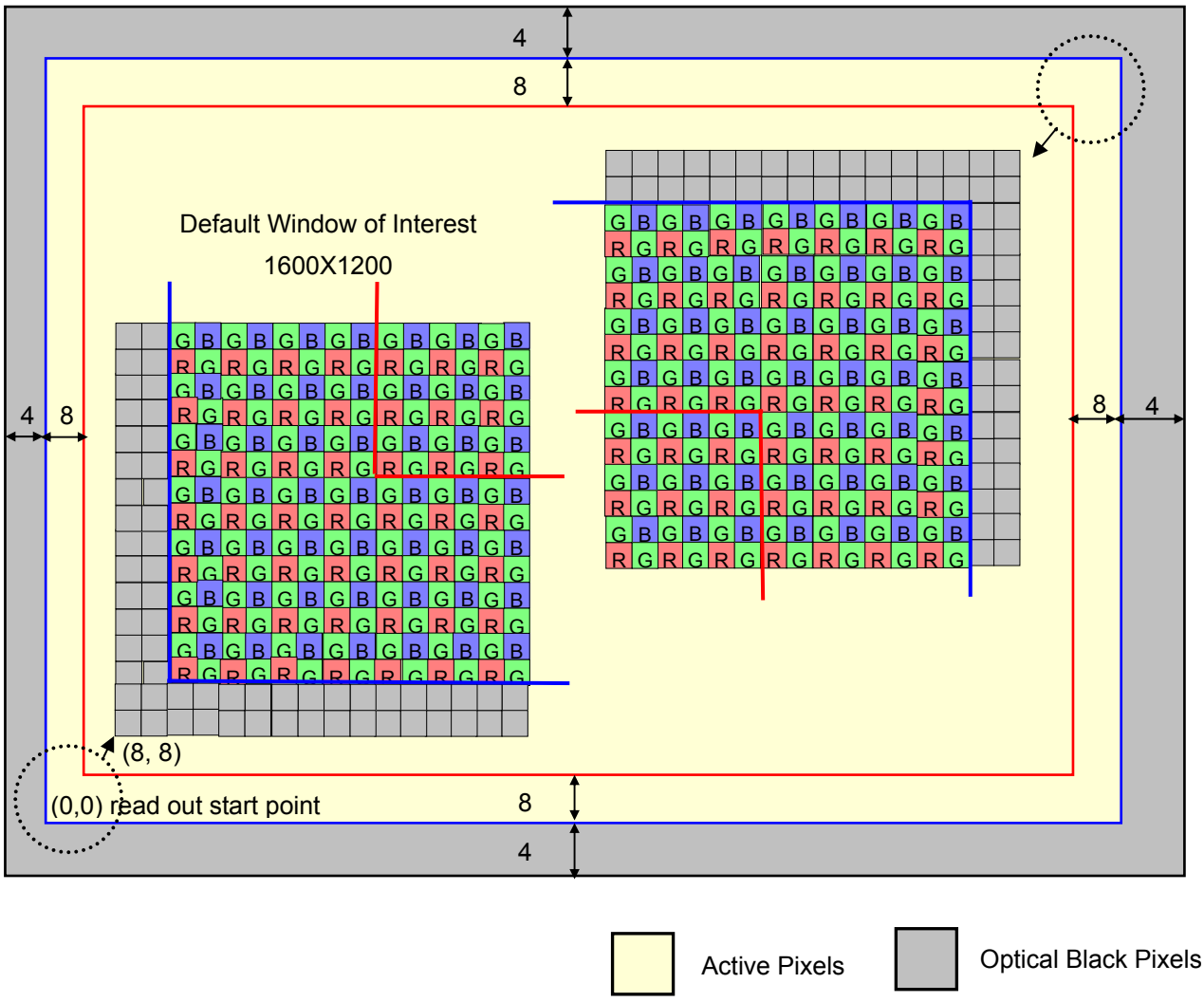


Figure 4: Pixel Array Information

I/O TIMING DESCRIPTION

Video Output Timing

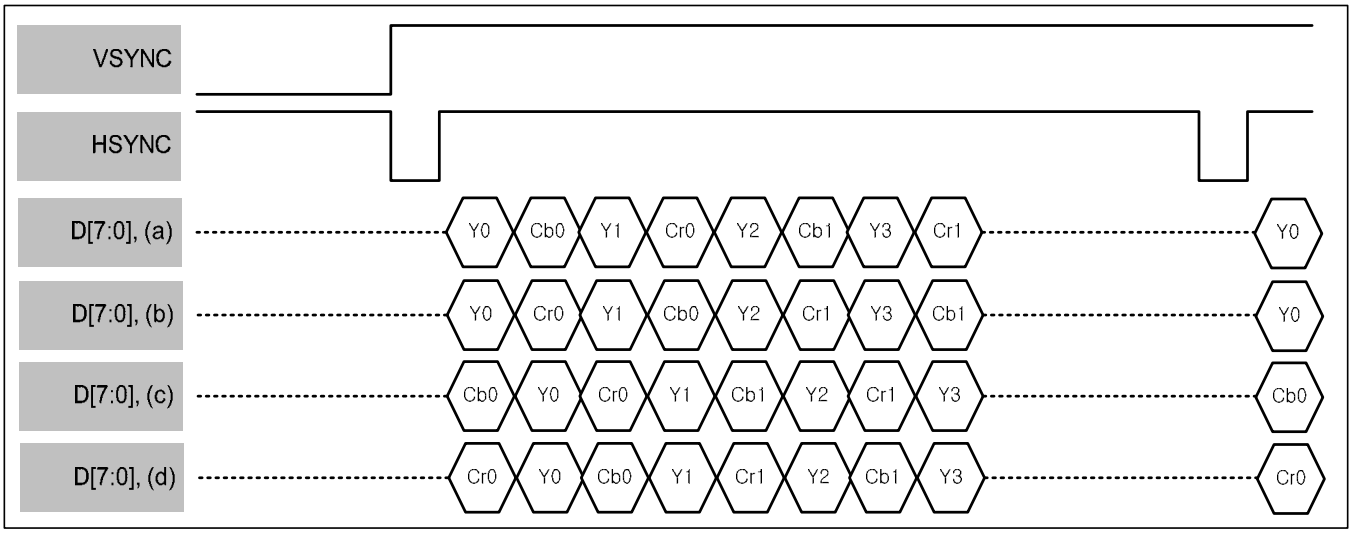
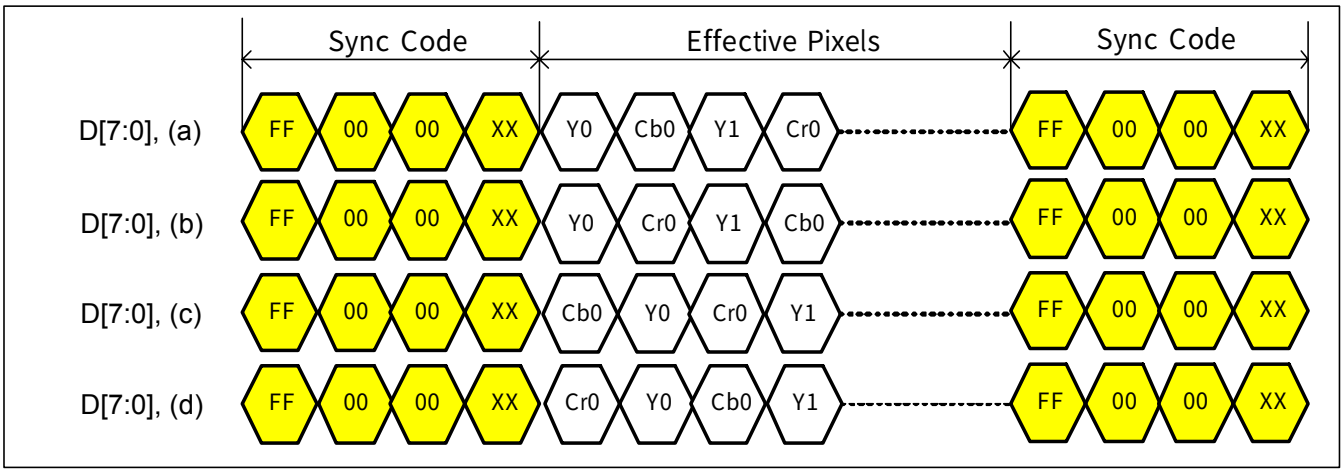


Figure 5: ITU-R.601 YCbCr Data Output Timing



[NOTE] XX = C7, DA, EC, F1
C7 : Start code of line in vertical active
DA : End code of line in vertical active
EC : Start code of line in vertical blank
F1 : End code of line in vertical blank

Figure 6: ITU-R.656 YCbCr Data Output Timing

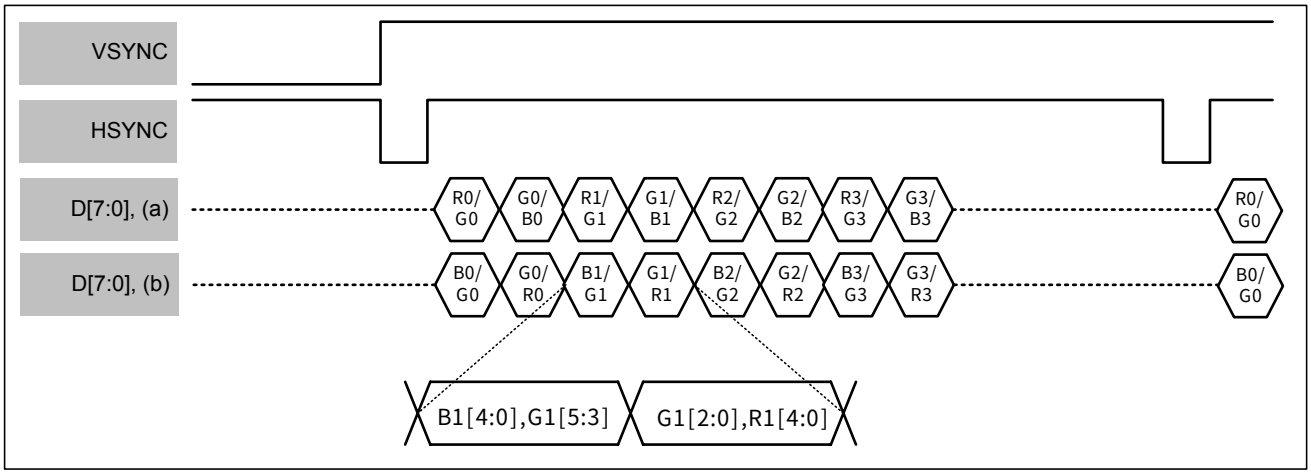
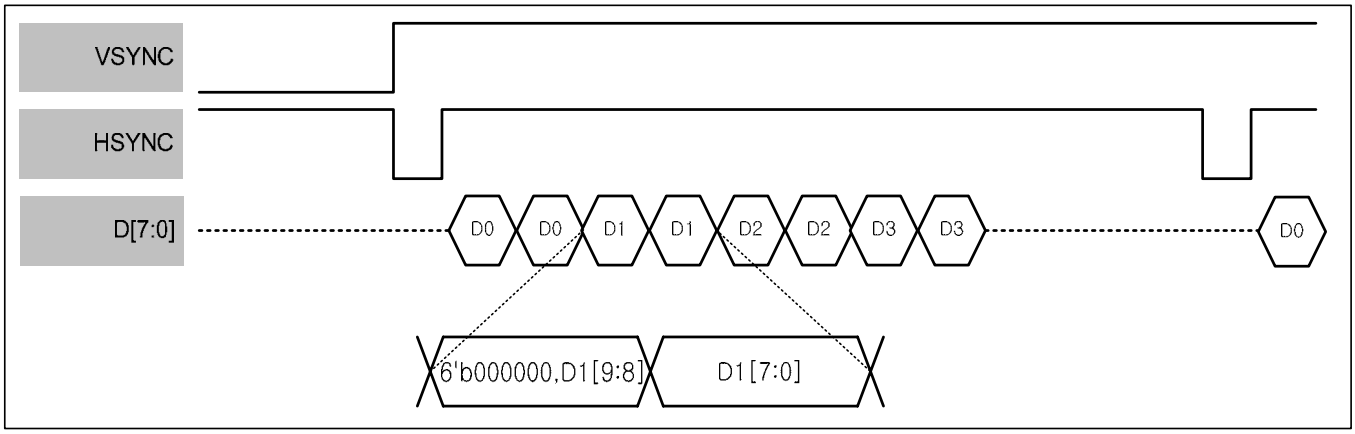
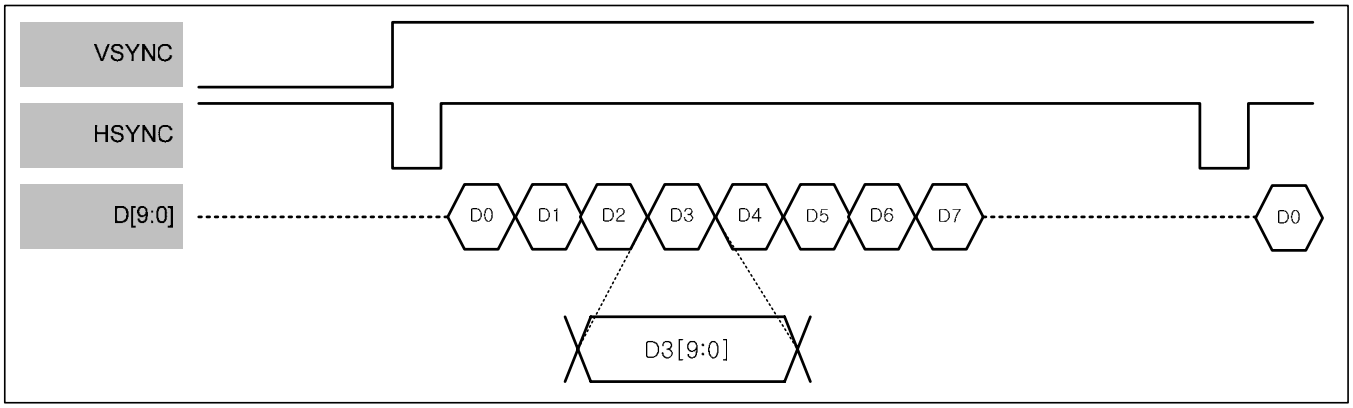


Figure 7: RGB565 Data Out Timing



[NOTE] It shows 10-bit CIS raw data output timing.



[NOTE] It works at raw data output mode (CIS only test mode),
TST pin is connected to VDDIO “1”

Figure 8: CIS Raw Data Output Timing

Control Interface Timing

IIC Bus Overview

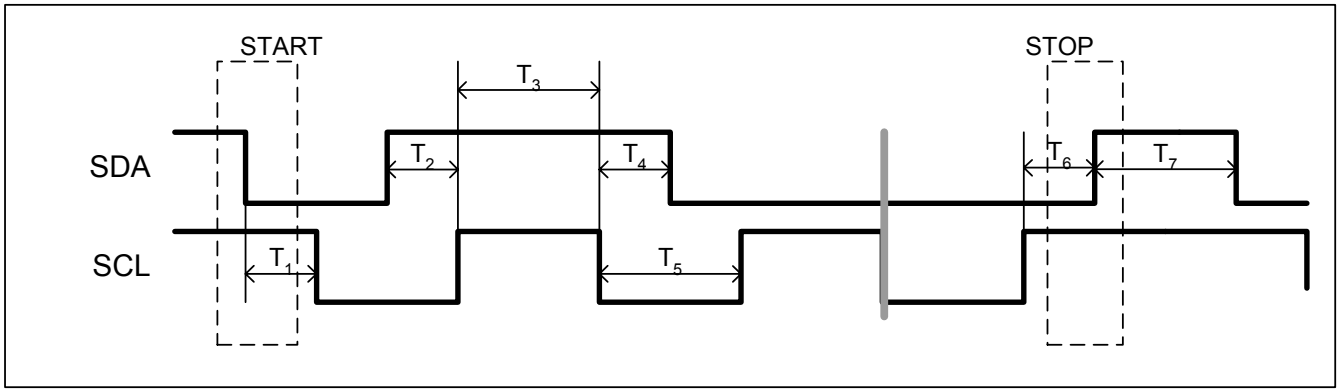
The IIC contains a serial two-wire (half duplex) interface that features bi-directional operation, master or slave mode. The general SDA and SCL are the bi-directional data and clock pins, respectively. These pins are open-drain type ports and will require a pull-up resistor to VDDIO. The SDA bus line may only be changed while SCL is low. The data on the SDA bus line is valid on the high-to-low transition of SCL.

Protocol

The IIC bus interface is composed of following parts. START signal, 7-bit slave device address (0101101b) transmission followed by a read/write bit, an acknowledgement signal from the slave, 8-bit data transfer followed by an acknowledgement signal and STOP signal.

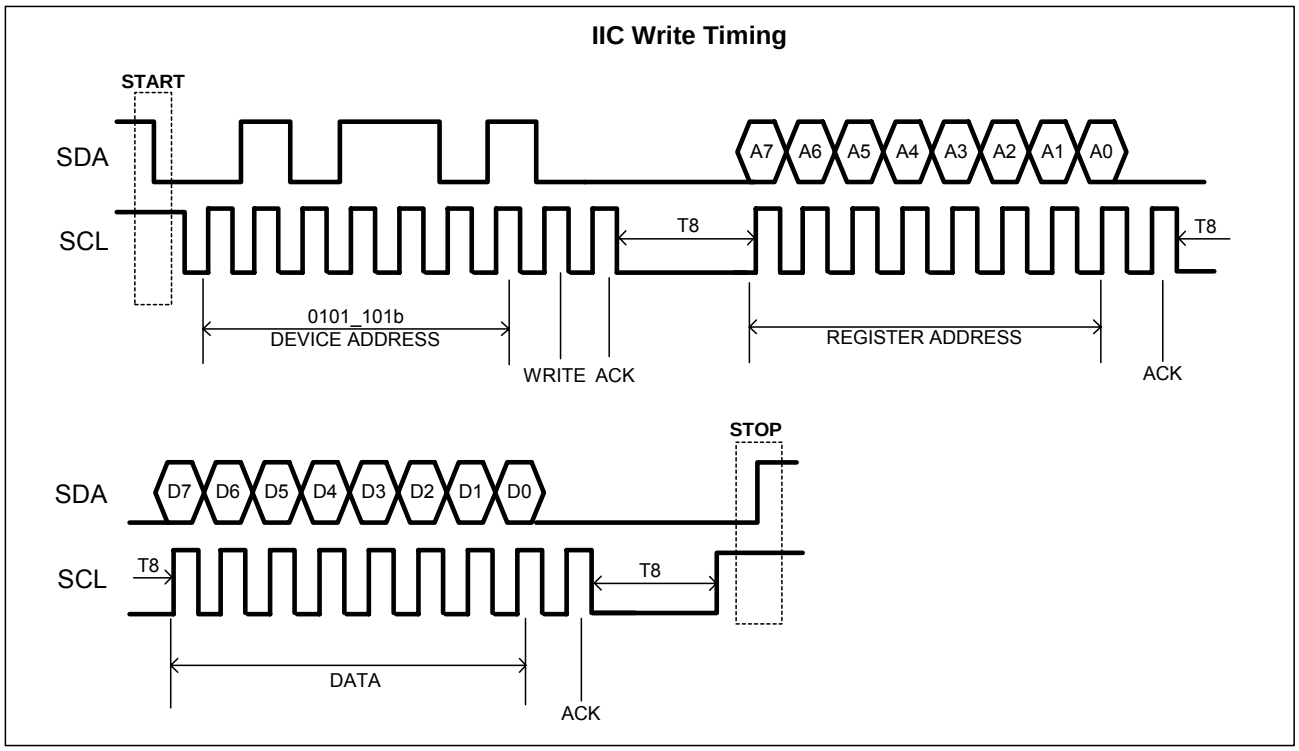
Notice & Usage

The S5K4BAFB internal registers have several pages to expand its address space. Our host interface uses only 8-bit data to assign a register, thus a page setting must be required in advance and its selected page will be kept until changed.



SYMBOL	PARAMETER	MIN	MAX	UNIT
	SCL clock frequency	-	400	KHz
T1	Hold time for START condition	0.6	-	us
T2	Data setup time	100	-	ns
T3	High period of the SCL clock	0.6	-	us
T4	Data hold time	10	-	ns
T5	Low period of the SCL clock	1.3	-	us
T6	Setup time for STOP condition	0.6	-	us
T7	Bus free time between a STOP and START condition	1.3	-	us
	SCL Rise/Fall Time		300	ns
	SDA Rise/Fall Time		300	ns

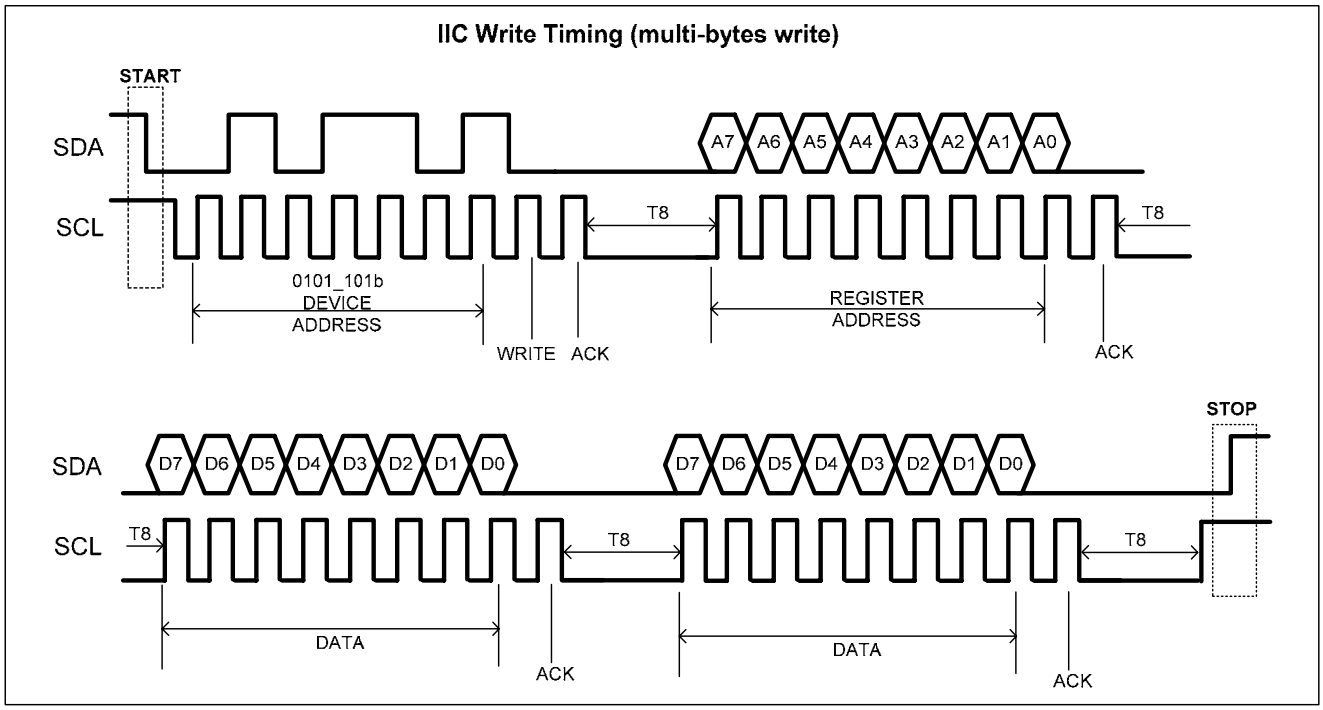
Figure 9: IIC General Timing



SYMBOL	PARAMETER	MIN	MAX	UNIT
T8	Minimum required time for slave Interrupt processing	300	-	cycle
	Minimum required time for slave Interrupt processing (For Sensor only)	20	-	cycle

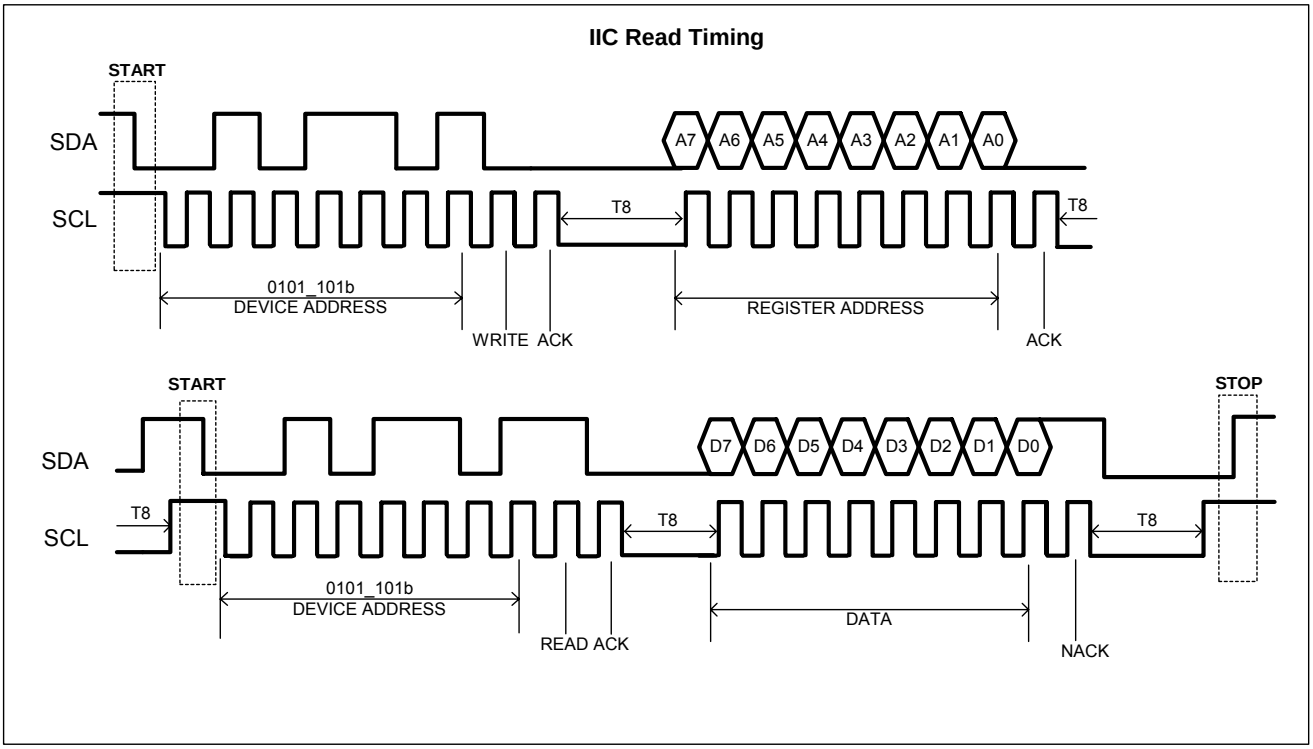
[NOTE]
(1) Cycle: ARM cycle time
(2) While the S5K4BAFB has been in an interrupt service routine, it may hold the clock line SCL LOW to force the master into a wait state. If a master does NOT support this standard protocol, the master ought to obey the timing condition, T8 or wait for the releasing of clock line SCL before the continuous data transmission to ensure the stable communication.
(3) Example : If you want to write data(12h) to address 01h in page 1, IIC command is as follows,
If IIC_ID is Low
<5Ah> <FCh> <01h> : page setting
<5Ah> <01h> <12h> : 1-byte write
If IIC_ID is High
<52h> <FCh> <01h> : page setting
<52h> <01h> <12h> : 1-byte write
(4) Sequential Write mode is supported.
(5) External pull-up resistor 2.2kΩ is recommended.

Figure 10: IIC Write Timing



[NOTE]
(1) cycle : ARM cycle time
(2) While the S5K4BAFB has been in an interrupt service routine, it may hold the clock line SCL LOW to force the master into a wait state. If a master does NOT support this standard protocol, the master ought to obey the timing condition, T8 or wait for the releasing of clock line SCL before the continuous data transmission to ensure the stable communication.
(3) Sequential Write mode is supported.
When using Sequential Write mode, data should be enough size, not to exceed the end of the page address.
(4) Example : If you want to write multi-byte data(34h, BAh, 54h) to address 01h, 02h, 03h in page 1,
IIC command is as follows,
If IIC_ID is Low
<5Ah> <FCh> <01h> : page setting
<5Ah> <01h> <34h> <BAh> <54h> : 3-bytes write
If IIC_ID is High
<52h> <FCh> <01h> : page setting
<52h> <01h> <34h> <BAh> <54h> : 3-bytes write
(5) External pull-up resistor 2.2kΩ is recommended.

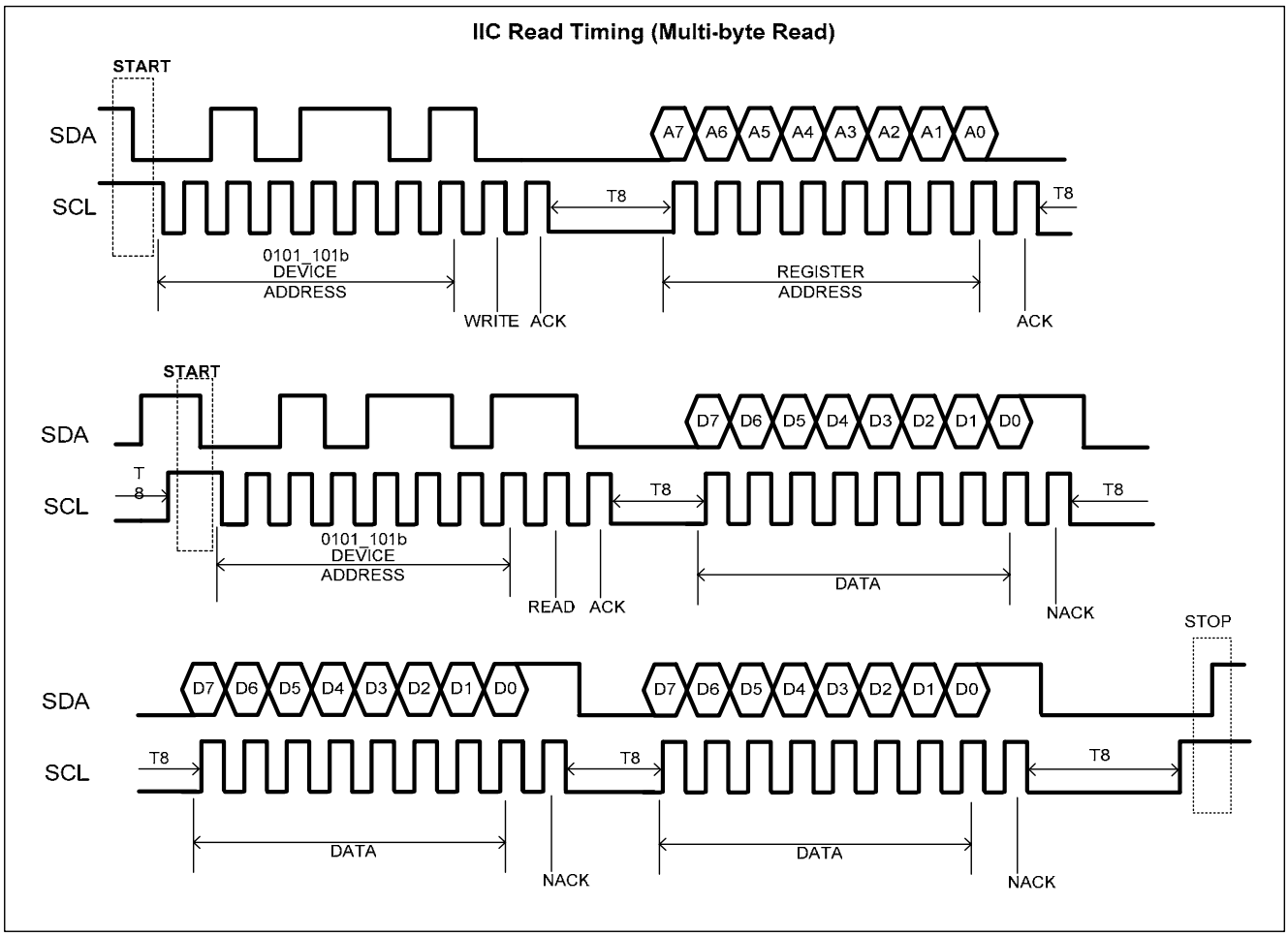
Figure 11: IIC Multi-byte Write Timing



SYMBOL	PARAMETER	MIN	MAX	UNIT
T8	Minimum required time for slave Interrupt processing	300	-	cycle
	Minimum required time for slave Interrupt processing (For Sensor only)	20	-	cycle

[NOTE]
(1) cycle : ARM cycle time
(2) While the S5K4BAFB has been in an interrupt service routine, it may hold the clock line SCL LOW to force the master into a wait state. If a master does NOT support this standard protocol, the master ought to obey the timing condition, T8 or wait for the releasing of clock line SCL before the continuous data transmission to ensure the stable communication.
(3) Example : If you want to read 1-byte data from address 01h in page 1, IIC command is as follows,
If IIC_ID is Low
<5Ah> <FCh> <01h> : page setting
<5Ah> <01h> <5Bh> <XXh> : 1-byte read
If IIC_ID is High
<52h> <FCh> <01h> : page setting
<52h> <01h> <53h> <XXh> : 1-byte read
(4) A repeated START is required

Figure 12 : IIC Read Timing



[NOTE]
(1) cycle : ARM cycle time
(2) While the S5K4BAFB has been in an interrupt service routine, it may hold the clock line SCL LOW to force the master into a wait state. If a master does NOT support this standard protocol, the master ought to obey the timing condition, T8 or wait for the releasing of clock line SCL before the continuous data transmission to ensure the stable communication.
(3) Example : If you want to read 3-bytes data from address 01h in page 1, IIC command is as follows,
If IIC_ID is Low
<5Ah> <FCh> <01h> : page setting
<5Ah> <01h> <5Bh> <64h> <C1h> <XXh> : 3-byte read
If IIC_ID is High
<52h> <FCh> <01h> : page setting
<52h> <01h> <53h> <64h> <C1h> <XXh> : 3-byte read
(4) A repeated START is required

Figure 13: IIC Multi-byte Read Timing

PLL DESCRIPTION (CLKSEL SET TO “1”)

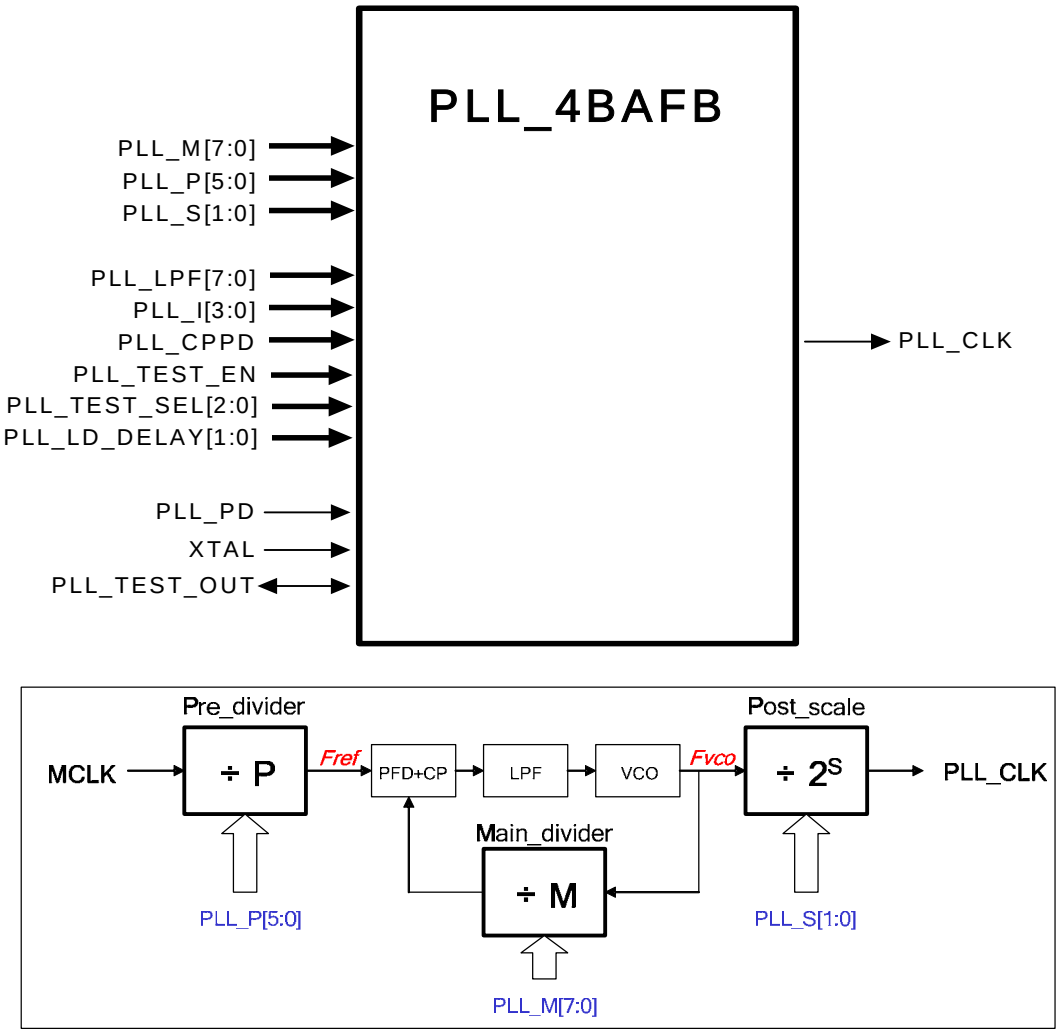


Figure 94: PLL Block Diagram

$$F_{PLL\_CLK} = F_{MCLK} \times \left[\frac{M}{P} \cdot \frac{1}{2^S} \right]$$

F_{MCLK}	$F_{PLL\_CLK,MAX}$	PLL_M[7:0]	PLL_P[5:0]	PLL_S[1:0]
14MHz	46.2MHz	66d	10d	1
27MHz	89.1MHz	66d	10d	1

[NOTE]

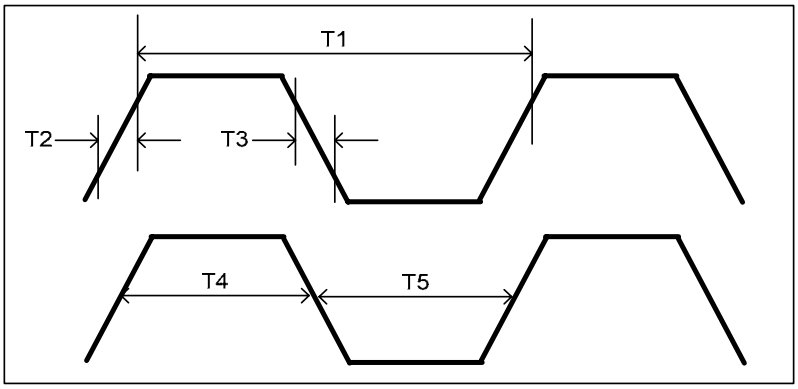
1) Default Setting: M = 66, P = 10, S = 1
2) F_{MCLK} : 14MHz ~ 27MHz, F_{VCO} (MCLK * M / P) Range : 80MHz ~ 210MHz,
3) F_{ref} (F_{MCLK} / P) : 2MHz ~ 12MHz
4) Output frequency synthesis by programmable divider setting

- P value : 2 ~63 by 6-bit pre-divider
- M value : 2~255 by 8-bit main-divider
- S value : 0, 1, 2, 3 by 2-bit post scaler

5) S value can be changed for making the suitable PLL_CLK.
6) Clock Definition

CLOCK SYMBOL	DESCRIPTION
MCLK	External Master Clock Input Using PLL : 14MHz ~ 27MHz Not using PLL : 27MHz ~ 75MHz
DCLK	CIS Internal Clock
PCLK	External Pixel Clock Output

MCLK Description



Parameter		Min	Max	Unit
MCLK Frequency		14	75	MHz
MCLK Period	T1	71.42	13.33	ns
MCLK Rise Time	T2	-	4	ns
MCLK Fall Time	T3	-	4	ns
MCLK Duty Tolerance	max(T4,T5)/min(T4,T5)	1	1.5	-

Figure 15: MCLK Timing

[NOTE]
The conditions for V_{IL} and V_{IH} in the Electrical Characteristics are also applied to MCLK.

FUNCTIONAL DESCRIPTION

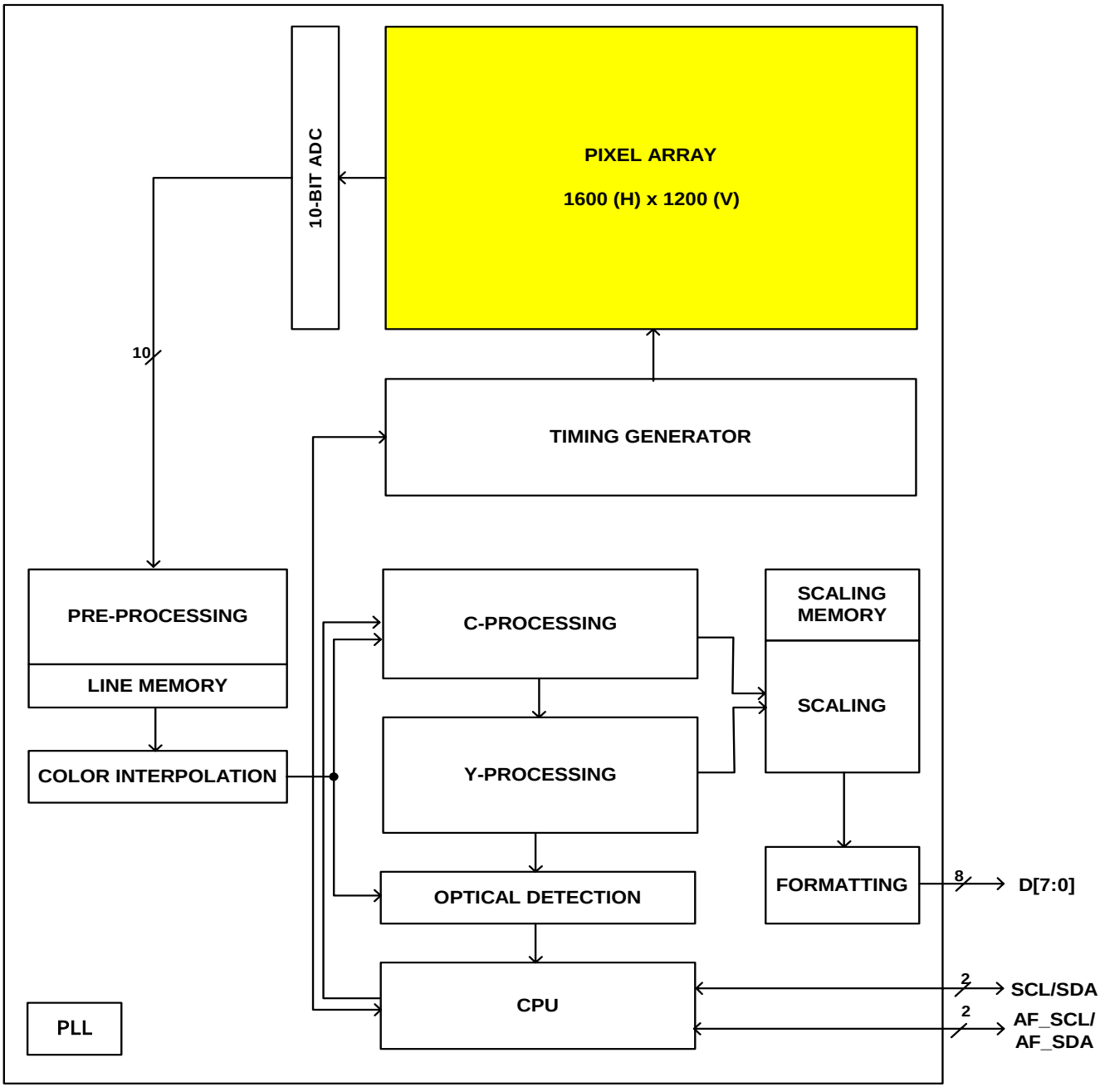


Figure 10: Functional Block Diagram

1. Analog to Digital Converter (ADC)

The image sensor has an on-chip ADC. Column parallel ADC scheme is used for low power analog processing.

1-1. ADC resolution

The default value of ADC resolution is 10bit and can be changed to 9bit or 8bit by control the ADC Resolution Control Register (adc_res, **<2.02h[1:0]>**). Lowering "**adc_res**" register and increasing "**DCLK_div,<2.02h[5:3]>**" register reduce the required minimum line time (*refer to 2.5. Frame Rate Control*). When the number of effective output bits is reduced, upper n-bits of output ports are valid and lower bits always have value of "0".

1-2. Correlated Double Sampling (CDS)

The analog output signal of each pixel includes some temporal random noise caused by the pixel reset action and some fixed pattern noise by the in-pixel amplifier offset deviation. To eliminate those noise components, a correlated double sampling (CDS) circuit is used before converting to digital code. The input signal level of each pixel is determined as the differential value between the pre-reset pixel value and its current charged one. Therefore its value is sampled twice during a pixel period, once for the reference(reset) level detection and then the actual signal level.

1-3. Programmable Gain and Offset Control

The user can control the gain and offset of pixel signal by Gain Control Register (gain_ctrl, <2.33h> ~ <2.36h>) and Offset Control Registers (offset_ctrl, <2.2Fh> ~ <2.32h>) respectively. As increasing the signal gain control register, the ADC conversion range slope becomes decreased and its output code value is increased. The gain increased as following equation but the control range actually needed by user will be less than 8:

Channel Gain = 128 / (128 – Gain Control Register Value[6:0])

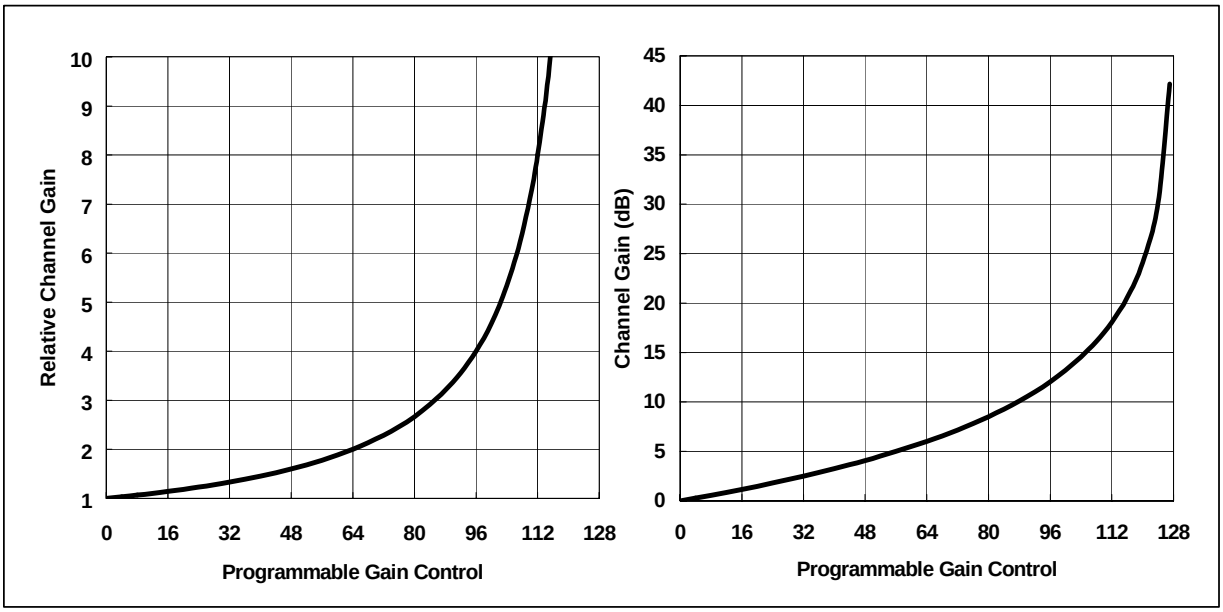


Figure 11: Relative Channel Gain

2. TG function

2-1. CIS Raw Data Output

S5K4BAFB supports 10-bit CIS raw data output by setting external pin TST=1. By applying TST, this product outputs 10-bit pixel raw data instead of 8-bit ISP video data.

2-2. Pixel array addresses

Addressable pixel array is defined as the pixel address range to be read. The Addressable pixel array can be assigned anywhere on the pixel array. The addressed region of the pixel array is controlled by **h_addr_start(<2.0Ch> ~ <2.0Dh>)**, **v_addr_start(<2.10h> ~ <2.11h>)**, **h_addr_end(<2.0Eh> ~ <2.0Fh>)** and **v_addr_end(<2.12h> ~ <2.13h>)** register.

Figure 18. refers to a pictorial representation of the Addressable pixel array on the Physical pixel array.

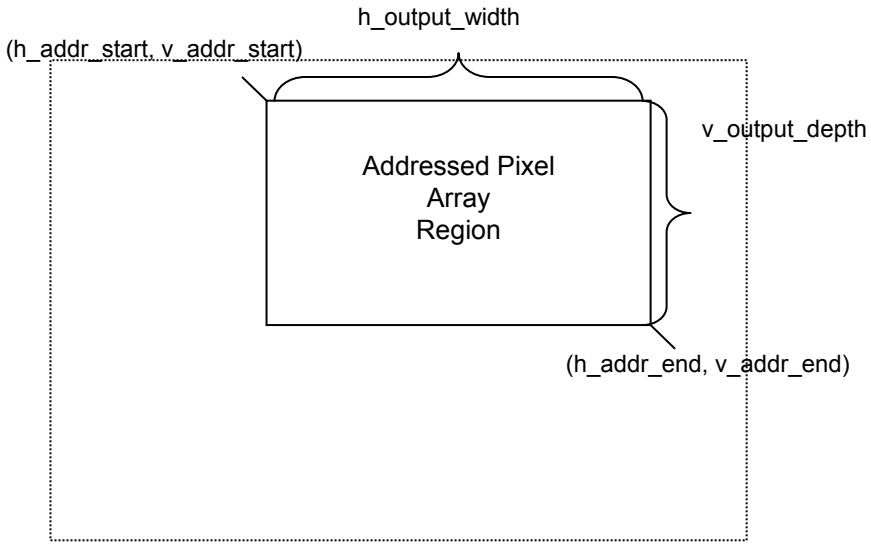


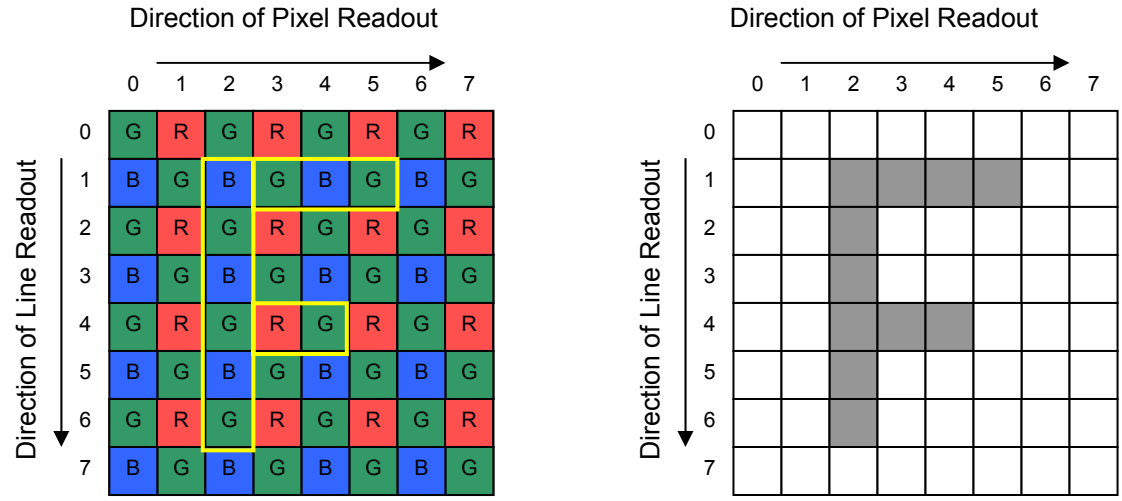
Figure 12: Physical Pixel Array

2-3. Mirror/Flip

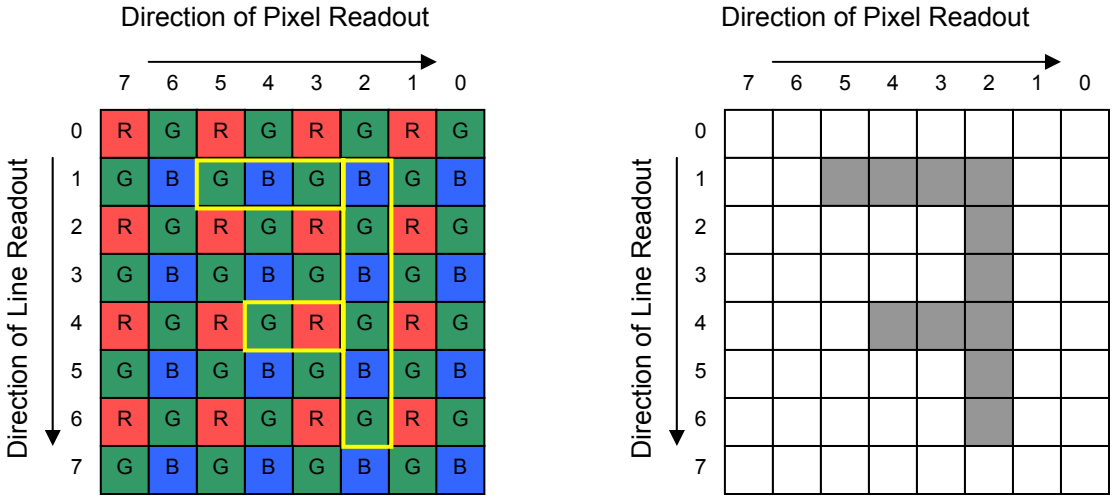
The pixel data are read out from left to right in horizontal direction and from top to bottom in vertical direction normally. By changing the mirror/flip mode, the read-out sequence can be reversed and the resulting image can be flipped like a mirror image. Pixel data are read out from right to left in horizontal mirror mode and from bottom to top in vertical flip mode. The horizontal mirror and the vertical flip mode can be programmed by image orientation register(<0.75h>).

The sensor module support 4 possible pixel readout order

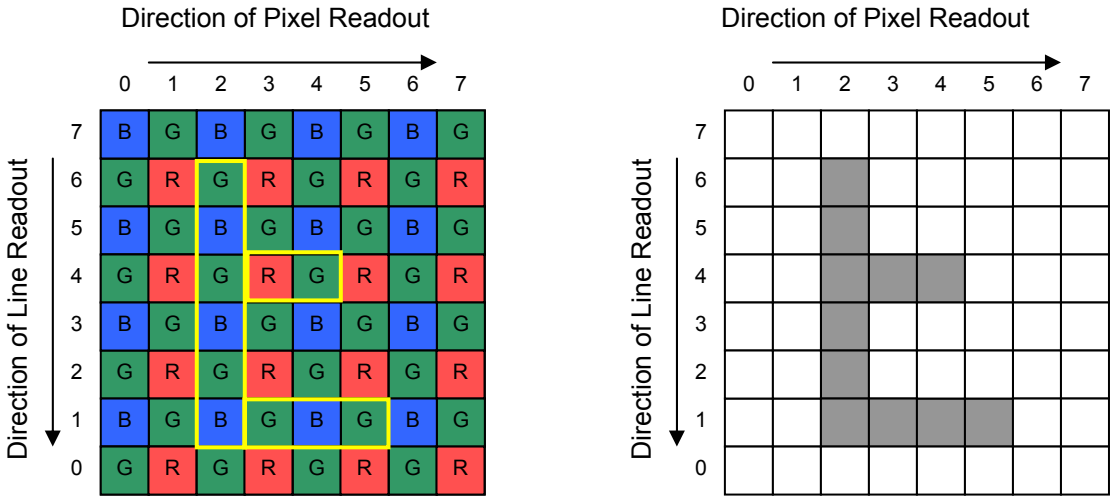
1) Standard readout.
2) Horizontally mirrored readout.
3) Vertical flipped readout.
4) Horizontally mirrored and vertically flipped readout.



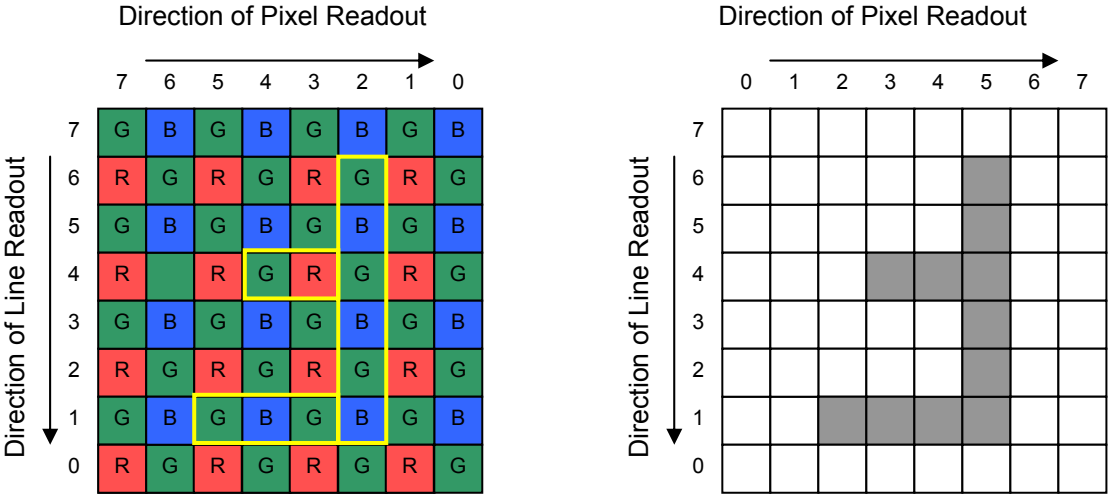
1) Standard Readout



2) Horizontally Mirrored Readout



3) Vertically Flipped Readout



4) Horizontally Mirrored and Vertically Flipped Readout

Figure 13: Horizontal Mirror and Vertical Flip

2-4. Sub-Sampled readout

By programming the x and y odd and even increment register (h_even_inc (<2.14h ~ 2.15h>), h_odd_inc (<2.16h ~ 2.17h>), v_even_inc (<2.18h ~ 2.19h>), v_odd_inc (<2.1Ah ~ 2.1Bh>)). The sensor can be configured to readout sub-sampled pixel data.

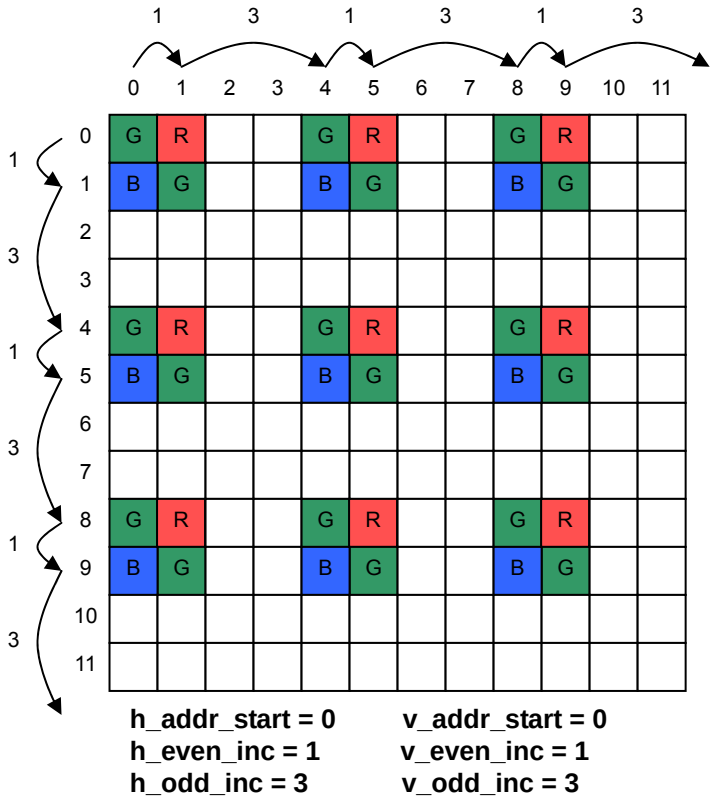


Figure 14: Sub-Sampled readout

2-5. Frame Rate Control (Virtual Frame)

The line rate and the frame rate can be changeable by varying the size of virtual frame. The virtual frame's width and depth are controlled by frame_h_width(<2.04h ~ 2.05h>) and frame_v_depth(<2.06h ~ 2.07h>) register.

Frame rate = MCLK / (frame_h_width * frame_v_depth * 2)

And the horizontal and vertical blanking time (horizontal blanking time: frame_h_width – h_output_width (<2.08h ` 2.09h>), vertical blanking time: frame_v_depth – v_output_depth (<2.0Ah ~ 2.0Bh>)) should be over 70 and 10, respectively.

The detailed restriction of frame_h_width is shown in the followings

RESTRICTION OF FRAME_H_WIDTH

	MINIMUM 1H-PERIOD(DCLK)		
DCLK_DIV[2:0] (<2.02H>[5:3])	10BIT OUTPUT MODE	9BIT OUTPUT MODE	8BIT OUTPUT MODE
0	1716	1204	948
1	1076	820	692
2	756	628	564
3	596	532	500
4	516	484	468

2-6. Integration Time Control (Electronic Shutter Control)

The pixel integration time is controlled by shutter operation. In shutter operation, the amount of time, integration time, is determined by the column Step Integration Time Control Register (col_int_time, <2.22h> ~ <2.23h>) and line Step Integration Time Control Register (line_int_time, <2.20h> ~ <2.21h>).

The total integration time of sensor module can be calculated using the following formula

Total_integration_time =
{(line_int_time * frame_h_width) + col_int_time + 186 } * dclk period [sec]

2-7. Single Frame Capture Mode (SFCM) Integration Time Control

To capture a still image, SFCM can be set by Single Frame Capture Enable Register (**sfcm_mode<2.24h,[0]>**). There are two types of integration mode implemented. In the rolling shutter mode (**grr_mode<2.24h,[1]>**=0), the integration time is controlled by Integration Time Control Registers (when bulb_mode <2.24[2]>=0, **line_int_time{<2.20h>,<2.21h>}**, **col_int_time{<2.22h>,<2.23h>}**) or the external input signal STRB_IN(when bulb_mode<2.24h[2]>=1) (refer to 2-8. Operation mode) . The light integration period for each rows progresses with reading rows. The integration time is expressed as:

Total_integration_time =
{(line_int_time * frame_h_width) + col_int_time + 186 } * dclk period [sec]

In the mechanical shutter mode **(grr_mode<2.24h,[1]>**=1), the integration time for all rows is the same period during the external input signal, STRB_IN is active(when bulb_mode<2.24h[2]>=1) or controlled by Integration Time Control Registers (when bulb_mode<2.24[2]>=0). After Integration time goes to be inactive, the external mechanical shutter should shut off incident light on image sensor and the data readout sequence starts.

2-8. Operation mode

There are two types of operation mode. The two types are CFCM(Continuous Frame Capture Mode) and SFCM(Single Frame Capture Mode), default mode is CFCM. To capture a still image, SFCM can be set by SFCM register and STRB_IN, STRB_OUT pins. There are two types of integration(*) mode implemented. One is a Electronic Rolling Shutter(ERS), Other is a Mechanical Shutter(MS or GRR).

(*)integration = exposure

1. Electronic Rolling Shutter
    1) ERS, SNAPSHOT (No Bulb)

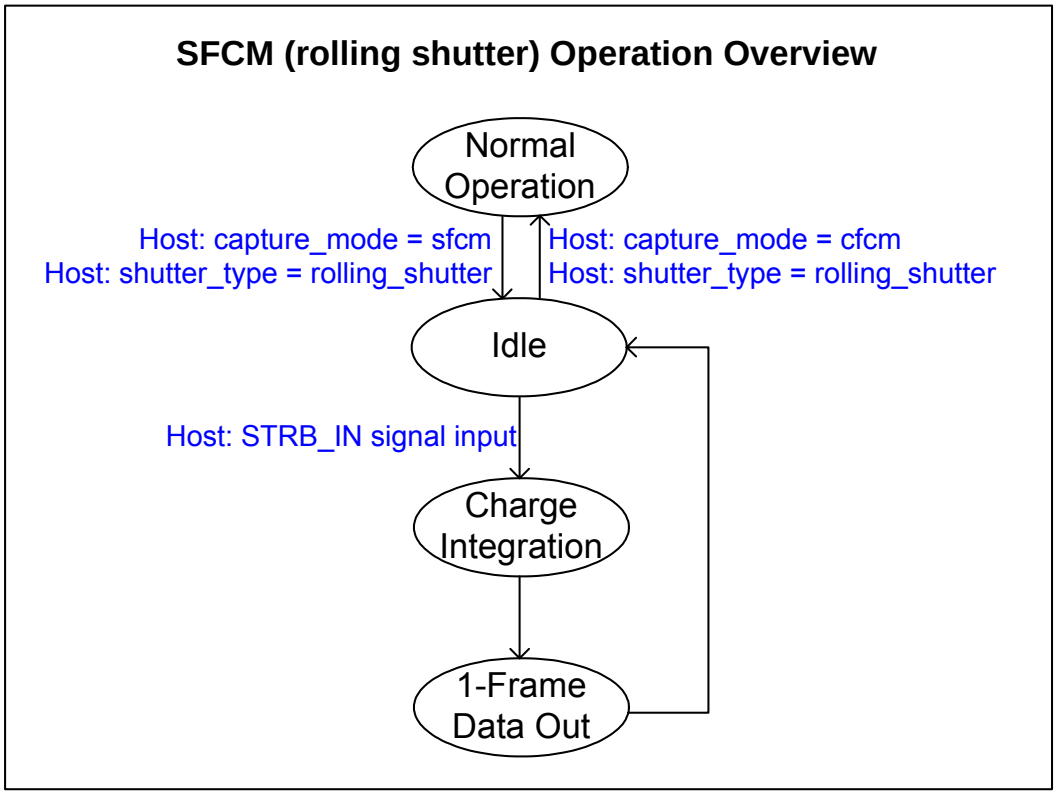


Figure 21: Rolling Shutter Operation (ERS/No Bulb, FSM)

1) SFCM is set by sf_mode register, wait for the releasing of STRB_IN signal.
2) STRB_IN signal is active, the integration time is controlled by Integration time control registers.
3) The integration is finished, the each rows are readout.
4) One frame data is all readout, mode is changed by sf_mode register. (if sf_mode=0, CFCM)

ROLLING SHUTTER

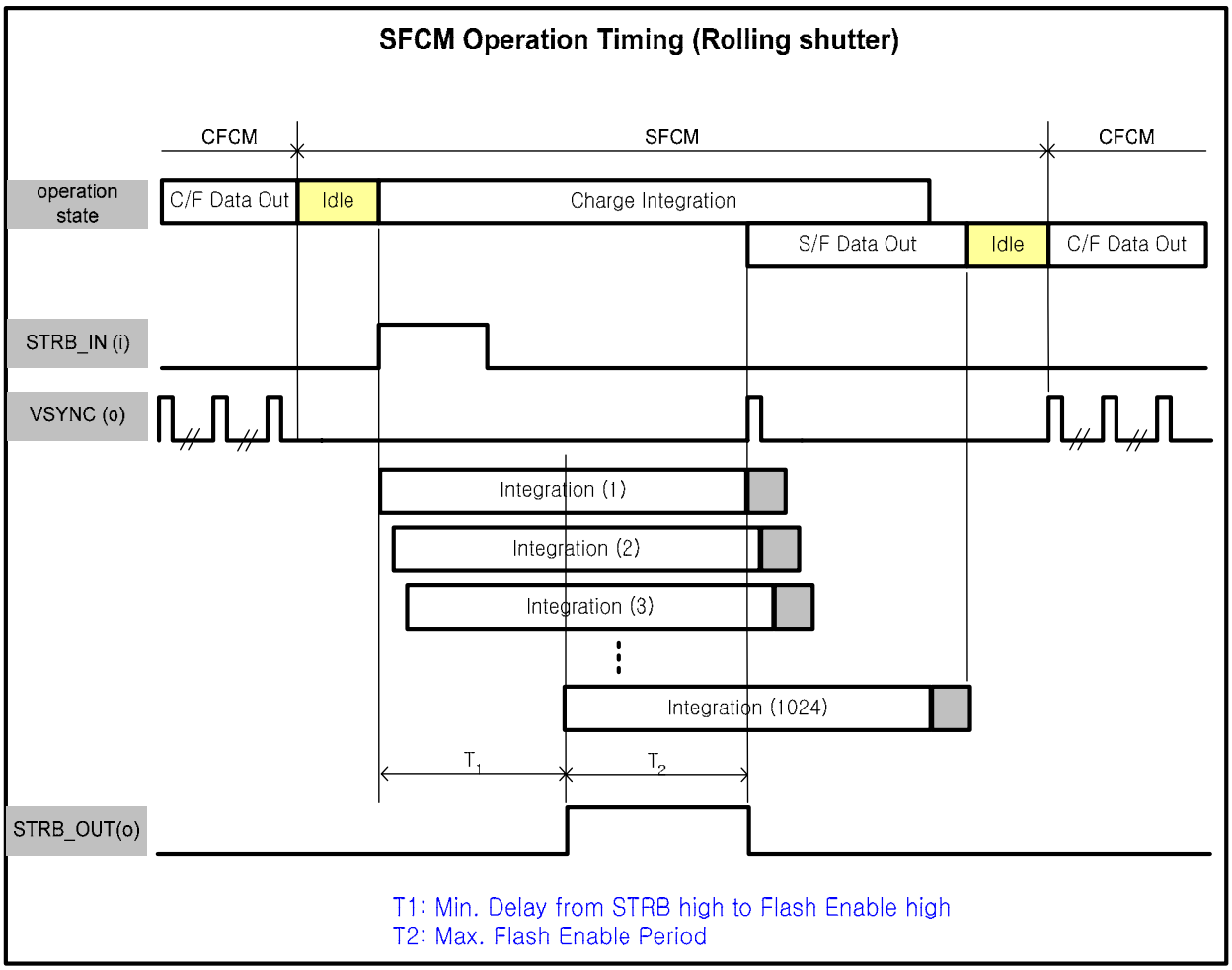


Figure 22: Rolling Shutter Operation (ERS/No Bulb, Timing)

2) ERS, SNAPSHOT (Bulb)

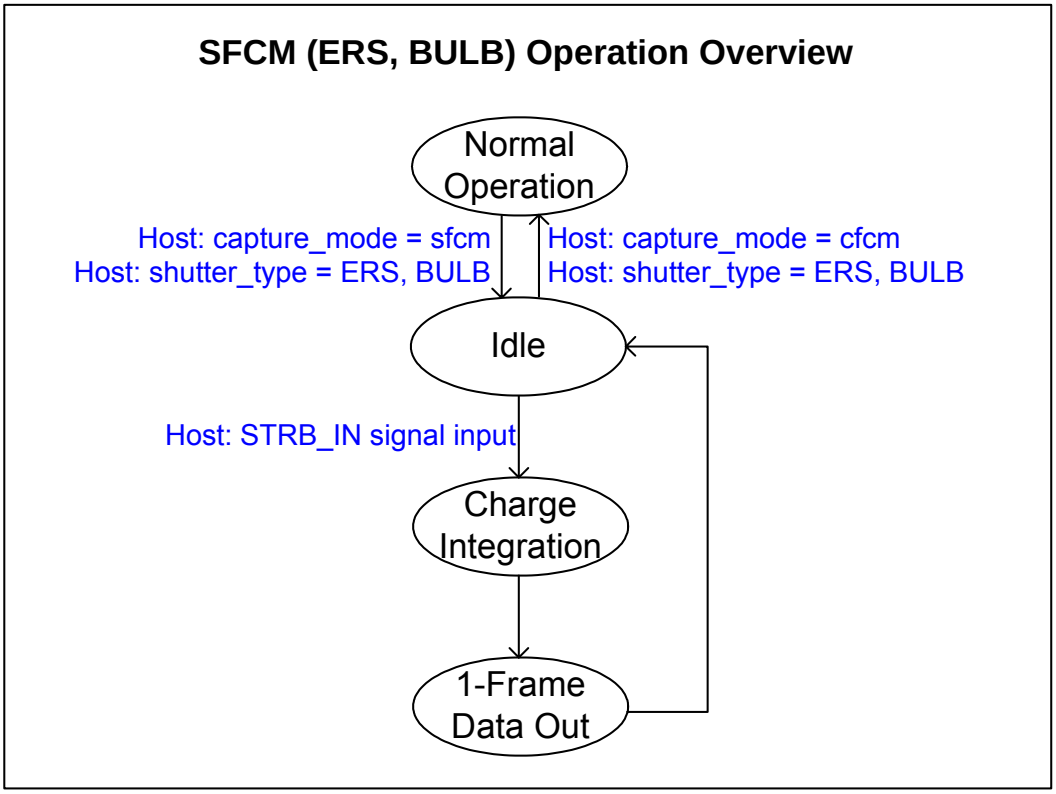


Figure 23: Rolling Shutter Operation (ERS Bulb, FSM)

1) Set shutter type to ERS, BULB mode (grr_mode=0, bulb_mode=1), at first.
2) SFCM is set by sf_mode (=1) register, wait for the releasing of STRB_IN signal.
3) STRB_IN signal is active (0 to 1), the integration is running during STRB_IN signal activation.
4) STRB_OUT signal (flash enable) is readout during T2 time(controlled by flash_width register), after T1.
5) The integration is finished, the each rows are readout at first line.
6) One frame data is all readout, after waiting, mode is changed by sf_mode register. (if sf_mode=0, CFCM)

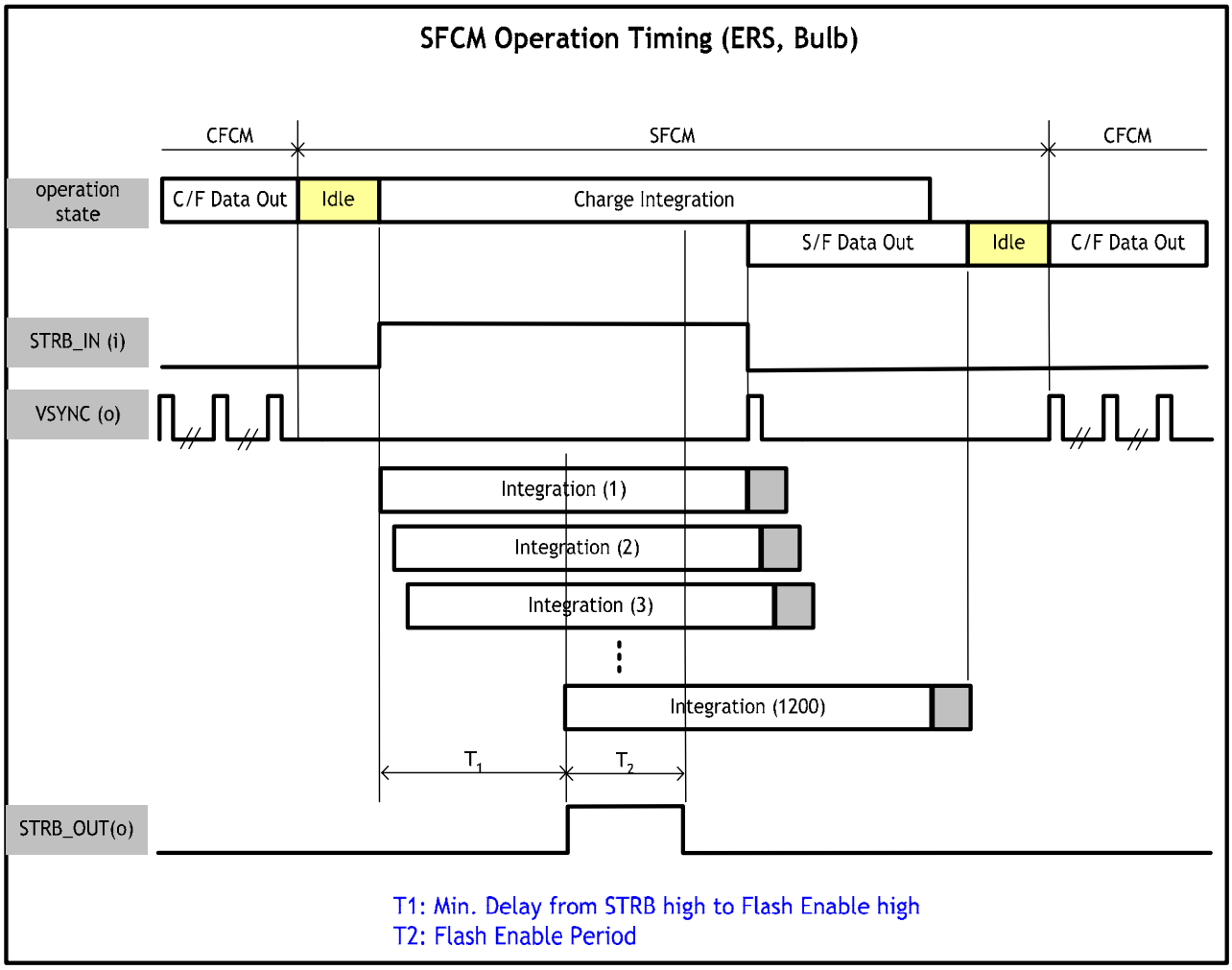


Figure 24: Rolling Shutter Operation (ERS Bulb, Timing)

MECAHNICAL SHUTTER

1) MS, SNAPSHOT (No Bulb)

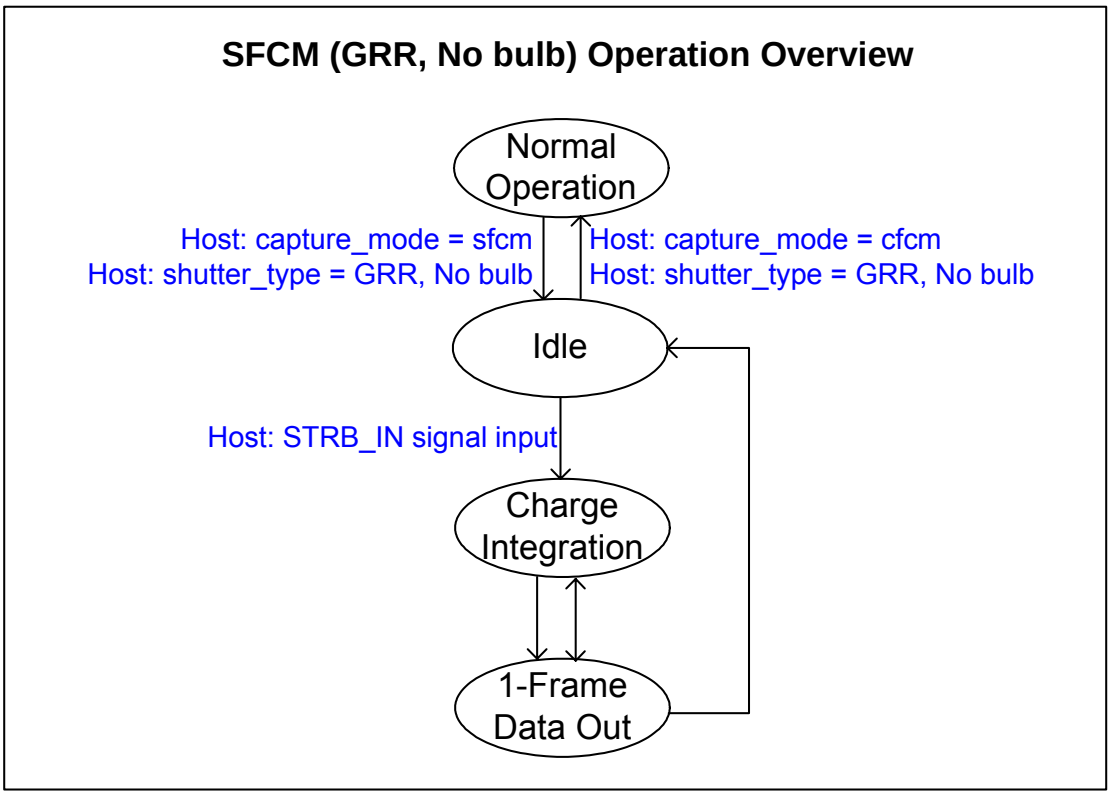


Figure 25: Mechanical Shutter Operation (GRS/No Bulb, FSM)

1) Set shutter type to ERS, no BULB mode (grr_mode=0, bulb_mode=1), at first.
2) SFCM is set by sf_mode (=1) register, wait for the releasing of STRB_IN signal.
3) STRB_IN signal is active (0 to 1), the integration is beginning during total integration time
4) STRB_OUT signal begins high level from the 3rd line after STRB_IN signal rising, until the integration is end.
5) The integration is finished, the each rows are readout at first line.
6) (If you want to readout multi frame) Repeat step 2 to step 4 during STRB_IN signal high.
7) One frame data is all readout, after waiting, mode is changed by sf_mode register. (if sf_mode=0, CFCM)

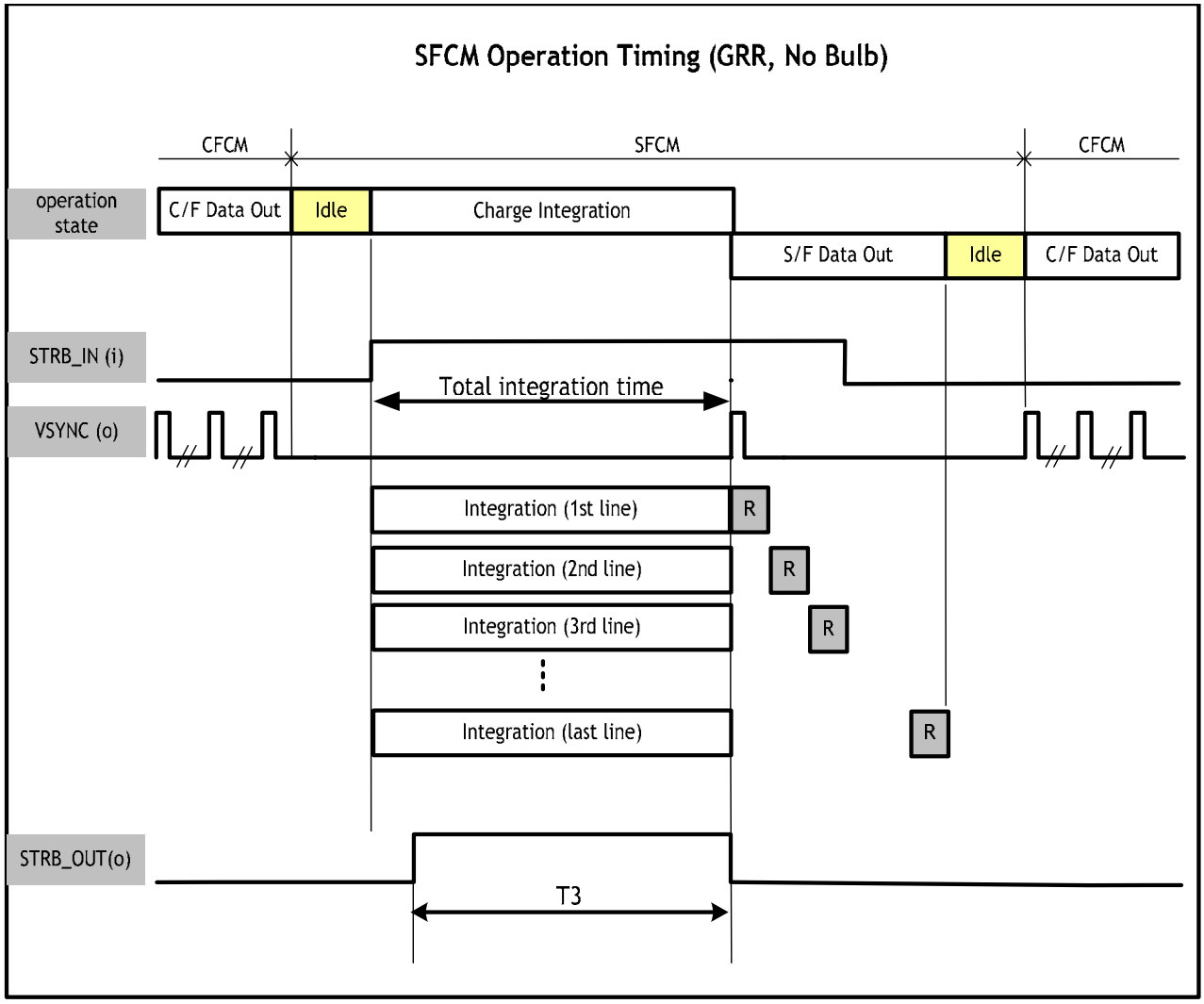


Figure 26: Mechanical Shutter Operation (GRS/No Bulb, Timing)

2) MS, SNAPSHOT (Bulb)

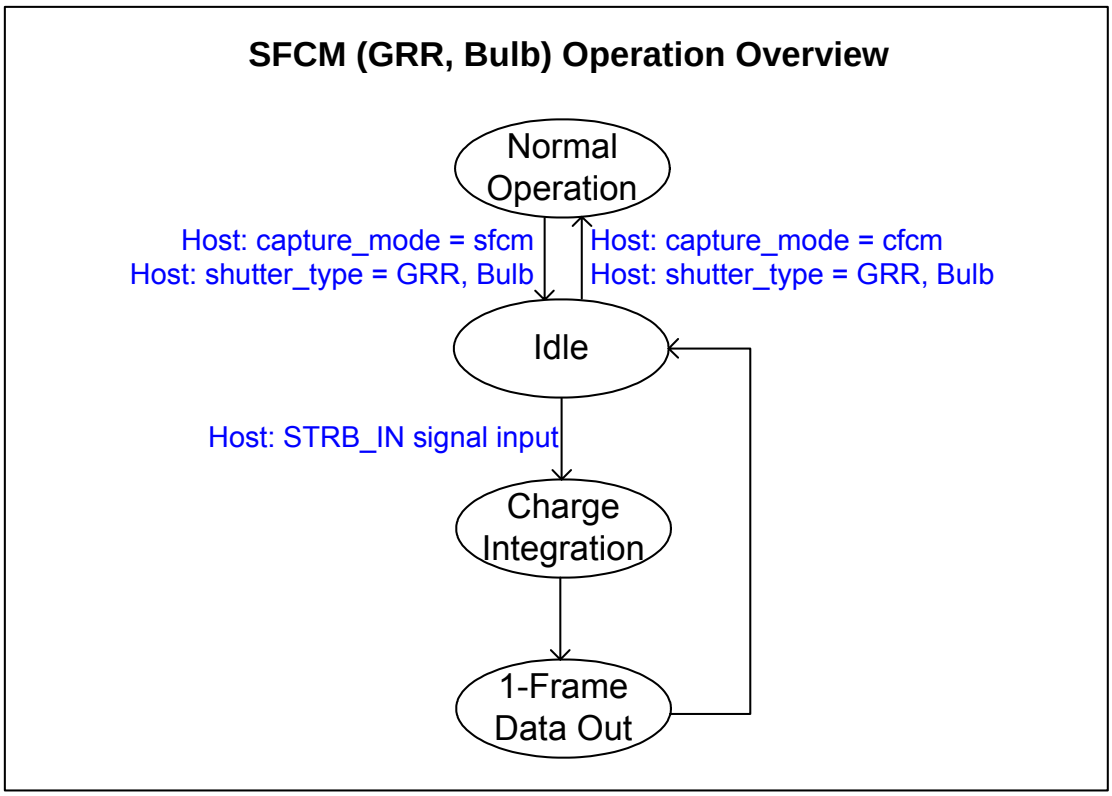


Figure 27: Mechanical Shutter Operation (GRS Bulb, FSM)

1) Set shutter type to mech_mode(=1'b1) , at first.
2) And then SFCM is set by sf_mode register, wait for the releasing of STRB_IN signal.
3) STRB_IN signal is release, the STRB_OUT signal that the width is controlled by flash_width register is output. If STRB_IN high period is shorter than flash width, the STRB_OUT signal is output by STRB_IN signal.
4) If the integration is finished, the each row is readout.
5) One frame data is all read out, mode is changed by sf_mode register. (if sf_mode=0, CFCM)

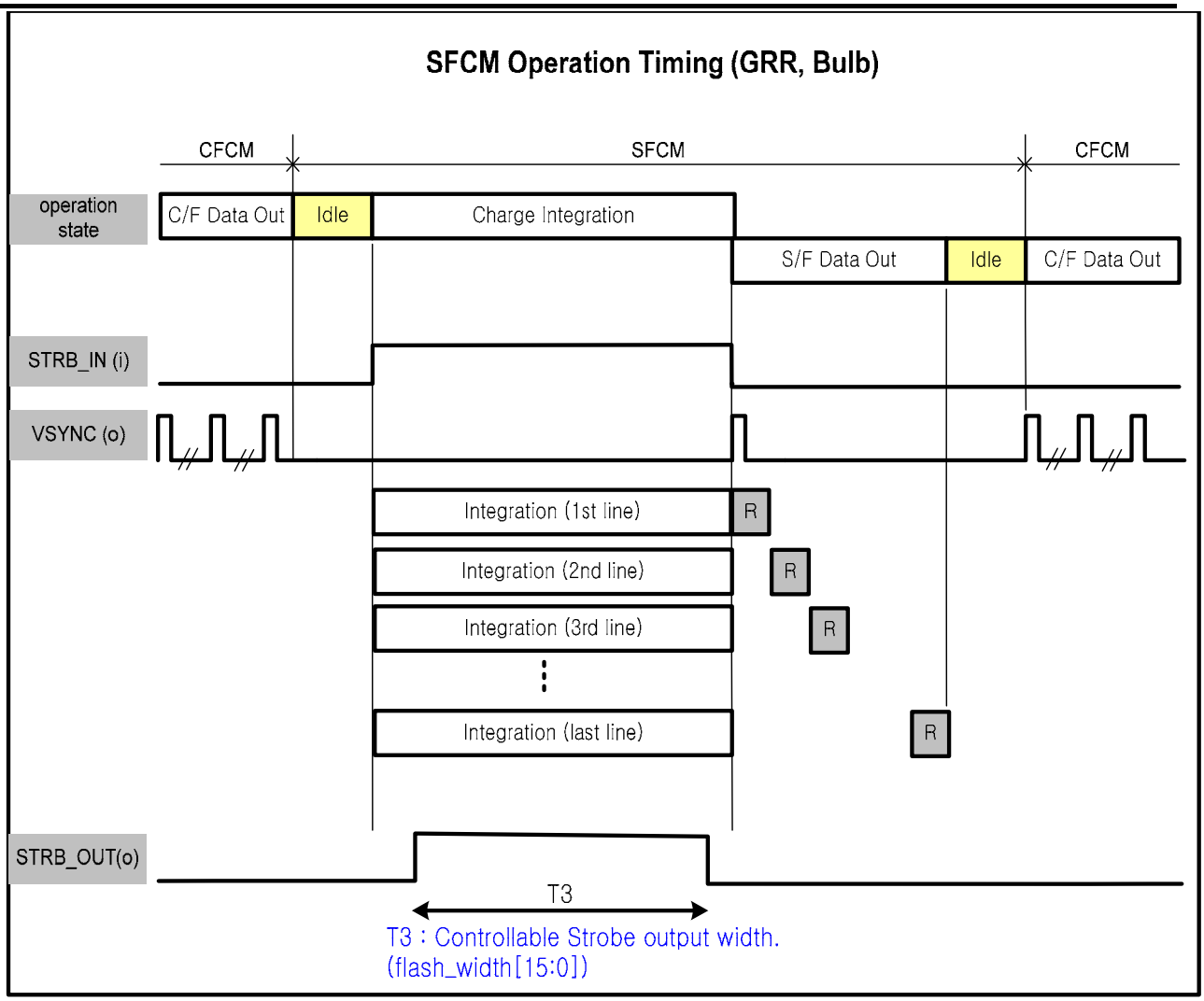


Figure 28: **Mechanical Shutter Operation (GRR/Bulb, Timing)**

3. Image Signal Processing

The S5K4BAFB is a high performance and low power UXGA CMOS image sensor embedded with an image signal processor (ISP). The ISP outputs 8-bit luminance and chrominance data from 10-bit sensor raw data input with maximum frame rate of 15 fps at UXGA resolution.

It performs sophisticated image processing functions including color correction, edge enhancement, auto defect correction, lens shading correction, gamma correction, auto exposure (AE) and auto white balance (AWB), auto flicker correction and image scaling. The AE and AWB functions are preformed by an embedded RISC processor. The host controller is able to access and control it through I^2C bus interface.

For auto exposure (AE) and auto white balance (AWB), Y/C data are integrated for pre-defined AE/AWB windows, and the data are read by the CPU in every frame. The CPU, 32-bit RISC core and peripherals, read data from optical detection block and calculates analog R/G/B gains and shutter values of sensor for the auto exposure. It also controls digital R/G/B gains and offsets, and hue for the auto white balance.

3-1. Gain & Offset Control

The offset and gain values of the raw Bayer image can be controlled for each Green (red), Green (blue), Red and Blue channel respectively.

3-2. Auto Exposure

The embedded AE control algorithm tracks the change of the luminance in the selected windows, and compares it to the AE target value. The image brightness is adjusted by controlling analog and digital gains and integration time of the image sensor. Hardwired Image Statistics Calculator block gathers statistical information for Auto Exposure control support. Sixty four flexible windows are available to support various exposure algorithm modes, which include Center Weighted, Center, and Bottom Weighted, Flat and full manual modes.

3-3. Auto White Balance

The embedded AWB algorithm tracks the white using AWB boundary on R-gain and B-gain plane according to the different color temperatures and then compensates the white balance with digital gains and offsets control. When a white object is illuminated with different color temperatures, its color appears reddish or bluish and so on. It is necessary to compensate the difference of color rendition caused by light source so that a white object appears as white under any light source. Hardwired Image Statistics Calculator block gathers statistical information for Auto White Balance support.
Normalized AWB is new AWB algorithm. The Color space is very important to AWB. Each color space has its own property. For example, well-known CIE USC(Uniform Chromaticity Scale) space is more uniform and more linear than the other CIE color space. In our AWB method 2, we use normalized r/b space. Normalized r/b means that red or blue color is divided by total sum of color component red, green and blue. Normalized r/b space is expected that it has linearity for color intensity and robustness for variation of color characteristics of sensors.
Originally, the algorithm of AWB method 2 requires thousands of samples. It is not feasible requirement for small camera module. So, we have reduced number of samples to only 64 patches. And we added hard-wired pixel filter to prohibit loss of performance.
H/w pixel filter remove all pixel in the outside of gray region which is controllable by I2C register setting. In addition it calculate sum of R/G/B and numbers of pixel in the inside of gray region. Sum of R/G/B and numbers of pixel is separated into 2 classes, one is from high illuminant environment and the other is from low illuminant environment. Only one is used at each time.

3-4. Color Interpolation

Each color Bayer pixel from the image sensor is converted into an R/G/B pixel and the missing color information of a Bayer pixel can be derived from average value of adjacent pixels. The interpolation involves a trade-off between image noise and resolution in general.

3-5. Gamma Correction
Gamma correction operates on the R, G, B component respectively to improve non-linear relation between the video signal and the display device output.

3-6. Color Correction
A 3x3 color correction matrix is used to improve color representation. It is achieved by reducing color crosstalk on spectral characteristics of the image sensor through a linear transformation.

3-7. Auto Defect Correction
Auto Bad Pixel Replacement detects and replaces isolated bad pixels on the raw image data based on their neighbor pattern and average. Probability of detection and false detection of bad pixel is controllable via a threshold level. To reduce artifacts of replacement, it uses gradient information of neighborhood.

3-8. Lens Shading Correction
Due to the lens characteristic, the light intensity injected to an image sensor tends to decrease near an image edge. The lens shading artifacts will be differently affected by each color component therefore it is necessary to be individually calibrated for each of the RGB channels to keep the color and luminance balance across the frame. However the S/N at the image edge will be lower than the S/N at the center area. Radial shading profile is fitted to 4^{th} order polynomial separately for each RGB channels. Correction of corners vignetted more than 70% to the center value is possible.

3-9. Auto Flicker Correction
Flicker may be occurred when the sensor integration time is not an integer multiple of the period of light intensity like the environment under a 50Hz or 60Hz fluorescent lamp. The flicker is detected using a dedicated algorithm and can be corrected by adjusting the integration time to some limited values. Under strong periodic light intensity, the short integration time may be required and if the value is smaller than 1/100 (or 1/120) second, the flicker band noise can be seen.

3-10. Image Scaling
The image from the sensor can be scaled down in the format of SXGA, VGA, QVGA, QQVGA, CIF, and QCIF in a smooth manner. In this case the frame rate is not changed. In order to increase the frame rate, a sub-sampled scaling is supported.

3-11. Noise Reduction
Noise reducer can effectively eliminate patterned noise caused by cross-talk between color components and sensor random noise. The amount of noise and gradient information in the image are measured for choosing best smoothing parameters.

3-12. Special Effects

The special effects create a Sepia (warm tone), Aqua (cool tone), and Negative effect on Image. The user can get more special effect tone by controlling the Cr/Cb register (<1.06h>, <1.07h>) value. A choice of Cr/Cb value allows the user to be a little more creative on images.

3-13. Output Formatting

The ISP outputs 8-bit processed video data or sensor raw data with related vertical/horizontal sync and pixel clock signals in the form of a standard ITU-R.656/601 and RGB data.

3-14. Edge Enhancement
To improve edge information, 2D edge improvement processing is supported. The level of enhancement is programmable.

3-15. Color Space Converter
Fully programmable 3X3 Matrix for Color space conversion from RGB to YUV is supported.

3-16. Hue & Saturation Controller
Hue and Saturation are independently controllable.

3-17. I^2C Bus Interface
The I^2C contains a serial two-wire half duplex interface that features bi-directional operation, master or slave mode. The general SDA and SCL are the bi-directional data and clock pins, respectively. These pins are open-drain type ports and will require a pull-up resistor to VDD. The I^2C bus interface is composed of following parts. START signal, 7-bit slave device address (if IIC_ID is Low 0101101b, if IIC_ID is high 0101001b) transmission followed by a read/write bit, an acknowledgement signal from the slave, 8-bit data transfer followed by an acknowledgement signal and STOP signal. The SDA bus line may only be changed while SCL is low. The data on the SDA bus line is valid on the high-to-low transition of SCL.

.

AUTO FOCUS

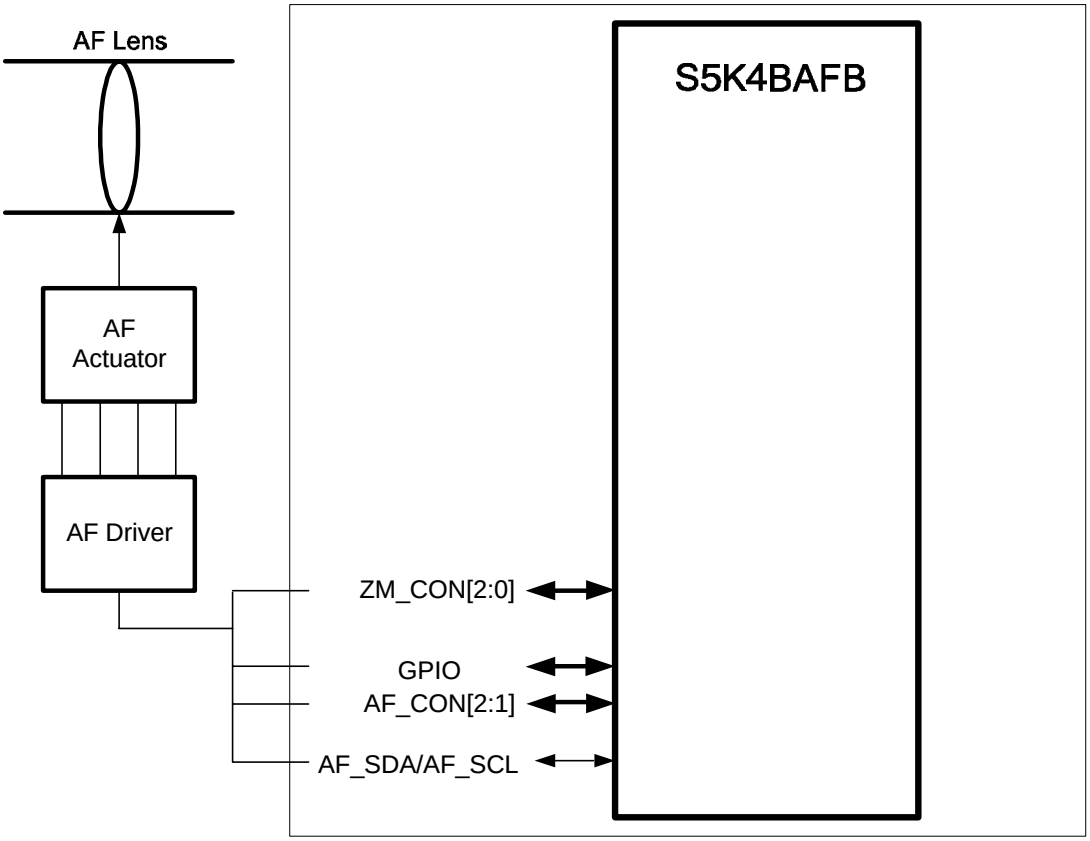


Figure 29: AF Interface

[NOTE]

(1) Auto Focusing controlled by embedded firmware
(2) IIC bus interface for driver control
(3) 5-ch PWM outputs for driver control
(4) 1-lens position sensor inputs
(5) We support optional ROM code. It depends on the AF method you want. So, if the method you want is different from the one we support, ROM code must be revised.

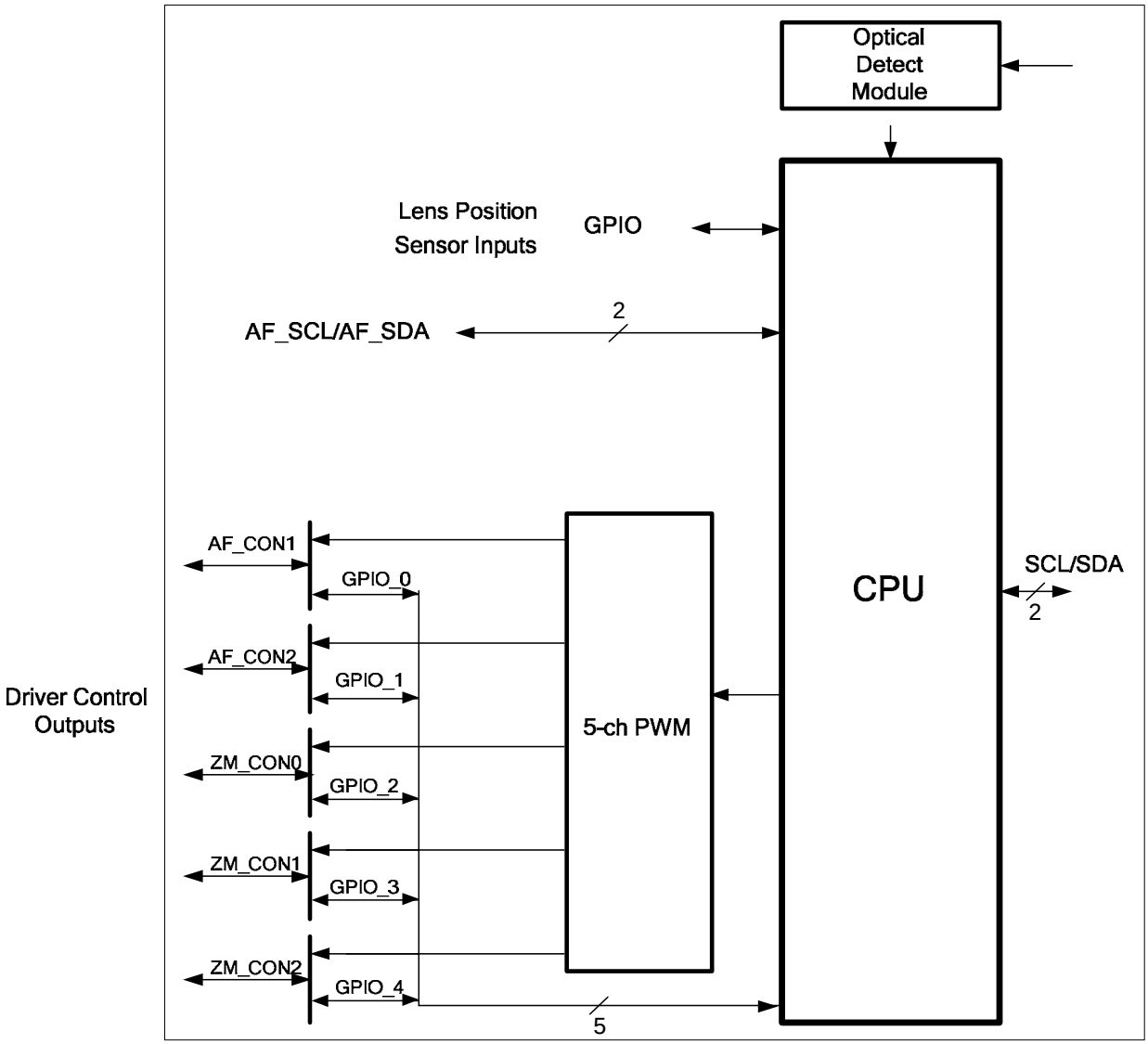


Figure 30: Functional Block Diagram For AF

[NOTE]

1) The S/W can access 4-registers, two (AF1_SUM_W1, AF2_SUM_W1) for results of two digital band-pass filters of window-1, and the other two (AF1_SUM_W2 and AF2_SUM_W2) for those of window-2 at anytime in every frame period. (The window-1 and the window-2 locations are independent)
2) 5-ch PWM output is used for zoom driving or auto focus control.
3) Also 6-ch output can be used with GPIO.

PWM TIMER

The S5K4BAFB has six 16-bit timers. Each timer has its own 16-bit down-counter which is driven by the timer clock. The down-counter is initially loaded from the Timer Count Buffer register (TCNTBn(<12.0Ch>, <12.0Dh>, <12.18h>, <12.19h>, <12.24h>, <12.25h>, <12.30h>, <12.31h>, <12.3Ch>, <12.3Dh>, <12.48h>, <12.49h>)). When the down-counter reaches zero, the timer interrupt request is generated to inform the CPU that the timer operation is completed. When the timer down-counter reaches zero, the value of corresponding TCNTBn can be automatically reloaded into the down-counter to start the next cycle. However, if the timer stops, for example, by clearing the timer enable bit of TCONn(<12.08h>, <12.09h>, <12.0Ah>, <12.0Bh>) during the timer running mode, the value of TCNTBn will not be reloaded into the counter.

The Pulse Width Modulation function (PWM) uses the value of the TCMPBn(<12.10h>, <12.11h>, <12.1Ch>, <12.1Dh>, <12.28h>, <12.29h>, <12.34h>, <12.35h>, <12.40h>, <12.41h>, <12.4Ch>, <12.4Dh>) register. The timer control logic changes the output level when the down-counter value matches the value of the compare register in the timer control logic. Therefore, the compare register determines the turn-on time (or turn-off time) of a PWM output.

The TCNTBn and TCMPBn registers are double buffered to allow the timer parameters to be updated in the middle of a cycle. The new values will not take effect until the current timer cycle completes.

A simple example of a PWM cycle is shown in the figure below.

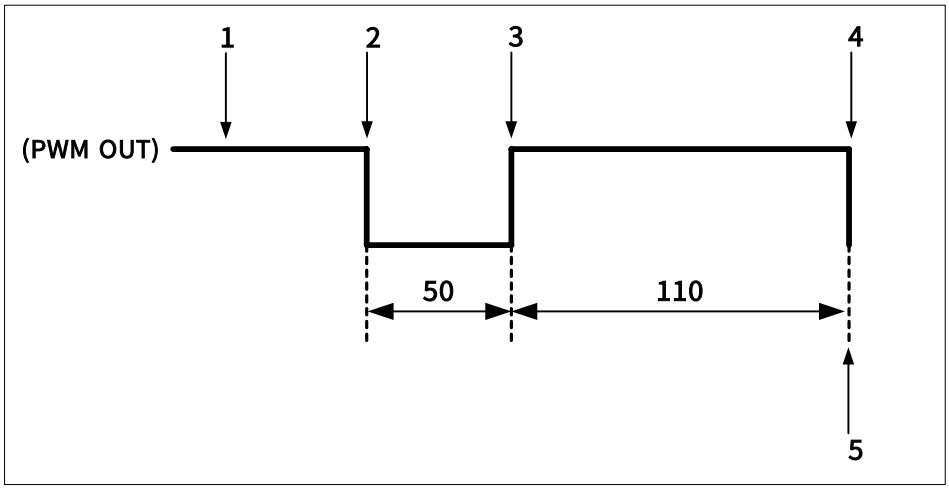


Figure 31: A simple example of a PWM cycle

Initialize the TCNTBn with 160(50+110) and the TCMPBn with 110.
Start timer by setting the start bit and manual update bit off. The TCNTBn value of 160 is loaded into the down-counter, the output is driven low.
When down-counter counts down to the value in the TCMPBn register(110), the output is changed from low to high.
When the down-counter reaches 0, the interrupt request is generated if the interrupt is enabled.
At the same time the down-counter is automatically reloaded with TCNTBn, which restarts the cycle.

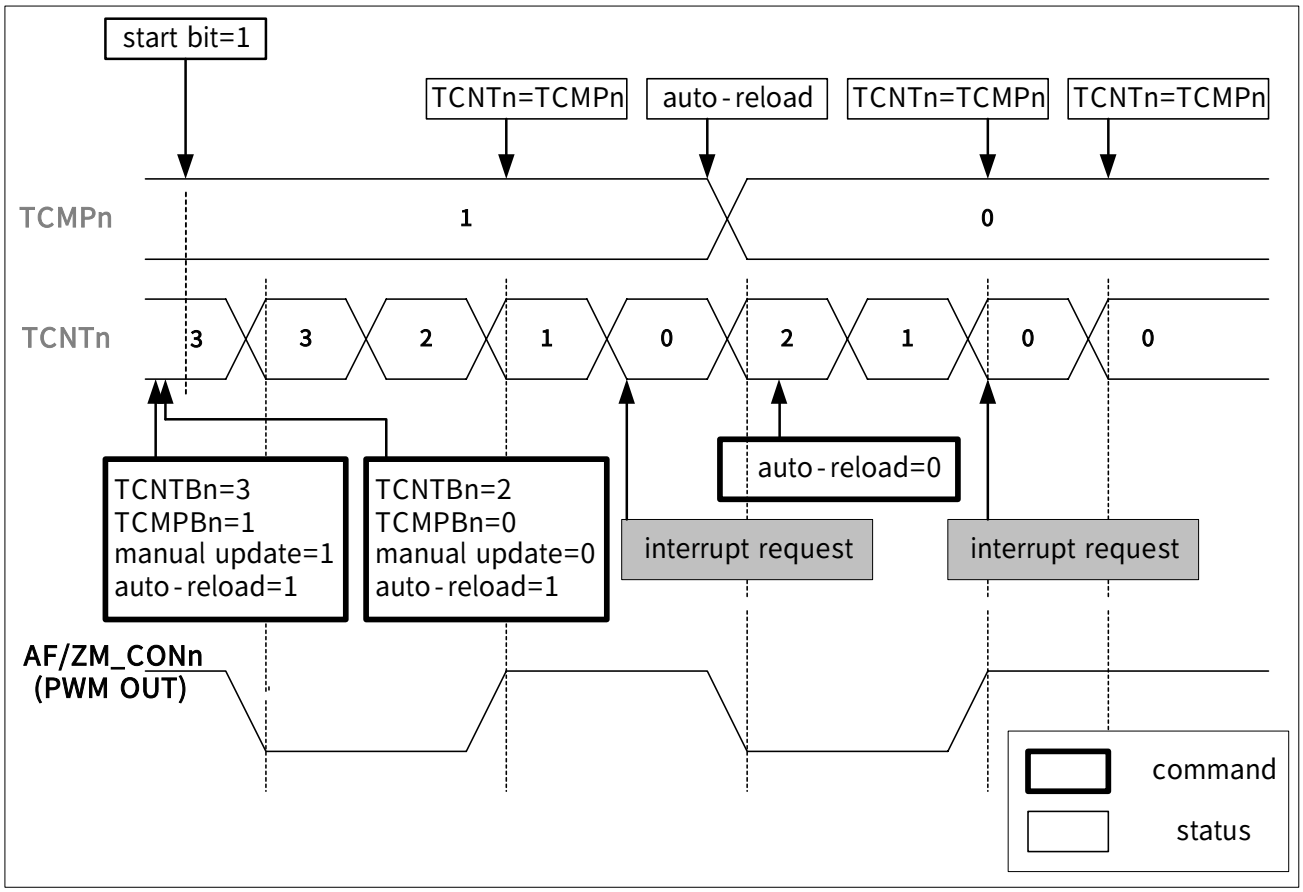


Figure 32: Basic PWM Timer Operation

[NOTE]

1) A Timer has TCNTBn, TCNTn, TCMPBn and TCMPn. TCNTBn and TCMPBn are loaded into TCNTn and TCMPn when the timer reaches 0. When TCNTn reaches 0, the interrupt request will occur if the interrupt is enabled.
2) TCNTn and TCMPn are the names of the internal registers.
   The TCNTn register can be read from the TCNTOn register.

[NOTE]

Initialize the PWM Timer (setting manual update and inverter)

Because an auto-reload operation of the pwm timer occurs when the down counter reaches to 0, a starting value of the TCNTn has to be defined by the user at first. In this case, the starting value has to be loaded by the manual update bit. The sequence to start a pwm timer is as follows;

1) Write the initial value into TCNTBn and TCMPBn.
2) Set the manual update bit of the corresponding timer and recommend to set the inverter on/off bit whether using inverter function or not.
3) Set the start bit of the corresponding timer to work the pwm function and clear only manual update bit.

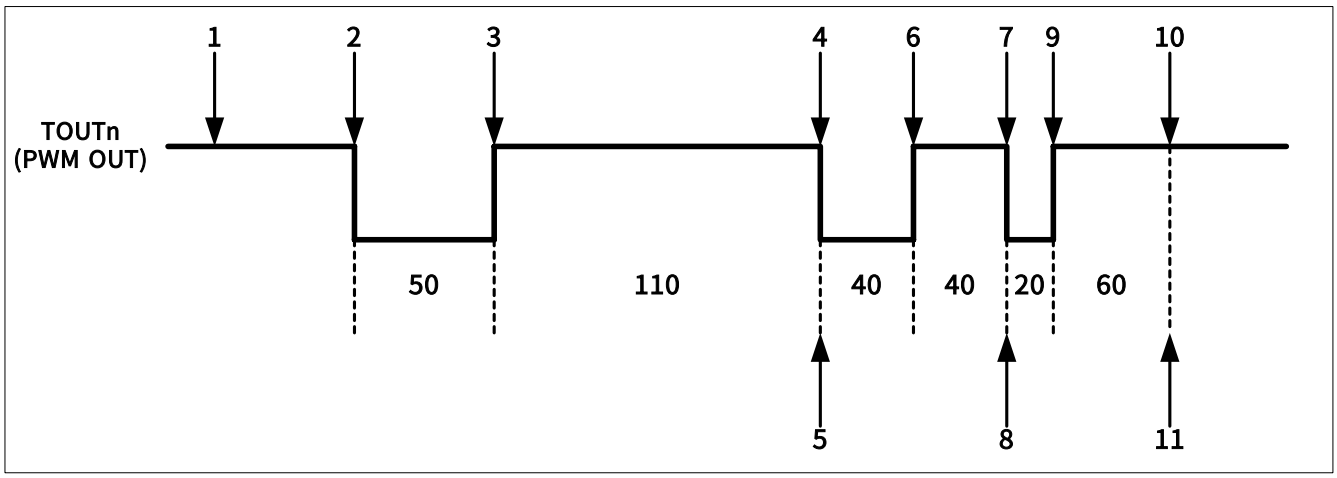


Figure 33: Example of a timer operation

1) Enable the auto-reload feature. Set the TCNTBn as 160(50+110) and the TCMPBn as 110. Set the manual update bit and inverter bit(on/off). The manual update bit makes the TCNTn, TCMPn set to the value of TCNTBn, TCMPBn. And then, set TCNTBn, TCMPBn as 80(40+40), 40 to determine the next reload value.
2) Start Timer by setting the start bit and manual update bit off.
3) When TCNTn has the same value with TCMPn, the logic level of TOUTn is changed from low to high
4) When TCNTn reaches to 0, TCNTn is reloaded automatically with TCNTBn. At the same time, the interrupt request is generated.
5) In the ISR(Interrupt Service Routine), the TNCTBn and TCMPBn is set as 80(20+60) and 60, which is used for next duration.
6) When TCNTn has the same value with TCMPn, the logic level of TOUTn is changed from low to high.
7) When TCNTn reached to 0, TCNTn is reloaded automatically with TCNTBn. At the same time, the interrupt request is generated.
8) In the ISR(Interrupt Service Routine), auto-reload and interrupt request are disabled to stop the timer.
9) When TCNTn has the same value with TCMPn, the logic level of TOUTn is changed from low to high.
10) Even when TCNTn reaches to 0, TCNTn is not any more reloaded and the timer is stopped because auto-reloaded is disabled.
11) No interrupt request is generated.

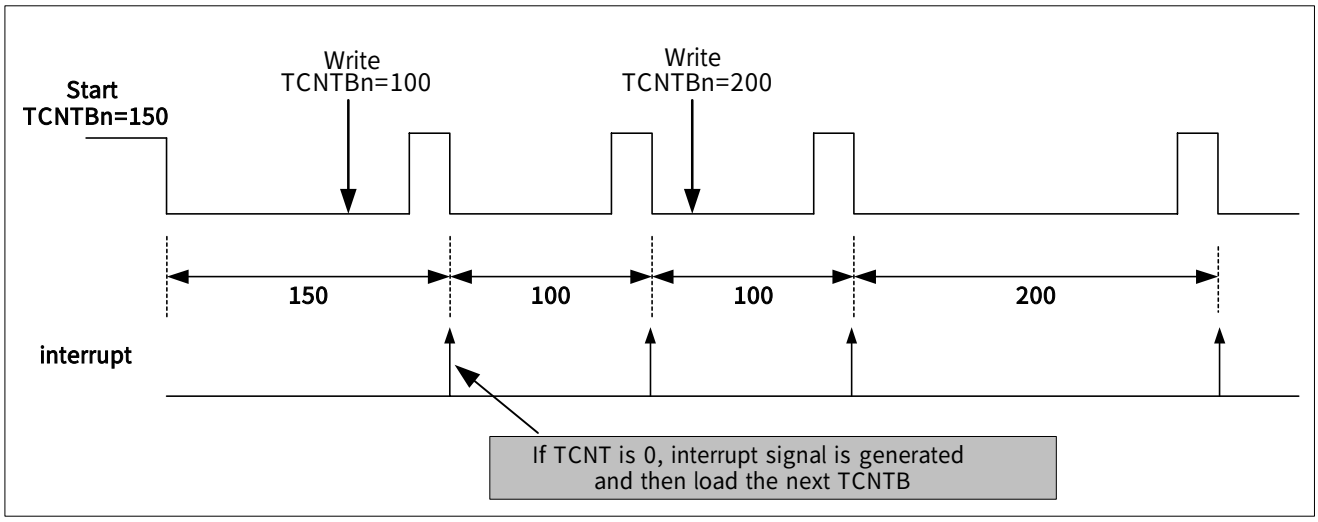


Figure 34: Example of double buffering feature (Fixed TCMPBn)

[NOTE]

1) The PWM Timer have a double buffering feature, which can change the reload value for the next timer operation without stopping the current timer operation. So, although the new timer value is set, a current timer operation is completed successfully.
2) The timer value can be written into TCNTBn (Timer Count Buffer register) and the current counter value of the timer can be read from TCNTOn (Timer Count Observation register). If TCNTBn is read, the read value is not the current state of the counter but the reload value for the next timer duration.
3) The auto-reload is the operation, which copies the TCNTBn into TCNTn when TCNTn reaches 0. The value, written into TCNTBn, is loaded to TCNTn only when the TCNTn reaches to 0 and auto-reload is enabled. If the TCNTn is 0 and the auto-reload bit is 0, the TCNTn does not operate any further.

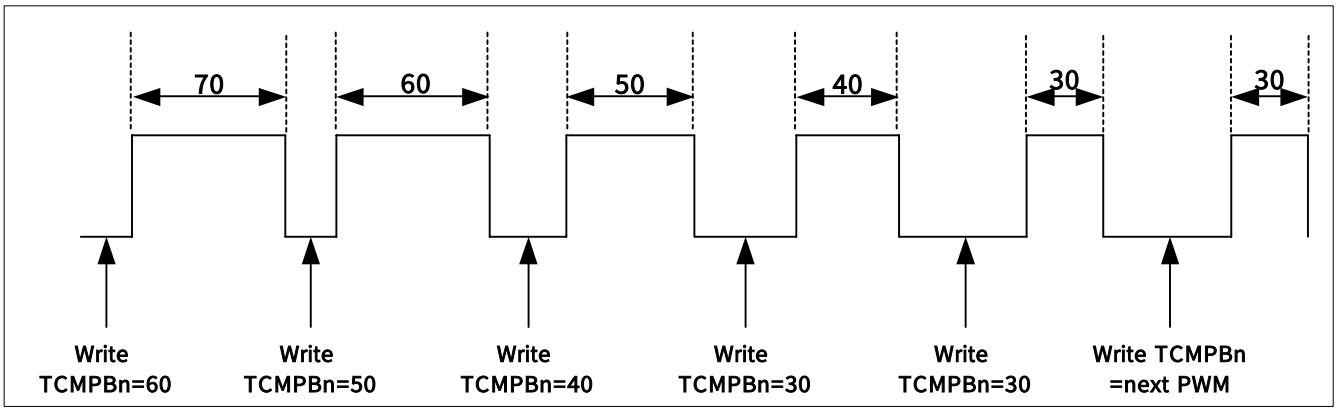


Figure 35: Example of double buffering feature (Fixed TCNTBn)

[NOTE]

1) PWM feature can implement by using the TCMPBn. PWM frequency is determined by TCNTBn. A PWM value is determined by TCMPBn in the Figure 28.
2) For higher PWM value, decrease TCMPBn value, For lower PWM value, increase TCMPBn value. If output inverter is enabled, the increment/decrement may be opposite.
3) Because of double buffering feature, TCMPBn, for a next PWM cycle, can be written in any point of current PWM cycle by ISR or something else.

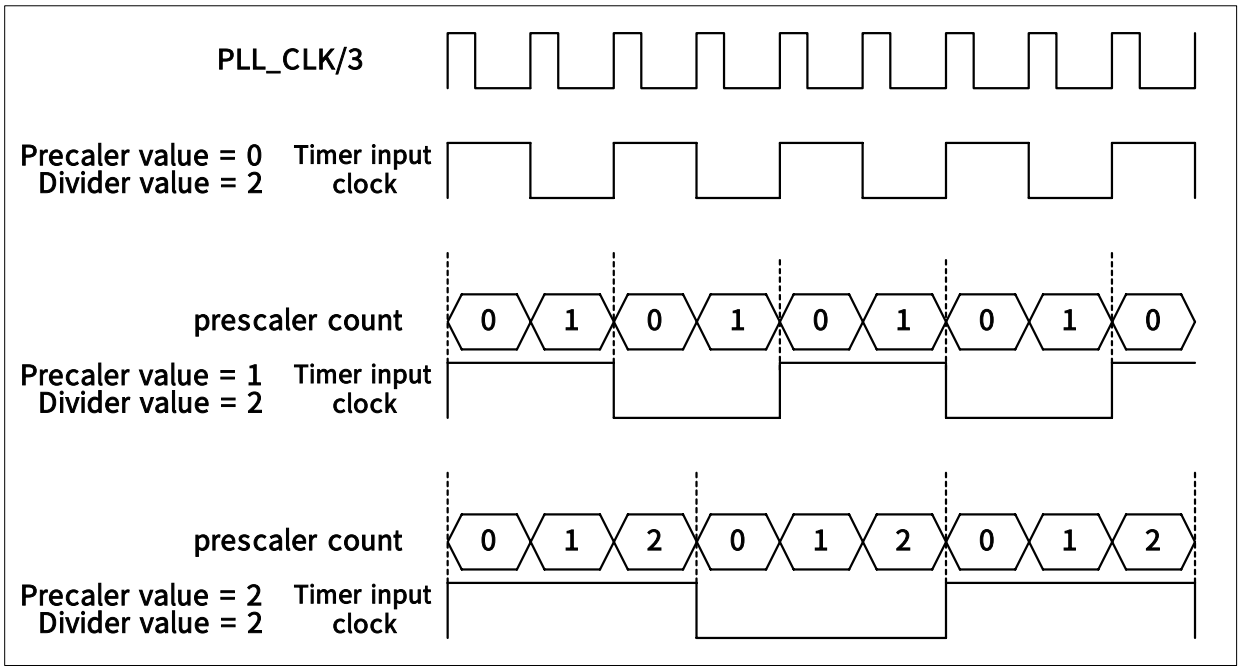


Figure 36: Prescaler & Divider

[NOTE]

1) Timer 0 and 1 share a programmable 8-bit pre-scaler that provides the first level of division for the PCLK. Timer 2, 3, and 4, 5 share a different 8-bit pre-scaler.
2) Each timer has its own, private clock-divider that provides a second level of clock division(pre-scaler divided by 2,4,8,16, or 32)
3) $F_{pwm\ timer}$ *(PWM timer input clock Frequency) = (PLL_CLK/3) / {(pre-scaler value + 1) * (divider value)}*
   pre-scaler value : 0 ~ 255
   divider value : 2, 4, 8, 16, 32
4) An 8-bit pre-scaler and 4-bit divider make the following output frequencies

4-bit divider settings	minimum resolution (prescaler=0)	maximum resolution (prescaler = 255)	maximum interval (TCNTBn = 65535)
2	0.0476us (21Mhz)	12.190us (82.03Khz)	0.7989s
4	0.0952us (10.5Mhz)	24.380us (41.01Khz)	1.597s
8	0.1904us (5.25Mhz)	48.761us (20.50Khz)	3.195s
16	0.3809us (2.625Mhz)	97.523us (10.25Khz)	6.391s
32	0.7619us (1.3125Mhz)	195.047us (5.12Khz)	12.7s

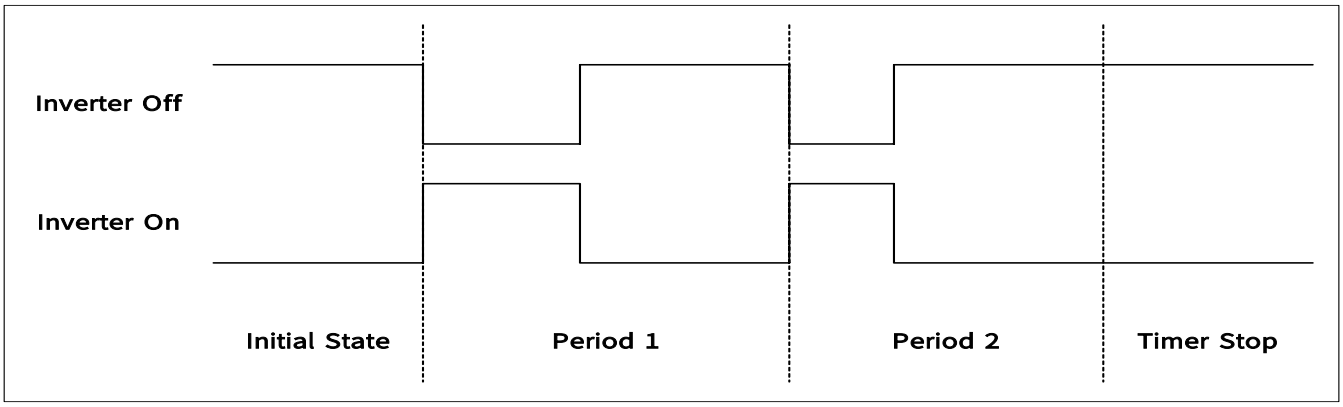


Figure 37: Inverter on/off

[NOTE]

1) Turn off the auto-reload bit. And then, in the inverter off mode, PWM OUT goes to high level and the timer is stopped after TCNTn reaches to 0. In this mode, when TCNTn > TCMPn, the output level is low and when TCNTn <= TCMPn, the output level is high.
2) Stop the timer by clearing the timer start/stop bit to 0.
3) PWM OUT can be inverted by the inverter on/off bit in TCON. The inverter removes the additional circuit to adjust the output level.

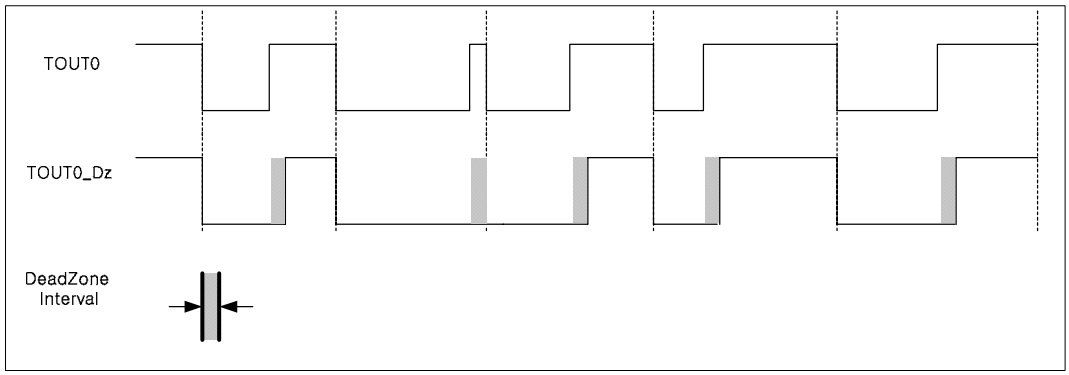


Figure 38: The Waveform when a deadzone feature is enabled

The deadzone is for the PWM control of power devices. This feature is used to insert the time gap between a turn-off of a switching device and a turn on of the other switching device. This time gap prohibit the two switching device turning on simultaneously even for a very short time.

[NOTE]

1) TOUT0 is the PWM output. If the dead-zone is enabled, the output wave-form of TOUT0 will be TOUT0_Dz.

PWM OVERVIEW

1) Five period parameters and counter setting.(PWMPERIOD, PWMT1, PWMT2, PWMT3, PWMT4)
2) 32MHz, 31.2ns accuracy 16bit data.
3) Enable control.
4) Support two trigger mode : Free trigger mode / Vsync mode
5) Number of PWM pulse can be set(PWM period x N)
6) Initial output level can be specified(H or L)
7) Output level is reversed at every PWMT*

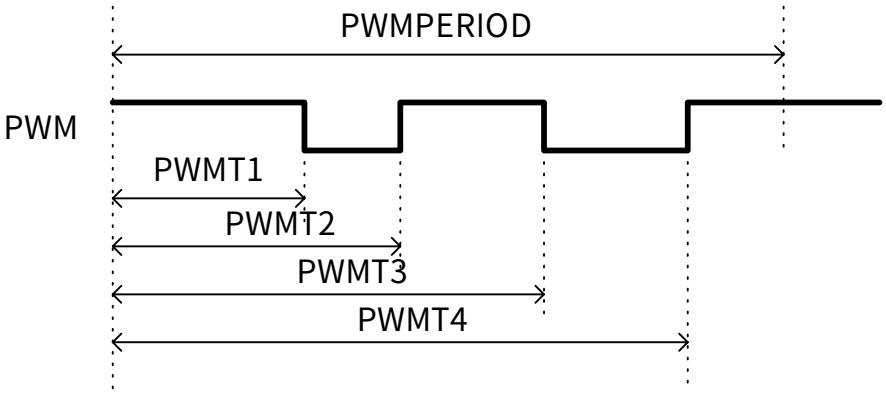
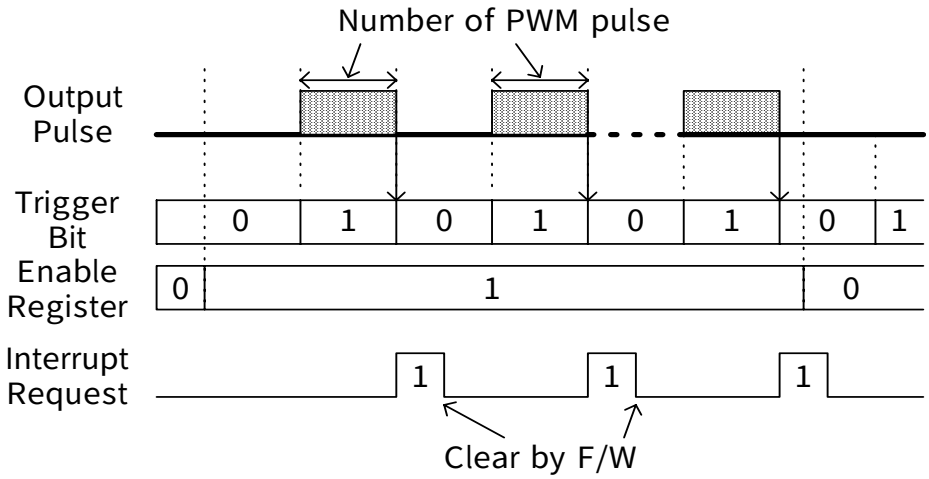


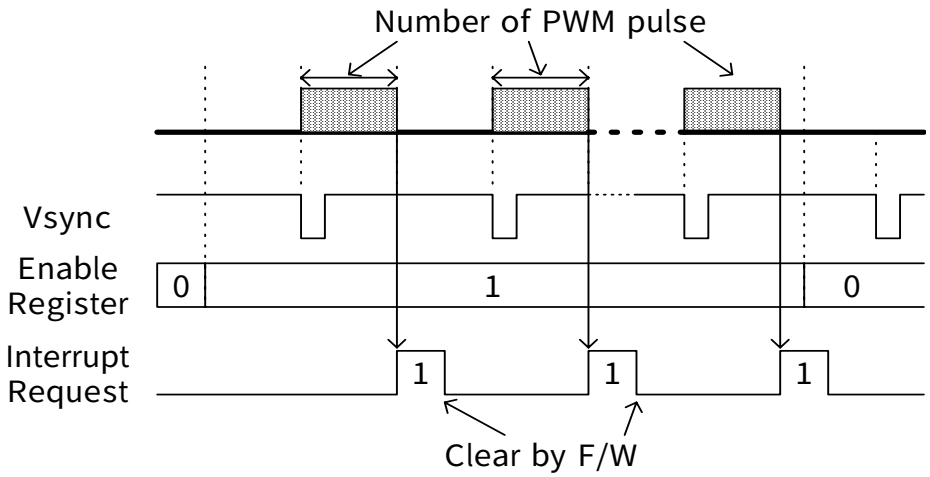
Figure 39: PWM 1 CYCLE TIMING

☞ **Free Trigger Mode**



1) PWM pulse output will start when trigger bit is set.
2) Generate interrupt request at the end of PWM output.
3) Trigger bit will be cleared at the end of PWM output.
4) Trigger bit is valid while enable register is set as “1”.

☞ **Vsync Mode**



1) PWM pulse will be outputted for every Vsync.
2) Generate interrupt request at the end of PWM output.
3) Vsync is effective while enable register is set as “1”.
4) Every PWM port that is set as this mode will start output simultaneously.

E-FUSE CELL ARRARY STRUCTURE

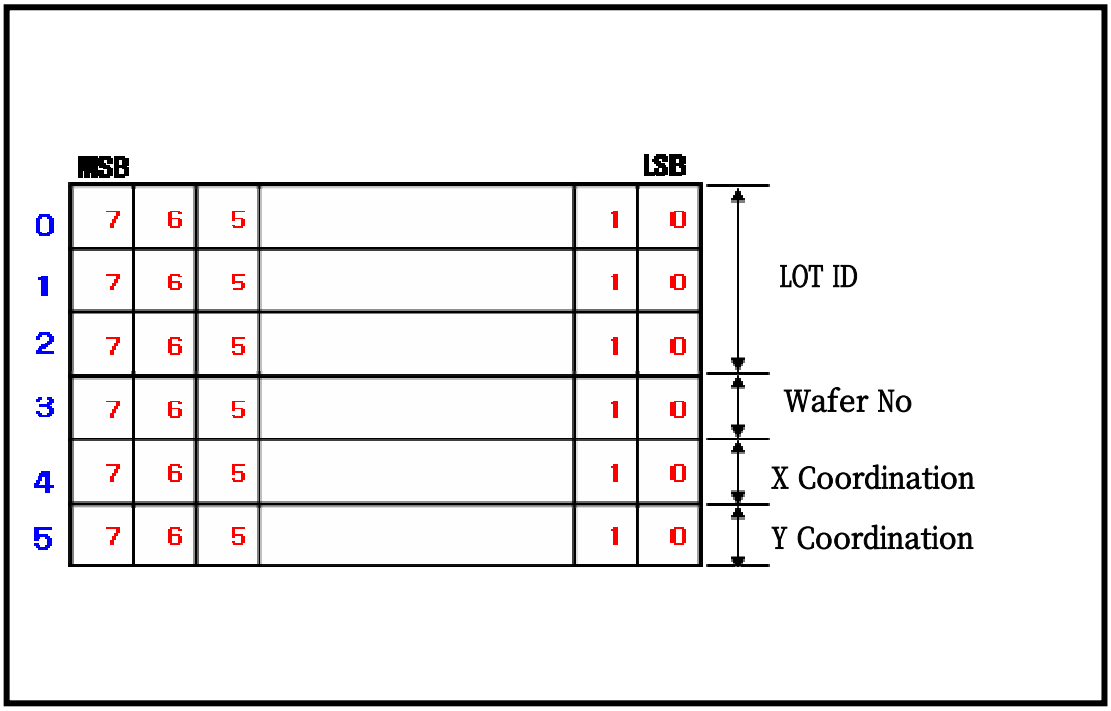


Figure 40: E-Fuse Array

E-FUSE WRITE TIMING

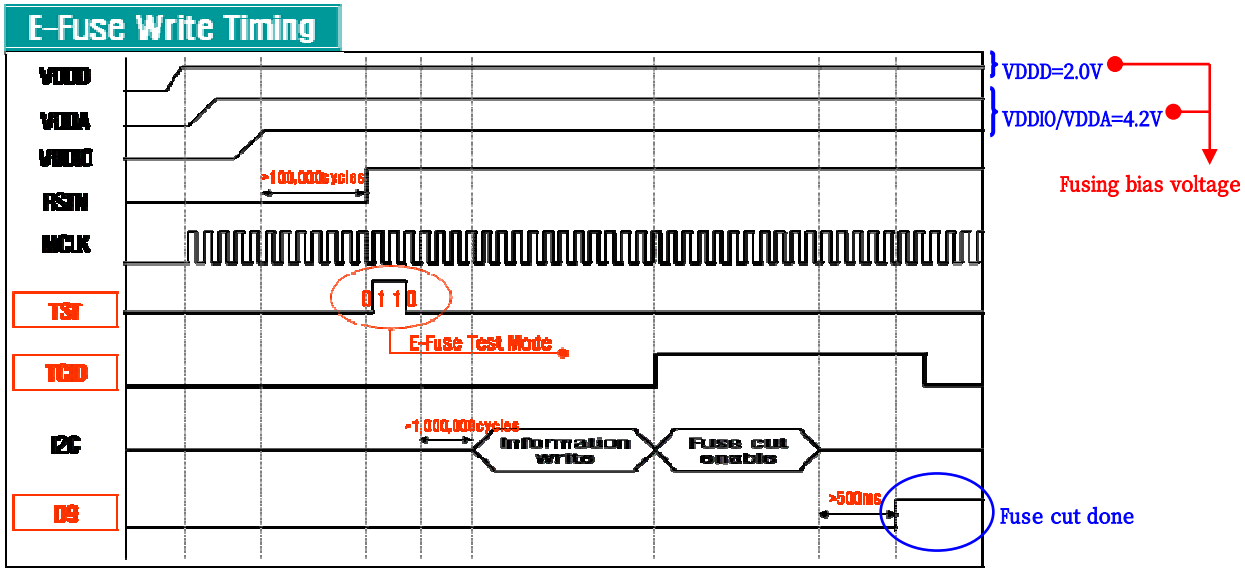


Figure 41: E-Fuse Program Mode

read reset time & fuse cut on time setting → <2.6Ah>=36h
module information assign register → <2.6Ch> ~ <2.71h> total 48bit is usable
fuse cut enable register → <2.6Ah> [7] = 1'b
→ if D9 pin state is high, fuse cut register must be disabled. <2.6Ah> [7] = 0'b

E-FUSE READ TIMING

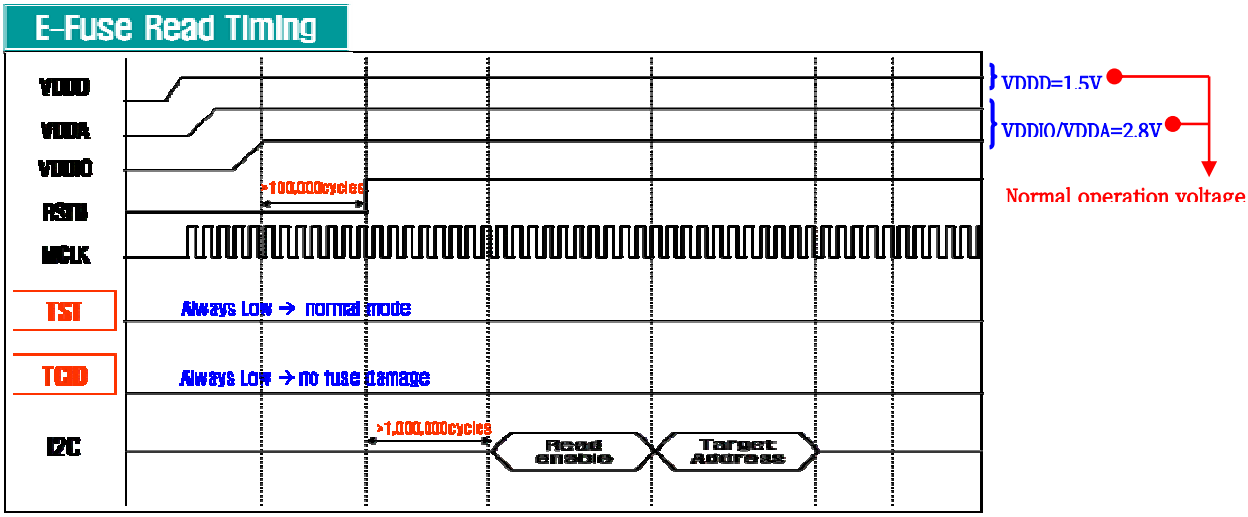
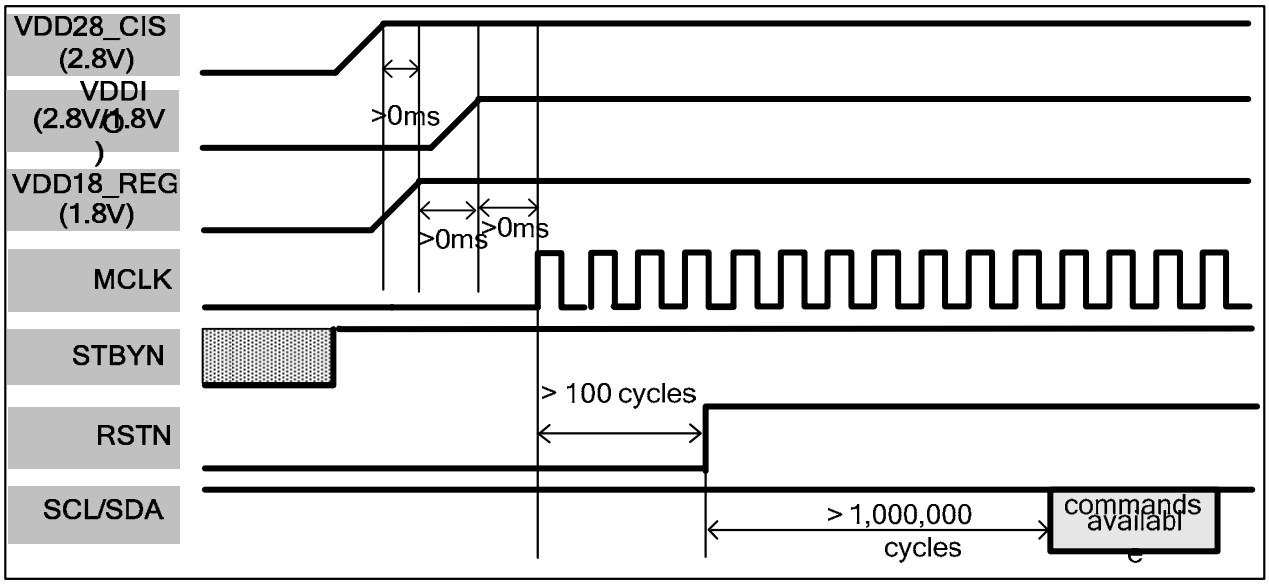


Figure 42: E-Fuse Read Mode

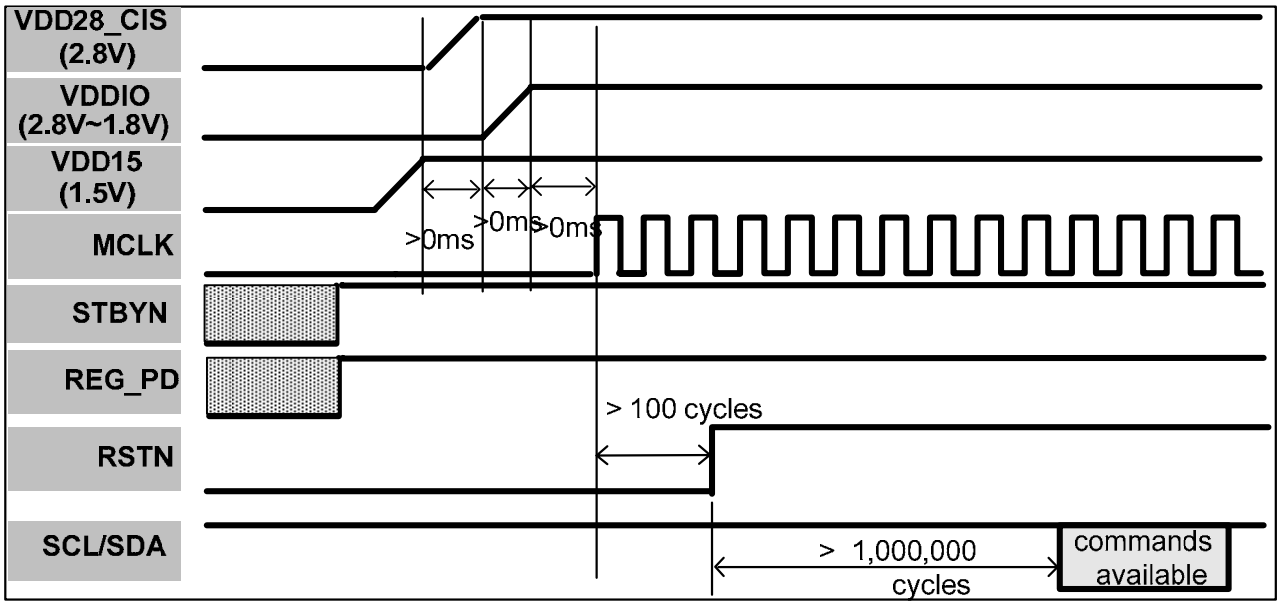
Chip-ID read enable register → <2.6Bh> [4] = 1'b
module information read register → <2.6Ch> ~ <2.71h>, that is Page 02

POWER UP/DOWN SEQUENCE



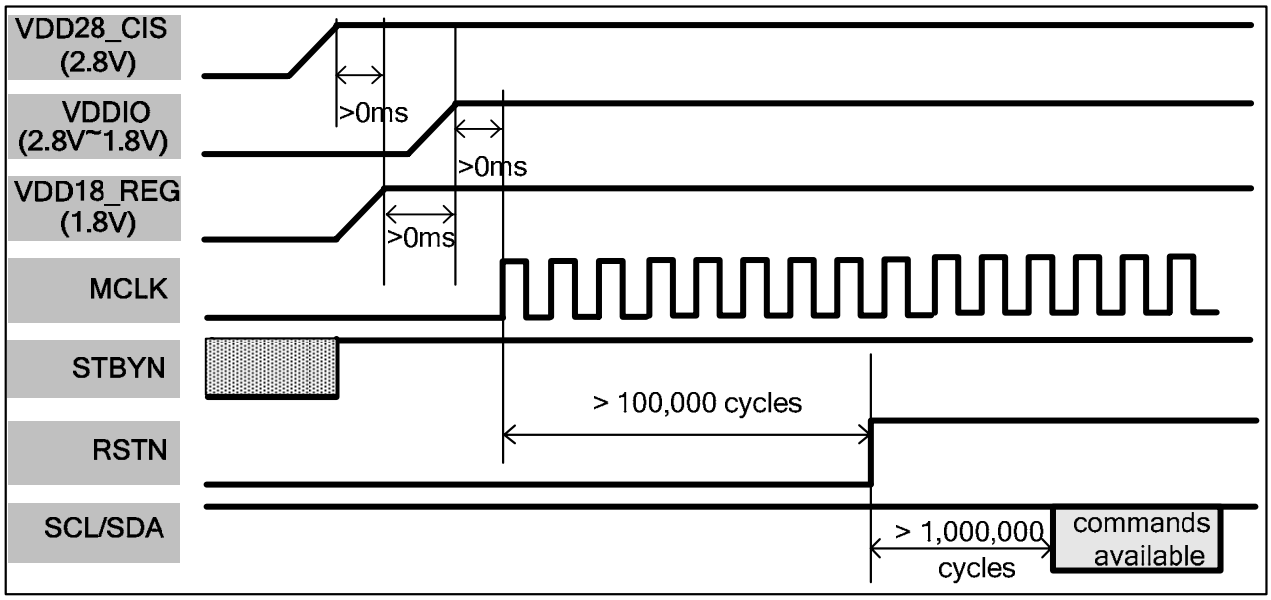
[NOTE]
1) If you don't use a STBYN signal, we recommend it holds a high instead of using a camera VDDIO.
2) If you use Internal Regulator, you should VDD15 connect 1uF Capacitor to digital ground.

Figure 43: Power Up Sequence for External Clock Using Internal Reaulator



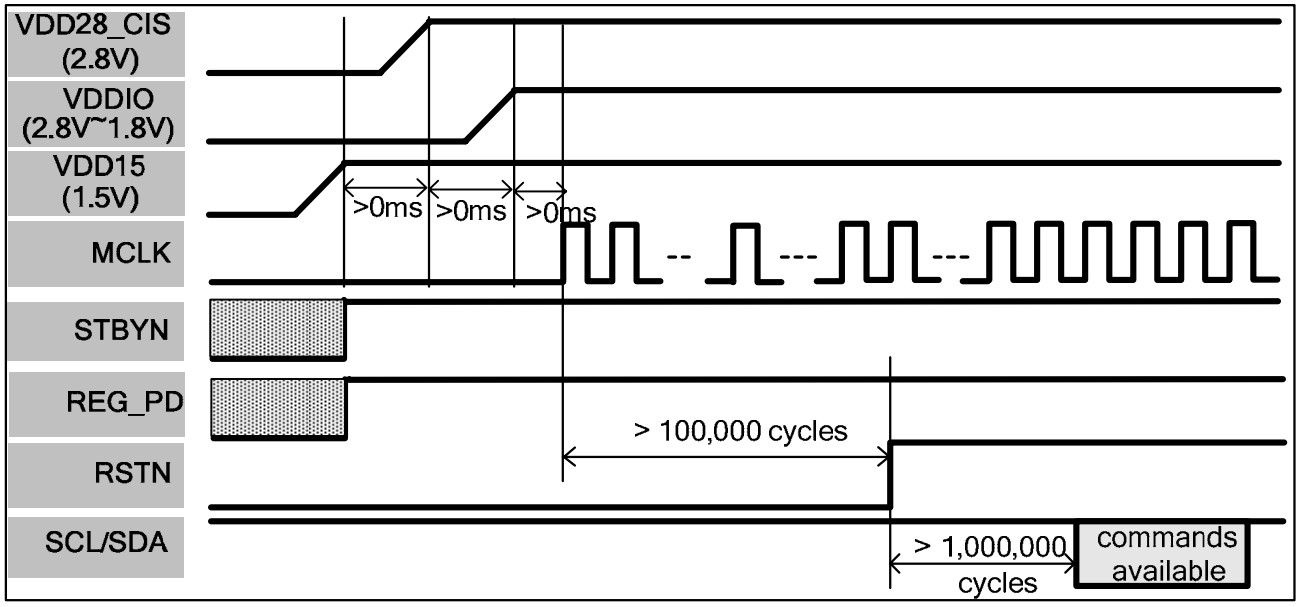
[NOTE]
1) If you don't use a STBYN signal, we recommend it holds a high instead of using a camera VDDIO.

Figure 44: Power Up Sequence for External Clock Not-Using Internal Regulator



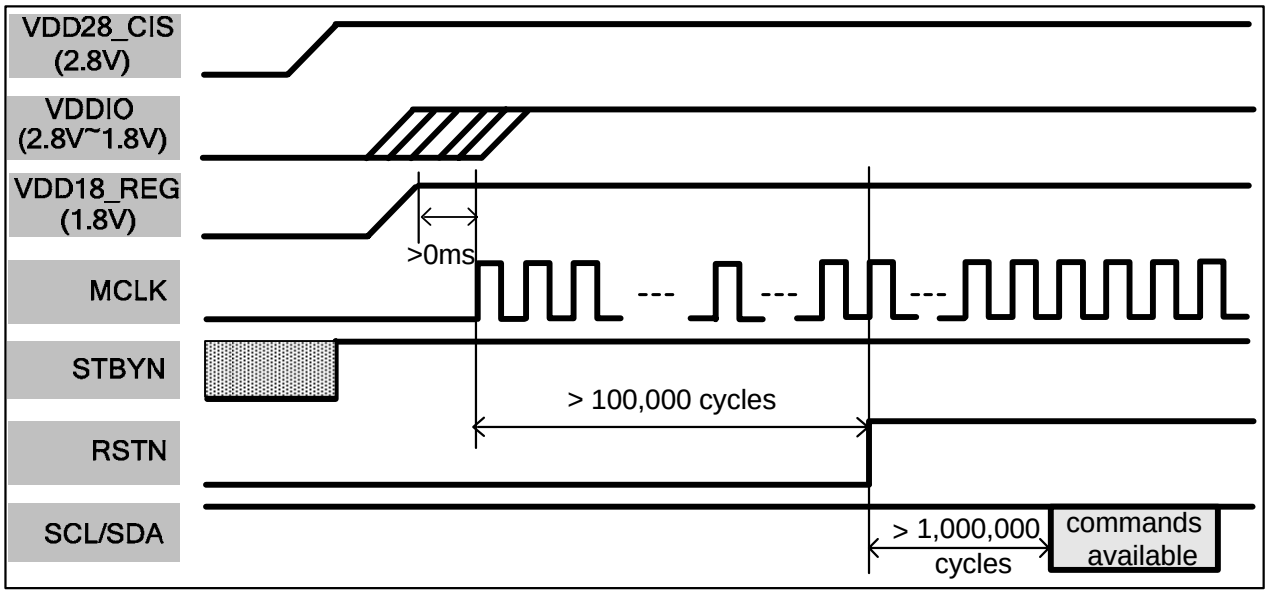
[NOTE]
1) If you use PLL Clock, we recommend a STBYN signal holds a low for 20 cycles(minimum) after VDDIO, VDD18_REG(VDD15), and VDD28_CIS go high completely.
2) If you use Internal Regulator, you should VDD15 connect 1uF Capacitor to digital ground.

Figure 45: Power Up Sequence for PLL Clock Using Internal Regulator



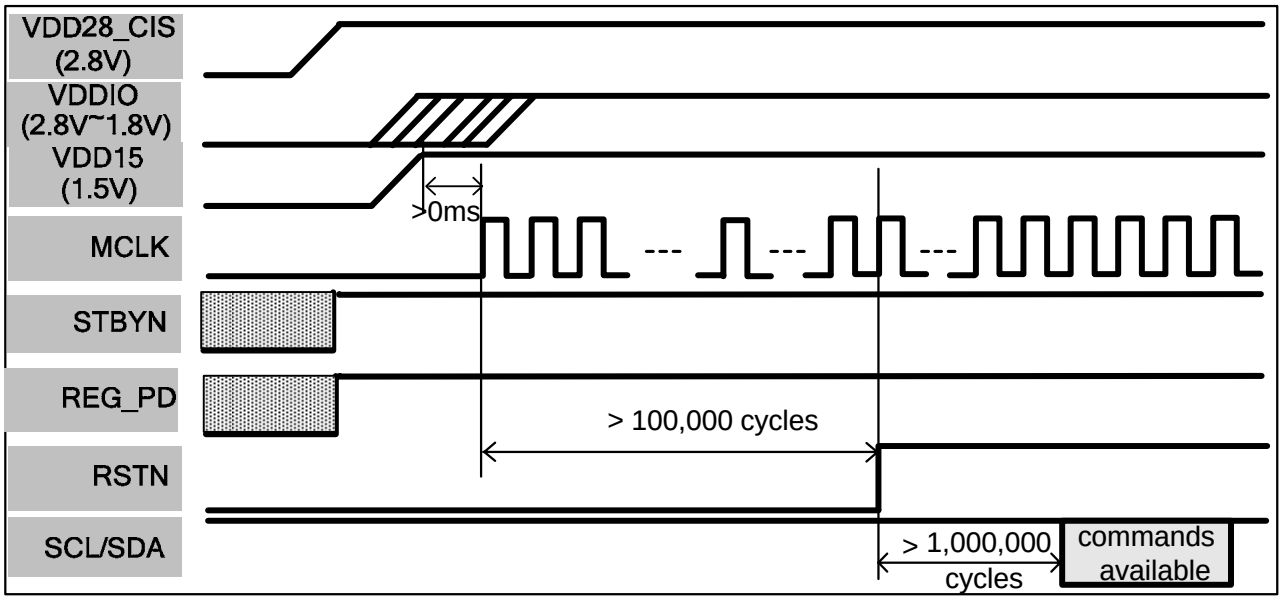
[NOTE]
If you use PLL Clock, we recommend a STBYN signal holds a low for 20 cycles(minimum) after VDDIO, VDD18_REG(VDD15), and VDD28_CIS go high completely.

Figure 46: Power Up Sequence for PLL Clock Not-Using Internal Regulator



[NOTE]
1) If you use an only one slave, VDDIO has no relation with VDD18_REG.
2) If you use Internal Regulator, you should VDD15 connect 1uF Capacitor to digital ground.

Figure 47: Power Up Sequence for only one slave operation Using Internal Regulator



[NOTE]
If you use an only one slave, VDDIO has no relation with VDD18_REG.

Figure 48: Power Up Sequence for only one slave operation Not-using Internal Regulator

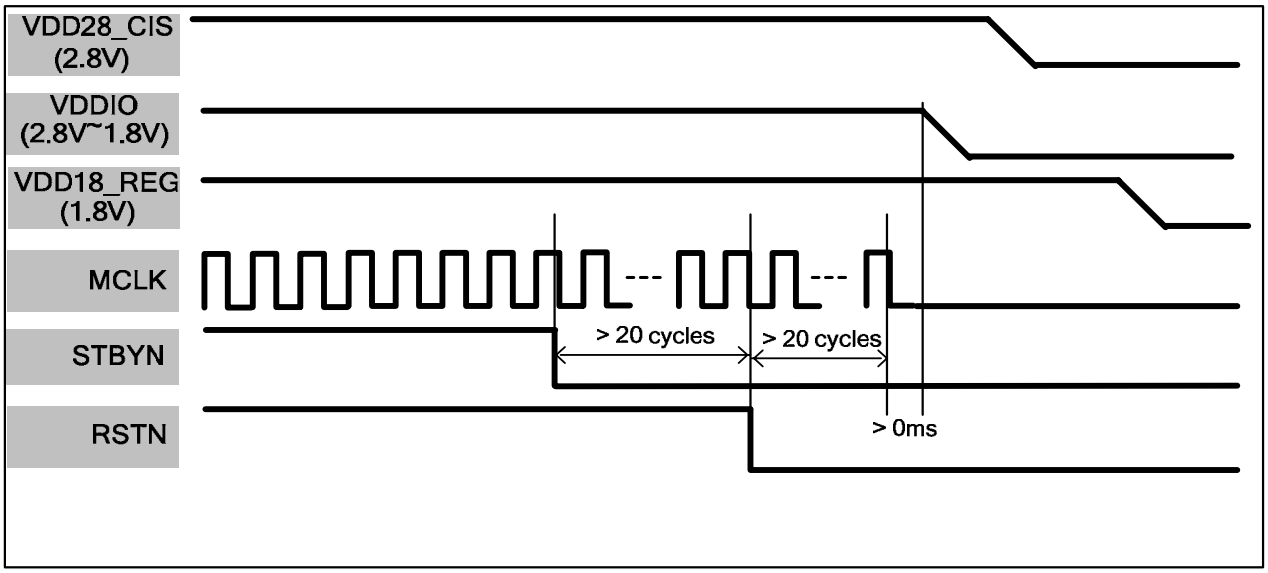


Figure 49: Power Down Sequence Using Internal Regulator

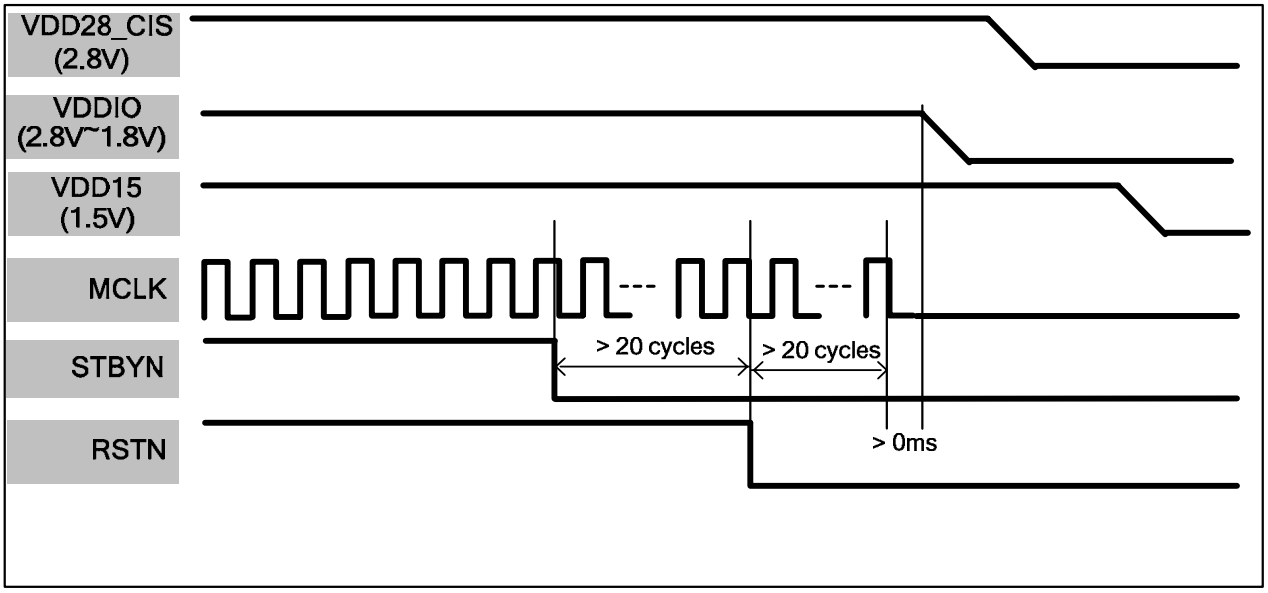
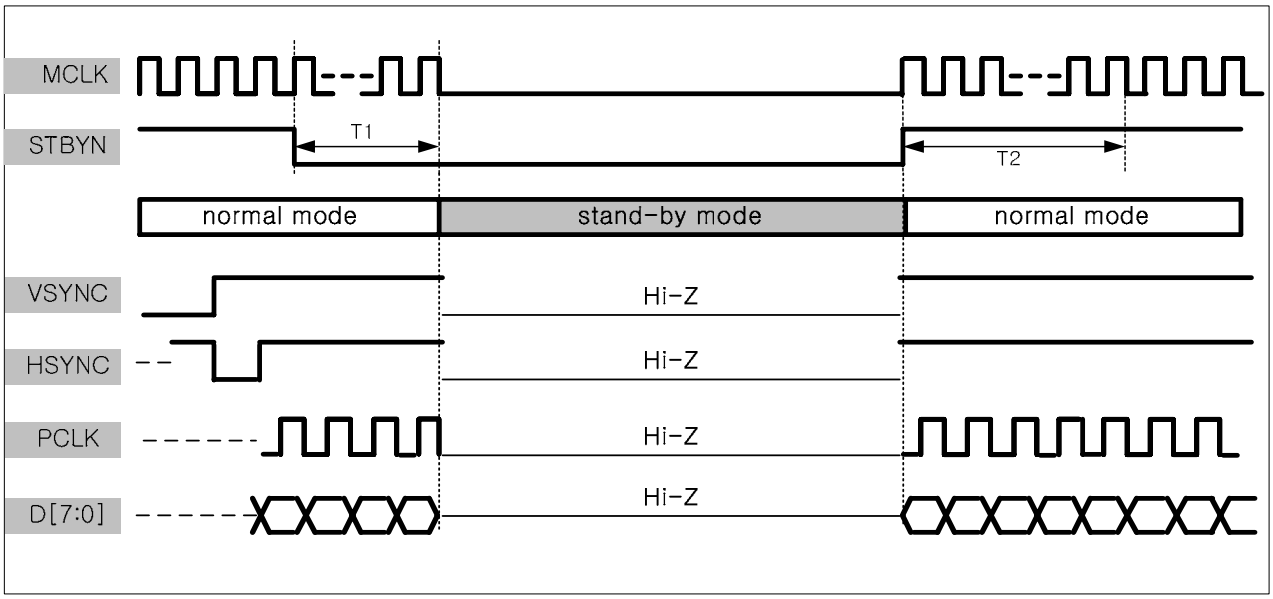


Figure 50: Power Down Sequence Not-using Internal Regulator

STAND-BY SEQUENCE



SYMBOL	PARAMETER	MIN	MAX	UNIT
T1	STBYN ↓ to Output Tri-state Delay	20	-	cycle
T2	STBYN ↑ to Valid Output Delay	100,000	-	cycle

[NOTE]
(1) cycle : MCLK
(2) PLL lock time of 28000 MCLK cycles is required after STBYN goes high.

Figure 51: Stand-By Sequence

IMAGING CHARACTERISTICS

Table 2: Imaging Characteristics

Parameter	Unit	Value	Remark
Effective resolution	pixel	1600 x 1200	
Active resolution	pixel	1616 x 1216	
Optical fomat	Inch	1/4	
Pixel size	Um	2.25um	
Shutter type	-	Electronic rolling shutter	
Full saturation	mV	580	
ADC saturation	mV	530	
Sensitivity	mV/lux.sec	TBD	
Dark current	mV/sec	< 1	
Random noise	e-	6	
Dynamic range	dB	> 59	
Max. SNR	dB	> 39	
Max. Gr/Gb ratio		< 1.05	
Max. frame rate	fps	15fps@full resolution	
ADC resolution	bit	10	

ELECTRICAL CHARACTERISTICS

Table 3: Absolute Maximum Rating

Characteristics	Symbol	Value	Unit
I/O Digital Power (2.8V ~ 1.8V)	V_{DDIO1}(1)	-0.3 to 3.8	V
	V_{DDIO2}(2)	-0.3 to 2.5	
Analog Power (2.8V)	V_{DDA}	-0.3 to 3.8	
Regulator Power (1.8V)	V_{DD18_REG}(3)	-0.3 to 2.5	
Core Digital Power (1.5V)	V_{DD15}(4)	-0.3 to 2.0	
Input Voltage	V_{IN}	-.0.3 to 3.8	
Operating Temperature	V_{OPR}	-20 to +60	°C
Storage Temperature	V_{STG}	-40 to +85	

[NOTE]
(1) 2.8V I/O Power Applied to VDDIO pins
(2) 1.8V I/O Power Applied to VDDIO pins
(3) 1.8V Regulator Power Applied to VDD18_REG pins
(4) Internal Regulator is not used and 1.5V Digital Power Applied to VDD15 pins directly

Table 4: DC Characteristics

(V_{DDH} = 2.8V ± 0.25V, V_{DDL} = 1.5V ± 0.1V, Ta = -20 to + 60 °C)

Characteristics	Symbol	Condition	Min	Typ	Max	Unit
Operating voltage	V_{DD28_CIS}	Applied to VDD28_CIS	2.55	2.8	3.05	V
	V_{DD18_REG}	Applied to VDD18_REG	1.65	1.8	1.95	
	V_{DD15}	Applied to VDD15	1.40	1.5	1.60	
	V_{DDIO1}	Applied to VDDIO	2.55	2.8	3.05	
	V_{DDIO2}	Applied to VDDIO	1.65	1.8	1.95	
Input voltage(1)	V_{IH}	-	0.7* V_{DDIO}	-	-	
	V_{IL}	-	-	-	0.2* V_{DDIO}	
Input leakage current(2)	I_{IL}	V_{IN} = V_{DDH} to V_{SS}	-10	-	10	uA
Input leakage current with pull-down(3)	I_{ILD}	V_{IN} = V_{DDH}	5	18	40	
Input leakage current with pull-up(4)	I_{ILU}	V_{IN} = V_{SS}	-40	-18	-5	

High level output voltage	V_{OH}	I_{OH} = -100uA(4)(5)	V_{DDIO}-0.2	-	-	V
		I_{OH} = -4mA(4) I_{OH} = -2,-4,-6,-8mA(5)	0.7*V_{DDIO}			
Low level output voltage	V_{OL}	I_{OL} = 100uA(4)(5)	-	-	0.2	
		I_{OL} = 4mA(4) I_{OL} = 2,4,6,8mA(5)			0.3*V_{DDIO}	
High-Z output leakage current (6)	I_{OZ}	V_{OUT} = V_{SS} or V_{DDH}	-10	-	10	uA
Input capacitance(1)	C_{IN}	-	-	-	4	pF
Supply current	I_{STB}	STBYN=Low(Active) All input clocks = Low 0 lux illumination	-	40	150	uA
	I_{DD}	f_{MCLK} = 27MHz	-	130	180	mA
Operation Power Consumption	P_{OP}	-	-	200	300	mW

[NOTE]
(1) Applied to STRB_IN, SCL, SDA, CLKSEL, TST, STBYN, SCE, RSTN, MCLK, AF_SCL, AF_SDA, IIC_ID pins
(2) Applied to SCL, SDA, CLKSEL, STBYN, RSTN, MCLK, AF_SCL, AF_SDA pins
(3) Applied to STRB_IN, TST, SCE, IIC_ID pins
(4) Applied to HSYNC, VSYNC pins
(5) Applied to SCL, SDA, PCLK, D0 to D9 pins
(6) Applied to SCL, SDA pins when in High-Z output state
Applied to HSYNC, VSYNC, PCLK, D0 to D9 pins when in Stand-by Mode

Table 5: Electrostatic Characteristics

INDEX		Electrostatic Standard			UNIT	Remark
		PIN NO.	Design Target	Reference Product		
Human Body Model		ALL	±2000V		V	
Machine Model		ALL	±200V		V	
Latch-up	I-Test	ALL	Positive trigger : +(Inominal + 100mA) Negative trigger : -100mA		mA	
	V-Test	Power	1.5X Max Vsupply		V	

Table 6: AC Characteristics

Characteristic		Symbol	Condition	Min	Typ	Max	Unit
Main input clock frequency	Using PLL	f_{MCLK}	Duty = 50%	14	-	27	MHz
	Not using PLL	f_{MCLK}	Duty = 50%	27	-	75	MHz
Data output clock frequency		f_{PCLK}	-	-	-	75	MHz
Using PLL		T1	D[7:0] output	3	-	-	ns
		T2	HSYNC output	3	-	-	ns
		T3	VSYNC output	3	-	-	ns
		T4	D[7:0] output	8	-	-	ns
		T5	HSYNC output	8	-	-	ns
		T6	VSYNC output	8	-	-	ns
Not Using PLL		T1	D[7:0] output	4	-	-	ns
		T2	HSYNC output	4	-	-	ns
		T3	VSYNC output	4	-	-	ns
		T4	D[7:0] output	8	-	-	ns
		T5	HSYNC output	8	-	-	ns
		T6	VSYNC output	8	-	-	ns

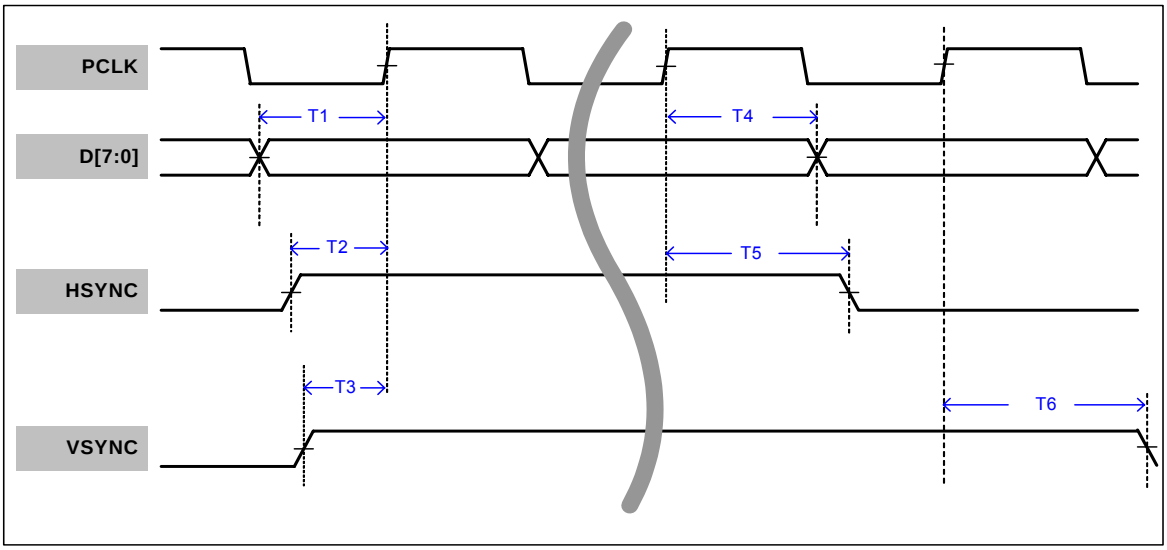
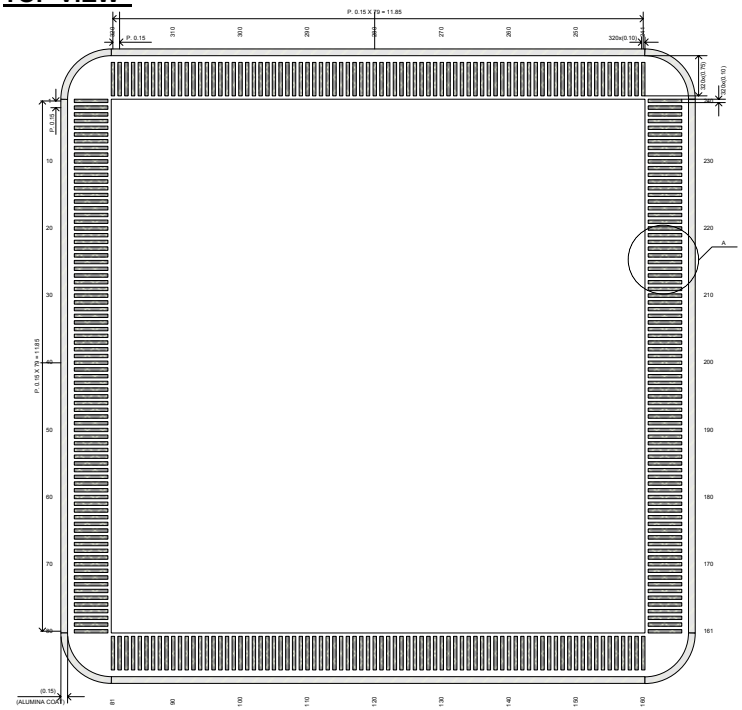


Figure 52: Output Timing

[NOTE]
(1) T1~T6 at PCLK(66MHz)=6mA, Data=6mA, Sync=4mA, External Cap=10pF

PACKAGE INFORMATION (320-CLCC)

TOP VIEW



BOTTOM VIEW

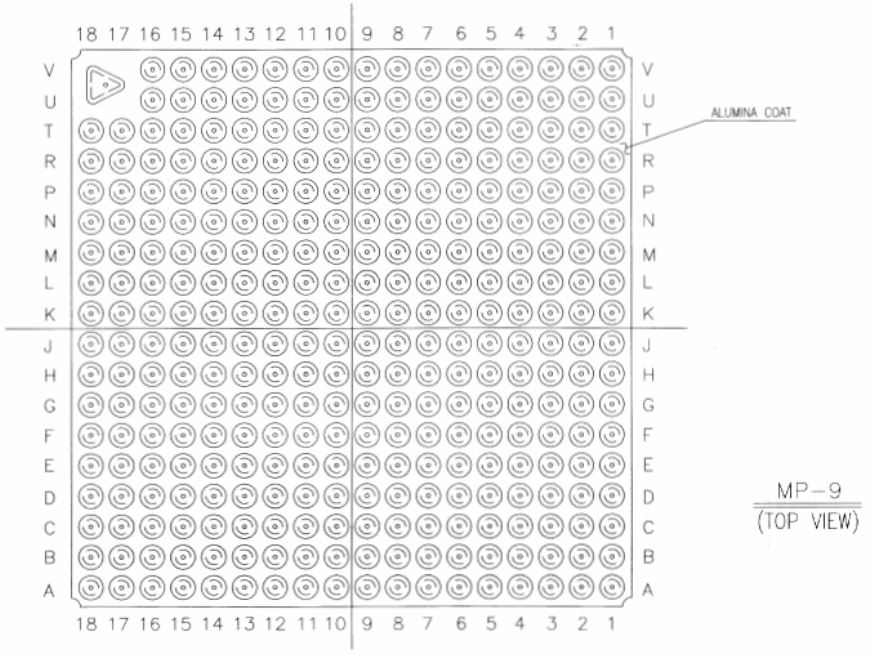


Figure 53: Package Information (320 CLCC)

REGISTER DESCRIPTION

Register control mode

Page	Name	Address
00h	Command	00h~FFh
01h	ISP 1	00h~EBh
02h	CIS	00h~79h
03h	Image Format(1)	00h~EFh
04h	Image Format(2)	00h~EFh
05h	ISP 5	00h~92h
06h	ODM zone	00h~6Fh
07h	Program constant	00h~9Fh
09h	ISP 9	00h~CDh
0Bh	Suppress	00h~DEh
0Eh	AF E	00h~37h
13h	AF 13	00h~DCh
14h	Image Format(3)	00h~8Fh
15h	Boundary	00h~37h
1Ah	CIS Chip ID	00h~0Dh
1Bh	ISP 1B	00h~D5h
1Ch	Shading	00h~FBh
1Dh	Gamma & Edge	00h~A2h
1Eh	Suppress 2	00h~1Fh
20h	AE Control	00h~C0h
22h	AWB2	00h~F8h
28h	Digital Zoom	00h~DFh
ALL	I2C Page Address	FCh

I2C format (standard)

IIC_ID is Low

WRITE : <5A> <Addr> <Data>

READ : <5A> <Addr> <restart> <5B> [Data]

IIC_ID is High

WRITE : <52> <Addr> <Data>

READ : <52> <Addr> <restart> <53> [Data]

Ex) If you try to WRITE data '2Fh' at address '30h' in ISP(page 01),

I2C command is as follows,

IIC_ID is Low

<5Ah> <FCh> <01h>

<5Ah> <30h> <2Fh>

IIC_ID is High

<52h> <FCh> <01h>

<52h> <30h> <2Fh>

If you try to READ data XXh at address '1Bh' in CIS(page 02),

I2C command is as follows,

IIC_ID is Low

<5Ah> <FCh> <02h>

<5Ah> <1Bh> <restart> <5B> [XXh]

IIC_ID is High

<52h> <FCh> <02h>

<52h> <1Bh> <restart> <52> [XXh]

I2C addresses are represented as below in this document.
<1.23h> : Page1, address 23h, 1byte
<0.23h[7]> : Page0, address 23h, bit7
<0.23h[3:0]> : Page0, address 23h, bit3 ~ bit0
<0.23h – 34h> : Page0, address from 23h to 34h, 11 bytes

1. ARM COMMAND REGISTER MAP (PAGE 00H)

Addr	Reset Value	Mnemonic	Attr	Bits	Descriptions
<0.00h>	00h	**Reserved**		[7:0]	
<0.01h>	10h	**Reserved**		[7:0]	
<0.02h>	00h	**Image Format**	R/W	[7] [6:0]	White Zoom Table Image Format 0x00 : UXGA 0x01 : SXGA 0x02 : VGA 0x03 : QVGA 0x04 : QQVGA 0x05 : CIF 0x06 : QCIF 0x07 : H = 2, V = 1 0x08 : H = 1, V =2 0x09 : H = 2, V = 2 0x0A : H = 4, V = 1 0x0B : H = 4, V = 4 0x0C : Reserved preset * Preset for Subsampling or scaling of Image format 1, 2 and 3 page(Page 3, 4 & 14h) will be loaded to Target Registers (Page 1,2,5, 9 & 1Bh) when performing this command.
<0.03h>	43h	**Function On Off 1**	R/W	[7] [6] [5] [4:2] [1] [0]	V sync wait for suppress related with AWB V sync wait for AWB AE_TARGET_SUPPRESS_ON (related reg. <7.26h~2Fh >) Reserved AWB_ON_BIT AE_ON_BIT
<0.04h>	33h	**Cloudy R,B offset**	R/W	[7:4] [3:0]	Cloudy R offset, Cloudy B offset
<0.05h>	75h	**Sunny R,B offset**	R/W	[7:4] [3:0]	Sunny R offset, Sunny B offset
<0.06h -0Ch>		**Reserved**		[7:0]	
<0.0Dh>	28h	**CIS_Mode**	R/W	[7:6] [5:4] [3:0]	Reserved shutterEnable_Mode - shutterEnable <2.02.[2]> 10b : shutterEnable_AlwaysOff 11b : shutterEnable_AlwaysOn if <0.83h>[2] is on, this function does not work. Reserved
<0.0Eh>	00h	**RGB_Shade_On**	R/W	[7:6] [0]	Reserved Fixed RGB Shade On 0b : RGB Shade Off 1b : RGB Shade On

Addr	Reset Value	Mnemonic	Attr	Bits	Descriptions
<0.0Fh>	00h	**DIGITAL_ZOOM**	R/W	[7:0]	The scaler will be set the preset table from index 0x00 to index 0x06. (refer to page 28h)
<0.10h -22h>		**Reserved**			
<0.23h>	98h	**Mirror Option**	R/W	[7] [6] [5] [4] [3] [2] [1] [0]	Mirror_FastExe_ON Wait for shading ON Reserved Pre G mirror On MIRROR_ISP_CONTROL Effect_Blackscreen_On related reg <0.25h> Reserved Mirror_BlackScreen_ON
<0.24h>	42h	**Image Format Option**	R/W	[7] [6] [5] [4] [3:0]	Write shading value table ON No wait for vsync during resizing BlackScreenS_ON BlackScreenE_ON SkipCount
<0.25h>	00h	**SPECIAL_EFFECT**	R/W	[7:5] [4] [3] [2] [1] [0]	Reserved Green Effect - It will be able to change by CIS input order (related reg <7.34h,35h>) Black & White Effect Negative Effect Aqua (or Sepia) Effect - It will be able to change by CIS input order (related reg <7.32h,33h>) Sepia (or Aqua) Effect - It will be able to change by CIS input order (related reg <7.30h,31h>)
<0.26h>	04h	**AE_MODE**	R	[7:0]	(INFO) 0- SHUTTER AE 1- AGC AE 2- FRAME AE 4- Dgain AE
<0.27h>		**Reserved**			
<0.28h>		**Reserved**			
<0.29h>	04h	**Brightness_H**	R/W	[7:4] [3:0]	Reserved Set Y gain value[11:8] (00h~FFFh) x1 : 400h (max x4)
<0.2Ah>	00h	**Brightness_L**	R/W	[7:0]	Set Y gain value[7:0] (00h~FFFh)
<0.2Bh>	04h	**Color_Level_H**	R/W	[7:4] [3:0]	Reserved Set C gain value[11:8] (00h~FFFh) x1 : 400h (max x4)
<0.2Ch>	A0h	**Color_Level_L**	R/W	[7:0]	Set C gain value[7:0] (00h~FFFh)
<0.2Dh>		**Reserved**			
<0.2Eh>	00h	**WB Manual Step**	R/W	[7:0]	auto mode White Step move 0 : nothing

Addr	Reset Value	Mnemonic	Attr	Bits	Descriptions
					plus : toward 3100 minus : toward 5100
<0.2Fh>		**Reserved**			
<0.30h>	00h	**WBMODE**	R/W	[7:0]	00h : AWB auto mode 01h : Indoor 3100 mode (Tungsten) 02h : Outdoor 5100 mode (Fluorescent) 03h : Indoor 2000 mode 04h : AE/AWB halt 05h : Cloudy (6000) Rgain_out = WBR5100 + Radj + Cloudy R offset Bgain_out = WBB5100 + Badj - Cloudy B offset 06h : Sunny (8000) Rgain_out = WBR5100 + Radj + Sunny R offset Bgain_out = WBB5100 + Badj - Sunny B offset
<0.31h>		**Reserved**			
<0.32h>	02h	**AWB_AVERAGE_NUM**	R/W	[7:0]	AWB average Number (max : 32)
<0.33h -3Ch>		**Reserved**			
<0.3Dh>	04h	**LOW_Y_Min**	R/W	[7:0]	Y Min level Limit for AWB when Low Y
<0.3Eh>	10h	**NORMAL_Y_Min**	R/W	[7:0]	Y Min level Limit for AWB when Normal Y
<0.3Fh -47h>		**Reserved**			
<0.48h>	40h	**R-Y POSI GAIN(2000)**	R/W	[7:0]	R-Y Positive Gain Coefficient of R-Y Signal(2000)
<0.49h>	40h	**R-Y NEGA GAIN(2000)**	R/W	[7:0]	R-Y Negative Gain Coefficient of R-Y Signal(2000)
<0.4Ah>	00h	**R-Y HUE POSI GAIN(2000)**	R/W	[7:0]	R-Y Positive Hue Coefficient of B-Y Signal(2000)
<0.4Bh>	16h	**R-Y HUE NEGA GAIN(2000)**	R/W	[7:0]	R-Y Negative Hue Coefficient of B-Y Signal(2000)
<0.4Ch>	4Ah	**B-Y POSI GAIN(2000)**	R/W	[7:0]	B-Y Positive Gain Coefficient of B-Y Signal(2000)
<0.4Dh>	40h	**B-Y NEGA GAIN(2000)**	R/W	[7:0]	B-Y Negative Gain Coefficient of B-Y Signal(2000)
<0.4Eh>	10h	**B-Y HUE POSI GAIN(2000)**	R/W	[7:0]	B-Y Positive Hue Coefficient of R-Y Signal(2000)
<0.4Fh>	00h	**B-Y HUE NEGA GAIN(2000)**	R/W	[7:0]	B-Y Negative Hue Coefficient of R-Y Signal(2000)
<0.50h>	40h	**R-Y POSI GAIN(INDOOR)**	R/W	[7:0]	R-Y Positive Gain Coefficient of R-Y Signal(INDOOR)
<0.51h>	40h	**R-Y NEGA GAIN(INDOOR)**	R/W	[7:0]	R-Y Negative Gain Coefficient of R-Y Signal(INDOOR)
<0.52h>	00h	**R-Y HUE POSI GAIN(INDOOR)**	R/W	[7:0]	R-Y Positive Hue Coefficient of B-Y Signal(INDOOR)
<0.53h>	20h	**R-Y HUE NEGA GAIN(INDOOR)**	R/W	[7:0]	R-Y Negative Hue Coefficient of B-Y Signal(INDOOR)
<0.54h>	4Ah	**B-Y POSI GAIN(INDOOR)**	R/W	[7:0]	B-Y Positive Gain Coefficient of B-Y Signal(INDOOR)
<0.55h>	40h	**B-Y NEGA GAIN(INDOOR)**	R/W	[7:0]	B-Y Negative Gain Coefficient of B-Y Signal(INDOOR)
<0.56h>	00h	**B-Y HUE POSI GAIN(INDOOR)**	R/W	[7:0]	B-Y Positive Hue Coefficient of R-Y Signal(INDOOR)

Addr	Reset Value	Mnemonic	Attr	Bits	Descriptions
<0.57h>	00h	**B-Y HUE NEGA GAIN(INDOOR)**	R/W	[7:0]	B-Y Negative Hue Coefficient of R-Y Signal(INDOOR)
<0.58h>	4Ah	**R-Y POSI GAIN(OUTDOOR)**	R/W	[7:0]	R-Y Positive Gain Coefficient of R-Y Signal(OUTDOOR)
<0.59h>	4Ah	**R-Y NEGA GAIN(OUTDOOR)**	R/W	[7:0]	R-Y Negative Gain Coefficient of R-Y Signal(OUTDOOR)
<0.5Ah>	00h	**R-Y HUE POSI GAIN(OUTDOOR)**	R/W	[7:0]	R-Y Positive Hue Coefficient of B-Y Signal(OUTDOOR)
<0.5Bh>	20h	**R-Y HUE NEGA GAIN(OUTDOOR)**	R/W	[7:0]	R-Y Negative Hue Coefficient of B-Y Signal(OUTDOOR)
<0.5Ch>	4Ah	**B-Y POSI GAIN(OUTDOOR)**	R/W	[7:0]	B-Y Positive Gain Coefficient of B-Y Signal(OUTDOOR)
<0.5Dh>	40h	**B-Y NEGA GAIN(OUTDOOR)**	R/W	[7:0]	B-Y Negative Gain Coefficient of B-Y Signal(OUTDOOR)
<0.5Eh>	18h	**B-Y HUE POSI GAIN(OUTDOOR)**	R/W	[7:0]	B-Y Positive Hue Coefficient of R-Y Signal(OUTDOOR)
<0.5Fh>	0Ah	**B-Y HUE NEGA GAIN(OUTDOOR)**	R/W	[7:0]	B-Y Negative Hue Coefficient of R-Y Signal(OUTDOOR)
<0.60h>		**Reserved**			
<0.61h>	00h	**EIT_SETTING**		[7:2] [1] [0]	Reserved EIT_Update EIT_Load related reg <0.E0h~E7h>
<0.62h>	02h	**Function On Off 3**	R/W	[7] [6] [5] [4] [3] [2] [1] [0]	RGB shading T2 suppress enable (related reg <B.B8h~C1h>) Color correction T suppress enable (related reg <B.96h~99h, C2h~D3h>) AWB_SHRINK_OPTION Reserved Mirror Shade Enable RGB Shading T1 suppress enable (related reg <B.9Ah~B7h>) Hue Enable Color correction interpolation enable (related reg <B.60h~95h>)
<0.63h -6Bh>		**Reserved**			
<0.6Ch>	10h	**AeTarget_Low**	R/W	[7:0]	AE Target Low
<0.6Dh>	01h	**AeTarget_High**	R/W	[7:0]	AE Target High
<0.6Eh>	00h	**AF Command**	R/W	[7:0]	AF command 00h : Idle state 01h : Initialize AF and move to the initial wanted position 02h : Move to the initial wanted position 03h : Single AF operation start 04h : Manual Focus operation start using <13.49h> 05h : Activate real continuous AF 06h : Activate pseudo continuous AF 07h : Manual Focus (forward) using <13.4Bh> as offset position. 17h : Manual Focus (Backward) using <13.4Bh> as offset position.

Addr	Reset Value	Mnemonic	Attr	Bits	Descriptions
					08h : Disable AF (to enable initilize should be called) 09h : test pulse generation by using table method 80h : Power OFF (forcely) 81h : Power ON (to enable initialize should be called)
<0.6Fh>	00h	**AF IIC R/W Command**	R/W	[7:0]	01h : Write Command Execution 02h : Read Command Execution
<0.70h>	FFh	**AE_AWB_STORE_RESTORE**	R/W	[7] [6] [5:2] [1] [0]	Not store/restore AWB setting Not store/restore AE setting Reserved AE/AWB setting restore from register <7.05h~0Eh> to module AE/AWB setting store to register <7.05h~0Eh> from module
<0.71h>	00h	**Clock_Divider**	R/W	[7:0]	00h : CIS = Mclk / 2 (default), ISP = XTAL / 2 (default) 01h : CIS = Mclk / 4, ISP = XTAL / 4 02h : CIS = Mclk / 8, ISP = XTAL / 8
<0.72h>	A0h	**CIS Main Clock**	R/W	[7:0]	00h : 27Mhz 01h : 13.5Mhz Others : Main Clock value = Used clock(Mhz)*10 / 2 Ex) if used clock is 20.0Mhz : (20)*10/2 + 0 = MainClock<0.72h> + ClockAdd<7.37h> = <0.72h>(=64h) * 2 + <7.37h>(=0h) 20.5Mhz : (20)*10/2 + 5 = MainClock<0.72h> + ClockAdd<7.37h> = <0.72h>(=64h) * 2 + <7.37h>(=5h)
<0.73h>	11h	**Frame_AE_Mode**	R/W	[7:4] [3:1] [0]	The number of Dummy VSize (N) Reserved Frame AE On/Off VBlankMax calculation for Frame AE (N) : VBlankMax = VBlank_init + (N) * VSize Ex) FrameRate/3 : 21h FrameRate/8 : 71h * Sub Sampling, Scale down Table Data(Page 3,4) will be loaded to Target Registers (Page 1,2) when performing this command.
<0.74h>	08h	**Flicker Command**	R/W	[7:0]	00h : Flicker Nothing 14h : Auto Flicker Mode, start from 50Hz 18h : Auto Flicker Mode, start from 60Hz 04h : Manual Flicker Mode, start from 50Hz 08h : Manual Flicker Mode, start from 60Hz 80h : FlickerTable_NoAccess (related reg <0.C0h~DFh>) * Data of Image size table(Page 03h, 04h, 14h, 15h, 1Ch) will be loaded to Target Registers (Page 01h, 02h, 09h, 1Bh) when performing this command.
<0.75h>	00h	**Mirror/ Flip Command**	R/W	[7:0]	01h : Vertical mirror (toggling mode) 02h : Horizontal mirror (toggling mode) 03h : Symmetric mirror (toggling mode)

Addr	Reset Value	Mnemonic	Attr	Bits	Descriptions
					04h : default screen (absolute mode) 05h : horizontal-vertical mirrored screen (absolute mode) 06h : horizontal mirrored screen (absolute mode) 07h : Vertical mirrored screen (absolute mode)
<0.76h>		**Reserved**			
<0.77h>		**Reserved**			
<0.78h>	6Ah	**AGC Maximum**	R/W	[7:0]	Set maximum value of AGC (00h~7Fh)
<0.79h>	FFh	**WhiteBalance R gain offset**	R/W	[7:0]	Radjust : 80h~7Fh (-128~127)
<0.7Ah>	01h	**WhiteBalance B gain offset**	R/W	[7:0]	Badjust : 80h~7Fh (-128~127)
<0.7Bh>	00h	**Vsync Skip Count**	R/W	[7:0]	00h(Fastest) ~ FEh(Slowest) FFh : AE, AWB Stop
<0.7Ch>	00h	**AWB Tracking Speed**	R/W	[7:0]	AWB Execution Values Per Vsync
<0.7Dh>		**Reserved**			
<0.7Eh>	00h	**Function On Off 0**	R/W	[7] [6] [5] [4] [3] [2] [1] [0]	Digital BPRM On(1)/Off(0) (related reg <B.0Bh~1Eh>) Noise Filter On(1)/Off(0) (related reg <B.28h~41h>) CLPF suppress On(1)/Off(0) (related reg <B.D4h~D9h>) GrGb G Suppress On(1)/Off(0) (related reg <B.21h~27h> AWB R,B offset Suppress (related reg <B.54h~5Bh> Color Gain Suppress On(1)/Off(0) (related reg <B.08h~0Ah>) Ygain On(1)/Off(0) (related reg <B.04h~07h>) Digital Clamp On(1)/Off(0) (related reg < B.00h~03h>)
<0.7Fh>	FFh	**Factory Use**	R/W	[7:0]	00h : 2000,3100 R,B save 01h : 3100 R,B save 02h : 5100 R,B save 03h : 2000 R,B save 04h : D65 R,B save 05h : CWF R,B save 06h : Incand A R,B save 0x10 : OneJump
<0.80h>		**Reserved**			
<0.81h>	10h	**Function On Off 2**	R/W	[7] [6] [5] [4] [3] [2] [1] [0]	AWB new classify option Wait Vsync for X shading zoom gain when AWB off X Shading zoom gain On (related reg <B.DEh>) Mirror xshading on Image Format Wait Vsync Reserved X_Shading suppress On(1)/Off(0) (related reg <B.DAh~DDh>) Ggain Offset On(1)/Off(0)
<0.82h>	01h	**SAVE_SVC_ON**	R/W	[7:1] [0]	Reserved Save service on(1)/Off(0)
<0.83h>	00h	**Function On Off 4**	R/W	[7:4] [3]	Reserved Execute suppress when image resizing

Addr	Reset Value	Mnemonic	Attr	Bits	Descriptions
				[2:0]	Reserved
<0.84h -88h>		**Reserved**			
<0.89h>	00h	**Edge_MODE**		[7] [6] [5:2] [1] [0]	Edge2 Negative Suppress Edge2 Positive Suppress Reserved Edge Negatice Suppress Edge Positive Suppress
<0.8Ah>	0Ah	**AWB_UNSTABLE_DIFF**	R/W	[7:0]	Awb stable constant
<0.8Bh>	05h	**AWB_UNSTABLE_COUNT**	R/W	[7:0]	Awb stable constant
<0.8Ch>	02h	**AWB Stable Count**	R/W	[7:0]	Digital Gain constant For Flicker
<0.8Dh>	08h	**AWB_UNSTABLE_MARGIN**	R/W	[7:0]	Awb stable margin
<0.8Eh -9Dh>		**Reserved**			
<0.9Eh>	02h	**Flicker Detection Status**	R	[7:0]	Flicker Status 00h : Off 01h : 50Hz 02h : 60Hz
<0.9Fh -AFh>		**Reserved**			
<0.B0h>	ABh	**Vendor ID**	R	[7:0]	Version Information
<0.B1h>	01h	**S/W Ver.**	R	[7:0]	Version Information
<0.B2h>	D2h	**Chip ID**	R	[7:0]	Version Information
<0.B3h>	01h	**Chip Ver.**	R	[7:0]	Version Information
<0.B4h>	01h	**AE Stable Status**	R	[7:0]	(info) AE stable status 0d : unstable 1d : stable
<0.B5h -B9h>		**Reserved**			
<0.BAh>	10h	**AWB/ AE Normal Difference**	R/W	[7:0]	Constant to run AWB
<0.BBh>	00h	**AWB_ AE DIFF_TH_H**	R/W	[7:0]	Constant to run AWB in AGC mode
<0.BCh>	80h	**AWB_AEDIFF_TH_L**	R/W	[7:0]	Constant to run AWB in AGC mode
<0.BDh -DFh>		**Reserved**			
<0.E0h>	00h	**EIT_LOAD_HH**	R/W	[7:0]	EIT value will be loaded
<0.E1h>	00h	**EIT_LOAD_HL**	R/W	[7:0]	EIT value will be loaded
<0.E2h>	00h	**EIT_LOAD_LH**	R/W	[7:0]	EIT value will be loaded

Addr	Reset Value	Mnemonic	Attr	Bits	Descriptions
<0.E3h>	00h	**EIT_LOAD_LL**	R/W	[7:0]	EIT value will be loaded
<0.E4h>	00h	**EIT_INFO_HH**	R/W	[7:0]	Current EIT value
<0.E5h>	03h	**EIT_INFO_HL**	R/W	[7:0]	Current EIT value
<0.E6h>	5Bh	**EIT_INFO_LH**	R/W	[7:0]	Current EIT value
<0.E7h>	F4h	**EIT_INFO_LL**	R/W	[7:0]	Current EIT value
<0.E8h -FFh>		**Reserved**			

2. ISP REGISTER MAP (PAGE 01H)

Addr	Reset Value	Mnemonic	RW	Bits	Descriptions
<1.00h>	80h	**TCMD**	R/W	[7] [6:5] [4] [3:2] [1] [0]	Div8_r 0b: using 1/4 PLL Clock 1b: using 1/2 PLL Clock(default) Main Clock Divider 00 : MCLK = XTAL/2(default) 01 : MCLK = XTAL/4 10: MCLK = XTAL/8 Red, Green Selection Inversion SCK : H → Red, SCK : L→ Green HSYNC_MODE 00 : No hsync during vertical blank 11 : According to Scaler Hsize Other : ISP counting Mode Vertical Input Sync Inversion Horizontal Input Sync Inversion
<1.01h>	55h	**SMODE**	R/W	[7:6] [5:4] [3:2] [1] [0]	AF_CON0 Output GPIO Port Control 00:PWM output 01:Pulse gen output 10,11: GPIO output AF_CON1 Output GPIO Port Control 00:PWM output 01:Pulse gen output 10,11: GPIO output AF_CON2 Output GPIO Port Control 00:PWM output 01:Pulse gen output 10,11: GPIO output Reserved Video Clock Inversion
<1.02h>	03h	**CRCB_SEL**	R/W	[7] [6] [5:4] [3:2] [1] [0] 	Reserved CK_RST_OFF, Main Clock Reset Off Every H Time CK_RST_SEL[1:0], Main Clock Phase Selection 00 : 0 Phase Shift, 01 : 90˚Phase Shift, 10 : 180˚Phase Shift, 11 : 270˚Phase Shift OUT_SEL[1:0], Output Data Type and Format Selection 00 : ITU.R-656 Format(YCbCr) 01 : ITU.R-601 Format(YCbCr) 10 : R/G/B Data 11 : CIS Raw Data YC_SEL, Y/C Inversion Data Output Order Selection Whether Y signal First or C signal First 0:C First(Cb/Y/Cr/Y) 1:Y First(Y/Cb/Y/Cr) CRCB_SEL, C Data Output Order Selection When Outputting YCbCr or RGB Data 0:Cb or R First(Y/Cb/Y/Cr or R/G/G) 1:Cr or B First(Y/Cr/Y/Cb or B/G/R)
<1.03h>	01h	**SW_RST**	R/W	[7:2] [1] [0]	Reserved Software Reset Enable Software Reset
<1.04h>	55h	**ARMCLK_DIV**	R/W	[7:6] [5:4] [3:2] [1:0	AZ_CON0 Output GPIO Port Control (AZ_CON0) 00:PWM output 01:Pulse gen output 10,11: GPIO output AZ_CON1 Output GPIO Port Control (AZ_CON1) 00:PWM output 01:Pulse gen output 10,11: GPIO output AZ_CON2 Output GPIO Port Control (AZ_CON2) 00:PWM output 01:Pulse gen output 10,11: GPIO output ARM Clock Divide (default : 1/2) 00:1/1 01:1/2 10:1/3 11:1/4
<1.05h>	60h	**SPECIAL_EFF_CON**	R/W	[7] [6] [5]	ylpf_on, y channel sigma filter on/off, 1 : on, 0 : off clpf_on, c channel low pass filter on/off, 1 : on, 0 : off CbCr_SEL, 1 : Cb 1st 422 format, 0 : Cr 1st 422 format

Addr	Reset Value	Mnemonic	RW	Bits	Descriptions
				[4] [3] [2] [1] [0]	NEGA_Y_EN, Y channel negative effect on/off, 1 : on, 0 : off NEGA_Cr_EN, Cr channel negative effect on/off, 1 : on, 0 : off NEGA_Cb_EN, Cb channel negative effect on/off, 1 : on, 0 : off SEPIA_Cr_EN, Cr channel sepia effect on/off, 1 : on, 0 : off SEPIA_Cb_EN, Cb channel sepia effect on/off, 1 : on, 0 : off
<1.06h>	E0h	**SEPIA_Cr**	R/W	[7:0]	When Cr channel sepia effect on, Cr channel value
<1.07h>	20h	**SEPIA_Cb**	R/W	[7:0]	When Cb channel sepia effect on, Cb channel value
<1.08h>	04h	**YGAIN_H**	R/W	[7:4] [3:0]	Reserved Luminance Level Gain (×0 ~ ×4) [11:8]
<1.09h>	00h	**YGAIN_L**	R/W	[7:0]	Luminance Level Gain (×0 ~ ×4) [7:0] [11:10] : integer part, [9:0] : fraction part xN : N * 512 (decimal value) → Y (hexa value) ex) x2 : 2 * 512 → 400h
<1.0Ah>	04h	**CGAIN_H**	R/W	[7:4] [3:0]	Reserved Color Level Gain (X0 ~ X4) [11:8]
<1.0Bh>	A0h	**CGAIN_L**	R/W	[7:0]	Color Level Gain (X0 ~ X4) [7:0] [11:10] : integer part, [9:0] : fraction part xN : N * 512 (decimal value) → Y (hexa value) ex) x2 : 2 * 512 → 400h
<1.0Ch>	00h	**FORMAT_CMD**	R/W	[7] [6] [5] [4] [3] [2] [1] [0]	Reserved CIS Direct Output Vertical Output Sync Inversion Horizontal Output Sync Inversion UV Output Selection 0 : Cb/Cr Output 1 : UV Output HSO, CBLK Output Selection 0 : CBLK Output 1 : HSO Output Full YC Output On/Off SCK656 Inversion
<1.0Dh>	08h	**CRCB_AH**	R/W	[7 :4] [3:0]	Reserved CrCb Coefficient for RGB (a) (0≤CRCB_A≤2) [11:8]
<1.0Eh>	00h	**CRCB_AL**	R/W	[7:0]	CrCb Coefficient for RGB (a) (0≤CRCB_A≤2) [7:0]
<1.0Fh>	0Ah	**CRCB_BH**	R/W	[7:4] [3:0]	Reserved CrCb Coefficient for RGB (b) (0≤CRCB_A≤2) [11:8]
<1.10h>	F8h	**CRCB_BL**	R/W	[7:0]	CrCb Coefficient for RGB (b) (0≤CRCB_A≤2) [7:0]
<1.11h>	05h	**CRCB_CH**	R/W	[7:4] [3:0]	Reserved CrCb Coefficient for RGB (c) (0≤CRCB_A≤1) [11:8]
<1.12h>	60h	**CRCB_CL**	R/W	[7:0]	CrCb Coefficient for RGB (c) (0≤CRCB_A≤2) [7:0]
<1.13h>	0Bh	**CRCB_DH**	R/W	[7:4] [3:0]	Reserved CrCb Coefficient for RGB (d) (0≤CRCB_A≤1) [11:8]
<1.14h>	2Bh	**CRCB_DL**	R/W	[7:0]	CrCb Coefficient for RGB (d) (0≤CRCB_A≤2) [7:0]
<1.15h>	0Dh	**CRCB_EH**	R/W	[7:4] [3:0]	Reserved CrCb Coefficient for RGB (e) (0≤CRCB_A≤1) [11:8]
<1.16h>	DBh	**CRCB_EL**	R/W	[7:0]	CrCb Coefficient for RGB (e) (0≤CRCB_A≤2) [7:0]

Addr	Reset Value	Mnemonic	RW	Bits	Descriptions
<1.17h>	00h	**FLK_LOGSEL**	R/W	[7:3] [2] [1] [0]	Reserved FZONE_R Ysample_R, 0: Every 2 lines 1: Every 4 lines SEL_R, 0 : New Algorithm 1 : Old Algorithm
<1.18h>	08h	**FLK_LGAIN1**	R/W	[7:0]	GY1_R[7:0] Logarithm Compensation Coefficient 1 (8BIT Output value about 23 Input)
<1.19h>	10h	**FLK_LGAIN2**	R/W	[7:0]	GY2_R[7:0] Logarithm Compensation Coefficient 1 (8BIT Output value about 24 Input)
<1.1Ah>	20h	**FLK_LGAIN3**	R/W	[7:0]	GY3_R[7:0] Logarithm Compensation Coefficient 1 (8BIT Output value about 25 Input)
<1.1Bh>	40h	**FLK_LGAIN4**	R/W	[7:0]	GY4_R[7:0] Logarithm Compensation Coefficient 1 (8BIT Output value about 26 Input)
<1.1Ch>	80h	**FLK_LGAIN5**	R/W	[7:0]	GY5_R[7:0] Logarithm Compensation Coefficient 1 (8BIT Output value about 27 Input)
<1.1Dh>	FFh	**FLK_LGAIN6**	R/W	[7:0]	GY6_R[7:0] Logarithm Compensation Coefficient 1 (8BIT Output value about 28 Input)
<1.1Eh>	50h	**FLK_HSTART**	R/W	[7:0]	FLK_HSTART_R[7:0]
<1.1Fh>	05h	**FLK_HWIDTH_H**	R/W	[7:5] [4:0]	Reserved HWIDTH_R[12:8]
<1.20h>	A3h	**FLK_HWIDTH_L**	R/W	[7:0]	HWIDTH_R[7:0]
<1.21h>	01h	**FLK_VSTART_H**	R/W	[7:3] [2:0]	Reserved VSTART_R[10:8]
<1.22h>	5Ah	**FLK_VSTART_L**	R/W	[7:0]	VSTART_R[7:0]
<1.23h>	10h	**FLK_VHEIGHT**	R/W	[7:0]	VHEIGHT_R[7:0]
<1.24h>	00h	**PCOMMAND1**	R/W	[7] [6:5] [4:3] [2] [1] [0]	Reserved For Delay Adjustment when the Horizontal Mirror Mode of CIS 00 : Default 01 : Default 10 : AD_DELAY 10 11 : AD_DELAY 00 AD clock delay selection 00 : 1CLK, 01 : 2CLK, 10 : 3CLK, 11 : 4CLK Reserved Defect test pattern generation enable signal 0 : Defect test pattern OFF1 : Defect test pattern ON Reserved
<1.25h>	00h	**POFFSET**	R/W	[7:0]	When Operating Digital Clamp, Compensation Offset Value in Range of -128 ~ +127Enable to Operate Regardless of Digital Clamp
<1.26h>	01h	**CLP_H_START**	R/W	[7:0]	Horizontal Start Point in Optical Black or CIS (x1)
<1.27h>	01h	**CLP_V_START**	R/W	[7:0]	Vertical Start Point in Optical Black or CIS (x2)
<1.28h>	02h	**PTHRESH_H**	R/W	[7:2] [1] [0]	Reserved If Bayer pattern is R 1st -> 1, Gr 1st -> 1, B 1st -> 0, Gb 1st -> 0 If Bayer pattern is R 1st -> 0, Gr 1st -> 1, B 1st -> 1, Gb 1st -> 0
<1.29h>	02h	**CIS_GAIN_H**	R/W	[7:4] [3:0]	Reserved CIS Input Global Level Gain[11:8] (x0~x8)

Addr	Reset Value	Mnemonic	RW	Bits	Descriptions
<1.2Ah>	00h	**CIS_GAIN_L**	R/W	[7:0]	CIS Input Global Level Gain[7:0] (x0~x8)
<1.2Bh>	02h	**CISGAIN_GR__H**	R/W	[7:4] [3:0]	Reserved CIS Input Gr Channel Level Gain[11:8] (x0~x8)
<1.2Ch>	00h	**CISGAIN_GR_L**	R/W	[7:0]	CIS Input Gr_Channel Level Gain[7:0] (x0~x8)
<1.2Dh>	02h	**CISGAIN_GB__H**	R/W	[7:4] [3:0]	Reserved CIS Input Gb Channel Level Gain[11:8] (x0~x8)
<1.2Eh>	00h	**CISGAIN_GB_L**	R/W	[7:0]	CIS Input Gb Channel Level Gain[7:0] (x0~x8)
<1.2Fh>	02h	**CISGAIN_R__H**	R/w	[7:4] [3:0]	Reserved CIS Input R Channel Level Gain[11:8] (x0~x8)
<1.30h>	00h	**CISGAIN_R_L**	R/W	[7:0]	CIS Input R Channel Level Gain[7:0] (x0~x8)
<1.31h>	02h	**CISGAIN_B__H**	R/W	[7:4] [3:0]	Reserved CIS Input B Channel Level Gain[11:8] (x0~x8)
<1.32h>	00h	**CISGAIN_B_L**	R/W	[7:0]	CIS Input B Channel Level Gain[7:0] (x0~x8)
<1.33h>	00h	**POFFSET_Gr**	R/W	[7:0]	CIS Input Gr Channel Offset (-128~127)
<1.34h>	00h	**POFFSET_Gb**	R/W	[7:0]	CIS Input Gb Channel Offset (-128~127)
<1.35h>	00h	**POFFSET_R**	R/W	[7:0]	CIS Input R Channel Offset (-128~127)
<1.36h>	00h	**POFFSET_B**	R/W	[7:0]	CIS Input B Channel Offset (-128~127)
<1.37h -3Ch>		**Reserved**			
<1.3Dh>	00h	**PATTERN**	R/W	[7:6] [5] [4] [3:2] [1:0]	Reserved BPR_PATTERN, R/B or G selection PBPR_ON, 0 : OFF, 1 : ON Reserved Internal Input Pattern Selection 00 : CIS output 01 : Color Bar Pattern 10 : Ramp Pattern 11 : Blue Screen Pattern
<1.3Eh>	78h	**BPR_TH_1L**	R/W	[7:0]	bpr_thr1[7:0] BPR Data Threshold for Difference of target pixel from around pixels.
<1.3Fh>	2Ch	**BPR_TH_3L**	R/W	[7:0]	bpr_thr3[7:0] BPR Data Threshold for Gradient
<1.40h>	01h	**BPR_TH_13H**	R/W	[7:4] [3:2] [1:0]	Reserved bpr_thr1[9:8] BPR Data Threshold for Difference of target pixel from around pixels. bpr_thr3[9:8], BPR Data Threshold for Gradient
<1.41h>	B4h	**BPR_TH_5L**	R/W	[7:0]	bpr_thr5[7:0] BPR Data Threshold for Edge (use with bpr_thr7)
<1.42h>	00h	**BPR_TH_5H**	R/W	[7:6] [5:0]	Reserved bpr_thr5[13:8] BPR Data Threshold for Edge (use with bpr_thr7)
<1.43h>	E8h	**BPR_TH_7L**	R/W	[7:0]	bpr_thr7[7:0] BPR Data Threshold for Edge (use with bpr_thr5)
<1.44h>	03h	**BPR_TH_7H**	R/W	[7:6] [5:0]	Reserved bpr_thr7[13:8] BPR Data Threshold for Edge (use with bpr_thr5)
<1.45h>	00h	**GRGB_CONT**	R/W	[7:4] [3] [2]	Reserved GrGb_Correction Enable for G-Channel GrGb_Correction Enable for R/B-Channel *** For R/B-Channel Correction, GRGB_ON must be on

Addr	Reset Value	Mnemonic	RW	Bits	Descriptions
				[1]	Reserved
				[0]	Reserved
<1.46h>	20h	**GRGB_GTHR**	R/W	[7:0]	GrGb_Correction Threshold for G-Channel
<1.47h>	10h	**GRGB_RBTHR**	R/W	[7:0]	GrGb_Correction Threshold for R/B-Channel
<1.48h>	0Ah	**SIGTHR_CONST**	R/W	[7:0]	Constant Value of Edge Detection for Noise Reduction [7:0] *** SigmaThreshod_01 = SIGTHR_CONST[9:0] + CurrentValue * SIGTHR01_MULT/32;
<1.49h>	15h	**SIGTHR_MULT**	R/W	[7:6]	Constant Value of Edge Detection for Noise Reduction [9:8]
				[5:4]	SIGTHR02_MULT, Multiplication Value of Edge Detection for Noise Reduction 00 : Sigma_Threshold_01 * 1.0; 01 : Sigma_Threshold_01 * 2.0; 10 : Sigma_Threshold_01 * 2.5; 11 : Sigma_Threshold_01 * 3.0;
				[3:0]	SIGTHR01_MULT, Multiplication Value of Edge Detection for Noise Reduction *** Multiplication_Value = SIGTHR01_MULT / 32;
<1.4Ah>	C8h	**PRETHR_CONST**	R/W	[7:0]	Constant Value of Noise Detection for Noise Reduction [7:0] *** Pre_Threshold = PRETHR_CONST[9:0] + CurrentValue * PRETHR_MULT/16;
<1.4Bh>	0Ah	**PRETHR_MULT**	R/W	[7:6]	Reserved
				[5:4]	Constant Value of Noise Detection for Noise Reduction [9:8]
				[3:0]	Multiplication Value of Noise Detection for Noise Reduction *** Multiplication_Value = PRETHR_MULT / 16;
<1.4Ch>	00h	**SIGFIL_CNTL**	R/W	[7:4]	Reserved
				[3]	RGB Linear Interpolation Enable *** If "1", Noise Reduction and Normal Interpolation will be off.
				[2]	Reserved
				[1]	Reserved
				[0]	Sigma Noise Filter Enable
<1.4Dh>	00h	**RCONTROL**	R/W	[7]	Reserved
				[6]	OFFSET_R[8], MSB [8] of R Channel Offset (-256 ~ 255)
				[5]	OFFSET_G[8], MSB [8] of G Channel Offset (-256 ~ 255)
				[4]	OFFSET_B[8], MSB [8] of B Channel Offset (-256 ~ 255)
				[3]	RV_CONT, Vertical Pixel Array Control of CIS 1 : (R/G/R/G or G/R/G/R) 0 : (G/B/G/B or B/G/B/G)
				[2]	RH_CONT, Horizontal Pixel Array Control of CIS 0 : SCK (R/G/R/G or G/B/G/B) 1 : ~SCK (G/R/G/R or B/G/B/G)
				[1]	sel_gam
				[0]	B/W CIS Mode Selection 0 : B/W CIS Mode input 1 : Color CIS Mode input
<1.4Eh>	C8h	**POSTTHR_CONST**	R/W	[7:0]	Constant Value of Noise Detection for Noise Reduction [7:0] *** Pre_Threshold = PRETHR_CONST[9:0] + CurrentValue * PRETHR_MULT/16;
<1.4Fh>	0Ah	**POSTTHR_MULT**	R/W	[5:4]	Constant Value of Noise Detection for Noise Reduction [9:8]
				[3:0]	Multiplication Value of Noise Detection for Noise Reduction. *** Multiplication_Value = PRETHR_MULT / 16;
<1.50h>	00h	**Reserved**			

Addr	Reset Value	Mnemonic	RW	Bits	Descriptions
<1.51h>	04h	**RRR_GAINH**	R/W	[7:4] [3:0]	Reserved RRR_GAIN[11:8] R Signal Gain for Color Correction of R Signal (x0 ~ x4)
<1.52h>	00h	**RRR_GAINL**	R/W	[7:0]	RRR_GAIN[7:0] R Signal Gain for Color Correction of R Signal (x0 ~ x4) [11:10] : integer part, [9:0] : fraction part xN : N * 512 (decimal value) → Y (hexa value) ex) x2 : 2 * 512 → 400h
<1.53h>	00h	**RRG_GAINH**	R/W	[7:4] [3:0]	Reserved RRG_GAIN[11:8] G Signal Gain for Color Correction of R Signal (x-2 ~ x2)
<1.54h>	00h	**RRG_GAINL**	R/W	[7:0]	RRG_GAIN[7:0] G Signal Gain for Color Correction of R Signal (x-2 ~ x2) [11] : Sign bit, [10] : integer part, [9:0] : fraction part ex) x-2 : - 2 * 512 (decimal value) → 400h (100 0000 0000b)
<1.55h>	00h	**RRB_GAINH**	R/W	[7:4] [3:0]	Reserved RRB_GAIN[11:8] B Signal Gain for Color Correction of R Signal (x-2 ~ x2)
<1.56h>	00h	**RRB_GAINL**	R/W	[7:0]	RRB_GAIN[7:0] B Signal Gain for Color Correction of R Signal (x-2 ~ x2) [11] : Sign bit, [10] : integer part, [9:0] : fraction part ex) x-2 : - 2 * 512 (decimal value) → 400h (100 0000 0000b)
<1.57h>	00h	**RGR_GAINH**	R/W	[7:4] [3:0]	Reserved RGR_GAIN[11:8] R Signal Gain for Color Correction of G Signal (x-2 ~ x2)
<1.58h>	00h	**RGR_GAINL**	R/W	[7:0]	RGR_GAIN[7:0] R Signal Gain for Color Correction of G Signal (x-2 ~ x2) [11] : Sign bit, [10] : integer part, [9:0] : fraction part ex) x-2 : - 2 * 512 (decimal value) → 400h (100 0000 0000b)
<1.59h>	04h	**RGG_GAINH**	R/W	[7:4] [3:0]	Reserved RGG_GAIN[11:8] G Signal Gain for Color Correction of G Signal (x0 ~ x4)
<1.5Ah>	00h	**RGG_GAINL**	R/W	[7:0]	RGG_GAIN[7:0] G Signal Gain for Color Correction of G Signal (x0 ~ x4) [11:10] : integer part, [9:0] : fraction part xN : N * 512 (decimal value) → Y (hexa value) ex) x2 : 2 * 512 → 400h
<1.5Bh>	00h	**RGB_GAINH**	R/W	[7:4] [3:0]	Reserved RGB_GAIN[11:8] B Signal Gain for Color Correction of G Signal (x-2 ~ x2)
<1.5Ch>	00h	**RGB_GAINL**	R/W	[7:0]	RGB_GAIN[7:0] B Signal Gain for Color Correction of G Signal (x-2 ~ x2) [11] : Sign bit, [10] : integer part, [9:0] : fraction part ex) x-2 : - 2 * 512 (decimal value) → 400h (100 0000 0000b)
<1.5Dh>	00h	**RBR_GAINH**	R/W	[7:4] [3:0]	Reserved RBR_GAIN[11:8]

Addr	Reset Value	Mnemonic	RW	Bits	Descriptions
					R Signal Gain for Color Correction of B Signal (x-2 ~ x2)
<1.5Eh>	00h	**RBR_GAINL**	R/W	[7:0]	RBR_GAIN[7:0] R Signal Gain for Color Correction of B Signal (x-2 ~ x2) [11] : Sign bit, [10] : integer part, [9:0] : fraction part ex) x-2 : - 2 * 512 (decimal value) → 400h (100 0000 0000b)
<1.5Fh>	00h	**RBG_GAINH**	R/W	[7:4] [3:0]	Reserved RBG_GAIN[11:8] G Signal Gain for Color Correction of B Signal (x-2 ~ x2)
<1.60h>	00h	**RBG_GAINL**	R/W	[7:0]	RBG_GAIN[7:0] G Signal Gain for Color Correction of B Signal (x-2 ~ x2) [11] : Sign bit, [10] : integer part, [9:0] : fraction part ex) x-2 : - 2 * 512 (decimal value) → 400h (100 0000 0000b)
<1.61h>	04h	**RBB_GAINH**	R/W	[7:4] [3:0]	Reserved RBB_GAIN[11:8] B Signal Gain for Color Correction of B Signal (x0 ~ x4)
<1.62h>	00h	**RBB_GAINL**	R/W	[7:0]	RBB_GAIN[7:0] B Signal Gain for Color Correction of B Signal (x0 ~ x4) [11:10] : integer part, [9:0] : fraction part xN : N * 512 (decimal value) → Y (hexa value) ex) x2 : 2 * 512 → 400h
<1.63h>	02h	**GAIN_R_H**	R/W	[7:4] [3:0]	Reserved R Channel Level gain [11:8] (X0 ~ X8)
<1.64h>	00h	**GAIN_R_L**	R/W	[7:0]	R Channel Level gain [7:0] (X0 ~ X8) [11:9] : integer part, [8:0] : fraction part xN : N * 256 (decimal value) → Y (hexa value) ex) x2 : 2 * 256 → 200h
<1.65h>	02h	**GAIN_G_H**	R/W	[7:4] [3:0]	Reserved G Channel Level gain [11:8] (X0 ~ X8)
<1.66h>	00h	**GAIN_G_L**	R/W	[7:0]	G Channel Level gain [7:0] (X0 ~ X8) [11:9] : integer part, [8:0] : fraction part xN : N * 256 (decimal value) → Y (hexa value) ex) x2 : 2 * 256 → 200h
<1.67h>	02h	**GAIN_B_H**	R/W	[7:4] [3:0]	Reserved B Channel Level gain [11:8] (X0 ~ X8)
<1.68h>	00h	**GAIN_B_L**	R/W	[7:0]	B Channel Level gain [7:0] (X0 ~ X8) [11:9] : integer part, [8:0] : fraction part xN : N * 256 (decimal value) → Y (hexa value) ex) x2 : 2 * 256 → 200h
<1.69h>	00h	**OFFSET_R**	R/W	[7:0]	LSB [7:0] of R Channel Offset (-256 ~ 255)
<1.6Ah>	00h	**OFFSET_G**	R/W	[7:0]	LSB [7:0] of G Channel Offset (-256 ~ 255)
<1.6Bh>	00h	**OFFSET_B**	R/W	[7:0]	LSB [7:0] of B Channel Offset (-256 ~ 255)
<1.6Ch -B6h>	00h	**Reserved**			
<1.B7h>	00h	**OAE_WH_START[15:8]**	R/W	[7:0]	OAEHS_H, AE window Horizontal start point high

Addr	Reset Value	Mnemonic	RW	Bits	Descriptions
<1.B8h>	0Ah	**OAE_WH_START[7:0]**	R/W	[7:0]	OAEHS_L, AE window Horizontal start point low
<1.B9h>	00h	**OAE_WH_WIDTH[15:8]**	R/W	[7:0]	OAEHE_H, AE window Horizontal Width high
<1.BAh>	C6h	**OAE_WH_WIDTH[7:0]**	R/W	[7:0]	OAEHE_L, AE window Horizontal Width low
<1.BBh>	00h	**OAE_WV_START[15:8]**	R/W	[7:0]	OAEVS_H, AE window Vertical start point high
<1.BCh>	18h	**OAE_WV_START[7:0]**	R/W	[7:0]	OAEVS_L, AE window Vertical start point low
<1.BDh>	00h	**OAE_WV_WIDTH[15:8]**	R/W	[7:0]	OAEVE_H, AE window Vertical start point high
<1.BEh>	C0h	**OAE_WV_WIDTH[7:0]**	R/W	[7:0]	OAEVE_L, AE window Vertical start point low
<1.BFh>	0Ah	**OAE_PEAK_THR**	R/W	[7:0]	AE Y Peak Threshold
<1.C0h>	00h	**OAWB_WH_START[15:8]**	R/W	[7:0]	AWB window Horizontal start point high
<1.C1h>	0Ah	**OAWB_WH_START[7:0]**	R/W	[7:0]	AWB window Horizontal start point low
<1.C2h>	00h	**OAWB_WH_WIDTH[15:8]**	R/W	[7:0]	AWB window Horizontal Width high
<1.C3h>	C6h	**OAWB_WH_WIDTH[7:0]**	R/W	[7:0]	AWB window Horizontal Width low
<1.C4h>	00h	**OAWB_WV_START[15:8]**	R/W	[7:0]	AWB window Vertical start point high
<1.C5h>	18h	**OAWB_WV_START[7:0]**	R/W	[7:0]	AWB window Vertical start point low
<1.C6h>	00h	**OAWB_WV_HEIGHT[15:8]**	R/W	[7:0]	AWB window Vertical Height high
<1.C7h>	8Fh	**OAWB_WV_HEIGHT[7:0]**	R/W	[7:0]	AWB window Vertical Height low
<1.C8h>	FFh	**OYH_AWB**	R/W	[7:0]	For AWB, High Threshold Value of Y signal(0~255)
<1.C9h>	10h	**OYL_AWB**	R/W	[7:0]	For AWB, Low Threshold Value of Y signal(0~255)
<1.CAh>	48h	**OY_TH_AWB**	R/W	[7:0]	For AWB Threshold Value of Y signal (0~255)
<1.CBh>	FFh	**AWB_WIN_SEL1**	R/W	[7:0]	AWB window selection (w1~w8)
<1.CCh>	FFh	**AWB_WIN_SEL2**	R/W	[7:0]	AWB window selection (w9~w16)
<1.CDh>	FFh	**AWB_WIN_SEL3**	R/W	[7:0]	AWB window selection (w17~w24)
<1.CEh>	FFh	**AWB_WIN_SEL4**	R/W	[7:0]	AWB window selection (w25~w32)
<1.CFh>	FFh	**AWB_WIN_SEL5**	R/W	[7:0]	AWB window selection (w33~w408)
<1.D0h>	FFh	**AWB_WIN_SEL6**	R/W	[7:0]	AWB window selection (w41~w48)
<1.D1h>	FFh	**AWB_WIN_SEL7**	R/W	[7:0]	AWB window selection (w49~w56)
<1.D2h>	FFh	**AWB_WIN_SEL8**	R/W	[7:0]	AWB window selection (w57~w64)
<1.D3h>	FFh	**AWB_R_NOR_MAXH**	R/W	[7:0]	AWB2 Normalized R maximum High Value, integer : 0bit, fractional : 8bit
<1.D4h>	FFh	**AWB_R_NOR_MAXL**	R/W	[7:0]	AWB2 Normalized R maximum Low Value, integer : 0bit, fractional : 8bit
<1.D5h>	00h	**AWB_R_NOR_MINH**	R/W	[7:0]	AWB2 Normalized R minimum High Value, integer : 0bit, fractional : 8bit
<1.D6h>	00h	**AWB_R_NOR_MINL**	R/W	[7:0]	AWB2 Normalized R minimum Low Value, integer : 0bit, fractional : 8bit
<1.D7h>	FFh	**AWB_B_NOR_MAXH**	R/W	[7:0]	AWB2 Normalized B maximum High Value, integer : 0bit, fractional : 8bit
<1.D8h>	FFh	**AWB_B_NOR_MAXL**	R/W	[7:0]	AWB2 Normalized B maximum Low Value, integer : 0bit, fractional : 8bit
<1.D9h>	00h	**AWB_B_NOR_MINH**	R/W	[7:0]	AWB2 Normalized B minimum High Value, integer : 0bit, fractional : 8bit
<1.DAh>	00h	**AWB_B_NOR_MINL**	R/W	[7:0]	AWB2 Normalized B minimum Low Value, integer : 0bit, fractional : 8bit
<1.DBh>	FFh	**AWB_NOR_CONST_1H**	R/W	[7:0]	Constant of AWB straight line 1, integer : 4bit, fractional : 12bit
<1.DCh>	FFh	**AWB_NOR_CONST_1L**	R/W	[7:0]	Constant of AWB straight line 1
<1.DDh>	FFh	**AWB_NOR_CONST_2H**	R/W	[7:0]	Constant of AWB straight line 2, integer : 4bit, fractional : 12bit

Addr	Reset Value	Mnemonic	RW	Bits	Descriptions
<1.DEh>	FFh	**AWB_NOR_CONST_2L**	R/W	[7:0]	Constant of AWB straight line 2
<1.DFh>	00h	**AWB_NOR_CONST_3H**	R/W	[7:0]	Constant of AWB straight line 3, integer : 4bit, fractional : 12bit
<1.E0h>	00h	**AWB_NOR_CONST_3L**	R/W	[7:0]	Constant of AWB straight line 3
<1.E1h>	00h	**AWB_NOR_CONST_4H**	R/W	[7:0]	Constant of AWB straight line 4, integer : 4bit, fractional : 12bit
<1.E2h>	00h	**AWB_NOR_CONST_4L**	R/W	[7:0]	Constant of AWB straight line 4
<1.E3h>	01h	**AWB_R_COEF1**	R/W	[7:0]	AWB2 R Gradient Value1, [7:4] : integer part, [3:0] : fractional part N : N * 16 (decimal value) → Y (hexa value) ex) 3 : 3 * 16 → 30h
<1.E4h>	01h	**AWB_R_COEF2**	R/W	[7:0]	AWB2 R Gradient Value2, [7:4] : integer part, [3:0] : fractional part N : N * 16 (decimal value) → Y (hexa value) ex) 3 : 3 * 16 → 30h
<1.E5h>	01h	**AWB_R_COEF3**	R/W	[7:0]	AWB2 R Gradient Value3, [7:4] : integer part, [3:0] : fractional part N : N * 16 (decimal value) → Y (hexa value) ex) 3 : 3 * 16 → 30h
<1.E6h>	01h	**AWB_R_COEF4**	R/W	[7:0]	AWB2 R Gradient Value4, [7:4] : integer part, [3:0] : fractional part N : N * 16 (decimal value) → Y (hexa value) ex) 3 : 3 * 16 → 30h
<1.E7h>	01h	**AWB_B_COEF1**	R/W	[7:0]	AWB2 B Gradient Value1, [7:4] : integer part, [3:0] : fractional part N : N * 16 (decimal value) → Y (hexa value) ex) 3 : 3 * 16 → 30h
<1.E8h>	01h	**AWB_B_COEF2**	R/W	[7:0]	AWB2 B Gradient Value2, [7:4] : integer part, [3:0] : fractional part N : N * 16 (decimal value) → Y (hexa value) ex) 3 : 3 * 16 → 30h
<1.E9h>	01h	**AWB_B_COEF3**	R/W	[7:0]	AWB2 B Gradient Value3, [7:4] : integer part, [3:0] : fractional part N : N * 16 (decimal value) → Y (hexa value) ex) 3 : 3 * 16 → 30h
<1.EAh>	01h	**AWB_B_COEF4**	R/W	[7:0]	AWB2 B Gradient Value4, [7:4] : integer part, [3:0] : fractional part N : N * 16 (decimal value) → Y (hexa value) ex) 3 : 3 * 16 → 30h
<1.EBh>	01h	**AWB_COEF_MAX**	R/W	[7:2] [1] [0]	Reserved AWB Coef Up Maximum AWB Coef Down Maximum

3. CIS REGISTER MAP (PAGE 02H)

Addr	Reset Value	Mnemonic	Attr	Bits	Descriptions
<2.00h>	00h	**Reserved**			Reserved
<2.01h>	00h	**Reserved**			Reserved
<2.02h>	0Eh	**NORMAL_BPR_ON** **Reserved** **DCLK_DIV** **SHUT_CTRL** **ADC_RES**	R/W	[7] [6] [5:3] [2] [1:0]	BPR control without EFUSE ROM (0:OFF, 1:ON) Reserved main clock divider (000:1/1, 001:1/2, 010:1/4, 011:1/8, 100 : 1/16) E-shutter operation control output data bit selection (00: 8bits, 01: 9bits, 10: 10bits)
<2.03h>	00h	**Reserved** **ROW_ID_INV** **SCK_ID_INV** **PWR_SAVE** **AVE_SUB_SMP_EN** **V_FLIP** **H_MIRR** **Reserved**	R/W	[7] [6] [5] [4] [3] [2] [1] [0]	Reserved line channel inversion (0:normal, 1:inversion) column channel inversion (0:normal, 1:inversion) power_save mode (0: off 1: on) 1: save mode on, APS off 0: save mode off, APS on average sub-sampling op. control (0:off, 1:on) vertical Flip operation control (0:normal, 1:flip) horizontal mirror operation reserved
<2.04h>	06h	**FRAME_H_WIDTH_UP**	R/W	[7:0]	total frame horizontal width (default = 1760d)
<2.05h>	E0h	**FRAME_H_WIDTH_DN**	R/W	[7:0]	total frame horizontal width (default = 1760d)
<2.06h>	04h	**FRAME_V_DEPTH_UP**	R/W	[7:0]	total frame vertical depth (default = 1212d)
<2.07h>	BCh	**FRAME_V_DEPTH_DN**	R/W	[7:0]	total frame vertical depth (default = 1212d)
<2.08h>	06h	**H_OUTPUT_WIDTH_UP**	R/W	[7:4] [3:0]	reserved WOI horizontal width (default = 1604d)
<2.09h>	44h	**H_OUTPUT_WIDTH_DN**	R/W	[7:0]	WOI horizontal width (default = 1604d)
<2.0Ah>	04h	**reserved** **V_OUTPUT_DEPTH_UP**	R/W	[7:4] [3:0]	reserved WOI vertical depth (default = 1204d)
<2.0Bh>	B4h	**V_OUTPUT_DEPTH_DN**	R/W	[7:0]	WOI vertical depth (default = 1204d)
<2.0Ch>	00h	**reserved** **H_ADDR_START_UP**	R/W	[7:4] [3:0]	reserved WOI horizontal start address (default = 12d)
<2.0Dh>	00h	**H_ADDR_START_DN**		[7:0]	WOI horizontal start address (default = 12d)
<2.0Eh>	06h	**reserved** **H_ADDR_END_UP**	R/W	[7:4] [3:0]	Reserved WOI horizontal end address (default = 1615d)
<2.0Fh>	4Fh	**H_ADDR_END_DN**	R/W	[7:0]	WOI horizontal end address (default = 1615d)
<2.10h>	00h	**reserved** **V_ADDR_START_UP**	R/W	[7:4] [3:0]	reserved WOI vertical start address (default = 22d)
<2.11h>	00h	**V_ADDR_START_DN**	R/W	[7:0]	WOI vertical start address (default = 22d)
<2.12h>	04h	**reserved** **V_ADDR_END_UP**	R/W	[7:4] [3:0]	reserved WOI vertical end address (default = 1225d)
<2.13h>	BFh	**V_ADDR_END_DN**	R/W	[7:0]	WOI vertical end address (default = 1225d)
<2.14h>	00h	**reserved** **H_EVEN_INC_UP**	R/W	[7:4] [3:0]	reserved horizontal even address increment

Addr	Reset Value	Mnemonic	Attr	Bits	Descriptions
<2.15h>	01h	**H_EVEN_INC_DN**	R/W	[7:0]	horizontal even address increment
<2.16h>	00h	**reserved** **H_ODD_INC_UP**	R/W	[7:4] [3:0]	reserved horizontal odd address increment
<2.17h>	01h	**H_ODD_INC_DN**	R/W	[7:0]	horizontal odd address increment
<2.18h>	00h	**reserved** **V_EVEN_INC_UP**	R/W	[7:4] [3:0]	reserved vertical even address increment
<2.19h>	01h	**V_EVEN_INC_DN**	R/W	[7:0]	vertical even address increment
<2.1Ah>	00h	**reserved** **V_ODD_INC_UP**	R/W	[7:4] [3:0]	reserved vertical odd address increment
<2.1Bh>	01h	**V_ODD_INC_DN**	R/W	[7:0]	vertical odd address increment
<2.1Ch>	00h	**Reserved**			Reserved
<2.1Dh>	08h	**Reserved**			Reserved
<2.1Eh>	00h	**VS_POSTC_UP**	R/W	[7:0]	compensating Frame rate in zooming mode, column step
<2.1Fh>	00h	**VS_POSTC_DN**	R/W	[7:0]	compensating Frame rate in zooming mode, column step
<2.20h>	04h	**LINE_INT_TIME_UP**	R/W	[7:0]	line step integration time
<2.21h>	24h	**LINE_INT_TIME_DN**	R/W	[7:0]	default = 606d
<2.22h>	03h	**COL_INT_TIME_UP**	R/W	[7:0]	column step integration time
<2.23h>	A5h	**COL_INT_TIME_DN**	R/W	[7:0]	default = 0d
<2.24h>	A0h	**VS_INV** **VS_DISPLAY** **HS_INV** **HS_DISPLAY** **Reserved** **BULB_MODE** **Reserved** **SFCM_MODE**	R/W	[7] [6] [5] [4] [3] [2] [1] [0]	vertical sync. polarity inversion (0:normal, 1:inversion) vertical sync. high when data valid period (0:normal, 1:valid) horizontal sync. polarity inversion (0:normal, 1:inversion) horizontal sync. high when data valid period (0:normal, 1:valid) Reserved Bulb mode (1:on, 0:off) Reserved single frame capture mode (1:on, 0:off)
<2.25h>	00h	**VS_START_UP**	R/W	[7:0]	vertical sync start position
<2.26h>	00h	**VS_START_DN**	R/W	[7:0]	vertical sync start position
<2.27h>	00h	**VS_WIDTH_UP**	R/W	[7:0]	vertical sync width
<2.28h>	01h	**VS_WIDTH_DN**	R/W	[7:0]	vertical sync width
<2.29h>	00h	**HS_START_UP**	R/W	[7:0]	horizontal sync start position
<2.2Ah>	00h	**HS_START_DN**	R/W	[7:0]	horizontal sync start position
<2.2Bh>	00h	**HS_WIDTH_UP**	R/W	[7:0]	horizontal sync width
<2.2Ch>	20h	**HS_WIDTH_DN**	R/W	[7:0]	horizontal sync width
<2.2Dh>	48h	**D_SHUT_CTRL**	R/W	[7:4] [3] [2:0]	double shutter width control double shutter enable Reserved
<2.2Eh>	80h	**OFFSET_CTRL_REFERENCE**	R/W	[7:0]	analog Reference offset control (default = 80h)
<2.2Fh>	80h	**OFFSET_R_CTRL**	R/W	[7:0]	analog R-channel offset control (default = 80h)
<2.30h>	80h	**OFFSET_GR_CTRL**	R/W	[7:0]	analog GR-channel offset control (default = 80h)
<2.31h>	80h	**OFFSET_GB_CTRL**	R/W	[7:0]	analog GB-channel offset control (default = 80h)

Addr	Reset Value	Mnemonic	Attr	Bits	Descriptions
<2.32h>	80h	**OFFSET_B_CTRL**	R/W	[7:0]	analog B-channel offset control (default = 80h)
<2.33h>	00h	**Reserved** **ANALOG_R_GAIN_CTRL**	R/W	[7] [6:0]	Reserved analog R-channel gain control register (default = 0(1X))
<2.34h>	14h	**Reserved** **ANALOG_GR_GAIN_CTRL**	R/W	[7] [6:0]	Reserved analog GR-channel gain control register (default = 0(1X))
<2.35h>	00h	**Reserved** **ANALOG_GB_GAIN_CTRL**	R/W	[7] [6:0]	Reserved analog GB-channel gain control register (default = 0(1X))
<2.36h>	00h	**Reserved** **ANALOG_B_GAIN_CTRL**	R/W	[7] [6:0]	Reserved analog B-channel gain control register (default = 0(1X))
<2.37h>	31h	**Reserved** **GLB_CTRL_ALL**	R/W	[7:6] [5:0]	Reserved global gain all channel control (default = 18h)
<2.38h>	31h	**Reserved** **GLB_CTRL_SEC1**	R/W	[7:6] [5:0]	Reserved global gain R-channel control (default = 18h)
<2.39h>	31h	**Reserved** **GLB_CTRL_SEC2**	R/W	[7:6] [5:0]	Reserved global gain GR-channel control (default = 18h)
<2.3Ah>	31h	**Reserved** **GLB_CTRL_SEC3**	R/W	[7:6] [5:0]	Reserved global gain GB-channel control (default = 18h)
<2.3Bh>	31h	**Reserved** **GLB_CTRL_SEC4**	R/W	[7:6] [5:0]	Reserved global gain B-channel control (default = 18h)
<2.3Ch>	00h	**NORMAL_BPR_THRESH**	R/W	[7:0]	Normal BPR Threshould
<2.3Dh>	26h	**Reserved**	R/W	[7:0]]	reserved
<2.3Eh>	00h	**Reserved**	R/W	[7:0]	Reserved
<2.3Fh>	00h	**Reserved**	R/W	[7:0]	Reserved
<2.40h>	00h	**HOLDLINE_UP**	R/W	[7:0]	data output time delay
<2.41h>	00h	**HOLDLINE_DN**	R/W	[7:0]	data output time delay
<2.42h -4Dh>		**Reserved**			Reserved
<2.4Eh>	09h	**Reserved** **SCL_PUEN** **SCL_SC1** **SCL_SC2** **SDA_PUEN** **SDA_SC1** **SDA_SC2**	R/W	[7:6] [5] [4] [3] [2] [1] [0]	Reserved SCL_PUEN : bi-directional pad pull up control (0:enable, 1:disable) SCL output driving strength control {SCL_SC1,SCL_SC2} => 11 : 8mA, 01 : 6mA, 10 : 4mA, 00 : 2mA SDA_PUEN : bi-directional pad pull up control (0:enable, 1:disable) SDA output driving strength control {SDA_SC1,SDA_SC2} => 11 : 8mA, 01 : 6mA, 10 : 4mA, 00 : 2mA
<2.4Fh>	5Ah	**PCLK_SC1** **PCLK_SC2** **YC_SC1** **YC_SC2** **AF_SC1**	R/W	[7] [6] [5] [4] [3]	PCLK output driving strength control {PCLK_sc1,PCLK_sc2} => 11 : 8mA, 01 : 6mA, 10 : 4mA, 00 : 2mA YC output driving strength control {YC_sc1,YC_sc2} => 11 : 8mA, 01 : 6mA, 10 : 4mA, 00 : 2mA AF output driving strength control {AF_sc1, AF_sc2}

Addr	Reset Value	Mnemonic	Attr	Bits	Descriptions
		AF_SC2		[2]	=> 11 : 8mA, 01 : 6mA, 10 : 4mA, 00 : 2mA
		ZM_SC1 **ZM_SC2**		[1] [0]	ZM output driving strength control {ZM_sc1, ZM_sc2} => 11 : 8mA, 01 : 6mA, 10 : 4mA, 00 : 2mA
<2.50h>	4Ah	**PLL_S** **PLL_P**	R/W	[7:6] [5:0]	Dividing-ratio of PLL Post scaler Dividing-ratio of PLL Pre-divider
<2.51h>	0Ah	**Reserved** **PLL_CPPD** **PLL_I** **Reserved**	R/W	[7:6] [5] [4:1] [0]	Reserved Charge pump off control Charge pump & V-I converter current control PLL_I[3:2] : Charge pump current control PLL_I[1:0] : V-I converter current control Reserved
<2.52h>	42h	**PLL_M**	R/W	[7:0]	PLL_M[7:0], Dividing-ratio of PLL Main divider
<2.53h>	88h	**PLL_LPF**	R/W	[7:0]	PLL loop filter coefficient control PLL_LPF[7:4] : Resistance control PLL_LPF[3:0] : Capacitance control
<2.54h>	00h	**V_TEST_MODE** **H_TEST_MODE** **DCLK_INV_CON** **Reserved** **LATCH_SEL_AON** **ATEG_SUBS_EN** **Reserved**	R/W	[7] [6] [5] [4] [3] [2] [1:0]	TG test mode 1. TG test mode 2. DCLK polarity control Reserved Databus latch control analog teg control in sub-sampling mode Reserved
<2.55h -69h>		**Reserved**			Reserved
<2.6Ah>	36h	**EFUSE_CUT**	R/W	[7] [6:4] [3:0]	Efuse Cut on Efuse reset time selection Efuse cut time selection
<2.6Bh>	00h	**EFUSE Read**	R/W	[7:5] [4] [3] [2:0]	Reserved Efuse read on Reserved Efuse Id Selection
<2.6Ch>	00h	**CHIP_ID_0**	R/W	[7:0]	Chip_id_0
<2.6Dh>	00h	**CHIP_ID_1**	R/W	[7:0]	Chip_id_1
<2.6Eh>	00h	**CHIP_ID_2**	R/W	[7:0]	Chip_id_2
<2.6Fh>	00h	**CHIP_ID_3**	R/W	[7:0]	Chip_id_3
<2.70h>	00h	**CHIP_ID_4**	R/W	[7:0]	Chip_id_4
<2.71h>	00h	**CHIP_ID_5**	R/W	[7:0]	Chip_id_5
<2.72h -79h>		**Reserved**			Reserved

4. IMAGE FORMAT(1) (PAGE 03H)

* Image Format Registers will be loaded to Target Registers (ISP and CIS registers) when performing Image Format command <0.02h> or <0.73h> or <0.74h>.

* Image Format Table Index = <0.02h>

TABLE 1. SUB-SAMPLING TABLE INDEX

Table Index <0.02h>	Page	Address	Table Name
0 (Table 0)	03h	00h~2Fh	UXGA
1 (Table 1)		30h~5Fh	SXGA
2 (Table 2)		60h~8Fh	VGA
3 (Table 3)		90h~BFh	QVGA
4 (Table 4)		C0h~EFh	QQVGA
5 (Table 5)	04h	00h~2Fh	CIF
6 (Table 6)		30h~5Fh	QCIF
7 (Table 7)		60h~8Fh	H = 2, V = 1
8 (Table 8)		90h~BFh	H = 1, V =2
9 (Table 9)		C0h~EFh	H = 2, V = 2
10 (Table 10)	14h	00h~2Fh	H = 4, V = 1
11 (Table11)		30h~5Fh	H = 4, V = 4
12 (Table 12)		60h~8Fh	Reserved

Table 2. Detailed register Table of Table 1 – Page 03h (Attribute of all these values is R/W)

Addr [4:0]	Target Register	Bits	Descriptions	Table Index 0	Table Index 1	Table Index 2	Table Index 3	Table Index 4
00h	<2.04h>	[7:0]	**CIS_FRAME_H_WIDTH_H**	06h	06h	06h	06h	06h
01h	<2.05h>	[7:0]	**CIS_FRAME_H_WIDTH_L**	E2h	E2h	E2h	E2h	E2h
02h	<2.06h>	[7:0]	**CIS_FRAME_V_DEPTH_H**	04h	04h	04h	04h	04h
03h	<2.07h>	[7:0]	**CIS_FRAME_V_DEPTH_L**	BCh	BCh	BCh	BCh	BEh
04h	<2.08h>	[7:0]	**CIS_OUTPUT_H_WIDTH_H**	06h	06h	06h	06h	06h
05h	<2.09h>	[7:0]	**CIS_OUTPUT_H_WIDTH_L**	46h	46h	46h	46h	46h
06h	<2.0Ah>	[7:0]	**CIS_OUTPUT_V_DEPTH_H**	04h	04h	04h	04h	04h
07h	<2.0Bh>	[7:0]	**CIS_OUTPUT_V_DEPTH_L**	B4h	B4h	B4h	B4h	B4h
08h	<2.15h>	[7:0]	**CIS_H_EVEN_INC_L**	01h	01h	01h	01h	01h
09h	<2.17h>	[7:0]	**CIS_H_ODD_INC_L**	01h	01h	01h	01h	01h
0Ah	<2.19h>	[7:0]	**CIS_V_EVEN_INC_L**	01h	01h	01h	01h	01h
0Bh	<2.1Bh>	[7:0]	**CIS_V_ODD_INC_L**	01h	01h	01h	01h	01h
0Ch	<2.03h>[3]	[7:0]	**CIS_MIRR_ETC(Average sub)**	00h	00h	00h	00h	00h
0Dh	<5.6Eh>	[7:0]	**DSP5_POST_HSTART_H**	00h	00h	00h	00h	00h
0Eh	<5.6Fh>	[7:0]	**DSP5_POST_HSTART_L**	04h	04h	04h	04h	04h
0Fh	<5.70h>	[7:0]	**DSP5_POST_HWIDTH_H**	06h	06h	06h	06h	06h
10h	<5.71h>	[7:0]	**DSP5_POST_HWIDTH_L**	40h	40h	40h	40h	40h

Addr [4:0]	Target Register	Bits	Descriptions	Table Index 0	Table Index 1	Table Index 2	Table Index 3	Table Index 4
11h	<5.72h>	[7:0]	**DSP5_POST_VSTART_H**	00h	00h	00h	00h	00h
12h	<5.73h>	[7:0]	**DSP5_POST_VSTART_L**	02h	02h	02h	02h	02h
13h	<5.74h>	[7:0]	**DSP5_POST_VHEIGHT_H**	04h	04h	04h	04h	04h
14h	<5.75h>	[7:0]	**DSP5_POST_VHEIGHT_L**	B0h	B0h	B0h	B0h	B0h
15h	<5.7Ah>	[7:0]	**DSP5_IMG_HSIZEH**	06h	06h	06h	06h	06h
16h	<5.7Bh>	[7:0]	**DSP5_IMG_HSIZEL**	40h	40h	40h	40h	40h
17h	<5.7Ch>	[7:0]	**DSP5_IMG_VSIZEH**	04h	04h	04h	04h	04h
18h	<5.7Dh>	[7:0]	**DSP5_IMG_VSIZEL**	B0h	B0h	B0h	B0h	B0h
19h	<5.7Eh>	[7:0]	**DSP5_PSF**	00h	00h	22h	44h	88h
1Ah	<5.7Fh>	[7:0]	**DSP5_MSFX_H**	00h	40h	40h	40h	40h
1Bh	<5.80h>	[7:0]	**DSP5_MSFX_L**	00h	00h	00h	00h	00h
1Ch	<5.81h>	[7:0]	**DSP5_MSFY_H**	00h	2Ch	40h	40h	40h
1Dh	<5.82h>	[7:0]	**DSP5_MSFY_L**	00h	00h	00h	00h	00h
1Eh	<5.83h>	[7:0]	**DSP5_DW_HSIZEH**	06h	05h	02h	01h	00h
1Fh	<5.84h>	[7:0]	**DSP5_DW_HSIZEL**	40h	00h	80h	40h	A0h
20h	<5.85h>	[7:0]	**DSP5_DW_VSIZEH**	04h	04h	01h	00h	00h
21h	<5.86h>	[7:0]	**DSP5_DW_VSIZEL**	B0h	00h	E0h	F0h	78h
22h	<5.87h>	[7:0]	**DSP5_STARTXH**	00h	00h	00h	00h	00h
23h	<5.88h>	[7:0]	**DSP5_STARTXL**	00h	00h	00h	00h	00h
24h	<5.89h>	[7:0]	**DSP5_STARTYH**	00h	00h	00h	00h	00h
25h	<5.8Ah>	[7:0]	**DSP5_STARTYL**	00h	00h	00h	00h	00h
26h	<5.8Bh>	[7:0]	**DSP5_CLIP_HSIZEH**	06h	05h	02h	01h	00h
27h	<5.8Ch>	[7:0]	**DSP5_CLIP_HSIZEL**	40h	00h	80h	40h	A0h
28h	<5.8Dh>	[7:0]	**DSP5_CLIP_VSIZEH**	04h	04h	01h	00h	00h
29h	<5.8Eh>	[7:0]	**DSP5_CLIP_VSIZEL**	B0h	00h	E0h	F0h	78h
2Ah	<5.8Fh>	[7:0]	**DSP5_SEL_MAIN**	00h	00h	00h	00h	00h
2Bh	<5.90h>	[7:0]	**DSP5_HTERMH**	00h	00h	00h	00h	00h
2Ch	<5.91h>	[7:0]	**DSP5_HTERMM**	06h	08h	11h	22h	44h
2Dh	<5.92h>	[7:0]	**DSP5_HTERML**	E0h	12h	36h	6Ah	D4h
2Eh	<1.02h>	[7:0]	**DSP1_CRCB_SEL**	03h	03h	03h	03h	03h
2Fh	06h,15h, 1Ch Page	[7:0]	**OZONE, Boundary_INDEX**	00h	00h	00h	00h	00h

5. IMAGE FORMAT(2) (PAGE 04H)

* Image Format Registers will be loaded to Target Registers (ISP and CIS registers) when performing Image Format command <0.02h> or <0.73h> or <0.74h>.

* Image Format Table Index = <0.02h>

TABLE 1. SUB-SAMPLING TABLE INDEX

Table Index <0.02h>	Page	Address	Table Name
0 (Table 0)	03h	00h~2Fh	UXGA
1 (Table 1)		30h~5Fh	SXGA
2 (Table 2)		60h~8Fh	VGA
3 (Table 3)		90h~BFh	QVGA
4 (Table 4)		C0h~EFh	QQVGA
5 (Table 5)	04h	00h~2Fh	CIF
6 (Table 6)		30h~5Fh	QCIF
7 (Table 7)		60h~8Fh	H = 2, V = 1
8 (Table 8)		90h~BFh	H = 1, V =2
9 (Table 9)		C0h~EFh	H = 2, V = 2
10 (Table 10)	14h	00h~2Fh	H = 4, V = 1
11 (Table11)		30h~5Fh	H = 4, V = 4
12 (Table 12)		60h~8Fh	Reserved

Table 2. Detailed register Table of Table 1 - Page04h (Attribute of all these values is R/W)

Addr [4:0]	Target Register	Bits	Descriptions	Table Index 5	Table Index 6	Table Index 7	Table Index 8	Table Index 9
00h	<2.04h>	[7:0]	**CIS_FRAME_H_WIDTH_H**	06h	06h	06h	06h	06h
01h	<2.05h>	[7:0]	**CIS_FRAME_H_WIDTH_L**	E2h	E2h	E2h	E2h	E2h
02h	<2.06h>	[7:0]	**CIS_FRAME_V_DEPTH_H**	04h	04h	04h	02h	02h
03h	<2.07h>	[7:0]	**CIS_FRAME_V_DEPTH_L**	BCh	BFh	BCh	BDh	87h
04h	<2.08h>	[7:0]	**CIS_OUTPUT_H_WIDTH_H**	06h	06h	03h	06h	03h
05h	<2.09h>	[7:0]	**CIS_OUTPUT_H_WIDTH_L**	46h	46h	26h	46h	26h
06h	<2.0Ah>	[7:0]	**CIS_OUTPUT_V_DEPTH_H**	04h	04h	04h	02h	02h
07h	<2.0Bh>	[7:0]	**CIS_OUTPUT_V_DEPTH_L**	B4h	B4h	B4h	5Ch	5Ch
08h	<2.15h>	[7:0]	**CIS_H_EVEN_INC_L**	01h	01h	01h	01h	01h
09h	<2.17h>	[7:0]	**CIS_H_ODD_INC_L**	01h	01h	03h	01h	03h
0Ah	<2.19h>	[7:0]	**CIS_V_EVEN_INC_L**	01h	01h	01h	01h	01h
0Bh	<2.1Bh>	[7:0]	**CIS_V_ODD_INC_L**	01h	01h	01h	03h	03h
0Ch	<2.03h>[3]	[7:0]	**CIS_MIRR_ETC(Average sub)**	00h	00h	00h	08h	08h
0Dh	<5.6Eh>	[7:0]	**DSP5_POST_HSTART_H**	00h	00h	00h	00h	00h

Addr [4:0]	Target Register	Bits	Descriptions	Table Index 5	Table Index 6	Table Index 7	Table Index 8	Table Index 9
0Eh	<5.6Fh>	[7:0]	**DSP5_POST_HSTART_L**	04h	04h	04h	04h	04h
0Fh	<5.70h>	[7:0]	**DSP5_POST_HWIDTH_H**	06h	06h	03h	06h	03h
10h	<5.71h>	[7:0]	**DSP5_POST_HWIDTH_L**	40h	40h	20h	40h	20h
11h	<5.72h>	[7:0]	**DSP5_POST_VSTART_H**	00h	00h	00h	00h	00h
12h	<5.73h>	[7:0]	**DSP5_POST_VSTART_L**	02h	02h	02h	02h	02h
13h	<5.74h>	[7:0]	**DSP5_POST_VHEIGHT_H**	04h	04h	04h	02h	02h
14h	<5.75h>	[7:0]	**DSP5_POST_VHEIGHT_L**	B0h	B0h	B0h	58h	58h
15h	<5.7Ah>	[7:0]	**DSP5_IMG_HSIZEH**	06h	06h	03h	06h	03h
16h	<5.7Bh>	[7:0]	**DSP5_IMG_HSIZEL**	40h	40h	20h	40h	20h
17h	<5.7Ch>	[7:0]	**DSP5_IMG_VSIZEH**	04h	04h	04h	02h	02h
18h	<5.7Dh>	[7:0]	**DSP5_IMG_VSIZEL**	B0h	B0h	B0h	58h	58h
19h	<5.7Eh>	[7:0]	**DSP5_PSF**	44h	88h	00h	00h	00h
1Ah	<5.7Fh>	[7:0]	**DSP5_MSFX_H**	22h	22h	00h	00h	00h
1Bh	<5.80h>	[7:0]	**DSP5_MSFX_L**	E8h	E8h	00h	00h	00h
1Ch	<5.81h>	[7:0]	**DSP5_MSFY_H**	0Ah	0Ah	00h	00h	00h
1Dh	<5.82h>	[7:0]	**DSP5_MSFY_L**	AAh	AAh	00h	00h	00h
1Eh	<5.83h>	[7:0]	**DSP5_DW_HSIZEH**	01h	00h	03h	06h	03h
1Fh	<5.84h>	[7:0]	**DSP5_DW_HSIZEL**	60h	B0h	20h	40h	20h
20h	<5.85h>	[7:0]	**DSP5_DW_VSIZEH**	01h	00h	04h	02h	02h
21h	<5.86h>	[7:0]	**DSP5_DW_VSIZEL**	20h	90h	B0h	58h	58h
22h	<5.87h>	[7:0]	**DSP5_STARTXH**	00h	00h	00h	00h	00h
23h	<5.88h>	[7:0]	**DSP5_STARTXL**	00h	00h	00h	00h	00h
24h	<5.89h>	[7:0]	**DSP5_STARTYH**	00h	00h	00h	00h	00h
25h	<5.8Ah>	[7:0]	**DSP5_STARTYL**	00h	00h	00h	00h	00h
26h	<5.8Bh>	[7:0]	**DSP5_CLIP_HSIZEH**	01h	00h	03h	06h	03h
27h	<5.8Ch>	[7:0]	**DSP5_CLIP_HSIZEL**	60h	B0h	20h	40h	20h
28h	<5.8Dh>	[7:0]	**DSP5_CLIP_VSIZEH**	01h	00h	04h	02h	02h
29h	<5.8Eh>	[7:0]	**DSP5_CLIP_VSIZEL**	20h	90h	B0h	58h	58h
2Ah	<5.8Fh>	[7:0]	**DSP5_SEL_MAIN**	00h	00h	00h	00h	00h
2Bh	<5.90h>	[7:0]	**DSP5_HTERMH**	00h	00h	00h	00h	00h
2Ch	<5.91h>	[7:0]	**DSP5_HTERMM**	1Ch	39h	06h	06h	06h
2Dh	<5.92h>	[7:0]	**DSP5_HTERML**	AEh	5Ch	E0h	E0h	E0h
2Eh	<1.02h>	[7:0]	**DSP1_CRCB_SEL**	03h	03h	03h	03h	03h
2Fh	06h,15h, 1Ch Page	[7:0]	**OZONE, Boundary_INDEX**	00h	00h	10h	20h	30h

6. ISP REGISTER MAP (PAGE 05H)

Addr	Reset Value	Mnemonic	Attr	Bits	Descriptions
<5.00h>	04h	**YR_COEF_H**	R/W	[7:0]	R Signal Coefficient for Y Signal Generation (x0 ~ x1) [11:8] See REG_NAME YB_COEF_L!
<5.01h>	C9h	**YR_COEF_L**	R/W	[7:0]	R Signal Coefficient for Y Signal Generation (x0 ~ x1) [7:0] integer : 0bit, fraction : [11:0] 12bit See REG_NAME YB_COEF_L!
<5.02h>	09h	**YG_COEF_H**	R/W	[7:0]	G Signal Coefficient for Y Signal Generation (x0 ~ x1) [11:8] See REG_NAME YB_COEF_L!
<5.03h>	64h	**YG_COEF_L**	R/W	[7:0]	G Signal Coefficient for Y Signal Generation (x0 ~ x1) [7:0] integer : 0bit, fraction : [11:0] 12bit See REG_NAME YB_COEF_L!
<5.04h>	01h	**YB_COEF_H**	R/W	[7:0]	B Signal Coefficient for Y Signal Generation (x0 ~ x1) [11:8] See REG_NAME YB_COEF_L!
<5.05h>	D3h	**YB_COEF_L**	R/W	[7:0]	B Signal Coefficient for Y Signal Generation (x0 ~ x1) [7:0] integer : 0bit, fraction : [11:0] 12bit Y = (R*YR_COEF + G*YG_COEF + B*YB_COEF) / 4096
<5.06h>	08h	**CRR_H**	R/W	[7:0]	R Signal Coefficient for Cr Signal Generation (x0 ~ x1) [11:8] See REG_NAME CRB_L!
<5.07h>	2Dh	**CRR_L**	R/W	[7:0]	R Signal Coefficient for Cr Signal Generation (x0 ~ x1) [7:0] integer : 0bit, fraction : [11:0] 12bit See REG_NAME CRB_L!
<5.08h>	09h	**CRG_H**	R/W	[7:0]	G Signal Coefficient for Cr Signal Generation (x0 ~ x1) [11:8] See REG_NAME CRB_L!
<5.09h>	27h	**CRG_L**	R/W	[7:0]	G Signal Coefficient for Cr Signal Generation (x0 ~ x1) [7:0] integer : 0bit, fraction : [11:0] 12bit See REG_NAME CRB_L!
<5.0Ah>	0Eh	**CRB_H**	R/W	[7:0]	B Signal Coefficient for Cr Signal Generation (x0 ~ x1) [11:8] See REG_NAME CRB_L!
<5.0Bh>	ACh	**CRB_L**	R/W	[7:0]	B Signal Coefficient for Cr Signal Generation (x0 ~ x1) [7:0] integer : 0bit, fraction : [11:0] 12bit Cr = (R*CRR + G*CRG + B*CRB) / 4096
<5.0Ch>	0Dh	**CBR_H**	R/W	[7:0]	R Signal Coefficient for Cb Signal Generation (x0 ~ x1) [11:8] See REG_NAME CBB_L!
<5.0Dh>	3Fh	**CBR_L**	R/W	[7:0]	R Signal Coefficient for Cb Signal Generation (x0 ~ x1) [7:0] integer : 0bit, fraction : [11:0] 12bit See REG_NAME CBB_L!
<5.0Eh>	0Ah	**CBG_H**	R/W	[7:0]	G Signal Coefficient for Cb Signal Generation (x0 ~ x1) [11:8] See REG_NAME CBB_L!
<5.0Fh>	93h	**CBG_L**	R/W	[7:0]	G Signal Coefficient for Cb Signal Generation (x0 ~ x1) [7:0] integer : 0bit, fraction : [11:0] 12bit See REG_NAME CBB_L!
<5.10h>	08h	**CBB_H**	R/W	[7:0]	B Signal Coefficient for Cb Signal Generation (x0 ~ x1) [11:8] See REG_NAME CBB_L!
<5.11h>	2Dh	**CBB_L**	R/W	[7:0]	B Signal Coefficient for Cb Signal Generation (x0 ~ x1) [7:0]

Addr	Reset Value	Mnemonic	Attr	Bits	Descriptions
					integer : 0bit, fraction : [11:0] 12bit Cb = (R*CBR + G*CBG + B*CBB) / 4096
<5.12h>	3Eh	**YEDGE_Y0V1**	R/W	[7:0]	Y Edge Detection Filter Coefficient 01
<5.13h>	3Ch	**YEDGE_Y0V2**	R/W	[7:0]	Y Edge Detection Filter Coefficient 02
<5.14h>	3Ch	**YEDGE_Y0V3**	R/W	[7:0]	Y Edge Detection Filter Coefficient 03
<5.15h>	3Ch	**YEDGE_Y0V4**	R/W	[7:0]	Y Edge Detection Filter Coefficient 04
<5.16h>	3Eh	**YEDGE_Y0V5**	R/W	[7:0]	Y Edge Detection Filter Coefficient 05
<5.17h>	3Ch	**YEDGE_Y1V1**	R/W	[7:0]	Y Edge Detection Filter Coefficient 11
<5.18h>	00h	**YEDGE_Y1V2**	R/W	[7:0]	Y Edge Detection Filter Coefficient 12
<5.19h>	08h	**YEDGE_Y1V3**	R/W	[7:0]	Y Edge Detection Filter Coefficient 13
<5.1Ah>	00h	**YEDGE_Y1V4**	R/W	[7:0]	Y Edge Detection Filter Coefficient 14
<5.1Bh>	3Ch	**YEDGE_Y1V5**	R/W	[7:0]	Y Edge Detection Filter Coefficient 15
<5.1Ch>	3Ch	**YEDGE_Y2V1**	R/W	[7:0]	Y Edge Detection Filter Coefficient 21
<5.1Dh>	08h	**YEDGE_Y2V2**	R/W	[7:0]	Y Edge Detection Filter Coefficient 22
<5.1Eh>	18h	**YEDGE_Y2V3**	R/W	[7:0]	Y Edge Detection Filter Coefficient 23
<5.1Fh>	08h	**YEDGE_Y2V4**	R/W	[7:0]	Y Edge Detection Filter Coefficient 24
<5.20h>	3Ch	**YEDGE_Y2V5**	R/W	[7:0]	Y Edge Detection Filter Coefficient 25
<5.21h>	3Ch	**YEDGE_Y3V1**	R/W	[7:0]	Y Edge Detection Filter Coefficient 31
<5.22h>	00h	**YEDGE_Y3V2**	R/W	[7:0]	Y Edge Detection Filter Coefficient 32
<5.23h>	08h	**YEDGE_Y3V3**	R/W	[7:0]	Y Edge Detection Filter Coefficient 33
<5.24h>	00h	**YEDGE_Y3V4**	R/W	[7:0]	Y Edge Detection Filter Coefficient 34
<5.25h>	3Ch	**YEDGE_Y3V5**	R/W	[7:0]	Y Edge Detection Filter Coefficient 35
<5.26h>	3Eh	**YEDGE_Y4V1**	R/W	[7:0]	Y Edge Detection Filter Coefficient 41
<5.27h>	3Ch	**YEDGE_Y4V2**	R/W	[7:0]	Y Edge Detection Filter Coefficient 42
<5.28h>	3Ch	**YEDGE_Y4V3**	R/W	[7:0]	Y Edge Detection Filter Coefficient 43
<5.29h>	3Ch	**YEDGE_Y4V4**	R/W	[7:0]	Y Edge Detection Filter Coefficient 44
<5.2Ah>	3Eh	**YEDGE_Y4V5**	R/W	[7:0]	Y Edge Detection Filter Coefficient 45
<5.2Bh>	00h	**YCOEFMAT_P_HH**	R/W	[7:2] [1:0]	Reserved Y Edge Enhancement Positive Data Gain (x0 ~ x2) [25:24]
<5.2Ch>	04h	**YCOEFMAT_P_HL**	R/W	[7:0]	Y Edge Enhancement Positive Data Gain (x0 ~ x2) [23:16]
<5.2Dh>	00h	**YCOEFMAT_P_LH**	R/W	[7:0]	Y Edge Enhancement Positive Data Gain (x0 ~ x2) [15:8]
<5.2Eh>	00h	**YCOEFMAT_P_LL**	R/W	[7:0]	Y Edge Enhancement Positive Data Gain (x0 ~ x2) [7:0] [25] : integer part, [24:0] : fraction part xN : N * 33554432 (decimal value) → Y (hexa value) ex) x1 : 1* 33554432 → 2 00 00 00h
<5.2Fh>	00h	**YCOEFMAT_N_HH**	R/W	[7:2] [1:0]	Reserved Y Edge Enhancement Negative Data Gain (x0 ~ x2) [25:24]
<5.30h>	04h	**YCOEFMAT_N_HL**	R/W	[7:0]	Y Edge Enhancement Negative Data Gain (x0 ~ x2) [23:16]
<5.31h>	00h	**YCOEFMAT_N_LH**	R/W	[7:0]	Y Edge Enhancement Negative Data Gain (x0 ~ x2) [15:8]
<5.32h>	00h	**YCOEFMAT_N_LL**	R/W	[7:0]	Y Edge Enhancement Negative Data Gain (x0 ~ x2) [7:0] [25] : integer part, [24:0] : fraction part

Addr	Reset Value	Mnemonic	Attr	Bits	Descriptions
					xN : N * 33554432 (decimal value) → Y (hexa value) ex) x1 : 1* 33554432 → 2 00 00 00h
<5.33h>	00h	**YEG_DELAY**	R/W	[7:4] [3] [2:0]	Reserved Y Signal Selection for Edge Detection [3] 0 : Y Signal 1 : G Signal Y Edge Enhancement Signal Delay Match Control [2:0] 000 : 0 CK Delay 001 : 1 CK Delay 010 : 2 CK Delay 011 : 3 CK Delay 100 : -4 CK Delay 101 : -3 CK Delay 110 : -2 CK Delay 111 : -1 CK Delay
<5.34h>	20h	**YAPTCLP**	R/W	[7:0]	Y Edge Enhancement Clip Level (x2) (0 ~ 510) N : N / 2 (decimal value) → Y (hexa value) ex) 128 : 128 / 2 → 40h
<5.35h>	08h	**YAPTSC**	R/W	[7:0]	Y Edge Enhancement Noise Slice Level (0 ~ 63)
<5.36h>	0Bh	**YENHANTH**	R/W	[7:5] [4:3] [2:0]	Reserved Y Edge Detail Enhancement Gain [4:3] 00 : x0 01 : x1.25 10 : x1.5 11 : x1.75 Y Edge Detail Enhancement Threshold Value [2:0] 000 : 0 001 : 32 010 : 48 011 : 64 100 : 80 101 : 96 110 : 112 111 : 128
<5.37h>	0Ah	**YHCLP**	R/W	[7:4] [3:0]	Reserved Y High-Light Enhancement Clip Level (x8) (0 ~ 15)
<5.38h>	10h	**YHLGAIN**	R/W	[7:5] [4:0]	Reserved Y High-Light Aperture Gain (0~1) [4:0] : fraction part N : N * 32 (decimal) → Y (hexa value) ex) 0.5 : 0.5 * 32 → 10h
<5.39h>	7Fh	**YHLSC**	R/W	[7] [6:0]	Reserved Y High-Light Enhancement Noise Slice Level (0 ~ 127)
<5.3Ah>	FFh	**YWHITECLP**	R/W	[7:0]	Y Signal White Clip Level [7:0]
<5.3Bh>	FFh	**YEDGECLIPTH**	R/W	[7:0]	Y Edge Enhancement Signal Clip Level [7:0]
<5.3Ch>	FFh	**YAPTWHTH**	R/W	[7:0]	Y Edge Enhancement Signal Clip Level for High-Light Suppress [7:0]
<5.3Dh>	00h	**YWHITESLOPE**	R/W	[7:0]	Y Edge Enhancement Signal Gain Slope for High-Light Suppress [7:0]
<5.3Eh>	FCh	**YWHITE_H**	R/W	[7:6] [5:4] [3:2] [1:0]	Y Signal White Clip Level [9:8] Y Edge Enhancement Signal Clip Level [9:8] Y Edge Enhancement Signal Clip Level for High-Light Suppress [9:8] Y Edge Enhancement Signal Gain Slope for High-Light Suppress [9:8]
<5.3Fh>	00h	**YNONLIN**	R/W	[7:4] [3:2] [1:0]	Reserved Y Edge Enhancement Non-Linear Control Threshold Value 00 : 0 01 : 16(1.6%) 10 : 32(3.1%) 11 : 64(6.3%)" Y Edge Enhancement Non-Linear Control Gain 00 : x0 01 : x1.25

Addr	Reset Value	Mnemonic	Attr	Bits	Descriptions
					10 : x1.5 11 : x1
<5.40h>	41h	**YDELAY**	R/W	[7] [6:5] [4] [3:0]	0 : ODM or Flicker Zone Window Display 1 : Edge Display 00, 11 : Flicker Zone Display 01 : AF Zone Display 10 : ODM Zone Display Reserved Y Delay Match
<5.41h>	09h	**YDELAY_HVD**	R/W	[7:0]	H/V Sync Delay match Control
<5.42h>	10h	**CEGFALL**	R/W	[7:0]	Edge Color Suppress Gain Slope (0 ~ 1)
<5.43h>	00h	**CHLFALL**	R/W	[7:0]	High-Light Color Suppress Gain Slope (0 ~ 1)
<5.44h>	08h	**CLLFALL**	R/W	[7:0]	Low-Light Color Suppress Gain Slope (0 ~ 1)
<5.45h>	A0h	**CEGREF**	R/W	[7:0]	Edge Color Suppress Reference Threshold Value [7:0]
<5.46h>	7Ah	**CHLREF**	R/W	[7:0]	High-Light Color Suppress Reference Threshold Value [7:0]
<5.47h>	40h	**CLLREF**	R/W	[7:0]	Low-Light Color Suppress Reference Threshold Value [7:0]
<5.48h>	0Ch	**CEGREF_H**	R/W	[7:6] [5:4] [3:2] [1:0]	Reserved Edge Color Suppress Reference Threshold Value [9:8] High-Light Color Suppress Reference Threshold Value [9:8] Low-Light Color Suppress Reference Threshold Value [9:8]
<5.49h>	31h	**CCS_SEL**	R/W	[7:6] [5:4] [3] [2:0]	Reserved Color Suppress Selection Signal 00 : No Suppress 01 : High/Low-Light Color Suppress 10 : Edge Color Suppress 11 : All" Edge Signal Selection for Edge Color Suppress 0 : Edge Filter 1 Output 1 : Edge Filter 2 Output (Edge Enhancement Filter Output) Color Suppress Signal Delay Match Control 000 : 0 CK Delay 001 : 1 CK Delay 010 : 2 CK Delay 011 : 3 CK Delay 100 : -4 CK Delay 101 : -3 CK Delay 110 : -2 CK Delay 111 : -1 CK Delay
<5.4Ah>	04h	**CCS_EGGAIN_HH**	R/W	[7:3] [2:0]	Reserved Color Suppress Signal Gain (x0 ~ x4) [26:24]
<5.4Bh>	00h	**CCS_EGGAIN_HL**	R/W	[7:0]	Color Suppress Signal Gain (x0 ~ x4) [23:16]
<5.4Ch>	00h	**CCS_EGGAIN_LH**	R/W	[7:0]	Color Suppress Signal Gain (x0 ~ x4) [15:8]
<5.4Dh>	00h	**CCS_EGGAIN_LL**	R/W	[7:0]	Color Suppress Signal Gain (x0 ~ x4) [7:0] [26:25] : integer part, [24:0] : fraction part N : N * 33554432 (decimal value) → Y (hexa value) ex) x2 : 2 * 33554432 → 4 00 00 00h
<5.4Eh>	5Ah	**CRYGP**	R/W	[7:0]	Positive Cr Signal Gain for Hue Control (x0 ~ x4)[7:0] [11:10] : integer part, [9:0] : fraction part N : N * 1024 (decimal value) → Y (hexa value) ex) x2 : 2 * 1024 → 8 00h
<5.4Fh>	5Ah	**CRYGN**	R/W	[7:0]	Negative Cr Signal Gain for Hue Control (x0 ~ x4)[7:0] [11:10] : integer part, [9:0] : fraction part N : N * 1024 (decimal value) → Y (hexa value) ex) x2 : 2 * 1024 → 8 00h

Addr	Reset Value	Mnemonic	Attr	Bits	Descriptions
<5.50h>	44h	**CRYG_UP**	R/W	[7:4] [3:0]	Positive Cr Signal Gain for Hue Control (x0 ~ x4) [11:8] Positive Cr Signal Gain for Hue Control (x0 ~ x4) [11:8]
<5.51h>	00h	**CRYHP**	R/W	[7:0]	Positive Cr Signal Hue Control Coefficient for Hue Control (x0 ~ x4)[7:0] [11:10] : integer part, [9:0] : fraction part N : N * 1024 (decimal value) → Y (hexa value) ex) x2 : 2 * 1024 → 8 00h
<5.52h>	00h	**CRYHN**	R/W	[7:0]	Negative Cr Signal Hue Control Coefficient for Hue Control (x0 ~ x4)[7:0] [11:10] : integer part, [9:0] : fraction part N : N * 1024 (decimal value) → Y (hexa value) ex) x2 : 2 * 1024 → 8 00h
<5.53h>	02h	**CRYH_UP**	R/W	[7:4] [3:0]	Positive Cr Signal Hue Control Coefficient for Hue Control (x0 ~ x4) [11:8] Negative Cr Signal Hue Control Coefficient for Hue Control (x0 ~ x4) [11:8]
<5.54h>	A0h	**CBYGP**	R/W	[7:0]	Positive Cb Signal Gain for Hue Control (x0 ~ x4)[7:0] [11:10] : integer part, [9:0] : fraction part N : N * 1024 (decimal value) → Y (hexa value) ex) x2 : 2 * 1024 → 8 00h
<5.55h>	00h	**CBYGN**	R/W	[7:0]	Negative Cb Signal Gain for Hue Control (x0 ~ x4)[7:0] [11:10] : integer part, [9:0] : fraction part N : N * 1024 (decimal value) → Y (hexa value) ex) x2 : 2 * 1024 → 8 00h
<5.56h>	44h	**CBYG_UP**	R/W	[7:4] [3:0]	Positive Cb Signal Gain for Hue Control (x0 ~ x4) [11:8] Negative Cb Signal Gain for Hue Control (x0 ~ x4) [11:8]
<5.57h>	D9h	**CBYHP**	R/W	[7:0]	Positive Cb Signal Hue Control Coefficient for Hue Control (x0 ~ x4)[7:0] [11:10] : integer part, [9:0] : fraction part N : N * 1024 (decimal value) → Y (hexa value) ex) x2 : 2 * 1024 → 8 00h
<5.58h>	5Ah	**CBYHN**	R/W	[7:0]	Negative Cb Signal Hue Control Coefficient for Hue Control (x0 ~ x4)[7:0] [11:10] : integer part, [9:0] : fraction part N : N * 1024 (decimal value) → Y (hexa value) ex) x2 : 2 * 1024 → 8 00h
<5.59h>	00h	**CBYH_UP**	R/W	[7:4] [3:0]	Positive Cb Signal Hue Control Coefficient for Hue Control (x0 ~ x4) [11:8] Negative Cb Signal Hue Control Coefficient for Hue Control (x0 ~ x4) [11:8] Cr(hue) = Cr*CRYG + Cb*CRYH Cb(hue) = Cr*CBYH + Cb*CBYG
<5.5Ah>	32h	**CRYTH_H**	R/W	[7:0]	High-Threshold Value for Hue Boundary Control of Cr Signal
<5.5Bh>	14h	**CRYTH_L**	R/W	[7:0]	Low-Threshold Value for Hue Boundary Control of Cr Signal
<5.5Ch>	32h	**CBYTH_H**	R/W	[7:0]	High-Threshold Value for Hue Boundary Control of Cb Signal
<5.5Dh>	14h	**CBYTH_L**	R/W	[7:0]	Low-Threshold Value for Hue Boundary Control of Cb Signal
<5.5Eh>	00h	**CHUE**	R/W	[7:2] [1] [0]	Reserved Hue Boundary Control Enable 0 : Off 1 : On Hue Gab Fix 0 : Normal 1 : x1
<5.5Fh>		**Reserved**			
<5.60h>		**Reserved**			

Addr	Reset Value	Mnemonic	Attr	Bits	Descriptions
<5.61h>		**Reserved**			
<5.62h>		**Reserved**			
<5.63h>		**Reserved**			
<5.64h>	00h	**CRDS**	R/W	[7:0]	Dark Slice Coefficient of R Signal (-128≤CRDS≤127)
<5.65h>	00h	**CGDS**	R/W	[7:0]	Dark Slice Coefficient of G Signal (-128≤CGDS≤127)
<5.66h>	00h	**CBDS**	R/W	[7:0]	Dark Slice Coefficient of B Signal (-128≤CBDS≤127)
<5.67h>	ACh	**CRWB**	R/W	[7:0]	CRWB [7:0], White Balance Coefficient of R Signal (0≤CRWB≤32)
<5.68h>	40h	**CGWB**	R/W	[7:0]	White Balance Coefficient of G Signal (0≤CGWB≤4) R(Black & White) = CRWB×R + CRDS(0≤CRWB<32 , -128≤CRDS≤127) G(Black & White) = CGWB×G + CGDS(0≤CGWB<4 , -128≤CGDS≤127) B(Black & White) = CBWB×B + CBDS (0≤CBWB<32 , -128≤CBDS≤127)
<5.69h>	9Eh	**CBWB**	R/W	[7:0]	CBWB [7:0]. White Balance Coefficient of B Signal (0≤CBWB≤32)
<5.6Ah>	00h	**CRGBWB_UP**	R/W	[7:4] [3:0]	CRWB[11:8] CBWB[11:8]
<5.6Bh>		**Reserved**			
<5.6Ch>	00h	**CLPF_SIGTHR01**	R/W	[7:0]	Low Threshold of 1-Dimension C-Noise Filter[7:0]
<5.6Dh>	00h	**CLPF_SIGTHR01**	R/W	[7:0]	High Threshold of 1-Dimension C-Noise Filter[7:0]
<5.6Eh>	00h	**POST_HSTART_H**	R/W	[7:0]	post processor output h sync start position [15:8]
<5.6Fh>	02h	**POST_HSTART_L**	R/W	[7:0]	post processor output h sync start position [7:0]
<5.70h>	06h	**POST_HWIDTH_H**	R/W	[7:0]	post processor output h sync width [15:8]
<5.71h>	40h	**POST_HWIDTH_L**	R/W	[7:0]	post processor output h sync width [7:0]
<5.72h>	00h	**POST_VSTART_H**	R/W	[7:0]	post processor output v sync start [15:8]
<5.73h>	02h	**POST_VSTART_L**	R/W	[7:0]	post processor output v sync start [7:0]
<5.74h>	04h	**POST_VHEIGHT_H**	R/W	[7:0]	post processor output v sync height [15:8]
<5.75h>	B0h	**POST_VHEIGHT_L**	R/W	[7:0]	post processor output v sync height [7:0]
<5.76h>	1Eh	**YLPF_SIGTHR01**	R/W	[7:0]	Low Threshold of 1-Dimension Y-Noise Filter[7:0].
<5.77h>	32h	**YLPF_SIGTHR02**	R/W	[7:0]	High Threshold of 1-Dimension Y-Noise Filter[7:0].
<5.78h>	00h	**YLPF_SIGTHR_H**	R/W	[7:4] [3:2] [1:0]	Reserved High Threshold of 1-Dimension Y-Noise Filter[9:8]. Low Threshold of 1-Dimension Y-Noise Filter[9:8].
<5.79h>		**Reserved**			
<5.7Ah>	06h	**IMG_HSIZEH**	R/W	[7:0]	Scaler H size (H order)
<5.7Bh>	40h	**IMG_HSIZEL**	R/W	[7:0]	Scaler H size (L order)
<5.7Ch>	04h	**IMG_VSIZEH**	R/W	[7:0]	Scaler V size (H order)
<5.7Dh>	B0h	**IMG_VSIZEL**	R/W	[7:0]	Scaler V size (L order)
<5.7Eh>	00h	**PSF**	R/W	[7:0]	pre-scale factor PSF[7:4] : for horizontal direction PSF[3:0] : for vertical direction. Its value can be 0, 2, 4 and 8.
<5.7Fh>	00h	**MSFXH**	R/W	[7:0]	Horizontal main scaling factor
<5.80h>	00h	**MSFXL**	R/W	[7:0]	Horizontal main scaling factor
<5.81h>	00h	**MSFYH**	R/W	[7:0]	Vertical main scaling factor

Addr	Reset Value	Mnemonic	Attr	Bits	Descriptions
<5.82h>	00h	**MSFYL**	R/W	[7:0]	Vertical main scaling factor
<5.83h>	06h	**DW_HSIZEH**	R/W	[7:0]	Down scaled horizontal size (H order)
<5.84h>	40h	**DW_HSIZEL**	R/W	[7:0]	Down scaled horizontal size (L order)
<5.85h>	04h	**DW_VSIZEH**	R/W	[7:0]	Down scaled vertical size (H order)
<5.86h>	B0h	**DW_VSIZEL**	R/W	[7:0]	Down scaled vertical size (L order)
<5.87h>	00h	**STARTXH**	R/W	[7:0]	Horizontal start location (H)
<5.88h>	00h	**STARTXL**	R/W	[7:0]	Horizontal start location (L)
<5.89h>	00h	**STARTYH**	R/W	[7:0]	Vertical start location (H)
<5.8Ah>	00h	**STARTYL**	R/W	[7:0]	Vertical start location (L)
<5.8Bh>	06h	**CLIP_HSIZEH**	R/W	[7:0]	Target width (H)
<5.8Ch>	40h	**CLIP_HSIZEL**	R/W	[7:0]	Target width (L)
<5.8Dh>	04h	**CLIP_VSIZEH**	R/W	[7:0]	Target height (H)
<5.8Eh>	B0h	**CLIP_VSIZEL**	R/W	[7:0]	Target height (L)
<5.8Fh>	00h	**SEL_MAIN**	R/W	[7:3] [2] [1] [0]	Reserved FORMAT_656 Half PCLK Enable Selection of main scaler method 1’b0 : bi-linear interpolation 1’b1 : sub-sampling
<5.90h>	00h	**HTERMH**	R/W	[7:0]	Clock count of one H period(active + blank) (H)
<5.91h>	06h	**HTERMM**	R/W	[7:0]	Clock count of one H period(active + blank) (M)
<5.92h>	E0h	**HTERML**	R/W	[7:0]	Clock count of one H period(active + blank) (L)

7. ODM ZONE REGISTER MAP (PAGE 06H)

* ODM Zone Page (Page6) Registers will be loaded to Target Registers (ISP registers) when performing Image Format command <0.02h> or <0.73h> or <0.74h>.

* ODM Zone Table Index
  case of (Sub-sampling Table Index = 0)
    ODM Index = <3.2Fh>
  case of (Sub-sampling Table Index = 1)
    ODM Index = <4.5Fh>
  case of (Sub-sampling Table Index = 2)
    ODM Index = <4.8Fh>

TABLE 1. ODM TABLE

Address 1	ODM Index	Size
00h~0Fh	00h	H = 1,V = 1
10h~1Fh	10h	H = 2,V = 1
20h~2Fh	20h	H = 1,V = 2
30h~3Fh	30h	H = 2,V = 2
40h~4Fh	40h	H = 4,V = 1
50h~5Fh	50h	H = 4,V = 4
60h~6Fh	60h	Reserved

TABLE 2. DETAILED REGISTER TABLE OF TABLE 1 (ATTRIBUTE OF ALL THESE VALUES IS R/W)

Addr 1 [3:0]	Target Register	Bits	Descriptions	Table Index 00h	Table Index 10h	Table Index 20h	Table Index 30h	Table Index 40h	Table Index 50h	Table Index 60h
00h	<1.B7h>	[7:0]	**AE H Start H**	00h	00h	00h	00h	00h	00h	00h
01h	<1.B8h>	[7:0]	**AE H Start L**	0Ah	0Ah	0Ah	0Ah	0Ah	0Ah	0Ah
02h	<1.B9h>	[7:0]	**AE H Width H**	00h	00h	00h	00h	00h	00h	00h
03h	<1.BAh>	[7:0]	**AE H width L**	C6h	61h	C5h	61h	2Fh	30h	C6h
04h	<1.BBh>	[7:0]	**AE V Start H**	00h	00h	00h	00h	00h	00h	00h
05h	<1.BCh>	[7:0]	**AE V Start L**	18h	18h	08h	08h	18h	08h	18h
06h	<1.BDh>	[7:0]	**AE V Height H**	00h	00h	00h	00h	00h	00h	00h
07h	<1.BEh>	[7:0]	**AE V Height L**	C0h	C0h	60h	60h	C0h	30h	C0h
08h	<1.C0h>	[7:0]	**AWB H Start H**	00h	00h	00h	00h	00h	00h	00h
09h	<1.C1h>	[7:0]	**AWB H Start L**	0Ah	0Ah	0Ah	0Ah	0Ah	0Ah	0Ah
0Ah	<1.C2h>	[7:0]	**AWB H Width H**	00h	00h	00h	00h	00h	00h	00h
0Bh	<1.C3h>	[7:0]	**AWB H Width L**	C6h	5Eh	C6h	61h	31h	31h	C6h
0Ch	<1.C4h>	[7:0]	**AWB V Start H**	00h	00h	00h	00h	00h	00h	00h
0Dh	<1.C5h>	[7:0]	**AWB V Start L**	18h	18h	08h	08h	18h	08h	18h
0Eh	<1.C6h>	[7:0]	**AWB V Height H**	00h	00h	00h	00h	00h	00h	00h
0Fh	<1.C7h>	[7:0]	**AWB V Height L**	8Fh	8Fh	4Ah	4Ah	8Fh	25h	8Fh

8. PROGRAM CONSTANT REGISTER MAP (PAGE 07H)

Addr	Reset Value	Mnemonic	Attr	Bits	Descriptions
<7.00h>	00h	**AWB_SAT_QMOVE_OPTION**	R/W	[7] [6:0]	AWB saturation Quick Move Option QMOVE option on QMOVE Method 01h : goto 5000K 02h : goto 3000K 03h : goto 2000K 04h : goto predefined 05h : goto auto
<7.01h>	C0h	**AWB_SAT_QMOVE_THR**	R/W	[7:0]	AWB saturation Quick Move Y threshold
<7.02h>	A2h	**AWB_SAT_QMOVE_RGAIN**	R/W	[7:0]	Rgain for AWB saturation quick move option
<7.03h>	40h	**AWB_SAT_QMOVE_GGAIN**	R/W	[7:0]	Ggain for AWB saturation quick move option
<7.04h>	A7h	**AWB_SAT_QMOVE_BGAIN**	R/W	[7:0]	Bgain for AWB saturation quick move option
<7.05h>	00h	**STORE_AE_HH**	R/W	[7:0]	EIT value [31:24] will be restored (or stored) for <0.70h>
<7.06h>	00h	**STORE_AE_HL**	R/W	[7:0]	EIT value [23:16] will be restored (or stored) for <0.70h>
<7.07h>	00h	**STORE_AE_LH**	R/W	[7:0]	EIT value [15:8] will be restored (or stored) for <0.70h>
<7.08h>	00h	**STORE_AE_LL**	R/W	[7:0]	EIT value [7:0] will be restored (or stored) for <0.70h>
<7.09h>	00h	**STORE_AWB_RGAIN_H**	R/W	[7:2] [1:0]	Reserved AWB R point value [9:8] will be restored (or stored) for <0.70h>
<7.0Ah>	00h	**STORE_AWB_RGAIN_L**	R/W	[7:0]	AWB R point value [7:0] will be restored (or stored) for <0.70h>
<7.0Bh>	00h	**STORE_AWB_BGAIN_H**	R/W	[7:2] [1:0]	Reserved AWB B point value [9:8] will be restored (or stored) for <0.70h>
<7.0Ch>	00h	**STORE_AWB_BGAIN_L**	R/W	[7:0]	AWB B point value [7:0]will be restored (or stored) for <0.70h>
<7.0Dh>	00h	**STORE_AWB_GGAIN_H**	R/W	[7:2] [1:0]	Reserved AWB G point value [9:8] will be restored (or stored) for <0.70h>
<7.0Eh>	00h	**STORE_AWB_GGAIN_L**	R/W	[7:0]	AWB G point value [7:0] will be restored (or stored) for <0.70h>
<7.0Fh>	01h	**Reserved**			
<7.10h>	01h	**Reserved**			
<7.11h>	00h	**GGAIN_Offset**	R/W	[7:0]	G gain offset
<7.12h>	00h	**GGAIN_AGC0**	R/W	[7:0]	AGC 0 to get G gain
<7.13h>	40h	**GGAIN_AGC1**	R/W	[7:0]	AGC 1 to get G gain
<7.14h>	60h	**GGAIN_AGC2**	R/W	[7:0]	AGC 2 to get G gain
<7.15h>	70h	**GGAIN_AGC3**	R/W	[7:0]	AGC 3 to get G gain
<7.16h>	78h	**GGAIN_AGC4**	R/W	[7:0]	AGC 4 to get G gain
<7.17h>	40h	**GGAIN_Ggain0**	R/W	[7:0]	G gain 0 to get G gain
<7.18h>	47h	**GGAIN_Ggain1**	R/W	[7:0]	G gain 1 to get G gain
<7.19h>	44h	**GGAIN_Ggain2**	R/W	[7:0]	G gain 2 to get G gain
<7.1Ah>	41h	**GGAIN_Ggain3**	R/W	[7:0]	G gain 3 to get G gain
<7.1Bh>	3Bh	**GGAIN_Ggain4**	R/W	[7:0]	G gain 4 to get G gain
<7.1Ch		**Reserved**			

Addr	Reset Value	Mnemonic	Attr	Bits	Descriptions
-25h>					
<7.26h>	04h	**SHT_1**	R/W	[7:0]	Constant for AE target suppress in AE shutter mode
<7.27h>	40h	**SHT_2**	R/W	[7:0]	Constant for AE target suppress in AE shutter mode
<7.28h>	40h	**AGC_1**	R/W	[7:0]	Constant for AE target suppress in AE AGC mode
<7.29h>	60h	**AGC_2**	R/W	[7:0]	Constant for AE target suppress in AE AGC mode
<7.2Ah>	00h	**TOFF_SHT0**	R/W	[7:0]	Constant for AE target suppress in AE shutter mode
<7.2Bh>	00h	**TOFF_SHT1**	R/W	[7:0]	Constant for AE target suppress in AE shutter mode
<7.2Ch>	00h	**TOFF_SHT2**	R/W	[7:0]	Constant for AE target suppress in AE shutter mode
<7.2Dh>	00h	**TOFF_AGC0**	R/W	[7:0]	Constant for AE target suppress in AE AGC mode
<7.2Eh>	00h	**TOFF_AGC1**	R/W	[7:0]	Constant for AE target suppress in AE AGC mode
<7.2Fh>	00h	**TOFF_AGC2**	R/W	[7:0]	Constant for AE target suppress in AE AGC mode
<7.30h>	C0h	**SEPIA_CR**	R/W	[7:0]	Cr value for sepia special effect 1
<7.31h>	20h	**SEPIA_CB**	R/W	[7:0]	Cb value for sepia special effect 1
<7.32h>	40h	**AQUA_CR**	R/W	[7:0]	Cr value for aqua special effect 2
<7.33h>	C0h	**AQUA_CB**	R/W	[7:0]	Cb value for aqua special effect 2
<7.34h>	00h	**GREEN_CR**	R/W	[7:0]	Cr value for green special effect 2
<7.35h>	B0h	**GREEN_CB**	R/W	[7:0]	Cb value for green special effect 2
<7.36h>	00h	**NO_WAITVSYNC**	R/W	[7:0]	Don't wait Vsync On(1) / Off(0)
<7.37h>	00h	**CLOCK_ADD**	R/W	[7:0]	Main clock precision, refer to <0.72h>
<7.38h -41h>		**Reserved**			
<7.42h>	04h	**LOW_BRIGHT_AWB**	R/W	[7] [6:4] [3:0]	LOW_BRIGHT_EN Reserved LOW_TARGET_RATIO
<7.43h>	6Bh	**LOW_BRIGHT_AWB_AGC_THR**	R/W	[7:0]	Low Bright AGC Threshold (recommend MAX AGC)
<7.44h>	00h	**LOW_BRIGHT_AWB_MODE**	R/W	[7:0]	0x01 : NORMAL 0x02 : INTERPOLATION 0x03 : FULL_AVG
<7.45h>	30h	**LOW_BRIGHT_AWB_MIN_R**	R/W	[7:0]	R_MIN Threshold for Low bright AWB
<7.46h>	30h	**LOW_BRIGHT_AWB_MIN_B**	R/W	[7:0]	B_MIN Threshold for Low bright AWB
<7.47h>	10h	**LOW_BRIGHT_AWB_Y_MIN**	R/W	[7:0]	Y_MIN Threshold for Low bright AWB
<7.48h -4Dh>		**Reserved**			
<7.4Eh>	04h	**ODM_AE on off**	R/W	[7:3] [2] [1:0]	Reserved AE_ODM_INT Reserved
<7.4Fh -5Fh>		**Reserved**			
<7.60h>	02h	**FLK_THR**	R/W	[7:0]	Threshold for flicker detection (0x01~0xFF) Do not set by zero If this value increase then detector's sensibility decrease.

Addr	Reset Value	Mnemonic	Attr	Bits	Descriptions
<7.61h>	10h	**FLK_WIN_LOWHI**	R/W	[7:4] [3:0]	Upper boundary offset to check a valid interval for flicker detection Lower boundary offset to check a valid interval for flicker detection
<7.62h>	11h	**FLK_EDGE_LOWHI**	R/W	[7:4] [3:0]	Upper boundary offset to check a valid edges for flicker detection Lower boundary offset to check a valid edges for flicker detection
<7.63h>	07h	**FLK_DECI_OPT**	R/W	[7:5] [4:0]	Boundary for flicker frequency detection Duration of flicker
<7.64h>	2Dh	**FLK_OPTION**	R/W	[7] [6] [5] [4] [3] [2] [1] [0]	Reserved Flicker one time detection On(1)/Off(0) Flicker zone auto resize On(1)/Off(0) Reserved Flicker difference On(1)/Off(0) Flicker detect when shutter is bigger than minimum On(1)/Off(0) Flicker detect when mode is not AGC On(1)/Off(0) Flicker detect when AE Stable On(1)/Off(0)
<7.65h>	00h	**FLK_EXIT_AGCVALUE**	R/W	[7:0]	Min AGC value : relate with <7.64h [1]>
<7.66h>	00h	**WDTCR**	R/W	[7:1] [0]	Reserved Watch Dog Timer On(1)/Off(0)
<7.67h>	FFh	**WDTLDR_H**	R/W	[7:0]	WDT time [15:8]
<7.68h>	FFh	**WDTLDR_L**	R/W	[7:0]	WDT time [7:0]
<7.69h>	00h	**MIRROR_XOR**	R/W	[7:0]	Constant for mirror
<7.6Ah -84h>		**Reserved**			
<7.85h>	82h	**AWB_D65_R**	R/W	[7:0]	AWB2 White point R for D65
<7.86h>	B8h	**AWB_D65_B**	R/W	[7:0]	AWB2 White point B for D65
<7.87h>	A0h	**AWB_CWF_R**	R/W	[7:0]	AWB2 White point R for CWF
<7.88h>	8Eh	**AWB_CWF_B**	R/W	[7:0]	AWB2 White point B for CWF
<7.89h>	C0h	**AWB_A_R**	R/W	[7:0]	AWB2 White point R for Incand A
<7.8Ah>	7Eh	**AWB_A_B**	R/W	[7:0]	AWB2 White point B for Incand A
<7.8Bh>	0Bh	**AWB_D65_R_LEFT_MIN**	R/W	[7:0]	AWB2 Tracking Boundary Constant
<7.8Ch>	0Bh	**AWB_D65_B_UP_MAX**	R/W	[7:0]	AWB2 Tracking Boundary Constant
<7.8Dh>	0Bh	**AWB_A_R_RIGHT_MAX**	R/W	[7:0]	AWB2 Tracking Boundary Constant
<7.8Eh>	0Bh	**AWB_A_B_DOWN_MIN**	R/W	[7:0]	AWB2 Tracking Boundary Constant
<7.8Fh>	0Fh	**AWB_SLOPE_TOP**	R/W	[7:0]	AWB2 Tracking Boundary Constant
<7.90h>	12h	**AWB_SLOPE_BOTTOM**	R/W	[7:0]	AWB2 Tracking Boundary Constant
<7.91h>	67h	**AWB_INTERCEPT_NORMAL_R**	R/W	[7:0]	Constant for AWB2
<7.92h>	1Dh	**AWB_INTERCEPT_NORMAL_B**	R/W	[7:0]	Constant for AWB2
<7.93h>	15h	**AWB_CENTER_COLOR_WEIGHT_AVG**	R/W	[7:4] [3:0]	AWB2_93_INTCT_R_H AWB2_93_WEIGHT
<7.94h>	11h	**AWB_CENTER_COLOR_WEIGHT_CNTR**	R/W	[7:4] [3:0]	AWB2_94_INTCT_B_H AWB2_94_WEIGHT
<7.95h>		**Reserved**			

Addr	Reset Value	Mnemonic	Attr	Bits	Descriptions
<7.96h>		**Reserved**			
<7.97h>	10h	**AWB Lowest**	R/W	[7:0]	Constant for AWB
<7.98h>		**Reserved**			
<7.99h>		**Reserved**			
<7.9Ah>	02h	**AWB_MOVE_STEP2_DIFF**	R/W	[7:0]	Constant for AWB Speed
<7.9Bh>	04h	**AWB_MOVE_STEP3_DIFF**	R/W	[7:0]	Constant for AWB Speed
<7.9Ch>	08h	**AWB_MOVE_STEP4_DIFF**	R/W	[7:0]	Constant for AWB Speed
<7.9Dh>	08h	**AWB_MOVE_STEP_MAX_DIFF**	R/W	[7:0]	Constant for AWB Speed (this reg >= 1)
<7.9Eh>	01h	**AWB_MOVE_STEP_DIV**	R/W	[7:0]	Constant for AWB Speed (this reg >= 0)
<7.9Fh>		**Reserved**			

9. R SHADE COEFFICIENT REGISTER MAP((PAGE 09H)

*** MSB [23 or 7] is sign bit(1 = minus)**

Addr	Reset Value	Mnemonic	Attr	Bits	Descriptions
<9.00h>	20h	**SHADE_CMD**	R/W	[7:6] [5] [4] [3] [2] [1] [0]	Reserved R/B or G selection (For 1Channel) Gr or Gb line selection (For 1Channel) Center Line display for test mode radial shade selection 0 : 3ch, 1 : 1ch RGB shade 0 : OFF 1 : ON Reserved
<9.01h>	06h	**WIDTH_R[11:8]**	R/W	[7:4] [3:0]	Reserved WIDTH_R[11:8] Shading Active Area Horizontal Size
<9.02h>	40h	**WIDTH_R[7:0]**	R/W	[7:0]	WIDTH_R[7:0]
<9.03h>	04h	**HEIGHT_R[11:8]**	R/W	[7:4] [3:0]	Reserved HEIGHT_R[11:8] Shading Active Area Vertical Size
<9.04h>	B0h	**HEIGHT_R[7:0]**	R/W	[15:8]	HEIGHT_R[7:0]
<9.05h>	03h	**SH_XCH_R**	R/W	[7:4] [3:0]	Reserved SHADE_XC_R_r[11:8] Horizontal Center Value For RGB Shading
<9.06h>	20h	**SH_XCL_R**	R/W	[7:0]	SHADE_XC_R_r[7:0]
<9.07h>	02h	**SH_YCH_R**	R/W	[7:4] [3:0]	Reserved SHADE_YC_R_r[11:8] Vertical Center Value For RGB Shading
<9.08h>	58h	**SH_YCL_R**	R/W	[7:0]	SHADE_YC_R_r[7:0]
<9.09h>	03h	**SH_XCH_G**	R/W	[7:4] [3:0]	Reserved SHADE_XC_G_r[11:8] Horizontal Center Value For RGB Shading
<9.0Ah>	20h	**SH_XCL_G**	R/W	[7:0]	SHADE_XC_G_r[7:0]
<9.0Bh>	02h	**SH_YCH_G**	R/W	[7:4] [3:0]	Reserved SHADE_YC_G_r[11:8] Vertical Center Value For RGB Shading
<9.0Ch>	58h	**SH_YCL_G**	R/W	[7:0]	SHADE_YC_G_r[7:0]
<9.0Dh>	03h	**SH_XCH_B**	R/W	[7:4] [3:0]	Reserved SHADE_XC_B_r[11:8] Horizontal Center Value For RGB Shading
<9.0Eh>	20h	**SH_XCL_B**	R/W	[7:0]	SHADE_XC_B_r[7:0]
<9.0Fh>	02h	**SH_YCH_B**	R/W	[7:4] [3:0]	Reserved SHADE_YC_B_r[11:8] Vertical Center Value For RGB Shading
<9.10h>	58h	**SH_YCL_B**	R/W	[7:0]	SHADE_YC_B_r[7:0]
<9.11h>	00h	**SH_OFF_XH_R**	R/W	[7:0]	Offset_X_R[15:8] Horizontal Start Offset For R channel (0<= Offset<256)
<9.12h>	00h	**SH_OFF_XL_R**	R/W	[7:0]	Offset_X_R[7:0]
<9.13h>	00h	**SH_OFF_YH_R**	R/W	[7:0]	Offset_Y_R[15:8] Vertical Start Offset For R channel (0<= Offset<256)
<9.14h>	00h	**SH_OFF_YL_R**	R/W	[7:0]	Offset_Y_R[7:0]
<9.15h>	00h	**SH_OFF_XH_G**	R/W	[7:0]	Offset_X_G[15:8] Horizontal Start Offset For G channel (0<= Offset<256)
<9.16h>	00h	**SH_OFF_XL_G**	R/W	[7:0]	Offset_X_G[7:0]
<9.17h>	00h	**SH_OFF_YH_G**	R/W	[7:0]	Offset_Y_G[15:8] Vertical Start Offset For G channel (0<= Offset<256)

Addr	Reset Value	Mnemonic	Attr	Bits	Descriptions
<9.18h>	00h	**SH_OFF_YL_G**	R/W	[7:0]	Offset_Y_G[7:0]
<9.19h>	00h	**SH_OFF_XH_B**	R/W	[7:0]	Offset_X_B[15:8] Horizontal Start Offset For B channel (0<= Offset<256)
<9.1Ah>	00h	**SH_OFF_XL_B**	R/W	[7:0]	Offset_X_B[7:0]
<9.1Bh>	00h	**SH_OFF_YH_B**	R/W	[7:0]	Offset_Y_B[15:8] Vertical Start Offset For B channel (0<= Offset<256)
<9.1Ch>	00h	**SH_OFF_YL_B**	R/W	[7:0]	Offset_Y_B[7:0]
<9.1Dh>	80h	**SH_Del_eH_R**	R/W	[7:0]	Delta_e_R[15:8] Horizontal right delta For R channel (0<= Delta <=1)
<9.1Eh>	00h	**SH_Del_eL_R**	R/W	[7:0]	Delta_e_R[7:0]
<9.1Fh>	80h	**SH_Del_wH_R**	R/W	[7:0]	Delta_w_R[15:8] Horizontal left delta For R channel (0<= Delta <=1)
<9.20h>	00h	**SH_Del_wL_R**	R/W	[7:0]	Delta_w_R[7:0]
<9.21h>	80h	**SH_Del_sH_R**	R/W	[7:0]	Delta_s_R[15:8] Vertical bottom delta For R channel (0<= Delta <=1)
<9.22h>	00h	**SH_Del_sL_R**	R/W	[7:0]	Delta_s_R[7:0]
<9.23h>	80h	**SH_Del_nH_R**	R/W	[7:0]	Delta_n_R[15:8] Vertical top delta For R channel (0<= Delta <=1)
<9.24h>	00h	**SH_Del_nL_R**	R/W	[7:0]	Delta_n_R[7:0]
<9.25h>	80h	**SH_Del_eH_G**	R/W	[7:0]	Delta_e_G[15:8] Horizontal right delta For G channel (0<= Delta <=1)
<9.26h>	00h	**SH_Del_eL_G**	R/W	[7:0]	Delta_e_G[7:0]
<9.27h>	80h	**SH_Del_wH_G**	R/W	[7:0]	Delta_w_G[15:8] Horizontal left delta For G channel (0<= Delta <=1)
<9.28h>	00h	**SH_Del_wL_G**	R/W	[7:0]	Delta_w_G[7:0]
<9.29h>	80h	**SH_Del_sH_G**	R/W	[7:0]	Delta_s_G[15:8] Vertical bottom delta For G channel (0<= Delta <=1)
<9.2Ah>	00h	**SH_Del_sL_G**	R/W	[7:0]	Delta_s_G[7:0]
<9.2Bh>	80h	**SH_Del_nH_G**	R/W	[7:0]	Delta_n_G[15:8] Vertical top delta For G channel (0<= Delta <=1)
<9.2Ch>	00h	**SH_Del_nL_G**	R/W	[7:0]	Delta_n_G[7:0]
<9.2Dh>	80h	**SH_Del_eH_B**	R/W	[7:0]	Delta_e_B[15:8] Horizontal right delta For B channel (0<= Delta <=1)
<9.2Eh>	00h	**SH_Del_eL_B**	R/W	[7:0]	Delta_e_B[7:0]
<9.2Fh>	80h	**SH_Del_wH_B**	R/W	[7:0]	Delta_w_B[15:8] Horizontal left delta For B channel (0<= Delta <=1)
<9.30h>	00h	**SH_Del_wL_B**	R/W	[7:0]	Delta_w_B[7:0]
<9.31h>	80h	**SH_Del_sH_B**	R/W	[7:0]	Delta_s_B[15:8] Vertical bottom delta For B channel (0<= Delta <=1)
<9.32h>	00h	**SH_Del_sL_B**	R/W	[7:0]	Delta_s_B[7:0]
<9.33h>	80h	**SH_Del_nH_B**	R/W	[7:0]	Delta_n_B[15:8] Vertical top delta For B channel (0<= Delta <=1)
<9.34h>	00h	**SH_Del_nL_B**	R/W	[7:0]	Delta_n_B[7:0]
<9.35h>	01h	**SH_VAL_R0H**	R/W	[7:4] [3:0]	Reserved SH_VAL_R0[11:8] Red Gain at 0 % of Max_radial For RGB Shading
<9.36h>	00h	**SH_VAL_R0L**	R/W	[7:0]	SH_VAL_R0[7:0] Red Gain at 0 % of Max_radial For RGB Shading
<9.37h>	01h	**SH_VAL_R1H**	R/W	[7:4] [3:0]	Reserved SH_VAL_R1[11:8] Red Gain at 20 % of Max_radial For RGB Shading
<9.38h>	00h	**SH_VAL_R1L**	R/W	[7:0]	SH_VAL_R1[7:0] Red Gain at 20 % of Max_radial For RGB Shading

Addr	Reset Value	Mnemonic	Attr	Bits	Descriptions
<9.39h>	01h	**SH_VAL_R2H**	R/W	[7:4] [3:0]	Reserved SH_VAL_R2[11:8] Red Gain at 40 % of Max_radial For RGB Shading
<9.3Ah>	00h	**SH_VAL_R2L**	R/W	[7:0]	SH_VAL_R2[7:0] Red Gain at 40 % of Max_radial For RGB Shading
<9.3Bh>	01h	**SH_VAL_R3H**	R/W	[7:4] [3:0]	Reserved SH_VAL_R3[11:8] Red Gain at 60 % of Max_radial For RGB Shading
<9.3Ch>	00h	**SH_VAL_R3L**	R/W	[7:0]	SH_VAL_R3[7:0] Red Gain at 60 % of Max_radial For RGB Shading
<9.3Dh>	01h	**SH_VAL_R4H**	R/W	[7:4] [3:0]	Reserved SH_VAL_R4[11:8] Red Gain at 70 % of Max_radial For RGB Shading
<9.3Eh>	00h	**SH_VAL_R4L**	R/W	[7:0]	SH_VAL_R4[7:0] Red Gain at 70 % of Max_radial For RGB Shading
<9.3Fh>	01h	**SH_VAL_R5H**	R/W	[7:4] [3:0]	Reserved SH_VAL_R5[11:8] Red Gain at 80 % of Max_radial For RGB Shading
<9.40h>	00h	**SH_VAL_R5L**	R/W	[7:0]	SH_VAL_R5[7:0] Red Gain at 80 % of Max_radial For RGB Shading
<9.41h>	01h	**SH_VAL_R6H**	R/W	[7:4] [3:0]	Reserved SH_VAL_R6[11:8] Red Gain at 90 % of Max_radial For RGB Shading
<9.42h>	00h	**SH_VAL_R6L**	R/W	[7:0]	SH_VAL_R6[7:0] Red Gain at 90 % of Max_radial For RGB Shading
<9.43h>	01h	**SH_VAL_R7H**	R/W	[7:4] [3:0]	Reserved SH_VAL_R7[11:8] Red Gain at 100 % of Max_radial For RGB Shading
<9.44h>	00h	**SH_VAL_R7L**	R/W	[7:0]	SH_VAL_R7[7:0] Red Gain at 100 % of Max_radial For RGB Shading
<9.45h>	01h	**SH_VAL_G0H**	R/W	[7:4] [3:0]	Reserved SH_VAL_G0[11:8] Green Gain at 0 % of Max_radial For RGB Shading
<9.46h>	00h	**SH_VAL_G0L**	R/W	[7:0]	SH_VAL_G0[7:0] Green Gain at 0 % of Max_radial For RGB Shading
<9.47h>	01h	**SH_VAL_G1H**	R/W	[7:4] [3:0]	Reserved SH_VAL_G1[11:8] Green Gain at 20 % of Max_radial For RGB Shading
<9.48h>	00h	**SH_VAL_G1L**	R/W	[7:0]	SH_VAL_G1[7:0] Green Gain at 20 % of Max_radial For RGB Shading
<9.49h>	01h	**SH_VAL_G2H**	R/W	[7:4] [3:0]	Reserved SH_VAL_G2[11:8] Green Gain at 40 % of Max_radial For RGB Shading
<9.4Ah>	00h	**SH_VAL_G2L**	R/W	[7:0]	SH_VAL_G2[7:0] Green Gain at 40 % of Max_radial For RGB Shading
<9.4Bh>	01h	**SH_VAL_G3H**	R/W	[7:4] [3:0]	Reserved SH_VAL_G3[11:8] Green Gain at 60 % of Max_radial For RGB Shading
<9.4Ch>	00h	**SH_VAL_G3L**	R/W	[7:0]	SH_VAL_G3[7:0] Green Gain at 60 % of Max_radial For RGB Shading
<9.4Dh>	01h	**SH_VAL_G4H**	R/W	[7:4] [3:0]	Reserved SH_VAL_G4[11:8] Green Gain at 70 % of Max_radial For RGB Shading
<9.4Eh>	00h	**SH_VAL_G4L**	R/W	[7:0]	SH_VAL_G4[7:0] Green Gain at 70 % of Max_radial For RGB Shading
<9.4Fh>	01h	**SH_VAL_G5H**	R/W	[7:4] [3:0]	Reserved SH_VAL_G5[11:8] Green Gain at 80 % of Max_radial For RGB Shading
<9.50h>	00h	**SH_VAL_G5L**	R/W	[7:0]	SH_VAL_G5[7:0] Green Gain at 80 % of Max_radial For RGB Shading
<9.51h>	01h	**SH_VAL_G6H**	R/W	[7:4] [3:0]	Reserved SH_VAL_G6[11:8] Green Gain at 90 % of Max_radial For RGB Shading
<9.52h>	00h	**SH_VAL_G6L**	R/W	[7:0]	SH_VAL_G6[7:0] Green Gain at 90 % of Max_radial For RGB Shading
<9.53h>	01h	**SH_VAL_G7H**	R/W	[7:4]	Reserved

Addr	Reset Value	Mnemonic	Attr	Bits	Descriptions
				[3:0]	SH_VAL_G7[11:8] Green Gain at 100 % of Max_radial For RGB Shading
<9.54h>	00h	**SH_VAL_G7L**	R/W	[7:0]	SH_VAL_G7[7:0] Green Gain at 100 % of Max_radial For RGB Shading
<9.55h>	01h	**SH_VAL_B0H**	R/W	[7:4] [3:0]	Reserved SH_VAL_B0[11:8] Blue Gain at 0 % of Max_radial For RGB Shading
<9.56h>	00h	**SH_VAL_B0L**	R/W	[7:0]	SH_VAL_B0[7:0] Blue Gain at 0 % of Max_radial For RGB Shading
<9.57h>	01h	**SH_VAL_B1H**	R/W	[7:4] [3:0]	Reserved SH_VAL_B1[11:8] Blue Gain at 20 % of Max_radial For RGB Shading
<9.58h>	00h	**SH_VAL_B1L**	R/W	[7:0]	SH_VAL_B1[7:0] Blue Gain at 20 % of Max_radial For RGB Shading
<9.59h>	01h	**SH_VAL_B2H**	R/W	[7:4] [3:0]	Reserved SH_VAL_B2[11:8] Blue Gain at 40 % of Max_radial For RGB Shading
<9.5Ah>	00h	**SH_VAL_B2L**	R/W	[7:0]	SH_VAL_B2[7:0] Blue Gain at 40 % of Max_radial For RGB Shading
<9.5Bh>	01h	**SH_VAL_B3H**	R/W	[7:4] [3:0]	Reserved SH_VAL_B3[11:8] Blue Gain at 60 % of Max_radial For RGB Shading
<9.5Ch>	00h	**SH_VAL_B3L**	R/W	[7:0]	SH_VAL_B3[7:0] Blue Gain at 60 % of Max_radial For RGB Shading
<9.5Dh>	01h	**SH_VAL_B4H**	R/W	[7:4] [3:0]	Reserved SH_VAL_B4[11:8] Blue Gain at 70 % of Max_radial For RGB Shading
<9.5Eh>	00h	**SH_VAL_B4L**	R/W	[7:0]	SH_VAL_B4[7:0] Blue Gain at 70 % of Max_radial For RGB Shading
<9.5Fh>	01h	**SH_VAL_B5H**	R/W	[7:4] [3:0]	Reserved SH_VAL_B5[11:8] Blue Gain at 80 % of Max_radial For RGB Shading
<9.60h>	00h	**SH_VAL_B5L**	R/W	[7:0]	SH_VAL_B5[7:0] Blue Gain at 80 % of Max_radial For RGB Shading
<9.61h>	01h	**SH_VAL_B6H**	R/W	[7:4] [3:0]	Reserved SH_VAL_B6[11:8] Blue Gain at 90 % of Max_radial For RGB Shading
<9.62h>	00h	**SH_VAL_B6L**	R/W	[7:0]	SH_VAL_B6[7:0] Blue Gain at 90 % of Max_radial For RGB Shading
<9.63h>	01h	**SH_VAL_B7H**	R/W	[7:4] [3:0]	Reserved SH_VAL_B7[11:8] Blue Gain at 100 % of Max_radial For RGB Shading
<9.64h>	00h	**SH_VAL_B7L**	R/W	[7:0]	SH_VAL_B7[7:0] Blue Gain at 100 % of Max_radial For RGB Shading
<9.65h>	00h	**SH_M_R2_R1H**	R/W	[7:0]	max_r2_R1[23:16] $(max\_radial)^2$ at 20 % of Max_radial For RGB Shading
<9.66h>	9Ch	**SH_M_R2_R1M**	R/W	[7:0]	max_r2_R1[15:8]
<9.67h>	40h	**SH_M_R2_R1L**	R/W	[7:0]	max_r2_R1[7:0]
<9.68h>	02h	**SH_M_R2_R2H**	R/W	[7:0]	max_r2_R2[23:16] $(max\_radial)^2$ at 40 % of Max_radial For RGB Shading
<9.69h>	71h	**SH_M_R2_R2M**	R/W	[7:0]	max_r2_R2[15:8]
<9.6Ah>	00h	**SH_M_R2_R2L**	R/W	[7:0]	max_r2_R2[7:0]
<9.6Bh>	05h	**SH_M_R2_R3H**	R/W	[7:0]	max_r2_R3[23:16] $(max\_radial)^2$ at 60 % of Max_radial For RGB Shading
<9.6Ch>	7Eh	**SH_M_R2_R3M**	R/W	[7:0]	max_r2_R3[15:8]
<9.6Dh>	40h	**SH_M_R2_R3L**	R/W	[7:0]	max_r2_R3[7:0]
<9.6Eh>	07h	**SH_M_R2_R4H**	R/W	[7:0]	max_r2_R4[23:16] $(max\_radial)^2$ at 70 % of Max_radial For RGB Shading
<9.6Fh>	7Ah	**SH_M_R2_R4M**	R/W	[7:0]	max_r2_R4[15:8]
<9.70h>	10h	**SH_M_R2_R4L**	R/W	[7:0]	max_r2_R4[7:0]

Addr	Reset Value	Mnemonic	Attr	Bits	Descriptions
<9.71h>	09h	**SH_M_R2_R5H**	R/W	[7:0]	max_r2_R5[23:16] (max_radial)^2 at 80 % of Max_radial For RGB Shading
<9.72h>	C4h	**SH_M_R2_R5M**	R/W	[7:0]	max_r2_R5[15:8]
<9.73h>	00h	**SH_M_R2_R5L**	R/W	[7:0]	max_r2_R5[7:0]
<9.74h>	0Ch	**SH_M_R2_R6H**	R/W	[7:0]	max_r2_R6[23:16] (max_radial)^2 at 90 % of Max_radial For RGB Shading
<9.75h>	5Ch	**SH_M_R2_R6M**	R/W	[7:0]	max_r2_R6[15:8]
<9.76h>	10h	**SH_M_R2_R6L**	R/W	[7:0]	max_r2_R6[7:0]
<9.77h>	0Fh	**SH_M_R2_R7H**	R/W	[7:0]	max_r2_R7[23:16] (max_radial)^2 at 100 % of Max_radial For RGB Shading
<9.78h>	42h	**SH_M_R2_R7M**	R/W	[7:0]	max_r2_R7[15:8]
<9.79h>	40h	**SH_M_R2_R7L**	R/W	[7:0]	max_r2_R7[7:0]
<9.7Ah>	00h	**SH_M_R2_G1H**	R/W	[7:0]	max_r2_G1[23:16] (max_radial)2 at 20 % of Max_radial For RGB Shading
<9.7Bh>	9Ch	**SH_M_R2_G1M**	R/W	[7:0]	max_r2_G1[15:8]
<9.7Ch>	40h	**SH_M_R2_G1L**	R/W	[7:0]	max_r2_G1[7:0]
<9.7Dh>	02h	**SH_M_R2_G2H**	R/W	[7:0]	max_r2_G2[23:16] (max_radial)2 at 40 % of Max_radial For RGB Shading
<9.7Eh>	71h	**SH_M_R2_G2M**	R/W	[7:0]	max_r2_G2[15:8]
<9.7Fh>	00h	**SH_M_R2_G2L**	R/W	[7:0]	max_r2_G2[7:0]
<9.80h>	05h	**SH_M_R2_G3H**	R/W	[7:0]	max_r2_G3[23:16] (max_radial)2 at 60 % of Max_radial For RGB Shading
<9.81h>	7Eh	**SH_M_R2_G3M**	R/W	[7:0]	max_r2_G3[15:8]
<9.82h>	40h	**SH_M_R2_G3L**	R/W	[7:0]	max_r2_G3[7:0]
<9.83h>	07h	**SH_M_R2_G4H**	R/W	[7:0]	max_r2_G4[23:16] (max_radial)2 at 70 % of Max_radial For RGB Shading
<9.84h>	7Ah	**SH_M_R2_G4M**	R/W	[7:0]	max_r2_G4[15:8]
<9.85h>	10h	**SH_M_R2_G4L**	R/W	[7:0]	max_r2_G4[7:0]
<9.86h>	09h	**SH_M_R2_G5H**	R/W	[7:0]	max_r2_G5[23:16] (max_radial)2 at 80 % of Max_radial For RGB Shading
<9.87h>	C4h	**SH_M_R2_G5M**	R/W	[7:0]	max_r2_G5[15:8]
<9.88h>	00h	**SH_M_R2_G5L**	R/W	[7:0]	max_r2_G5[7:0]
<9.89h>	0Ch	**SH_M_R2_G6H**	R/W	[7:0]	max_r2_G6[23:16] (max_radial)2 at 90 % of Max_radial For RGB Shading
<9.8Ah>	5Ch	**SH_M_R2_G6M**	R/W	[7:0]	max_r2_G6[15:8]
<9.8Bh>	10h	**SH_M_R2_G6L**	R/W	[7:0]	max_r2_G6[7:0]
<9.8Ch>	0Fh	**SH_M_R2_G7H**	R/W	[7:0]	max_r2_G7[23:16] (max_radial)2 at 100 % of Max_radial For RGB Shading
<9.8Dh>	42h	**SH_M_R2_G7M**	R/W	[7:0]	max_r2_G7[15:8]
<9.8Eh>	40h	**SH_M_R2_G7L**	R/W	[7:0]	max_r2_G7[7:0]
<9.8Fh>	00h	**SH_M_R2_B1H**	R/W	[7:0]	max_r2_B1[23:16] (max_radial)2 at 20 % of Max_radial For RGB Shading
<9.90h>	9Ch	**SH_M_R2_B1M**	R/W	[7:0]	max_r2_B1[15:8]
<9.91h>	40h	**SH_M_R2_B1L**	R/W	[7:0]	max_r2_B1[7:0]
<9.92h>	02h	**SH_M_R2_B2H**	R/W	[7:0]	max_r2_B2[23:16] (max_radial)2 at 40 % of Max_radial For RGB Shading
<9.93h>	71h	**SH_M_R2_B2M**	R/W	[7:0]	max_r2_B2[15:8]

Addr	Reset Value	Mnemonic	Attr	Bits	Descriptions
<9.94h>	00h	**SH_M_R2_B2L**	R/W	[7:0]	max_r2_B2[7:0]
<9.95h>	05h	**SH_M_R2_B3H**	R/W	[7:0]	max_r2_B3[23:16] (max_radial)2 at 60 % of Max_radial For RGB Shading
<9.96h>	7Eh	**SH_M_R2_B3M**	R/W	[7:0]	max_r2_B3[15:8]
<9.97h>	40h	**SH_M_R2_B3L**	R/W	[7:0]	max_r2_B3[7:0]
<9.98h>	07h	**SH_M_R2_B4H**	R/W	[7:0]	max_r2_B4[23:16] (max_radial)2 at 70 % of Max_radial For RGB Shading
<9.99h>	7Ah	**SH_M_R2_B4M**	R/W	[7:0]	max_r2_B4[15:8]
<9.9Ah>	10h	**SH_M_R2_B4L**	R/W	[7:0]	max_r2_B4[7:0]
<9.9Bh>	09h	**SH_M_R2_B5H**	R/W	[7:0]	max_r2_B5[23:16] (max_radial)2 at 80 % of Max_radial For RGB Shading
<9.9Ch>	C4h	**SH_M_R2_B5M**	R/W	[7:0]	max_r2_B5[15:8]
<9.9Dh>	00h	**SH_M_R2_B5L**	R/W	[7:0]	max_r2_B5[7:0]
<9.9Eh>	0Ch	**SH_M_R2_B6H**	R/W	[7:0]	max_r2_B6[23:16] (max_radial)2 at 90 % of Max_radial For RGB Shading
<9.9Fh>	5Ch	**SH_M_R2_B6M**	R/W	[7:0]	max_r2_B6[15:8]
<9.A0h>	10h	**SH_M_R2_B6L**	R/W	[7:0]	max_r2_B6[7:0]
<9.A1h>	0Fh	**SH_M_R2_B7H**	R/W	[7:0]	max_r2_B7[23:16] (max_radial)2 at 100 % of Max_radial For RGB Shading
<9.A2h>	42h	**SH_M_R2_B7M**	R/W	[7:0]	max_r2_B7[15:8]
<9.A3h>	40h	**SH_M_R2_B7L**	R/W	[7:0]	max_r2_B7[7:0]
<9.A4h>	68h	**SH_SUB_RR0H**	R/W	[7:0]	sub_range_R0[15:8] sub_range_R0 = 1 / (max_r2_R1-0)
<9.A5h>	DBh	**SH_SUB_RR0L**	R/W	[7:0]	sub_range_R0[7:0]
<9.A6h>	22h	**SH_SUB_RR1H**	R/W	[7:0]	sub_range_R1[15:8] sub_range_R1 = 1 / (max_r2_R2-max_r2_R1)
<9.A7h>	F3h	**SH_SUB_RR1L**	R/W	[7:0]	sub_range_R1[7:0]
<9.A8h>	14h	**SH_SUB_RR2H**	R/W	[7:0]	sub_range_R2[15:8] sub_range_R2 = 1 / (max_r2_R3-max_r2_R2)
<9.A9h>	F8h	**SH_SUB_RR2L**	R/W	[7:0]	sub_range_R2[7:0]
<9.AAh>	20h	**SH_SUB_RR3H**	R/W	[7:0]	sub_range_R3[15:8] sub_range_R3 = 1 / (max_r2_R4-max_r2_R3)
<9.ABh>	43h	**SH_SUB_RR3L**	R/W	[7:0]	sub_range_R3[7:0]
<9.ACh>	1Bh	**SH_SUB_RR4H**	R/W	[7:0]	sub_range_R4[15:8] sub_range_R4 = 1 / (max_r2_R5-max_r2_R4)
<9.ADh>	F6h	**SH_SUB_RR4L**	R/W	[7:0]	sub_range_R4[7:0]
<9.AEh>	18h	**SH_SUB_RR5H**	R/W	[7:0]	sub_range_R5[15:8] sub_range_R5 = 1 / (max_r2_R6-max_r2_R5)
<9.AFh>	ACh	**SH_SUB_RR5L**	R/W	[7:0]	sub_range_R5[7:0]
<9.B0h>	16h	**SH_SUB_RR6H**	R/W	[7:0]	sub_range_R6[15:8] sub_range_R6 = 1 / (max_r2_R7-max_r2_R6)
<9.B1h>	13h	**SH_SUB_RR6L**	R/W	[7:0]	sub_range_R6[7:0]
<9.B2h>	68h	**SH_SUB_RG0H**	R/W	[7:0]	sub_range_G0[15:8] sub_range_G0 = 1 / (max_r2_G1-0)
<9.B3h>	DBh	**SH_SUB_RG0L**	R/W	[7:0]	sub_range_G0[7:0]
<9.B4h>	22h	**SH_SUB_RG1H**	R/W	[7:0]	sub_range_G1[15:8] sub_range_G1 = 1 / (max_r2_G2-max_r2_G1)
<9.B5h>	F3h	**SH_SUB_RG1L**	R/W	[7:0]	sub_range_G1[7:0]
<9.B6h>	14h	**SH_SUB_RG2H**	R/W	[7:0]	sub_range_G2[15:8] sub_range_G2 = 1 / (max_r2_G3-max_r2_G2)
<9.B7h>	F8h	**SH_SUB_RG2L**	R/W	[7:0]	sub_range_G2[7:0]
<9.B8h>	20h	**SH_SUB_RG3H**	R/W	[7:0]	sub_range_G3[15:8] sub_range_G3 = 1 / (max_r2_G4-max_r2_G3)
<9.B9h>	43h	**SH_SUB_RG3L**	R/W	[7:0]	sub_range_G3[7:0]
<9.BAh>	1Bh	**SH_SUB_RG4H**	R/W	[7:0]	sub_range_G4[15:8] sub_range_G4 = 1 / (max_r2_G5-max_r2_G4)

Addr	Reset Value	Mnemonic	Attr	Bits	Descriptions
<9.BBh>	F6h	**SH_SUB_RG4L**	R/W	[7:0]	sub_range_G4[7:0]
<9.BCh>	18h	**SH_SUB_RG5H**	R/W	[7:0]	sub_range_G5[15:8] sub_range_G5 = 1 / (max_r2_G6-max_r2_G5)
<9.BDh>	ACh	**SH_SUB_RG5L**	R/W	[7:0]	sub_range_G5[7:0]
<9.BEh>	16h	**SH_SUB_RG6H**	R/W	[7:0]	sub_range_G6[15:8] sub_range_G6 = 1 / (max_r2_G7-max_r2_G6)
<9.BFh>	13h	**SH_SUB_RG6L**	R/W	[7:0]	sub_range_G6[7:0]
<9.C0h>	68h	**SH_SUB_RB0H**	R/W	[7:0]	sub_range_B0[15:8] sub_range_B0 = 1 / (max_r2_B1-0)
<9.C1h>	DBh	**SH_SUB_RB0L**	R/W	[7:0]	sub_range_B0[7:0]
<9.C2h>	22h	**SH_SUB_RB1H**	R/W	[7:0]	sub_range_B1[15:8] sub_range_B1 = 1 / (max_r2_B2-max_r2_B1)
<9.C3h>	F3h	**SH_SUB_RB1L**	R/W	[7:0]	sub_range_B1[7:0]
<9.C4h>	14h	**SH_SUB_RB2H**	R/W	[7:0]	sub_range_B2[15:8] sub_range_B2 = 1 / (max_r2_B3-max_r2_B2)
<9.C5h>	F8h	**SH_SUB_RB2L**	R/W	[7:0]	sub_range_B2[7:0]
<9.C6h>	20h	**SH_SUB_RB3H**	R/W	[7:0]	sub_range_B3[15:8] sub_range_B3 = 1 / (max_r2_B4-max_r2_B3)
<9.C7h>	43h	**SH_SUB_RB3L**	R/W	[7:0]	sub_range_B3[7:0]
<9.C8h>	1Bh	**SH_SUB_RB4H**	R/W	[7:0]	sub_range_B4[15:8] sub_range_B4 = 1 / (max_r2_B5-max_r2_B4)
<9.C9h>	F6h	**SH_SUB_RB4L**	R/W	[7:0]	sub_range_B4[7:0]
<9.CAh>	18h	**SH_SUB_RB5H**	R/W	[7:0]	sub_range_B5[15:8] sub_range_B5 = 1 / (max_r2_B6-max_r2_B5)
<9.CBh>	ACh	**SH_SUB_RB5L**	R/W	[7:0]	sub_range_B5[7:0]
<9.CCh>	16h	**SH_SUB_RB6H**	R/W	[7:0]	sub_range_B6[15:8] sub_range_B6 = 1 / (max_r2_B7-max_r2_B6)
<9.CDh>	13h	**SH_SUB_RB6L**	R/W	[7:0]	sub_range_B6[7:0]

10. SUPPRESS (PAGE 0BH)

Addr	Reset Value	Mnemonic	Attr	Bits	Descriptions
<B.00h>	20h	**DCLP_AGCMIN**	R/W	[7:0]	Minimum AGC value of Digital Clamp suppress
<B.01h>	00h	**DCLP_TH_AGCMIN**	R/W	[7:0]	DCLP threshold for AGC MIN target register <1.25h>
<B.02h>	60h	**DCLP_AGCMAX**	R/W	[7:0]	Maximum AGC value of Digital Clamp suppress
<B.03h>	10h	**DCLP_TH_AGCMAX**	R/W	[7:0]	DCLP threshold for AGC MAX
<B.04h>	80h	**YGAIN_PERCENT_LOW**	R/W	[7:0]	Y gain graph constant for Y gain suppress
<B.05h>	03h	**YGAIN_MAXVALUE_H**	R/W	[7:4] [3:0]	Reserved Maximum Y gain value high address of Y suppress [11:8]
<B.06h>	00h	**YGAIN_MAXVALUE_L**	R/W	[7:0]	Maximum Y gain value low address of Y suppress [7:0]
<B.07h>	E0h	**YGAIN_PERCENT_HIGH**	R/W	[7:0]	Y gain graph constant for Y gain suppress
<B.08h>	58h	**COLORSUPP_AGCMIN**	R/W	[7:0]	Minimum AGC value of Color Suppress
<B.09h>	03h	**COLORSUPP_COLORMIN_H**	R/W	[7:4] [3:0]	Reserved Minimum color value high address of color suppress [11:8]
<B.0Ah>	80h	**COLORSUPP_COLORMIN_L**	R/W	[7:0]	Minimum color value low address of color suppress [7:0]
<B.0Bh>	00h	**ISP_BPRM_ON_Start**	R/W	[7:0]	AGC Minimum value to start ISP BPRM
<B.0Ch>	40h	**DBPRM_TH13_AGCMIN**	R/W	[7:0]	Minimum AGC value of DBPRM threshold 1,3 suppress
<B.0Dh>	5Ah	**DBPRM_TH13_AGCMAX**	R/W	[7:0]	Maximum AGC value of DBPRM threshold 1,3 suppress
<B.0Eh>	00h	**DBPRM_TH1_MAX_H**	R/W	[7:2] [1:0]	Reserved DBPRM threshold 1 for AGC MIN [9:8] target register <1.3Eh~40h>
<B.0Fh>	20h	**DBPRM_TH1_MAX_L**	R/W	[7:0]	DBPRM threshold 1 for AGC MIN [7:0]
<B.10h>	00h	**DBPRM_TH1_MIN_H**	R/W	[7:2] [1:0]	Reserved DBPRM threshold 1 for AGC MAX [9:8]
<B.11h>	10h	**DBPRM_TH1_MIN_L**	R/W	[7:0]	DBPRM threshold 1 for AGC MAX [7:0]
<B.12h>	00h	**DBPRM_TH3_MAX_H**	R/W	[7:2] [1:0]	Reserved DBPRM threshold 3 for AGC MIN [9:8]
<B.13h>	00h	**DBPRM_TH3_MAX_L**	R/W	[7:0]	DBPRM threshold 3 for AGC MIN [7:0]
<B.14h>	FFh	**DBPRM_TH3_MIN_H**	R/W	[7:2] [1:0]	Reserved DBPRM threshold 3 for AGC MAX [9:8]
<B.15h>	FFh	**DBPRM_TH3_MIN_L**	R/W	[7:0]	DBPRM threshold 3 for AGC MAX [7:0]
<B.16h>	48h	**DBPRM_TH57_AGCMIN**	R/W	[7:0]	Minimum AGC value of DBPRM threshold 5,7 suppress
<B.17h>	60h	**DBPRM_TH57_AGCMAX**	R/W	[7:0]	Maximum AGC value of DBPRM threshold 5,7 suppress
<B.18h>	00h	**DBPRM_TH5_MAX_H**	R/W	[7:6] [5:0]	Reserved DBPRM threshold 5 for AGC MIN [13:8] target register <1.41h~44h>
<B.19h>	00h	**DBPRM_TH5_MAX_L**	R/W	[7:0]	DBPRM threshold 5 for AGC MIN [7:0]
<B.1Ah>	00h	**DBPRM_TH5_MIN_H**	R/W	[7:6]	Reserved

Addr	Reset Value	Mnemonic	Attr	Bits	Descriptions
				[5:0]	DBPRM threshold 5 for AGC MAX [13:8]
<B.1Bh>	20h	**DBPRM_TH5_MIN_L**	R/W	[7:0]	DBPRM threshold 5 for AGC MAX [7:0]
<B.1Ch>	00h	**DBPRM_TH7_MAX_H**	R/W	[7:6] [5:0]	Reserved DBPRM threshold 7 for AGC MIN [13:8]
<B.1Dh>	00h	**DBPRM_TH7_MAX_L**	R/W	[7:0]	DBPRM threshold 7 for AGC MIN [7:0]
<B.1Eh>	00h	**DBPRM_TH7_MIN_H**	R/W	[7:6] [5:0]	Reserved DBPRM threshold 7 for AGC MAX [13:8]
<B.1Fh>	20h	**DBPRM_TH7_MIN_L**	R/W	[7:0]	DBPRM threshold 7 for AGC MAX [7:0]
<B.20h>	40h	**BILINEAR_POS**	R/W	[7:0]	AGC value to start bilinear interpolation
<B.21h>	00h	**GRGB_ON_START_AGC**	R/W	[7:0]	AGC Minimum value to start GrGb suppress
<B.22h>	40h	**GRGB_NR_AGCMIN**	R/W	[7:0]	Minimum AGC value of GrGb & NR suppress
<B.23h>	60h	**GRGB_NR_AGCMAX**	R/W	[7:0]	Maximum AGC value of GrGb & NR suppress
<B.24h>	0Dh	**GRGB_GTHR_AMIN**	R/W	[7:0]	G threshold for AGC MIN target register <1.46h>
<B.25h>	20h	**GRGB_GTHR_AMAX**	R/W	[7:0]	G threshold for AGC MAX
<B.26h>	0Dh	**GRGB_RBTHR_AMIN**	R/W	[7:0]	RB threshold for AGC MIN target register <1.47h>
<B.27h>	20h	**GRGB_RBTHR_AMAX**	R/W	[7:0]	RB threshold for AGC MAX
<B.28h>	00h	**NR_ON_START_AGC**	R/W	[7:0]	AGC Minimum value to start NR suppress
<B.29h>	00h	**NR_SIGTHR01_CONST_AMIN_H**	R/W	[7:2] [1:0]	Reserved SIGTHR01_Const for AGC MIN target register <1.48h, 49h>
<B.2Ah>	14h	**NR_SIGTHR01_CONST_AMIN_L**	R/W	[7:0]	SIGTHR01_Const for AGC MIN
<B.2Bh>	00h	**NR_SIGTHR01_CONST_AMAX_H**	R/W	[7:2] [1:0]	Reserved SIGTHR01_Const for AGC MAX
<B.2Ch>	14h	**NR_SIGTHR01_CONST_AMAX_L**	R/W	[7:0]	SIGTHR01_Const for AGC MAX
<B.2Dh>	00h	**NR_PRETHR_CONST_AMIN_H**	R/W	[7:2] [1:0]	Reserved PRETHR_Const for AGC MIN target register <1.4Ah, 4Bh>
<B.2Eh>	90h	**NR_PRETHR_CONST_AMIN_L**	R/W	[7:0]	PRETHR_Const for AGC MIN
<B.2Fh>	00h	**NR_PRETHR_CONST_AMAX_H**	R/W	[7:2] [1:0]	Reserved PRETHR_Const for AGC MAX
<B.30h>	C0h	**NR_PRETHR_CONST_AMAX_L**	R/W	[7:0]	PRETHR_Const for AGC MAX
<B.31h>	00h	**NR_POSTTHR_CONST_AMIN_H**	R/W	[7:2] [1:0]	Reserved POSTTHRE_Const for AGC MIN target register <1.4Eh, 4Fh>
<B.32h>	A0h	**NR_POSTTHR_CONST_AMIN_L**	R/W	[7:0]	POSTTHRE_Const for AGC MIN
<B.33h>	00h	**NR_POSTTHR_CONST_AMAX_H**	R/W	[7:2] [1:0]	Reserved POSTTHRE_Const for AGC MAX
<B.34h>	D0h	**NR_POSTTHR_CONST_AMAX_L**	R/W	[7:0]	POSTTHRE_Const for AGC MAX

Addr	Reset Value	Mnemonic	Attr	Bits	Descriptions
<B.35h>	00h	**YLPF_ON_START_AGC**	R/W	[7:0]	AGC Minimum value to Y noise filter suppress
<B.36h>	40h	**YLPF_01_AGCMIN**	R/W	[7:0]	Minimum AGC value of YLPF_01 suppress
<B.37h>	60h	**YLPF_01_AGCMAX**	R/W	[7:0]	Maximum AGC value of YLPF_01 suppress
<B.38h>	00h	**YLPF_SIGTHR01_AMIN_H**	R/W	[7:2] [1:0]	Reserved YLPF_SIGTHR01_Const for AGC MIN target register <5.78h, 7Ah>
<B.39h>	18h	**YLPF_SIGTHR01_AMIN_L**	R/W	[7:0]	YLPF_SIGTHR01_Const for AGC MIN
<B.3Ah>	00h	**YLPF_SIGTHR01_AMAX_H**	R/W	[7:2] [1:0]	Reserved YLPF_SIGTHR01_Const for AGC MAX
<B.3Bh>	40h	**YLPF_SIGTHR01_AMAX_L**	R/W	[7:0]	YLPF_SIGTHR01_Const for AGC MAX
<B.3Ch>	50h	**YLPF_02_AGCMIN**	R/W	[7:0]	Minimum AGC value of YLPF_02 suppress
<B.3Dh>	60h	**YLPF_02_AGCMAX**	R/W	[7:0]	Maximum AGC value of YLPF_02 suppress
<B.3Eh>	00h	**YLPF_SIGTHR02_AMIN_H**	R/W	[7:2] [1:0]	Reserved YLPF_SIGTHR02_Const for AGC MIN [9:8] target register <5.79h, 7Ah>
<B.3Fh>	30h	**YLPF_SIGTHR02_AMIN_L**	R/W	[7:0]	YLPF_SIGTHR02_Const for AGC MIN [7:0]
<B.40h>	00h	**YLPF_SIGTHR02_AMAX_H**	R/W	[7:2] [1:0]	Reserved YLPF_SIGTHR02_Const for AGC MAX [9:8]
<B.41h>	40h	**YLPF_SIGTHR02_AMAX_L**	R/W	[7:0]	YLPF_SIGTHR02_Const for AGC MAX [7:0]
<B.42h>	50h	**EDGE_AGCMIN**	R/W	[7:0]	Minimum AGC value of edge suppress
<B.43h>	60h	**EDGE_AGCMAX**	R/W	[7:0]	Maximum AGC value of edge suppress
<B.44h>	00h	**POS_GAIN_HH_AMIN**	R/W	[7:2] [1:0]	Reserved POS_GAIN for AGC MIN [25:24] target register <5.2Bh~2Eh>
<B.45h>	18h	**POS_GAIN_HL_AMIN**	R/W	[7:0]	POS_GAIN for AGC MIN [23:16]
<B.46h>	00h	**POS_GAIN_LH_AMIN**	R/W	[7:0]	POS_GAIN for AGC MIN [15:8]
<B.47h>	00h	**POS_GAIN_LL_AMIN**	R/W	[7:0]	POS_GAIN for AGC MIN [7:0]
<B.48h>	00h	**POS_GAIN_HH_AMAX**	R/W	[7:2] [1:0]	Reserved POS_GAIN for AGC MAX [25:24]
<B.49h>	0Ah	**POS_GAIN_HL_AMAX**	R/W	[7:0]	POS_GAIN for AGC MAX [23:16]
<B.4Ah>	00h	**POS_GAIN_LH_AMAX**	R/W	[7:0]	POS_GAIN for AGC MAX [15:8]
<B.4Bh>	00h	**POS_GAIN_LL_AMAX**	R/W	[7:0]	POS_GAIN for AGC MAX
<B.4Ch>	00h	**NEG_GAIN_HH_AMIN**	R/W	[7:2] [1:0]	Reserved NEG_GAIN for AGC MIN [25:24] target register <5.2Fh~32h>
<B.4Dh>	18h	**NEG_GAIN_HL_AMIN**	R/W	[7:0]	NEG_GAIN for AGC MIN [23:16]
<B.4Eh>	00h	**NEG_GAIN_LH_AMIN**	R/W	[7:0]	NEG_GAIN for AGC MIN [15:8]
<B.4Fh>	00h	**NEG_GAIN_LL_AMIN**	R/W	[7:0]	NEG_GAIN for AGC MIN [7:0]
<B.50h>	00h	**NEG_GAIN_HH_AMAX**	R/W	[7:2]	Reserved

Addr	Reset Value	Mnemonic	Attr	Bits	Descriptions
				[1:0]	NEG_GAIN for AGC MAX [25:24]
<B.51h>	0Ah	**NEG_GAIN_HL_AMAX**	R/W	[7:0]	NEG_GAIN for AGC MAX [23:16]
<B.52h>	00h	**NEG_GAIN_LH_AMAX**	R/W	[7:0]	NEG_GAIN for AGC MAX [15:8]
<B.53h>	00h	**NEG_GAIN_LL_AMAX**	R/W	[7:0]	NEG_GAIN for AGC MAX [7:0]
<B.54h>	00h	**AWB_RB_OFFSET_SHT_MIN_H**	R/W	[7:0]	Minimum Cintr for AWB R,B offset suppress
<B.55h>	01h	**AWB_RB_OFFSET_SHT_MIN_L**	R/W	[7:0]	Minimum Cintr for AWB R,B offset suppress
<B.56h>	00h	**AWB_RB_OFFSET_SHT_MAX_H**	R/W	[7:0]	Maximum Cintr for AWB R,B offset suppress
<B.57h>	10h	**AWB_RB_OFFSET_SHT_MAX_L**	R/W	[7:0]	Maximum Cintr for AWB R,B offset suppress
<B.58h>	01h	**AWB_R_OFFSET_FOR_MIN**	R/W	[7:0]	AWB R offset for Cintr MIN
<B.59h>	00h	**AWB_R_OFFSET_FOR_MAX**	R/W	[7:0]	AWB R offset for Cintr MAX
<B.5Ah>	FFh	**AWB_B_OFFSET_FOR_MIN**	R/W	[7:0]	AWB B offset for Cintr MIN
<B.5Bh>	00h	**AWB_B_OFFSET_FOR_MAX**	R/W	[7:0]	AWB B offset for Cintr MAX
<B.5Ch>	5Ah	**Reserved**			
<B.5Dh>	5Ah	**Reserved**			
<B.5Eh>	5Ah	**Reserved**			
<B.5Fh>	33h	**Reserved**			
<B.60h>	04h	**COLCORR_RRR_GAINH_5000**	R/W	[7:4] [3:0]	Reserved Color Correction Coefficient for 5000K [11:8] target register <1.51h~62h>
<B.61h>	00h	**COLCORR_RRR_GAINL_5000**	R/W	[7:0]	Color Correction Coefficient for 5000K [7:0]
<B.62h>	00h	**COLCORR_RRG_GAINH_5000**	R/W	[7:4] [3:0]	Reserved Color Correction Coefficient for 5000K [11:8]
<B.63h>	00h	**COLCORR_RRG_GAINL_5000**	R/W	[7:0]	Color Correction Coefficient for 5000K [7:0]
<B.64h>	00h	**COLCORR_RRB_GAINH_5000**	R/W	[7:4] [3:0]	Reserved Color Correction Coefficient for 5000K [11:8]
<B.65h>	00h	**COLCORR_RRB_GAINL_5000**	R/W	[7:0]	Color Correction Coefficient for 5000K [7:0]
<B.66h>	00h	**COLCORR_RGR_GAINH_5000**	R/W	[7:4] [3:0]	Reserved Color Correction Coefficient for 5000K [11:8]
<B.67h>	00h	**COLCORR_RGR_GAINL_5000**	R/W	[7:0]	Color Correction Coefficient for 5000K [7:0]
<B.68h>	04h	**COLCORR_RGG_GAINH_5000**	R/W	[7:4] [3:0]	Reserved Color Correction Coefficient for 5000K [11:8]
<B.69h>	00h	**COLCORR_RGG_GAINL_5000**	R/W	[7:0]	Color Correction Coefficient for 5000K [7:0]
<B.6Ah>	00h	**COLCORR_RGB_GAINH_5000**	R/W	[7:4] [3:0]	Reserved Color Correction Coefficient for 5000K [11:8]
<B.6Bh>	00h	**COLCORR_RGB_GAINL_5000**	R/W	[7:0]	Color Correction Coefficient for 5000K [7:0]
<B.6Ch>	00h	**COLCORR_RBR_GAINH_5000**	R/W	[7:4] [3:0]	Reserved Color Correction Coefficient for 5000K [11:8]
<B.6Dh>	00h	**COLCORR_RBR_GAINL_5000**	R/W	[7:0]	Color Correction Coefficient for 5000K [7:0]
<B.6Eh>	00h	**COLCORR_RBG_GAINH_5000**	R/W	[7:4] [3:0]	Reserved Color Correction Coefficient for 5000K [11:8]
<B.6Fh>	00h	**COLCORR_RBG_GAINL_5000**	R/W	[7:0]	Color Correction Coefficient for 5000K [7:0]

Addr	Reset Value	Mnemonic	Attr	Bits	Descriptions
<B.70h>	04h	**COLCORR_RBB_GAINH_5000**	R/W	[7:4] [3:0]	Reserved Color Correction Coefficient for 5000K [11:8]
<B.71h>	00h	**COLCORR_RBB_GAINL_5000**	R/W	[7:0]	Color Correction Coefficient for 5000K [7:0]
<B.72h>	05h	**COLCORR_RRR_GAINH_3000**	R/W	[7:4] [3:0]	Reserved Color Correction Coefficient for 3000K [11:8]
<B.73h>	00h	**COLCORR_RRR_GAINL_3000**	R/W	[7:0]	Color Correction Coefficient for 3000K [7:0]
<B.74h>	00h	**COLCORR_RRG_GAINH_3000**	R/W	[7:4] [3:0]	Reserved Color Correction Coefficient for 3000K [11:8]
<B.75h>	00h	**COLCORR_RRG_GAINL_3000**	R/W	[7:0]	Color Correction Coefficient for 3000K [7:0]
<B.76h>	00h	**COLCORR_RRB_GAINH_3000**	R/W	[7:4] [3:0]	Reserved Color Correction Coefficient for 3000K [11:8]
<B.77h>	00h	**COLCORR_RRB_GAINL_3000**	R/W	[7:0]	Color Correction Coefficient for 3000K [7:0]
<B.78h>	00h	**COLCORR_RGR_GAINH_3000**	R/W	[7:4] [3:0]	Reserved Color Correction Coefficient for 3000K [11:8]
<B.79h>	00h	**COLCORR_RGR_GAINL_3000**	R/W	[7:0]	Color Correction Coefficient for 3000K [7:0]
<B.7Ah>	05h	**COLCORR_RGG_GAINH_3000**	R/W	[7:4] [3:0]	Reserved Color Correction Coefficient for 3000K [11:8]
<B.7Bh>	00h	**COLCORR_RGG_GAINL_3000**	R/W	[7:0]	Color Correction Coefficient for 3000K [7:0]
<B.7Ch>	00h	**COLCORR_RGB_GAINH_3000**	R/W	[7:4] [3:0]	Reserved Color Correction Coefficient for 3000K [11:8]
<B.7Dh>	00h	**COLCORR_RGB_GAINL_3000**	R/W	[7:0]	Color Correction Coefficient for 3000K [7:0]
<B.7Eh>	00h	**COLCORR_RBR_GAINH_3000**	R/W	[7:4] [3:0]	Reserved Color Correction Coefficient for 3000K [11:8]
<B.7Fh>	00h	**COLCORR_RBR_GAINL_3000**	R/W	[7:0]	Color Correction Coefficient for 3000K [7:0]
<B.80h>	00h	**COLCORR_RBG_GAINH_3000**	R/W	[7:4] [3:0]	Reserved Color Correction Coefficient for 3000K [11:8]
<B.81h>	00h	**COLCORR_RBG_GAINL_3000**	R/W	[7:0]	Color Correction Coefficient for 3000K [7:0]
<B.82h>	05h	**COLCORR_RBB_GAINH_3000**	R/W	[7:4] [3:0]	Reserved Color Correction Coefficient for 3000K [11:8]
<B.83h>	00h	**COLCORR_RBB_GAINL_3000**	R/W	[7:0]	Color Correction Coefficient for 3000K [7:0]
<B.84h>	06h	**COLCORR_RRR_GAINH_2000**	R/W	[7:4] [3:0]	Reserved Color Correction Coefficient for 2000K [11:8]
<B.85h>	00h	**COLCORR_RRR_GAINL_2000**	R/W	[7:0]	Color Correction Coefficient for 2000K [7:0]
<B.86h>	00h	**COLCORR_RRG_GAINH_2000**	R/W	[7:4] [3:0]	Reserved Color Correction Coefficient for 2000K [11:8]
<B.87h>	00h	**COLCORR_RRG_GAINL_2000**	R/W	[7:0]	Color Correction Coefficient for 2000K [7:0]
<B.88h>	00h	**COLCORR_RRB_GAINH_2000**	R/W	[7:4] [3:0]	Reserved Color Correction Coefficient for 2000K [11:8]
<B.89h>	00h	**COLCORR_RRB_GAINL_2000**	R/W	[7:0]	Color Correction Coefficient for 2000K [7:0]
<B.8Ah>	00h	**COLCORR_RGR_GAINH_2000**	R/W	[7:4] [3:0]	Reserved Color Correction Coefficient for 2000K [11:8]
<B.8Bh>	00h	**COLCORR_RGR_GAINL_2000**	R/W	[7:0]	Color Correction Coefficient for 2000K [7:0]

Addr	Reset Value	Mnemonic	Attr	Bits	Descriptions
<B.8Ch>	06h	**COLCORR_RGG_GAINH_2000**	R/W	[7:4] [3:0]	Reserved Color Correction Coefficient for 2000K [11:8]
<B.8Dh>	00h	**COLCORR_RGG_GAINL_2000**	R/W	[7:0]	Color Correction Coefficient for 2000K [7:0]
<B.8Eh>	00h	**COLCORR_RGB_GAINH_2000**	R/W	[7:4] [3:0]	Reserved Color Correction Coefficient for 2000K [11:8]
<B.8Fh>	00h	**COLCORR_RGB_GAINL_2000**	R/W	[7:0]	Color Correction Coefficient for 2000K [7:0]
<B.90h>	00h	**COLCORR_RBR_GAINH_2000**	R/W	[7:4] [3:0]	Reserved Color Correction Coefficient for 2000K [11:8]
<B.91h>	00h	**COLCORR_RBR_GAINL_2000**	R/W	[7:0]	Color Correction Coefficient for 2000K [7:0]
<B.92h>	00h	**COLCORR_RBG_GAINH_2000**	R/W	[7:4] [3:0]	Reserved Color Correction Coefficient for 2000K [11:8]
<B.93h>	00h	**COLCORR_RBG_GAINL_2000**	R/W	[7:0]	Color Correction Coefficient for 2000K [7:0]
<B.94h>	06h	**COLCORR_RBB_GAINH_2000**	R/W	[7:4] [3:0]	Reserved Color Correction Coefficient for 2000K [11:8]
<B.95h>	00h	**COLCORR_RBB_GAINL_2000**	R/W	[7:0]	Color Correction Coefficient for 2000K [7:0]
<B.96h>	10h	**COLCORR_T_AGC_MIN**	R/W	[7:0]	Minimum AGC value of color correction T gain suppress
<B.97h>	50h	**COLCORR_T_AGC_MAX**	R/W	[7:0]	Maximum AGC value of color correction T gain suppress
<B.98h>	FFh	**COLCORR_T_GAIN_AMIN**	R/W	[7:0]	Color correction T gain of R for AGC_MIN from 0x00 to 0xFF (0xFF is 1.00)
<B.99h>	20h	**COLCORR_T_GAIN_AMAX**	R/W	[7:0]	Color correction T gain of R for AGC_MAX
<B.9Ah>	00h	**RGB_SHD_T1_K1_POS_H**	R/W	[7:0]	K1 position_H(AWB_R) value of RGB shading T1 gain suppress
<B.9Bh>	EEh	**RGB_SHD_T1_K1_POS_L**	R/W	[7:0]	K1 position_L(AWB_R) value of RGB shading T1 gain suppress
<B.9Ch>	00h	**RGB_SHD_T1_K2_POS_H**	R/W	[7:0]	K2 position_H(AWB_R) value of RGB shading T1 gain suppress
<B.9Dh>	C2h	**RGB_SHD_T1_K2_POS_L**	R/W	[7:0]	K2 position_L(AWB_R) value of RGB shading T1 gain suppress
<B.9Eh>	00h	**RGB_SHD_T1_K3_POS_H**	R/W	[7:0]	K3 position_H(AWB_R) value of RGB shading T1 gain suppress
<B.9Fh>	B2h	**RGB_SHD_T1_K3_POS_L**	R/W	[7:0]	K3 position_L(AWB_R) value of RGB shading T1 gain suppress
<B.A0h>	03h	**RGB_SHD_T1_GAIN_R_K1_H**	R/W	[7:0]	RGB shading T1 gain_H of R for K1
<B.A1h>	00h	**RGB_SHD_T1_GAIN_R_K1_L**	R/W	[7:0]	RGB shading T1 gain_L of R for K1 from 0x000 to 0x300 (0x300 is 3.00)
<B.A2h>	03h	**RGB_SHD_T1_GAIN_G_K1_H**	R/W	[7:0]	RGB shading T1 gain_H of G for K1
<B.A3h>	00h	**RGB_SHD_T1_GAIN_G_K1_L**	R/W	[7:0]	RGB shading T1 gain_L of G for K1
<B.A4h>	03h	**RGB_SHD_T1_GAIN_B_K1_H**	R/W	[7:0]	RGB shading T1 gain_H of B for K1
<B.A5h>	00h	**RGB_SHD_T1_GAIN_B_K1_L**	R/W	[7:0]	RGB shading T1 gain_L of B for K1
<B.A6h>	03h	**RGB_SHD_T1_GAIN_Gb_r_K1_H**	R/W	[7:0]	RGB shading T1 gain_H of Gb_r for K1
<B.A7h>	00h	**RGB_SHD_T1_GAIN_Gb_r_K1_L**	R/W	[7:0]	RGB shading T1 gain_L of Gb_r for K1
<B.A8h>	02h	**RGB_SHD_T1_GAIN_R_K2_H**	R/W	[7:0]	RGB shading T1 gain_H of R for K2
<B.A9h>	00h	**RGB_SHD_T1_GAIN_R_K2_L**	R/W	[7:0]	RGB shading T1 gain_L of R for K2
<B.AAh>	02h	**RGB_SHD_T1_GAIN_G_K2_H**	R/W	[7:0]	RGB shading T1 gain_H of G for K2
<B.ABh>	00h	**RGB_SHD_T1_GAIN_G_K2_L**	R/W	[7:0]	RGB shading T1 gain_L of G for K2
<B.ACh>	02h	**RGB_SHD_T1_GAIN_B_K2_H**	R/W	[7:0]	RGB shading T1 gain_H of B for K2
<B.ADh>	00h	**RGB_SHD_T1_GAIN_B_K2_L**	R/W	[7:0]	RGB shading T1 gain_L of B for K2

Addr	Reset Value	Mnemonic	Attr	Bits	Descriptions
<B.AEh>	02h	**RGB_SHD_T1_GAIN_Gb_r_K2_H**	R/W	[7:0]	RGB shading T1 gain_H of Gb_r for K2
<B.AFh>	00h	**RGB_SHD_T1_GAIN_Gb_r_K2_L**	R/W	[7:0]	RGB shading T1 gain_L of Gb_r for K2
<B.B0h>	01h	**RGB_SHD_T1_GAIN_R_K3_H**	R/W	[7:0]	RGB shading T1 gain_H of R for K3
<B.B1h>	00h	**RGB_SHD_T1_GAIN_R_K3_L**	R/W	[7:0]	RGB shading T1 gain_L of R for K3
<B.B2h>	01h	**RGB_SHD_T1_GAIN_G_K3_H**	R/W	[7:0]	RGB shading T1 gain_H of G for K3
<B.B3h>	00h	**RGB_SHD_T1_GAIN_G_K3_L**	R/W	[7:0]	RGB shading T1 gain_L of G for K3
<B.B4h>	01h	**RGB_SHD_T1_GAIN_B_K3_H**	R/W	[7:0]	RGB shading T1 gain_H of B for K3
<B.B5h>	00h	**RGB_SHD_T1_GAIN_B_K3_L**	R/W	[7:0]	RGB shading T1 gain_L of B for K3
<B.B6h>	01h	**RGB_SHD_T1_GAIN_Gb_r_K3_H**	R/W	[7:0]	RGB shading T1 gain_H of Gb_r for K3
<B.B7h>	00h	**RGB_SHD_T1_GAIN_Gb_r_K3_L**	R/W	[7:0]	RGB shading T1 gain_L of Gb_r for K3
<B.B8h>	10h	**RGB_SHD_T2_AGC_MIN**	R/W	[7:0]	Minimum AGC value of RGB shading T2 gain suppress
<B.B9h>	50h	**RGB_SHD_T2_AGC_MAX**	R/W	[7:0]	Maximum AGC value of RGB shading T2 gain suppress
<B.BAh>	FFh	**RGB_SHD_T2_GAIN_R_AMIN**	R/W	[7:0]	RGB shading T2 gain of R for AGC_MIN from 0x00 to 0xFF (0xFF is 1.00)
<B.BBh>	20h	**RGB_SHD_T2_GAIN_R_AMAX**	R/W	[7:0]	RGB shading T2 gain of R for AGC_MAX
<B.BCh>	FFh	**RGB_SHD_T2_GAIN_G_AMIN**	R/W	[7:0]	RGB shading T2 gain of G for AGC_MIN
<B.BDh>	20h	**RGB_SHD_T2_GAIN_G_AMAX**	R/W	[7:0]	RGB shading T2 gain of G for AGC_MAX
<B.BEh>	FFh	**RGB_SHD_T2_GAIN_B_AMIN**	R/W	[7:0]	RGB shading T2 gain of B for AGC_MIN
<B.BFh>	20h	**RGB_SHD_T2_GAIN_B_AMAX**	R/W	[7:0]	RGB shading T2 gain of B for AGC_MAX
<B.C0h>	FFh	**RGB_SHD_T2_GAIN_Gb_r_AMIN**	R/W	[7:0]	RGB shading T2 gain of Gb_r for AGC_MIN
<B.C1h>	20h	**RGB_SHD_T2_GAIN_Gb_r_AMAX**	R/W	[7:0]	RGB shading T2 gain of Gb_r for AGC_MAX
<B.C2h>	04h	**COLCORR_T_SUPP_RRR_H**	R/W	[7:4] [3:0]	Reserved Color correction T gain suppress coefficient [11:8]
<B.C3h>	00h	**COLCORR_T_SUPP_RRR_L**	R/W	[7:0]	Color correction T gain suppress coefficient [7:0]
<B.C4h>	00h	**COLCORR_T_SUPP_RRG_H**	R/W	[7:4] [3:0]	Reserved Color correction T gain suppress coefficient [11:8]
<B.C5h>	00h	**COLCORR_T_SUPP_RRG_L**	R/W	[7:0]	Color correction T gain suppress coefficient [7:0]
<B.C6h>	00h	**COLCORR_T_SUPP_RRB_H**	R/W	[7:4] [3:0]	Reserved Color correction T gain suppress coefficient [11:8]
<B.C7h>	00h	**COLCORR_T_SUPP_RRB_L**	R/W	[7:0]	Color correction T gain suppress coefficient [7:0]
<B.C8h>	00h	**COLCORR_T_SUPP_RGR_H**	R/W	[7:4] [3:0]	Reserved Color correction T gain suppress coefficient [11:8]
<B.C9h>	00h	**COLCORR_T_SUPP_RGR_L**	R/W	[7:0]	Color correction T gain suppress coefficient [7:0]
<B.CAh>	04h	**COLCORR_T_SUPP_RGG_H**	R/W	[7:4] [3:0]	Reserved Color correction T gain suppress coefficient [11:8]
<B.CBh>	00h	**COLCORR_T_SUPP_RGG_L**	R/W	[7:0]	Color correction T gain suppress coefficient [7:0]
<B.CCh>	00h	**COLCORR_T_SUPP_RGB_H**	R/W	[7:4] [3:0]	Reserved Color correction T gain suppress coefficient [11:8]
<B.CDh>	00h	**COLCORR_T_SUPP_RGB_L**	R/W	[7:0]	Color correction T gain suppress coefficient [7:0]
<B.CEh>	00h	**COLCORR_T_SUPP_RBR_H**	R/W	[7:4] [3:0]	Reserved Color correction T gain suppress coefficient [11:8]

Addr	Reset Value	Mnemonic	Attr	Bits	Descriptions
<B.CFh>	00h	**COLCORR_T_SUPP_RBR_L**	R/W	[7:0]	Color correction T gain suppress coefficient [7:0]
<B.D0h>	00h	**COLCORR_T_SUPP_RBG_H**	R/W	[7:4] [3:0]	Reserved Color correction T gain suppress coefficient [11:8]
<B.D1h>	00h	**COLCORR_T_SUPP_RBG_L**	R/W	[7:0]	Color correction T gain suppress coefficient [7:0]
<B.D2h>	04h	**COLCORR_T_SUPP_RBB_H**	R/W	[7:4] [3:0]	Reserved Color correction T gain suppress coefficient [11:8]
<B.D3h>	00h	**COLCORR_T_SUPP_RBB_L**	R/W	[7:0]	Color correction T gain suppress coefficient [7:0]
<B.D4h>	40h	**CLPF_SUPP_AGCMIN**	R/W	[7:0]	Minimum AGC value of CLPF suppress
<B.D5h>	60h	**CLPF_SUPP_AGCMAX**	R/W	[7:0]	Maximum AGC value of CLPF suppress
<B.D6h>	B0h	**CLPF_SIGTHR01_AMIN**	R/W	[7:0]	CLPF SIGTHR01 for AGCMIN target register <5.6Eh>
<B.D7h>	F0h	**CLPF_SIGTHR01_AMAX**	R/W	[7:0]	CLPF SIGTHR01 for AGCMAX
<B.D8h>	B0h	**CLPF_SIGTHR02_AMIN**	R/W	[7:0]	CLPF SIGTHR02 for AGCMIN target register <5.6Fh>
<B.D9h>	F0h	**CLPF_SIGTHR02_AMAX**	R/W	[7:0]	CLPF SIGTHR02 for AGCMAX
<B.DAh>	00h	**X_SHD_T0_POS_H**	R/W	[7:0]	Color temporature that is determined X-shading coefficient (R Gain H)
<B.DBh>	C2h	**X_SHD_T0_POS_L**	R/W	[7:0]	Color temporature that is determined X-shading coefficient (R Gain L)
<B.DCh>	00h	**X_SHD_TC_POS_H**	R/W	[7:0]	Color temporature that is set X-shading coefficient to zero (R Gain H)
<B.DDh>	EEh	**X_SHD_TC_POS_L**	R/W	[7:0]	Color temporature that is set X-shading coefficient to zero (R Gain L)
<B.DEh>	FFh	**X_SHD_ZGAIN_VALUE**	R/W	[7:0]	X Shading gain for Zoom (x1 = 0xFF)

11. AF REGISTER MAP(1) (PAGE 0EH)

Addr	Reset Value	Mnemonic	Attr	Bits	Descriptions
<E.00h>	77h	**AF_F1_W1_SUM_LL**	R	[7:0]	Output of Window 1 of AF filter 1(LSB)
<E.01h>	55h	**AF_F1_W1_SUM_LH**	R	[7:0]	Output of Window 1 of AF filter 1
<E.02h>	28h	**AF_F1_W1_SUM_HL**	R	[7:0]	Output of Window 1 of AF filter 1
<E.03h>	00h	**AF_F1_W1_SUM_HH**	R	[7:0]	Output of Window 1 of AF filter 1(MSB)
<E.04h>	77h	**AF_F2_W1_SUM_LL**	R	[7:0]	Output of Window 1 of AF filter 2(LSB)
<E.05h>	55h	**AF_F2_W1_SUM_LH**	R	[7:0]	Output of Window 1 of AF filter 2
<E.06h>	28h	**AF_F2_W1_SUM_HL**	R	[7:0]	Output of Window 1 of AF filter 2
<E.07h>	00h	**AF_F2_W1_SUM_HH**	R	[7:0]	Output of Window 1 of AF filter 2(MSB)
<E.08h>	10h	**AF_F1_W1_PEAK_L**	R	[7:0]	Peak value of Window 1 of AF filter 1 (LSB)
<E.09h>	2Bh	**AF_F1_W1_PEAK_M**	R	[7:0]	Peak value of Window 1 of AF filter 1
<E.0Ah>	01h	**AF_F1_W1_PEAK_H**	R	[7:0]	Peak value of Window 1 of AF filter 1 (MSB)
<E.0Bh>		**Reserved**		[7:0]	
<E.0Ch>	10h	**AF_F2_W1_PEAK_L**	R	[7:0]	Peak value of Window 1 of AF filter 2 (LSB)
<E.0Dh>	2Bh	**AF_F2_W1_PEAK_M**	R	[7:0]	Peak value of Window 1 of AF filter 2
<E.0Eh>	01h	**AF_F2_W1_PEAK_H**	R	[7:0]	Peak value of Window 1 of AF filter 2 (MSB)
<E.0Fh>		**Reserved**		[7:0]	
<E.10h>	58h	**AF_F1_W2_SUM_LL**	R	[7:0]	Output of Window 2 of AF filter 1(LSB)
<E.11h>	0Bh	**AF_F1_W2_SUM_LH**	R	[7:0]	Output of Window 2 of AF filter 1
<E.12h>	00h	**AF_F1_W2_SUM_HL**	R	[7:0]	Output of Window 2 of AF filter 1
<E.13h>	00h	**AF_F1_W2_SUM_HH**	R	[7:0]	Output of Window 2 of AF filter 1(MSB)
<E.14h>	58h	**AF_F2_W2_SUM_LL**	R	[7:0]	Output of Window 2 of AF filter 2(LSB)
<E.15h>	0Bh	**AF_F2_W2_SUM_LH**	R	[7:0]	Output of Window 2 of AF filter 2
<E.16h>	00h	**AF_F2_W2_SUM_HL**	R	[7:0]	Output of Window 2 of AF filter 2
<E.17h>	00h	**AF_F2_W2_SUM_HH**	R	[7:0]	Output of Window 2 of AF filter 2(MSB)
<E.18h>	5Fh	**AF_F1_W2_PEAK_L**	R	[7:0]	Peak value of Window 2 of AF filter 1 (LSB)
<E.19h>	01h	**AF_F1_W2_PEAK_M**	R	[7:0]	Peak value of Window 2 of AF filter 1
<E.1Ah>	00h	**AF_F1_W2_PEAK_H**	R	[7:0]	Peak value of Window 2 of AF filter 1 (MSB)
<E.1Bh>		**Reserved**		[7:0]	
<E.1Ch>	5Fh	**AF_F2_W2_PEAK_L**	R	[7:0]	Peak value of Window 2 of AF filter 2 (LSB)
<E.1Dh>	01h	**AF_F2_W2_PEAK_M**	R	[7:0]	Peak value of Window 2 of AF filter 2
<E.1Eh>	00h	**AF_F2_W2_PEAK_H**	R	[7:0]	Peak value of Window 2 of AF filter 2 (MSB)
<E.1Fh>		**Reserved**		[7:0]	
<E.20h>	D2h	**AF_FILT_CLIP_WIN1_L**	R	[7:0]	Filter Clip value of Windows 1 (LSB)
<E.21h>	2Ch	**AF_FILT_CLIP_WIN1_M**	R	[7:0]	Filter Clip value of Windows 1

Addr	Reset Value	Mnemonic	Attr	Bits	Descriptions
<E.22h>	00h	**AF_FILT_CLIP_WIN1_H**	R	[7:0]	Filter Clip value of Windows 1 (MSB)
<E.23h>		**Reserved**		[7:0]	
<E.24h>	00h	**AF_FILT_CLIP_WIN2_L**	R	[7:0]	Filter Clip value of Windows 2 (LSB)
<E.25h>	00h	**AF_FILT_CLIP_WIN2_M**	R	[7:0]	Filter Clip value of Windows 2
<E.26h>	00h	**AF_FILT_CLIP_WIN2_H**	R	[7:0]	Filter Clip value of Windows 2 (MSB)
<E.27h>		**Reserved**		[7:0]	
<E.28h>	5Eh	**AF_F3_W1_PEAK_L**	R	[7:0]	Peak value of Window 1 of AF filter 3 (LSB)
<E.29h>	13h	**AF_F3_W1_PEAK_M**	R	[7:0]	Peak value of Window 1 of AF filter 3
<E.2Ah>	00h	**AF_F3_W1_PEAK_H**	R	[7:0]	Peak value of Window 1 of AF filter 3 (MSB)
<E.2Bh>		**Reserved**		[7:0]	
<E.2Ch>	85hh	**AF_F3_W2_PEAK_L**	R	[7:0]	Peak value of Window 2 of AF filter 3 (LSB)
<E.2Dh>	00h	**AF_F3_W2_PEAK_M**	R	[7:0]	Peak value of Window 2 of AF filter 3
<E.2Eh>	00h	**AF_F3_W2_PEAK_H**	R	[7:0]	Peak value of Window 2 of AF filter 3 (MSB)
<E.2Fh>		**Reserved**		[7:0]	
<E.30h>	B3h	**AF_F3_W1_SUM_LL**	R	[7:0]	Output of Window 1 of AF filter 3(LSB)
<E.31h>	DBh	**AF_F3_W1_SUM_LH**	R	[7:0]	Output of Window 1 of AF filter 3
<E.32h>	07h	**AF_F3_W1_SUM_HL**	R	[7:0]	Output of Window 1 of AF filter 3
<E.33h>	00h	**AF_F3_W1_SUM_HH**	R	[7:0]	Output of Window 1 of AF filter 3(MSB)
<E.34h>	A5h	**AF_F3_W2_SUM_LL**	R	[7:0]	Output of Window 2 of AF filter 3(LSB)
<E.35h>	0Fh	**AF_F3_W2_SUM_LH**	R	[7:0]	Output of Window 2 of AF filter 3
<E.36h>	00h	**AF_F3_W2_SUM_HL**	R	[7:0]	Output of Window 2 of AF filter 3
<E.37h>	00h	**AF_F3_W2_SUM_HH**	R	[7:0]	Output of Window 2 of AF filter 3(MSB)

12. AF REGISTER MAP(2) (PAGE 13H)

Addr	Reset Value	Mnemonic	Attr	Bits	Descriptions
<13.00h -09h>	00h	**Reserved**		[7:0]	Reserved
<13.0Ah>	00h	**AF Error**	R	[7:5] [4] [3] [2:1] [0]	Reserved 1b : Error during AF parameter initialization (invalid parameter is specified) - port setting error : duplication. 1b : Error during AF parameter initialization (invalid parameter is specified) - Photo interrupt no detect Reserved 1b : Error during actuator initialization * If the value of this register is 00h, it means "No Error"
<13.0Bh>	00h	**AF Driver Status**	R	[7:5] [4] [3] [2] [1] [0]	Reserved PI indicator : when you use manual focus with 07h / 17h command without detecting home position. This indicator informs home position detected or not 1b : Actuator “Power On” indicator flag. Set when the actuator is powered on. (Ex : continuous AF by internal algorithm) 1b : Actuator “Busy” indicator flag. Set when the actuator is moving. Reserved Actuator “Initialized” indicator flag. 1b : Set after the actuator is properly initialized. * If the value of this register is 00h, it means "Before initializing driver" or "Not defined"
<13.0Ch>	00h	**AF Operation Status**	R	[7:0]	AF operation status code 00h : Before initializing AF 01h : AF is idle 02h : AF operation is in process 03h : Low confidence – sharpness statistics does not have well defined maximum. This status code is reported when there is high probability of AF error. At that time, user can select forcely moving position. Refer to "Low confidence position" 04h : AF operation was successful 05h : AF operation was automatically terminated due to large change in scene (Brightness, Focus Value or etc) 06h : AF operation did not start because of unstable AE 07h : AF operation was successful. the searched position is start or end position. That is, there is no peak of mountain, The focus values is just continuously increasing or decreasing.. 10h : peak confirm before moving to best focus position

Addr	Reset Value	Mnemonic	Attr	Bits	Descriptions
<13.0Dh>	00h	**AF Speed Monitor**	R	[7:0]	It is an indicator of AF speed as frame number after One-Shot AF
<13.0Eh>	00h	**Spot Indicator**	R	[7:1] [0]	Reserved Indicator spot case or not 0b : It isn't spot case or set to off sopt avoidance 1b : It Is spot case
<13.0Fh>	00h	**AF Mode**	R	[7:0]	Current AF command: 01h : initial AF 02h : Move to initial wanted position (mistake at first version) 03h : single AF 04h : Manual focus 06h : Pseudo continous AF
<13.10h>		**Reserved**		[7:0]	
<13.11h>		**Reserved**		[7:0]	
<13.12h>	0Eh	**Searching Option**	R/W	[7] [6] [5] [4] [3] [2] [1] [0]	AE On/Off during focusing 0b : Off AE during focusing 1b : On AE during focusing (sometimes needed for evaluation) AWB On/Off during focusing 0b : Off AWB during focusing 1b : On AWB during focusing (sometimes needed for evaluation) When searching focus position, how to refer position 0b : With using lens position table 1b : With using linear step specified Macro mode : Searching from macro start position to end lens position 0b : Off macro mode - searching full range (start position ~ end position) 1b : On macro mode Global/Local search selection (adopt to pseudo-continuous AF and stepping motor) 0b : Global search is used (coarse search starts from start position) 1b : Local search is used (coarse search starts from last AF position) Coarse searching option2) 0b : dual fly-back to coarse search maximum (compensate hysteresis) 1b : fly-back to create search maximum (no hysteresis compensation) Fine searching option after coarse searching2) 0b : dual fly-back to coarse search maximum (compensate hysteresis) 1b : fly-back to create search maximum (no hysteresis compensation) Fine searching On/Off 0b : Fine Searching Off 1b : Fine Searching On -> drive back to coarse search maximum followed by fine search

Addr	Reset Value	Mnemonic	Attr	Bits	Descriptions
					in this neighborhood
<13.13h>		**Reserved**		[7:0]	
<13.14h>	5Ah	**Direction Threshold (Peak Sensitivity)**	R/W	[7] [6:0]	Reserved Default value is 90%(5Ah) This threshold decides to go which dirrection for searching. Peak sensitivity of the search algorithm. This parameter is used for AF statistics peak detection for early coarse search algorithm stopping. Higher values of this parameter make the search algorithm more sensitive to smaller peaks. This may result in faster AF performance, but also increase the probability of false (local maximum) peak detection. When this parameter is set to zero the full global search will be performed.
<13.15h>	33h	**AF Control**	R/W	[7] [6:5] [4] [3] [2] [1] [0]	AE histogram check ON/OFF (0: off, 1: on) for spot avoidance Spot searching option 00h : Off spot avoidance 01h : On spot avoidance 02h : Automatic change on/off for spot avoidance Go to peak directly in pseudo continuous AF mode 0b : no directly 1b : directly Enables “safe AE timing” to synchronize actuator movements and AF operation in low light. When safe AE timing is ON the AF algorithm always skips 1 frame statistics in low light conditions after the actuator completed its motion. This is necessary to make sure that AF statistics is not affected by lens motion. “Safe AE timing” may result in slower but more reliable AF operation in low light. When this option is OFF then in both highlight and low light conditions the AF algorithm tries to calculate (using AE data) if AF statistics was affected by the motion or not. Enables AE stability check before starting AF operation. If this bit is set the AF will start only if AE is stable. Enable “AE Tracking” during AF operation. When “AE Tracking” is enabled the AF operation will terminate if large change is detected in scene brightness. When this flag is set AF algorithm may terminate early if the brightness of the scene has changed significantly. This feature may be used to stop Single shot AF in case the scene has changed. 2D/1D AF filter selection. When this bit is set to 1 the 2D AF filter will be used for focusing. When this bit is set to 0, the 1-D AF filter will be used for focusing.
<13.16h>		**Reserved**		[7:0]	
<13.17h>		**Reserved**		[7:0]	
<13.18h>		**Reserved**		[7:0]	
<13.19h>		**Reserved**		[7:0]	

Addr	Reset Value	Mnemonic	Attr	Bits	Descriptions
<13.1Ah>	00h	**Response Time Delay**	R/W	[7:3] [2:0]	Reserved Actuator respose time (unit=frame) In test mode, this register means delay. Timer uses 2 times unit. (ex : if timer set 500us, this unit is (ms))
<13.1Bh>		**Reserved**		[7:0]	
<13.1Ch>		**Reserved**		[7:0]	
<13.1Dh>		**Reserved**		[7:0]	
<13.1Eh>	05h	**Inner Window Confidence Threshold**	R/W	[7:0]	confidence threshold in inner window (max/avg). Unit : % percentage
<13.1Fh>	03h	**Outer Window Confidence Threshold**	R/W	[7:0]	confidence threshold in outer window (max/avg). Unit : % percentage
<13.20h>		**Reserved**		[7:0]	
<13.21h>	07h	**AE tracker (low Y)**	R/W	[7:0]	Low-light condition threshold increase to limit scene brightness change for “AE Tracking” feature. “AE Stable” condition is used to detect scene brightness change. Unit : % percentage
<13.22h>	0Ah	**AE tracker (normal Y)**	R/W	[7:0]	Normal-light (highlight) condition threshold increase to limit scene brightness change for “AE Tracking” feature. “AE Stable” condition is used to detect scene brightness change. Unit : % percentage
<13.23h>	00h	**Selected Window**	R/W	[7:0]	This register has read access and display the AF algorithm decision - which AF window is used for current(lateset) AF operation 0b : inner window 1b : outer window
<13.24h>		**Reserved**		[7:0]	
<13.25h>		**Reserved**		[7:0]	
<13.26h>		**Reserved**		[7:0]	
<13.27h>		**Reserved**		[7:0]	
<13.28h>		**Reserved**		[7:0]	
<13.29h>	84h	**Inflection Point**	R/W	[7:0]	Inflection Point refer to figure 4, For calculating lens moving time (lens response time)
<13.2Ah>	1Eh	**Inflection Time**	R/W	[7:0]	Inflection Time refer to figure 4, For calculating lens moving time (lens response time)
<13.2Bh>	50h	**Max time of RT**	R/W	[7:0]	max time at maximum position. For calculating lens moving time (lens response time)
<13.2Ch>		**Reserved**		[7:0]	
<13.2Dh>	05h	**Stable Threshold**	R/W	[7:4] [3:0]	Reserved Stable Counter for detecting scene change
<13.2Eh>	0Ah	**Pseudo Threshold**	R/W	[7:0]	The difference threshold for deciding start of pseudo continuous AF. (unit : % percentage) This difference is refered before best focused value.

Addr	Reset Value	Mnemonic	Attr	Bits	Descriptions
<13.2Fh>		**Reserved**		[7:0]	
<13.30h>	5Ah	**Prescaler PWM [Timer]**	R/W	[7:0]	Prescaler value for PWM Timers pair (port 4 and 5)
<13.31h>	00h	**Divider PWM [Timer]**	R/W	[7:4] [3:0]	Reserved Divider values for PWM Timer : 0=2, 1=4, 2=8, 3=16
<13.32h>	00h	**Counter [Timer](MSB)**	R/W	[7:0]	Counter value for PWM Timer (MSB)
<13.33h>	44h	**Counter [Timer](LSB)**	R/W	[7:0]	Counter value for PWM Timer (LSB)
<13.34h>	00h	**Prescaler PWM [Control]**	R/W	[7:0]	Prescaler value for PWM Timers pair (Even and Odd , ex: 0 and 1)
<13.35h>	00h	**Divider PWM [Control]**	R/W	[7:4] [3:0]	Divider values for PWM Timer : 0=2, 1=4, 2=8, 3=16
<13.36h>	00h	**Counter [Control](MSB)**	R/W	[7:0]	Counter value for PWM Timer (MSB)
<13.37h>	D8h	**Counter [Control](LSB)**	R/W	[7:4] [3:0]	Counter value for PWM Timer (LSB)
<13.38h>		**Reserved**		[7:0]	
<13.39h>		**Reserved**		[7:0]	
<13.3Ah>		**Reserved**		[7:0]	
<13.3Bh>		**Reserved**		[7:0]	
<13.3Ch>		**Reserved**		[7:0]	
<13.3Dh>		**Reserved**		[7:0]	
<13.3Eh>		**Reserved**		[7:0]	
<13.3Fh>		**Reserved**		[7:0]	
<13.40h>	00h	**Position Multiplier**	R/W	[7:3] [2:0]	Reserved The multiplier for increasing bit resolution about position 00h and 01h : 1 time at every position registers 02h : 2 times at every position registers 03h : 3 times at every position registers 04h : 4 times at every position registers 05h : 5 times at every position registers 06h : 6 times at every position registers 07h : 7 times at every position registers
<13.41h>		**Reserved**		[7:0]	
<13.42h>		**Reserved**		[7:0]	
<13.43h>		**Reserved**		[7:0]	
<13.44h>	08h	**Minimum Position**	R/W	[7:0]	It can't move physically under the minimum position
<13.45h>	D8h	**Maximum Position**	R/W	[7:0]	It can't move physically over the maximum position
<13.46h>	10h	**Low Confidence Position**	R/W	[7:0]	The position user want to move, when the result of AF is low confidence level
<13.47h>	10h	**Intial Wanted Position**	R/W	[7:0]	After initializing AF, the position is you want to move initially
<13.48h>	00h	**Previous Position**	R/W	[7:0]	Previous moved position

Addr	Reset Value	Mnemonic	Attr	Bits	Descriptions
<13.49h>	00h	**Current Position**	R/W	[7:0]	Current focused position. These registers contain current AF position and are updated after all AF commands that affect current AF position. The host can change these registers and send "Start manual AF operation" (Command code 04h) to main AF command register (<00h.6Eh>) to move the lens to specified position.
<13.4Ah>	00h	**Physical Position**	R/W	[7:0]	Physical initial position (= Home Position) : It is role as the base of logical position. - In STM case, the position is decided by photo interrupt - In VCM case, the position is decided at power on, It is always zero
<13.4Bh>	80h	**Macro Start Position**	R/W	[7:0]	It is means searchign start position of macro mode. When you set this register, you input the index of table or the order number of linear step type In special, when you use <0.6Eh>=07h or 17h command this register used as offset position
<13.4Ch>	08h	**Fine Step Size**	R/W	[7:0]	Step size for fine searching
<13.4Dh>	04h	**Fine Step #**	R/W	[7:0]	When fine searching, it is searching lens step number. Using this register, we can also calculate the start position for fine searching before coarse peak position. When fine step size is 2, fine step number is 10 and coarse peak is 125, the start fine searching position is 115 (= 125 - [[2*10]/2])
<13.4Eh>	10h	**Coarse Step Size**	R/W	[7:0]	Step size for coarse searching with using linear step, not table type
<13.4Fh>	0Ch	**Coarse Step #**	R/W	[7:0]	When coarse searching, it is searching lens step number. Using this register, we can also calculate end lens position for searching and middle lens position
<13.50h>	18h	**Coarse Position 0**	R/W	[7:0]	Intermediate coarse search position 0 / Start lens position for searching
<13.51h>	2Eh	**Coarse Position 1**	R/W	[7:0]	Intermediate coarse search position 1
<13.52h>	40h	**Coarse Position 2**	R/W	[7:0]	Intermediate coarse search position 2
<13.53h>	50h	**Coarse Position 3**	R/W	[7:0]	Intermediate coarse search position 3
<13.54h>	6Eh	**Coarse Position 4**	R/W	[7:0]	Intermediate coarse search position 4
<13.55h>	7Dh	**Coarse Position 5**	R/W	[7:0]	Intermediate coarse search position 5
<13.56h>	8Ch	**Coarse Position 6**	R/W	[7:0]	Intermediate coarse search position 6
<13.57h>	9Bh	**Coarse Position 7**	R/W	[7:0]	Intermediate coarse search position 7
<13.58h>	AAh	**Coarse Position 8**	R/W	[7:0]	Intermediate coarse search position 8
<13.59h>	B8h	**Coarse Position 9**	R/W	[7:0]	Intermediate coarse search position 9
<13.5Ah>	C7h	**Coarse Position 10**	R/W	[7:0]	Intermediate coarse search position 10
<13.5Bh>	D8h	**Coarse Position 11**	R/W	[7:0]	Intermediate coarse search position 11

Addr	Reset Value	Mnemonic	Attr	Bits	Descriptions
<13.5Ch>	E9h	**Coarse Position 12**	R/W	[7:0]	Intermediate coarse search position 12
<13.5Dh>	FAh	**Coarse Position 13**	R/W	[7:0]	Intermediate coarse search position 13
<13.5Eh>	00h	**Coarse Position 14**	R/W	[7:0]	Intermediate coarse search position 14
<13.5Fh>	00h	**Coarse Position 15**	R/W	[7:0]	Intermediate coarse search position 15
<13.60h>	00h	**Coarse Position 16**	R/W	[7:0]	Intermediate coarse search position 16
<13.61h>	00h	**Coarse Position 17**	R/W	[7:0]	Intermediate coarse search position 17
<13.62h>	00h	**Coarse Position 18**	R/W	[7:0]	Intermediate coarse search position 18
<13.63h>	00h	**Coarse Position 19**	R/W	[7:0]	Intermediate coarse search position 19
<13.64h>	00h	**Coarse Position 20**	R/W	[7:0]	Intermediate coarse search position 20
<13.65h>	00h	**Coarse Position 21**	R/W	[7:0]	Intermediate coarse search position 21
<13.66h>	00h	**Coarse Position 22**	R/W	[7:0]	Intermediate coarse search position 22
<13.67h>	00h	**Coarse Position 23**	R/W	[7:0]	Intermediate coarse search position 23
<13.68h>	00h	**Coarse Position 24**	R/W	[7:0]	Intermediate coarse search position 24
<13.69h>	00h	**Coarse Position 25**	R/W	[7:0]	Intermediate coarse search position 25
<13.6Ah>	00h	**Coarse Position 26**	R/W	[7:0]	Intermediate coarse search position 26
<13.6Bh>	00h	**Coarse Position 27**	R/W	[7:0]	Intermediate coarse search position 27
<13.6Ch>	00h	**Coarse Position 28**	R/W	[7:0]	Intermediate coarse search position 28
<13.6Dh>	00h	**Coarse Position 29**	R/W	[7:0]	Intermediate coarse search position 29
<13.6Eh>	00h	**Coarse Position 30**	R/W	[7:0]	Intermediate coarse search position 30
<13.6Fh>	00h	**Coarse Position 31**	R/W	[7:0]	Intermediate coarse search position 31
<13.70h>	80h	**Window Preset**	R/W	[7] [6] [5:4] [3:2] [1:0] 	Using preset window or not (if set 0b, refer to the direct setting register <1B Page> Reserved Selection preset mode for AF inner window (Automatically set at center base) 00h : Small 01h : Midium 02h : Large Reserved Selection preset mode for AF outer window (Automatically set at center base) 00h : Small 01h : Midium 02h : Large
<13.71h>		**Reserved**		[7:0]	
<13.72h>	00h	**W1_S_Width_MSB**	R/W	[7:0]	Width of AF outer window with preset type Small
<13.73h>	C8h	**W1_S_Width_LSB**	R/W	[7:0]	Width of AF outer window with preset type Small
<13.74h>	00h	**W1_S_Height_MSB**	R/W	[7:0]	Height of AF outer window with preset type Small

Addr	Reset Value	Mnemonic	Attr	Bits	Descriptions
<13.75h>	64h	**W1_S_Height_LSB**	R/W	[7:0]	Height of AF outer window with preset type Small
<13.76h>	01h	**W1_M_Width_MSB**	R/W	[7:0]	Width of AF outer window with preset type Midium
<13.77h>	18h	**W1_M_Width_LSB**	R/W	[7:0]	Width of AF outer window with preset type Midium
<13.78h>	00h	**W1_M_Height_MSB**	R/W	[7:0]	Height of AF outer window with preset type Midium
<13.79h>	A0h	**W1_M_Height_LSB**	R/W	[7:0]	Height of AF outer window with preset type Midium
<13.7Ah>	01h	**W1_L_Width_MSB**	R/W	[7:0]	Width of AF outer window with preset type Large
<13.7Bh>	68h	**W1_L_Width_LSB**	R/W	[7:0]	Width of AF outer window with preset type Large
<13.7Ch>	00h	**W1_L_Height_MSB**	R/W	[7:0]	Height of AF outer window with preset type Large
<13.7Dh>	DCh	**W1_L_Height_LSB**	R/W	[7:0]	Height of AF outer window with preset type Large
<13.7Eh>	01h	**W2_S_Width_MSB**	R/W	[7:0]	Width of AF inner window with preset type Small
<13.7Fh>	B8h	**W2_S_Width_LSB**	R/W	[7:0]	Width of AF inner window with preset type Small
<13.80h>	01h	**W2_S_Height_MSB**	R/W	[7:0]	Height of AF inner window with preset type Small
<13.81h>	18h	**W2_S_Height_LSB**	R/W	[7:0]	Height of AF inner window with preset type Small
<13.82h>	02h	**W2_M_Width_MSB**	R/W	[7:0]	Width of AF inner window with preset type Midium
<13.83h>	08h	**W2_M_Width_LSB**	R/W	[7:0]	Width of AF inner window with preset type Midium
<13.84h>	01h	**W2_M_Height_MSB**	R/W	[7:0]	Height of AF inner window with preset type Midium
<13.85h>	54h	**W2_M_Height_LSB**	R/W	[7:0]	Height of AF inner window with preset type Midium
<13.86h>	02h	**W2_L_Width_MSB**	R/W	[7:0]	Width of AF inner window with preset type Large
<13.87h>	58h	**W2_L_Width_LSB**	R/W	[7:0]	Width of AF inner window with preset type Large
<13.88h>	01h	**W2_L_Height_MSB**	R/W	[7:0]	Height of AF inner window with preset type Large
<13.89h>	90h	**W2_L_Height_LSB**	R/W	[7:0]	Height of AF inner window with preset type Large
<13.8Ah>		**Reserved**		[7:0]	
<13.8Bh>		**Reserved**		[7:0]	
<13.8Ch>		**Reserved**		[7:0]	
<13.8Dh>		**Reserved**		[7:0]	
<13.8Eh>		**Reserved**		[7:0]	
<13.8Fh>		**Reserved**		[7:0]	
<13.90h>	42h	**Select Interface**	R/W	[7:6] [5] [4] [3:2]	Selection motor type 00b : Stepping 01b : Voice Coil 10b : Piezo 11b : Etc Selection IIC type 0 : not IIC 1 : IIC Reserved Selection port type 00b : 1-port

Addr	Reset Value	Mnemonic	Attr	Bits	Descriptions
					01b : 2-port 02b : 4-port
				[1]	Exist enable/disable pin on driver IC 0b : No exist 1b : Exist
				[0]	Reserved
<13.91h>	42h	**Select Port # for Channel A-/+**	R/W	[7] [6:4] [3] [2:0]	Reserved Selection pin number for Channel A '-' & PWM2 (Port_0 ~ Port_4, Port_5 is fixed as Timer) Reserved Selection pin number for Channel A '+' & PWM 1 (VCM PWM case) (Port_0 ~ Port_4, Port_5 is fixed as Timer)
<13.92h>	03h	**Select Port # for Channel B-/+**	R/W	[7] [6:4] [3] [2:0]	Reserved Selection pin number for Channel B '-' (Port_0 ~ Port_4, Port_5 is fixed as Timer) Reserved Selection pin number for Channel B '+' (Port_0 ~ Port_4, Port_5 is fixed as Timer)
<13.93h>	01h	**Select Enable Pin**	R/W	[7:3] [2:0]	Reserved Selection port number for enable pin of driver IC (port_0 ~ port_4)
<13.94h>		**Reserved**		[7:0]	
<13.95h>	18h	**Set Chip ID for Driver**	R/W	[7:0]	Set slave address of driver IC (Refered from the AD5398 and MD118)
<13.96h>	02h	**Set IIC format**	R/W	[7:6] [5:4] [3:2] [1:0]	Reserved IIC Register Address Format 00b : There is no need to set register address because driver IC has just one register 01b : Register address 1 byte 10b : Register address 2 byte Reserved IIC Register Data Format 0Xb : Register data 1 byte 10b : Register data 2 byte
<13.97h>	00h	**Register Address (MSB)**		[7:0]	IIC Register Address Value (MSB)
<13.98h>	00h	**Register Address (LSB)**		[7:0]	IIC Register Address Value (LSB), if you select 1 byte address format, this register no affect
<13.99h>	00h	**Register Data (MSB)**		[7:0]	IIC Register Data Value (MSB) for read/write
<13.9Ah>	00h	**Register Data (LSB)**		[7:0]	IIC Register Data Value (LSB), if you select 1 byte data format, this register no affect
<13.9Bh>		**Reserved**		[7:0]	
<13.9Ch>	40h	**Special Init Command**	R/W	[7:0]	If there is special initialize command for IIC type driver IC, set it at this register. If so, when command <0.6Eh> = 01h, will give to driver IC with this register value as initialization
<13.9Dh>	80h	**S/W PD Command**	R/W	[7:0]	If there is S/W power down command for IIC type driver IC, set it at this register.

Addr	Reset Value	Mnemonic	Attr	Bits	Descriptions
<13.9Eh>	60h	**Move Command (Near)**	R/W	[7:0]	move command (infinity to macro) for IIC type driver
<13.9Fh>	70h	**Move Command (Far)**	R/W	[7:0]	move command (macro to infinity) for IIC type driver
<13.A0h>	03h	PI Threshold (MSB)	R/W	[7:2] [1:0]	Reserved ADC threshold for PI(Photo Interrupt) detection
<13.A1h>	F7h	PI Threshold (LSB)	R/W	[7:0]	ADC threshold for PI(Photo Interrupt) detection
<13.A2h>	00h	PI Detection Active	R/W	[7:0]	00b : Infinitive Mode 1 (Low --> High detection) 01b : Infinitive Mode 2 (High --> Low detection) 02b : Macro Mode 1 (Low --> High detection) 03b : Macro Mode 2 (High --> Low detection)
<13.A3h>	02h	PI Detection Delay	R/W	[7:0]	It is for detecting PI after settling (special position sensor has shaking, when goes to initial position) The unit is 500us, we can set 0 ~ 127.5ms(500usX255)
<13.A4h>		**Reserved**		[7:0]	
<13.A5h>		**Reserved**		[7:0]	
<13.A6h>		**Reserved**		[7:0]	
<13.A7h>	00h	Compensate Backlash Far	R/W	[7:0]	Stepping actuator backlash (in steps). This value is used to compensate stepping actuator backlash (if any present) for direction changing. Compensation is performed by overshooting required position added with the backlash amount, NOTE: backlash compensation may result in increasing actuator response time. Use it if it is really necessary.Specify zero if no compensation required.
<13.A8h>	00h	**Compensate Backlash Near**	R/W	[7:0]	Stepping actuator backlash (in steps). This value is used to compensate stepping actuator backlash (if any present) for direction changing. Compensation is performed by overshooting required position added with the backlash amount, NOTE: backlash compensation may result in increasing actuator response time. Use it if it is really necessary.Specify zero if no compensation required.
<13.A9h>	02h	**Chatter Value**	R/W	[7:0]	Number of pulses the stepping actuator has to move to remove value chatter in photo interrupter (which is used to specify zero position for the lens). Refer to Fig.6 for description of infinity margin parameter.
<13.AAh>	10h	**Infinity Margin**	R/W	[7:0]	The size of infinity margin in stepping actuator (in steps). That is, the distance home position with infinity. This infinity margin parameter is needed for stepping actuator initialization (resetting to zero position). Refer to Fig.6 for description of infinity margin parameter. When <13.A2h> is Infinitive Mode(00b or 01b), this register use as signed byte Whereas <13.A2h> is Macro Mode(02b or 03b), this register use as unsigned byte.

Addr	Reset Value	Mnemonic	Attr	Bits	Descriptions
<13.ABh>	02h	**Maximum Distance(MSB)**	R/W	[7:0]	Maximum distance the stepping actuator will move during initialization on stage 2 (MSB)
<13.ACh>	00h	**Maximum Distance(LSB)**	R/W	[7:0]	--//--//--(LSB)
<13.ADh>	01h	**Power On Delay**	R/W	[7:0]	Stepping actuator power-on delay (unit : Timer5 x 2 times)
<13.AEh>	01h	**Power Off Delay**	R/W	[7:0]	Stepping actuator power-off delay (unit : Timer5 x 2 times)
<13.AFh>	02h	**Init Delay**	R/W	[7:0]	Stepping actuator initialization delay (unit : Timer5 x 2 times)
<13.B0h>	01h	**Reverse Delay (near -> far)**	R/W	[7:0]	Stepping actuator positive -> negative reverse time delay (unit : Timer5 x 2 times)
<13.B1h>	01h	**Reverse Delay (far -> near)**	R/W	[7:0]	Stepping actuator negative -> positive reverse time delay (unit : Timer5 x 2 times)
<13.B2h>	05h	**Speed Delay**	R/W	[7:0]	Stepping actuator speed - delay between 2 steps (unit : Timer5 x1 time)
<13.B3h>		**Reserved**		[7:0]	
<13.B4h>		**Reserved**		[7:0]	
<13.B5h>		**Reserved**		[7:0]	
<13.B6h>		**Reserved**		[7:0]	
<13.B7h>		**Reserved**		[7:0]	
<13.B8h>		**Reserved**		[7:0]	
<13.B9h>		**Reserved**		[7:0]	
<13.BAh>		**Reserved**		[7:0]	
<13.BBh>		**Reserved**		[7:0]	
<13.BCh>		**Reserved**		[7:0]	
<13.BDh>		**Reserved**		[7:0]	
<13.BEh>		**Reserved**		[7:0]	
<13.BFh>		**Reserved**		[7:0]	
<13.C0h>		**Reserved**		[7:0]	
<13.C1h>		**Reserved**		[7:0]	
<13.C2h>		**Reserved**		[7:0]	
<13.C3h>		**Reserved**		[7:0]	
<13.C4h>		**Reserved**		[7:0]	
<13.C5h>		**Reserved**		[7:0]	
<13.C6h>		**Reserved**		[7:0]	
<13.C7h>	40h	Distance Threshold	R/W	[7:0]	If the distance current position with target position is long, when moving with using multi sub-step. This threshold will decide that multi sub-step apply or not. Without setting <13.C8h> for coarse setting.
<13.C8h>	01h	Multi Sub-Step On	R/W	[7:0]	Multi sub-step for shaking during coarse search 0b : multisubstep off 1b : multisubstep on
<13.C9h>	05h	Multisubstep #	R/W	[7:3] [2:0]	Reserved Multi sub-step number (Maximum 5)

Addr	Reset Value	Mnemonic	Attr	Bits	Descriptions
<13.CAh>	01h	Multisubstep width	R/W	[7:0]	Multi sub-step width (means delay time between steps) (unit : Timer5 x 1time)
<13.CBh>	46h	Multisubstep #1 Level	R/W	[7:0]	Moving level(percentage[1)]) of target position for multisubstep #1
<13.CCh>	54h	Multisubstep #2 Level	R/W	[7:0]	Moving level(percentage) of target position for multisubstep #2
<13.CDh>	5Bh	Multisubstep #3 Level	R/W	[7:0]	Moving level(percentage) of target position for multisubstep #3
<13.CEh>	5Fh	Multisubstep #4 Level	R/W	[7:0]	Moving level(percentage) of target position for multisubstep #4
<13.CFh>	62h	Multisubstep #5 Level	R/W	[7:0]	Moving level(percentage) of target position for multisubstep #5
<13.D0h>	00h	**Y Normalize (Def:80h)**	R/W	[7] [6:1] [0]	Y Normalize Type 0b : FV = FO / YC 1b : FV = (FO * YS) / YC Reserved Y Normalize On/Off using with Y average nearby AF window
<13.D1h>	00h	**AE Patch W1 R1**	R/W	[7:0]	4BA AE window consist of 48 patches (6V*8H). For Y-nomalization, select AE patch at 1st raw in window 1. Each bit represent each column as AE patch.
<13.D2h>	00h	**AE Patch W1 R2**	R/W	[7:0]	4BA AE window consist of 48 patches. For Y-nomalization, select AE patch at 2nd raw in window 1. Each bit represent each column as AE patch.
<13.D3h>	18h	**AE Patch W1 R3**	R/W	[7:0]	4BA AE window consist of 48 patches. For Y-nomalization, select AE patch at 3rd raw in window 1. Each bit represent each column as AE patch.
<13.D4h>	18h	**AE Patch W1 R4**	R/W	[7:0]	4BA AE window consist of 48 patches. For Y-nomalization, select AE patch at 4th raw in window 1. Each bit represent each column as AE patch.
<13.D5h>	00h	**AE Patch W1 R5**	R/W	[7:0]	4BA AE window consist of 48 patches. For Y-nomalization, select AE patch at 5th raw in window 1. Each bit represent each column as AE patch.
<13.D6h>	00h	**AE Patch W1 R6**	R/W	[7:0]	4BA AE window consist of 48 patches. For Y-nomalization, select AE patch at 6th raw in window 1. Each bit represent each column as AE patch.
<13.D7h>	00h	**AE Patch W2 R1**	R/W	[7:0]	4BA AE window consist of 48 patches (6V*8H). For Y-nomalization, select AE patch at 1st raw in window 2. Each bit represent each column as AE patch.
<13.D8h>	7Eh	**AE Patch W2 R2**	R/W	[7:0]	4BA AE window consist of 48 patches. For Y-nomalization, select AE patch at 2nd raw in window 2. Each bit represent each column as AE patch.
<13.D9h>	7Eh	**AE Patch W2 R3**	R/W	[7:0]	4BA AE window consist of 48 patches. For Y-nomalization, select AE patch at 3rd raw in window 2. Each bit represent each column as AE patch.
<13.DAh>	7Eh	**AE Patch W2 R4**	R/W	[7:0]	4BA AE window consist of 48 patches. For Y-nomalization, select AE patch at 4th raw in window 2. Each bit represent each column as AE patch.
<13.DBh>	7Eh	**AE Patch W2 R5**	R/W	[7:0]	4BA AE window consist of 48 patches. For Y-nomalization, select AE patch at 5th raw in window 2. Each bit represent each column as AE patch.

Addr	Reset Value	Mnemonic	Attr	Bits	Descriptions
<13.DCh>	00h	**AE Patch W2 R6**	R/W	[7:0]	4BA AE window consist of 48 patches. For Y-nomalization, select AE patch at 6th raw in window 2. Each bit represent each column as AE patch.

13. IMAGE FORMAT(3) (PAGE 14H)

* Image Format Registers will be loaded to Target Registers (ISP and CIS registers) when performing Image Format command <0.02h> or <0.73h> or <0.74h>.

* Image Format Table Index = <0.02h>

TABLE 1. SUB-SAMPLING TABLE INDEX

Table Index <0.02h>	Page	Address	Table Name
0 (Table 0)	03h	00h~2Fh	UXGA
1 (Table 1)		30h~5Fh	SXGA
2 (Table 2)		60h~8Fh	VGA
3 (Table 3)		90h~BFh	QVGA
4 (Table 4)		C0h~EFh	QQVGA
5 (Table 5)	04h	00h~2Fh	CIF
6 (Table 6)		30h~5Fh	QCIF
7 (Table 7)		60h~8Fh	H = 2, V = 1
8 (Table 8)		90h~BFh	H = 1, V =2
9 (Table 9)		C0h~EFh	H = 2, V = 2
10 (Table 10)	14h	00h~2Fh	H = 4, V = 1
11 (Table11)		30h~5Fh	H = 4, V = 4
12 (Table 12)		60h~8Fh	Reserved

Table 2. Detailed register Table of Table 1 – Page 14h (Attribute of all these values is R/W)

Addr [4:0]	Target Register	Bits	Descriptions	Table Index 10	Table Index 11	Table Index 12
00h	<2.04h>	[7:0]	**CIS_FRAME_H_WIDTH_H**	06h	06h	06h
01h	<2.05h>	[7:0]	**CIS_FRAME_H_WIDTH_L**	E2h	E2h	E2h
02h	<2.06h>	[7:0]	**CIS_FRAME_V_DEPTH_H**	04h	01h	04h
03h	<2.07h>	[7:0]	**CIS_FRAME_V_DEPTH_L**	BCh	57h	BCh
04h	<2.08h>	[7:0]	**CIS_OUTPUT_H_WIDTH_H**	01h	01h	06h
05h	<2.09h>	[7:0]	**CIS_OUTPUT_H_WIDTH_L**	96h	96h	46h
06h	<2.0Ah>	[7:0]	**CIS_OUTPUT_V_DEPTH_H**	04h	01h	04h
07h	<2.0Bh>	[7:0]	**CIS_OUTPUT_V_DEPTH_L**	B4h	30h	B4h
08h	<2.15h>	[7:0]	**CIS_H_EVEN_INC_L**	01h	01h	01h
09h	<2.17h>	[7:0]	**CIS_H_ODD_INC_L**	07h	07h	01h
0Ah	<2.19h>	[7:0]	**CIS_V_EVEN_INC_L**	01h	01h	01h
0Bh	<2.1Bh>	[7:0]	**CIS_V_ODD_INC_L**	01h	07h	01h
0Ch	<2.03h>[3]	[7:0]	**CIS_MIRR_ETC(Average sub)**	00h	08h	00h
0Dh	<5.6Eh>	[7:0]	**DSP5_POST_HSTART_H**	00h	00h	00h

Addr [4:0]	Target Register	Bits	Descriptions	Table Index 10	Table Index 11	Table Index 12
0Eh	<5.6Fh>	[7:0]	**DSP5_POST_HSTART_L**	04h	04h	04h
0Fh	<5.70h>	[7:0]	**DSP5_POST_HWIDTH_H**	01h	01h	06h
10h	<5.71h>	[7:0]	**DSP5_POST_HWIDTH_L**	90h	90h	40h
11h	<5.72h>	[7:0]	**DSP5_POST_VSTART_H**	00h	00h	00h
12h	<5.73h>	[7:0]	**DSP5_POST_VSTART_L**	02h	02h	02h
13h	<5.74h>	[7:0]	**DSP5_POST_VHEIGHT_H**	04h	01h	04h
14h	<5.75h>	[7:0]	**DSP5_POST_VHEIGHT_L**	B0h	2Ch	B0h
15h	<5.7Ah>	[7:0]	**DSP5_IMG_HSIZEH**	01h	01h	06h
16h	<5.7Bh>	[7:0]	**DSP5_IMG_HSIZEL**	90h	90h	40h
17h	<5.7Ch>	[7:0]	**DSP5_IMG_VSIZEH**	04h	01h	04h
18h	<5.7Dh>	[7:0]	**DSP5_IMG_VSIZEL**	B0h	2Ch	B0h
19h	<5.7Eh>	[7:0]	**DSP5_PSF**	00h	00h	00h
1Ah	<5.7Fh>	[7:0]	**DSP5_MSFX_H**	00h	00h	00h
1Bh	<5.80h>	[7:0]	**DSP5_MSFX_L**	00h	00h	00h
1Ch	<5.81h>	[7:0]	**DSP5_MSFY_H**	00h	00h	00h
1Dh	<5.82h>	[7:0]	**DSP5_MSFY_L**	00h	00h	00h
1Eh	<5.83h>	[7:0]	**DSP5_DW_HSIZEH**	01h	01h	06h
1Fh	<5.84h>	[7:0]	**DSP5_DW_HSIZEL**	90h	90h	40h
20h	<5.85h>	[7:0]	**DSP5_DW_VSIZEH**	04h	01h	04h
21h	<5.86h>	[7:0]	**DSP5_DW_VSIZEL**	B0h	2Ch	B0h
22h	<5.87h>	[7:0]	**DSP5_STARTXH**	00h	00h	00h
23h	<5.88h>	[7:0]	**DSP5_STARTXL**	00h	00h	00h
24h	<5.89h>	[7:0]	**DSP5_STARTYH**	00h	00h	00h
25h	<5.8Ah>	[7:0]	**DSP5_STARTYL**	00h	00h	00h
26h	<5.8Bh>	[7:0]	**DSP5_CLIP_HSIZEH**	01h	01h	06h
27h	<5.8Ch>	[7:0]	**DSP5_CLIP_HSIZEL**	90h	90h	40h
28h	<5.8Dh>	[7:0]	**DSP5_CLIP_VSIZEH**	04h	01h	04h
29h	<5.8Eh>	[7:0]	**DSP5_CLIP_VSIZEL**	B0h	2Ch	B0h
2Ah	<5.8Fh>	[7:0]	**DSP5_SEL_MAIN**	00h	00h	00h
2Bh	<5.90h>	[7:0]	**DSP5_HTERMH**	00h	00h	00h
2Ch	<5.91h>	[7:0]	**DSP5_HTERMM**	06h	06h	06h
2Dh	<5.92h>	[7:0]	**DSP5_HTERML**	E0h	E0h	E0h
2Eh	<1.02h>	[7:0]	**DSP1_CRCB_SEL**	03h	03h	03h
2Fh	06h,15h, 1Ch Page	[7:0]	**OZONE, Boundary_INDEX**	40h	50h	00h

14. BOUNDARY REGISTER MAP (PAGE 15H)

* Boundary Page (Page 0x15) Registers will be loaded to Target Registers (ISP registers) when performing Image Format command <0.02h> or <0.73h> or <0.74h>.

* Boundary Table Index
  case of (Image Format Table Index = 0)
    Boundary Index = <3.2Fh>
  case of (Image Format Table Index = 1)
    Boundary Index = <4.5Fh>
  case of (Image Format Table Index = 2)

Table 1. Sub-sampling Table Index

Address	ODM Index	Size
00h~07h	00h	H = 1,V = 1
08h~0Fh	10h	H = 2,V = 1
10h~17h	20h	H = 1,V = 2
18h~1Fh	30h	H = 2,V = 2
20h~27h	40h	H = 4,V = 1
28h~2Fh	50h	H = 4,V = 4
30h~37h	60h	Reserved

Table 2. Detailed register Table of Table 1 – Page 14h (Attribute of all these values is R/W)

Addr offset	Target Register	Bits	Descriptions	Table Index 00h	Table Index 10h	Table Index 20h	Table Index 30h	Table Index 40h	Table Index 50h	Table Index 60h
00h	<1.37h>	[7:0]	HEXTEND_START	81h	81h	81h	81h	81h	81h	81h
01h	<1.38h>	[7:0]	HEXTEND_END_H	06h	03h	06h	03h	01h	01h	06h
02h	<1.39h>	[7:0]	HEXTEND_END_L	44h	24h	44h	24h	94h	94h	44h
03h	<1.3Ah>	[7:0]	VEXTEND_START	81h	81h	81h	81h	81h	81h	81h
04h	<1.3Bh>	[7:0]	VEXTEND_END_H	04h	04h	02h	02h	04h	01h	04h
05h	<1.3Ch>	[7:0]	VEXTEND_END_L	B4h	B4h	5Ch	5Ch	B4h	30h	B4h
06h			Reversed	00h	00h	00h	00h	00h	00h	00h
07h			Reversed	00h	00h	00h	00h	00h	00h	00h

15. ISP REGISTER MAP (PAGE 1BH)

Addr	Reset Value	Mnemonic	Attr	Bits	Descriptions
<1B.00h>	00h	**OMODE**	R/W	[7] [6] [5] [4] [3] [2] [1:0]	AFZONE 0 : Disable 1 : Enable Horizontal LPF coefficient selection 0b : [½ ½] 1b : [¼ ½ ¼] Horizontal LPF bypass flag 0b : use LPF pre-filter 1b : bypass LPF pre-filter Horizontal LPF input data 10-bit to 8-bit conversion method 0b : Y >> 2 (Y[9:2]) 1b : sat (Y[7:0]) (255 clipping) OAWB_UPDATE 0b : Register no update 1b : Register update OAWB_MODE 0 : Overwrite Mode 1 : Write Protect Mode OZONE_SEL 01 : AE WINDOW DISPLAY 10 : AWB WINDOW DISPLAY
<1B.01h>	30h	**INT_SEL**	R/W	[7:4] [3] [2] [1] [0]	RGB Data Delay Selection, 0 ~ 6 Delay Selection AF interrupt Selection 0 : AF window1 interrupt 1:AF window2 interrupt AE_AWB_INT_SEL 0 : Auto interrupt mode 1:Manual interrupt AWV Algorithm Selection 0:SAIT AWB Algorithm 1:Old AWB Algorithm Interrupt Selection, 0 : AE window done, 1 : AE AWB all window done
<1B.02h>	E0h	**OAF_PEAK_TH**	R/W	[7:0]	AF_PEAK_TH[7:0], AF Threshold for saturated pixel count
<1B.03h>	00h	**OAFHS_W1H**	R/W	[7:0]	AF_W1H_START[15:8], AF Window1 Horizontal Start Point (High)
<1B.04h>	28h	**OAFHS_W1L**	R/W	[7:0]	AF_W1H_START[7:0], AF Window1 Horizontal Start Point (Low)
<1B.05h>	04h	**OAFHE_W1H**	R/W	[7:0]	AF_W1H_END[15:8], AF Window1 Horizontal End Point (High)
<1B.06h>	ECh	**OAFHE_W1L**	R/W	[7:0]	AF_W1H_END[7:0], AF Window1 Horizontal End Point (Low)
<1B.07h>	00h	**OAFVS_W1H**	R/W	[7:0]	AF_W1V_START[15:8], AF Window1 Vertical Start Point (High)
<1B.08h>	05h	**OAFVS_W1L**	R/W	[7:0]	AF_W1V_START[7:0], AF Window1 Vertical Start Point (Low)
<1B.09h>	03h	**OAFVE_W1H**	R/W	[7:0]	AF_W1V_END[15:8], AF Window1 Vertical End Point (High)
<1B.0Ah>	F2h	**OAFVE_W1L**	R/W	[7:0]	AF_W1V_END[7:0], AF Window1 Vertical End Point (Low)

Addr	Reset Value	Mnemonic	Attr	Bits	Descriptions
<1B.0Bh>	00h	**OAFHS_W2H**	R/W	[7:0]	AF_W2H_START[15:8], AF Window1 Horizontal Start Point (High)
<1B.0Ch>	64h	**OAFHS_W2L**	R/W	[7:0]	AF_W2H_START[7:0], AF Window1 Horizontal Start Point (Low)
<1B.0Dh>	00h	**OAFHE_W2H**	R/W	[7:0]	AF_W2H_END[15:8], AF Window1 Horizontal End Point (High)
<1B.0Eh>	FAh	**OAFHE_W2L**	R/W	[7:0]	AF_W2H_END[7:0], AF Window1 Horizontal End Point (Low)
<1B.0Fh>	00h	**OAFVS_W2H**	R/W	[7:0]	AF_W2V_START[15:8], AF Window1 Vertical Start Point (High)
<1B.10h>	32h	**OAFVS_W2L**	R/W	[7:0]	AF_W2V_START[7:0], AF Window1 Vertical Start Point (Low)
<1B.11h>	00h	**OAFVE_W2H**	R/W	[7:0]	AF_W2V_END[15:8], AF Window1 Vertical End Point (High)
<1B.12h>	A0h	**OAFVE_W2L**	R/W	[7:0]	AF_W2V_END[7:0], AF Window1 Vertical End Point (Low)
<1B.13h>	04h	**OAF_MODE**	R/W	[7] [6] [5] [4] [3] [2] [1:0]	Reserved Horizontal Gain Selection (1b: clip, 0b:shift) Vertical Gain Selection (1b: clip, 0b:shift) Y or G Selection Hpf12 vertical on Hpf3 vertical on H filter gain
<1B.14h>	00h	**OAF_HPF_SEL**	R/W	[7:5] [4:2]] [1:0]	HPF1 Selection HPF2 Selection HPF3 Selection
<1B.15h>	20h	**OAF_VCOEFF0**	R/W	[7:0]	Vertical AF Coefficient0
<1B.16h>	10h	**OAF_VCOEFF1**	R/W	[7:0]	Vertical AF Coefficient1
<1B.17h>	00h	**OAF_VCOEFF2**	R/W	[7:0]	Vertical AF Coefficient2
<1B.18h>	20h	**OAF_HCOEFF0**	R/W	[7:0]	Horizontal AF Coefficient0
<1B.19h>	10h	**OAF_HCOEFF1**	R/W	[7:0]	Horizontal AF Coefficient1
<1B.1Ah>	00h	**OAF_HCOEFF2**	R/W	[7:0]	Horizontal AF Coefficient2
<1B.1Bh>	40h	**OAF_HGAIN_SRC**	R/W	[7:0]	AF Horizontal gain source data (integer 2bit + fraction 4bit)
<1B.1Ch>	03h	**HV_DLY_SEL_AF**	R/W	[7:0]	Hsync, Vsync Delay Selection (0~6 delay)
<1B.1Dh>	00h	**AF_NOISE_TH_F1_W1**	R/W	[7:0]	Noise threshold of AF filter 1, window 1
<1B.1Eh>	00h	**AF_NOISE_TH_F1_W2**	R/W	[7:0]	Noise threshold of AF filter 1, window 2
<1B.1Fh>	00h	**AF_NOISE_TH_F2_W1**	R/W	[7:0]	Noise threshold of AF filter 2, window 1
<1B.20h>	00h	**AF_NOISE_TH_F2_W2**	R/W	[7:0]	Noise threshold of AF filter 2, window 2
<1B.21h>	00h	**AF_NOISE_TH_F3_W1**	R/W	[7:0]	Noise threshold of AF filter 3, window 1
<1B.22h>	00h	**AF_NOISE_TH_F3_W2**	R/W	[7:0]	Noise threshold of AF filter 3, window 2
<1B.23>	00h	AF_PEAK_SEM_SEL	R/W	[7] [6]	Reserved af_peak_sum_sel_f1_w1

Addr	Reset Value	Mnemonic	Attr	Bits	Descriptions
				[5] [4] [3] [2] [1] [0]	af_peak_sum_sel_f1_w2 af_peak_sum_sel_f2_w1 af_peak_sum_sel_f2_w2 af_peak_sum_sel_f3_w1 af_peak_sum_sel_f3_w2 af_ock_off, filter1, 2 subsampling clock off
<1B.24-30h>		Reserved			
<1B.31>	00h	PCLK_DLY	R/W	[7:0]	PCLK Delay Selection
<1B.32>	00h	SYNC_HOLD	R/W	[7:2] [1:0]	Reserved SYNC_HOLD 00 : Normal mode 01 : 8Bit Rolling Test Pattern 10 : 10bit Rolling Test Pattern 11 : VSYNC, HSYCN hold “0”
<1B.33-37h>		Reserved			
<1B.38h>	03h	SH_XCH_GB	R/W	[7:4] [3:0]	Reserved SHADE_XC_Gb_r[11:8] Horizontal Center Value For RGB Shading
<1B.39h>	20h	SH_XCL_GB	R/W	[7:0]	SHADE_XC_Gb_r[7:0]
<1B.3Ah>	02h	SH_YCH_GB	R/W	[7:4] [3:0]	SHADE_YC_Gb_r[11:8] Vertical Center Value For RGB Shading
<1B.3Bh>	58h	SH_YCL_GB	R/W	[7:0]	SHADE_YC_Gb_r[7:0]
<1B.3Ch>	00h	SH_OFF_XH_GB	R/W	[7:0]	Offset_X_Gb[15:8] Horizontal Start Offset For Gb channel (0<= Offset<256)
<1B.3Dh>	00h	SH_OFF_XL_GB	R/W	[7:0]	Offset_X_Gb[7:0]
<1B.3Eh>	00h	SH_OFF_YH_GB	R/W	[7:0]	Offset_Y_Gb[15:8] Vertical Start Offset For Gb channel (0<= Offset<256)
<1B.3Fh>	00h	SH_OFF_YL_GB	R/W	[7:0]	Offset_Y_Gb[7:0]
<1B.40h>	80h	SH_Del_eH_GB	R/W	[7:0]	Delta_e_B[15:8] Horizontal right delta For Gb channel (0<= Delta <=1)
<1B.41h>	00h	SH_Del_eL_GB	R/W	[7:0]	Delta_e_B[7:0]
<1B.42h>	80h	SH_Del_wH_GB	R/W	[7:0]	Delta_w_B[15:8] Horizontal left delta For Gb channel (0<= Delta <=1)
<1B.43h>	00h	SH_Del_wL_GB	R/W	[7:0]	Delta_w_B[7:0]
<1B.44h>	80h	SH_Del_sH_GB	R/W	[7:0]	Delta_s_B[15:8] Vertical bottom delta For Gb channel (0<= Delta <=1)
<1B.45h>	00h	SH_Del_sL_GB	R/W	[7:0]	Delta_s_B[7:0]
<1B.46h>	80h	SH_Del_nH_GB	R/W	[7:0]	Delta_n_B[15:8] Vertical top delta For Gb channel (0<= Delta <=1)

Addr	Reset Value	Mnemonic	Attr	Bits	Descriptions
<1B.47h>	00h	SH_Del_nL_GB	R/W	[7:0]	Delta_n_B[7:0]
<1B.48h>	01h	SH_VAL_GB0H	R/W	[7:4] [3:0]	Reserved SH_VAL_GB0[11:8] Gb Gain at 0 % of Max_radial For RGB Shading
<1B.49h>	00h	SH_VAL_GB0L	R/W	[7:0]	SH_VAL_GB0[7:0] Gb Gain at 0 % of Max_radial For RGB Shading
<1B.4Ah>	01h	SH_VAL_GB1H	R/W	[7:4] [3:0]	Reserved SH_VAL_GB1[11:8] Gb Gain at 20 % of Max_radial For RGB Shading
<1B.4Bh>	00h	SH_VAL_GB1L	R/W	[7:0]	SH_VAL_GB1[7:0] Gb Gain at 20 % of Max_radial For RGB Shading
<1B.4Ch>	01h	SH_VAL_GB2H	R/W	[7:4] [3:0]	Reserved SH_VAL_GB2[11:8] Gb Gain at 40 % of Max_radial For RGB Shading
<1B.4Dh>	00h	SH_VAL_GB2L	R/W	[7:0]	SH_VAL_GB2[7:0] Gb Gain at 40 % of Max_radial For RGB Shading
<1B.4Eh>	01h	SH_VAL_GB3H	R/W	[7:4] [3:0]	Reserved SH_VAL_GB3[11:8] Gb Gain at 60 % of Max_radial For RGB Shading
<1B.4Fh>	00h	SH_VAL_GB3L	R/W	[7:0]	SH_VAL_GB3[7:0] Gb Gain at 60 % of Max_radial For RGB Shading
<1B.50h>	01h	SH_VAL_GB4H	R/W	[7:4] [3:0]	Reserved SH_VAL_GB4[11:8] Gb Gain at 70 % of Max_radial For RGB Shading
<1B.51h>	00h	SH_VAL_GB4L	R/W	[7:0]	SH_VAL_GB4[7:0] Gb Gain at 70 % of Max_radial For RGB Shading
<1B.52h>	01h	SH_VAL_GB5H	R/W	[7:4] [3:0]	Reserved SH_VAL_GB5[11:8] Gb Gain at 80 % of Max_radial For RGB Shading
<1B.53h>	00h	SH_VAL_GB5L	R/W	[7:0]	SH_VAL_GB5[7:0] Gb Gain at 80 % of Max_radial For RGB Shading
<1B.54h>	01h	SH_VAL_GB6H	R/W	[7:4] [3:0]	Reserved SH_VAL_GB6[11:8] Gb Gain at 90 % of Max_radial For RGB Shading
<1B.55h>	00h	SH_VAL_GB6L	R/W	[7:0]	SH_VAL_GB6[7:0] Gb Gain at 90 % of Max_radial For RGB Shading
<1B.56h>	01h	SH_VAL_GB7H	R/W	[7:4] [3:0]	Reserved SH_VAL_GB7[11:8] Gb Gain at 100 % of Max_radial For RGB Shading
<1B.57h>	00h	SH_VAL_GB7L	R/W	[7:0]	SH_VAL_GB7[7:0] Gb Gain at 100 % of Max_radial For RGB Shading
<1B.58h>	00h	SH_M_R2_GB1H	R/W	[7:0]	max_r2_Gb1[23:16] (max_radial)2 at 20 % of Max_radial For RGB Shading
<1B.59h>	9Ch	SH_M_R2_GB1M	R/W	[7:0]	max_r2_Gb1[15:8]

Addr	Reset Value	Mnemonic	Attr	Bits	Descriptions
					(max_radial)2 at 20 % of Max_radial For RGB Shading
<1B.5Ah>	40h	SH_M_R2_GB1L	R/W	[7:0]	max_r2_Gb1[7:0] (max_radial)2 at 20 % of Max_radial For RGB Shading
<1B.5Bh>	02h	SH_M_R2_GB2H	R/W	[7:0]	max_r2_Gb2[23:16] (max_radial)2 at 40 % of Max_radial For RGB Shading
<1B.5Ch>	71h	SH_M_R2_GB2M	R/W	[7:0]	max_r2_Gb2[15:8] (max_radial)2 at 40 % of Max_radial For RGB Shading
<1B.5Dh>	00h	SH_M_R2_GB2L	R/W	[7:0]	max_r2_Gb2[7:0] (max_radial)2 at 40 % of Max_radial For RGB Shading
<1B.5Eh>	05h	SH_M_R2_GB3H	R/W	[7:0]	max_r2_Gb3[23:16] (max_radial)2 at 60 % of Max_radial For RGB Shading
<1B.5Fh>	7Eh	SH_M_R2_GB3M	R/W	[7:0]	max_r2_Gb3[15:8] (max_radial)2 at 60 % of Max_radial For RGB Shading
<1B.60h>	40h	SH_M_R2_GB3L	R/W	[7:0]	max_r2_Gb3[7:0] (max_radial)2 at 60 % of Max_radial For RGB Shading
<1B.61h>	07h	SH_M_R2_GB4H	R/W	[7:0]	max_r2_Gb4[23:16] (max_radial)2 at 70 % of Max_radial For RGB Shading
<1B.62h>	7Ah	SH_M_R2_GB4M	R/W	[7:0]	max_r2_Gb4[15:8] (max_radial)2 at 70 % of Max_radial For RGB Shading
<1B.63h>	10h	SH_M_R2_GB4L	R/W	[7:0]	max_r2_Gb4[7:0] (max_radial)2 at 70 % of Max_radial For RGB Shading
<1B.64h>	09h	SH_M_R2_GB5H	R/W	[7:0]	max_r2_Gb5[23:16] (max_radial)2 at 80 % of Max_radial For RGB Shading
<1B.65h>	C4h	SH_M_R2_GB5M	R/W	[7:0]	max_r2_Gb5[15:8] (max_radial)2 at 80 % of Max_radial For RGB Shading
<1B.66h>	00h	SH_M_R2_GB5L	R/W	[7:0]	max_r2_Gb5[7:0] (max_radial)2 at 80 % of Max_radial For RGB Shading
<1B.67h>	0Ch	SH_M_R2_GB6H	R/W	[7:0]	max_r2_Gb6[23:16] (max_radial)2 at 90 % of Max_radial For RGB Shading
<1B.68h>	5Ch	SH_M_R2_GB6M	R/W	[7:0]	max_r2_Gb6[15:8] (max_radial)2 at 90 % of Max_radial For RGB Shading
<1B.69h>	10h	SH_M_R2_GB6L	R/W	[7:0]	max_r2_Gb6[7:0] (max_radial)2 at 90 % of Max_radial For RGB Shading
<1B.6Ah>	0Fh	SH_M_R2_GB7H	R/W	[7:0]	max_r2_Gb7[23:16] (max_radial)2 at 100 % of Max_radial For RGB Shading
<1B.6Bh>	42h	SH_M_R2_GB7M	R/W	[7:0]	max_r2_Gb7[15:8] (max_radial)2 at 100 % of Max_radial For RGB Shading
<1B.6Ch>	40h	SH_M_R2_GB7L	R/W	[7:0]	max_r2_Gb7[7:0] (max_radial)2 at 100 % of Max_radial For RGB Shading
<1B.6Dh>	68h	SH_SUB_RGB0H	R/W	[7:0]	sub_range_Gb0[15:8] sub_range_Gb0 = 1 / (max_r2_Gb1-0)
<1B.6Eh>	DBh	SH_SUB_RGB0L	R/W	[7:0]	sub_range_Gb0[7:0]

Addr	Reset Value	Mnemonic	Attr	Bits	Descriptions
<1B.6Fh>	22h	SH_SUB_RGB1H	R/W	[7:0]	sub_range_Gb1[15:8] sub_range_Gb1 = 1 / (max_r2_Gb2-max_r2_Gb1)
<1B.70h>	F3h	SH_SUB_RGB1L	R/W	[7:0]	sub_range_Gb1[7:0]
<1B.71h>	14h	SH_SUB_RGB2H	R/W	[7:0]	sub_range_Gb2[15:8] sub_range_Gb2 = 1 / (max_r2_Gb3-max_r2_Gb2)
<1B.72h>	F8h	SH_SUB_RGB2L	R/W	[7:0]	sub_range_Gb2[7:0]
<1B.73h>	20h	SH_SUB_RGB3H	R/W	[7:0]	sub_range_Gb3[15:8] sub_range_Gb3 = 1 / (max_r2_Gb4-max_r2_Gb3)
<1B.74h>	43h	SH_SUB_RGB3L	R/W	[7:0]	sub_range_Gb3[7:0]
<1B.75h>	1Bh	SH_SUB_RGB4H	R/W	[7:0]	sub_range_Gb4[15:8] sub_range_Gb4 = 1 / (max_r2_Gb5-max_r2_Gb4)
<1B.76h>	F6h	SH_SUB_RGB4L	R/W	[7:0]	sub_range_Gb4[7:0]
<1B.77h>	18h	SH_SUB_RGB5H	R/W	[7:0]	sub_range_Gb5[15:8] sub_range_Gb5 = 1 / (max_r2_Gb6-max_r2_Gb5)
<1B.78h>	ACh	SH_SUB_RGB5L	R/W	[7:0]	sub_range_Gb5[7:0]
<1B.79h>	16h	SH_SUB_RGB6H	R/W	[7:0]	sub_range_Gb6[15:8] sub_range_Gb6 = 1 / (max_r2_Gb7-max_r2_Gb6)
<1B.7Ah>	13h	SH_SUB_RGB6L	R/W	[7:0]	sub_range_Gb6[7:0]
<1B.7Bh -7Fh>		**Reserved**			
<1B.80h>	00h	**XSHADE_MODE**	R/W	[7:2] [1] [0]	Reserved xs_rv_cont_r 0 : R, Gr 1st Image 1 : Gb, B 1st Image xshade_on_r 0 : xshade off , 1 : xshade on
<1B.81h>	00h	**XS_PATTERN**	R/W	[7:3] [2:1] [0]	Reserved xs_pattern_y_r y index counter offset (0 ~ 3) xs_pattern_x_r x index counter offset (0 ~ 1)
<1B.82h>	4Ch	**XS_HEIGHT**	R/W	[7:0]	XS_HEIGHT ceiling((image_height / 4) / 4)
<1B.83h>	00h	**XS_WIDTH_H**	R/W	[7:1] [0]	Reserved XS_WIDTH_H MSB [8], ceiling((image_width / 2) / 6)
<1B.84h>	86h	**XS_WIDTH_L**	R/W	[7:0]	XS_WIDTH_L LSB [7:0], ceiling((image_width / 2) / 6)
<1B.85h>	03h	**XS_STEP_Y_H**	R/W	[7:0]	XS_STEP_Y_H MSB [15:8], floor((2^16)/xs_blk_height_r)
<1B.86h>	5Eh	**XS_STEP_Y_L**	R/W	[7:0]	XS_STEP_Y_L LSB [7:0], floor((2^16)/xs_blk_height_r)

Addr	Reset Value	Mnemonic	Attr	Bits	Descriptions
<1B.87h>	00h	**XS_STEP_X_HH**	R/W	[7:2] [1:0]	Reserved XS_STEP_X_HH MSB [17:16], floor((2^18)/xs_blk_width_r)
<1B.88h>	07h	**XS_STEP_X_H**	R/W	[7:0]	XS_STEP_X_H [15:8], floor((2^18)/xs_blk_width_r)
<1B.89h>	A4h	**XS_STEP_X_L**	R/W	[7:0]	XS_STEP_X_L LSB [7:0], floor((2^18)/xs_blk_width_r)
<1B.8Ah -8Fh>		**Reserved**			
<1B.90h>	00h	**XS_DATA_00_H**	R/W	[7:3] [2:0]	Reserved XS_DATA_00_H MSB[10:8], (row, column) = (0, 0)th mesh's offset
<1B.91h>	51h	**XS_DATA_00_L**	R/W	[7:0]	XS_DATA_00_L [7:0] 1 sign + (2nd~11th) frac (max 0.25)
<1B.92h>	00h	**XS_DATA_01_H**	R/W	[7:3] [2:0]	Reserved XS_DATA_01_H MSB[10:8], (row, column) = (0, 1)th mesh's offset
<1B.93h>	78h	**XS_DATA_01_L**	R/W	[7:0]	XS_DATA_01_L [7:0] 1 sign + (2nd~11th) frac (max 0.25)
<1B.94h>	00h	**XS_DATA_02_H**	R/W	[7:3] [2:0]	Reserved XS_DATA_02_H MSB[10:8], (row, column) = (0, 2)th mesh's offset
<1B.95h>	9Ch	**XS_DATA_02_L**	R/W	[7:0]	XS_DATA_02_L [7:0] 1 sign + (2nd~11th) frac (max 0.25)
<1B.96h>	00h	**XS_DATA_03_H**	R/W	[7:3] [2:0]	Reserved XS_DATA_03_H MSB[10:8], (row, column) = (0, 3)th mesh's offset
<1B.97h>	CDh	**XS_DATA_03_L**	R/W	[7:0]	XS_DATA_03_L [7:0] 1 sign + (2nd~11th) frac (max 0.25)
<1B.98h>	01h	**XS_DATA_04_H**	R/W	[7:3] [2:0]	Reserved XS_DATA_04_H MSB[10:8], (row, column) = (0, 4)th mesh's offset
<1B.99h>	14h	**XS_DATA_04_L**	R/W	[7:0]	XS_DATA_04_L [7:0] 1 sign + (2nd~11th) frac (max 0.25)
<1B.9Ah>	01h	**XS_DATA_05_H**	R/W	[7:3] [2:0]	Reserved XS_DATA_05_H MSB[10:8], (row, column) = (0, 5)th mesh's offset
<1B.9Bh>	3Eh	**XS_DATA_05_L**	R/W	[7:0]	XS_DATA_05_L [7:0] 1 sign + (2nd~11th) frac (max 0.25)
<1B.9Ch>	01h	**XS_DATA_06_H**	R/W	[7:3] [2:0]	Reserved XS_DATA_06_H MSB[10:8], (row, column) = (0, 6)th mesh's offset
<1B.9Dh>	16h	**XS_DATA_06_L**	R/W	[7:0]	XS_DATA_06_L [7:0] 1 sign + (2nd~11th) frac (max 0.25)

Addr	Reset Value	Mnemonic	Attr	Bits	Descriptions
<1B.9Eh>	00h	**XS_DATA_10_H**	R/W	[7:3] [2:0]	Reserved XS_DATA_10_H MSB[10:8], (row, column) = (1, 0)th mesh's offset
<1B.9Fh>	31h	**XS_DATA_10_L**	R/W	[7:0]	XS_DATA_10_L [7:0] 1 sign + (2nd~11th) frac (max 0.25)
<1B.A0h>	00h	**XS_DATA_11_H**	R/W	[7:3] [2:0]	Reserved XS_DATA_11_H MSB[10:8], (row, column) = (1, 1)th mesh's offset
<1B.A1h>	4Bh	**XS_DATA_11_L**	R/W	[7:0]	XS_DATA_11_L [7:0] 1 sign + (2nd~11th) frac (max 0.25)
<1B.A2h>	00h	**XS_DATA_12_H**	R/W	[7:3] [2:0]	Reserved XS_DATA_12_H MSB[10:8], (row, column) = (1, 2)th mesh's offset
<1B.A3h>	64h	**XS_DATA_12_L**	R/W	[7:0]	XS_DATA_12_L [7:0] 1 sign + (2nd~11th) frac (max 0.25)
<1B.A4h>	00h	**XS_DATA_13_H**	R/W	[7:3] [2:0]	Reserved XS_DATA_13_H MSB[10:8], (row, column) = (1, 3)th mesh's offset
<1B.A5h>	7Ah	**XS_DATA_13_L**	R/W	[7:0]	XS_DATA_13_L [7:0] 1 sign + (2nd~11th) frac (max 0.25)
<1B.A6h>	00h	**XS_DATA_14_H**	R/W	[7:3] [2:0]	Reserved XS_DATA_14_H MSB[10:8], (row, column) = (1, 4)th mesh's offset
<1B.A7h>	C3h	**XS_DATA_14_L**	R/W	[7:0]	XS_DATA_14_L [7:0] 1 sign + (2nd~11th) frac (max 0.25)
<1B.A8h>	00h	**XS_DATA_15_H**	R/W	[7:3] [2:0]	Reserved XS_DATA_15_H MSB[10:8], (row, column) = (1, 5)th mesh's offset
<1B.A9h>	D1h	**XS_DATA_15_L**	R/W	[7:0]	XS_DATA_15_L [7:0] 1 sign + (2nd~11th) frac (max 0.25)
<1B.AAh>	00h	**XS_DATA_16_H**	R/W	[7:3] [2:0]	Reserved XS_DATA_16_H MSB[10:8], (row, column) = (1, 6)th mesh's offset
<1B.ABh>	B8h	**XS_DATA_16_L**	R/W	[7:0]	XS_DATA_16_L [7:0] 1 sign + (2nd~11th) frac (max 0.25)
<1B.ACh>	00h	**XS_DATA_20_H**	R/W	[7:3] [2:0]	Reserved XS_DATA_20_H MSB[10:8], (row, column) = (2, 0)th mesh's offset
<1B.ADh>	11h	**XS_DATA_20_L**	R/W	[7:0]	XS_DATA_20_L [7:0] 1 sign + (2nd~11th) frac (max 0.25)
<1B.AEh>	00h	**XS_DATA_21_H**	R/W	[7:3] [2:0]	Reserved XS_DATA_21_H MSB[10:8], (row, column) = (2, 1)th mesh's offset
<1B.AFh>	16h	**XS_DATA_21_L**	R/W	[7:0]	XS_DATA_21_L

Addr	Reset Value	Mnemonic	Attr	Bits	Descriptions
					[7:0] 1 sign + (2nd~11th) frac (max 0.25)
<1B.B0h>	00h	**XS_DATA_22_H**	R/W	[7:3] [2:0]	Reserved XS_DATA_22_H MSB[10:8], (row, column) = (2, 2)th mesh's offset
<1B.B1h>	02h	**XS_DATA_22_L**	R/W	[7:0]	XS_DATA_22_L [7:0] 1 sign + (2nd~11th) frac (max 0.25)
<1B.B2h>	07h	**XS_DATA_23_H**	R/W	[7:3] [2:0]	Reserved XS_DATA_23_H MSB[10:8], (row, column) = (2, 3)th mesh's offset
<1B.B3h>	F3h	**XS_DATA_23_L**	R/W	[7:0]	XS_DATA_23_L [7:0] 1 sign + (2nd~11th) frac (max 0.25)
<1B.B4h>	07h	**XS_DATA_24_H**	R/W	[7:3] [2:0]	Reserved XS_DATA_24_H MSB[10:8], (row, column) = (2, 4)th mesh's offset
<1B.B5h>	F3h	**XS_DATA_24_L**	R/W	[7:0]	XS_DATA_24_L [7:0] 1 sign + (2nd~11th) frac (max 0.25)
<1B.B6h>	07h	**XS_DATA_25_H**	R/W	[7:3] [2:0]	Reserved XS_DATA_25_H MSB[10:8], (row, column) = (2, 5)th mesh's offset
<1B.B7h>	F8h	**XS_DATA_25_L**	R/W	[7:0]	XS_DATA_25_L [7:0] 1 sign + (2nd~11th) frac (max 0.25)
<1B.B8h>	07h	**XS_DATA_26_H**	R/W	[7:3] [2:0]	Reserved XS_DATA_26_H MSB[10:8], (row, column) = (2, 6)th mesh's offset
<1B.B9h>	F1h	**XS_DATA_26_L**	R/W	[7:0]	XS_DATA_26_L [7:0] 1 sign + (2nd~11th) frac (max 0.25)
<1B.BAh>	07h	**XS_DATA_30_H**	R/W	[7:3] [2:0]	Reserved XS_DATA_30_H MSB[10:8], (row, column) = (3, 0)th mesh's offset
<1B.BBh>	EEh	**XS_DATA_30_L**	R/W	[7:0]	XS_DATA_30_L [7:0] 1 sign + (2nd~11th) frac (max 0.25)
<1B.BCh>	07h	**XS_DATA_31_H**	R/W	[7:3] [2:0]	Reserved XS_DATA_31_H MSB[10:8], (row, column) = (3, 1)th mesh's offset
<1B.BDh>	D8h	**XS_DATA_31_L**	R/W	[7:0]	XS_DATA_31_L [7:0] 1 sign + (2nd~11th) frac (max 0.25)
<1B.BEh>	07h	**XS_DATA_32_H**	R/W	[7:3] [2:0]	Reserved XS_DATA_32_H MSB[10:8], (row, column) = (3, 2)th mesh's offset
<1B.BFh>	B5h	**XS_DATA_32_L**	R/W	[7:0]	XS_DATA_32_L [7:0] 1 sign + (2nd~11th) frac (max 0.25)
<1B.C0h>	07h	**XS_DATA_33_H**	R/W	[7:3] [2:0]	Reserved XS_DATA_33_H MSB[10:8], (row, column) = (3, 3)th mesh's offset

Addr	Reset Value	Mnemonic	Attr	Bits	Descriptions
<1B.C1h>	7Fh	**XS_DATA_33_L**	R/W	[7:0]	XS_DATA_33_L [7:0] 1 sign + (2nd~11th) frac (max 0.25)
<1B.C2h>	07h	**XS_DATA_34_H**	R/W	[7:3] [2:0]	Reserved XS_DATA_34_H MSB[10:8], (row, column) = (3, 4)th mesh's offset
<1B.C3h>	49h	**XS_DATA_34_L**	R/W	[7:0]	XS_DATA_34_L [7:0] 1 sign + (2nd~11th) frac (max 0.25)
<1B.C4h>	07h	**XS_DATA_35_H**	R/W	[7:3] [2:0]	Reserved XS_DATA_35_H MSB[10:8], (row, column) = (3, 5)th mesh's offset
<1B.C5h>	49h	**XS_DATA_35_L**	R/W	[7:0]	XS_DATA_35_L [7:0] 1 sign + (2nd~11th) frac (max 0.25)
<1B.C6h>	07h	**XS_DATA_36_H**	R/W	[7:3] [2:0]	Reserved XS_DATA_36_H MSB[10:8], (row, column) = (3, 6)th mesh's offset
<1B.C7h>	5Fh	**XS_DATA_36_L**	R/W	[7:0]	XS_DATA_36_L [7:0] 1 sign + (2nd~11th) frac (max 0.25)
<1B.C8h>	07h	**XS_DATA_40_H**	R/W	[7:3] [2:0]	Reserved XS_DATA_40_H MSB[10:8], (row, column) = (4, 0)th mesh's offset
<1B.C9h>	CFh	**XS_DATA_40_L**	R/W	[7:0]	XS_DATA_40_L [7:0] 1 sign + (2nd~11th) frac (max 0.25)
<1B.CAh>	07h	**XS_DATA_41_H**	R/W	[7:3] [2:0]	Reserved XS_DATA_41_H MSB[10:8], (row, column) = (4, 1)th mesh's offset
<1B.CBh>	AAh	**XS_DATA_41_L**	R/W	[7:0]	XS_DATA_41_L [7:0] 1 sign + (2nd~11th) frac (max 0.25)
<1B.CCh>	07h	**XS_DATA_42_H**	R/W	[7:3] [2:0]	Reserved XS_DATA_42_H MSB[10:8], (row, column) = (4, 2)th mesh's offset
<1B.CDh>	6Fh	**XS_DATA_42_L**	R/W	[7:0]	XS_DATA_42_L [7:0] 1 sign + (2nd~11th) frac (max 0.25)
<1B.CEh>	07h	**XS_DATA_43_H**	R/W	[7:3] [2:0]	Reserved XS_DATA_43_H MSB[10:8], (row, column) = (4, 3)th mesh's offset
<1B.CFh>	28h	**XS_DATA_43_L**	R/W	[7:0]	XS_DATA_43_L [7:0] 1 sign + (2nd~11th) frac (max 0.25)
<1B.D0h>	06h	**XS_DATA_44_H**	R/W	[7:3] [2:0]	Reserved XS_DATA_44_H MSB[10:8], (row, column) = (4, 4)th mesh's offset
<1B.D1h>	ECh	**XS_DATA_44_L**	R/W	[7:0]	XS_DATA_44_L [7:0] 1 sign + (2nd~11th) frac (max 0.25)
<1B.D2h>	06h	**XS_DATA_45_H**	R/W	[7:3] [2:0]	Reserved XS_DATA_45_H

Addr	Reset Value	Mnemonic	Attr	Bits	Descriptions
					MSB[10:8], (row, column) = (4, 5)th mesh's offset
<1B.D3h>	D7h	**XS_DATA_45_L**	R/W	[7:0]	XS_DATA_45_L [7:0] 1 sign + (2^{nd}~11th) frac (max 0.25)
<1B.D4h>	07h	**XS_DATA_46_H**	R/W	[7:3] [2:0]	Reserved XS_DATA_46_H MSB[10:8], (row, column) = (4, 6)th mesh's offset
<1B.D5h>	0Fh	**XS_DATA_46_L**	R/W	[7:0]	XS_DATA_46_L [7:0] 1 sign + (2nd~11th) frac (max 0.25)

16. SHADING REGISTER MAP (PAGE 1CH)

* Shading Page (Page 0x1C) Registers will be loaded to Target Registers (ISP registers) when performing Image Format command <0.02h> or <0.73h> or <0.74h>.

* Shading Table Index
  case of (Image Format Table Index = 0)
    Shading Index = <3.2Fh>
  case of (Image Format Table Index = 1)
    Shading Index = <4.5Fh>
  case of (Image Format Table Index = 2)
    Boundary Index = <4.8Fh>

* SH_VAL(<00h~17h>) registers will be loaded when option <0.24h>[7] is on
- if you use 1/4 sub-sampling table then SH_VAL table(=table index of 1/4 sub-sampling) will be loaded
- or not table index 00h's SH_VAL will be loaded.

Table 1. Shading Table

Address 1	Address 2	ODM Index	Size
00h~1Fh	E0h~E3h	00h	H = 1,V = 1
20h~3Fh	E4h~E7h	10h	H = 2,V = 1
40h~5Fh	E8h~EBh	20h	H = 1,V = 2
60h~7Fh	ECh~EFh	30h	H = 2,V = 2
80h~9Fh	F0h~F3h	40h	H = 4,V = 1
A0h~BFh	F4h~F7h	50h	H = 4,V = 4
C0h~DFh	F8h~FBh	60h	Reserved

Table 2. Detailed register Table of Table 1 – Page 1Ch (Attribute of all these values is R/W)

Addr1 [4:0]	Target Register	Bits	Descriptions	Table Index 00h	Table Index 10h	Table Index 20h	Table Index 30h	Table Index 40h	Table Index 50h	Table Index 60h
00h	<9.35h>	[3:0]	SH_VAL_R0H	01h	01h	01h	01h	01h	01h	01h
01h	<9.36h>	[7:0]	SH_VAL_R0L	00h	00h	00h	00h	00h	00h	00h
02h	<9.37h>	[3:0]	SH_VAL_R1H	01h	01h	01h	01h	01h	01h	01h
03h	<9.38h>	[7:0]	SH_VAL_R1L	00h	00h	00h	00h	00h	00h	00h
04h	<9.39h>	[3:0]	SH_VAL_R2H	01h	01h	01h	01h	01h	01h	01h
05h	<9.3Ah>	[7:0]	SH_VAL_R2L	00h	00h	00h	00h	00h	00h	00h
06h	<9.45h>	[3:0]	SH_VAL_G0H	01h	01h	01h	01h	01h	01h	01h
07h	<9.46h>	[7:0]	SH_VAL_G0L	00h	00h	00h	00h	00h	00h	00h
08h	<9.47h>	[3:0]	SH_VAL_G1H	01h	01h	01h	01h	01h	01h	01h
09h	<9.48h>	[7:0]	SH_VAL_G1L	00h	00h	00h	00h	00h	00h	00h

Addr1 [4:0]	Target Register	Bits	Descriptions	Table Index 00h	Table Index 10h	Table Index 20h	Table Index 30h	Table Index 40h	Table Index 50h	Table Index 60h
0Ah	<9.49h>	[3:0]	SH_VAL_G2H	01h	01h	01h	01h	01h	01h	01h
0Bh	<9.4Ah>	[7:0]	SH_VAL_G2L	00h	00h	00h	00h	00h	00h	00h
0Ch	<9.55h>	[3:0]	SH_VAL_B0H	01h	01h	01h	01h	01h	01h	01h
0Dh	<9.56h>	[7:0]	SH_VAL_B0L	00h	00h	00h	00h	00h	00h	00h
0Eh	<9.57h>	[3:0]	SH_VAL_B1H	01h	01h	01h	01h	01h	01h	01h
0Fh	<9.58h>	[7:0]	SH_VAL_B1L	00h	00h	00h	00h	00h	00h	00h
10h	<9.59h>	[3:0]	SH_VAL_B2H	01h	01h	01h	01h	01h	01h	01h
11h	<9.5Ah>	[7:0]	SH_VAL_B2L	00h	00h	00h	00h	00h	00h	00h
12h	<1B.48h>	[3:0]	SH_VAL_GB0H	01h	01h	01h	01h	01h	01h	01h
13h	<1B.49h>	[7:0]	SH_VAL_GB0L	00h	00h	00h	00h	00h	00h	00h
14h	<1B.4Ah>	[3:0]	SH_VAL_GB1H	01h	01h	01h	01h	01h	01h	01h
15h	<1B.4Bh>	[7:0]	SH_VAL_GB1L	00h	00h	00h	00h	00h	00h	00h
16h	<1B.4Ch>	[3:0]	SH_VAL_GB2H	01h	01h	01h	01h	01h	01h	01h
17h	<1B.4Dh>	[7:0]	SH_VAL_GB2L	00h	00h	00h	00h	00h	00h	00h
18h	<1B.82h>	[7:0]	XS_HEIGHT	4Ch	4Ch	26h	26h	4Ch	13h	4Ch
19h	<1B.83h>	[0]	XS_WIDTH_H	00h	00h	00h	00h	00h	00h	00h
1Ah	<1B.84h>	[7:0]	XS_WIDTH_L	86h	43h	86h	43h	22h	22h	86h
1Bh	<1B.85h>	[7:0]	XS_STEP_Y_H	03h	03h	06h	06h	03h	0Dh	03h
1Ch	<1B.86h>	[7:0]	XS_STEP_Y_L	5Eh	5Eh	BCh	BCh	5Eh	79h	5Eh
1Dh	<1B.87h>	[1:0]	XS_STEP_X_HH	00h	00h	00h	00h	00h	00h	00h
1Eh	<1B.88h>	[7:0]	XS_STEP_X_H	07h	0Fh	07h	0Fh	1Eh	1Eh	07h
1Fh	<1B.89h>	[7:0]	XS_STEP_XL	A4h	48h	A4h	48h	1Eh	1Eh	A4h
Addr2 [1:0]	**Target Register**	**Bits**	**Descriptions**	**Table Index 00h**	**Table Index 10h**	**Table Index 20h**	**Table Index 30h**	**Table Index 40h**	**Table Index 50h**	**Table Index 60h**
E0h	None	[7:0]	SH_DEL_EW_GAIN	01h	02h	01h	02h	02h	02h	01h
E1h	None	[7:0]	SH_DEL_NS_GAIN	01h	01h	02h	02h	01h	02h	01h
E2h	None	[7:0]	SH_XC_GAIN	01h	01h	01h	01h	02h	02h	01h
E3h	None	[7:0]	SH_YC_GAIN	01h	01h	01h	01h	01h	02h	01h

17. GAMMA & EDGE REGISTER MAP (PAGE 1DH)

Addr	Reset Value	Mnemonic	Attr	Bits	Descriptions
<1D.00h>	08h	**RGM1L**	R/W	[7:0]	LSB 7:0 of R Channel Gamma Correction Coefficient 1 (x = 8)
<1D.01h>	10h	**RGM2L**	R/W	[7:0]	LSB 7:0 of R Channel Gamma Correction Coefficient 2 (x = 16)
<1D.02h>	20h	**RGM3L**	R/W	[7:0]	LSB 7:0 of R Channel Gamma Correction Coefficient 3 (x = 32)
<1D.03h>	40h	**RGM4L**	R/W	[7:0]	LSB 7:0 of R Channel Gamma Correction Coefficient 4 (x = 64)
<1D.04h>	00h	**RGM_14H**	R/W	[7:6] [5:4] [3:2] [1:0]	RGM1L[9:8], MSB 9:8 of R Channel Gamma Correction Coefficient 1 (x = 8) RGM2L[9:8], MSB 9:8 of R Channel Gamma Correction Coefficient 2 (x = 16) RGM3L[9:8], MSB 9:8 of R Channel Gamma Correction Coefficient 3 (x = 32) RGM4L[9:8], MSB 9:8 of R Channel Gamma Correction Coefficient 4 (x = 64)
<1D.05h>	60h	**RGM5L**	R/W	[7:0]	LSB 7:0 of R Channel Gamma Correction Coefficient 5 (x = 96)
<1D.06h>	80h	**RGM6L**	R/W	[7:0]	LSB 7:0 of R Channel Gamma Correction Coefficient 6 (x = 128)
<1D.07h>	A0h	**RGM7L**	R/W	[7:0]	LSB 7:0 of R Channel Gamma Correction Coefficient 7 (x = 160)
<1D.08h>	C0h	**RGM8L**	R/W	[7:0]	LSB 7:0 of R Channel Gamma Correction Coefficient 8 (x = 192)
<1D.09h>	00h	**RGM_58H**	R/W	[7:6] [5:4] [3:2] [1:0]	RGM5L[9:8], MSB 9:8 of R Channel Gamma Correction Coefficient 5 (x =96) RGM6L[9:8], MSB 9:8 of R Channel Gamma Correction Coefficient 6 (x = 128) RGM7L[9:8], MSB 9:8 of R Channel Gamma Correction Coefficient 7 (x = 160) RGM8L[9:8], MSB 9:8 of R Channel Gamma Correction Coefficient 8 (x = 192)
<1D.0Ah>	E0h	**RGM9L**	R/W	[7:0]	LSB 7:0 of R Channel Gamma Correction Coefficient 9 (x = 224)
<1D.0Bh>	00h	**RGM10L**	R/W	[7:0]	LSB 7:0 of R Channel Gamma Correction Coefficient 10 (x = 256)
<1D.0Ch>	20h	**RGM11L**	R/W	[7:0]	LSB 7:0 of R Channel Gamma Correction Coefficient 11 (x = 288)
<1D.0Dh>	40h	**RGM12L**	R/W	[7:0]	LSB 7:0 of R Channel Gamma Correction Coefficient 12 (x = 320)
<1D.0Eh>	15h	**RGM912H**	R/W	[7:6] [5:4] [3:2] [1:0]	RGM9L[9:8], MSB 9:8 of R Channel Gamma Correction Coefficient 9 (x = 352) RGM10L[9:8], MSB 9:8 of R Channel Gamma Correction Coefficient 10 (x = 384) RGM11L[9:8], MSB 9:8 of R Channel Gamma Correction Coefficient 11 (x = 416) RGM12L[9:8], MSB 9:8 of R Channel Gamma Correction Coefficient 12 (x = 448)
<1D.0Fh>	60h	**RGM13L**	R/W	[7:0]	LSB 7:0 of R Channel Gamma Correction Coefficient 13 (x = 352)
<1D.10h>	80h	**RGM14L**	R/W	[7:0]	LSB 7:0 of R Channel Gamma Correction Coefficient 14 (x = 384)
<1D.11h>	A0h	**RGM15L**	R/W	[7:0]	LSB 7:0 of R Channel Gamma Correction Coefficient 15 (x = 416)
<1D.12h>	C0h	**RGM16L**	R/W	[7:0]	LSB 7:0 of R Channel Gamma Correction Coefficient 16 (x = 448)
<1D.13h>	55h	**RGM1316H**	R/W	[7:6] [5:4] [3:2] [1:0]	RGM13L[9:8], MSB 9:8 of R Channel Gamma Correction Coefficient 13 (x = 352) RGM14L[9:8], MSB 9:8 of R Channel Gamma Correction Coefficient 14 (x = 384) RGM15L[9:8], MSB 9:8 of R Channel Gamma Correction Coefficient 15 (x = 416) RGM16L[9:8], MSB 9:8 of R Channel Gamma Correction Coefficient 16 (x = 448)
<1D.14h>	E0h	**RGM17L**	R/W	[7:0]	LSB 7:0 of R Channel Gamma Correction Coefficient 17 (x = 480)
<1D.15h>	00h	**RGM18L**	R/W	[7:0]	LSB 7:0 of R Channel Gamma Correction Coefficient 18 (x = 512)
<1D.16h>	20h	**RGM19L**	R/W	[7:0]	LSB 7:0 of R Channel Gamma Correction Coefficient 19 (x = 544)
<1D.17h>	40h	**RGM20L**	R/W	[7:0]	LSB 7:0 of R Channel Gamma Correction Coefficient 20 (x = 576)
<1D.18h>	6Ah	**RGM1720H**	R/W	[7:6]	RGM17L[9:8], MSB 9:8 of R Channel Gamma Correction Coefficient 17 (x = 480)

Addr	Reset Value	Mnemonic	Attr	Bits	Descriptions
				[5:4] [3:2] [1:0]	RGM18L[9:8], MSB 9:8 of R Channel Gamma Correction Coefficient 18 (x = 512) RGM19L[9:8], MSB 9:8 of R Channel Gamma Correction Coefficient 19 (x = 544) RGM20L[9:8], MSB 9:8 of R Channel Gamma Correction Coefficient 20 (x = 576)
<1D.19h>	60h	**RGM21L**	R/W	[7:0]	LSB 7:0 of R Channel Gamma Correction Coefficient 21 (x = 608)
<1D.1Ah>	80h	**RGM22L**	R/W	[7:0]	LSB 7:0 of R Channel Gamma Correction Coefficient 22 (x = 640)
<1D.1Bh>	A0h	**RGM23L**	R/W	[7:0]	LSB 7:0 of R Channel Gamma Correction Coefficient 23 (x = 672)
<1D.1Ch>	C0h	**RGM24L**	R/W	[7:0]	LSB 7:0 of R Channel Gamma Correction Coefficient 24 (x = 704)
<1D.1Dh>	AAh	**RGM2124H**	R/W	[7:6] [5:4] [3:2] [1:0]	RGM21L[9:8], MSB 9:8 of R Channel Gamma Correction Coefficient 21 (x = 608) RGM22L[9:8], MSB 9:8 of R Channel Gamma Correction Coefficient 22 (x = 640) RGM23L[9:8], MSB 9:8 of R Channel Gamma Correction Coefficient 23 (x = 672) RGM24L[9:8], MSB 9:8 of R Channel Gamma Correction Coefficient 24 (x = 704)
<1D.1Eh>	E0h	**RGM25L**	R/W	[7:0]	LSB 7:0 of R Channel Gamma Correction Coefficient 25 (x = 736)
<1D.1Fh>	00h	**RGM26L**	R/W	[7:0]	LSB 7:0 of R Channel Gamma Correction Coefficient 26 (x = 768)
<1D.20h>	20h	**RGM27L**	R/W	[7:0]	LSB 7:0 of R Channel Gamma Correction Coefficient 27 (x = 800)
<1D.21h>	40h	**RGM28L**	R/W	[7:0]	LSB 7:0 of R Channel Gamma Correction Coefficient 28 (x = 832)
<1D.22h>	BFh	**RGM2528H**	R/W	[7:6] [5:4] [3:2] [1:0]	RGM25L[9:8], MSB 9:8 of R Channel Gamma Correction Coefficient 25 (x = 736) RGM26L[9:8], MSB 9:8 of R Channel Gamma Correction Coefficient 26 (x = 768) RGM27L[9:8], MSB 9:8 of R Channel Gamma Correction Coefficient 27 (x = 800) RGM28L[9:8], MSB 9:8 of R Channel Gamma Correction Coefficient 28 (x = 832)
<1D.23h>	60h	**RGM29L**	R/W	[7:0]	LSB 7:0 of R Channel Gamma Correction Coefficient 29 (x = 864)
<1D.24h>	80h	**RGM30L**	R/W	[7:0]	LSB 7:0 of R Channel Gamma Correction Coefficient 30 (x = 896)
<1D.25h>	A0h	**RGM31L**	R/W	[7:0]	LSB 7:0 of R Channel Gamma Correction Coefficient 31 (x = 928)
<1D.26h>	C0h	**RGM32L**	R/W	[7:0]	LSB 7:0 of R Channel Gamma Correction Coefficient 32 (x = 960)
<1D.27h>	FFh	**RGM2932H**	R/W	[7:6] [5:4] [3:2] [1:0]	RGM29L[9:8], MSB 9:8 of R Channel Gamma Correction Coefficient 29 (x = 864) RGM30L[9:8], MSB 9:8 of R Channel Gamma Correction Coefficient 30 (x = 896) RGM31L[9:8], MSB 9:8 of R Channel Gamma Correction Coefficient 31 (x = 928) RGM32L[9:8], MSB 9:8 of R Channel Gamma Correction Coefficient 32 (x = 960)
<1D.28h>	E0h	**RGM33L**	R/W	[7:0]	LSB 7:0 of R Channel Gamma Correction Coefficient 33 (x = 992)
<1D.29h>	FFh	**RGM34L**	R/W	[7:0]	LSB 7:0 of R Channel Gamma Correction Coefficient 34 (x = 1024)
<1D.2Ah>	F0h	**RGM3334H**	R/W	[7:6] [5:4] [3:0]	RGM33L[9:8], MSB 9:8 of R Channel Gamma Correction Coefficient 33 (x = 992) RGM34L[9:8], MSB 9:8 of R Channel Gamma Correction Coefficient 34 (x = 1024) Reserved
<1D.2Bh>	08h	**GGM1L**	R/W	[7:0]	LSB 7:0 of G Channel Gamma Correction Coefficient 1 (x = 8)
<1D.2Ch>	10h	**GGM2L**	R/W	[7:0]	LSB 7:0 of G Channel Gamma Correction Coefficient 2 (x = 16)
<1D.2Dh>	20h	**GGM3L**	R/W	[7:0]	LSB 7:0 of G Channel Gamma Correction Coefficient 3 (x = 32)
<1D.2Eh>	40h	**GGM4L**	R/W	[7:0]	LSB 7:0 of G Channel Gamma Correction Coefficient 4 (x = 64)
<1D.2Fh>	00h	**GGM_14H**	R/W	[7:6] [5:4] [3:2] [1:0]	GGM1L[9:8], MSB 9:8 of G Channel Gamma Correction Coefficient 1 (x = 8) GGM2L[9:8], MSB 9:8 of G Channel Gamma Correction Coefficient 2 (x = 16) GGM3L[9:8], MSB 9:8 of G Channel Gamma Correction Coefficient 3 (x = 32) GGM4L[9:8], MSB 9:8 of G Channel Gamma Correction Coefficient 4 (x = 64)

Addr	Reset Value	Mnemonic	Attr	Bits	Descriptions
<1D.30h>	60h	**GGM5L**	R/W	[7:0]	LSB 7:0 of G Channel Gamma Correction Coefficient 5 (x = 96)
<1D.31h>	80h	**GGM6L**	R/W	[7:0]	LSB 7:0 of G Channel Gamma Correction Coefficient 6 (x = 128)
<1D.32h>	A0h	**GGM7L**	R/W	[7:0]	LSB 7:0 of G Channel Gamma Correction Coefficient 7 (x = 160)
<1D.33h>	C0h	**GGM8L**	R/W	[7:0]	LSB 7:0 of G Channel Gamma Correction Coefficient 8 (x = 192)
<1D.34h>	00h	**GGM_58H**	R/W	[7:6] [5:4] [3:2] [1:0]	GGM5L[9:8], MSB 9:8 of G Channel Gamma Correction Coefficient 5 (x =96) GGM6L[9:8], MSB 9:8 of G Channel Gamma Correction Coefficient 6 (x = 128) GGM7L[9:8], MSB 9:8 of G Channel Gamma Correction Coefficient 7 (x = 160) GGM8L[9:8], MSB 9:8 of G Channel Gamma Correction Coefficient 8 (x = 192)
<1D.35h>	E0h	**GGM9L**	R/W	[7:0]	LSB 7:0 of G Channel Gamma Correction Coefficient 9 (x = 224)
<1D.36h>	00h	**GGM10L**	R/W	[7:0]	LSB 7:0 of G Channel Gamma Correction Coefficient 10 (x = 256)
<1D.37h>	20h	**GGM11L**	R/W	[7:0]	LSB 7:0 of G Channel Gamma Correction Coefficient 11 (x = 288)
<1D.38h>	40h	**GGM12L**	R/W	[7:0]	LSB 7:0 of G Channel Gamma Correction Coefficient 12 (x = 320)
<1D.39h>	15h	**GGM912H**	R/W	[7:6] [5:4] [3:2] [1:0]	GGM9L[9:8], MSB 9:8 of G Channel Gamma Correction Coefficient 9 (x = 352) GGM10L[9:8], MSB 9:8 of G Channel Gamma Correction Coefficient 10 (x = 384) GGM11L[9:8], MSB 9:8 of G Channel Gamma Correction Coefficient 11 (x = 416) GGM12L[9:8], MSB 9:8 of G Channel Gamma Correction Coefficient 12 (x = 448)
<1D.3Ah>	60h	**GGM13L**	R/W	[7:0]	LSB 7:0 of G Channel Gamma Correction Coefficient 13 (x = 352)
<1D.3Bh>	80h	**GGM14L**	R/W	[7:0]	LSB 7:0 of G Channel Gamma Correction Coefficient 14 (x = 384)
<1D.3Ch>	A0h	**GGM15L**	R/W	[7:0]	LSB 7:0 of G Channel Gamma Correction Coefficient 15 (x = 416)
<1D.3Dh>	C0h	**GGM16L**	R/W	[7:0]	LSB 7:0 of G Channel Gamma Correction Coefficient 16 (x = 448)
<1D.3Eh>	55h	**GGM1316H**	R/W	[7:6] [5:4] [3:2] [1:0]	GGM13L[9:8], MSB 9:8 of G Channel Gamma Correction Coefficient 13 (x = 352) GGM14L[9:8], MSB 9:8 of G Channel Gamma Correction Coefficient 14 (x = 384) GGM15L[9:8], MSB 9:8 of G Channel Gamma Correction Coefficient 15 (x = 416) GGM16L[9:8], MSB 9:8 of G Channel Gamma Correction Coefficient 16 (x = 448)
<1D.3Fh>	E0h	**GGM17L**	R/W	[7:0]	LSB 7:0 of G Channel Gamma Correction Coefficient 17 (x = 480)
<1D.40h>	00h	**GGM18L**	R/W	[7:0]	LSB 7:0 of G Channel Gamma Correction Coefficient 18 (x = 512)
<1D.41h>	20h	**GGM19L**	R/W	[7:0]	LSB 7:0 of G Channel Gamma Correction Coefficient 19 (x = 544)
<1D.42h>	40h	**GGM20L**	R/W	[7:0]	LSB 7:0 of G Channel Gamma Correction Coefficient 20 (x = 576)
<1D.43h>	6Ah	**GGM1720H**	R/W	[7:6] [5:4] [3:2] [1:0]	GGM17L[9:8], MSB 9:8 of G Channel Gamma Correction Coefficient 17 (x = 480) GGM18L[9:8], MSB 9:8 of G Channel Gamma Correction Coefficient 18 (x = 512) GGM19L[9:8], MSB 9:8 of G Channel Gamma Correction Coefficient 19 (x = 544) GGM20L[9:8], MSB 9:8 of G Channel Gamma Correction Coefficient 20 (x = 576)
<1D.44h>	60h	**GGM21L**	R/W	[7:0]	LSB 7:0 of G Channel Gamma Correction Coefficient 21 (x = 608)
<1D.45h>	80h	**GGM22L**	R/W	[7:0]	LSB 7:0 of G Channel Gamma Correction Coefficient 22 (x = 640)
<1D.46h>	A0h	**GGM23L**	R/W	[7:0]	LSB 7:0 of G Channel Gamma Correction Coefficient 23 (x = 672)
<1D.47h>	C0h	**GGM24L**	R/W	[7:0]	LSB 7:0 of G Channel Gamma Correction Coefficient 24 (x = 704)
<1D.48h>	AAh	**GGM2124H**	R/W	[7:6] [5:4] [3:2] [1:0]	GGM21L[9:8], MSB 9:8 of G Channel Gamma Correction Coefficient 21 (x = 608) GGM22L[9:8], MSB 9:8 of G Channel Gamma Correction Coefficient 22 (x = 640) GGM23L[9:8], MSB 9:8 of G Channel Gamma Correction Coefficient 23 (x = 672) GGM24L[9:8], MSB 9:8 of G Channel Gamma Correction Coefficient 24 (x = 704)

Addr	Reset Value	Mnemonic	Attr	Bits	Descriptions
<1D.49h>	E0h	**GGM25L**	R/W	[7:0]	LSB 7:0 of G Channel Gamma Correction Coefficient 25 (x = 736)
<1D.4Ah>	00h	**GGM26L**	R/W	[7:0]	LSB 7:0 of G Channel Gamma Correction Coefficient 26 (x = 768)
<1D.4Bh>	20h	**GGM27L**	R/W	[7:0]	LSB 7:0 of G Channel Gamma Correction Coefficient 27 (x = 800)
<1D.4Ch>	40h	**GGM28L**	R/W	[7:0]	LSB 7:0 of G Channel Gamma Correction Coefficient 28 (x = 832)
<1D.4Dh>	BFh	**GGM2528H**	R/W	[7:6] [5:4] [3:2] [1:0]	GGM25L[9:8], MSB 9:8 of G Channel Gamma Correction Coefficient 25 (x = 736) GGM26L[9:8], MSB 9:8 of G Channel Gamma Correction Coefficient 26 (x = 768) GGM27L[9:8], MSB 9:8 of G Channel Gamma Correction Coefficient 27 (x = 800) GGM28L[9:8], MSB 9:8 of G Channel Gamma Correction Coefficient 28 (x = 832)
<1D.4Eh>	60h	**GGM29L**	R/W	[7:0]	LSB 7:0 of G Channel Gamma Correction Coefficient 29 (x = 864)
<1D.4Fh>	80h	**GGM30L**	R/W	[7:0]	LSB 7:0 of G Channel Gamma Correction Coefficient 30 (x = 896)
<1D.50h>	A0h	**GGM31L**	R/W	[7:0]	LSB 7:0 of G Channel Gamma Correction Coefficient 31 (x = 928)
<1D.51h>	C0h	**GGM32L**	R/W	[7:0]	LSB 7:0 of G Channel Gamma Correction Coefficient 32 (x = 960)
<1D.52h>	FFh	**GGM2932H**	R/W	[7:6] [5:4] [3:2] [1:0]	GGM29L[9:8], MSB 9:8 of G Channel Gamma Correction Coefficient 29 (x = 864) GGM30L[9:8], MSB 9:8 of G Channel Gamma Correction Coefficient 30 (x = 896) GGM31L[9:8], MSB 9:8 of G Channel Gamma Correction Coefficient 31 (x = 928) GGM32L[9:8], MSB 9:8 of G Channel Gamma Correction Coefficient 32 (x = 960)
<1D.53h>	E0h	**GGM33L**	R/W	[7:0]	LSB 7:0 of G Channel Gamma Correction Coefficient 33 (x = 992)
<1D.54h>	FFh	**GGM34L**	R/W	[7:0]	LSB 7:0 of G Channel Gamma Correction Coefficient 34 (x = 1024)
<1D.55h>	F0h	**GGM3334H**	R/W	[7:6] [5:4] [3:0]	GGM33L[9:8], MSB 9:8 of G Channel Gamma Correction Coefficient 33 (x = 992) GGM34L[9:8], MSB 9:8 of G Channel Gamma Correction Coefficient 34 (x = 1024) Reserved
<1D.56h>	08h	**BGM1L**	R/W	[7:0]	LSB 7:0 of B Channel Gamma Correction Coefficient 1 (x = 8)
<1D.57h>	10h	**BGM2L**	R/W	[7:0]	LSB 7:0 of B Channel Gamma Correction Coefficient 2 (x = 16)
<1D.58h>	20h	**BGM3L**	R/W	[7:0]	LSB 7:0 of B Channel Gamma Correction Coefficient 3 (x = 32)
<1D.59h>	40h	**BGM4L**	R/W	[7:0]	LSB 7:0 of B Channel Gamma Correction Coefficient 4 (x = 64)
<1D.5Ah>	00h	**BGM_14H**	R/W	[7:6] [5:4] [3:2] [1:0]	BGM1L[9:8], MSB 9:8 of B Channel Gamma Correction Coefficient 1 (x = 8) BGM2L[9:8], MSB 9:8 of B Channel Gamma Correction Coefficient 2 (x = 16) BGM3L[9:8], MSB 9:8 of B Channel Gamma Correction Coefficient 3 (x = 32) BGM4L[9:8], MSB 9:8 of B Channel Gamma Correction Coefficient 4 (x = 64)
<1D.5Bh>	60h	**BGM5L**	R/W	[7:0]	LSB 7:0 of B Channel Gamma Correction Coefficient 5 (x = 96)
<1D.5Ch>	80h	**BGM6L**	R/W	[7:0]	LSB 7:0 of B Channel Gamma Correction Coefficient 6 (x = 128)
<1D.5Dh>	A0h	**BGM7L**	R/W	[7:0]	LSB 7:0 of B Channel Gamma Correction Coefficient 7 (x = 160)
<1D.5Eh>	C0h	**BGM8L**	R/W	[7:0]	LSB 7:0 of B Channel Gamma Correction Coefficient 8 (x = 192)
<1D.5Fh>	00h	**BGM_58H**	R/W	[7:6] [5:4] [3:2] [1:0]	BGM5L[9:8], MSB 9:8 of B Channel Gamma Correction Coefficient 5 (x =96) BGM6L[9:8], MSB 9:8 of B Channel Gamma Correction Coefficient 6 (x = 128) BGM7L[9:8], MSB 9:8 of B Channel Gamma Correction Coefficient 7 (x = 160) BGM8L[9:8], MSB 9:8 of B Channel Gamma Correction Coefficient 8 (x = 192)
<1D.60h>	E0h	**BGM9L**	R/W	[7:0]	LSB 7:0 of B Channel Gamma Correction Coefficient 9 (x = 224)
<1D.61h>	00h	**BGM10L**	R/W	[7:0]	LSB 7:0 of B Channel Gamma Correction Coefficient 10 (x = 256)

Addr	Reset Value	Mnemonic	Attr	Bits	Descriptions
<1D.62h>	20h	**BGM11L**	R/W	[7:0]	LSB 7:0 of B Channel Gamma Correction Coefficient 11 (x = 288)
<1D.63h>	40h	**BGM12L**	R/W	[7:0]	LSB 7:0 of B Channel Gamma Correction Coefficient 12 (x = 320)
<1D.64h>	15h	**BGM912H**	R/W	[7:6] [5:4] [3:2] [1:0]	BGM9L[9:8], MSB 9:8 of B Channel Gamma Correction Coefficient 9 (x = 352) BGM10L[9:8], MSB 9:8 of B Channel Gamma Correction Coefficient 10 (x = 384) BGM11L[9:8], MSB 9:8 of B Channel Gamma Correction Coefficient 11 (x = 416) BGM12L[9:8], MSB 9:8 of B Channel Gamma Correction Coefficient 12 (x = 448)
<1D.65h>	60h	**BGM13L**	R/W	[7:0]	LSB 7:0 of B Channel Gamma Correction Coefficient 13 (x = 352)
<1D.66h>	80h	**BGM14L**	R/W	[7:0]	LSB 7:0 of B Channel Gamma Correction Coefficient 14 (x = 384)
<1D.67h>	A0h	**BGM15L**	R/W	[7:0]	LSB 7:0 of B Channel Gamma Correction Coefficient 15 (x = 416)
<1D.68h>	C0h	**BGM16L**	R/W	[7:0]	LSB 7:0 of B Channel Gamma Correction Coefficient 16 (x = 448)
<1D.69h>	55h	**BGM1316H**	R/W	[7:6] [5:4] [3:2] [1:0]	BGM13L[9:8], MSB 9:8 of B Channel Gamma Correction Coefficient 13 (x = 352) BGM14L[9:8], MSB 9:8 of B Channel Gamma Correction Coefficient 14 (x = 384) BGM15L[9:8], MSB 9:8 of B Channel Gamma Correction Coefficient 15 (x = 416) BGM16L[9:8], MSB 9:8 of B Channel Gamma Correction Coefficient 16 (x = 448)
<1D.6Ah>	E0h	**BGM17L**	R/W	[7:0]	LSB 7:0 of B Channel Gamma Correction Coefficient 17 (x = 480)
<1D.6Bh>	00h	**BGM18L**	R/W	[7:0]	LSB 7:0 of B Channel Gamma Correction Coefficient 18 (x = 512)
<1D.6Ch>	20h	**BGM19L**	R/W	[7:0]	LSB 7:0 of B Channel Gamma Correction Coefficient 19 (x = 544)
<1D.6Dh>	40h	**BGM20L**	R/W	[7:0]	LSB 7:0 of B Channel Gamma Correction Coefficient 20 (x = 576)
<1D.6Eh>	6Ah	**BGM1720H**	R/W	[7:6] [5:4] [3:2] [1:0]	BGM17L[9:8], MSB 9:8 of B Channel Gamma Correction Coefficient 17 (x = 480) BGM18L[9:8], MSB 9:8 of B Channel Gamma Correction Coefficient 18 (x = 512) BGM19L[9:8], MSB 9:8 of B Channel Gamma Correction Coefficient 19 (x = 544) BGM20L[9:8], MSB 9:8 of B Channel Gamma Correction Coefficient 20 (x = 576)
<1D.6Fh>	60h	**BGM21L**	R/W	[7:0]	LSB 7:0 of B Channel Gamma Correction Coefficient 21 (x = 608)
<1D.70h>	80h	**BGM22L**	R/W	[7:0]	LSB 7:0 of B Channel Gamma Correction Coefficient 22 (x = 640)
<1D.71h>	A0h	**BGM23L**	R/W	[7:0]	LSB 7:0 of B Channel Gamma Correction Coefficient 23 (x = 672)
<1D.72h>	C0h	**BGM24L**	R/W	[7:0]	LSB 7:0 of B Channel Gamma Correction Coefficient 24 (x = 704)
<1D.73h>	AAh	**BGM2124H**	R/W	[7:6] [5:4] [3:2] [1:0]	BGM21L[9:8], MSB 9:8 of B Channel Gamma Correction Coefficient 21 (x = 608) BGM22L[9:8], MSB 9:8 of B Channel Gamma Correction Coefficient 22 (x = 640) BGM23L[9:8], MSB 9:8 of B Channel Gamma Correction Coefficient 23 (x = 672) BGM24L[9:8], MSB 9:8 of B Channel Gamma Correction Coefficient 24 (x = 704)
<1D.74h>	E0h	**BGM25L**	R/W	[7:0]	LSB 7:0 of B Channel Gamma Correction Coefficient 25 (x = 736)
<1D.75h>	00h	**BGM26L**	R/W	[7:0]	LSB 7:0 of B Channel Gamma Correction Coefficient 26 (x = 768)
<1D.76h>	20h	**BGM27L**	R/W	[7:0]	LSB 7:0 of B Channel Gamma Correction Coefficient 27 (x = 800)
<1D.77h>	40h	**BGM28L**	R/W	[7:0]	LSB 7:0 of B Channel Gamma Correction Coefficient 28 (x = 832)
<1D.78h>	BFh	**BGM2528H**	R/W	[7:6] [5:4] [3:2] [1:0]	BGM25L[9:8], MSB 9:8 of B Channel Gamma Correction Coefficient 25 (x = 736) BGM26L[9:8], MSB 9:8 of B Channel Gamma Correction Coefficient 26 (x = 768) BGM27L[9:8], MSB 9:8 of B Channel Gamma Correction Coefficient 27 (x = 800) BGM28L[9:8], MSB 9:8 of B Channel Gamma Correction Coefficient 28 (x = 832)
<1D.79h>	60h	**BGM29L**	R/W	[7:0]	LSB 7:0 of B Channel Gamma Correction Coefficient 29 (x = 864)
<1D.7Ah>	80h	**BGM30L**	R/W	[7:0]	LSB 7:0 of B Channel Gamma Correction Coefficient 30 (x = 896)

Addr	Reset Value	Mnemonic	Attr	Bits	Descriptions
<1D.7Bh>	A0h	**BGM31L**	R/W	[7:0]	LSB 7:0 of B Channel Gamma Correction Coefficient 31 (x = 928)
<1D.7Ch>	C0h	**BGM32L**	R/W	[7:0]	LSB 7:0 of B Channel Gamma Correction Coefficient 32 (x = 960)
<1D.7Dh>	FFh	**BGM2932H**	R/W	[7:6] [5:4] [3:2] [1:0]	BGM29L[9:8], MSB 9:8 of B Channel Gamma Correction Coefficient 29 (x = 864) BGM30L[9:8], MSB 9:8 of B Channel Gamma Correction Coefficient 30 (x = 896) BGM31L[9:8], MSB 9:8 of B Channel Gamma Correction Coefficient 31 (x = 928) BGM32L[9:8], MSB 9:8 of B Channel Gamma Correction Coefficient 32 (x = 960)
<1D.7Eh>	E0h	**BGM33L**	R/W	[7:0]	LSB 7:0 of B Channel Gamma Correction Coefficient 33 (x = 992)
<1D.7Fh>	FFh	**BGM34L**	R/W	[7:0]	LSB 7:0 of B Channel Gamma Correction Coefficient 34 (x = 1024)
<1D.80h>	F0h	**BGM3334H**	R/W	[7:6] [5:4] [3:0]	BGM33L[9:8], MSB 9:8 of B Channel Gamma Correction Coefficient 33 (x = 992) BGM34L[9:8], MSB 9:8 of B Channel Gamma Correction Coefficient 34 (x = 1024) Reserved
<1D.81h>	00h	**Reserved**			
<1D.82h>	00h	**Reserved**			
<1D.83h>	00h	**Reserved**			
<1D.84h>	00h	**Reserved**			
<1D.85h>	00h	**EE_WIDE_LUMA_ON**	R/W	[7:1] [0]	Reserved ee_wide_luma_on, 1 : on, 0 : off
<1D.86h>	00h	**EE_WL_LUMA_MIN_H**	R/W	[7:2] [1:0]	Reserved MSB [9:8] luma min
<1D.87h>	64h	**EE_WL_LUMA_MIN_L**	R/W	[7:0]	Reserved LSB [7:0] luma_min
<1D.88h>	02h	**EE_WL_LUMA_MAX_H**	R/W	[7:2] [1:0]	Reserved MSB [9:8] luma max
<1D.89h>	58h	**EE_WL_LUMA_MAX_L**	R/W	[7:0]	LSB [7:0] luma_max
<1D.8Ah>	00h	**EE_WL_COEFF_P_HIGH_HH**	R/W	[7:2] [1:0]	Reserved [25:24] ee_wl_coeff_p_high
<1D.8Bh>	03h	**EE_WL_COEFF_P_HIGH_HL**	R/W	[7:0]	[23:16] ee_wl_coeff_p_high
<1D.8Ch>	CBh	**EE_WL_COEFF_P_HIGH_LH**	R/W	[7:0]	[15:8] ee_wl_coeff_p_high
<1D.8Dh>	00h	**EE_WL_COEFF_P_HIGH_LL**	R/W	[7:0]	[7:0] ee_wl_coeff_p_high
<1D.8Eh>	00h	**EE_WL_COEFF_P_LOW_HH**	R/W	[7:2] [1:0]	Reserved [25:24] ee_wl_coeff_p_low
<1D.8Fh>	17h	**EE_WL_COEFF_P_LOW_HL**	R/W	[7:0]	[23:16] ee_wl_coeff_p_low
<1D.90h>	A1h	**EE_WL_COEFF_P_LOW_LH**	R/W	[7:0]	[15:8] ee_wl_coeff_p_low
<1D.91h>	20h	**EE_WL_COEFF_P_LOW_LL**	R/W	[7:0]	[7:0] ee_wl_coeff_p_low
<1D.92h>	00h	**EE_WL_COEFF_**	R/W	[7:2]	Reserved

Addr	Reset Value	Mnemonic	Attr	Bits	Descriptions
		N_HIGH_HH		[1:0]	[25:24] ee_wl_coeff_n_high
<1D.93h>	10h	EE_WL_COEFF_N_HIGH_HL	R/W	[7:0]	[23:16] ee_wl_coeff_n_high
<1D.94h>	00h	EE_WL_COEFF_N_HIGH_LH	R/W	[7:0]	[15:8] ee_wl_coeff_n_high
<1D.95h>	00h	EE_WL_COEFF_N_HIGH_LL	R/W	[7:0]	[7:0] ee_wl_coeff_n_high
<1D.96h>	00h	EE_WL_COEFF_N_LOW_HH	R/W	[7:2] [1:0]	Reserved [25:24] ee_wl_coeff_n_low
<1D.97h>	10h	EE_WL_COEFF_N_LOW_HL	R/W	[7:0]	[23:16] ee_wl_coeff_n_low
<1D.98h>	00h	EE_WL_COEFF_N_LOW_LH	R/W	[7:0]	[15:8] ee_wl_coeff_n_low
<1D.99h>	00h	EE_WL_COEFF_N_LOW_LL	R/W	[7:0]	[7:0] ee_wl_coeff_n_low
<1D.9Ah>	0Fh	EE_WL_SLOPE_P_HH	R/W	[7:4] [3:0]	Reserved [27:24] ee_wl_slope_p
<1D.9Bh>	EBh	EE_WL_SLOPE_P_HL	R/W	[7:0]	[23:16] ee_wl_slope_p
<1D.9Ch>	B0h	EE_WL_SLOPE_P_LH	R/W	[7:0]	[15:8] ee_wl_slope_p
<1D.9Dh>	00h	EE_WL_SLOPE_P_LL	R/W	[7:0]	[7:0] ee_wl_slope_p
<1D.9Eh>	00h	EE_WL_SLOPE_N_HH	R/W	[7:4] [3:0]	Reserved [27:24] ee_wl_slope_n
<1D.9Fh>	00h	EE_WL_SLOPE_N_HL	R/W	[7:0]	[23:16] ee_wl_slope_n
<1D.A0h>	00h	EE_WL_SLOPE_N_LH	R/W	[7:0]	[15:8] ee_wl_slope_n
<1D.A1h>	00h	EE_WL_SLOPE_N_LL	R/W	[7:0]	[7:0] ee_wl_slope_n
<1D.A2h>	09h	EE_WL_SHIFT	R/W	[7:4] [3:0]	Reserved ee_wl_shift_r

18. SUPPRESS2 REGISTER MAP (PAGE 1EH)

Addr	Reset Value	Mnemonic	Attr	Bits	Descriptions
<1E.00h>	00h	**EE_WL_COEFF_P_HIGH_HH_AMIN**	R/W	[7:0]	P_HIGH for AGC MIN<B.42h> target register <1D.8Ah~91h>
<1E.01h>	18h	**EE_WL_COEFF_P_HIGH_HL_AMIN**	R/W	[7:0]	P_HIGH for AGC MIN
<1E.02h>	00h	**EE_WL_COEFF_P_HIGH_LH_AMIN**	R/W	[7:0]	P_HIGH for AGC MIN
<1E.03h>	00h	**EE_WL_COEFF_P_HIGH_LL_AMIN**	R/W	[7:0]	P_HIGH for AGC MIN
<1E.04h>	00h	**EE_WL_COEFF_P_LOW_HH_AMIN**	R/W	[7:0]	P_LOW_ for AGC MIN<B.42h>
<1E.05h>	17h	**EE_WL_COEFF_P_LOW_HL_AMIN**	R/W	[7:0]	P_LOW_ for AGC MIN
<1E.06h>	00h	**EE_WL_COEFF_P_LOW_LH_AMIN**	R/W	[7:0]	P_LOW_ for AGC MIN
<1E.07h>	00h	**EE_WL_COEFF_P_LOW_LL_AMIN**	R/W	[7:0]	P_LOW_ for AGC MIN
<1E.08h>	00h	**EE_WL_COEFF_P_HIGH_HH_AMAX**	R/W	[7:0]	P_HIGH for AGC MAX<B.43h>
<1E.09h>	0Ah	**EE_WL_COEFF_P_HIGH_HL_AMAX**	R/W	[7:0]	P_HIGH for AGC MAX
<1E.0Ah>	00h	**EE_WL_COEFF_P_HIGH_LH_AMAX**	R/W	[7:0]	P_HIGH for AGC MAX
<1E.0Bh>	00h	**EE_WL_COEFF_P_HIGH_LL_AMAX**	R/W	[7:0]	P_HIGH for AGC MAX
<IE.0Ch>	00h	**EE_WL_COEFF_P_LOW_HH_AMAX**	R/W	[7:0]	P_LOW for AGC MAX<B.43h>
<1E.0Dh>	09h	**EE_WL_COEFF_P_LOW_HL_AMAX**	R/W	[7:0]	P_LOW for AGC MAX
<1E.0Eh>	00h	**EE_WL_COEFF_P_LOW_LH_AMAX**	R/W	[7:0]	P_LOW for AGC MAX
<1E.0Fh>	00h	**EE_WL_COEFF_P_LOW_LL_AMAX**	R/W	[7:0]	P_LOW for AGC MAX
<1E.10h>	00h	**EE_WL_COEFF_N_HIGH_HH_AMIN**	R/W	[7:0]	N_HIGH for AGC MIN<B.42h> target register <1D.92h~99h>
<1E.11h>	18h	**EE_WL_COEFF_N_HIGH_HL_AMIN**	R/W	[7:0]	N_HIGH for AGC MIN
<1E.12h>	00h	**EE_WL_COEFF_N_HIGH_LH_AMIN**	R/W	[7:0]	N_HIGH for AGC MIN
<1E.13h>	00h	**EE_WL_COEFF_N_HIGH_LL_AMIN**	R/W	[7:0]	N_HIGH for AGC MIN
<1E.14h>	00h	**EE_WL_COEFF_N_LOW_HH_AMIN**	R/W	[7:0]	N_LOW_ for AGC MIN<B.42h>
<1E.15h>	17h	**EE_WL_COEFF_N_LOW_HL_AMIN**	R/W	[7:0]	N_LOW_ for AGC MIN
<1E.16h>	00h	**EE_WL_COEFF_N_LOW_LH_AMIN**	R/W	[7:0]	N_LOW_ for AGC MIN
<1E.17h>	00h	**EE_WL_COEFF_N_LOW_LL_AMIN**	R/W	[7:0]	N_LOW_ for AGC MIN
<1E.18h>	00h	**EE_WL_COEFF_N_HIGH_HH_AMAX**	R/W	[7:0]	N_HIGH for AGC MAX<B.43h>
<1E.19h>	0Ah	**EE_WL_COEFF_N_HIGH_HL_AMAX**	R/W	[7:0]	N_HIGH for AGC MAX
<1E.1Ah>	00h	**EE_WL_COEFF_N_HIGH_LH_AMAX**	R/W	[7:0]	N_HIGH for AGC MAX
<1E.1Bh>	00h	**EE_WL_COEFF_N_HIGH_LL_AMAX**	R/W	[7:0]	N_HIGH for AGC MAX
<1E.1Ch>	00h	**EE_WL_COEFF_N_LOW_HH_AMAX**	R/W	[7:0]	N_LOW for AGC MAX<B.43h>
<1E.1Dh>	09h	**EE_WL_COEFF_N_LOW_HL_AMAX**	R/W	[7:0]	N_LOW for AGC MAX
<1E.1Eh>	00h	**EE_WL_COEFF_N_LOW_LH_AMAX**	R/W	[7:0]	N_LOW for AGC MAX

Addr	Reset Value	Mnemonic	Attr	Bits	Descriptions
<1E.1Fh>	00h	**EE_WL_COEFF_N_LOW_LL_AMAX**	R/W	[7:0]	N_LOW for AGC MAX

19. AE CONTROL REGISTER MAP (PAGE 20H)

Addr	Reset Value	Mnemonic	Attr	Bits	Descriptions
<20.00h>	01h	**OPERATION**	R/W	[7:2] [1] [0]	Reserved AE Fast Limit One Jump Mode AE Fast One Jump Mode
<20.01h>	00h	**FRAMEAE_MODE**	R/W	[7:4] [3] [2] [1] [0]	Reserved FRAMEAE_FLICKERSTEP_DGAIN_ON FRAMEAE_VSIZE_MAX_ON FRAMEAE_FLICKERSTEP_ON When frame-AE mode, max integration time is limited to multiple period of the lighting flicker. FRAMEAE_FINE_ON Enable precise control (related reg.< FRAMEAE_GAIN_H,L>)
<20.02h>	02h	**FLICKER_MODE**	R/W	[7:6] [5] [4] [3] [2] [1] [0]	Reserved FLK_STEP_MULTIPLE_4 (1,2,4,8,12,16,20...) FLK_STEP_EXPONENT_2 (1,2,4,8,16,32,64...) FLK_LIMIT_2_ON min integration time is limited to <FLICKERBAND_LIMIT2_NUM> period of the lighting flicker. FLICKER_ALLSTEP_ON 0h : even integer multiples of flicker period 1h : integer multiples of flicker period FLICKERAGC 0h : Dgain compensation for flicker 1h : Agc compensation for flicker FLK_LIMIT_ON min integration time is limited to one period of the lighting flicker.
<20.03h>	00h	**ETC_MODE**	R/W	[7] [6] [5] [4] [3] [2] [1] [0]	PRE_GGAIN_MODE VMIRROR_WEIGHT_MANUAL EXT_MCLK WAIT_VSYNC CINTC_MAX_LIMIT STABLE_NEW_METHOD SHUTTER_LIMIT related reg : <SHUTTER_LIMIT_H, L> it will be off automatically after frame AE mode. The option for speed shutter. DGAINAGC related reg : <DGAINAGC_START>
<20.04h -07h>		**Reserved**			
<20.08h>	02h	**FLICKERBAND_LIMIT2_NUM**	R/W	[7:0]	Min integration time is limited to this register value period of the lighting flicker.<20h.02h>[2]
<20.09h -0Bh>		**Reserved**			

Addr	Reset Value	Mnemonic	Attr	Bits	Descriptions
<20.0Ch>	60h	**AEAVG_GAIN**	R/W	[7] [6] [5:0]	Reserved AEAVG_GAIN_X1 Reserved
<20.0Dh>		**Reserved**			
<20.0Eh>		**Reserved**			
<20.0Fh>	00h	**MIRROR_WEIGHT_MODE**	R/W	[7:1] [0]	Reserved WEIGHT_V_MIRRORED
<20.10h>	03h	**SHUTTER_LIMIT_H**	R/W	[7:0]	Maximum shutter value related reg <20.03h>[1]
<20.11h>	00h	**SHUTTER_LIMIT_L**	R/W	[7:0]	Maximum shutter value
<20.12h>	02h	**FRAMEAE_GAIN_H**	R/W	[7:0]	FRAMEAE_GAIN integer part
<20.13h>	00h	**FRAMEAE_GAIN_L**	R/W	[7:0]	FRAMEAE_GAIN fraction part
<20.14h>	70h	**BRIGHT_OFFSET**	R/W	[7:0]	Bright offset value when image resizing. x1 : 0x80
<20.15h>	02h	**IMAGEFORMAT_SUPPORT**	R/W	[7:2] [1] [0]	Reserved AEFAST_IFMT_WAIT AEFAST_IFMT_UPDATE
<20.16h>	5Ah	**FRAMEAE_START**	R/W	[7:0]	AGC value to start frame AE
<20.17h>	60h	**DGAINAGC_START**	R/W	[7:0]	AGC value to start D gain usage related reg <20.03h>[0]
<20.18h>		**Reserved**			
<20.19h>		**Reserved**			
<20.1Ah>		**Reserved**			
<20.1Bh>		**Reserved**			
<20.1Ch>	00h	**WEIGHT_MODE**	R/W	[7:0]	00h : WEIGHTMODE_FLAT, related reg.<60h - 7Fh 01h : WEIGHTMODE_CENTER, related reg.<80h- 9Fh> 02h : WEIGHTMODE_MANUAL , related reg.<A0h - BFh>
<20.1Dh -1Eh>		**Reserved**			
<20.1Fh>	F0h	**AF_WRITE_MODE**	R/W	[7] [6] [5] [4] [3:0]	WR_FINE WR_COARSE WR_AGC WR_FRAMESIZE Reserved
<20.20h -29h>		**Reserved**			
<20.2Ah>	03h	**4SHR_MODE**	R/W	[7:2] [1] [0]	Reserved 4SHR_AGC_ENABLE 4SHR_ENABLE
<20.2Bh>	02h	**4SHR_CINTC_LIMIT_MIN_H**	R/W	[7:0]	cintc limit min high for 4 shared structure Forbidden area is set by H_End - 4SHR_CINTC_LIMIT_MIN <= CINTC

Addr	Reset Value	Mnemonic	Attr	Bits	Descriptions
					Forbidden <= H_End - 4SHR_CINTC_LIMIT_MAX
<20.2Ch>	64h	**4SHR_CINTC_LIMIT_MIN_L**	R/W	[7:0]	cintc limit min low for 4 shared structure
<20.2Dh>	00h	**4SHR_CINTC_LIMIT_MAX_H**	R/W	[7:0]	cintc limit max high for 4 shared structure
<20.2Eh>	00h	**4SHR_CINTC_LIMIT_MAX_L**	R/W	[7:0]	cintc limit max low for 4 shared structure
<20.2Fh>	03h	**4SHR_CINTR_LIMIT_MIN**	R/W	[7:0]	cintr limit min for AGC compensation in forbidden area when cintr <= 4SHR_CINTR_LIMIT_MIN
<20.30h -4Bh>		**Reserved**			
<20.4Ch>	00h	**BLOOMING_MODE**	R/W	[7:1] [0]	Reserved Blooming avoidance mode enable
<20.4Dh>	02h	**BLOOMING_CINTR**	R/W	[7:0]	Blooming avoidance mode enable when cintr <= BLOOMING_CITR
<20.4Eh>	B0h	**BLOOMING_GAIN**	R/W	[7:0]	when blooming avoidance mode enabled, gain is weighted to AGC (gain = BLOOMING_GAIN / 0x80)
<20.4Fh>		**Reserved**			
<20.50h>	10h	**POS_CINTR**	R/W	[7:0]	The boundary between cintr 1 and cintr 2
<20.51h>	40h	**POS_AGC**	R/W	[7:0]	The boundary between AGC 1 and AGC 2
<20.52h>	10h	**STABLE_CINTR1**	R/W	[7:0]	Stable area for cintr 1
<20.53h>	10h	**STABLE_CINTR2**	R/W	[7:0]	Stable area for cintr 2
<20.54h>	10h	**STABLE_DGAIN**	R/W	[7:0]	Stable area for D gain
<20.55h>	10h	**STABLE_AGC1**	R/W	[7:0]	Stable area for AGC1
<20.56h>	10h	**STABLE_AGC2**	R/W	[7:0]	Stable area for AGC2
<20.57h>	18h	**STABLE_FRAME**	R/W	[7:0]	Stable area for Frame AE
<20.58h -5Fh>		**Reserved**			
<20.60h>	11h	**AE Flat Weight Preset 0**	R/W	[7:4] [3:0]	Weight value for AE window 0 (Weight value can be set from 0x00 to 0x0F) Weight value for AE window 1
<20.61h>	11h	**AE Flat Weight Preset 1**	R/W	[7:4] [3:0]	Weight value for AE window 2 Weight value for AE window 3
<20.62h>	11h	**AE Flat Weight Preset 2**	R/W	[7:4] [3:0]	Weight value for AE window 4 Weight value for AE window 5
<20.63h>	11h	**AE Flat Weight Preset 3**	R/W	[7:4] [3:0]	Weight value for AE window 6 Weight value for AE window 7
<20.64h>	11h	**AE Flat Weight Preset 4**	R/W	[7:4] [3:0]	Weight value for AE window 8 Weight value for AE window 9
<20.65h>	11h	**AE Flat Weight Preset 5**	R/W	[7:4] [3:0]	Weight value for AE window 10 Weight value for AE window 11
<20.66h>	11h	**AE Flat Weight Preset 6**	R/W	[7:4] [3:0]	Weight value for AE window 12 Weight value for AE window 13

Addr	Reset Value	Mnemonic	Attr	Bits	Descriptions
<20.67h>	11h	**AE Flat Weight Preset 7**	R/W	[7:4] [3:0]	Weight value for AE window 14 Weight value for AE window 15
<20.68h>	11h	**AE Flat Weight Preset 8**	R/W	[7:4] [3:0]	Weight value for AE window 16 Weight value for AE window 17
<20.69h>	11h	**AE Flat Weight Preset 9**	R/W	[7:4] [3:0]	Weight value for AE window 18 Weight value for AE window 19
<20.6Ah>	11h	**AE Flat Weight Preset 10**	R/W	[7:4] [3:0]	Weight value for AE window 20 Weight value for AE window 21
<20.6Bh>	11h	**AE Flat Weight Preset 11**	R/W	[7:4] [3:0]	Weight value for AE window 22 Weight value for AE window 23
<20.6Ch>	11h	**AE Flat Weight Preset 12**	R/W	[7:4] [3:0]	Weight value for AE window 24 Weight value for AE window 25
<20.6Dh>	11h	**AE Flat Weight Preset 13**	R/W	[7:4] [3:0]	Weight value for AE window 26 Weight value for AE window 27
<20.6Eh>	11h	**AE Flat Weight Preset 14**	R/W	[7:4] [3:0]	Weight value for AE window 28 Weight value for AE window 29
<20.6Fh>	11h	**AE Flat Weight Preset 15**	R/W	[7:4] [3:0]	Weight value for AE window 30 Weight value for AE window 31
<20.70h>	11h	**AE Flat Weight Preset 16**	R/W	[7:4] [3:0]	Weight value for AE window 32 Weight value for AE window 33
<20.71h>	11h	**AE Flat Weight Preset 17**	R/W	[7:4] [3:0]	Weight value for AE window 34 Weight value for AE window 35
<20.72h>	11h	**AE Flat Weight Preset 18**	R/W	[7:4] [3:0]	Weight value for AE window 36 Weight value for AE window 37
<20.73h>	11h	**AE Flat Weight Preset 19**	R/W	[7:4] [3:0]	Weight value for AE window 38 Weight value for AE window 39
<20.74h>	11h	**AE Flat Weight Preset 20**	R/W	[7:4] [3:0]	Weight value for AE window 40 Weight value for AE window 41
<20.75h>	11h	**AE Flat Weight Preset 21**	R/W	[7:4] [3:0]	Weight value for AE window 42 Weight value for AE window 43
<20.76h>	11h	**AE Flat Weight Preset 22**	R/W	[7:4] [3:0]	Weight value for AE window 44 Weight value for AE window 45
<20.77h>	11h	**AE Flat Weight Preset 23**	R/W	[7:4] [3:0]	Weight value for AE window 46 Weight value for AE window 47
<20.78h>		**Reserved**			
<20.79h>		**Reserved**			
<20.7Ah>		**Reserved**			
<20.7Bh>		**Reserved**			
<20.7Ch>		**Reserved**			
<20.7Dh>		**Reserved**			
<20.7Eh>		**Reserved**			

Addr	Reset Value	Mnemonic	Attr	Bits	Descriptions
<20.7Fh>		**Reserved**			
<20.80h>	11h	**AE Center Weight Preset 0**	R/W	[7:4] [3:0]	Weight value for AE window 0 Weight value for AE window 1
<20.81h>	11h	**AE Center Weight Preset 1**	R/W	[7:4] [3:0]	Weight value for AE window 2 Weight value for AE window 3
<20.82h>	11h	**AE Center Weight Preset 2**	R/W	[7:4] [3:0]	Weight value for AE window 4 Weight value for AE window 5
<20.83h>	11h	**AE Center Weight Preset 3**	R/W	[7:4] [3:0]	Weight value for AE window 6 Weight value for AE window 7
<20.84h>	11h	**AE Center Weight Preset 4**	R/W	[7:4] [3:0]	Weight value for AE window 8 Weight value for AE window 9
<20.85h>	11h	**AE Center Weight Preset 5**	R/W	[7:4] [3:0]	Weight value for AE window 10 Weight value for AE window 11
<20.86h>	11h	**AE Center Weight Preset 6**	R/W	[7:4] [3:0]	Weight value for AE window 12 Weight value for AE window 13
<20.87h>	11h	**AE Center Weight Preset 7**	R/W	[7:4] [3:0]	Weight value for AE window 14 Weight value for AE window 15
<20.88h>	11h	**AE Center Weight Preset 8**	R/W	[7:4] [3:0]	Weight value for AE window 16 Weight value for AE window 17
<20.89h>	1Fh	**AE Center Weight Preset 9**	R/W	[7:4] [3:0]	Weight value for AE window 18 Weight value for AE window 19
<20.8Ah>	F1h	**AE Center Weight Preset 10**	R/W	[7:4] [3:0]	Weight value for AE window 20 Weight value for AE window 21
<20.8Bh>	11h	**AE Center Weight Preset 11**	R/W	[7:4] [3:0]	Weight value for AE window 22 Weight value for AE window 23
<20.8Ch>	11h	**AE Center Weight Preset 12**	R/W	[7:4] [3:0]	Weight value for AE window 24 Weight value for AE window 25
<20.8Dh>	1Fh	**AE Center Weight Preset 13**	R/W	[7:4] [3:0]	Weight value for AE window 26 Weight value for AE window 27
<20.8Eh>	F1h	**AE Center Weight Preset 14**	R/W	[7:4] [3:0]	Weight value for AE window 28 Weight value for AE window 29
<20.8Fh>	11h	**AE Center Weight Preset 15**	R/W	[7:4] [3:0]	Weight value for AE window 30 Weight value for AE window 31
<20.90h>	11h	**AE Center Weight Preset 16**	R/W	[7:4] [3:0]	Weight value for AE window 32 Weight value for AE window 33
<20.91h>	11h	**AE Center Weight Preset 17**	R/W	[7:4] [3:0]	Weight value for AE window 34 Weight value for AE window 35
<20.92h>	11h	**AE Center Weight Preset 18**	R/W	[7:4] [3:0]	Weight value for AE window 36 Weight value for AE window 37
<20.93h>	11h	**AE Center Weight Preset 19**	R/W	[7:4] [3:0]	Weight value for AE window 38 Weight value for AE window 39
<20.94h>	11h	**AE Center Weight Preset 20**	R/W	[7:4] [3:0]	Weight value for AE window 40 Weight value for AE window 41

Addr	Reset Value	Mnemonic	Attr	Bits	Descriptions
<20.95h>	11h	**AE Center Weight Preset 21**	R/W	[7:4] [3:0]	Weight value for AE window 42 Weight value for AE window 43
<20.96h>	11h	**AE Center Weight Preset 22**	R/W	[7:4] [3:0]	Weight value for AE window 44 Weight value for AE window 45
<20.97h>	11h	**AE Center Weight Preset 23**	R/W	[7:4] [3:0]	Weight value for AE window 46 Weight value for AE window 47
<20.98h>		**Reserved**			
<20.99h>		**Reserved**			
<20.9Ah>		**Reserved**			
<20.9Bh>		**Reserved**			
<20.9Ch>		**Reserved**			
<20.9Dh>		**Reserved**			
<20.9Eh>		**Reserved**			
<20.9Fh>		**Reserved**			
<20.A0h>	FFh	**AE Manual Weight Preset 0**	R/W	[7:4] [3:0]	Weight value for AE window 0 Weight value for AE window 1
<20.A1h>	FFh	**AE Manual Weight Preset 1**	R/W	[7:4] [3:0]	Weight value for AE window 2 Weight value for AE window 3
<20.A2h>	FFh	**AE Manual Weight Preset 2**	R/W	[7:4] [3:0]	Weight value for AE window 4 Weight value for AE window 5
<20.A3h>	FFh	**AE Manual Weight Preset 3**	R/W	[7:4] [3:0]	Weight value for AE window 6 Weight value for AE window 7
<20.A4h>	FFh	**AE Manual Weight Preset 4**	R/W	[7:4] [3:0]	Weight value for AE window 8 Weight value for AE window 9
<20.A5h>	11h	**AE Manual Weight Preset 5**	R/W	[7:4] [3:0]	Weight value for AE window 10 Weight value for AE window 11
<20.A6h>	11h	**AE Manual Weight Preset 6**	R/W	[7:4] [3:0]	Weight value for AE window 12 Weight value for AE window 13
<20.A7h>	FFh	**AE Manual Weight Preset 7**	R/W	[7:4] [3:0]	Weight value for AE window 14 Weight value for AE window 15
<20.A8h>	FFh	**AE Manual Weight Preset 8**	R/W	[7:4] [3:0]	Weight value for AE window 16 Weight value for AE window 17
<20.A9h>	11h	**AE Manual Weight Preset 9**	R/W	[7:4] [3:0]	Weight value for AE window 18 Weight value for AE window 19
<20.AAh>	11h	**AE Manual Weight Preset 10**	R/W	[7:4] [3:0]	Weight value for AE window 20 Weight value for AE window 21
<20.ABh>	FFh	**AE Manual Weight Preset 11**	R/W	[7:4] [3:0]	Weight value for AE window 22 Weight value for AE window 23
<20.ACh>	FFh	**AE Manual Weight Preset 12**	R/W	[7:4] [3:0]	Weight value for AE window 24 Weight value for AE window 25
<20.ADh>	11h	**AE Manual Weight Preset 13**	R/W	[7:4]	Weight value for AE window 26

Addr	Reset Value	Mnemonic	Attr	Bits	Descriptions
				[3:0]	Weight value for AE window 27
<20.AEh>	11h	**AE Manual Weight Preset 14**	R/W	[7:4] [3:0]	Weight value for AE window 28 Weight value for AE window 29
<20.AFh>	FFh	**AE Manual Weight Preset 15**	R/W	[7:4] [3:0]	Weight value for AE window 30 Weight value for AE window 31
<20.B0h>	FFh	**AE Manual Weight Preset 16**	R/W	[7:4] [3:0]	Weight value for AE window 32 Weight value for AE window 33
<20.B1h>	11h	**AE Manual Weight Preset 17**	R/W	[7:4] [3:0]	Weight value for AE window 34 Weight value for AE window 35
<20.B2h>	11h	**AE Manual Weight Preset 18**	R/W	[7:4] [3:0]	Weight value for AE window 36 Weight value for AE window 37
<20.B3h>	FFh	**AE Manual Weight Preset 19**	R/W	[7:4] [3:0]	Weight value for AE window 38 Weight value for AE window 39
<20.B4h>	11h	**AE Manual Weight Preset 20**	R/W	[7:4] [3:0]	Weight value for AE window 40 Weight value for AE window 41
<20.B5h>	11h	**AE Manual Weight Preset 21**	R/W	[7:4] [3:0]	Weight value for AE window 42 Weight value for AE window 43
<20.B6h>	11h	**AE Manual Weight Preset 22**	R/W	[7:4] [3:0]	Weight value for AE window 44 Weight value for AE window 45
<20.B7h>	11h	**AE Manual Weight Preset 23**	R/W	[7:4] [3:0]	Weight value for AE window 46 Weight value for AE window 47
<20.B8h - C0h>		**Reserved**			

20. AWB2 REGISTER MAP (PAGE 22H)

Addr	Reset Value	Mnemonic	Attr	Bits	Descriptions
<22.00h>	00h	**D65_Rgain_H**	R/W	[7:0]	D65 point for enhanced gain offset control (Gain Domain)
<22.01h>	D6h	**D65_Rgain_L**	R/W	[7:0]	D65 point for enhanced gain offset control (Gain Domain)
<22.02h>	00h	**D65_Bgain_H**	R/W	[7:0]	D65 point for enhanced gain offset control (Gain Domain)
<22.03h>	9Bh	**D65_Bgain_L**	R/W	[7:0]	D65 point for enhanced gain offset control (Gain Domain)
<22.04h>	00h	**O5K_Rgain_H**	R/W	[7:0]	D50 point for enhanced gain offset control (Gain Domain)
<22.05h>	CAh	**O5K_Rgain_L**	R/W	[7:0]	D50 point for enhanced gain offset control (Gain Domain)
<22.06h>	00h	**O5K_Bgain_H**	R/W	[7:0]	D50 point for enhanced gain offset control (Gain Domain)
<22.07h>	B8h	**O5K_Bgain_L**	R/W	[7:0]	D50 point for enhanced gain offset control (Gain Domain)
<22.08h>	00h	**CWF_Rgain_H**	R/W	[7:0]	CWF point for enhanced gain offset control (Gain Domain)
<22.09h>	A7h	**CWF_Rgain_L**	R/W	[7:0]	CWF point for enhanced gain offset control (Gain Domain)
<22.0Ah>	00h	**CWF_Bgain_H**	R/W	[7:0]	CWF point for enhanced gain offset control (Gain Domain)
<22.0Bh>	DCh	**CWF_Bgain_L**	R/W	[7:0]	CWF point for enhanced gain offset control (Gain Domain)
<22.0Ch>	00h	**INC_Rgain_H**	R/W	[7:0]	IncandA point for enhanced gain offset control (Gain Domain)
<22.0Dh>	98h	**INC_Rgain_L**	R/W	[7:0]	IncandA point for enhanced gain offset control (Gain Domain)
<22.0Eh>	00h	**INC_Bgain_H**	R/W	[7:0]	IncandA point for enhanced gain offset control (Gain Domain)
<22.0Fh>	E0h	**INC_Bgain_L**	R/W	[7:0]	IncandA point for enhanced gain offset control (Gain Domain)
<22.10h>	00h	**I3K_Rgain_H**	R/W	[7:0]	3000K point for enhanced gain offset control (Gain Domain)
<22.11h>	85h	**I3K_Rgain_L**	R/W	[7:0]	3000K point for enhanced gain offset control (Gain Domain)
<22.12h>	00h	**I3K_Bgain_H**	R/W	[7:0]	3000K point for enhanced gain offset control (Gain Domain)
<22.13h>	F6h	**I3K_Bgain_L**	R/W	[7:0]	3000K point for enhanced gain offset control (Gain Domain)
<22.14h>	00h	**C2K_Rgain_H**	R/W	[7:0]	2000K point for enhanced gain offset control (Gain Domain)
<22.15h>	80h	**C2K_Rgain_L**	R/W	[7:0]	2000K point for enhanced gain offset control (Gain Domain)
<22.16h>	01h	**C2K_Bgain_H**	R/W	[7:0]	2000K point for enhanced gain offset control (Gain Domain)
<22.17h>	00h	**C2K_Bgain_L**	R/W	[7:0]	2000K point for enhanced gain offset control (Gain Domain)
<22.18h>	00h	**GRAY_00_RB_H**	R/W	[7:4] [3:0]	Polygon point R_H Polygon point B_H
<22.19h>	6Ch	**GRAY_00_R_L**	R/W	[7:0]	Polygon point R_L
<22.1Ah>	DCh	**GRAY_00_B_L**	R/W	[7:0]	Polygon point B_L
<22.1Bh>	00h	**GRAY_01_RB_H**	R/W	[7:4] [3:0]	Polygon point R_H Polygon point B_H
<22.1Ch>	6Dh	**GRAY_01_R_L**	R/W	[7:0]	Polygon point R_L
<22.1Dh>	BEh	**GRAY_01_B_L**	R/W	[7:0]	Polygon point B_L
<22.1Eh>	00h	**GRAY_02_RB_H**	R/W	[7:4] [3:0]	Polygon point R_H Polygon point B_H
<22.1Fh>	91h	**GRAY_02_R_L**	R/W	[7:0]	Polygon point R_L
<22.20h>	90h	**GRAY_02_B_L**	R/W	[7:0]	Polygon point B_L
<22.21h>	00h	**GRAY_03_RB_H**	R/W	[7:4]	Polygon point R_H

Addr	Reset Value	Mnemonic	Attr	Bits	Descriptions
				[3:0]	Polygon point B_H
<22.22h>	A4h	**GRAY_03_R_L**	R/W	[7:0]	Polygon point R_L
<22.23h>	7Ch	**GRAY_03_B_L**	R/W	[7:0]	Polygon point B_L
<22.24h>	00h	**GRAY_04_RB_H**	R/W	[7:4] [3:0]	Polygon point R_H Polygon point B_H
<22.25h>	C1h	**GRAY_04_R_L**	R/W	[7:0]	Polygon point R_L
<22.26h>	65h	**GRAY_04_B_L**	R/W	[7:0]	Polygon point B_L
<22.27h>	00h	**GRAY_05_RB_H**	R/W	[7:4] [3:0]	Polygon point R_H Polygon point B_H
<22.28h>	DDh	**GRAY_05_R_L**	R/W	[7:0]	Polygon point R_L
<22.29h>	55h	**GRAY_05_B_L**	R/W	[7:0]	Polygon point B_L
<22.2Ah>	00h	**GRAY_06_RB_H**	R/W	[7:4] [3:0]	Polygon point R_H Polygon point B_H
<22.2Bh>	DDh	**GRAY_06_R_L**	R/W	[7:0]	Polygon point R_L
<22.2Ch>	60h	**GRAY_06_B_L**	R/W	[7:0]	Polygon point B_L
<22.2Dh>	00h	**GRAY_07_RB_H**	R/W	[7:4] [3:0]	Polygon point R_H Polygon point B_H
<22.2Eh>	CBh	**GRAY_07_R_L**	R/W	[7:0]	Polygon point R_L
<22.2Fh>	6Ch	**GRAY_07_B_L**	R/W	[7:0]	Polygon point B_L
<22.30h>	00h	**GRAY_08_RB_H**	R/W	[7:4] [3:0]	Polygon point R_H Polygon point B_H
<22.31h>	B7h	**GRAY_08_R_L**	R/W	[7:0]	Polygon point R_L
<22.32h>	7Ah	**GRAY_08_B_L**	R/W	[7:0]	Polygon point B_L
<22.33h>	00h	**GRAY_09_RB_H**	R/W	[7:4] [3:0]	Polygon point R_H Polygon point B_H
<22.34h>	A4h	**GRAY_09_R_L**	R/W	[7:0]	Polygon point R_L
<22.35h>	90h	**GRAY_09_B_L**	R/W	[7:0]	Polygon point B_L
<22.36h>	00h	**GRAY_10_RB_H**	R/W	[7:4] [3:0]	Polygon point R_H Polygon point B_H
<22.37h>	87h	**GRAY_10_R_L**	R/W	[7:0]	Polygon point R_L
<22.38h>	CFh	**GRAY_10_B_L**	R/W	[7:0]	Polygon point B_L
<22.39h>	00h	**GRAY_11_RB_H**	R/W	[7:4] [3:0]	Polygon point R_H Polygon point B_H
<22.3Ah>	00h	**GRAY_11_R_L**	R/W	[7:0]	Polygon point R_L
<22.3Bh>	00h	**GRAY_11_B_L**	R/W	[7:0]	Polygon point B_L
<22.3Ch>	00h	**GRAY_12_RB_H**	R/W	[7:4] [3:0]	Polygon point R_H Polygon point B_H
<22.3Dh>	00h	**GRAY_12_R_L**	R/W	[7:0]	Polygon point R_L
<22.3Eh>	00h	**GRAY_12_B_L**	R/W	[7:0]	Polygon point B_L
<22.3Fh>	00h	**GRAY_13_RB_H**	R/W	[7:4]	Polygon point R_H

Addr	Reset Value	Mnemonic	Attr	Bits	Descriptions
				[3:0]	Polygon point B_H
<22.40h>	00h	**GRAY_13_R_L**	R/W	[7:0]	Polygon point R_L
<22.41h>	00h	**GRAY_13_B_L**	R/W	[7:0]	Polygon point B_L
<22.42h>	00h	**GRAY_14_RB_H**	R/W	[7:4] [3:0]	Polygon point R_H Polygon point B_H
<22.43h>	00h	**GRAY_14_R_L**	R/W	[7:0]	Polygon point R_L
<22.44h>	00h	**GRAY_14_B_L**	R/W	[7:0]	Polygon point B_L
<22.45h>	00h	**GRAY_15_RB_H**	R/W	[7:4] [3:0]	Polygon point R_H Polygon point B_H
<22.46h>	00h	**GRAY_15_R_L**	R/W	[7:0]	Polygon point R_L
<22.47h>	00h	**GRAY_15_B_L**	R/W	[7:0]	Polygon point B_L
<22.48h>	00h	**GRAY_16_RB_H**	R/W	[7:4] [3:0]	Polygon point R_H Polygon point B_H
<22.49h>	00h	**GRAY_16_R_L**	R/W	[7:0]	Polygon point R_L
<22.4Ah>	00h	**GRAY_16_B_L**	R/W	[7:0]	Polygon point B_L
<22.4Bh>	00h	**GRAY_17_RB_H**	R/W	[7:4] [3:0]	Polygon point R_H Polygon point B_H
<22.4Ch>	00h	**GRAY_17_R_L**	R/W	[7:0]	Polygon point R_L
<22.4Dh>	00h	**GRAY_17_B_L**	R/W	[7:0]	Polygon point B_L
<22.4Eh>	00h	**GRAY_18_RB_H**	R/W	[7:4] [3:0]	Polygon point R_H Polygon point B_H
<22.4Fh>	00h	**GRAY_18_R_L**	R/W	[7:0]	Polygon point R_L
<22.50h>	00h	**GRAY_18_B_L**	R/W	[7:0]	Polygon point B_L
<22.51h>	00h	**GRAY_19_RB_H**	R/W	[7:4] [3:0]	Polygon point R_H Polygon point B_H
<22.52h>	00h	**GRAY_19_R_L**	R/W	[7:0]	Polygon point R_L
<22.53h>	00h	**GRAY_19_B_L**	R/W	[7:0]	Polygon point B_L
<22.54h>	00h	**GRAY_20_RB_H**	R/W	[7:4] [3:0]	Polygon point R_H Polygon point B_H
<22.55h>	00h	**GRAY_20_R_L**	R/W	[7:0]	Polygon point R_L
<22.56h>	00h	**GRAY_20_B_L**	R/W	[7:0]	Polygon point B_L
<22.57h>		**Reserved**			
<22.58h>	F6h	**R_OFFSET_D65**	R/W	[7:0]	D65 R gain offset
<22.59h>	00h	**B_OFFSET_D65**	R/W	[7:0]	D65 B gain offset
<22.5Ah>	F9h	**R_OFFSET_O5K**	R/W	[7:0]	D50 R gain offset
<22.5Bh>	01h	**B_OFFSET_O5K**	R/W	[7:0]	D50 B gain offset
<22.5Ch>	FCh	**R_OFFSET_CWF**	R/W	[7:0]	CWF R gain offset
<22.5Dh>	02h	**B_OFFSET_CWF**	R/W	[7:0]	CWF B gain offset
<22.5Eh>	00h	**R_OFFSET_INC**	R/W	[7:0]	IncandA R gain offset
<22.5Fh>	05h	**B_OFFSET_INC**	R/W	[7:0]	IncandA B gain offset

Addr	Reset Value	Mnemonic	Attr	Bits	Descriptions
<22.60h>	01h	**R_OFFSET_I3K**	R/W	[7:0]	3000K R gain offset
<22.61h>	07h	**B_OFFSET_I3K**	R/W	[7:0]	3000K B gain offset
<22.62h>	FCh	**R_OFFSET_C2K**	R/W	[7:0]	2000K R gain offset
<22.63h>	08h	**B_OFFSET_C2K**	R/W	[7:0]	2000K B gain offset
<22.64h>	00h	**FEW_PATCH_THR**	R/W	[7:0]	Shrink Fixed referecne1 R
<22.65h>	00h	**FEW_PATCH_WEIGHT**	R/W	[7:0]	Shrink Fixed referecne1 B
<22.66h>	10h	**THR_CLASSFY**	R/W	[7:0]	Shrink Fixed referecne2 R
<22.67h>	10h	**FIN_GAMUT_THR_1_H**	R/W	[7:0]	B_WIDTH_H 0xf0 B_HEIGHT_H 0x0f
<22.68h>	00h	**FIN_GAMUT_WIDTH_THR_4_H**	R/W	[7:0]	Shrink Cell1 R ratio
<22.69h -79h>		**Reserved**			
<22.7Ah>	00h	**MOD_RGN_OPTION**	R/W	[7] [6] [5] [4] [3] [2] [1] [0]	Aux4 enable Aux4 Delete mode Aux3 enable Aux3 Delete mode Aux2 enable Aux2 Delete mode Aux1 enable Aux1 Delete mode
<22.7Bh>	00h	**MOD_RGN_CIRC_1_CNTR_RL_H**	R/W	[7:4] [3:0]	Aux1 Center Point R_H Aux1 Center Point B_H
<22.7Ch>	00h	**MOD_RGN_CIRC_1_CNTR_R_L**	R/W	[7:0]	Aux1 Center Point R
<22.7Dh>	00h	**MOD_RGN_CIRC_1_CNTR_B_L**	R/W	[7:0]	Aux1 Center Point B
<22.7Eh>	00h	**MOD_RGN_CIRC_1_SIZE**	R/W	[7:0]	Aux1 Radius
<22.7Fh>	00h	**MOD_RGN_RECT_1_CNTR_RL_H**	R/W	[7:4] [3:0]	Aux2 Center Point R_H Aux2 Center Point B_H
<22.80h>	00h	**MOD_RGN_RECT_1_CNTR_R_L**	R/W	[7:0]	Aux2 Center Point R
<22.81h>	00h	**MOD_RGN_RECT_1_CNTR_B_L**	R/W	[7:0]	Aux2 Center Point B
<22.82h>	00h	**MOD_RGN_RECT_1_SIZE**	R/W	[7:0]	Aux2 Area
<22.83h>	00h	**MOD_RGN_CIRC_2_CNTR_RL_H**	R/W	[7:4] [3:0]	Aux3 Center Point R_H Aux3 Center Point B_H
<22.84h>	00h	**MOD_RGN_CIRC_2_CNTR_R_L**	R/W	[7:0]	Aux3 Center Point R
<22.85h>	00h	**MOD_RGN_CIRC_2_CNTR_B_L**	R/W	[7:0]	Aux3 Center Point B
<22.86h>	00h	**MOD_RGN_CIRC_2_SIZE**	R/W	[7:0]	Aux3 Radius
<22.87h>	00h	**MOD_RGN_RECT_2_CNTR_RL_H**	R/W	[7:4] [3:0]	Aux4 Center Point R_H Aux4 Center Point B_H
<22.88h>	00h	**MOD_RGN_RECT_2_CNTR_R_L**	R/W	[7:0]	Aux4 Center Point R
<22.89h>	00h	**MOD_RGN_RECT_2_CNTR_B_L**	R/W	[7:0]	Aux4 Center Point B
<22.8Ah>	00h	**MOD_RGN_RECT_2_SIZE**	R/W	[7:0]	Aux4 Area
<22.8Bh>	00h	**Reserved**			

Addr	Reset Value	Mnemonic	Attr	Bits	Descriptions
<22.8Ch>	03h	**YMIN_COEF**	R/W	[7:0]	Min Y weight
<22.8Dh>	07h	**YMAX_COEF**	R/W	[7:0]	Max Y weight
<22.8Eh>	07h	**YMED_COEF**	R/W	[7:0]	Median Y weight
<22.8Fh>	05h	**YAVG_COEF**	R/W	[7:0]	Average Y weight
<22.90h -93h>		**Reserved**			
<22.94h>	37h	**Y_NORM_R_THR_H**	R/W	[7:0]	Moving Equation R threshold H
<22.95h>	CCh	**Y_NORM_R_THR_L**	R/W	[7:0]	Moving Equation R threshold L
<22.96h>	62h	**Y_NORM_B_THR_H**	R/W	[7:0]	Moving Equation B threshold H
<22.97h>	3Ah	**Y_NORM_B_THR_L**	R/W	[7:0]	Moving Equation B threshold L
<22.98h>	07h	**Y_AXIS_THR**	R/W	[7:0]	Moving Equation Weight (recommand 5 ~ 12)
<22.99h -9Eh>		**Reserved**			
<22.9Fh>	1Ah	**LOWER_BOUND_NUM_GRAY_PATCH**	R/W	[7:0]	Min number of Gray patch
<22.A0h>	01h	**GLOB_CONST_h_H**	R/W	[7:0]	Global Coefficient
<22.A1h>	3Fh	**GLOB_CONST_h_L**	R/W	[7:0]	Global Coefficient
<22.A2h>	0Eh	**GLOB_COEF_j_H**	R/W	[7:0]	Global Coefficient
<22.A3h>	8Ah	**GLOB_COEF_j_L**	R/W	[7:0]	Global Coefficient
<22.A4h>	07h	**GLOB_COEF_k_H**	R/W	[7:0]	Global Coefficient
<22.A5h>	F6h	**GLOB_COEF_k_L**	R/W	[7:0]	Global Coefficient
<22.A6h>	11h	**GLOB_COEF_l_H**	R/W	[7:0]	Global Coefficient
<22.A7h>	9Ah	**GLOB_COEF_l_L**	R/W	[7:0]	Global Coefficient
<22.A8h>	05h	**Reserved**			
<22.A9h>	02h	**ILLUM_CAL_R_COEF_H**	R/W	[7:0]	Illuminant calibration R coefficient H
<22.AAh>	A8h	**ILLUM_CAL_R_COEF_L**	R/W	[7:0]	Illuminant calibration R coefficient L
<22.ABh>	7Fh	**ILLUM_CAL_R_CONST_H**	R/W	[7:0]	Illuminant calibration R constant H
<22.ACh>	E8h	**ILLUM_CAL_R_CONST_L**	R/W	[7:0]	Illuminant calibration R constant L
<22.ADh>	02h	**ILLUM_CAL_B_COEF_H**	R/W	[7:0]	Illuminant calibration B coefficient H
<22.AEh>	A1h	**ILLUM_CAL_B_COEF_L**	R/W	[7:0]	Illuminant calibration B coefficient L
<22.AFh>	4Fh	**ILLUM_CAL_B_CONST_H**	R/W	[7:0]	Illuminant calibration B constant H
<22.B0h>	CFh	**ILLUM_CAL_B_CONST_L**	R/W	[7:0]	Illuminant calibration B constant L
<22.B1h>	00h	**EIT_1_HH**	R/W	[7:0]	EIT threshold for Sunny
<22.B2h>	00h	**EIT_1_HL**	R/W	[7:0]	EIT threshold for Sunny
<22.B3h>	8Bh	**EIT_1_LH**	R/W	[7:0]	EIT threshold for Sunny
<22.B4h>	F5h	**EIT_1_LL**	R/W	[7:0]	EIT threshold for Sunny
<22.B5h>	00h	**EIT_2_HH**	R/W	[7:0]	EIT threshold for Cloudy
<22.B6h>	06h	**EIT_2_HL**	R/W	[7:0]	EIT threshold for Cloudy
<22.B7h>	A4h	**EIT_2_LH**	R/W	[7:0]	EIT threshold for Cloudy

Addr	Reset Value	Mnemonic	Attr	Bits	Descriptions
<22.B8h>	91h	**EIT_2_LL**	R/W	[7:0]	EIT threshold for Cloudy
<22.B9h>		**Reserved**			
<22.BAh>		**Reserved**			
<22.BBh>		**Reserved**			
<22.BCh>		**Reserved**			
<22.BDh>	8Ch	**AWB2_OPTION**	R/W	[7] [6:4] [3] [2] [1:0]	BD_OUTDOORCLASY Reserved WHITE_MODE_EN GREEN_STABLIZER Reserved
<22.BEh -CEh>		**Reserved**			
<22.CFh>	03h	**FINAL_CNT_THR**	R/W	[7:0]	Pixel Filter Counter Threshold
<22.D0h>	15h	**FIN_GAMUT_WIDTH_THR_1**	R/W	[7:0]	Gamut width threshold 1
<22.D1h>	31h	**FIN_GAMUT_WIDTH_THR_2**	R/W	[7:0]	Gamut width threshold 2
<22.D2h>	51h	**FIN_GAMUT_HEIGHT_THR_1**	R/W	[7:0]	Gamut Height threshold 1
<22.D3h>	2Ch	**FIN_GAMUT_HEIGHT_THR_2**	R/W	[7:0]	Gamut Height threshold 2
<22.D4h>	98h	**FIN_INIT_R_CONST**	R/W	[7:0]	Scene detection threshold 1
<22.D5h>	05h	**FIN_ILLUM_CNTR_R_COEF**	R/W	[7:0]	Scene detection threshold 2
<22.D6h>	05h	**FIN_ILLUM_CNTR_B_COEF**	R/W	[7:0]	Scene detection threshold 3
<22.D7h>	FFh	**EIT_IL_HH**	R/W	[7:0]	EIT threshold for Large Object
<22.D8h>	35h	**EIT_IL_HL**	R/W	[7:0]	EIT threshold for Large Object
<22.D9h>	20h	**EIT_IL_LH**	R/W	[7:0]	EIT threshold for Large Object
<22.DAh>	81h	**EIT_IL_LL**	R/W	[7:0]	EIT threshold for Large Object
<22.DBh>	31h	**FIN_GAMUT_WIDTH_THR_3**	R/W	[7:0]	Gamut width threshold 3
<22.DCh>	D0h	**FIN_GAMUT_WIDTH_THR_4**	R/W	[7:0]	Gamut width threshold 4
<22.DDh>	2Ch	**FIN_GAMUT_HEIGHT_THR_3**	R/W	[7:0]	Gamut Height threshold 3
<22.DEh>	00h	**FIN_ILLUM_COEF**	R/W	[7:0]	Final Illuminant coefficient
<22.DFh>	05h	**FIN_MAPP_COEF**	R/W	[7:0]	Final Mapping coefficient
<22.E0h -E6h>		**Reserved**			
<22.E7h>	00h	**LOW_TMP_WB_R_H**	R/W	[7:0]	Low temp region center R_H
<22.E8h>	D1h	**LOW_TMP_WB_R_L**	R/W	[7:0]	Low temp region center R_L
<22.E9h>	00h	**LOW_TMP_WB_B_H**	R/W	[7:0]	Low temp region center B_H
<22.EAh>	65h	**LOW_TMP_WB_B_L**	R/W	[7:0]	Low temp region center B_L
<22.EBh>	00h	**DIST_LOW_TMP_WB_H**	R/W	[7:0]	Low temp region Radius_H
<22.ECh>	21h	**DIST_LOW_TMP_WB_L**	R/W	[7:0]	Low temp region Radius_L
<22.EDh>	00h	**Reserved**			
<22.EEh>	98h	**FIN_INIT_R_CONST_HIGH**	R/W	[7:0]	Scene detection threshold 4

Addr	Reset Value	Mnemonic	Attr	Bits	Descriptions
<22.EFh>	05h	**AWB2_STATUS**	R/W	[7:0]	0x01 : OUTDOOR_SUNNY 0x02 : OUTDOOR_CLOUDY 0x03 : LOWTEMP 0x04 : HIGHTEMP 0x05 : GENERAL 0x06 : LARGEOBJECT 0x08 : WHITE
<22.F0h>	6Ah	**FIN_COND_TMP_RB_RATIO**	R/W	[7:0]	Scene detection threshold 5
<22.F1h -F8h>		**Reserved**			

21. DIGITAL ZOOM REGISTER MAP (PAGE 28H)

Table 1. Image Format Table Index

Table Index <0.0Fh>	Address
0(Table 0)	00h~1Fh
1(Table 1)	20h~3Fh
2(Table 2)	40h~5Fh
3(Table 3)	60h~7Fh
4(Table 4)	80h~9Fh
5(Table 5)	A0h~BFh
6(Table 6)	C0h~DFh

Table 2. Detailed register Table of Table 1 – Page 28h (Attribute of all these values is R/W)

Addr [4:0]	Target Register	Bits	Descriptions	Table Index 0	Table Index 1	Table Index 2	Table Index 3	Table Index 4	Table Index 5	Table Index 6
00h	<5.6Eh>	[7:0]	DSP5_POST_HSTART_H	00h	00h	00h	01h	01h	01h	01h
01h	<5.6Fh>	[7:0]	DSP5_POST_HSTART_L	08h	8Eh	EEh	34h	6Ch	98h	BCh
02h	<5.70h>	[7:0]	DSP5_POST_HWIDTH_H	06h	05h	04h	03h	03h	03h	02h
03h	<5.71h>	[7:0]	DSP5_POST_HWIDTH_L	40h	36h	76h	E8h	78h	20h	D8h
04h	<5.72h>	[7:0]	DSP5_POST_VSTART_H	00h	00h	00h	00h	01h	01h	01h
05h	<5.73h>	[7:0]	DSP5_POST_VSTART_L	08h	6Ch	B4h	EAh	14h	34h	50h
06h	<5.74h>	[7:0]	DSP5_POST_VHEIGHT_H	04h	03h	03h	02h	02h	02h	02h
07h	<5.75h>	[7:0]	DSP5_POST_VHEIGHT_L	B0h	E8h	59h	EEh	9Ah	58h	21h
08h	<5.7Ah>	[7:0]	DSP5_IMG_HSIZEH	06h	05h	04h	03h	03h	03h	02h
09h	<5.7Bh>	[7:0]	DSP5_IMG_HSIZEL	40h	36h	76h	E8h	78h	20h	D8h
0Ah	<5.7Ch>	[7:0]	DSP5_IMG_VSIZEH	04h	03h	03h	02h	02h	02h	02h
0Bh	<5.7Dh>	[7:0]	DSP5_IMG_VSIZEL	B0h	E8h	59h	EEh	9Ah	58h	21h
0Ch	<5.7Eh>	[7:0]	DSP5_PSF	22h	22h	00h	00h	00h	00h	00h
0Dh	<5.7Fh>	[7:0]	DSP5_MSFXH	40h	0Ah	C8h	90h	63h	40h	23h
0Eh	<5.80h>	[7:0]	DSP5_MSFXL	00h	CCh	CCh	00h	33h	00h	33h
0Fh	<5.81h>	[7:0]	DSP5_MSFYH	40h	0Ah	C9h	90h	63h	40h	22h
10h	<5.82h>	[7:0]	DSP5_MSFYL	00h	AAh	11h	00h	33h	00h	AAh
11h	<5.83h>	[7:0]	DSP5_DW_HSIZEH	02h	02h	02h	02h	02h	02h	02h
12h	<5.84h>	[7:0]	DSP5_DW_HSIZEL	80h	80h	80h	80h	80h	80h	80h
13h	<5.85h>	[7:0]	DSP5_DW_VSIZEH	01h	01h	01h	01h	01h	01h	01h
14h	<5.86h>	[7:0]	DSP5_DW_VSIZEL	E0h	E0h	E0h	E0h	E0h	E0h	E0h
15h	<5.87h>	[7:0]	DSP5_STARTXH	00h	00h	00h	00h	00h	00h	00h
16h	<5.88h>	[7:0]	DSP5_STARTXL	00h	00h	00h	00h	00h	00h	00h
17h	<5.89h>	[7:0]	DSP5_STARTYH	00h	00h	00h	00h	00h	00h	00h
18h	<5.8Ah>	[7:0]	DSP5_STARTYL	00h	00h	00h	00h	00h	00h	00h
19h	<5.8Bh>	[7:0]	DSP5_CLIP_HSIZEH	02h	02h	02h	02h	02h	02h	02h
1Ah	<5.8Ch>	[7:0]	DSP5_CLIP_HSIZEL	80h	80h	80h	80h	80h	80h	80h
1Bh	<5.8Dh>	[7:0]	DSP5_CLIP_VSIZEH	01h	01h	01h	01h	01h	01h	01h

Addr [4:0]	Target Register	Bits	Descriptions	Table Index 0	Table Index 1	Table Index 2	Table Index 3	Table Index 4	Table Index 5	Table Index 6
1Ch	<5.8Eh>	[7:0]	DSP5_CLIP_VSIZEL	E0h	E0h	E0h	E0h	E0h	E0h	E0h
1Dh	<5.90h>	[7:0]	DSP5_HTERMH	00h	00h	00h	00h	00h	00h	00h
1Eh	<5.91h>	[7:0]	DSP5_HTERMM	11h	0Eh	0Ch	0Ah	09h	08h	07h
1Fh	<5.92h>	[7:0]	DSP5_HTERML	30h	54h	48h	BEh	8Ah	98h	D0h

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For More Information

E-mail: drabin@samsung.com, kyungmin.shin@samsung.com, moosup.lim@samsung.com
http://samsungelectronics.com/semiconductors/