JSim Quick Reference v0.1

Iterators

	Syntax	Effect
duplication	A#5	A A A A A
buses	A[4:0]	A4 A3 A2 A1 A0
	A[11:10]	A11 A10
	A1[1:0] // DANGER!	A11 A10 // DANGER! Same as above!
	A1_[1:0] // SAFE	A1_1 A1_0
	A[1:0]#2	A1 A0 A1 A0
	A[7:0:2]	A7 A5 A3 A1
	A[2:0][1:0]	A21 A20 A11 A10 A01 A00
subcircuits	Xfoo A[2:0] B[1:0] Q Z[2:0] and2	Xfoo#0 A2 B1 Z2 and2 Xfoo#1 A1 B0 Z1 and2 Xfoo#2 A0 Q Z0 and2
connect (WRONG)	.connect A[1:0] B[1:0] // WRONG	.connect A1 A0 // Probably not .connect A1 B1 // what you .connect A1 B0 // wanted
connect (RIGHT)	.subckt S T join .connect S T .ends XjAB A[1:0] B[1:0] join	.connect A1 B1 .connect A0 B0 // Much better!

Device Statements

Subcircuit	Xid nodes… subname
Capacitor	Cid n+ n- capacitance
Inductor	Lid n+ n- inductance
Resistor	Rid n+ n- resistance
Current Source	Iid n+ n- {{DC=}dcvalue} {tran}
Voltage Source	Vid n+ n- {{DC=}dcvalue} {tran}
	// tran options:
	pulse(vA,vB,tdelay,tAtoB,tBtoA,tstable) // for clocks, starts at vA for tdelay, period is 2*tstable + tAtoB + tBtoA
	pwl(t1 v1, t2 v2, t3 v3 …) // for reset signals, signal transitions linearly from v1 at t1 to v2 at t2
MOSFET	Mid ndrain ngate nsource nbulk model L=meters W=meters {params} // a MOSFET exactly specified by L and W

MOSFET (Scaled)	Mid ndrain ngate nsource nbulk model SL=integer SW=integer {params}
	// a MOSFET specified by SL*SCALE and SW*SCALE
	// requires the .option SCALE=meters statement, defined in nominal.jsim

	// model is NENH or PENH, defined in stdcell.jsim
VCVS	Eid n+ n- ctl+ ctl- gain // voltage-controlled voltage source
CCCS	Fid n+ n- ctl+ ctl- gain // current-controlled current source
VCCS	Gid n+ n- ctl+ ctl- gain // voltage-controlled current source
CCVS	Hid n+ n- ctl+ ctl- gain // current-controlled voltage source
Digital Waveform	Wid nodes… nrz(vlow,vhigh,tperiod,tdelay,trise,tfall) data…

Memory	Xid ports… $memory width=w nlocations=nloc options…
	// each port has: oe clk wen $a_{naddr-1}$ … a_0 d_{w-1} … d_0
	// option file="filename" path is relative to jsim.jar location

Control Statements

.connect	.connect nodes… // connect all nodes together	

.dc	.dc Vds 0 5 .1 Vgs 0 5 1
	// dc analysis with voltage supplies
	// sweep Vds 0-5V in 0.1V steps
	// one plot each for Vgs 0-5V in 1V steps	

.global	.global vdd // node vdd is now accessible when creating subcircuits	

.include	.include "filename"
	// the contents of filename are included in the current file
	// path is relative to the including file	

.option	.option SCALE=35nm // set value of option SCALE to 35nm	
.plot	.plot A .plot b(B[3:0]) .plot d(…) .plot I(Vid) .plot L(…) .plot o(…) .plot sd(…) .plot x(…)	analog signal or bus format a bus as unsigned binary format a bus as unsigned decimal current into n+ of a voltage source format a bus as unsigned hexadecimal format a bus as unsigned octal format a bus as signed decimal format a bus as unsigned hexadecimal, same as L()

.plotdef	.plotdef Snakes Cobra Mamba Copperhead Sidewinder
	// when used with .plot Snakes(A[1:0]), displays snake names
	// zero value name first, case sensitive	

.subckt	.subckt subname nodes… .ends // create a subcircuit named subname	
.temp	.temp 100 // set circuit temperature to 100C	
.tran	.tran 100us // transient simulation for 100us	

Numbers

All jsim numbers are in SI units: meters, Farads, Henries, Volts, etc. Take care not to declare capacitors that are 8 meters wide.

A number may be an integer (`12`, `-44`), a floating point number (`3.14159`), an integer or floating point number followed by an integer exponent (`1E-14`, `2.65E3`), or an integer or a floating point number followed by a scale factor.

Letters immediately following a number that are not scale factors are ignored and letters immediately following a scale factor are ignored. Integers can be entered in binary, octal or hexadecimal notation by using the appropriate prefix:

`0b1011101110100`	6004 in binary ("0b" prefix)
`013564`	6004 in octal ("0" prefix)
`0x1774`	6004 in hex ("0x" prefix)

Scale Factor	Pronounced	Multiplier
T, t	tera	1E12
G, g	giga	1E9
MEG, meg	mega	1E6
K, k	kilo	1E3
M, m	milli	1E-3
U, u	micro	1E-6
MIL, mil		25.4E-6
N,n	nano	1E-9
P, p	pico	1E-12
F, f	femto	1E-15

Useful Advice

- "0" is ground.
- Don't end bus names with numbers. See above.
- Ctrl+S doesn't save, you must use the save button.
- You can add plots after you simulate, just type a plot command in the white boxes.
- Plot "0", it will be easier to see the time on a plot of "0".

Standard Cell Library from nominal.jsim

Netlist	*Function*	t_{CD} *(ns)*	t_{PD} *(ns)*	t_R *(ns/pf)*	t_F *(ns/pf)*	*load (pf)*	*size* (μ^2)
`Xid z constant0`	$Z = 0$	—	—	—	—	—	0
`Xid z constant1`	$Z = 1$	—	—	—	—	—	0
`Xid a z inverter`	$Z = \overline{A}$	.005	.02	2.3	1.2	.007	10
`Xid a z inverter_2`		.009	.02	1.1	.6	.013	13
`Xid a z inverter_4`		.009	.02	.56	.3	.027	20
`Xid a z inverter_8`		.02	.11	.28	.15	.009	56
`Xid a z buffer`	$Z = A$	.02	.08	2.2	1.2	.003	13
`Xid a z buffer_2`		.02	.07	1.1	.6	.005	17
`Xid a z buffer_4`		.02	.07	.56	.3	.01	30
`Xid a z buffer-8`		.02	.07	.28	.15	.02	43
`Xid e a z tristate`	$Z = A$ when e=1 else Z not driven	.03	.15	2.3	1.3	.004	23
`Xid e a z tristate_2`		.03	.13	1.1	.6	.006	30
`Xid e a z tristate_4`		.02	.12	.6	.3	.011	40
`Xid e a z tristate_8`		.02	.11	.3	.17	.02	56
`Xid a b z and2`	$Z = A \cdot B$	.03	.12	4.5	2.3	.002	13
`Xid a b c z and3`	$Z = A \cdot B \cdot C$	.03	.15	4.5	2.6	.002	17
`Xid a b c d z and4`	$Z = A \cdot B \cdot C \cdot D$	.03	.16	4.5	2.5	.002	20
`Xid a b z nand2`	$Z = \overline{A \cdot B}$	.01	.03	4.5	2.8	.004	10
`Xid a b c z nand3`	$Z = \overline{A \cdot B \cdot C}$	.01	.05	4.2	3.0	.005	13
`Xid a b c d z nand4`	$Z = \overline{A \cdot B \cdot C \cdot D}$	.01	.07	4.4	3.5	.005	17
`Xid a b z or2`	$Z = A + B$	.03	.15	4.5	2.5	.002	13
`Xid a b c z or3`	$Z = A + B + C$	.04	.21	4.5	2.5	.003	17
`Xid a b c d z or4`	$Z = A + B + C + D$	.06	.29	4.5	2.6	.003	20
`Xid a b z nor2`	$Z = \overline{A + B}$	.01	.05	6.7	2.4	.004	10
`Xid a b c z nor3`	$Z = \overline{A + B + C}$	.02	.08	8.5	2.4	.005	13
`Xid a b c d z nor4`	$Z = \overline{A + B + C + D}$	.02	.12	9.5	2.4	.005	20
`Xid a b z xor2`	$Z = A \oplus B$	.03	.14	4.5	2.5	.006	27
`Xid a b z xnor2`	$Z = \overline{A \oplus B}$	.03	.14	4.5	2.5	.006	27
`Xid a1 a2 b z aoi21`	$Z = \overline{(A1 \cdot A2) + B}$	.02	.07	6.8	2.7	.005	13
`Xid a1 a2 b z oai21`	$Z = \overline{(A1 + A2) \cdot B}$	.02	.07	6.7	2.7	.005	17
`Xid s d0 d1 z mux2`	Z = D0 when S = 0 Z = D1 when S = 1	.02	.12	4.5	2.5	.005	27
`Xid s0 s1 d0 d1 d2 d3 z mux4` *(Note order of s0 and s1!)*	Z=D0 when S_0=0, S_1=0 Z=D1 when S_0=1, S_1=0 Z=D2 when S_0=0, S_1=1 Z=D3 when S_0=1, S_1=1	.04	.19	4.5	2.5	.006	66
`Xid d clk q dreg` t_{setup} = .15, t_{hold} = 0	D→Q on CLK↑	.03	.19	4.3	2.5	.002	56
`Xid d clk q dlatch` *(do not use)*	D→Q while CLK↑	.03	.19	4.3	2.5	.002	36