Eksempler

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List

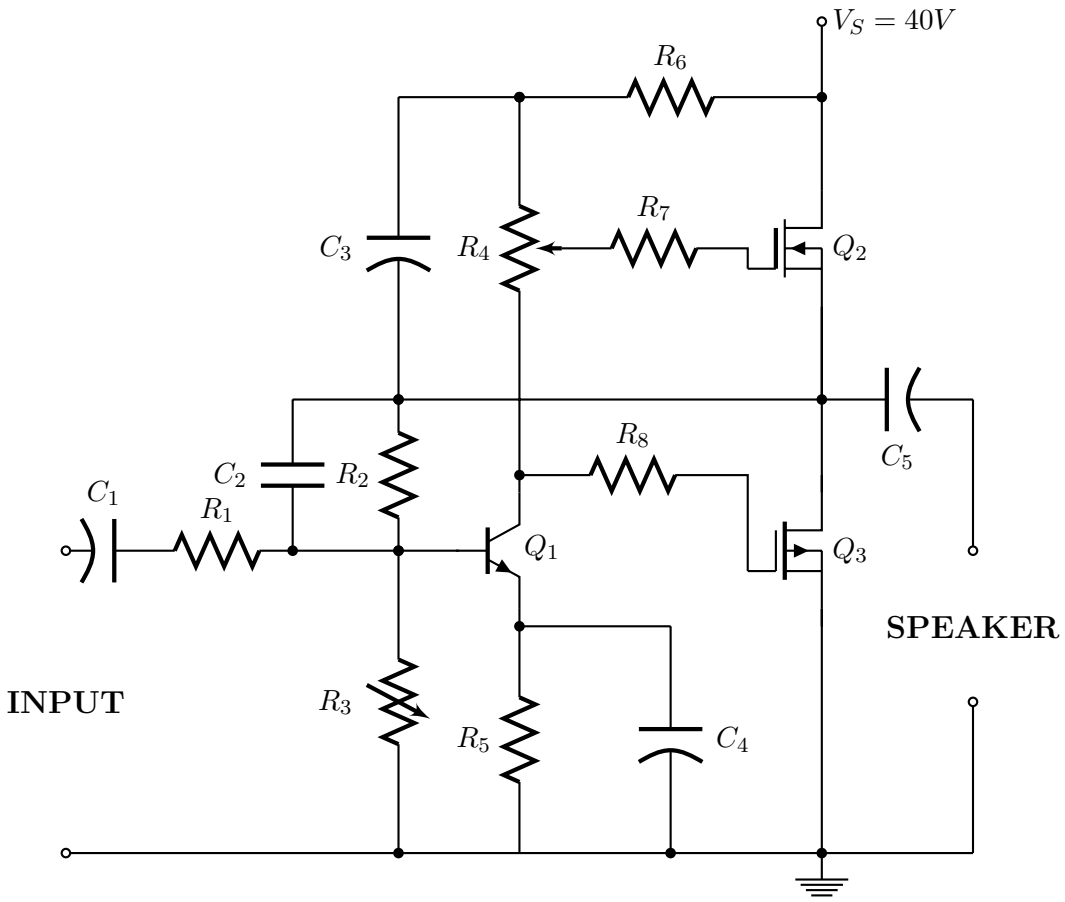
```
1  library ieee;
2  use ieee.std_logic_1164.all;
3
4  entity half_adder is              -- Initialising entity
5    port (a, b : in std_logic;          -- Defining inputs
6      sum, carry_out : out std_logic);  -- Defining outputs
7  end half_adder;
8
9  architecture dataflow2 of half_adder is   -- Architecture of half_adder
10   begin
11   sum <= a xor b;               -- (a xor b) is written to sum
12   carry_out <= a and b;           -- (a and b) is written to carry_out
13 end dataflow2;
```

Tabel

Condition	Invalid ECs	Valid ECs
Row	$< 0[1]; < 15[2]$	$0 - 15[3]$
Column	$< 0[4]; < 15[5]$	$0 - 15[6]$
Tiles	$\in \{mountains\}[7]$	$\notin \{mountains\}[8]$
Unit	$> 1[9]; friendlyunit[10]$	$1[11]; 0[12]$
Unit action	$moveUnit(fortify)$	

Figur 1: EC table of moveUnit

18W MOSFET



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