

<b>Course Title:</b>	Computer Organization and Architecture
<b>Course Number:</b>	COE608
<b>Semester/Year (e.g.F2016)</b>	Winter 2023

<b>Instructor:</b>	Demetres Kostas
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<b>Assignment/Lab Number:</b>	6
<b>Assignment/Lab Title:</b>	The Complete CPU (Overall Project)

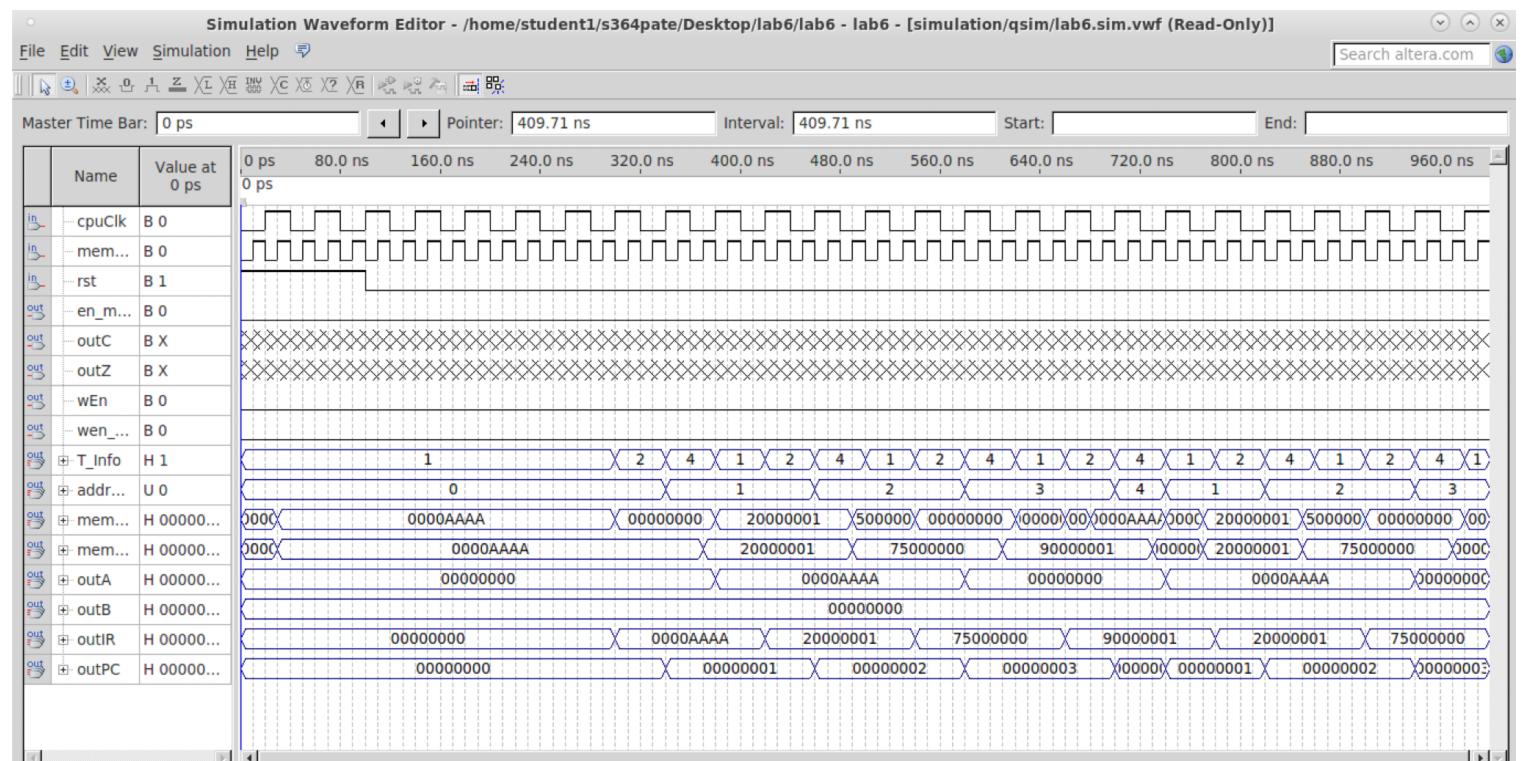
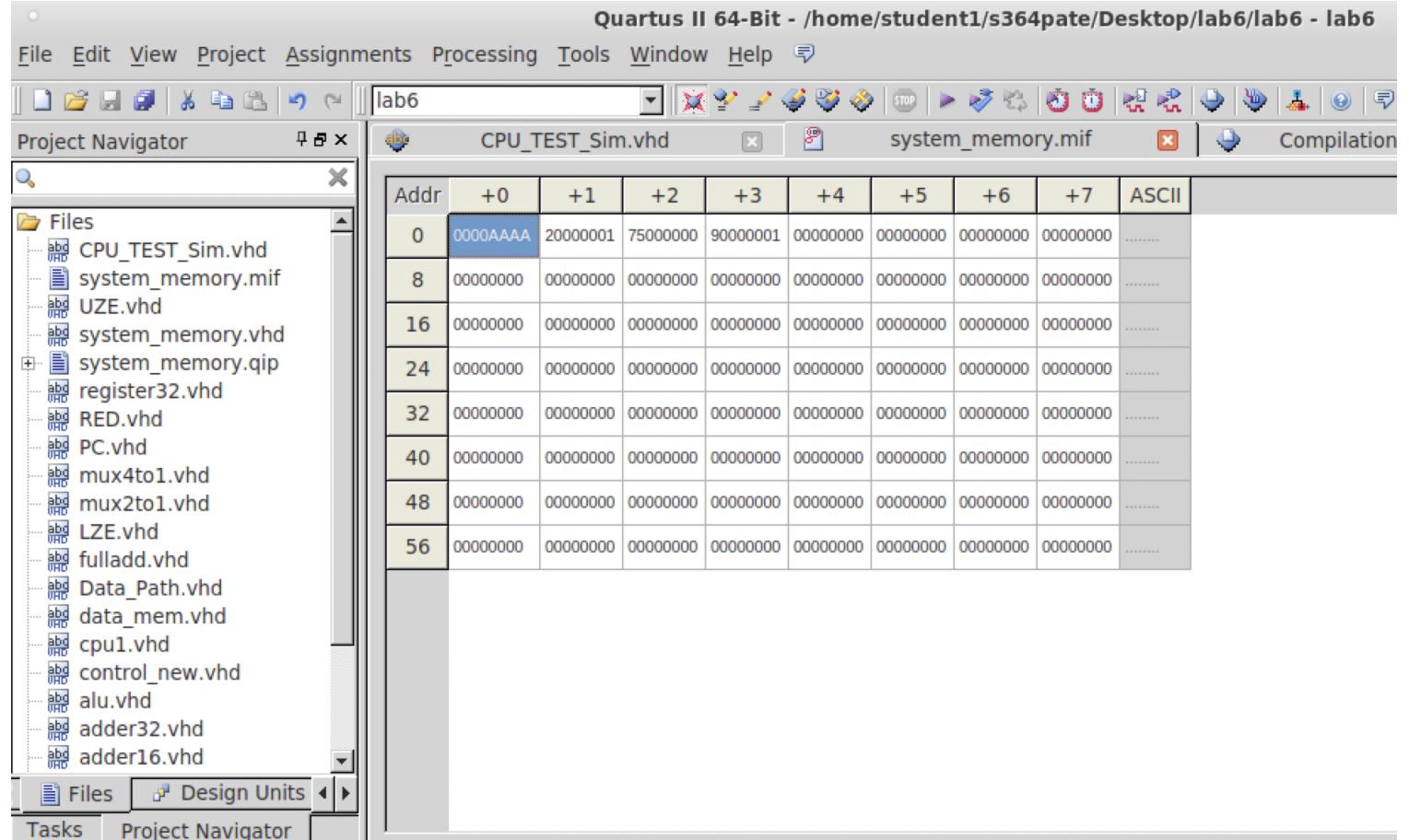
<b>Submission Date:</b>	Tuesday April 11 2023
<b>Due Date:</b>	Wednesday April 12 2023 3:00pm

Student LAST Name	Student FIRST Name	Student Number	Section	Signature*
Patel	Stuti	501026370	04	S.P

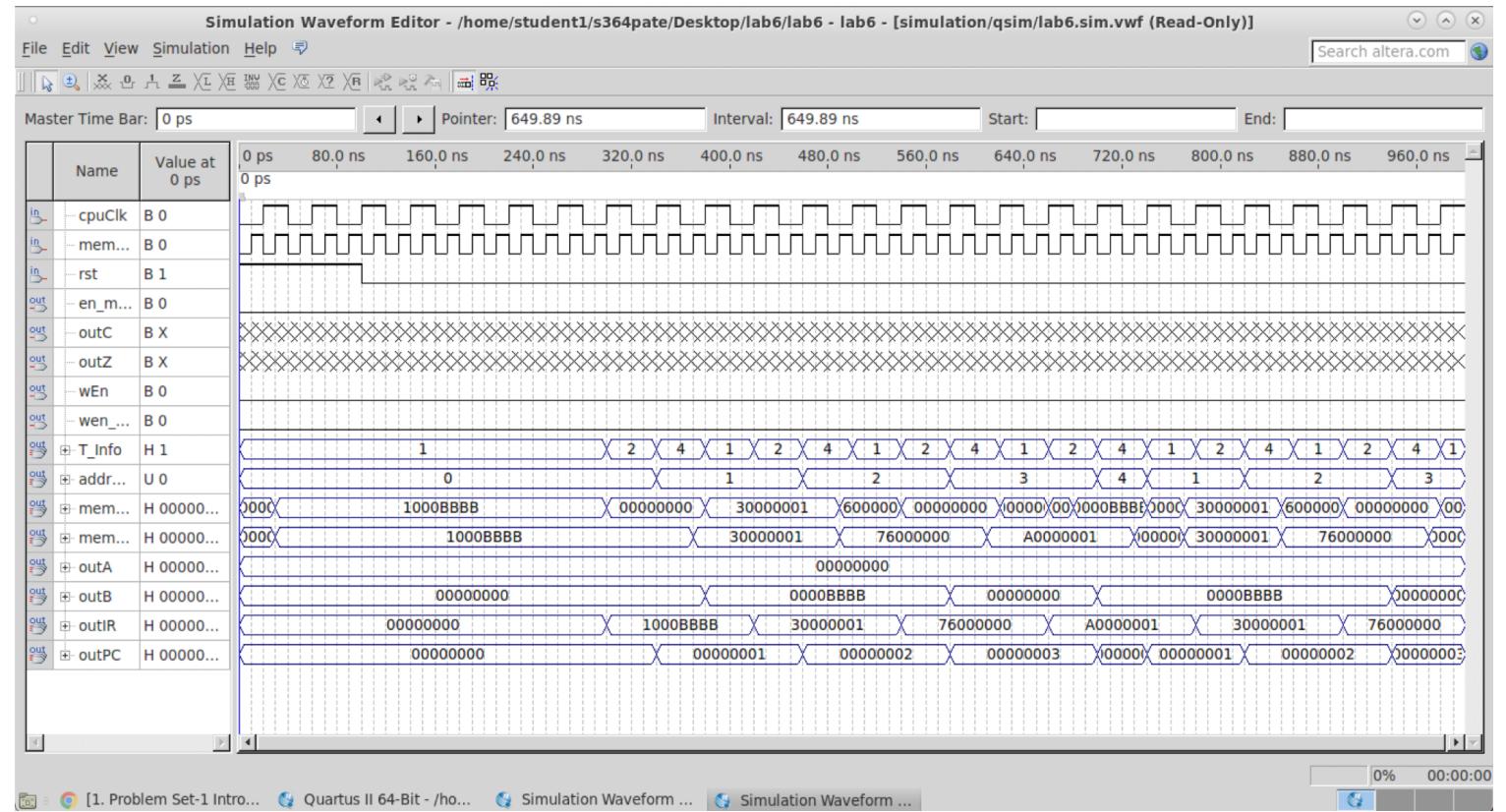
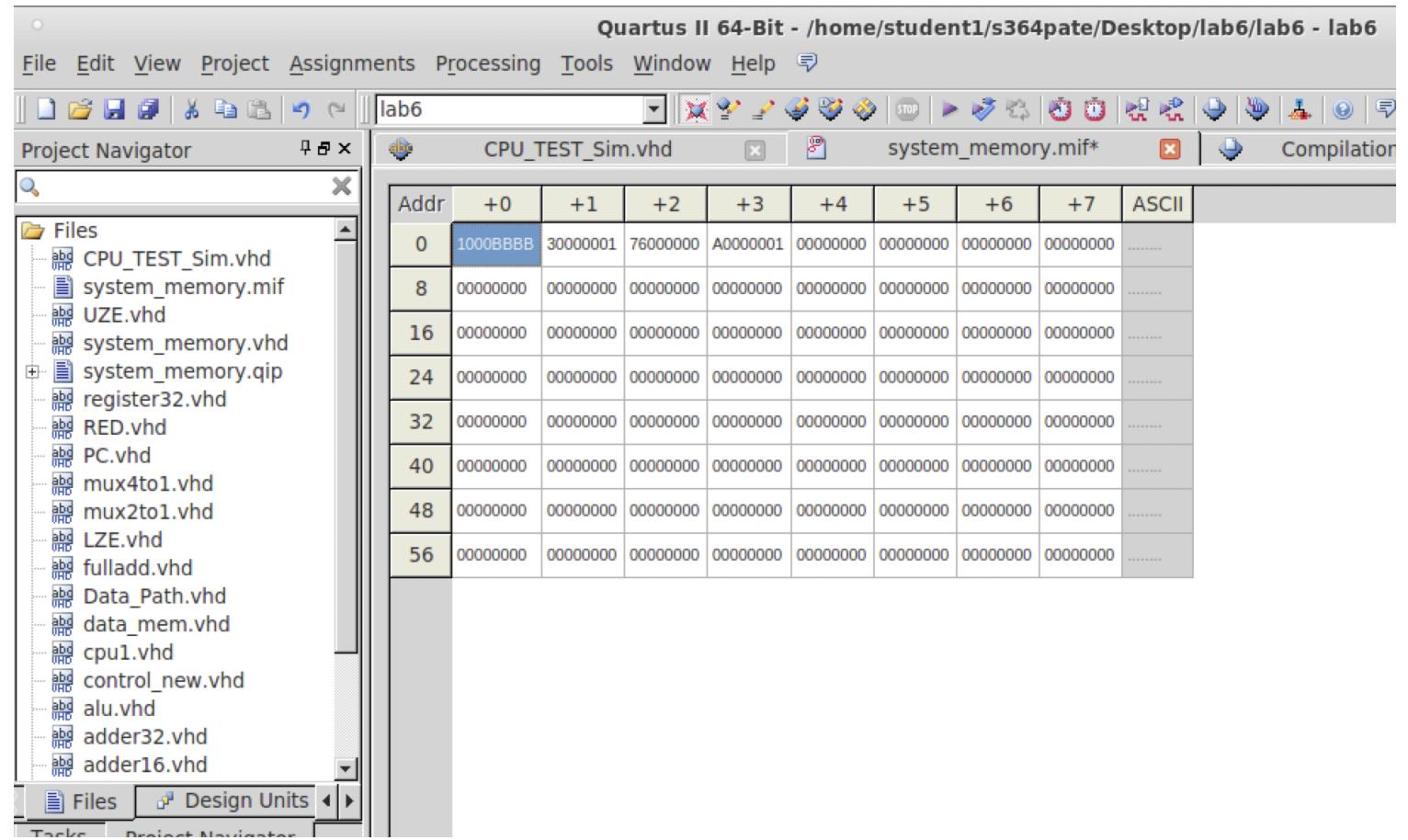
\*By signing above you attest that you have contributed to this written lab report and confirm that all work you have contributed to this lab report is your own work. Any suspicion of copying or plagiarism in this work will result in an investigation of Academic Misconduct and may result in a "0" on the work, an "F" in the course, or possibly more severe penalties, as well as a Disciplinary Notice on your academic record under the Student Code of Academic Conduct, which can be found online at: <http://www.ryerson.ca/senate/current/pol60.pdf>

## Functional Simulations

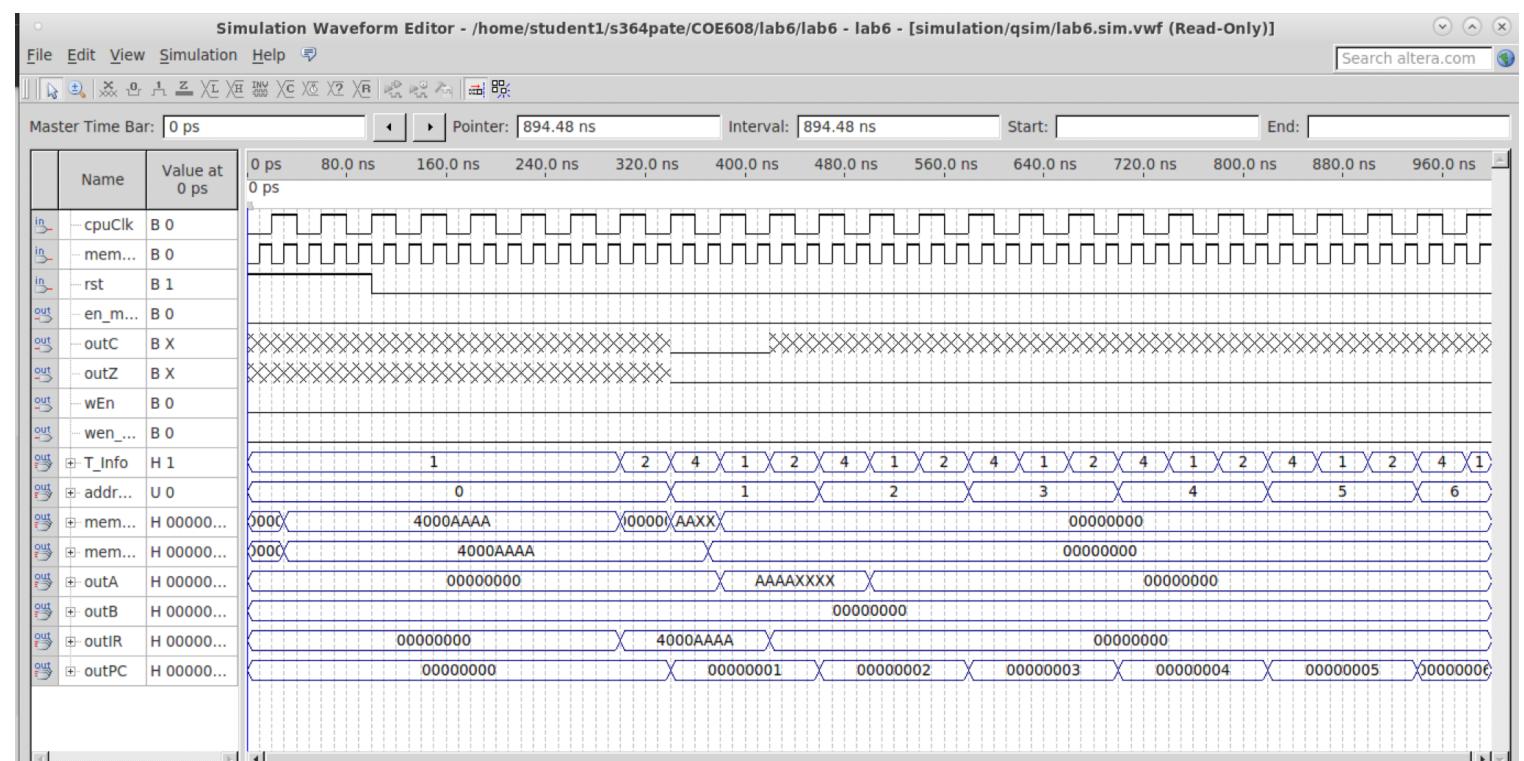
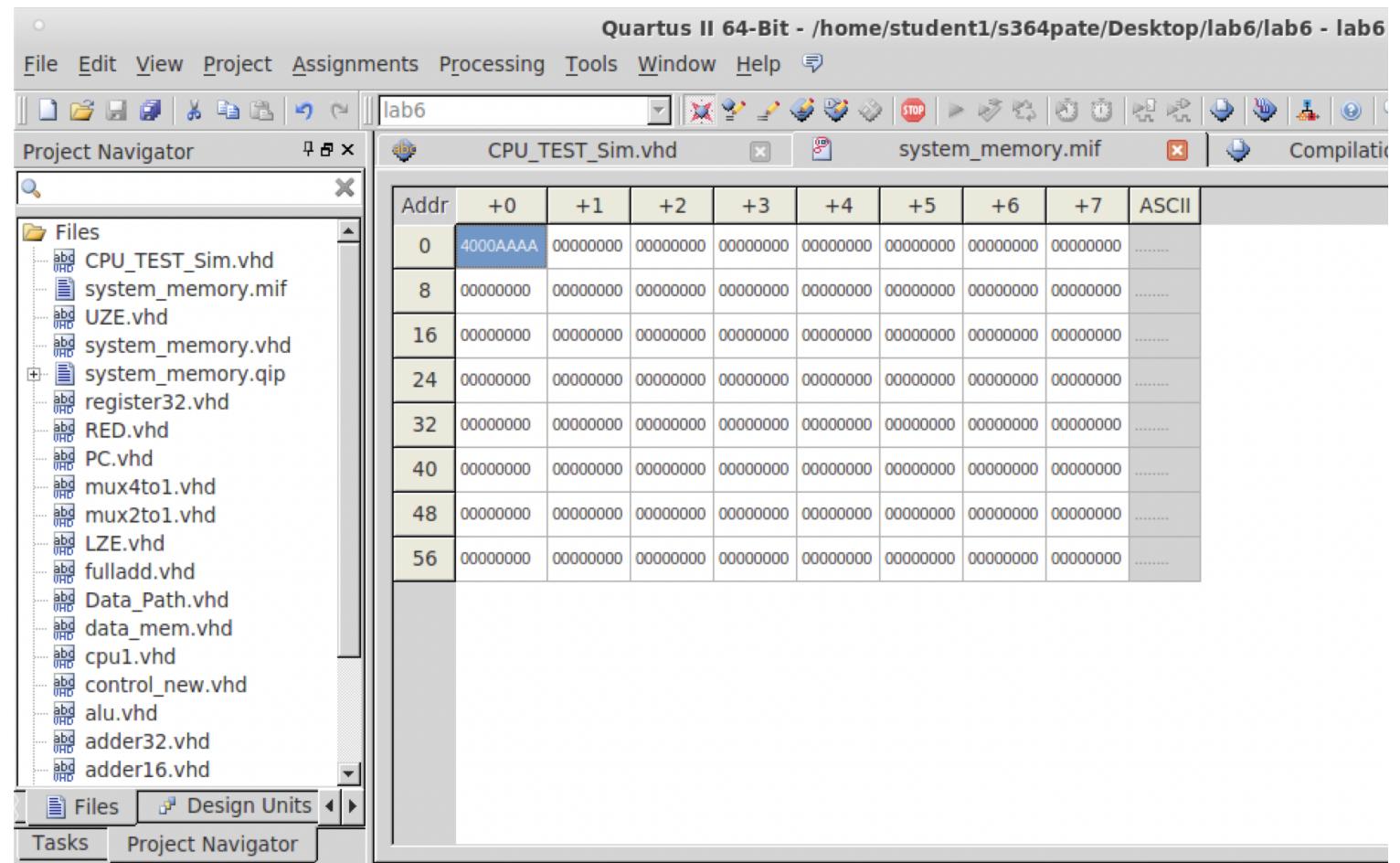
LDAI, STA, CLRA, LDA



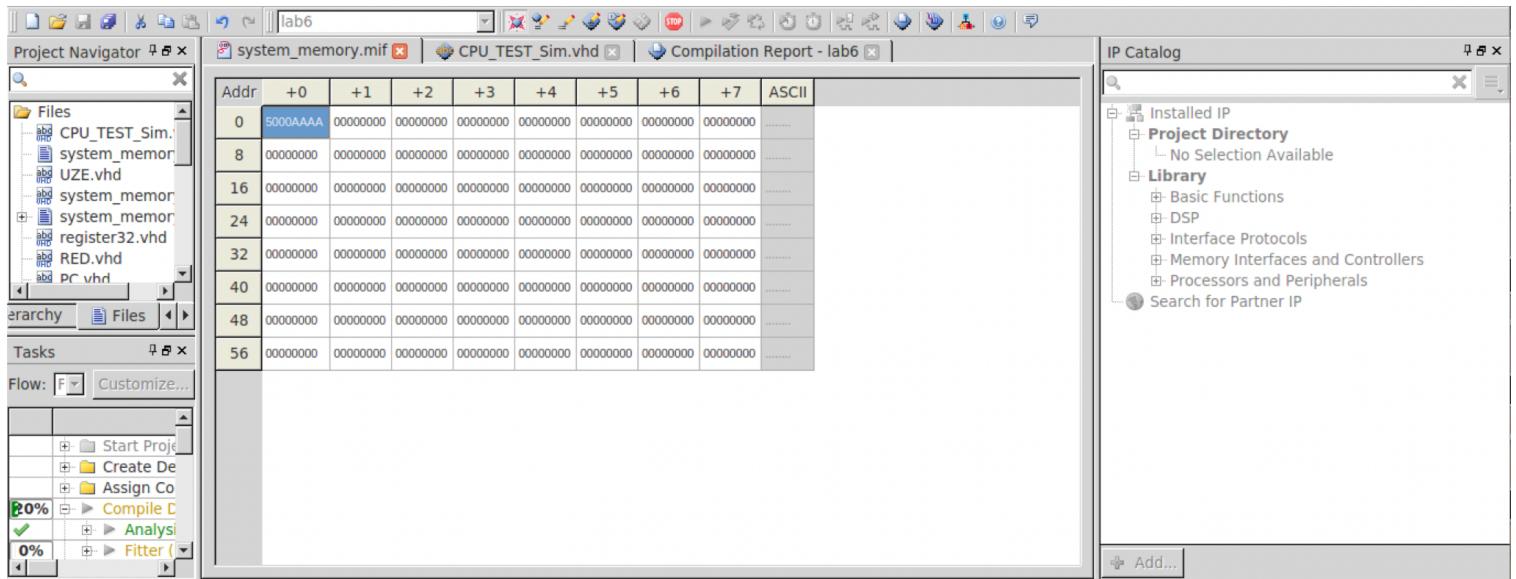
## LDBI, STB, CLRb, LDB



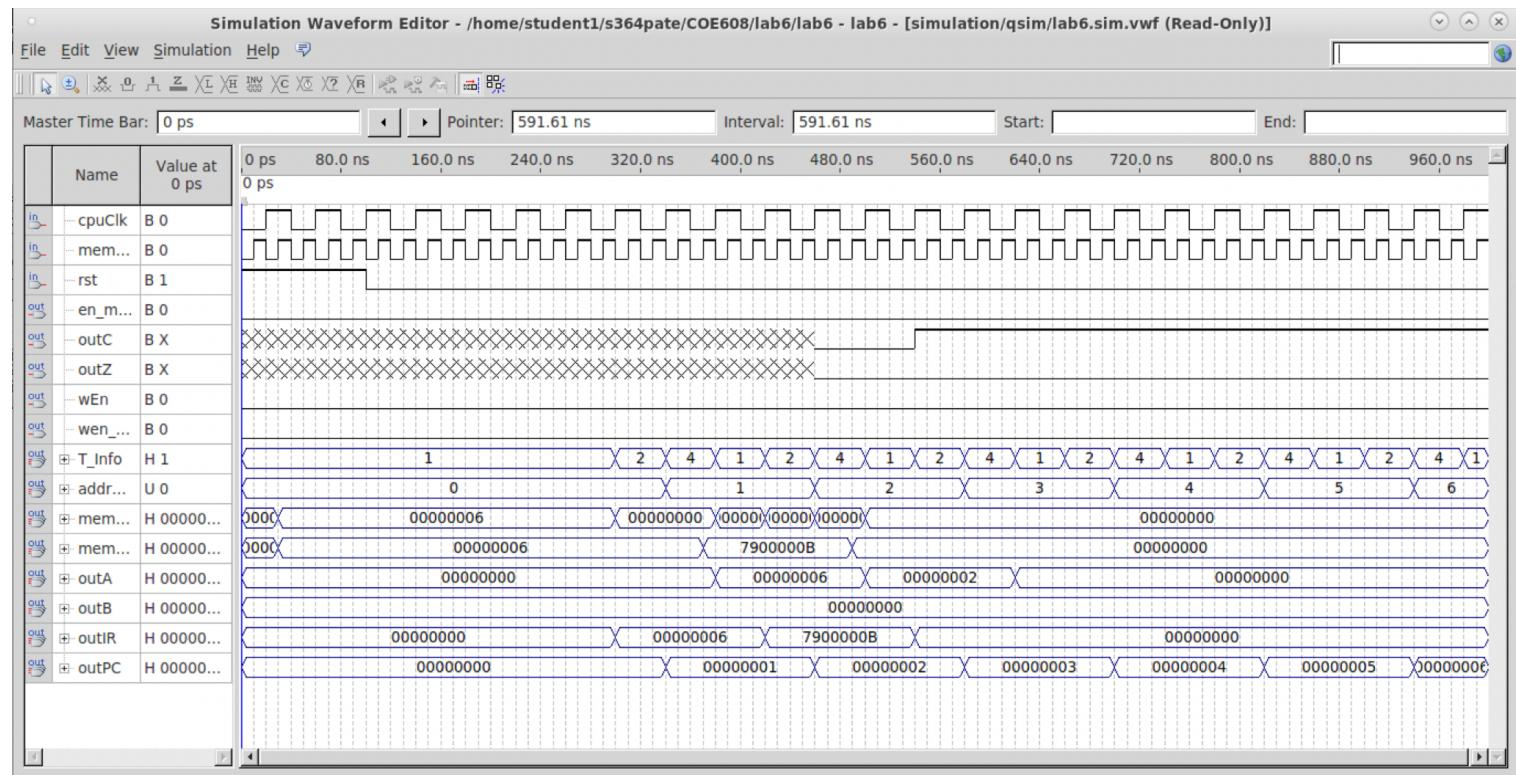
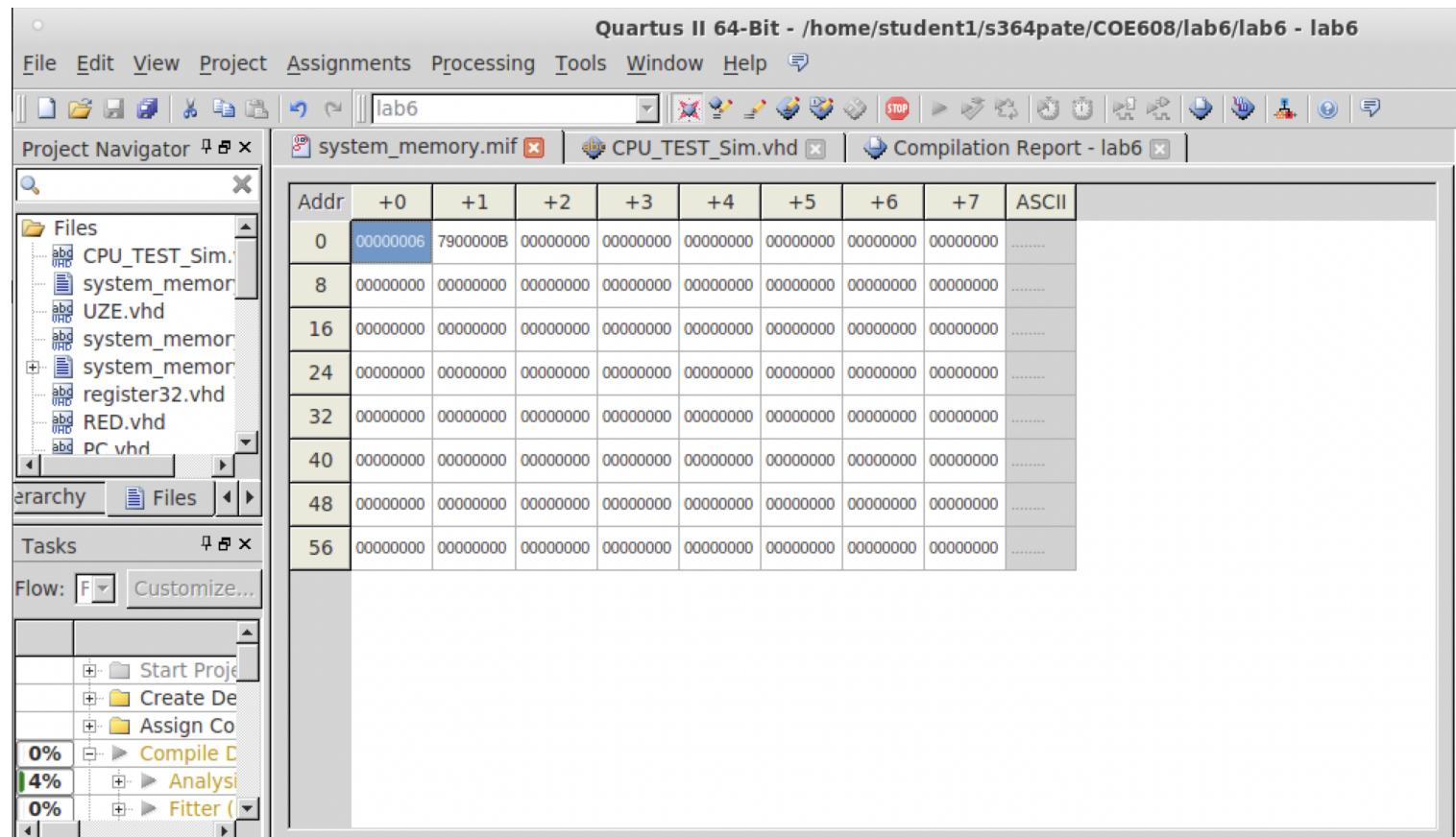
# LUI



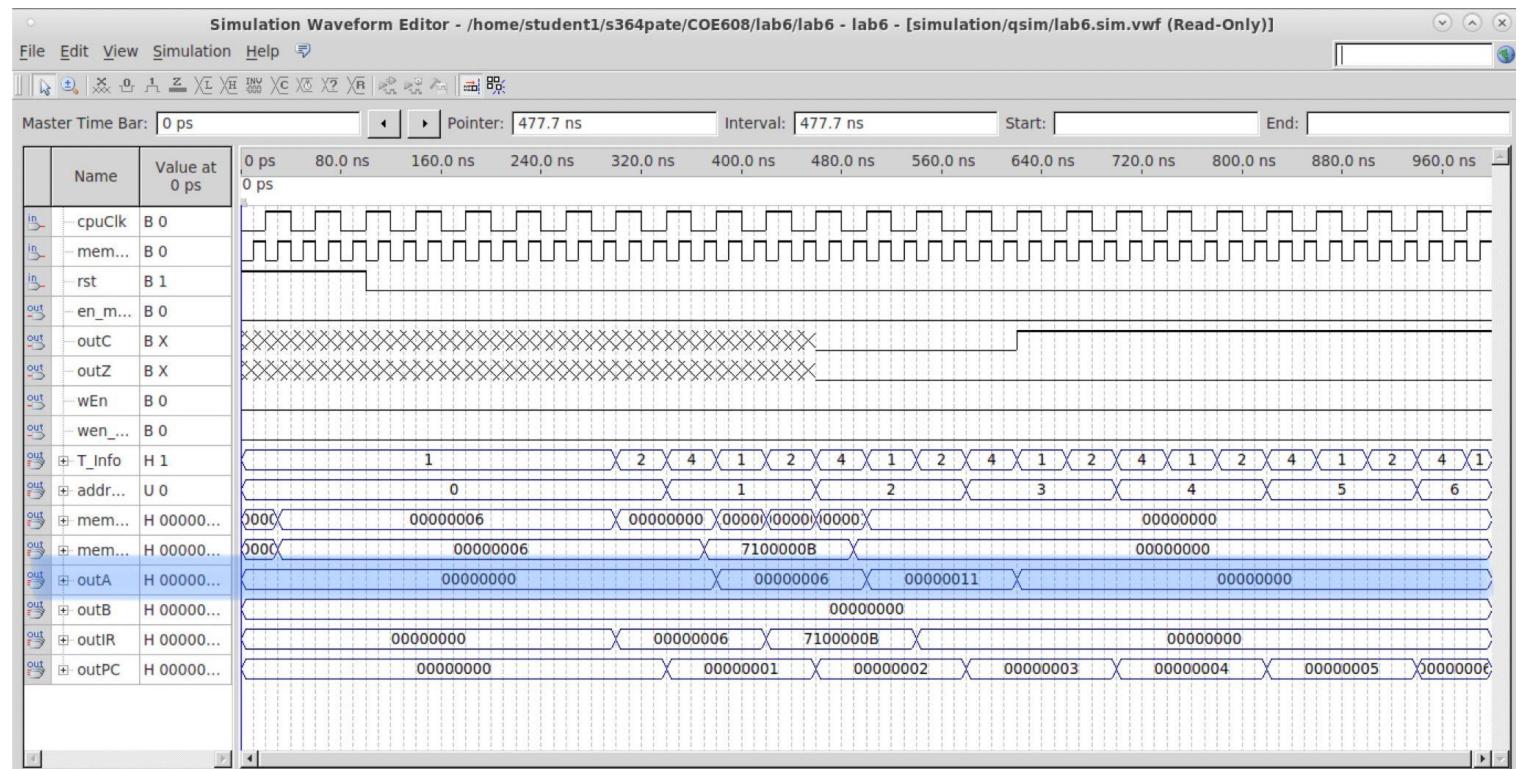
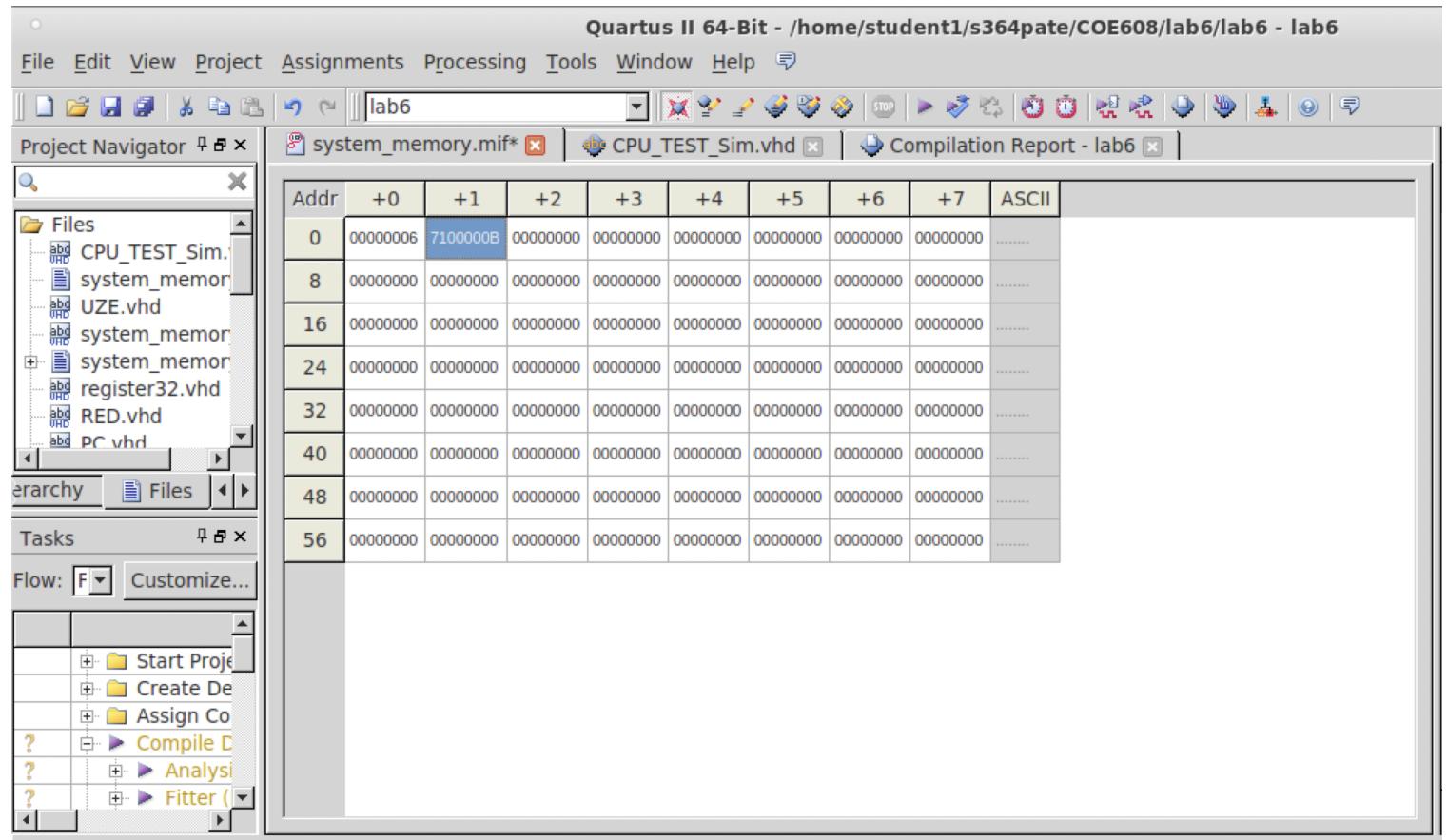
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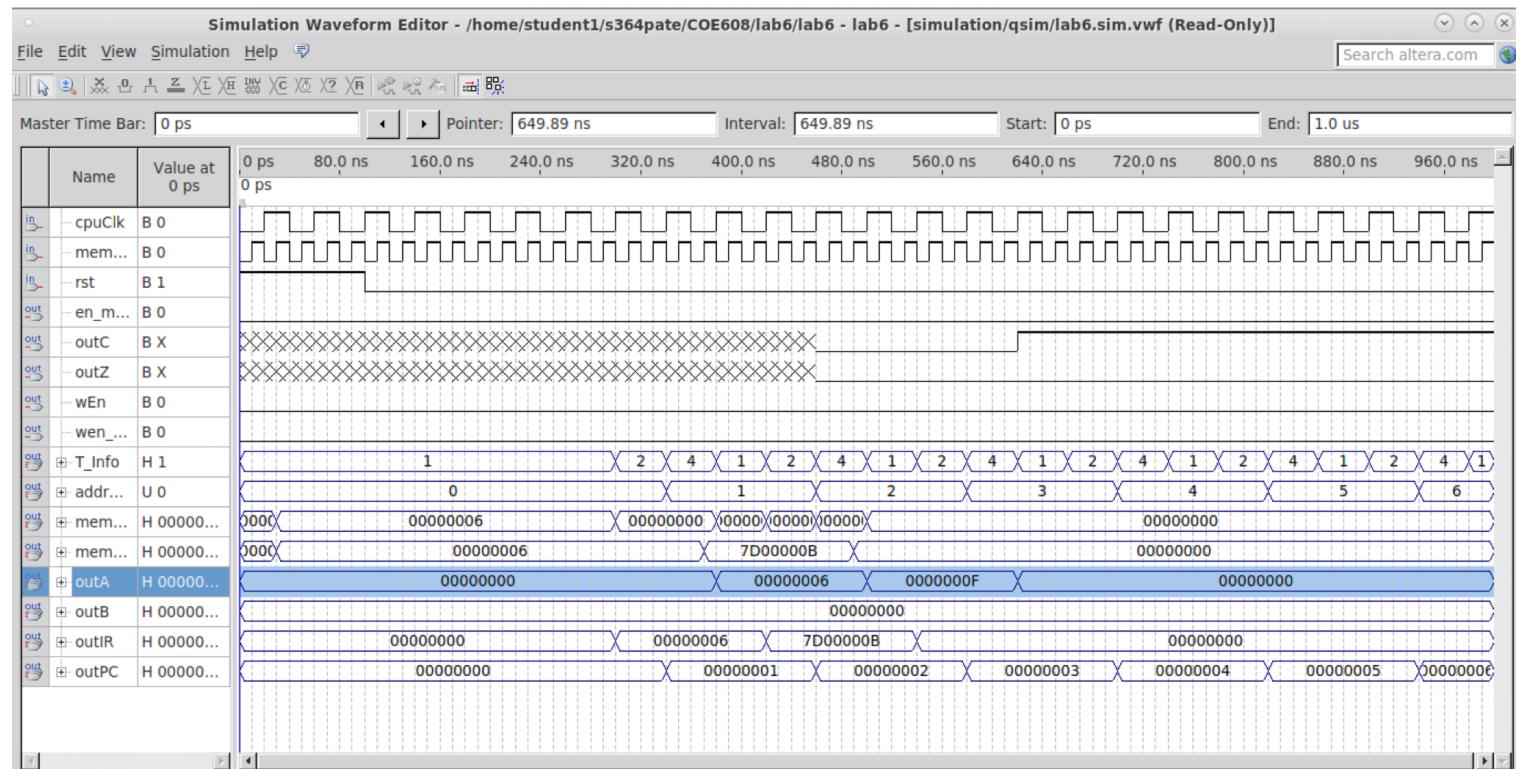
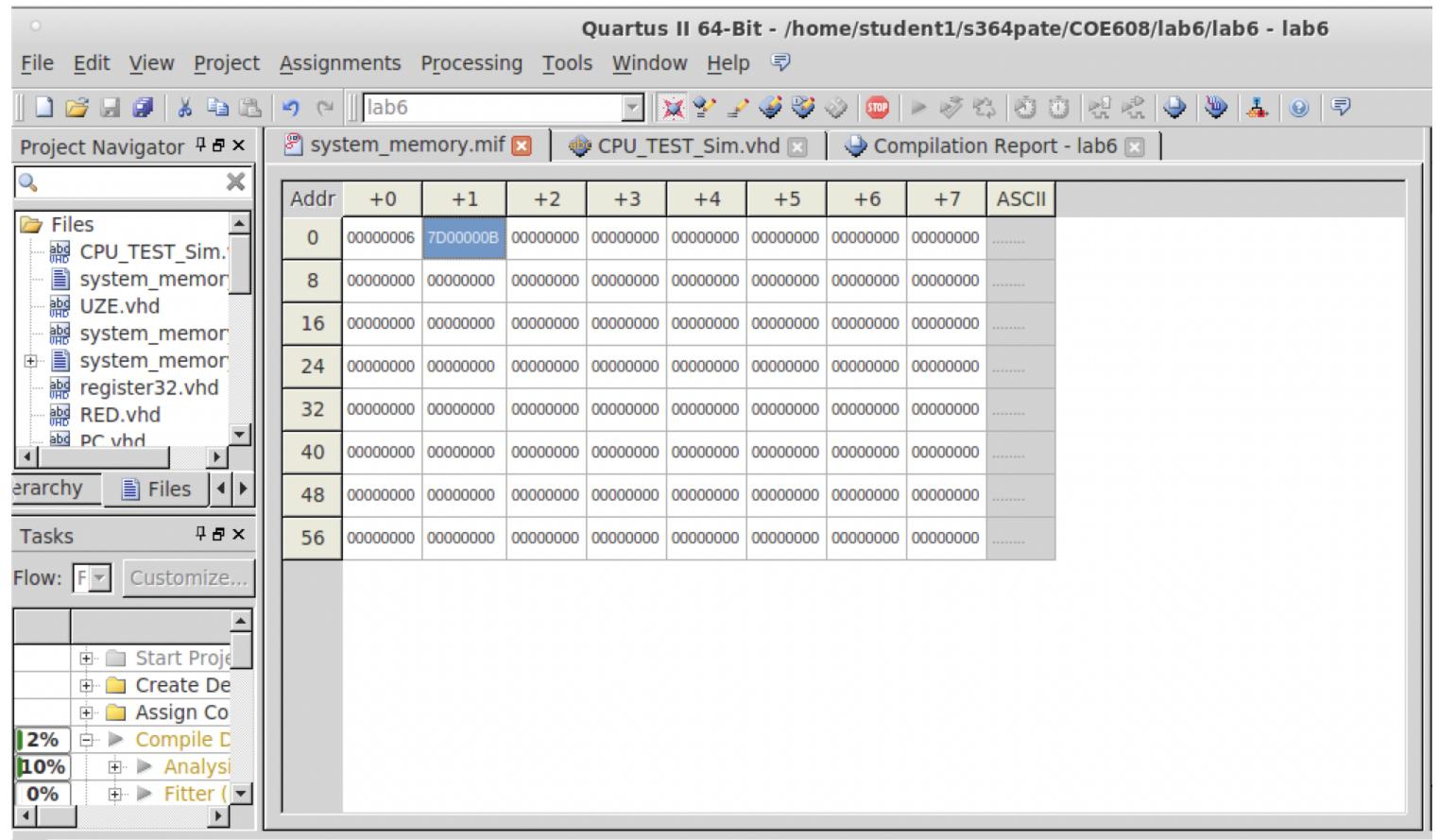
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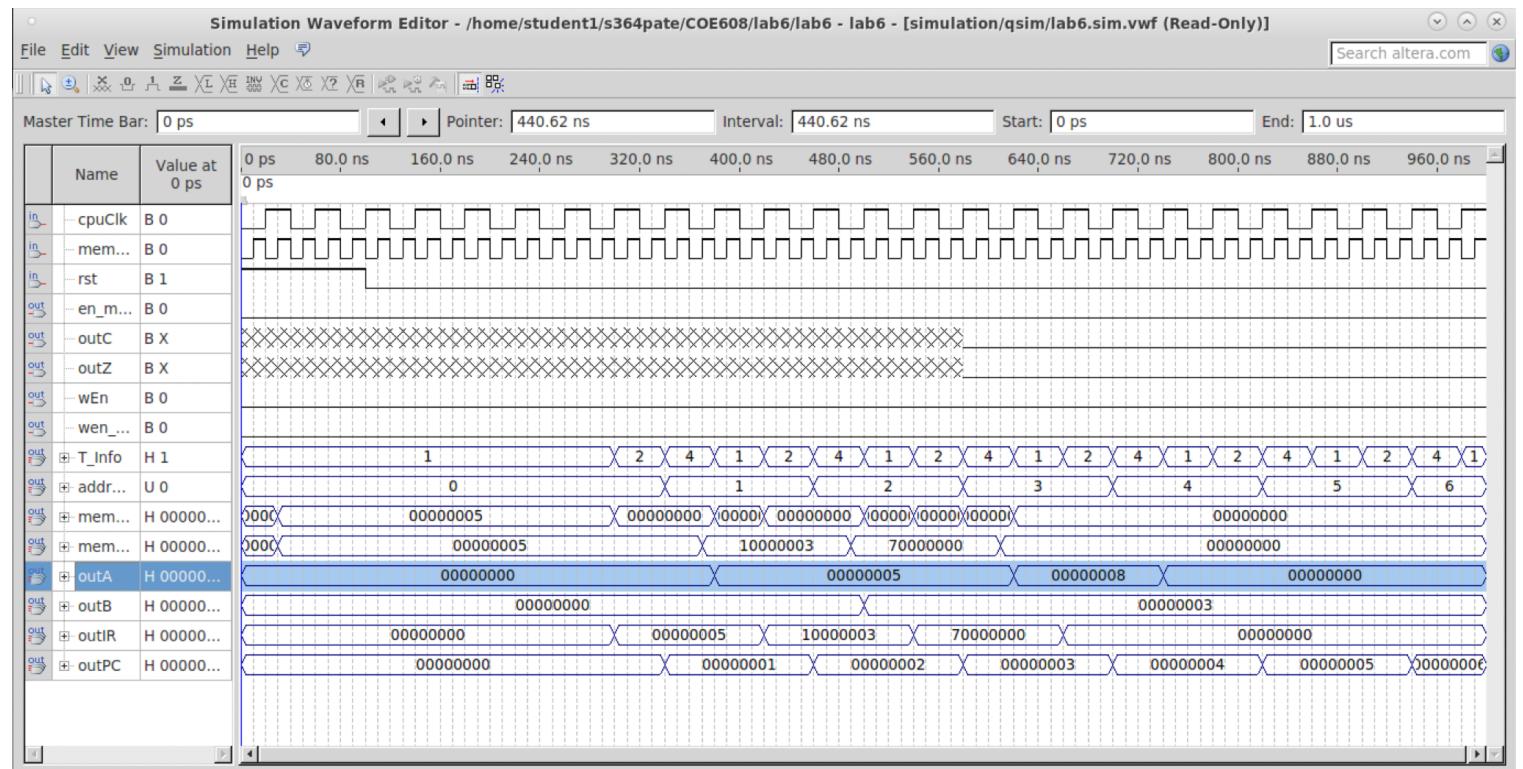
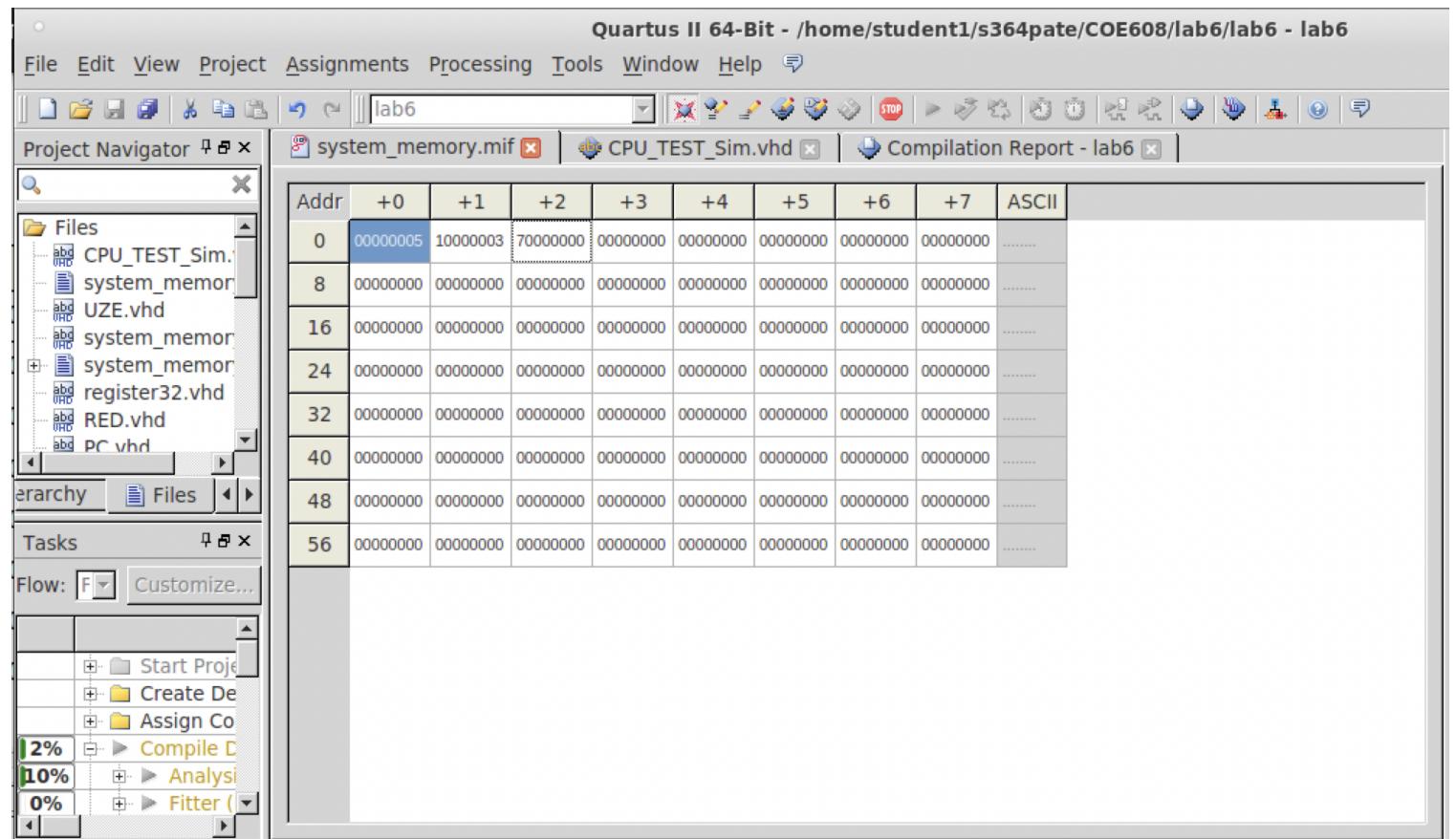
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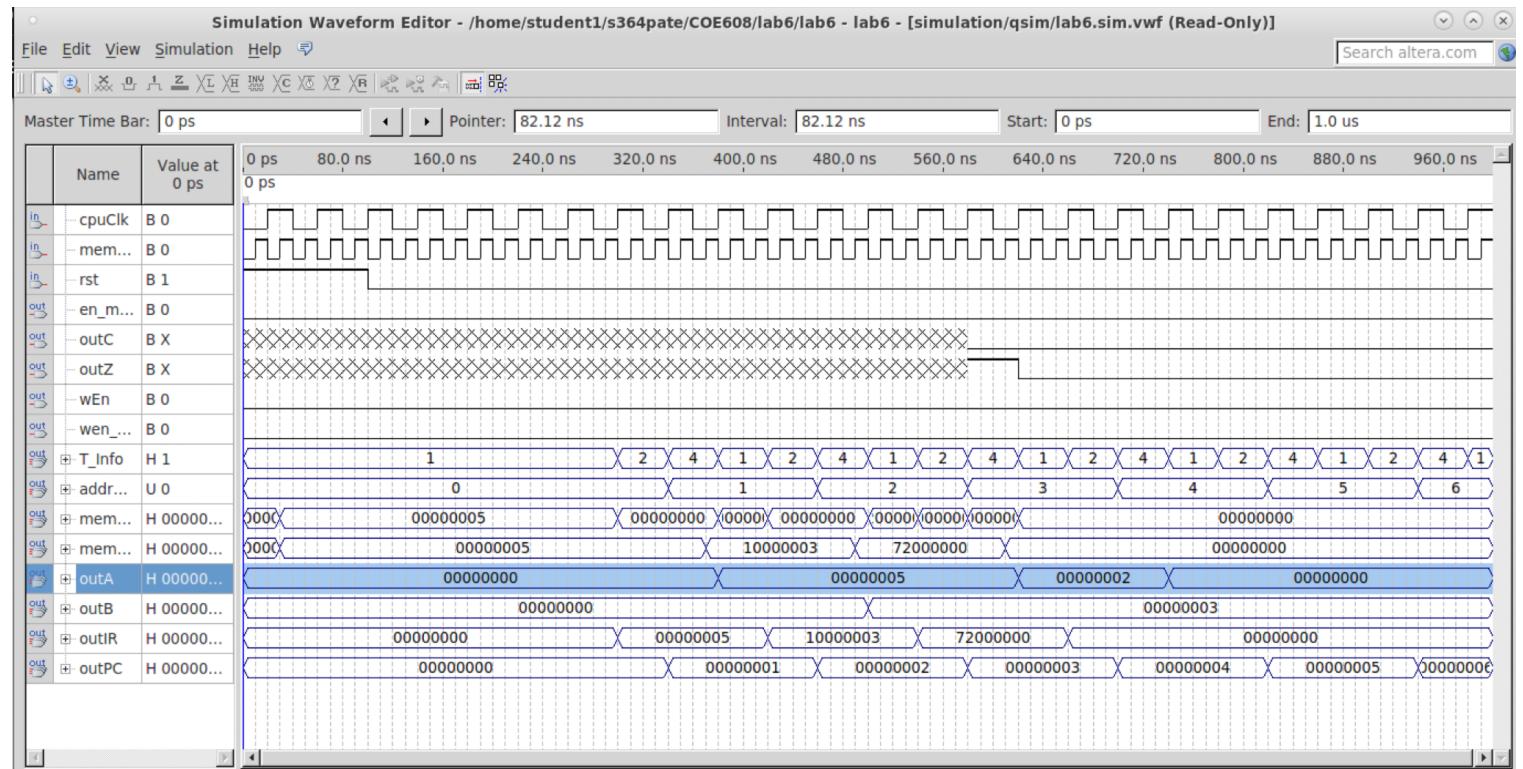
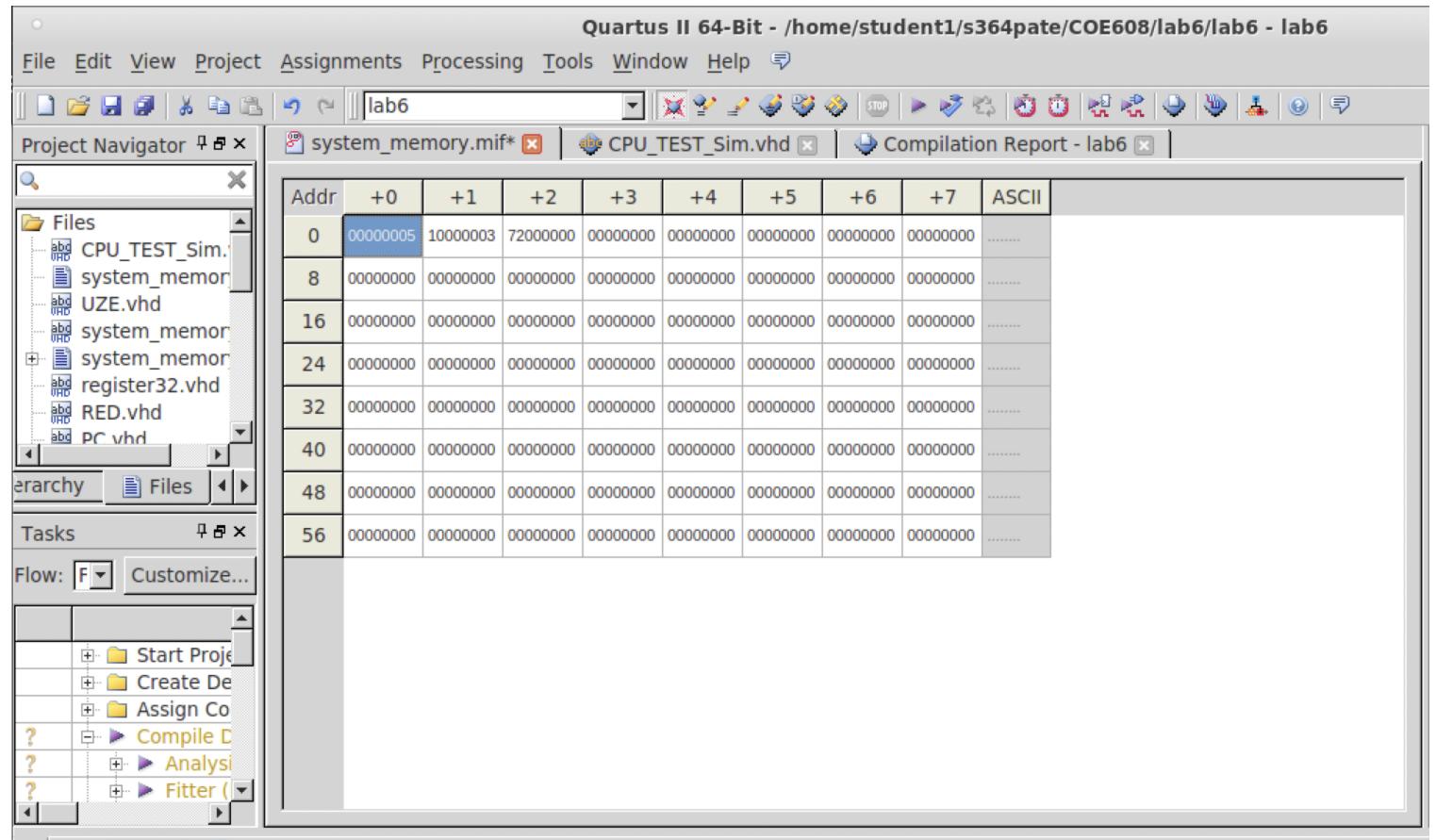
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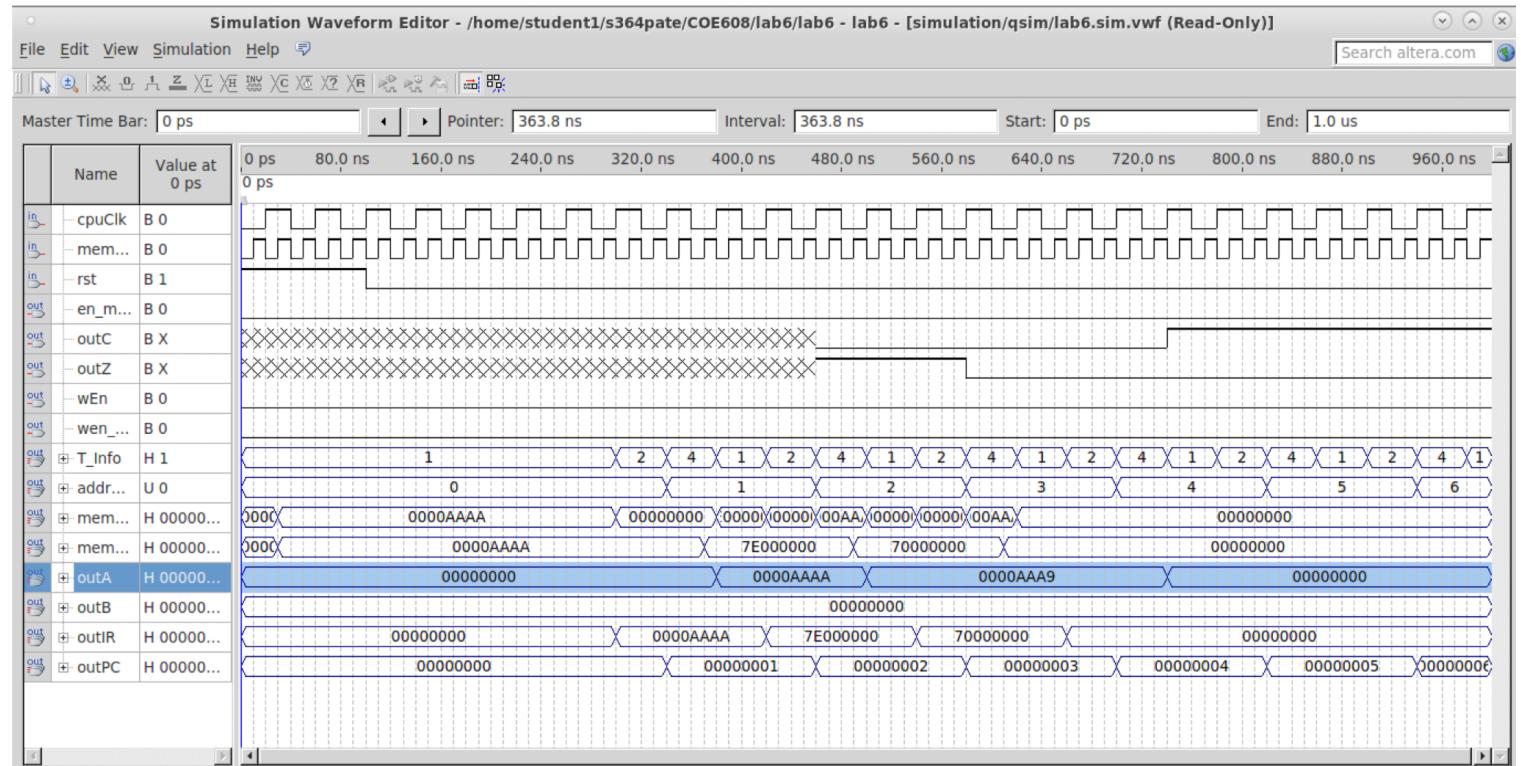
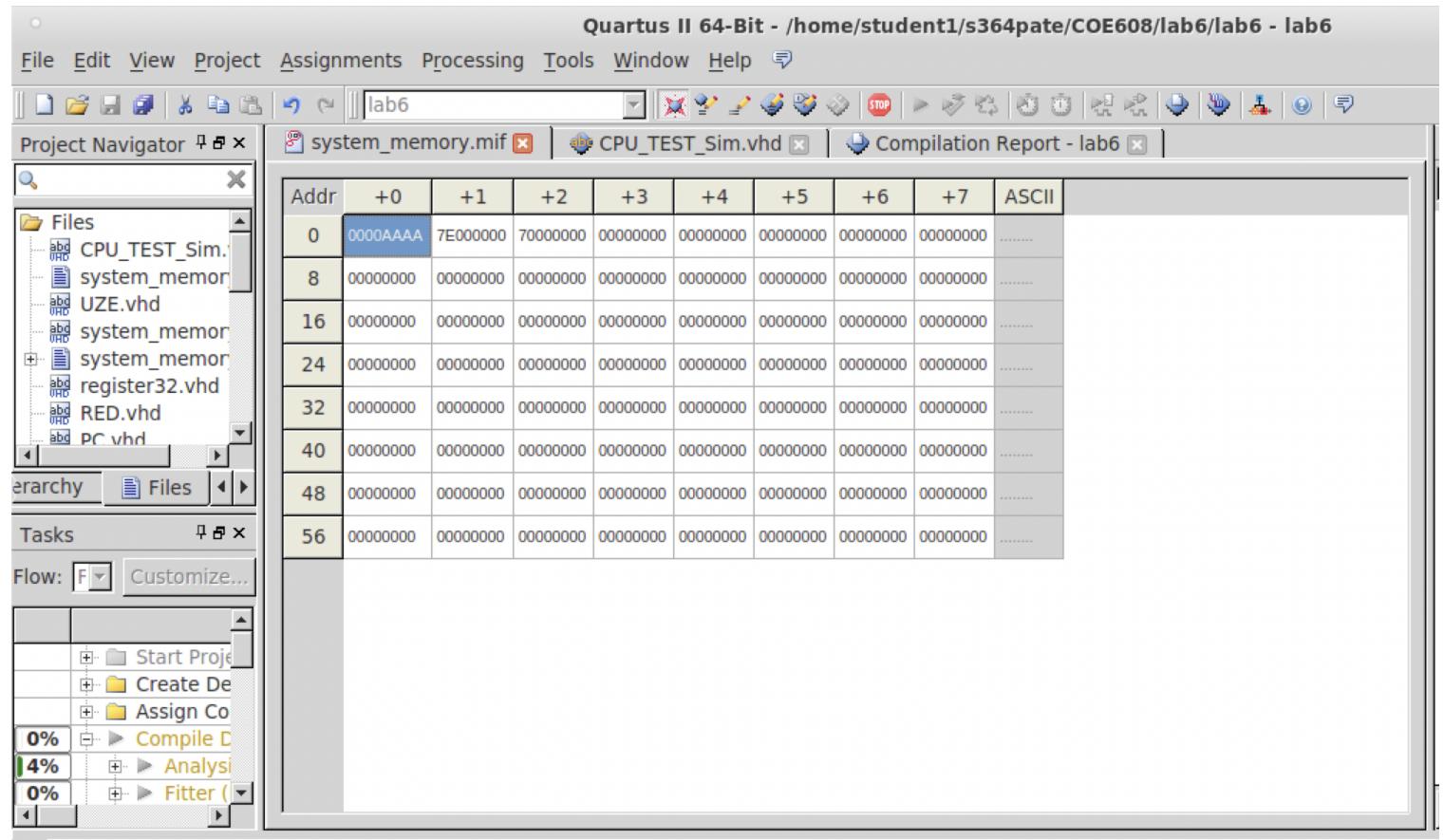
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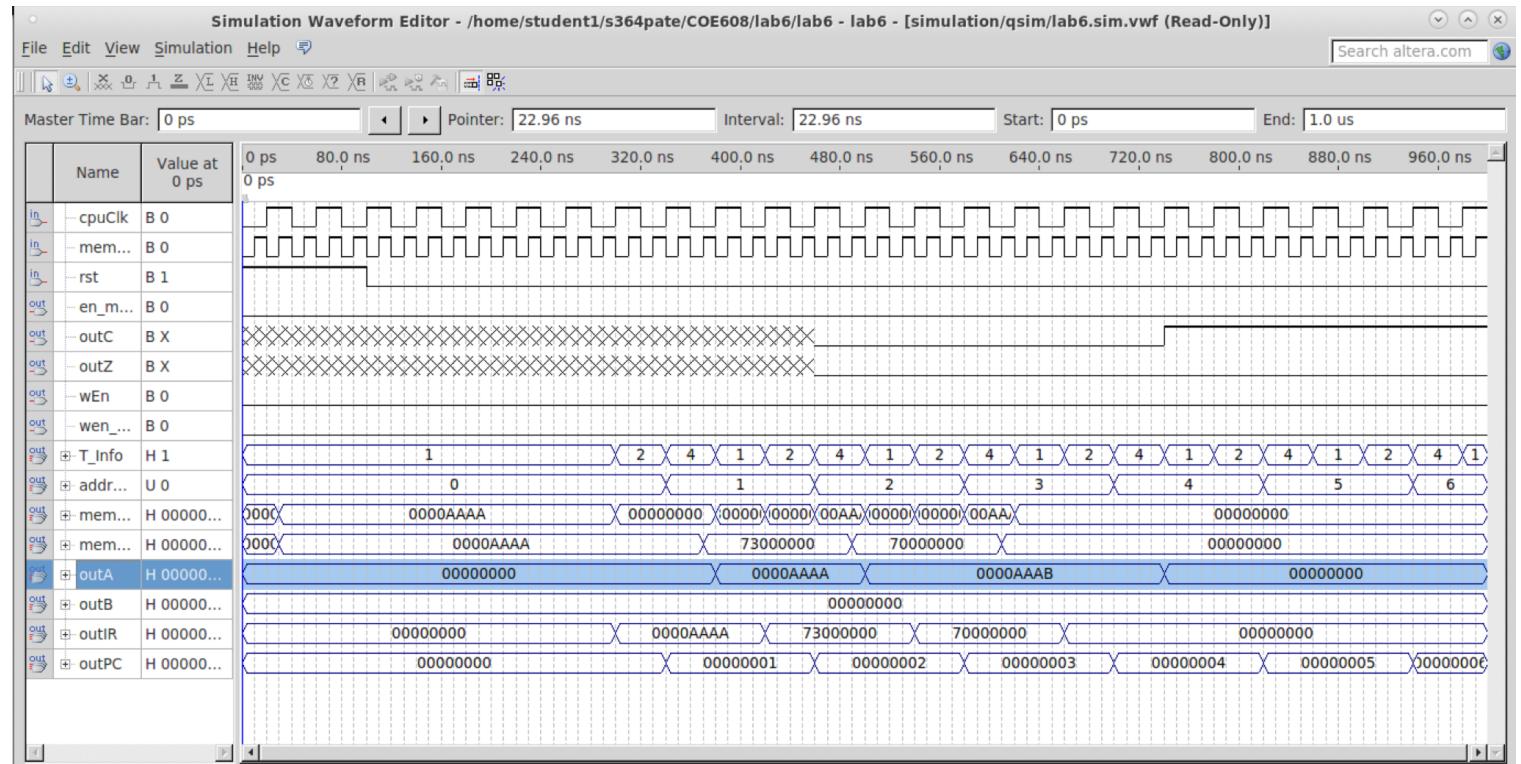
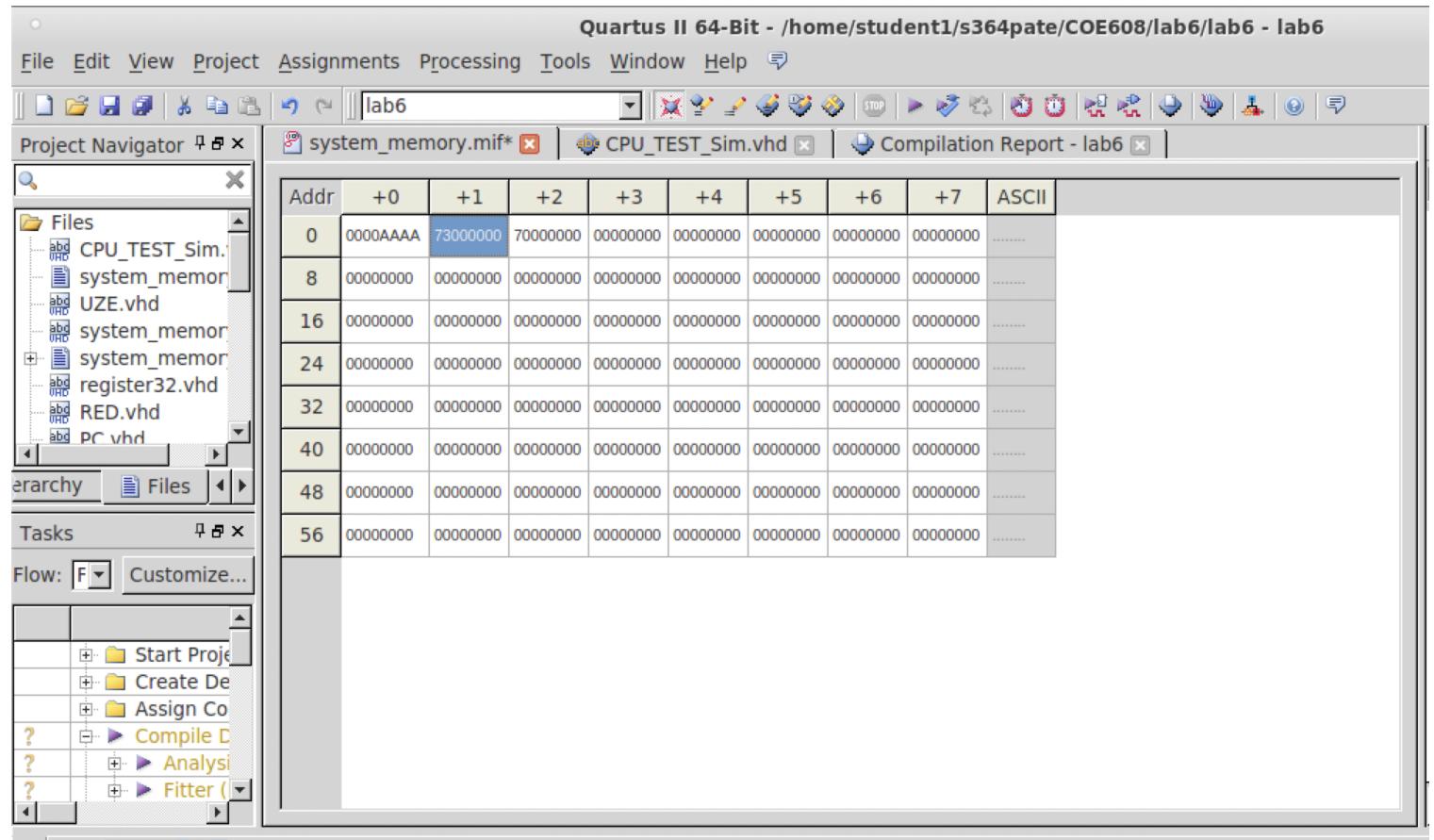
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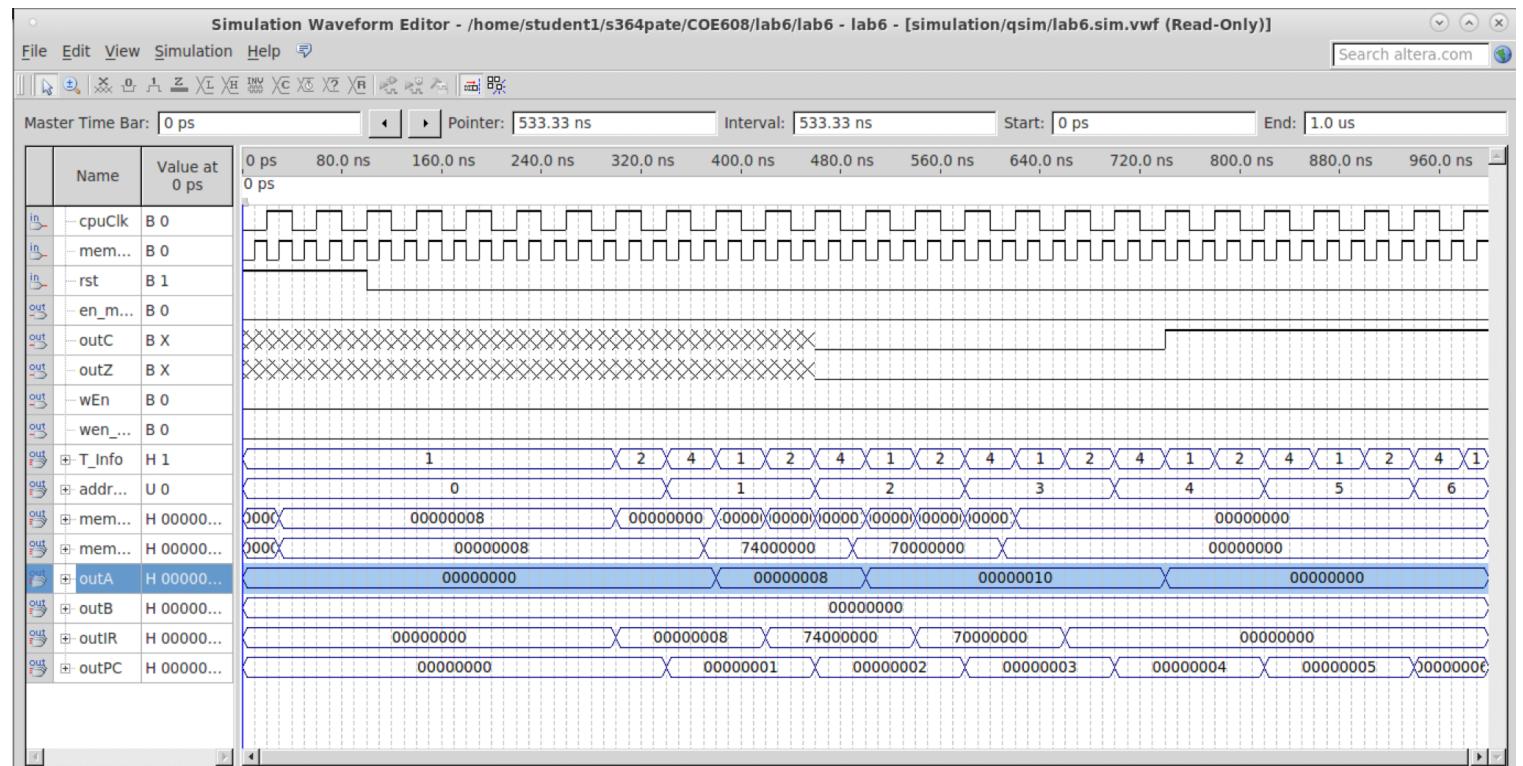
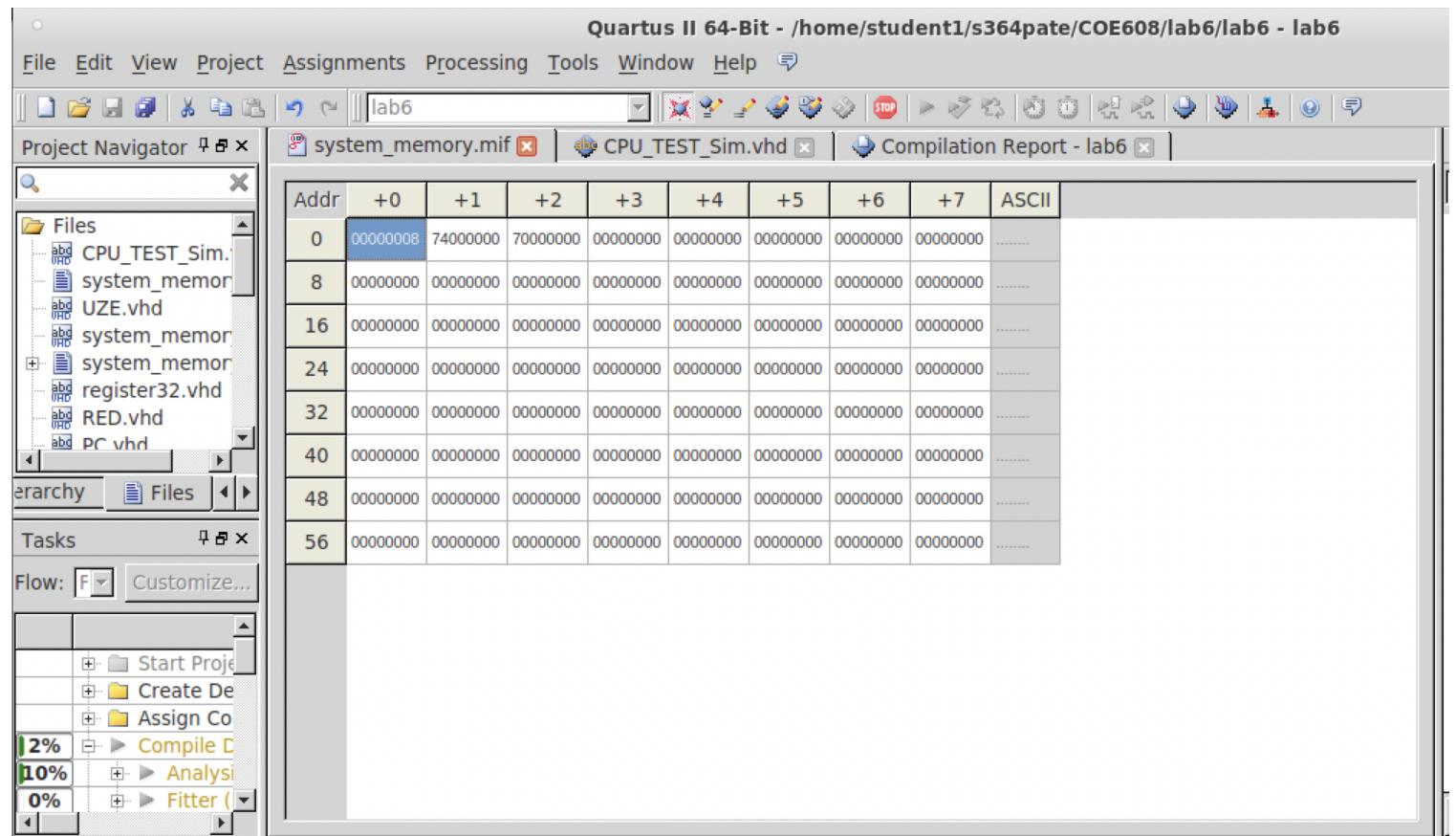
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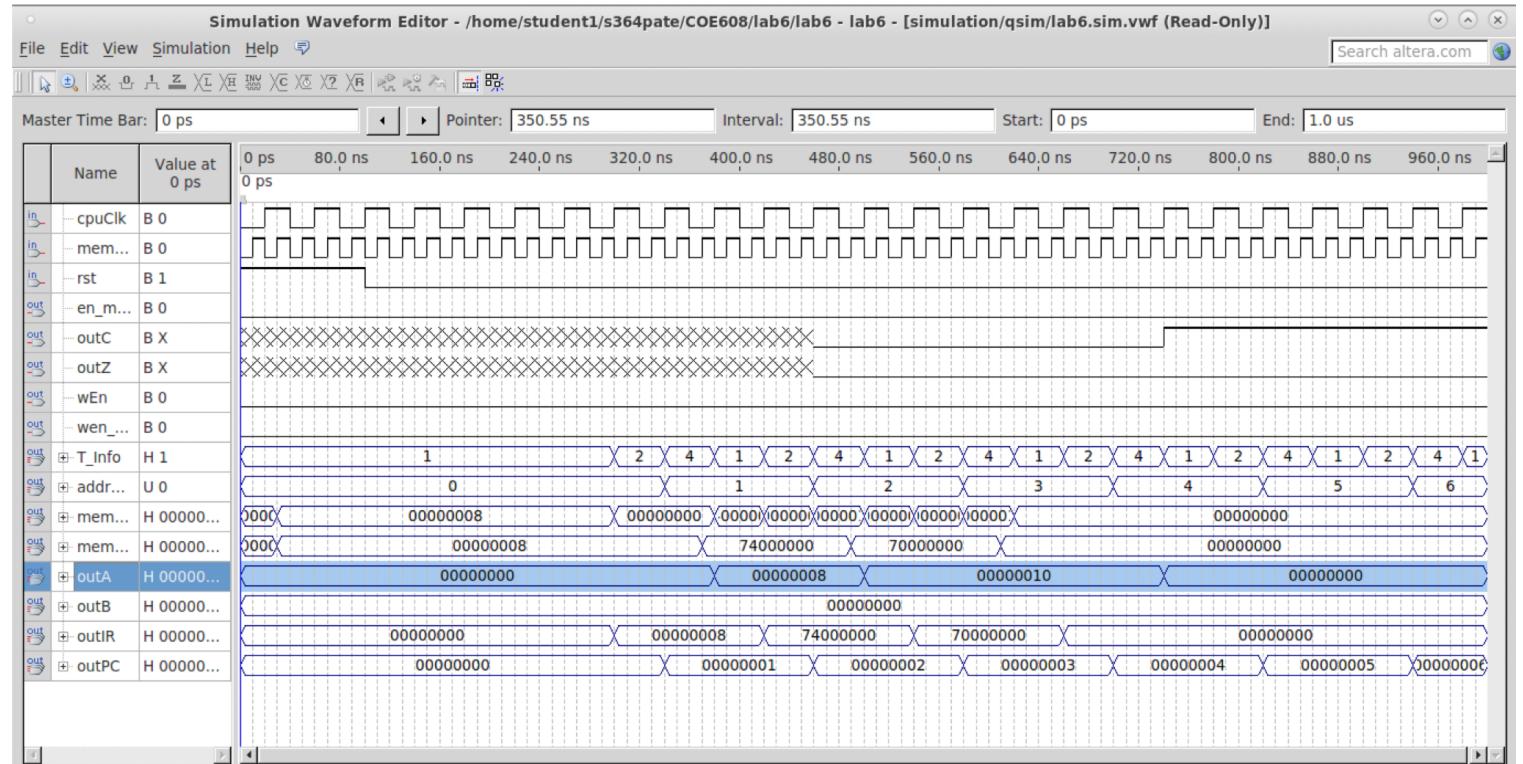
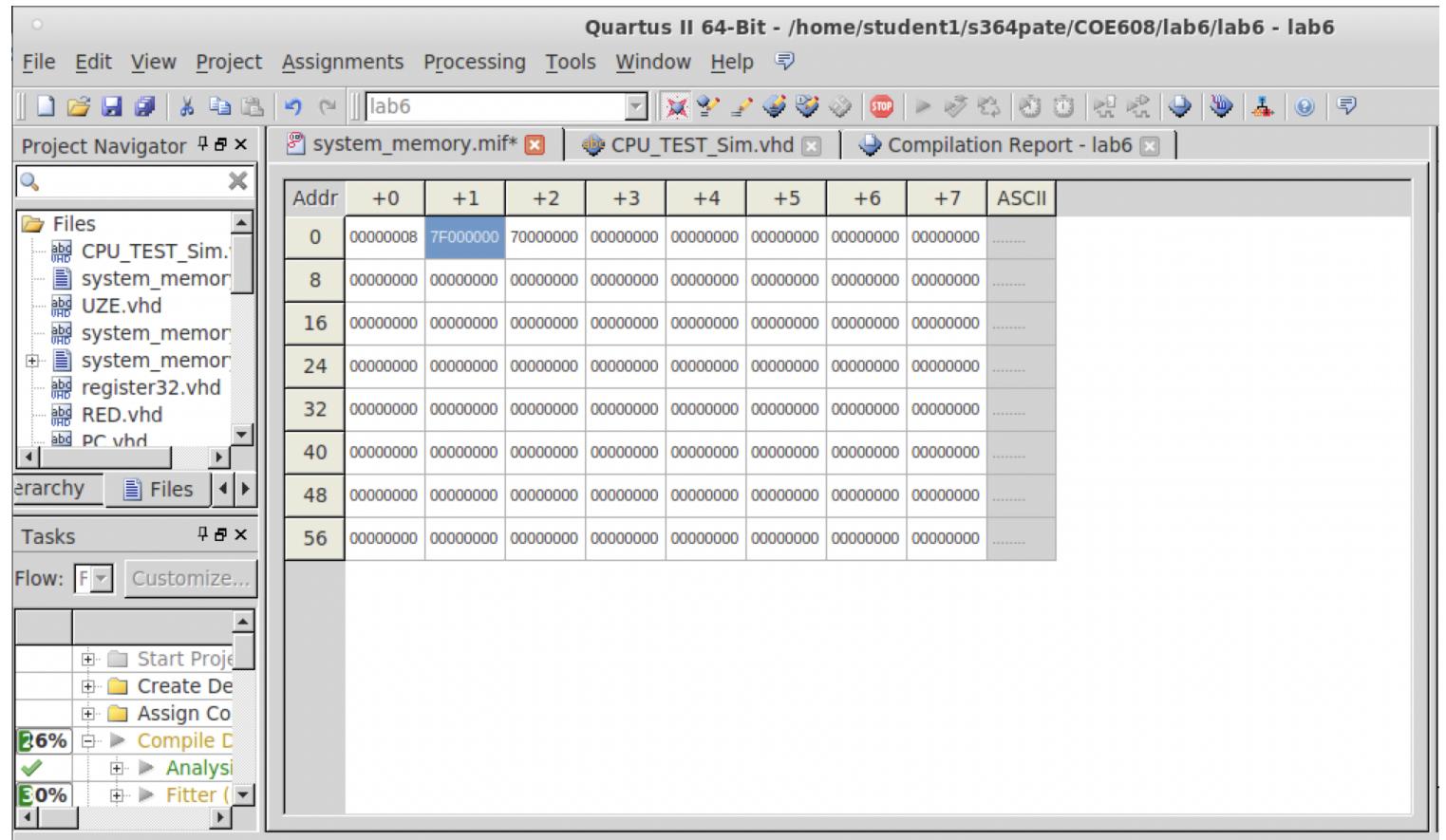
INCA



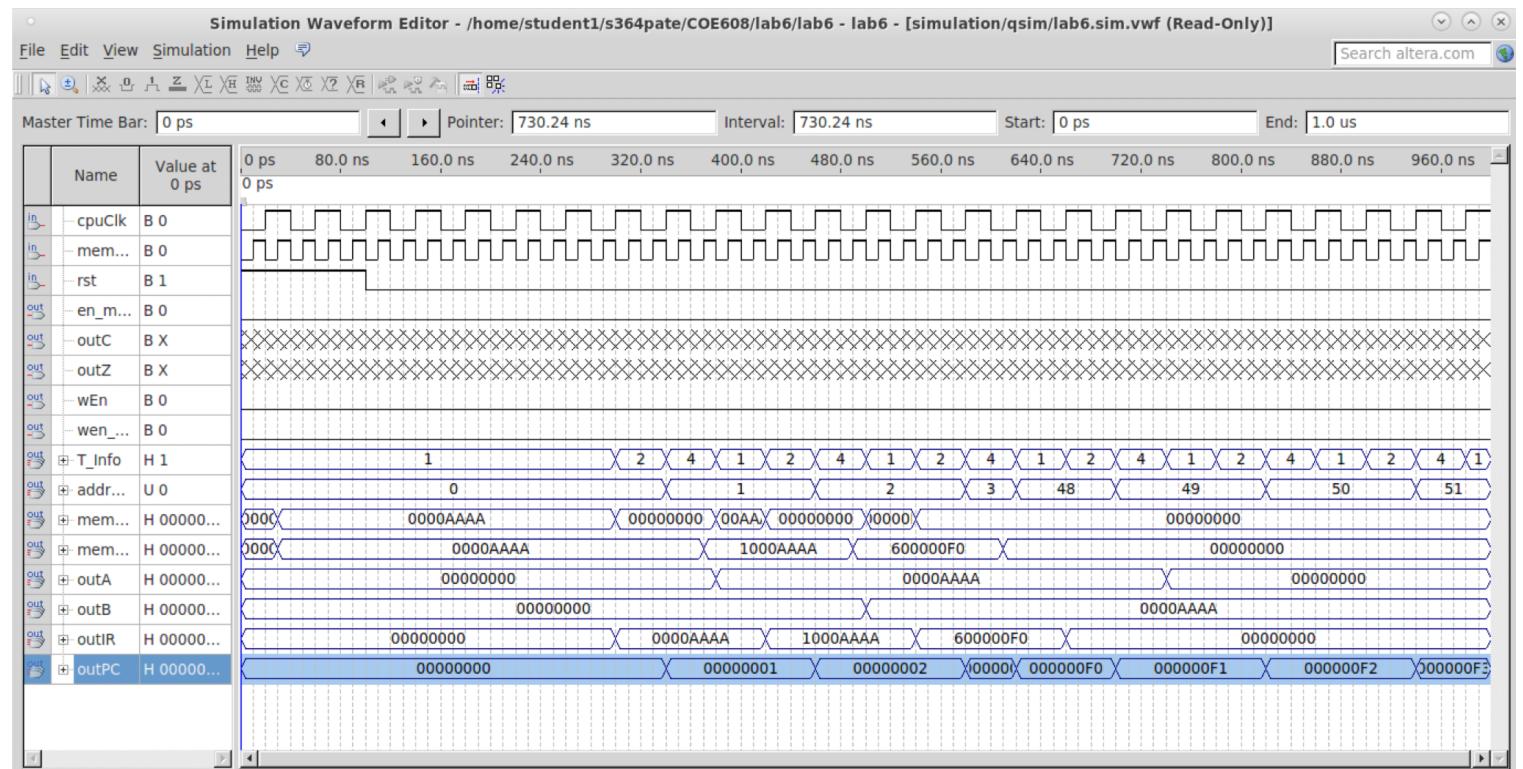
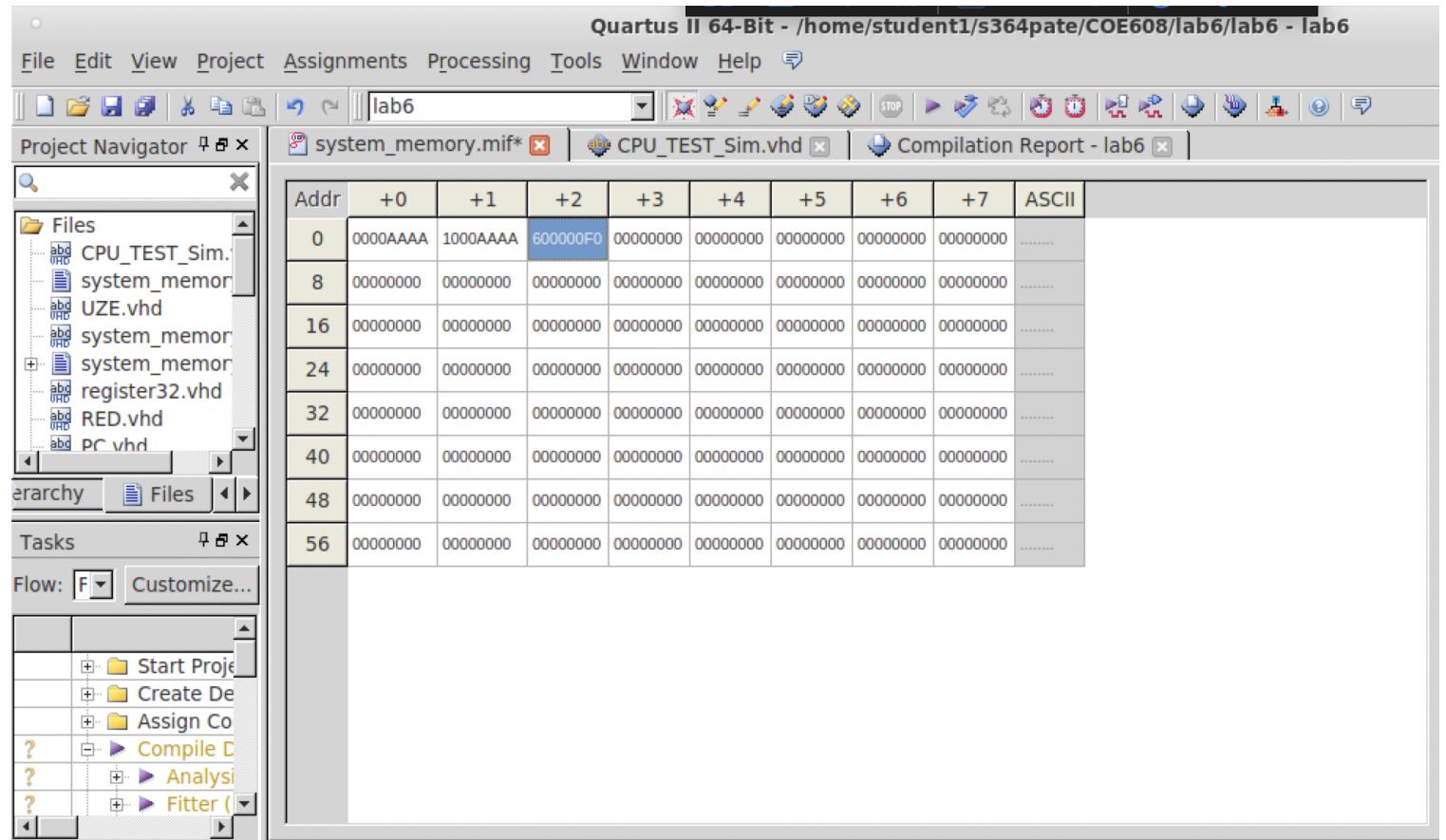
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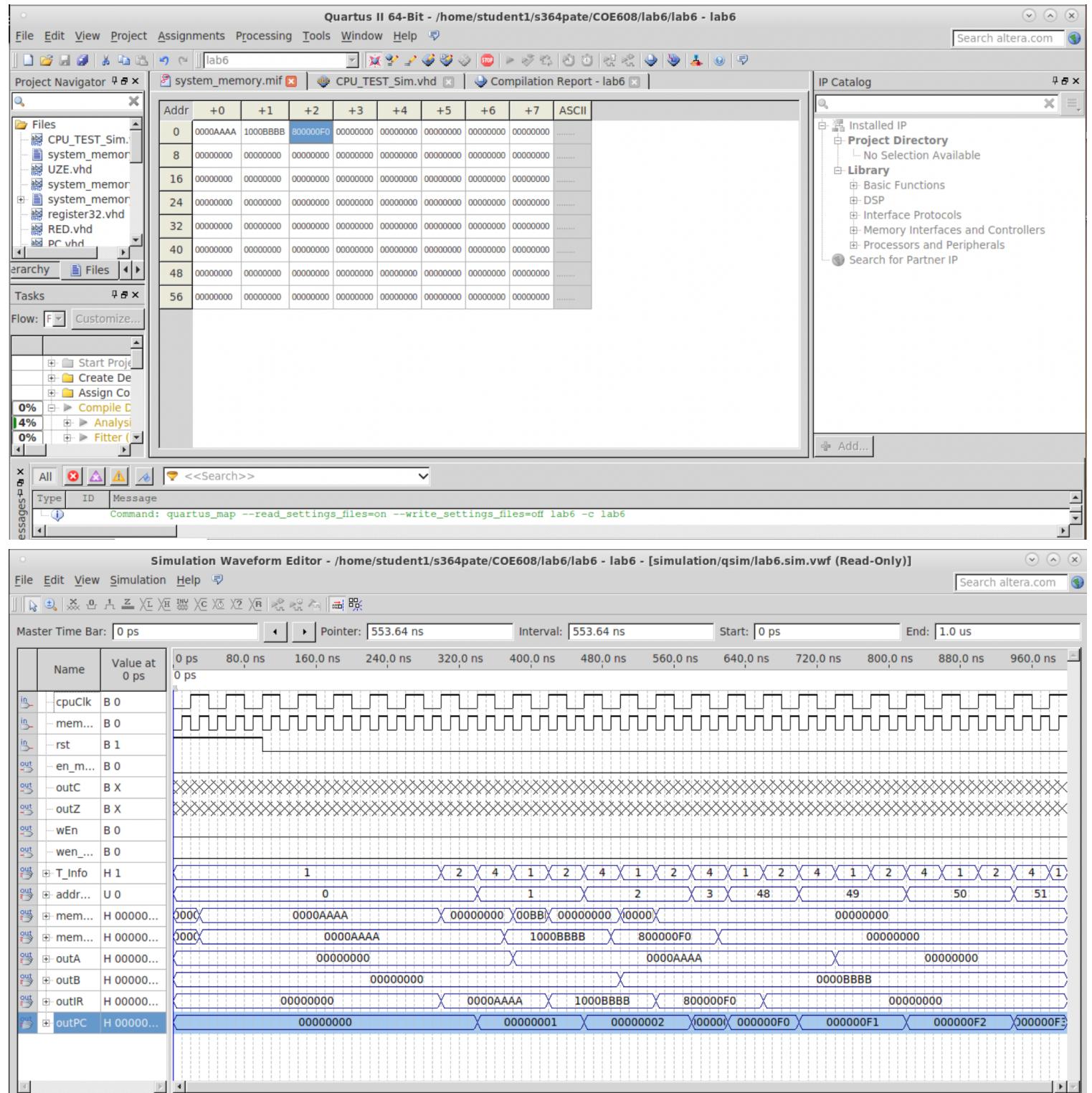
## ROR



BEQ



BNE



## **Conclusion**

In conclusion, this lab project aimed to implement a complete CPU system by combining the data path and control components designed in previous labs with a reset circuit. The reset circuit was designed to ensure proper functionality of the CPU by clearing the program counter and allowing the data surrounding the CPU to stabilize before operation begins.