



Course Number	COE608
Course Title	Computer Organization and Architecture
semester/year	Winter 2023
Instructor	Demetres Kostas
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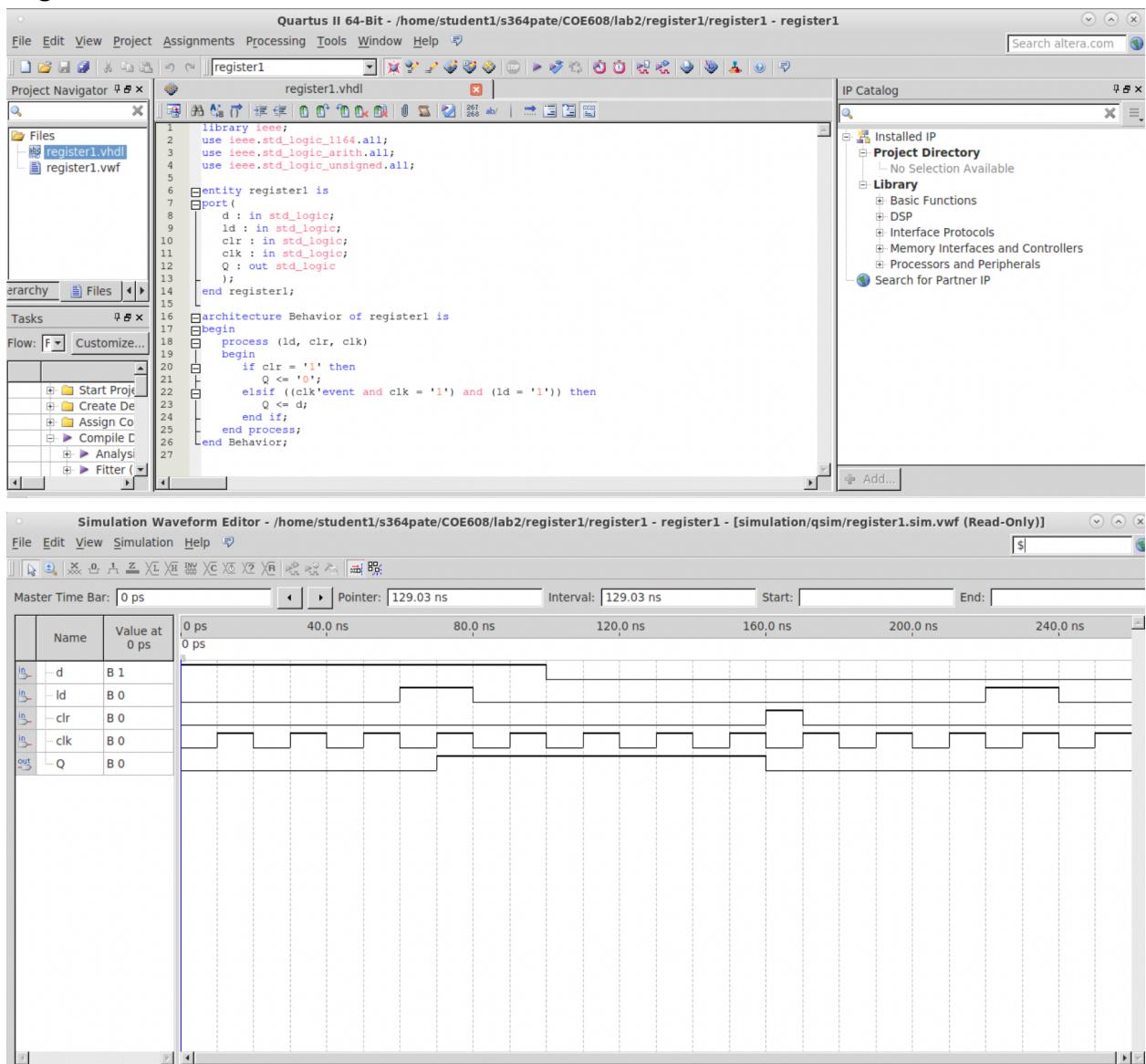
Lab report No.	2
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Report Title	Introduction to Quartus-II by a VHDL Based Design
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Section number	04
Submission date	
Due date	January 20 2023

Student Name	Student ID	Signature/Initials
Stuti Patel		SP

Register 1



Register 32

Quartus II 64-Bit - /home/student1/s364pate/COE608/lab2/register32/register32 - register32

File Edit View Project Assignments Processing Tools Window Help

Project Navigator

register32.vhd

register32.wvf

register32.vhd*

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_arith.all;
use ieee.std_logic_unsigned.all;

entity register32 is
port(
    d : in std_logic_vector(31 downto 0); --for 32 bits
    ld : in std_logic;
    clr : in std_logic;
    clk : in std_logic;
    Q : out std_logic_vector(31 downto 0)
);
end register32;

architecture behavior of register32 is
begin
process (ld, clr, clk)
begin
    if clr = '1' then
        Q <= (others => '0');
    elsif ((clk'event and clk = '1') and (ld = '1')) then
        Q <= d;
    end if;
end process;
end behavior;
```

Tasks

Flow: F Customize...

Start Project Create Design Assign Constraints Compile Design Analysis Filter

IP Catalog

Search altera.com

Simulation Waveform Editor - /home/student1/s364pate/COE608/lab2/register32/register32 - [simulation/qsim/register32.sim.wvf (Read-Only)]

File Edit View Simulation Help

Master Time Bar: 0 ps Pointer: 392.54 ns Interval: 392.54 ns Start: End:

	Name	Value at 0 ps
in	d	U 83574...
in	ld	B 0
in	clr	B 0
in	clk	B 0
out	Q	U 0

PC

Add.VHDI

Quartus II 64-Bit - /home/student1/s364pate/COE608/lab2/PC/pc - pc

File Edit View Project Assignments Processing Tools Window Help

Project Navigator

Files

- add.vhd
- mux2to1.vhd
- register32.vhd
- pc.vhd
- pc.vwf

Tasks

Flow: F Customize...

Start Project

Create De

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Compile C

Analysis

Fitter (

Messages

All <<Search>>

Type ID Message

System Processing

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_arith.all;
use ieee.std_logic_unsigned.all;

entity add is
port ( A : in std_logic_vector(31 downto 0);
       B : out std_logic_vector(31 downto 0)
      );
end add;

architecture Behavior of add is
begin
  B <= A + 4;
end Behavior;
```

Mux2to1.vhd

Browse and run installed applications Quartus II 64-Bit - /home/student1/s364pate/COE608/lab2/PC/pc - pc

File Edit View Project Assignments Processing Tools Window Help

Project Navigator add.vhd mux2to1.vhd

Files

- add.vhd
- mux2to1.vhd
- register32.vhd
- pc.vhd
- pc.vwf

Hierarchy Files

Tasks

Flow: F Customize...

Start Project Create Design Assign Constraints Compile Design Analysis Filter

Messages

All <>Search>>

Type ID Message

Simulation Waveform Editor - /home/student1/s364pate/COE608/lab2/PC/pc - pc - [simulation/qsim/pc.sim.vwf (Read-Only)]

File Edit View Simulation Help

Master Time Bar: 0 ps Pointer: 204.85 ns Interval: 204.85 ns Start: End:

Name	Value at 0 ps
clr	B 0
clk	B 0
ld	B 1
inc	B 1
d	U 5
q	U 0

0 ps 40.0 ns 80.0 ns 120.0 ns 160.0 ns 200.0 ns 240.0 ns 280.0 ns

0 4 8 12 16 5 0 5 9 5

PC.vhdl

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_arith.all;
use ieee.std_logic_unsigned.all;

entity pc is
port (
    clr      : in std_logic;
    clk      : in std_logic;
    ld       : in std_logic;
    inc      : in std_logic;
    d        : in std_logic_vector(31 downto 0);
    q        : out std_logic_vector(31 downto 0)
);
end pc;

architecture Behavior of pc is
component add
port (
    A        : in std_logic_vector (31 downto 0);
    B        : out std_logic_vector(31 downto 0)
);
component mux2tol
port (
    s         : in std_logic;
    w0,w1    : in std_logic_vector(31 downto 0);
    f         : out std_logic_vector(31 downto 0)
);
end component;
component register32
port(
    d        : in std_logic_vector(31 downto 0);
    ld      : in std_logic;
    clr    : in std_logic;
    clk    : in std_logic;
    Q      : out std_logic_vector(31 downto 0)
);
end component;

signal add_out      : std_logic_vector(31 downto 0);
signal mux_out      : std_logic_vector(31 downto 0);
signal q_out        : std_logic_vector(31 downto 0);

begin
    add0: add port map(q_out, add_out);
    mux0: mux2tol port map(inc, d, add_out, mux_out);
    reg0: register32 port map (mux_out, ld, clr, clk, q_out);
    q <= q_out;
end Behavior;
```