

Course Title:	Computer Organization and Architecture
Course Number:	COE608
Semester/Year (e.g.F2016)	Winter 2023

Instructor:	Demetres Kostas
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Assignment/Lab Number:	5
Assignment/Lab Title:	Data Memory Module

Submission Date:	Wednesday March 22 2023
Due Date:	Wednesday March 22 2023 3:00pm

Student LAST Name	Student FIRST Name	Student Number	Section	Signature*
Patel	Stuti		04	S.P

*By signing above you attest that you have contributed to this written lab report and confirm that all work you have contributed to this lab report is your own work. Any suspicion of copying or plagiarism in this work will result in an investigation of Academic Misconduct and may result in a "0" on the work, an "F" in the course, or possibly more severe penalties, as well as a Disciplinary Notice on your academic record under the Student Code of Academic Conduct, which can be found online at: <http://www.ryerson.ca/senate/current/pol60.pdf>

VHDL CODE

Control

Quartus II 64-Bit - /home/student1/s364pate/COE608/lab5/lab5 - lab5

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control.vhd*

```
library ieee;
use ieee.std_logic_1164.ALL;
entity control is
port(
    clk, mclk : in std_logic;
    enable : in std_logic;
    statusC, statusZ : in std_logic;
    INST : in std_logic_vector(31 downto 0);
    A_Mux, B_Mux : out std_logic;
    IM_MUX1, REG_Mux : out std_logic;
    IM_MUX2, DATA_Mux : out std_logic_vector(1 downto 0);
    ALU_op : out std_logic_vector(2 downto 0);
    inc_PC, ld_PC : out std_logic;
    clr_IR : out std_logic;
    ld_IR : out std_logic;
    clr_A, clr_B, clr_C, clr_Z : out std_logic;
    ld_A, ld_B, ld_C, ld_Z : out std_logic;
    T : out std_logic_vector(2 downto 0);
    wen, en : out std_logic
);
end control;
architecture description of control is
type statetype is (state_0, state_1, state_2);
signal present_state: statetype;
signal Instruction_sig: std_logic_vector(3 downto 0);
signal Instruction_sig2: std_logic_vector(7 downto 0);
begin
    Instruction_sig<= INST(31 downto 28);
    Instruction_sig2<= INST(31 downto 24);

    ----- OPERATION DECODER -----
process (present_state, INST, statusC, statusZ, enable, Instruction_sig, Instruction_sig2)
begin
    if enable = '1' then
        ...
    end if;
end process;
end;
```

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control.vhd*

```

35 BEGIN
36   if enable = '1' then
37     if present_state = state_0 then
38       DATA_Mux<="00";--Fetch Address of next instruction
39       clr_IR<='0';
40       ld_IR<='1';
41       ld_PC<='0';
42       inc_PC<='0';
43       clr_A<='0';
44       ld_A<='0';
45       ld_B<='0';
46       clr_B<='0';
47       clr_C<='0';
48       ld_C<='0';
49       clr_Z<='0';
50       ld_Z<='0';
51       en<='0';
52       wen<='0';
53
54   elsif present_state = state_1 then
55     clr_IR<='0'; --Increment PC Counter
56     ld_IR<='0';
57     ld_PC<='1';
58     inc_PC<='1';
59     clr_A<='0';
60     ld_A<='0';
61     ld_B<='0';
62     clr_B<='0';
63     clr_C<='0';
64     ld_C<='0';
65     clr_Z<='0';
66     ld_Z<='0';
67     en<='0';
68     wen<='0';
69
70   if Instruction_sig = "0010" then --STA
    
```

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control.vhd*

```

70   if Instruction_sig = "0010" then --STA
71     clr_IR<='0';
72     ld_IR<='0';
73     ld_PC<='1';
74     inc_PC<='1';
75     clr_A<='0';
76     ld_A<='0';
77     ld_B<='0';
78     clr_B<='0';
79     clr_C<='0';
80     ld_C<='0';
81     clr_Z<='0';
82     ld_Z<='0';
83     REG_Mux<='0';
84     DATA_Mux<="00";
85     en<='1';
86     wen<='1';
87
88   elsif Instruction_sig = "0011" then --STB
89     clr_IR<='0';
90     ld_Z<='0';
91     ld_IR<='0';
92     ld_PC<='1';
93     inc_PC<='1';
94     clr_A<='0';
95     ld_A<='0';
96     ld_B<='0';
97     clr_B<='0';
98     clr_C<='0';
99     ld_C<='0';
100    clr_Z<='0';
101    ld_Z<='0';
102    REG_Mux<='1';
103    DATA_Mux<="00";
104    en<='1';
105    wen<='1';
    
```

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control.vhd*

```

88      elsif Instruction_sig = "0011" then --STB
89          clr_IR<='0';
90          ld_Z<='0';
91          ld_IR<='0';
92          ld_PC<='1';
93          inc_PC<='1';
94          clr_A<='0';
95          ld_A<='0';
96          ld_B<='0';
97          clr_B<='0';
98          clr_C<='0';
99          ld_C<='0';
100         clr_Z<='0';
101         ld_Z<='0';
102         REG_Mux<='1';
103         DATA_Mux<="00";
104         en<='1';
105         wen<='1';
106     elsif Instruction_sig = "1001" then --LDA
107         clr_IR<='0';
108         ld_IR<='0';
109         ld_PC<='1';
110         inc_PC<='1';
111         clr_A<='0';
112         ld_A<='0';
113         ld_B<='0';
114         clr_B<='0';
115         clr_C<='0';
116         ld_C<='0';
117         clr_Z<='0';
118         ld_Z<='0';
119         A_Mux<='0';
120         DATA_Mux<="01";
121         en<='1';
122         wen<='0';
123     elsif Instruction_sig = "1010" then --LDB
           . . .

```

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control.vhd*

```

123      elsif Instruction_sig = "1010" then --LDB
124          clr_IR<='0';
125          ld_IR<='0';
126          ld_PC<='1';
127          inc_PC<='1';
128          clr_A<='0';
129          ld_A<='0';
130          ld_B<='1';
131          ld_B<='0';
132          clr_B<='0';
133          ld_C<='0';
134          clr_Z<='0';
135          ld_Z<='0';
136          B_Mux<='0';
137          DATA_Mux<="01";
138          en<='1';
139          wen<='0';
140      end if;
141
142      elsif present_state = state_2 then
143
144          if Instruction_sig = "0101" then --JUMP
145              clr_IR<='0';
146              ld_IR<='0';
147              ld_PC<='1';
148              inc_PC<='0';
149              clr_A<='0';
150              ld_A<='0';
151              ld_B<='0';
152              clr_B<='0';
153              clr_C<='0';
154              ld_C<='0';
155              clr_Z<='0';
156              ld_Z<='0';
157
158          elsif Instruction_sig = "0110" then --BEQ
           . . .

```

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control.vhd*

```

158    elsif Instruction_sig = "0110" then --BEQ
159        clr_IR<='0';
160        ld_IR<='0';
161        ld_PC<='1';
162        inc_PC<='0';
163        clr_A<='0';
164        ld_A<='0';
165        ld_B<='0';
166        clr_B<='0';
167        ld_C<='0';
168        clr_C<='0';
169        clr_Z<='0';
170        ld_Z<='0';
171
172    elsif Instruction_sig = "1000" then --BNE
173        clr_IR<='0';
174        ld_IR<='0';
175        ld_PC<='1';
176        inc_PC<='0';
177        clr_A<='0';
178        ld_A<='0';
179        ld_B<='0';
180        clr_B<='0';
181        clr_C<='0';
182        ld_C<='0';
183        clr_Z<='0';
184        ld_Z<='0';
185

```

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control.vhd*

```

185    elsif Instruction_sig = "1001" then --LDA
186        clr_IR<='0';
187        ld_IR<='0';
188        ld_PC<='1';
189        inc_PC<='0';
190        clr_A<='0';
191        ld_A<='1';
192        ld_B<='0';
193        clr_B<='0';
194        clr_C<='0';
195        ld_C<='0';
196        ld_Z<='0';
197        A_Mux<='0';
198        DATA_Mux<="01";
199        en<='1';
200        wen<='0';
201
202    elsif Instruction_sig = "1010" then --LDB
203        clr_IR<='0';
204        ld_IR<='0';
205        ld_PC<='1';
206        inc_PC<='0';
207        clr_A<='0';
208        ld_A<='0';
209        ld_B<='1';
210        clr_B<='0';
211        clr_C<='0';
212        ld_C<='0';
213        clr_Z<='0';
214        ld_Z<='0';
215        B_Mux<='0';
216        DATA_Mux<="01";
217        en<='1';
218        wen<='0';
219
220    elsif Instruction_sig = "0010" then --STA
221        ...

```

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control.vhd*

```

220      elsif Instruction_sig = "0010" then --STA
221          clr_IR<='0';
222          ld_IR<='0';
223          ld_PC<='0';
224          inc_PC<='0';
225          clr_A<='0';
226          ld_A<='0';
227          ld_B<='0';
228          clr_B<='0';
229          ld_C<='0';
230          clr_Z<='0';
231          ld_Z<='0';
232          REG_Mux<='0';
233          DATA_Mux<="00";
234          en<='1';
235          wen<='1';
236
237      elsif Instruction_sig = "0011" then --STB
238          clr_IR<='0';
239          ld_IR<='0';
240          ld_PC<='0';
241          inc_PC<='0';
242          clr_A<='0';
243          ld_A<='0';
244          ld_B<='0';
245          ld_B<='0';
246          clr_B<='0';
247          clr_C<='0';
248          ld_C<='0';
249          clr_Z<='0';
250          ld_Z<='0';
251          REG_Mux<='1';
252          DATA_Mux<="00";
253          en<='1';
254          wen<='1';
255      elsif Instruction_sig = "0000" then --LDAI

```

Ln 255 Col 18 VHDL File

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control.vhd*

```

254          wen<='1';
255      elsif Instruction_sig = "0000" then --LDAI
256          clr_IR<='0';
257          ld_IR<='0';
258          ld_PC<='0';
259          inc_PC<='0';
260          clr_A<='0';
261          ld_A<='1';
262          ld_B<='0';
263          clr_B<='0';
264          clr_C<='0';
265          ld_C<='0';
266          clr_Z<='0';
267          ld_Z<='0';
268          A_Mux<='1';
269      elsif Instruction_sig = "0001" then --LDBI
270          clr_IR<='0';
271          ld_IR<='0';
272          ld_PC<='0';
273          inc_PC<='0';
274          clr_A<='0';
275          ld_A<='0';
276          ld_B<='1';
277          clr_B<='0';
278          clr_C<='0';
279          ld_C<='0';
280          clr_Z<='0';
281          ld_Z<='0';
282          B_Mux<='1';
283      elsif Instruction_sig = "0100" then --LUI
284          clr_IR<='0';
285          ld_IR<='0';
286          ld_PC<='0';
287          inc_PC<='0';
288          clr_A<='0';
289          ld_A<='1';

```

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control.vhd*

```

284    clr_IR<='0';
285    ld_IR<='0';
286    ld_PC<='0';
287    inc_PC<='0';
288    clr_A<='0';
289    ld_A<='1';
290    ld_B<='0';
291    clr_B<='1';
292    clr_C<='0';
293    ld_C<='0';
294    clr_Z<='0';
295    ld_Z<='0';
296    ALU_op<="001";
297    A_Mux<='0';
298    DATA_Mux<="10";
299    IM_MUX1<='1';
300  elsif Instruction_sig2 = "01111001" then --ANDI
301    clr_IR<='0';
302    ld_IR<='0';
303    ld_PC<='0';
304    inc_PC<='0';
305    clr_A<='0';
306    ld_A<='1';
307    ld_B<='0';
308    clr_B<='0';
309    clr_C<='0';
310    ld_C<='1';
311    clr_Z<='0';
312    ld_Z<='1';
313    ALU_op<="000";
314    A_Mux<='0';
315    DATA_Mux<="10";
316    IM_MUX1<='0';
317    IM_MUX2<="01";
318  elsif Instruction_sig2 = "01111110" then --DECA
319    clr_IR<='0';
320    ld_IR<='0';
321    ld_PC<='0';
322    inc_PC<='0';
323    clr_A<='0';
324    ld_A<='1';
325    ld_B<='0';
326    clr_B<='0';
327    clr_C<='0';
328    ld_C<='1';
329    clr_Z<='0';
330    ld_Z<='1';
331    ALU_op<="110";
332    A_Mux<='0';
333    DATA_Mux<="10";
334    IM_MUX1<='0';
335    IM_MUX2<="10";
336  elsif Instruction_sig2 = "01111110" then --DECA
337    clr_IR<='0';
338    ld_IR<='0';
339    ld_PC<='0';
340    inc_PC<='0';
341    clr_A<='0';
342    ld_A<='1';
343    ld_B<='0';
344    clr_B<='0';
345    clr_C<='0';
346    ld_C<='1';
347    clr_Z<='0';
348    ld_Z<='1';
349    ALU_op<="010";
350    A_Mux<='0';
351    DATA_Mux<="10";
352    IM_MUX1<='0';
353    IM_MUX2<="00";
354  end if;

```

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control.vhd*

```

318  elsif Instruction_sig2 = "01111110" then --DECA
319    clr_IR<='0';
320    ld_IR<='0';
321    ld_PC<='0';
322    inc_PC<='0';
323    clr_A<='0';
324    ld_A<='1';
325    ld_B<='0';
326    clr_B<='0';
327    clr_C<='0';
328    ld_C<='1';
329    clr_Z<='0';
330    ld_Z<='1';
331    ALU_op<="110";
332    A_Mux<='0';
333    DATA_Mux<="10";
334    IM_MUX1<='0';
335    IM_MUX2<="10";
336  elsif Instruction_sig2 = "01110000" then --ADD
337    clr_IR<='0';
338    ld_IR<='0';
339    ld_PC<='0';
340    inc_PC<='0';
341    clr_A<='0';
342    ld_A<='1';
343    ld_B<='0';
344    clr_B<='0';
345    clr_C<='0';
346    ld_C<='1';
347    clr_Z<='0';
348    ld_Z<='1';
349    ALU_op<="010";
350    A_Mux<='0';
351    DATA_Mux<="10";
352    IM_MUX1<='0';
353    IM_MUX2<="00";
354  end if;

```

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control.vhd*

```

354    elsif Instruction_sig2 = "01110010" then --SUB
355        clr_IR<='0';
356        ld_IR<='0';
357        ld_PC<='0';
358        inc_PC<='0';
359        clr_A<='0';
360        ld_A<='1';
361        ld_B<='0';
362        clr_B<='0';
363        clr_C<='0';
364        ld_C<='1';
365        clr_Z<='0';
366        ld_Z<='1';
367        ALU_op<="110";
368        A_Mux<='0';
369        DATA_Mux<="10";
370        IM_MUX1<='0';
371        IM_MUX2<="00";
372    elsif Instruction_sig2 = "01110011" then --INCA
373        clr_IR<='0';
374        ld_IR<='0';
375        ld_PC<='0';
376        inc_PC<='0';
377        clr_A<='0';
378        ld_A<='1';
379        ld_B<='0';
380        clr_B<='0';
381        clr_C<='0';
382        ld_C<='1';
383        clr_Z<='0';
384        ld_Z<='1';
385        ALU_op<="010";
386        A_Mux<='0';
387        DATA_Mux<="10";
388        IM_MUX1<='0';
389        IM_MUX2<="10";

```

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control.vhd*

```

390    elsif Instruction_sig2 = "01111011" then --AND
391        clr_IR<='0';
392        ld_IR<='0';
393        ld_PC<='0';
394        inc_PC<='0';
395        clr_A<='0';
396        ld_A<='1';
397        ld_B<='0';
398        clr_B<='0';
399        clr_C<='0';
400        ld_C<='1';
401        clr_Z<='0';
402        ld_Z<='1';
403        ALU_op<="000";
404        A_Mux<='0';
405        DATA_Mux<="10";
406        IM_MUX1<='0';
407        IM_MUX2<="00";
408    elsif Instruction_sig2 = "01110001" then --ADDI
409        clr_IR<='0';
410        ld_IR<='0';
411        ld_PC<='0';
412        inc_PC<='0';
413        clr_A<='0';
414        ld_A<='1';
415        ld_B<='0';
416        clr_B<='0';
417        clr_C<='0';
418        ld_C<='1';
419        clr_Z<='0';
420        ld_Z<='1';
421        ALU_op<="010";
422        A_Mux<='0';
423        DATA_Mux<="10";
424        IM_MUX1<='0';
425        IM_MUX2<="01";

```

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control.vhd*

```

426    elsif Instruction_sig2 = "01111101" then --ORT
427        clr_IR<='0';
428        ld_IR<='0';
429        ld_PC<='0';
430        inc_PC<='0';
431        clr_A<='0';
432        ld_A<='1';
433        ld_B<='0';
434        clr_B<='0';
435        clr_C<='0';
436        ld_C<='1';
437        clr_Z<='0';
438        ld_Z<='1';
439        ALU_op<="001";
440        A_Mux<='0';
441        DATA_Mux<="10";
442        IM_MUX1<='0';
443        IM_MUX2<="01";
444    elsif Instruction_sig2 = "01110100" then --ROL
445        clr_IR<='0';
446        ld_IR<='0';
447        ld_PC<='0';
448        inc_PC<='0';
449        clr_A<='0';
450        ld_A<='1';
451        ld_B<='0';
452        clr_B<='0';
453        clr_C<='0';
454        ld_C<='1';
455        clr_Z<='0';
456        ld_Z<='1';
457        ALU_op<="100";
458        A_Mux<='0';
459        DATA_Mux<="10";
460        IM_MUX1<='0';
461    elsif Instruction_sig2 = "01111111" then --ROR
        ...

```

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control.vhd*

```

461    elsif Instruction_sig2 = "01111111" then --ROR
462        clr_IR<='0';
463        ld_IR<='0';
464        ld_PC<='0';
465        inc_PC<='0';
466        clr_A<='0';
467        ld_A<='1';
468        ld_B<='0';
469        clr_B<='0';
470        clr_C<='0';
471        ld_C<='1';
472        clr_Z<='0';
473        ld_Z<='1';
474        ALU_op<="101";
475        A_Mux<='0';
476        DATA_Mux<="10";
477        IM_MUX1<='0';
478    elsif Instruction_sig2 = "01110101" then --CLR_A
479        clr_IR<='0';
480        ld_IR<='0';
481        ld_PC<='0';
482        inc_PC<='0';
483        clr_A<='1';
484        ld_A<='0';
485        ld_B<='0';
486        clr_B<='0';
487        clr_C<='0';
488        ld_C<='0';
489        clr_Z<='0';
490        ld_Z<='0';
491    elsif Instruction_sig2 = "01110110" then --CLR_B
492        clr_IR<='0';
493        ld_IR<='0';
494        ld_PC<='0';
495        inc_PC<='0';
496        clr_A<='0';
        ...

```

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control.vhd*

```
491 elsif Instruction_sig2 = "01110110" then --CLR_B
492     clr_IR<='0';
493     ld_IR<='0';
494     ld_PC<='0';
495     inc_PC<='0';
496     clr_A<='0';
497     ld_A<='0';
498     ld_B<='0';
499     clr_B<='1';
500     clr_C<='0';
501     ld_C<='0';
502     clr_Z<='0';
503     ld_Z<='0';
504 elsif Instruction_sig2 = "01110111" then --CLR_C
505     clr_IR<='0';
506     ld_IR<='0';
507     ld_PC<='0';
508     inc_PC<='0';
509     clr_A<='0';
510     ld_A<='0';
511     ld_B<='0';
512     clr_B<='0';
513     clr_C<='1';
514     ld_C<='0';
515     clr_Z<='0';
516     ld_Z<='0';
517 elsif Instruction_sig2 = "01111000" then --CLR_Z
518     clr_IR<='0';
519     ld_IR<='0';
520     ld_PC<='0';
521     inc_PC<='0';
522     clr_A<='0';
523     ld_A<='0';
524     ld_B<='0';
525     clr_B<='0';
526     clr_C<='0';
527     ld_Z<='0';
528 end if;
```

Quartus II 64-Bit - /home/student1/s364pate/COE608/lab5/lab5 - lab5

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control.vhd*

```
517    elsif Instruction_sig2 = "01111000" then --CLR_Z
518        clr_IR<='0';
519        ld_IR<='0';
520        ld_PC<='0';
521        inc_PC<='0';
522        clr_A<='0';
523        ld_A<='0';
524        ld_B<='0';
525        clr_B<='0';
526        clr_C<='0';
527        ld_C<='0';
528        clr_Z<='1';
529        ld_Z<='0';
530    elsif Instruction_sig2 = "01111010" then --TSTZ
531        if(statusZ='1')then
532            clr_IR<='0'; --INCREMENT PC COUNTER
533            ld_IR<='0';
534            ld_PC<='1';
535            inc_PC<='1';
536            clr_A<='0';
537            ld_A<='0';
538            ld_B<='0';
539            clr_B<='0';
540            clr_C<='0';
541            ld_C<='0';
542            clr_Z<='0';
543            ld_Z<='0';
544        end if;
545    elsif Instruction_sig2 = "01111100" then --TSTC
546        if(statusC='1')then
547            clr_IR<='0'; --INCREMENT PC COUNTER
548            ld_IR<='0';
549            ld_PC<='1';
550            inc_PC<='1';
551            clr_A<='0';
552            ld_A<='0';
553            ld_B<='0';
554            clr_B<='0';
555            clr_C<='0';
556            ld_C<='0';
557            clr_Z<='0';
558            ld_Z<='0';
559        end if;
560    end if;
```

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control.vhd*

```

545      elsif Instruction_sig2 = "01111100" then --TSTC
546          if(statusC='1')then
547              clr_IR<='0'; --INCREMENT PC COUNTER
548              ld_IR<='0';
549              ld_PC<='1';
550              inc_PC<='1';
551              clr_A<='0';
552              ld_A<='0';
553              ld_B<='0';
554              clr_B<='0';
555              clr_C<='0';
556              ld_C<='0';
557              clr_Z<='0';
558              ld_Z<='0';
559      end if;--For state 2 Ops
560      end if;
561  end if; --For Enable
562 end if;
563 END process;
564 -----STATE MACHINE-----
565 PROCESS (clk, enable)
566 begin
567     if enable = '1' then
568         if rising_edge (clk) then
569             if present_state = state_0 then present_state <= state_1;
570             elsif present_state = state_1 then present_state <= state_2;
571             else present_state <= state_0;
572             end if;
573         end if;
574     else present_state <= state_0;
575     end if;
576 END process;
577
578 WITH present_state select
579     T <= "001" when state_0,
580     "010" when state_1,
581     "100" when state_2;

```

Quartus II 64-Bit - /home/student1/s364pate/COE608/lab6/lab6 - lab6

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Project Navigator

control_new.vhd

CPU_TEST_Sim.vhd

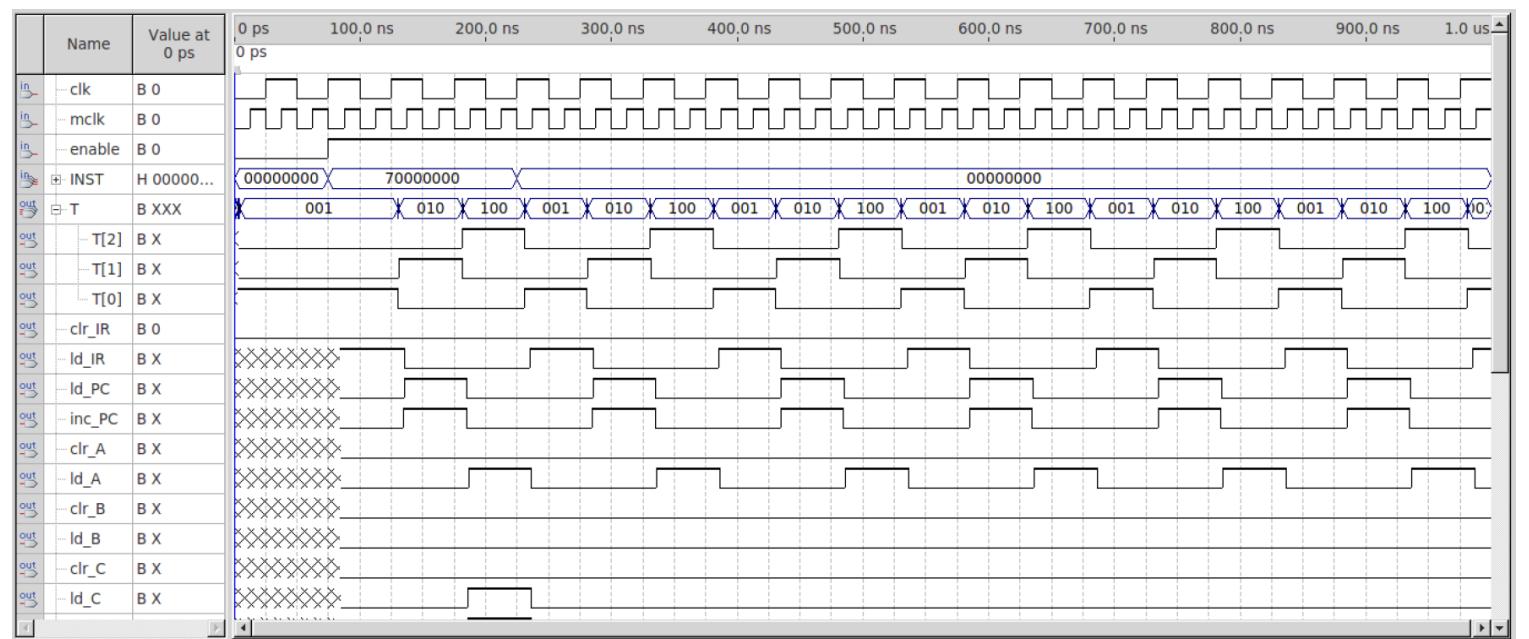
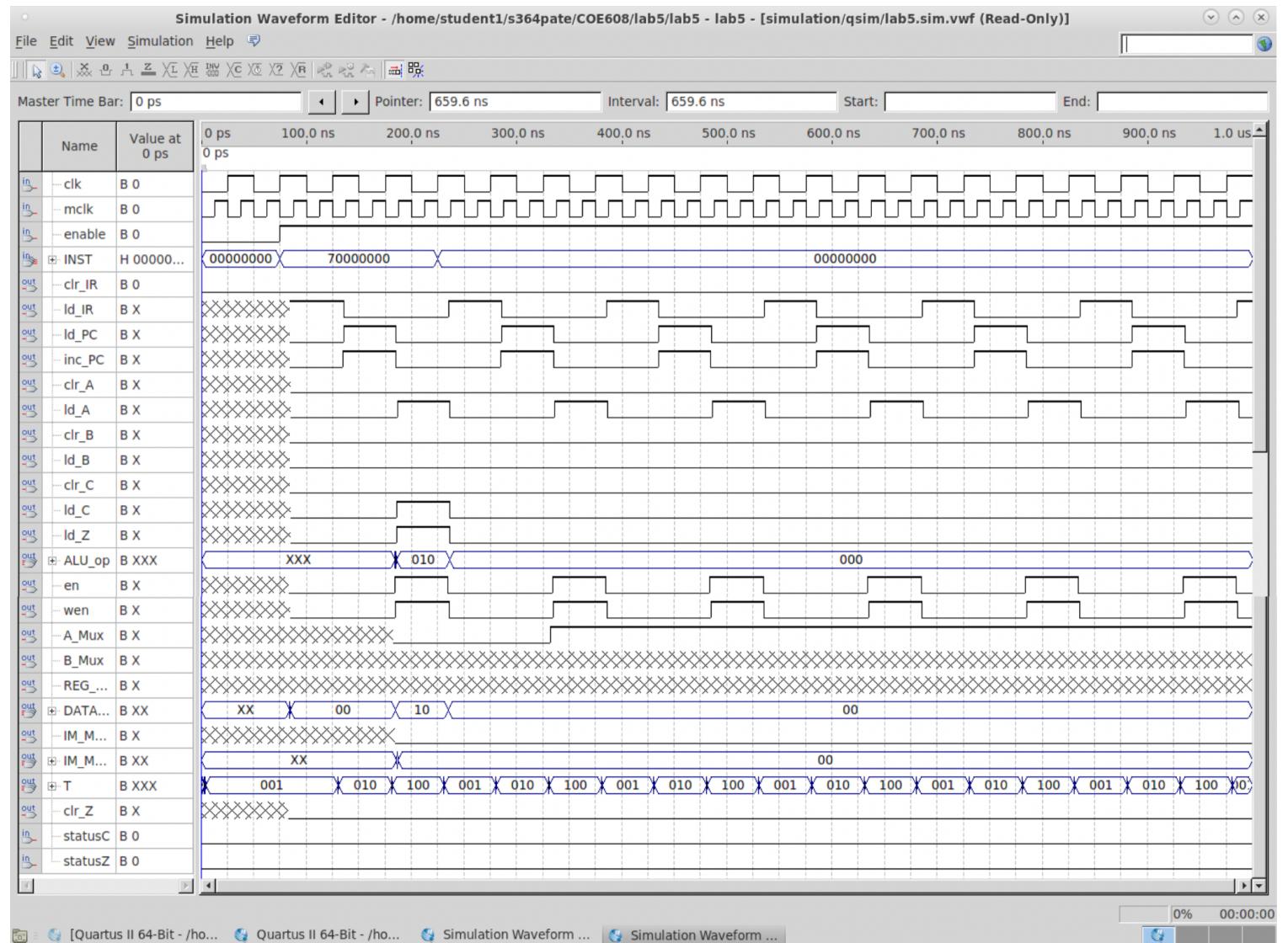
```

556         ld_C<='0';
557         clr_Z<='0';
558         ld_Z<='0';
559     end if;--For state 2 Ops
560     end if;
561     end if; --For Enable
562 end if;
563 END process;
564 -----STATE MACHINE-----
565 PROCESS (clk, enable)
566 begin
567     if enable = '1' then
568         if rising_edge (clk) then
569             if present_state = state_0 then present_state <= state_1;
570             elsif present_state = state_1 then present_state <= state_2;
571             else present_state <= state_0;
572             end if;
573         end if;
574     else present_state <= state_0;
575     end if;
576 END process;
577
578 WITH present_state select
579     T <= "001" when state_0, -- Fetch address of the next instruction
580     "010" when state_1, -- Increment PC Counter
581     "100" when state_2, -- Decode and Execute
582     "001" when others; -- N/A you will always have either state_0, state_1 or state_2
583 END description;

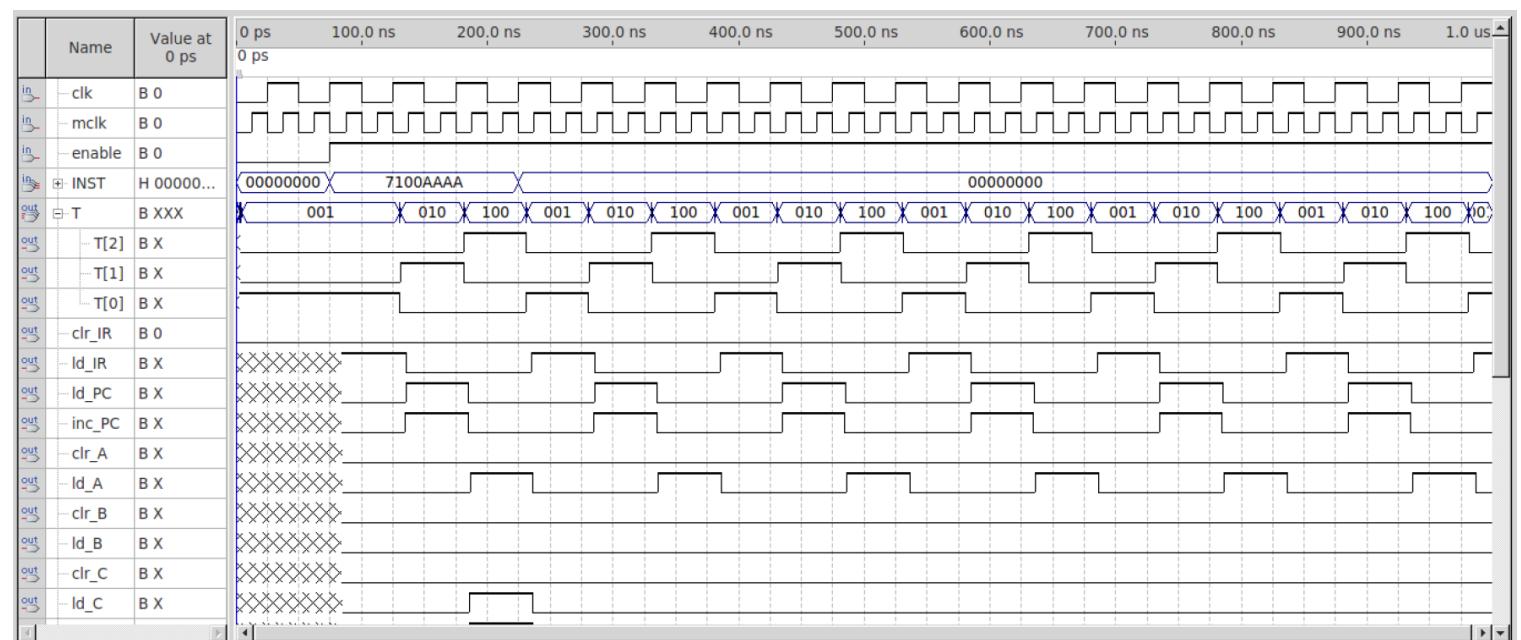
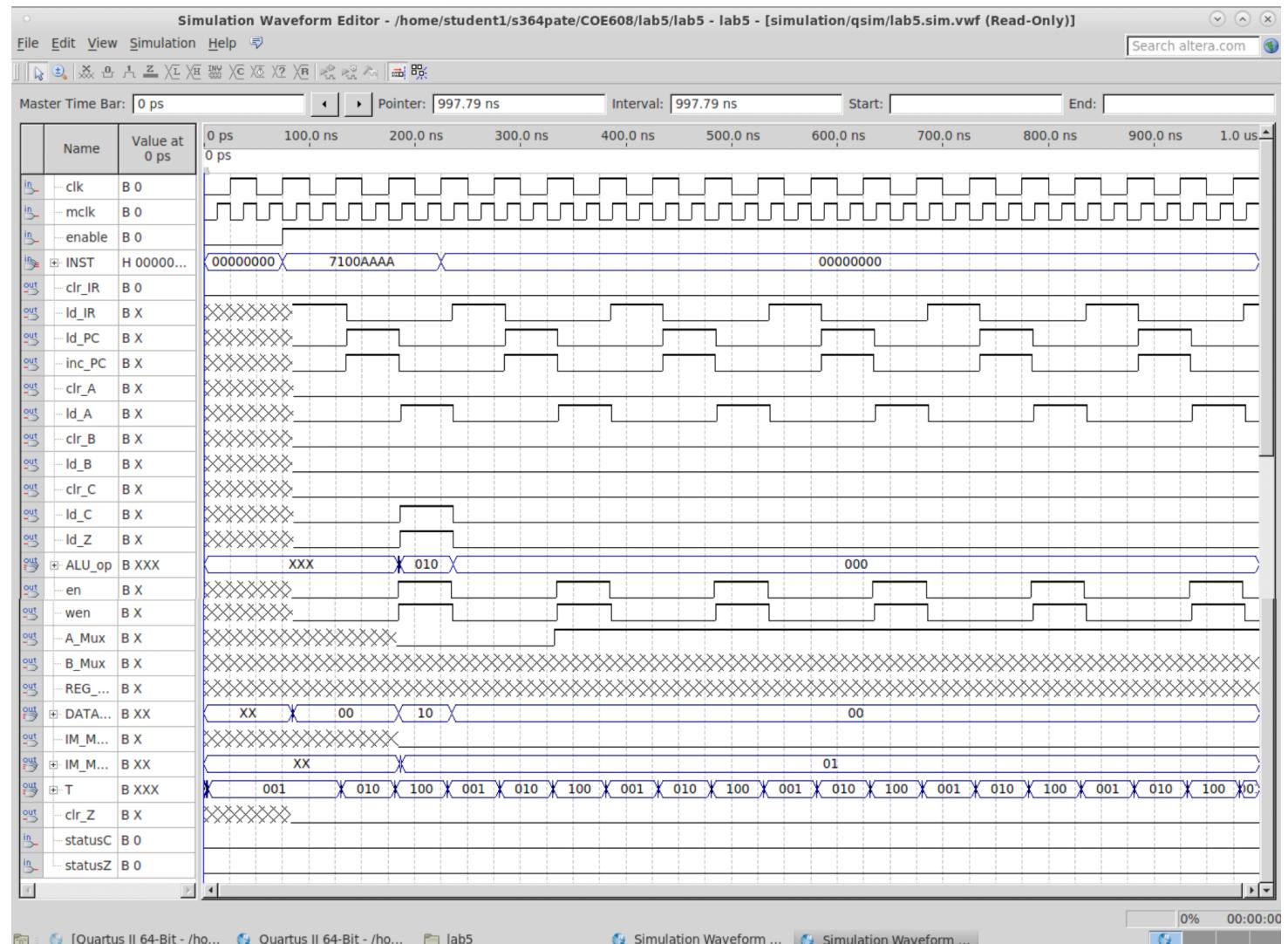
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Functional Simulations

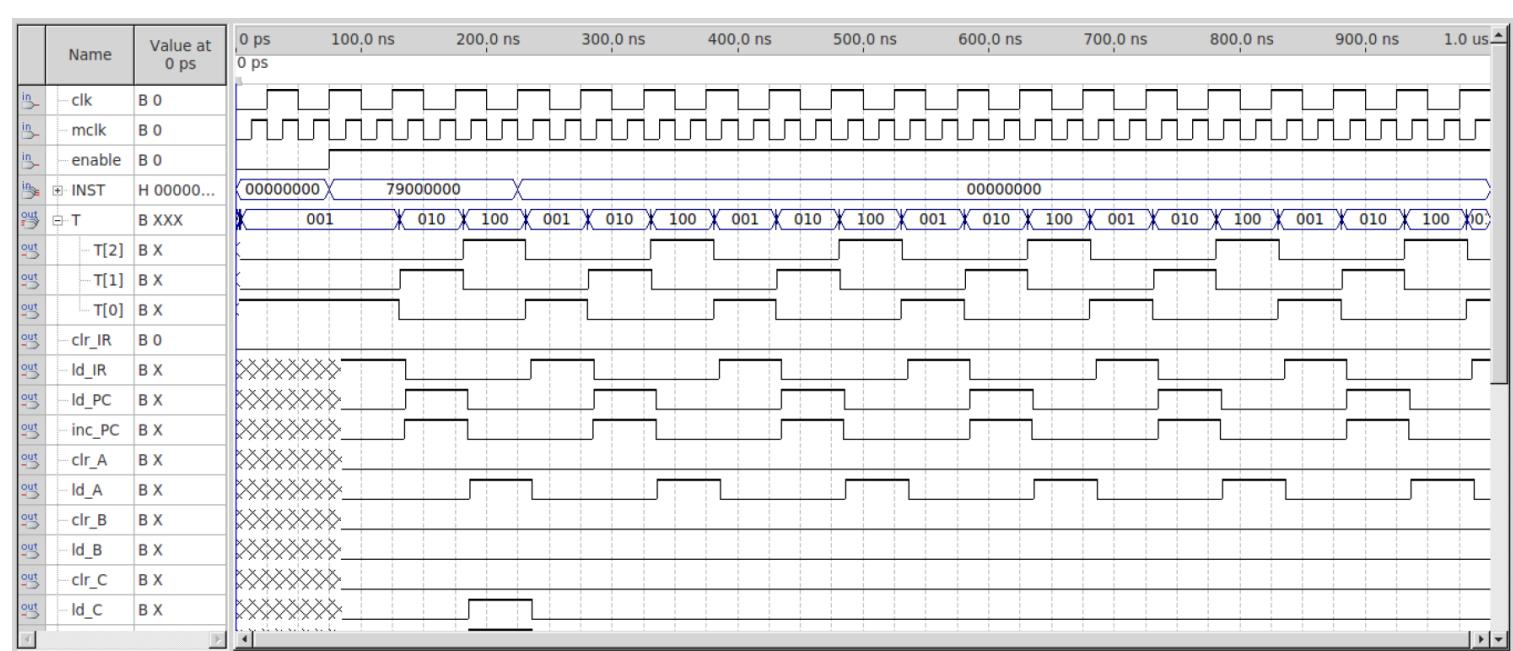
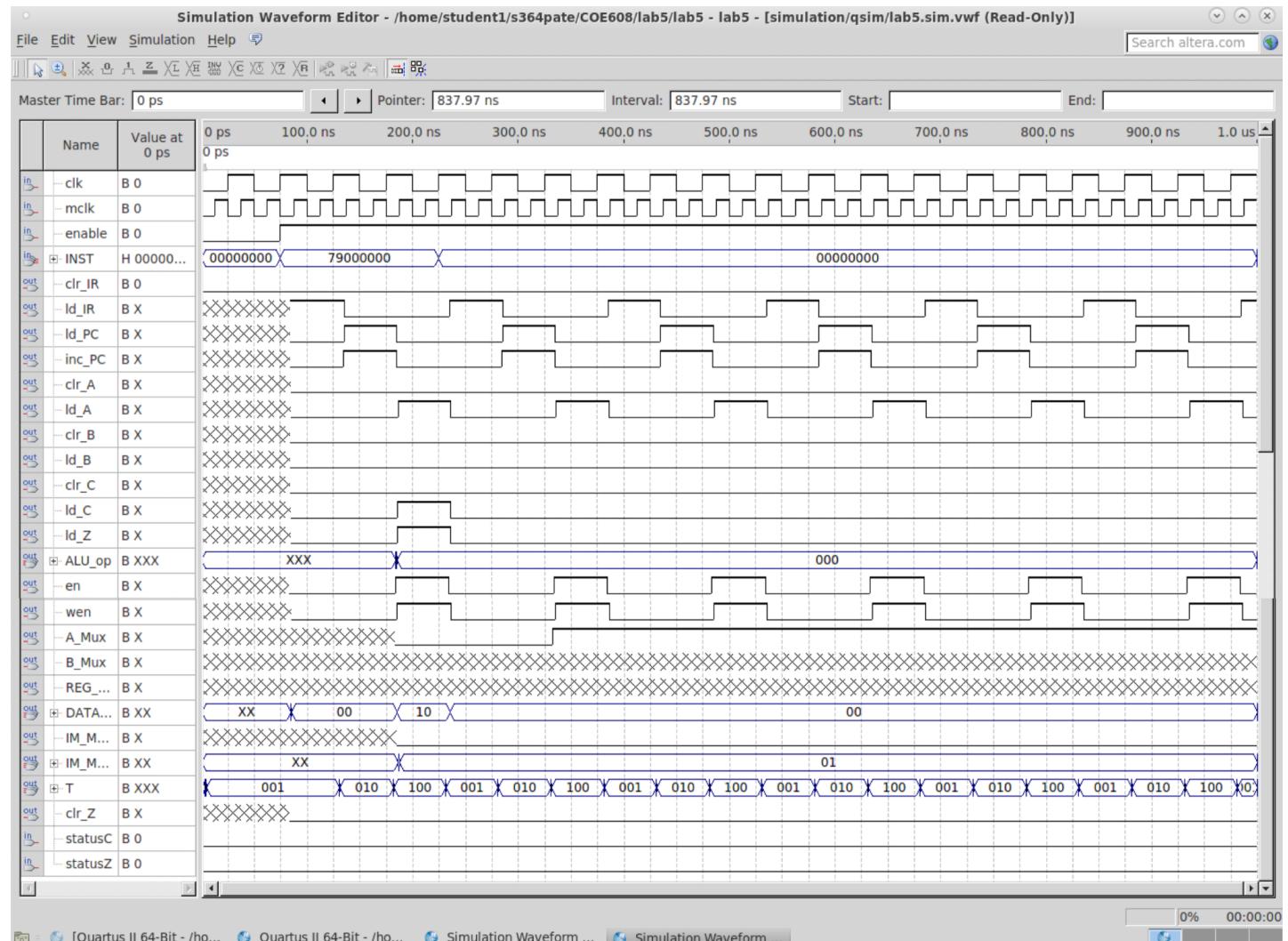
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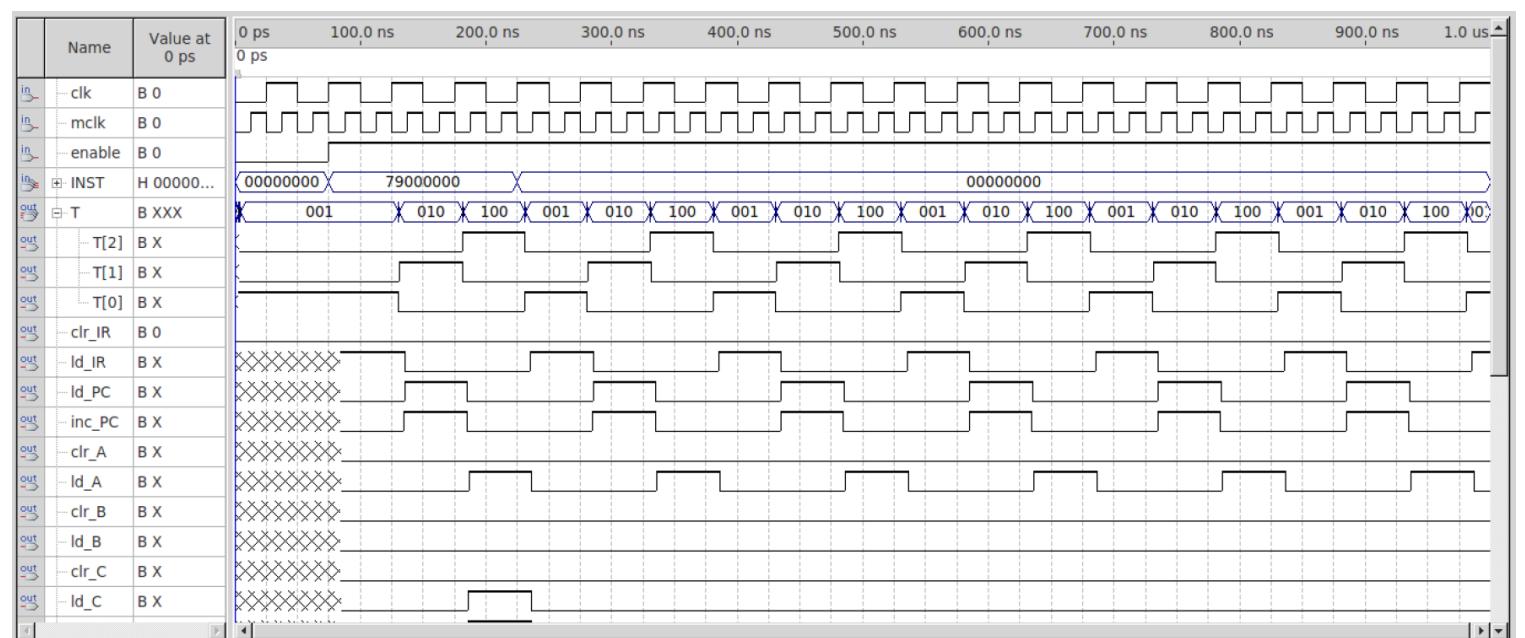
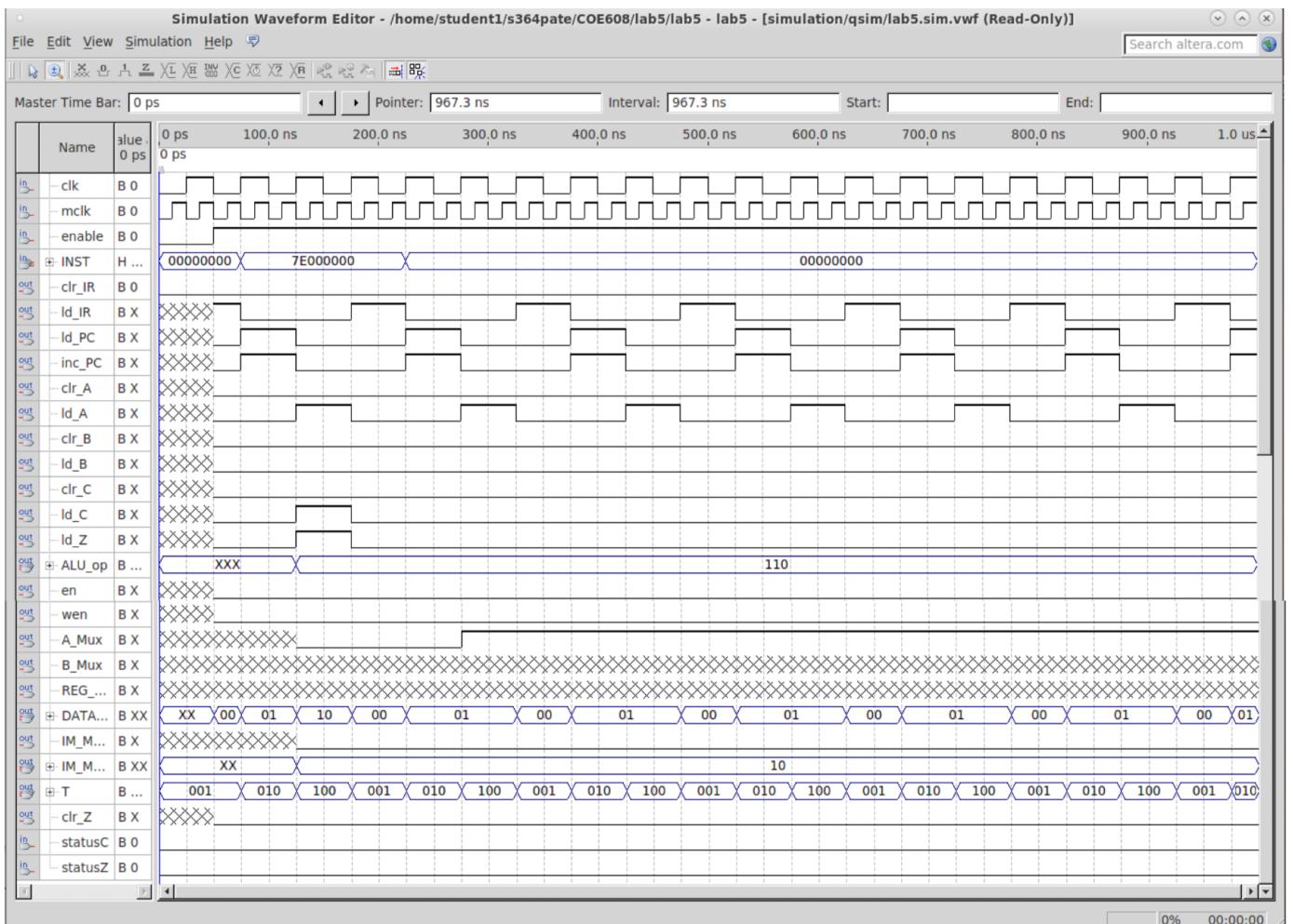
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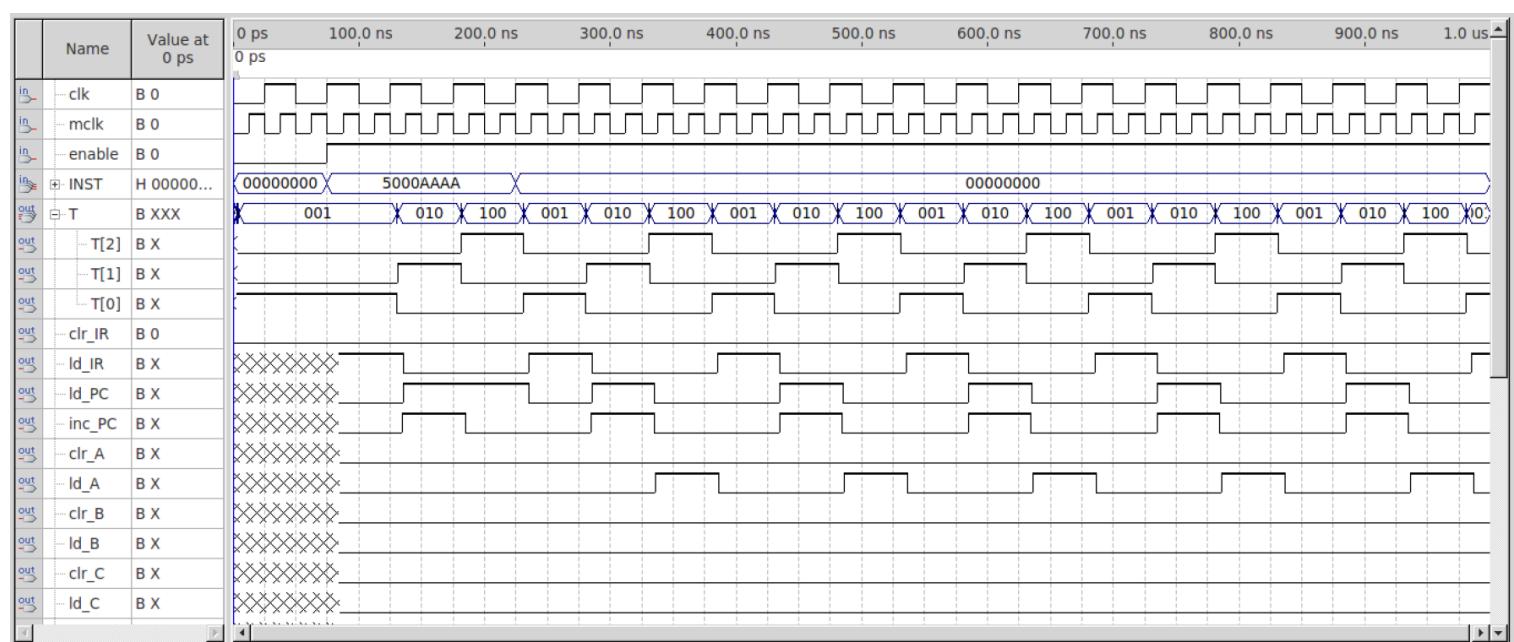
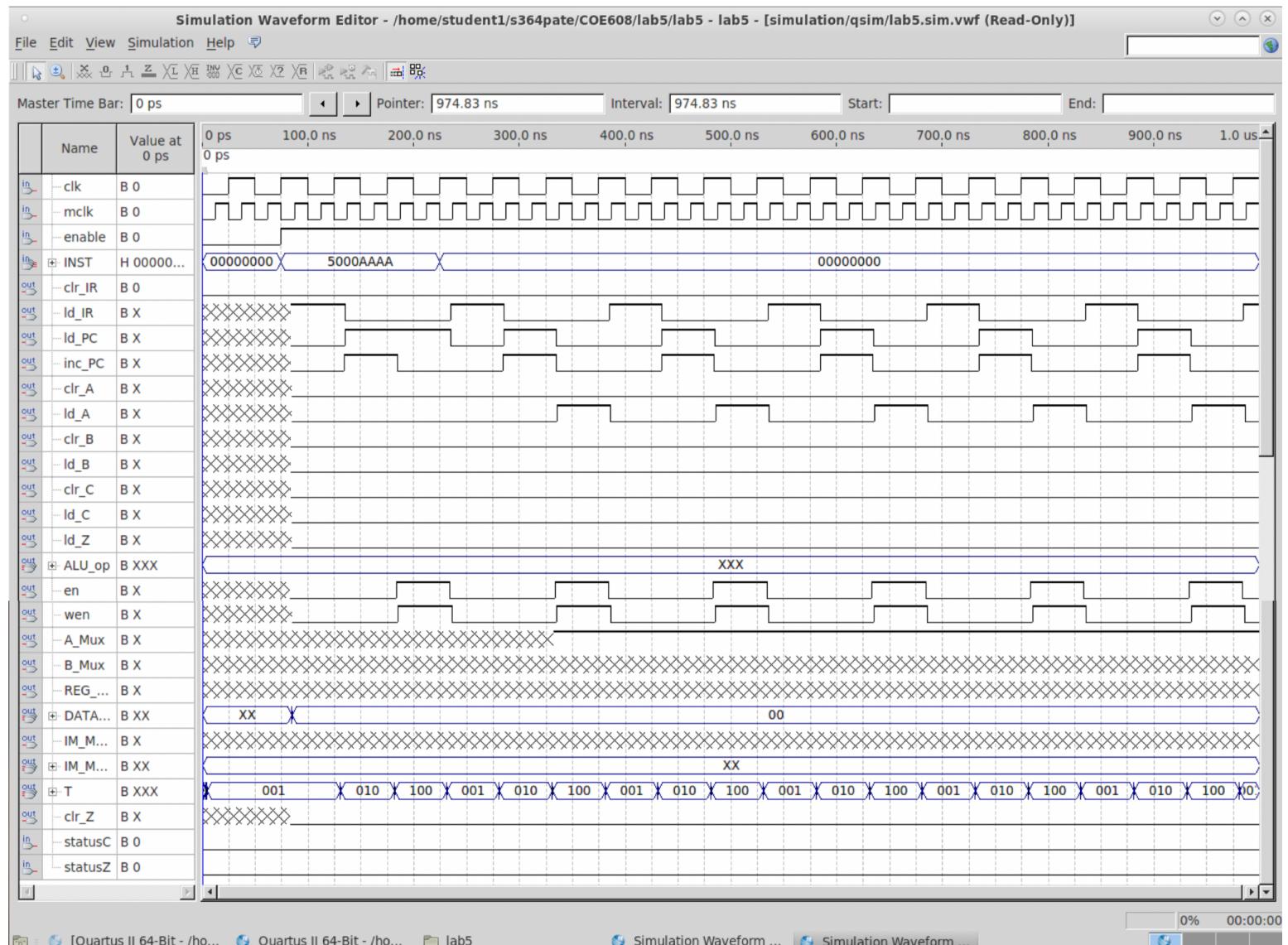
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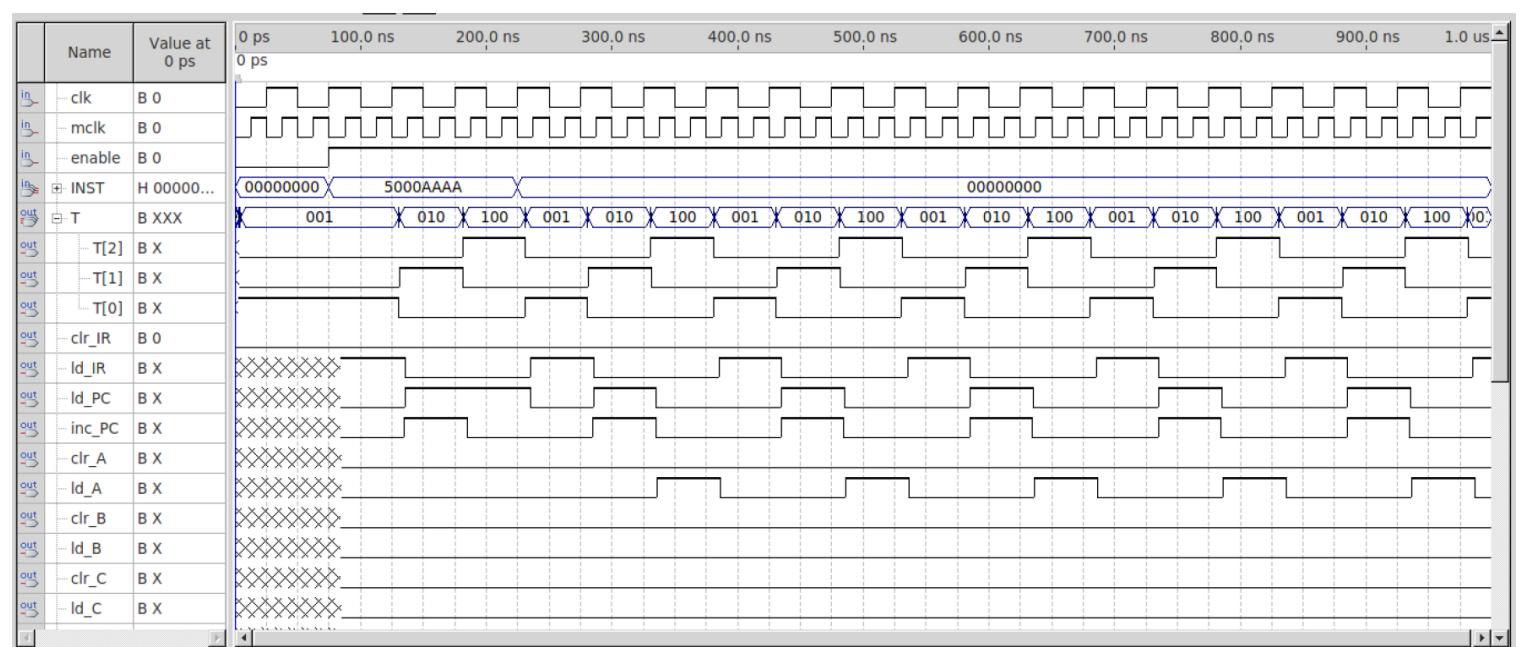
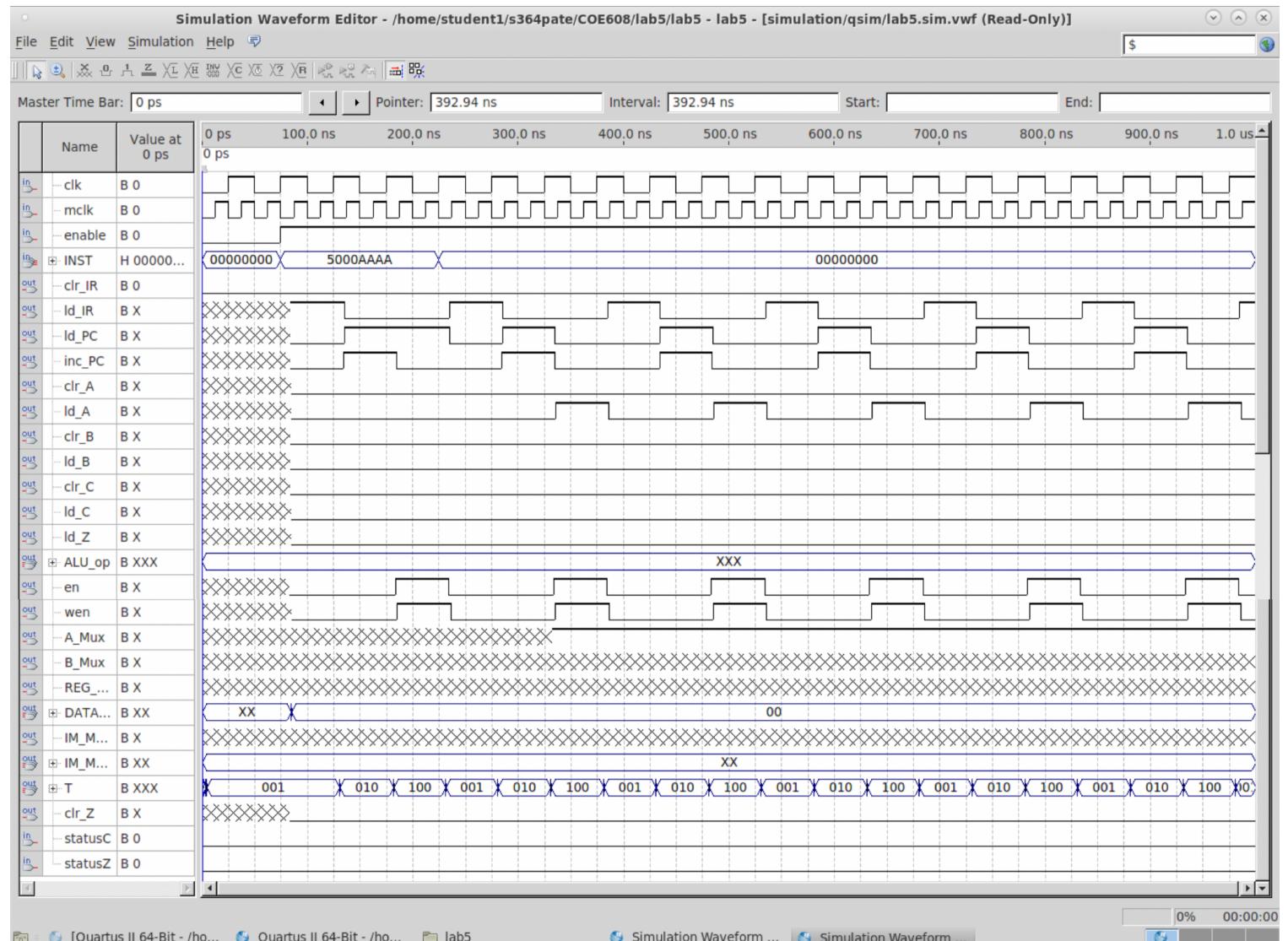
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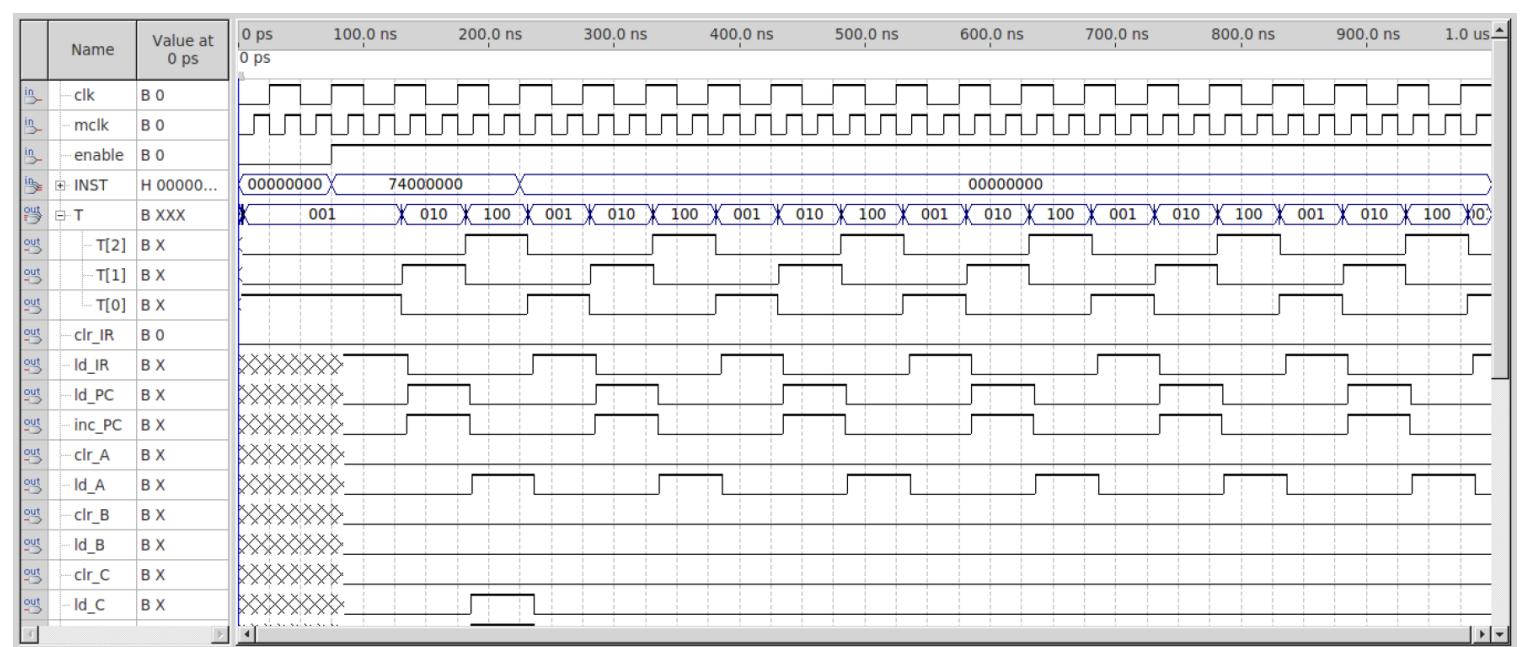
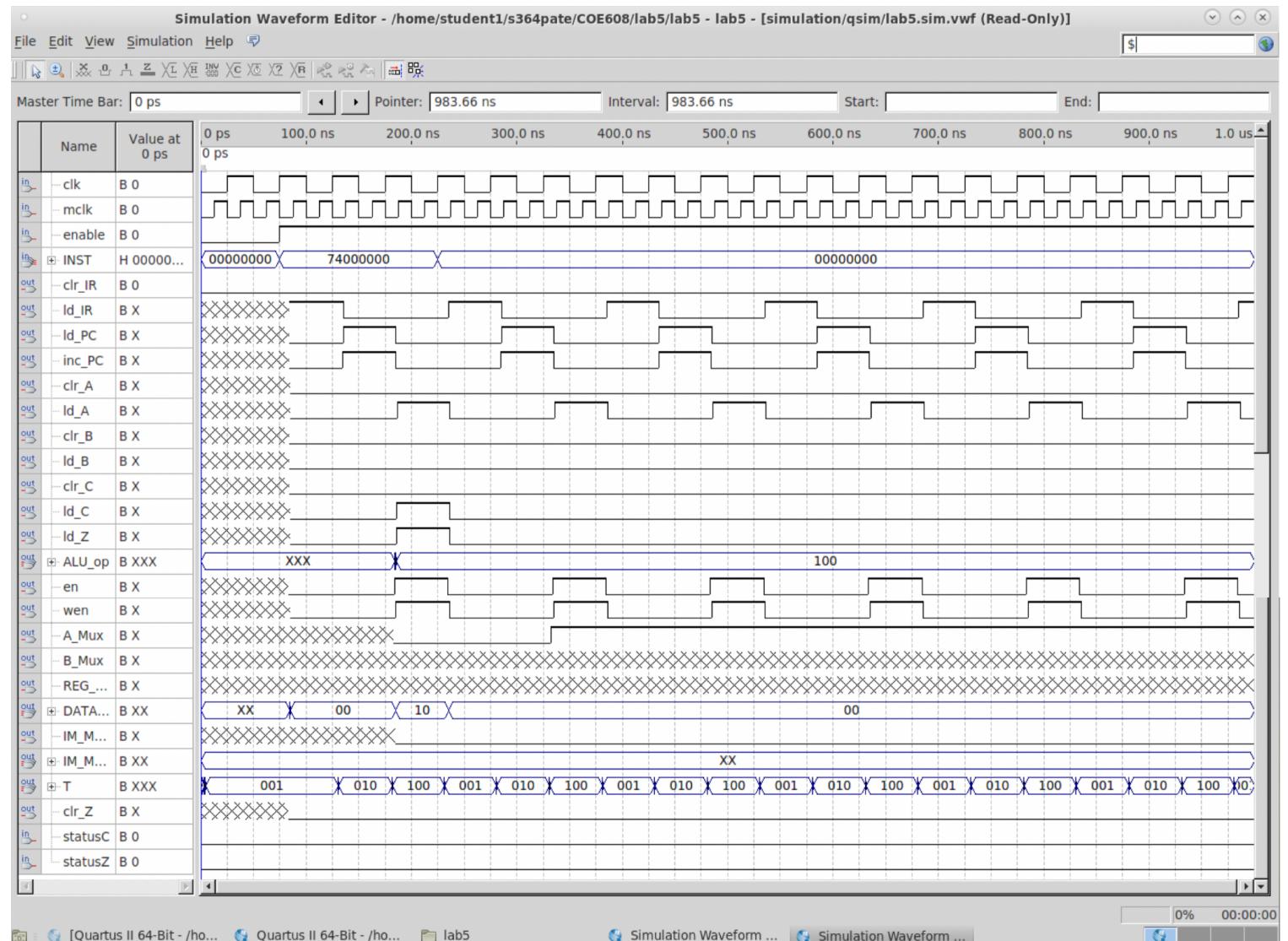
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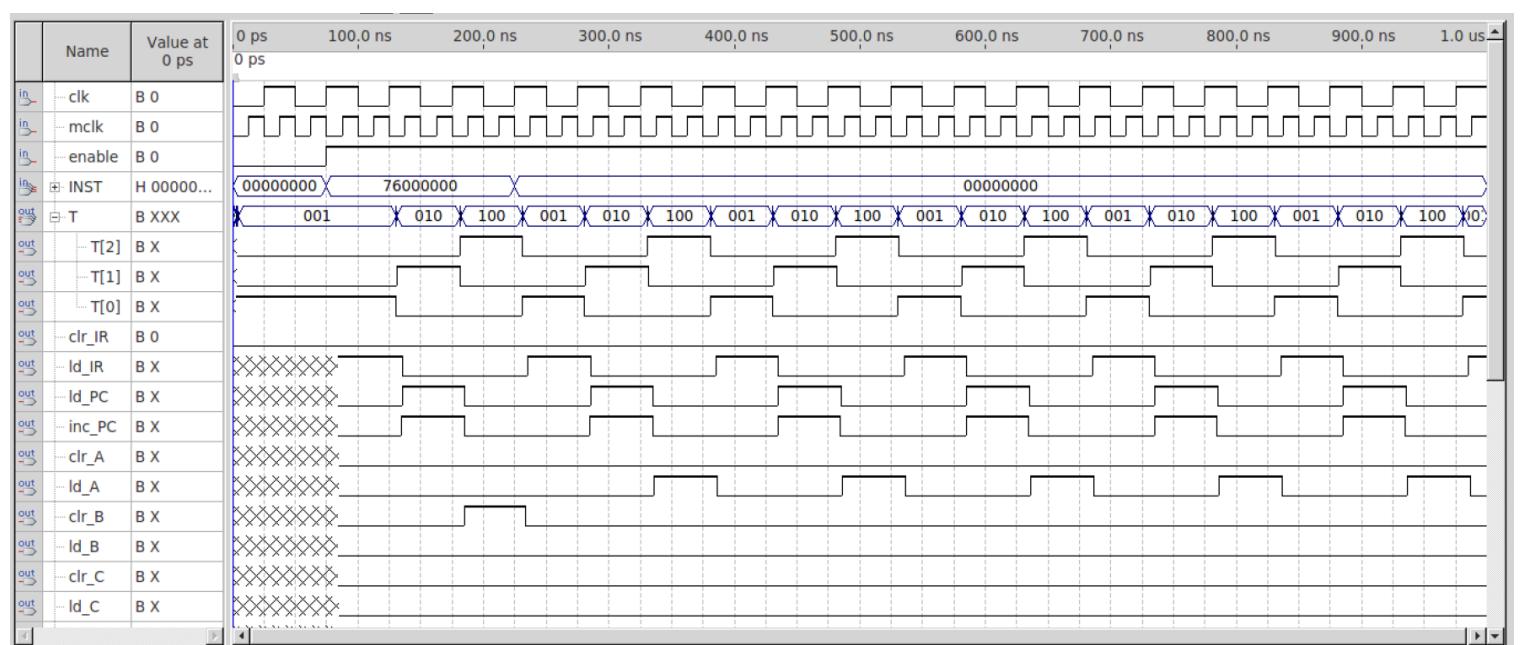
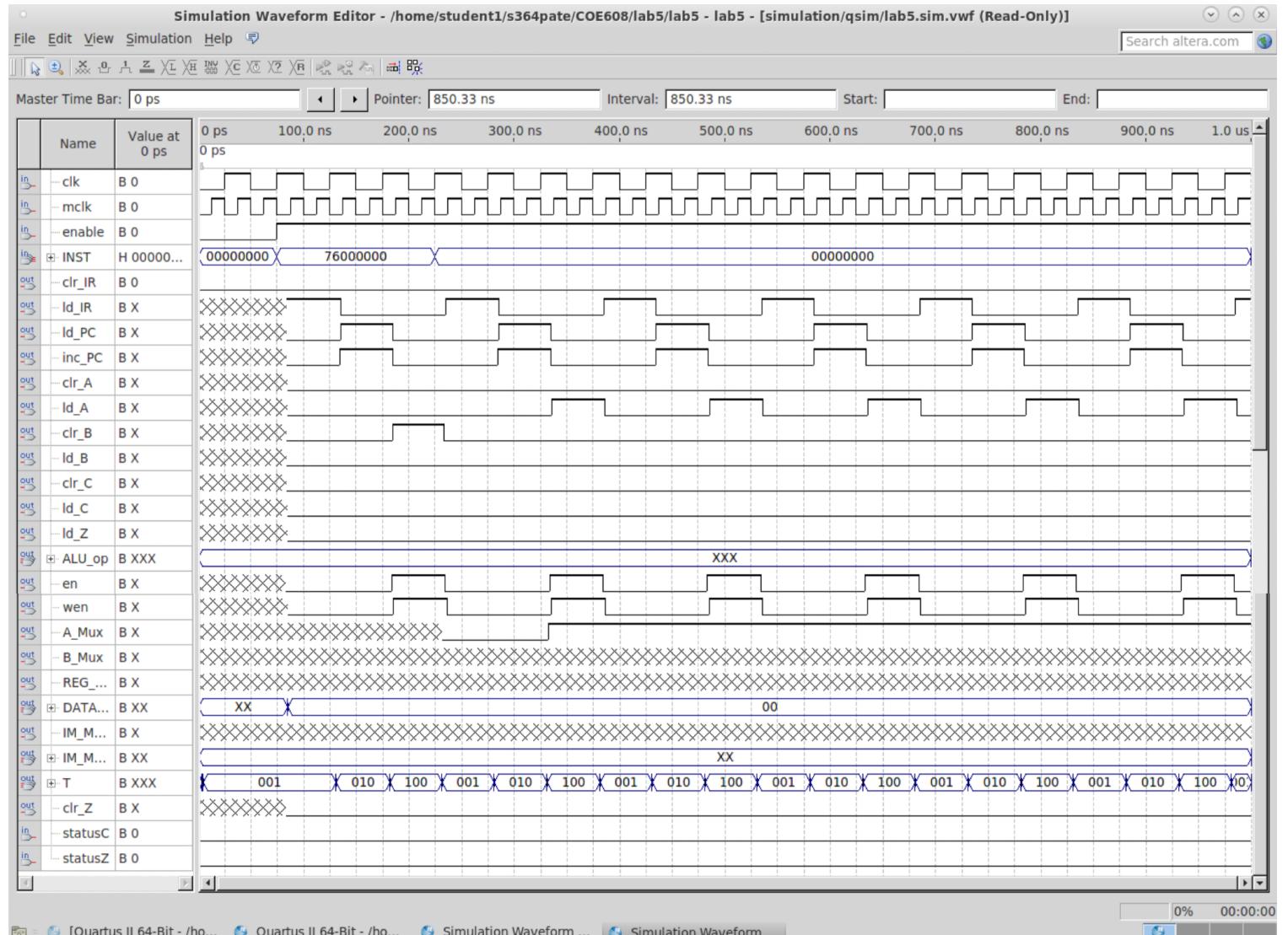
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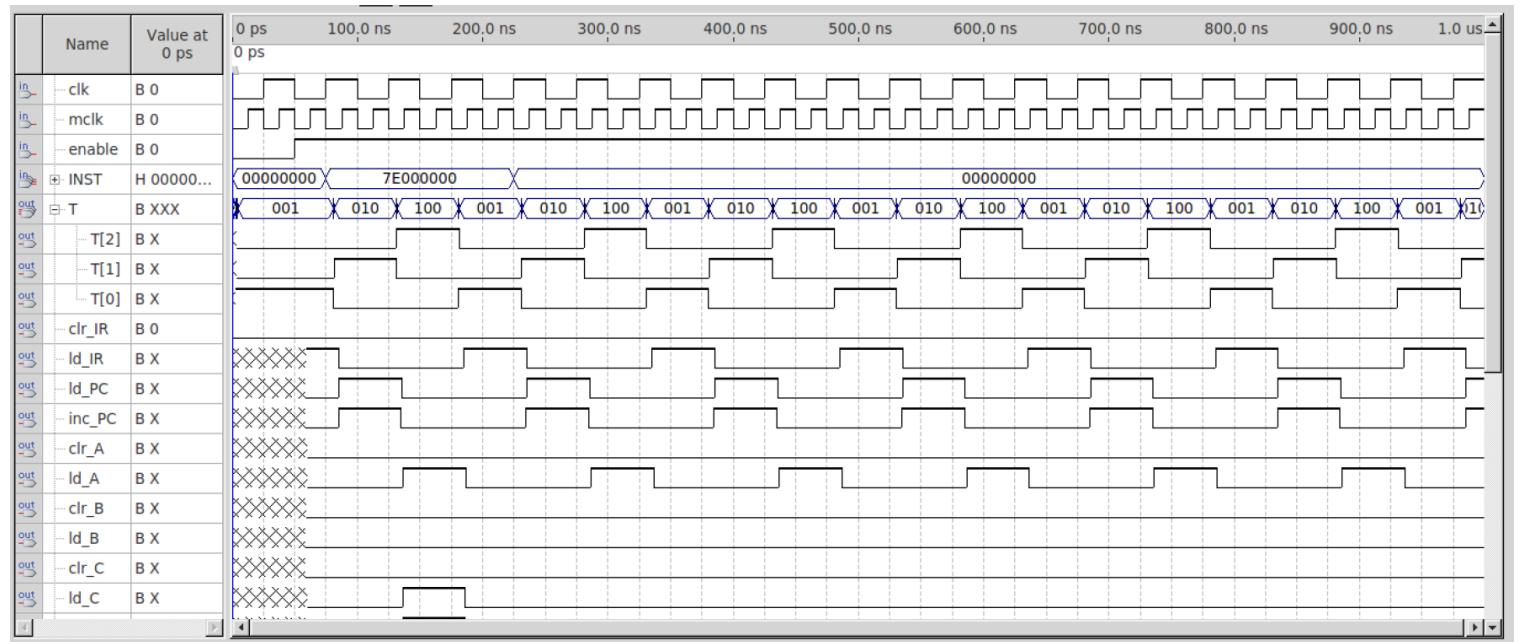
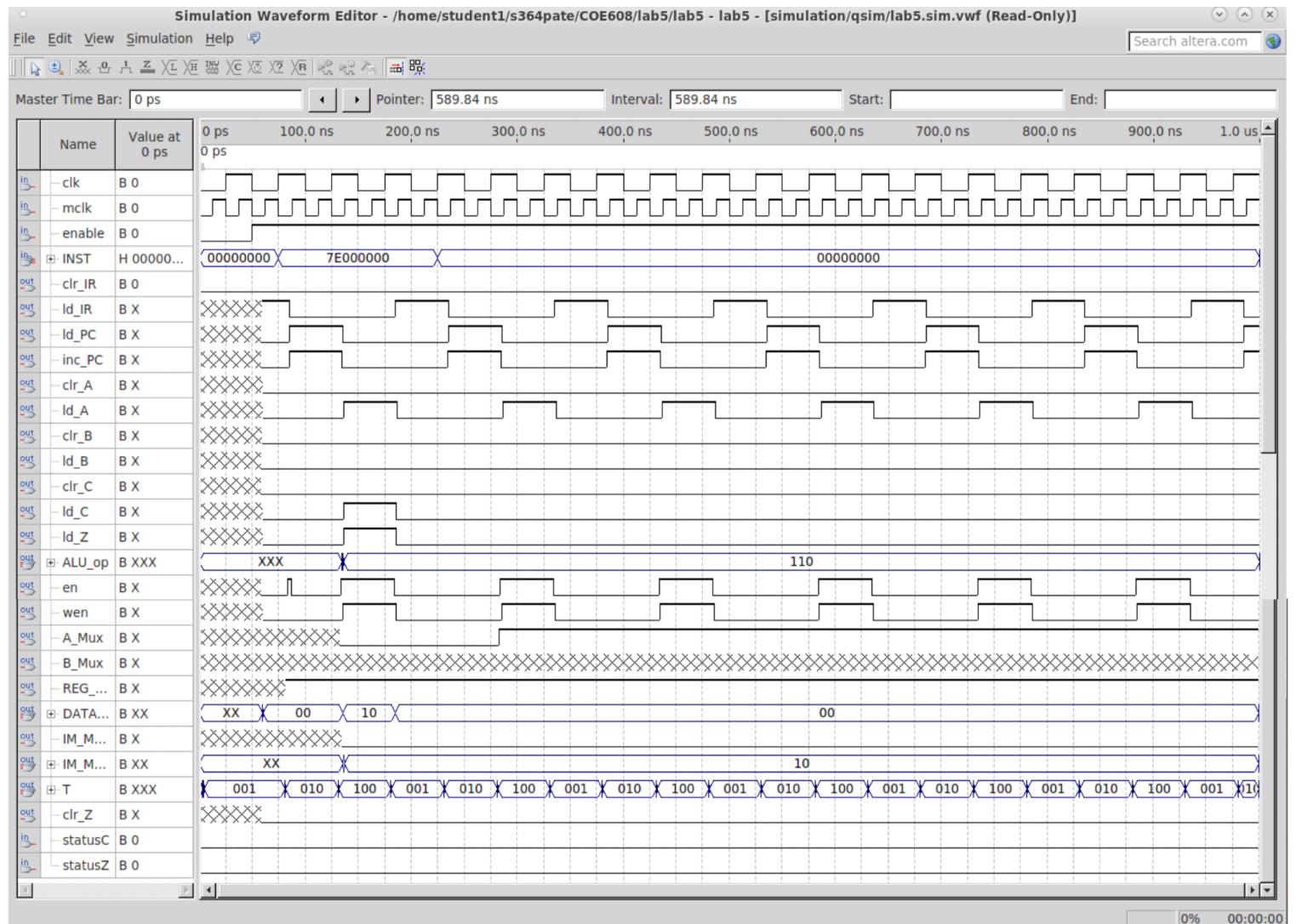
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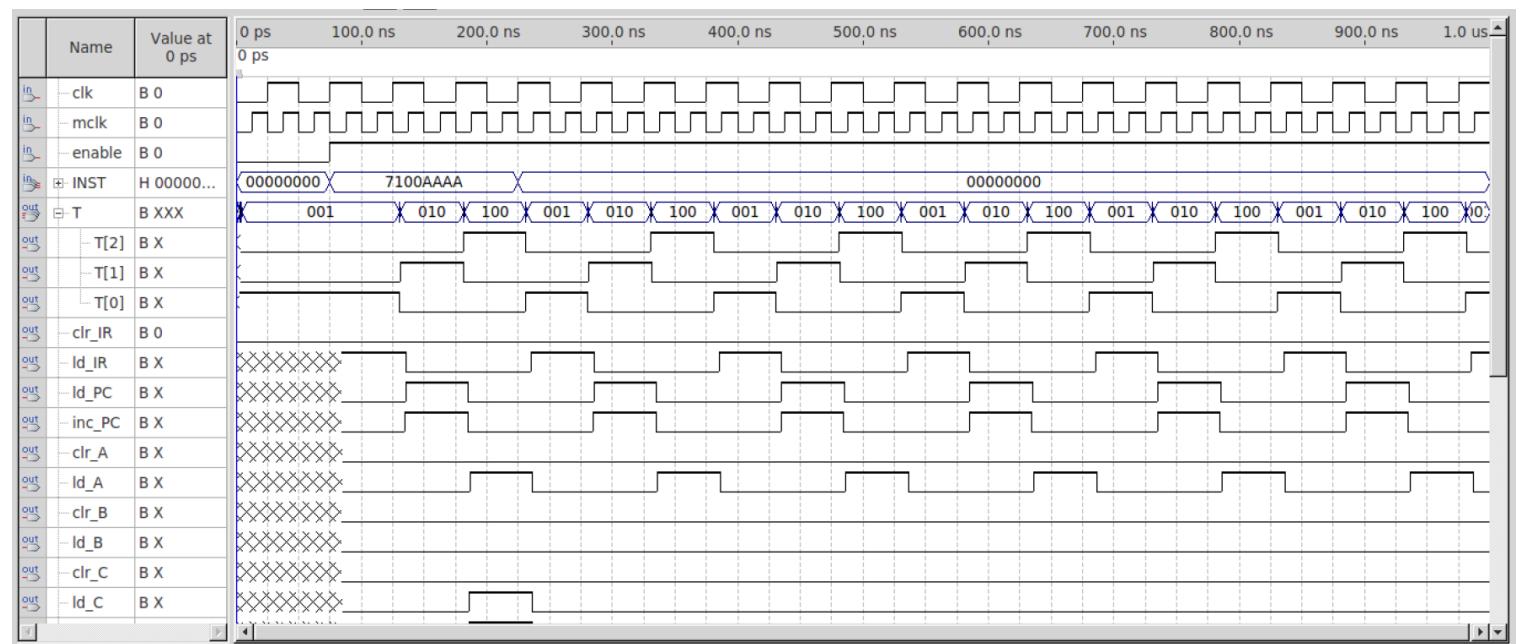
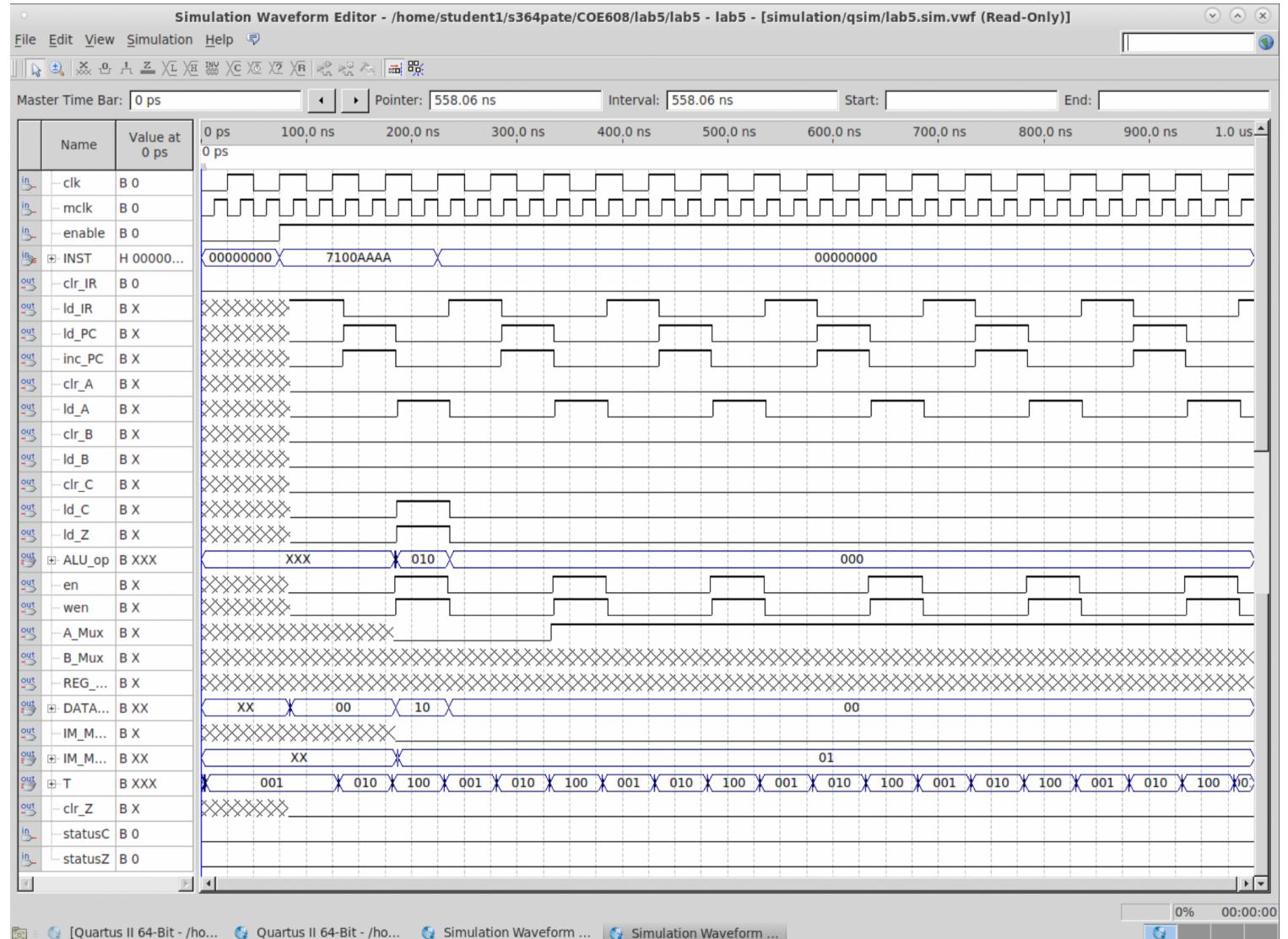
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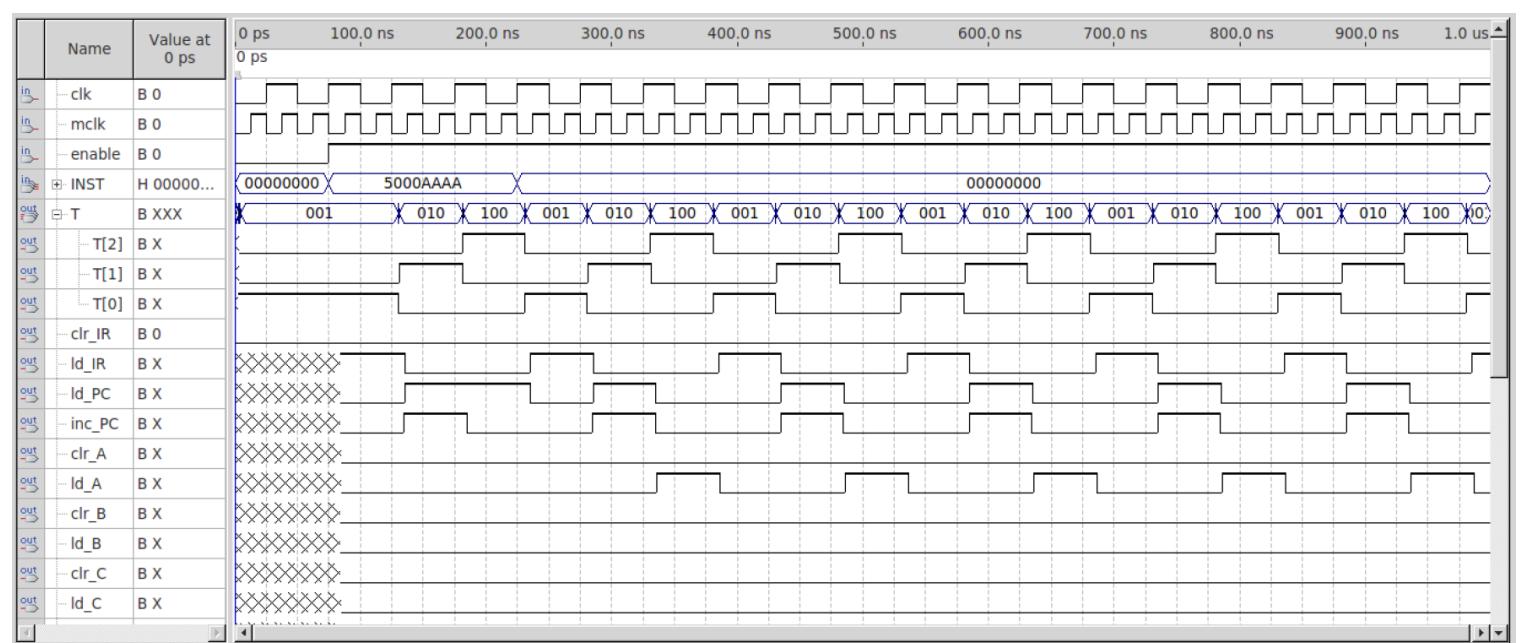
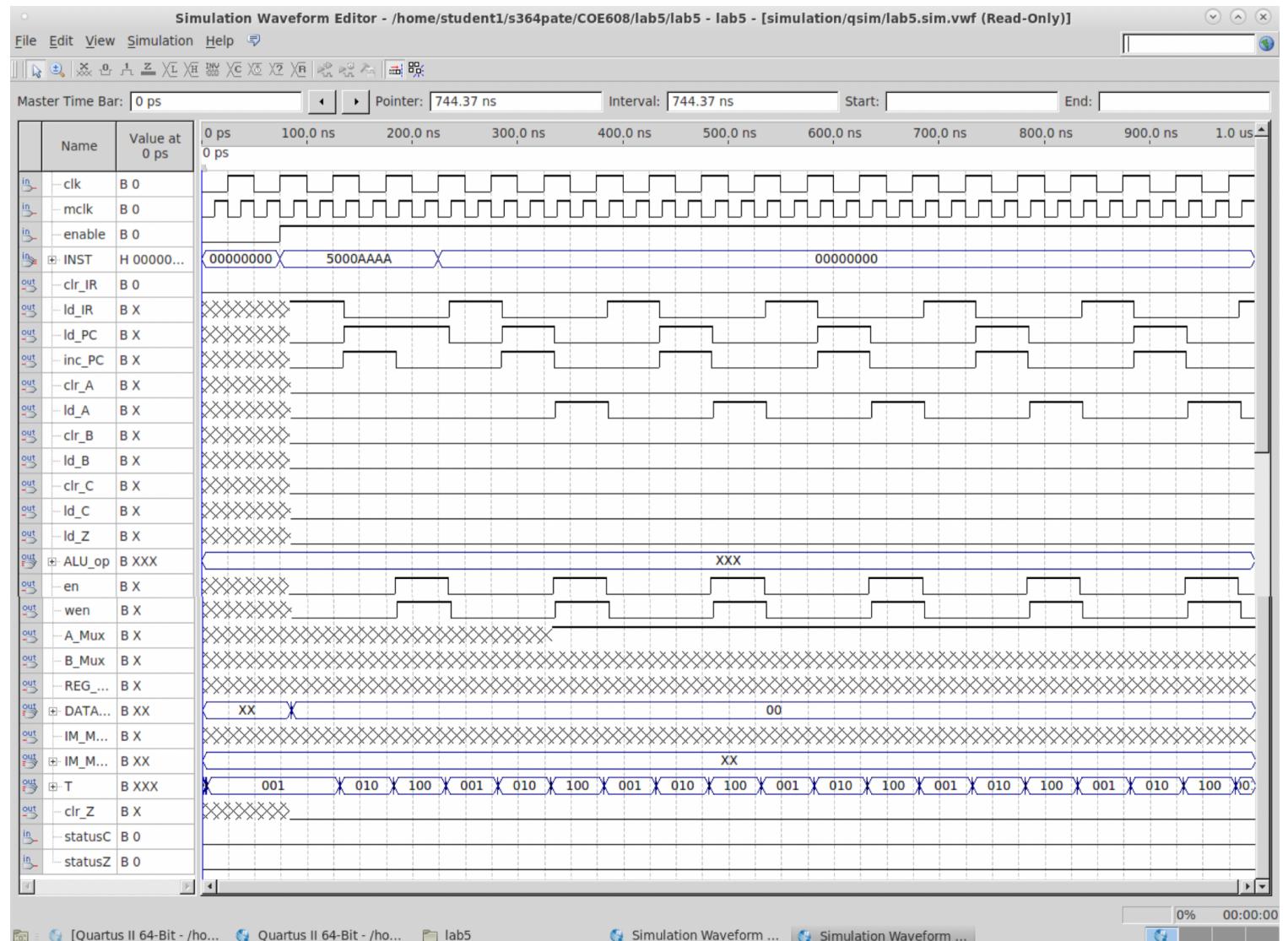
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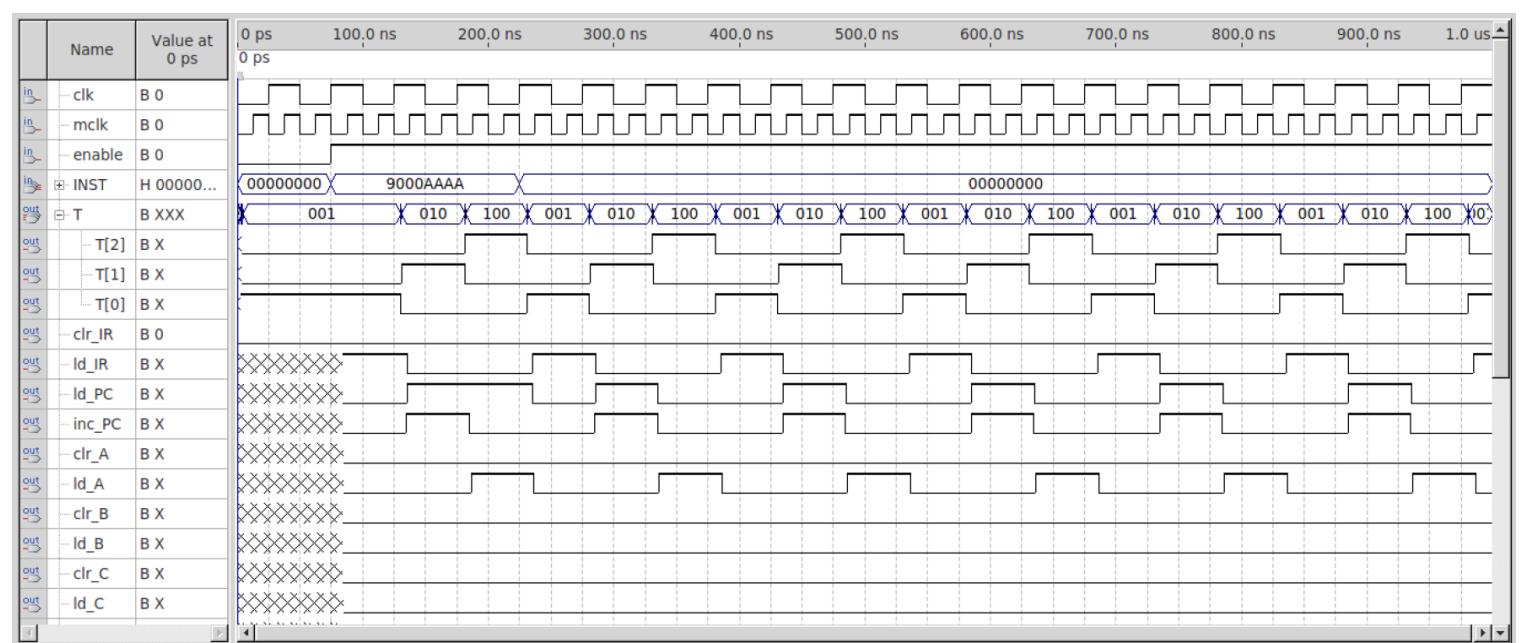
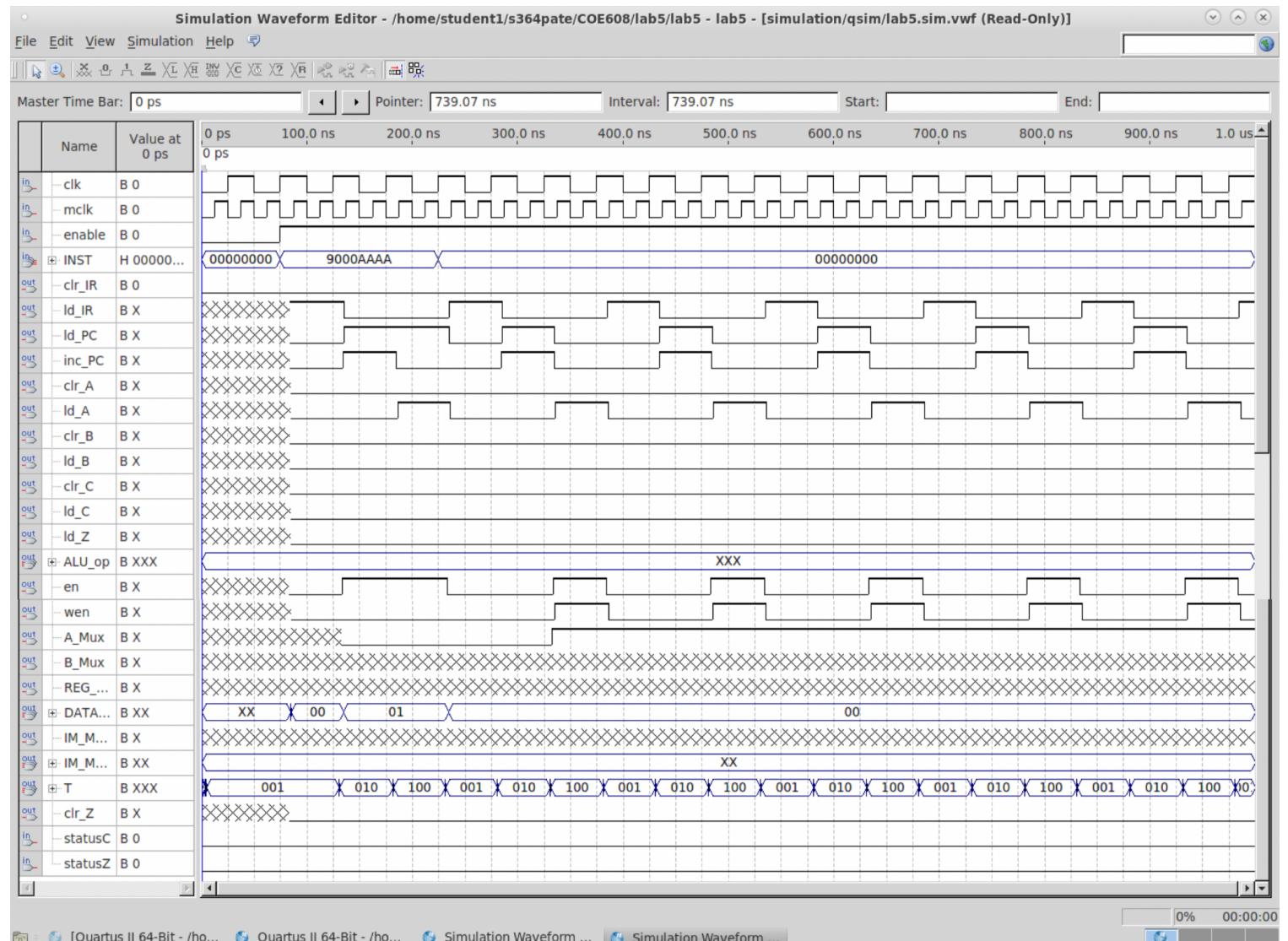
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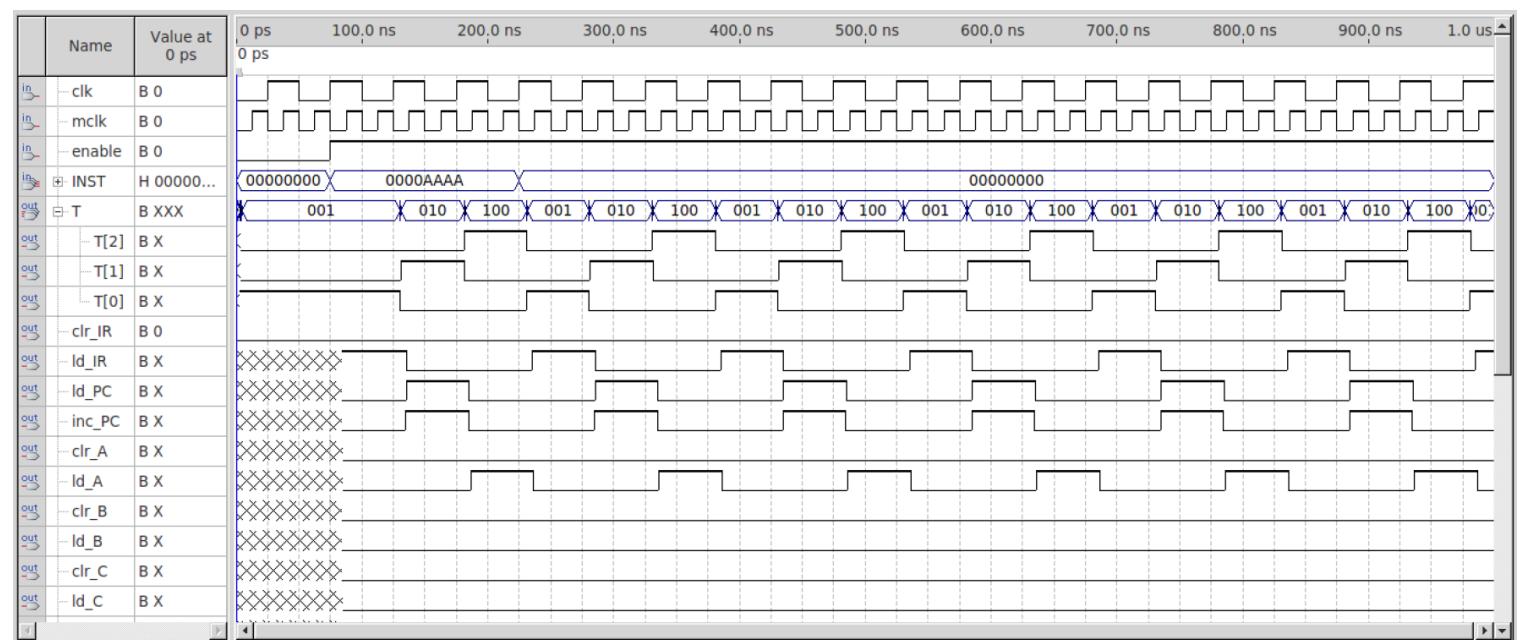
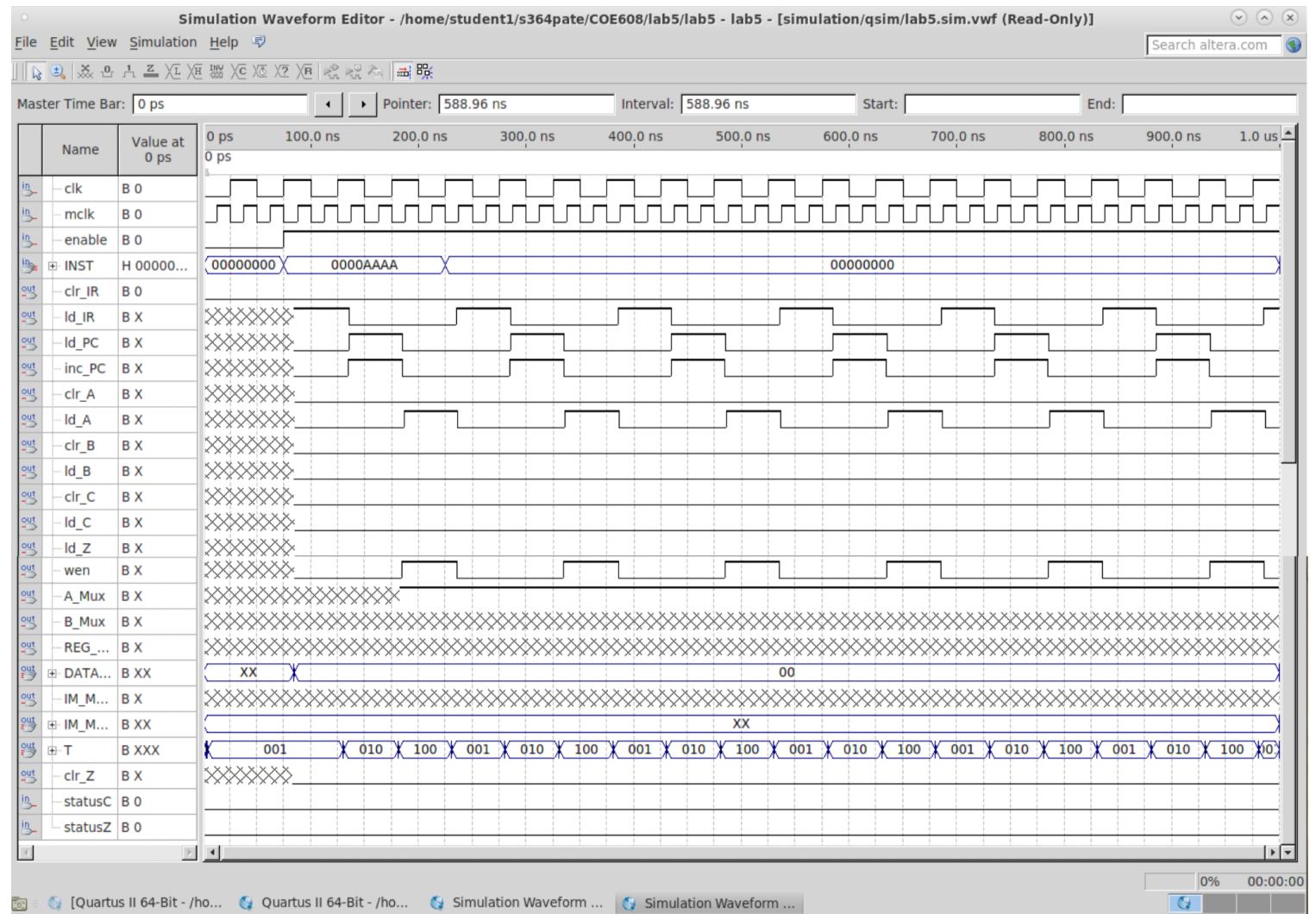
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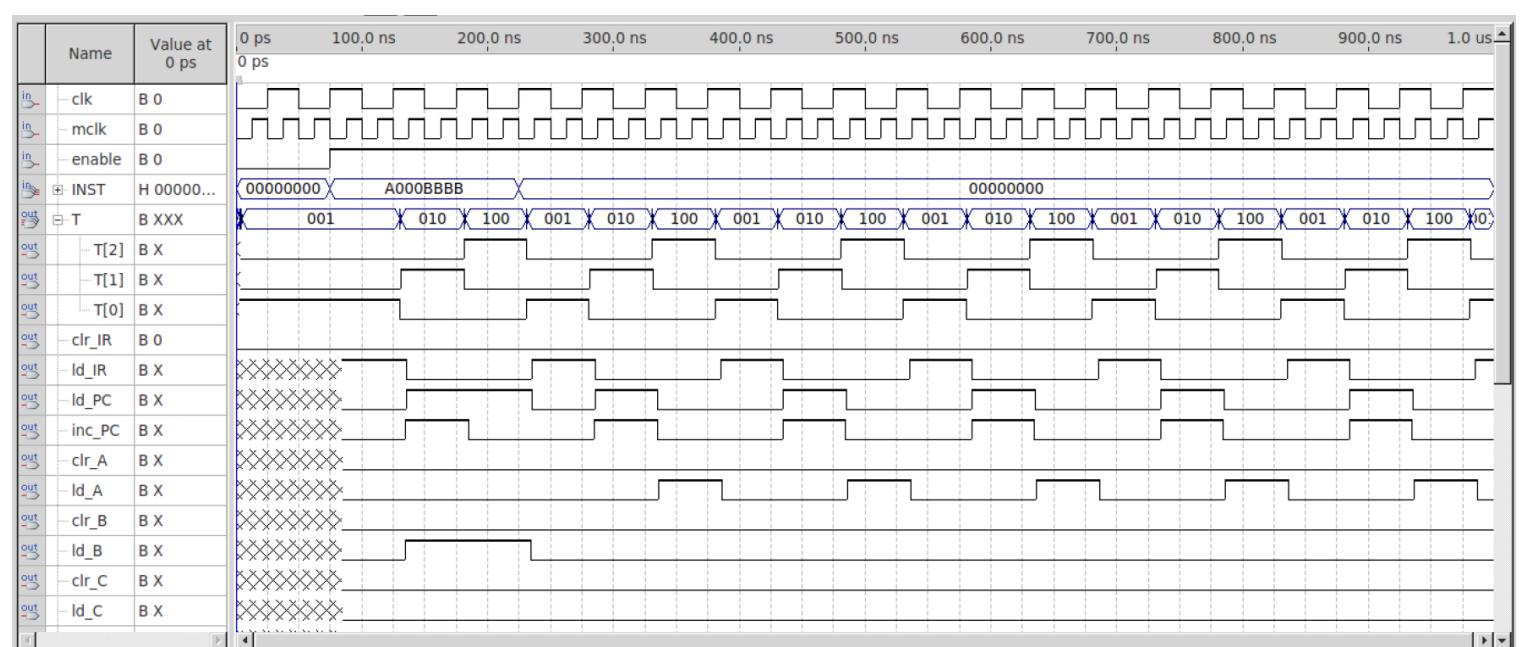
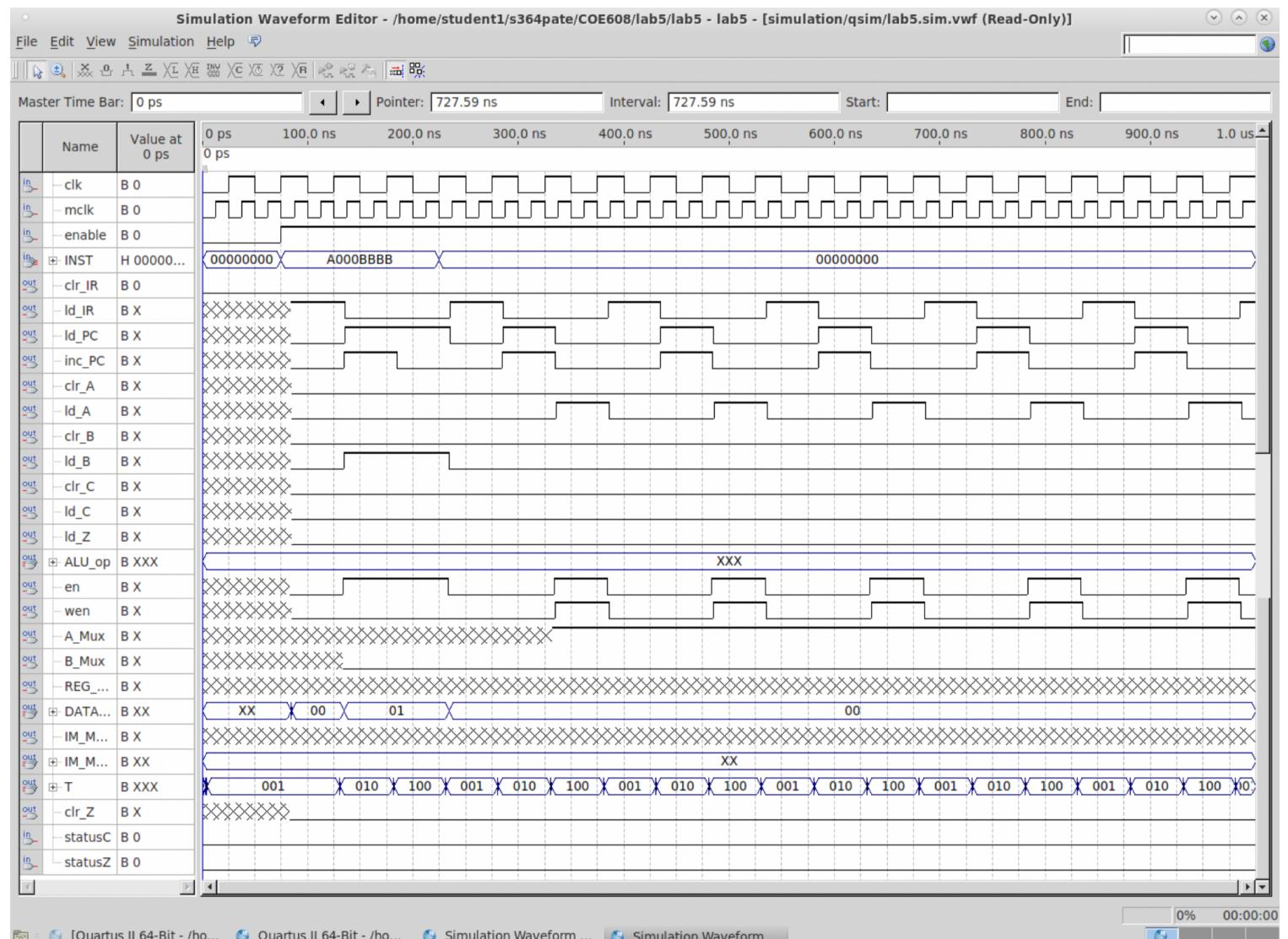
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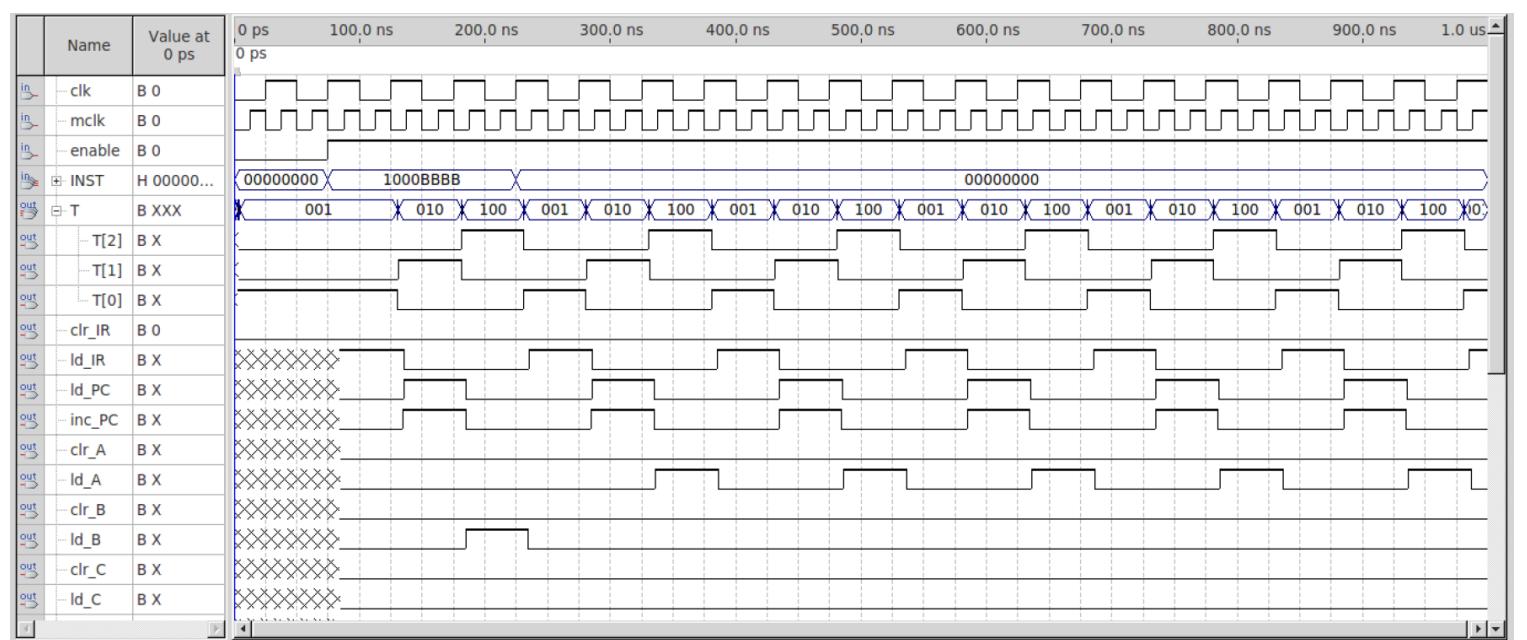
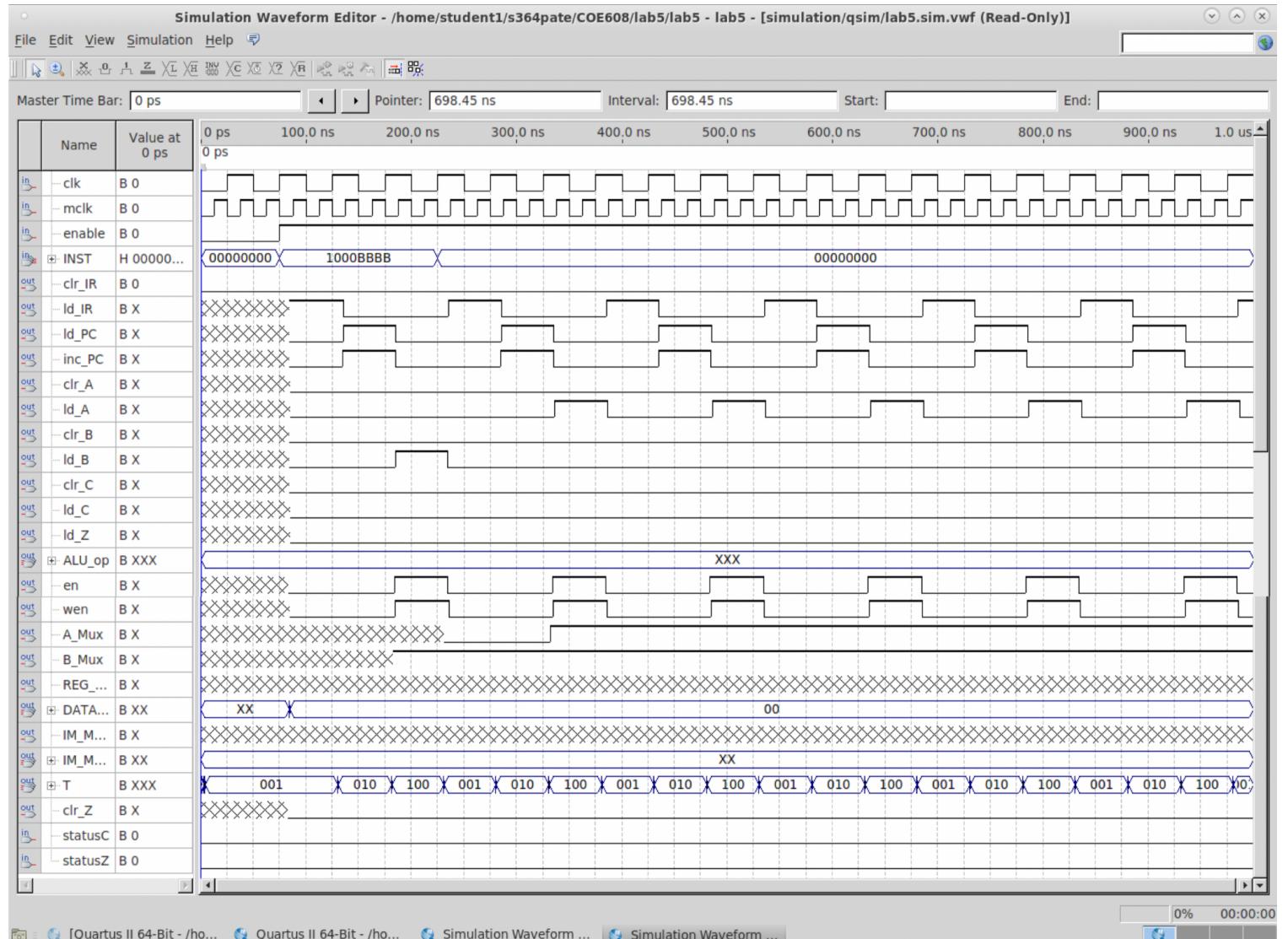
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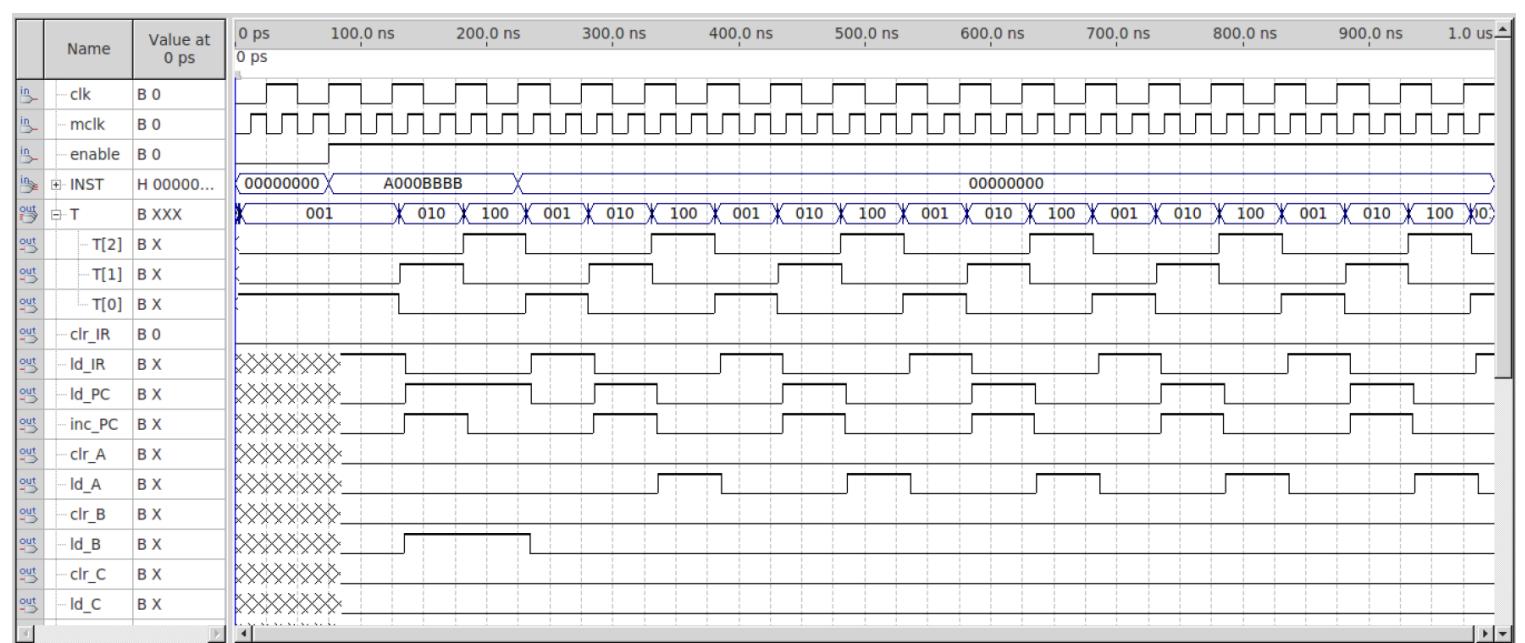
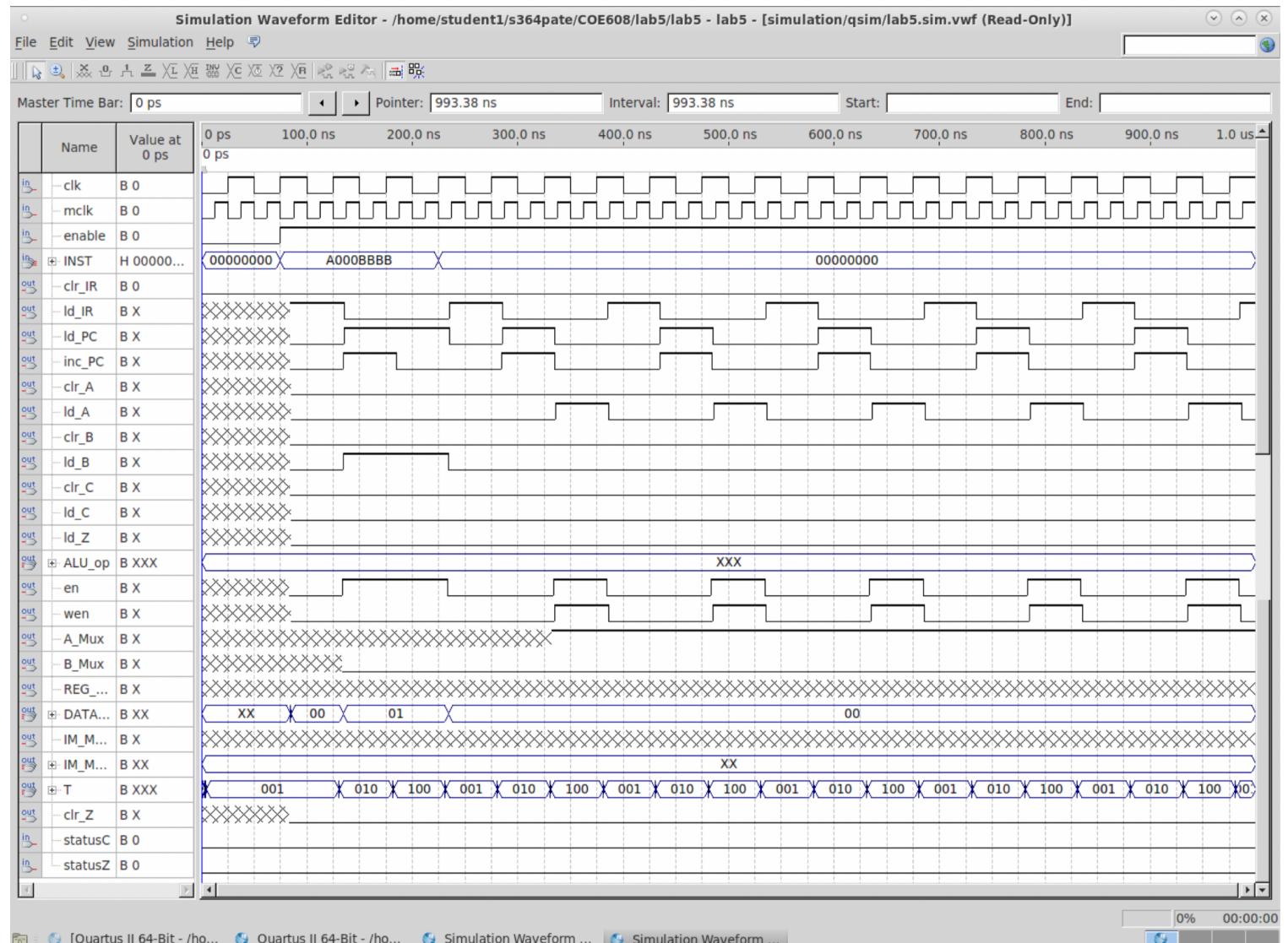
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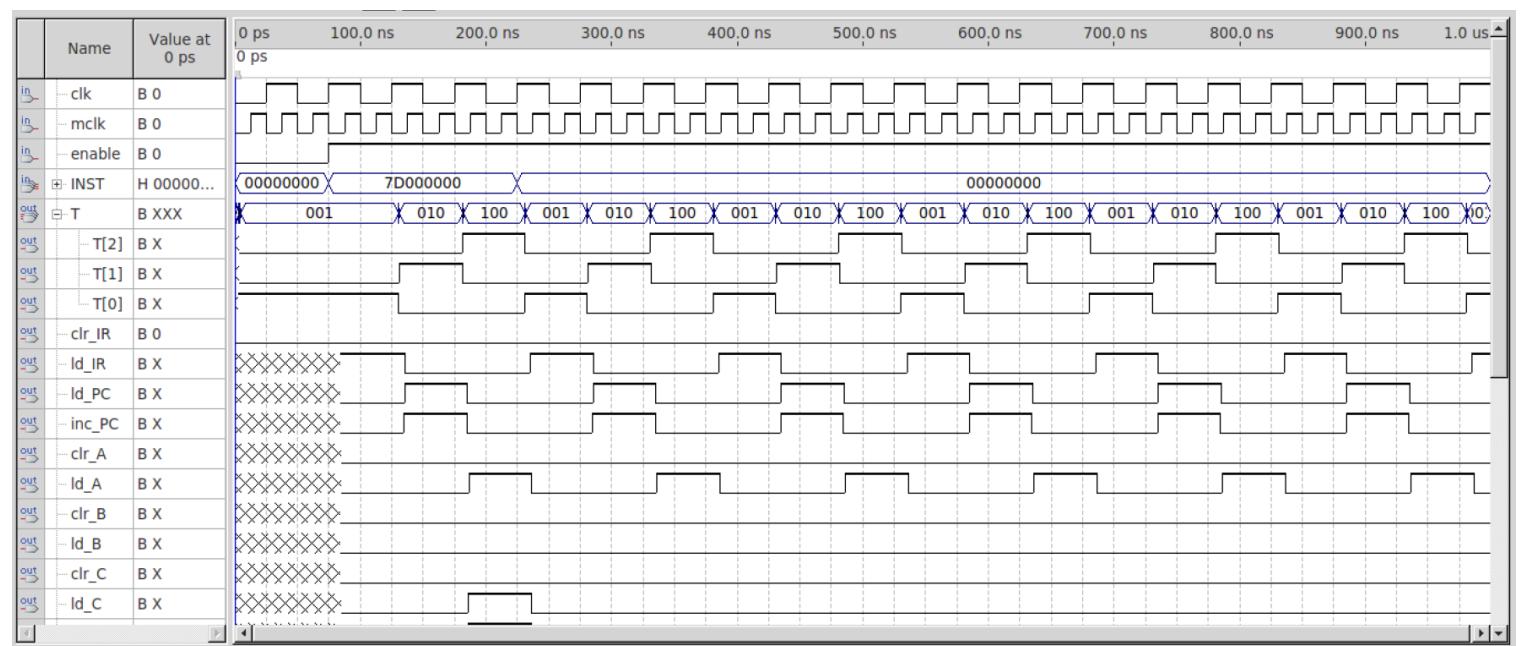
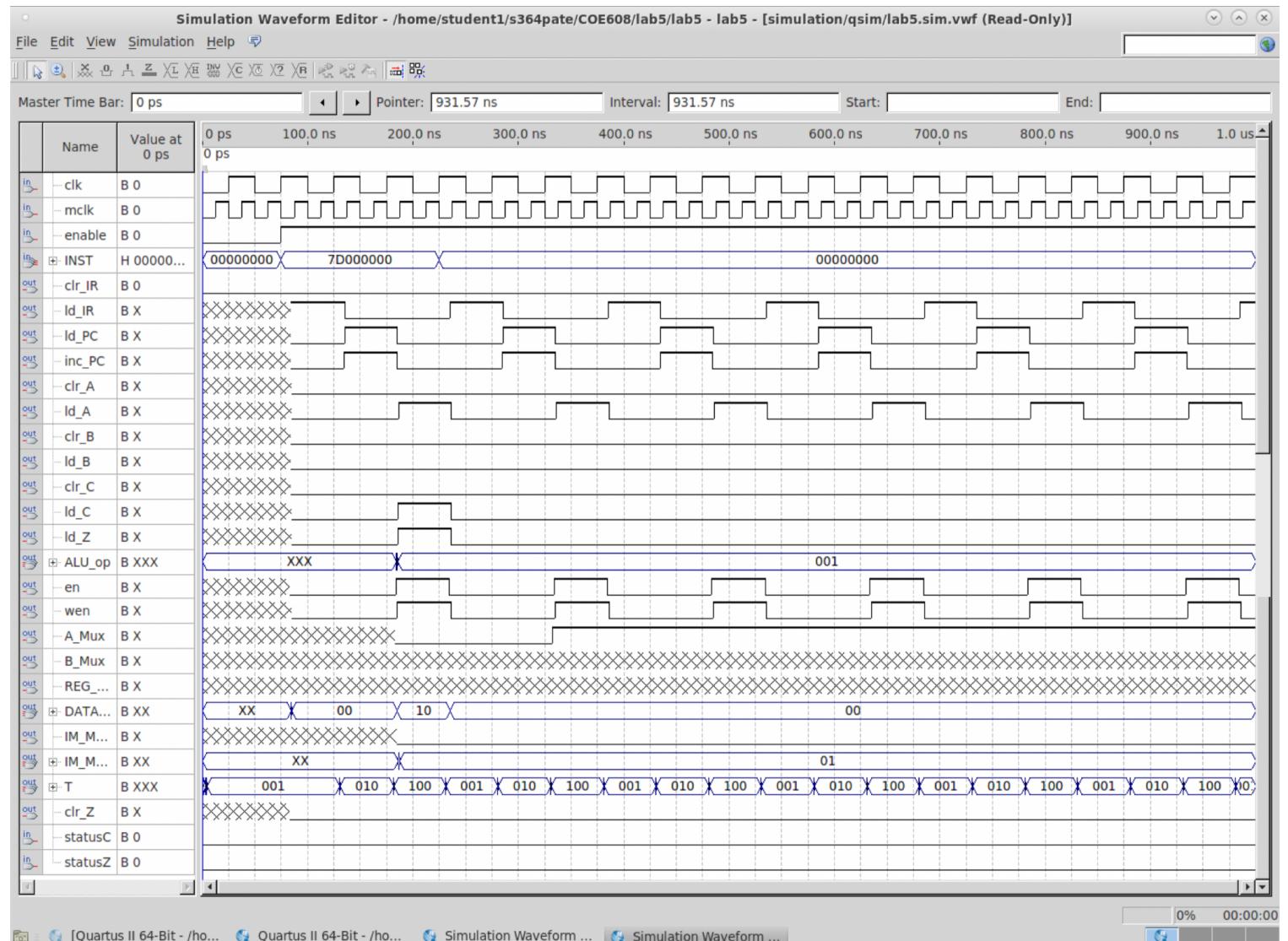
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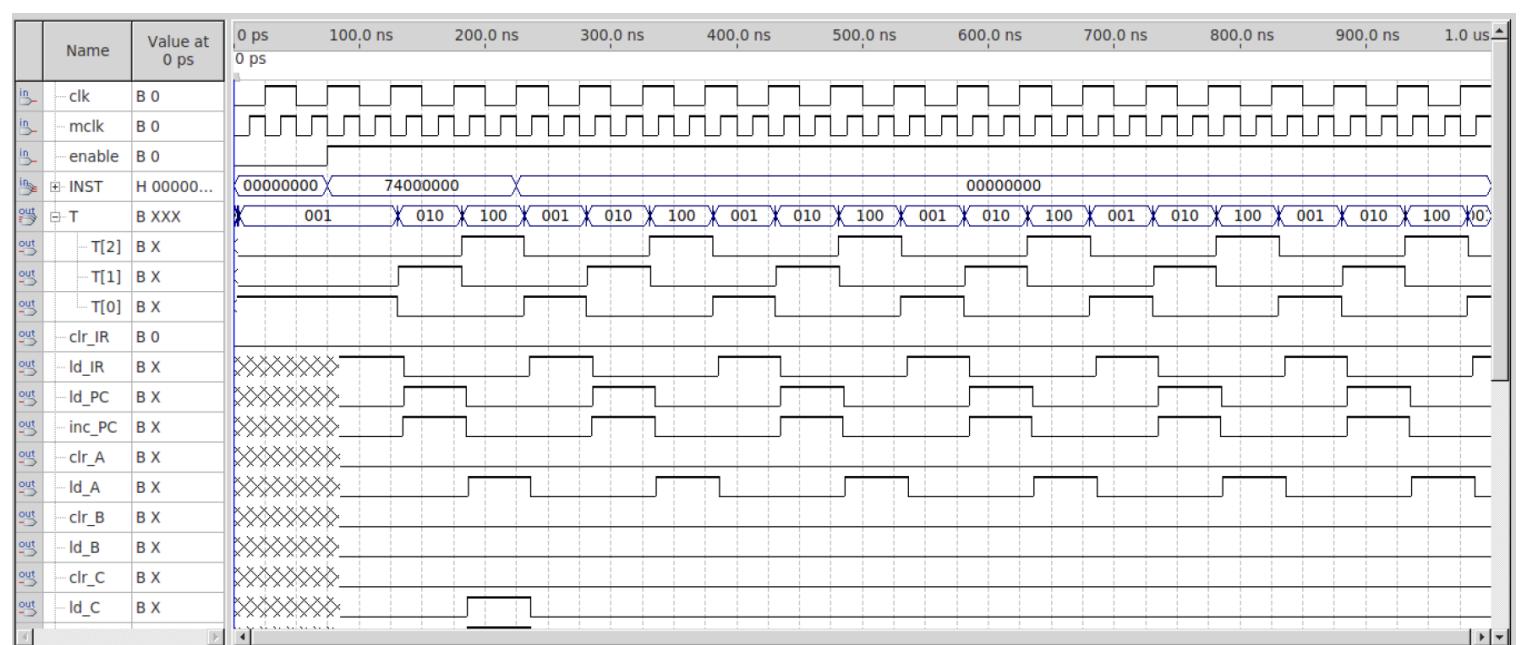
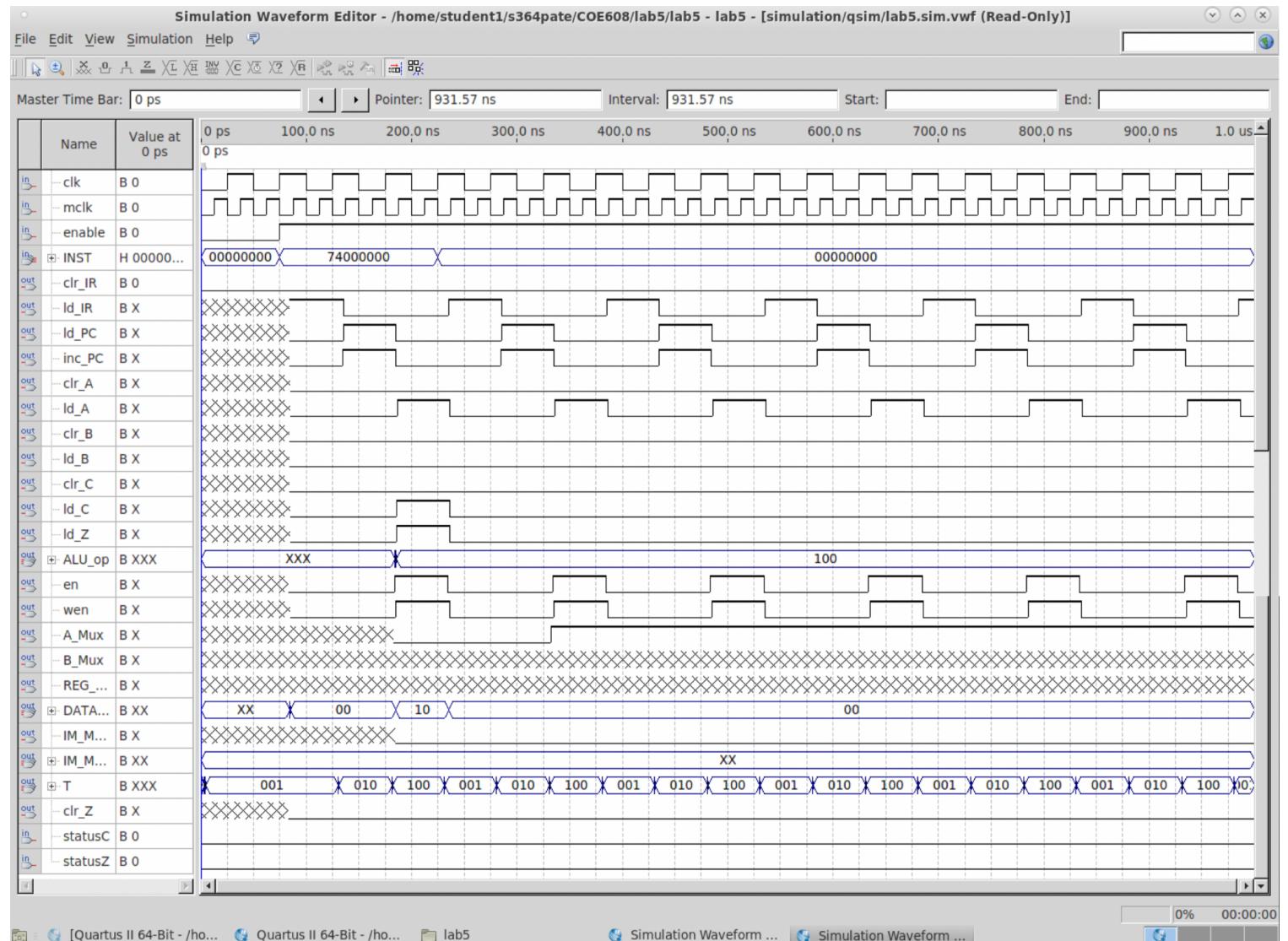
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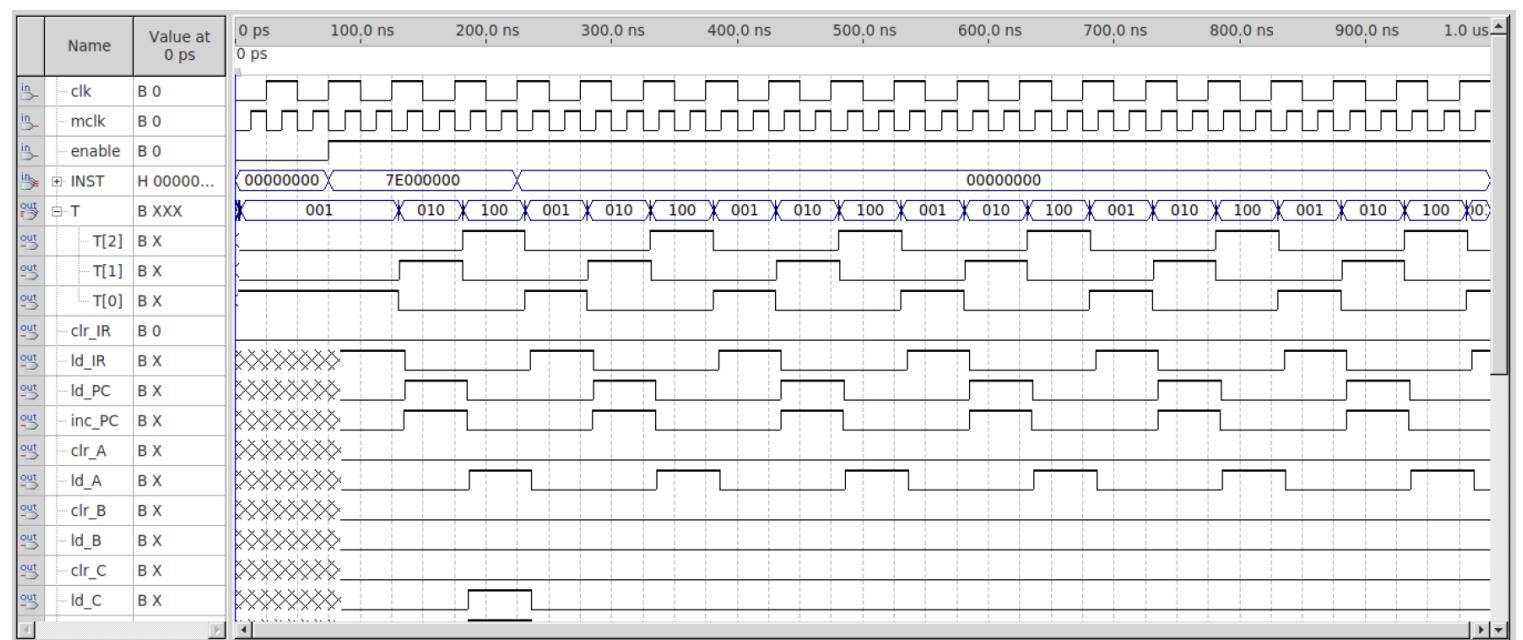
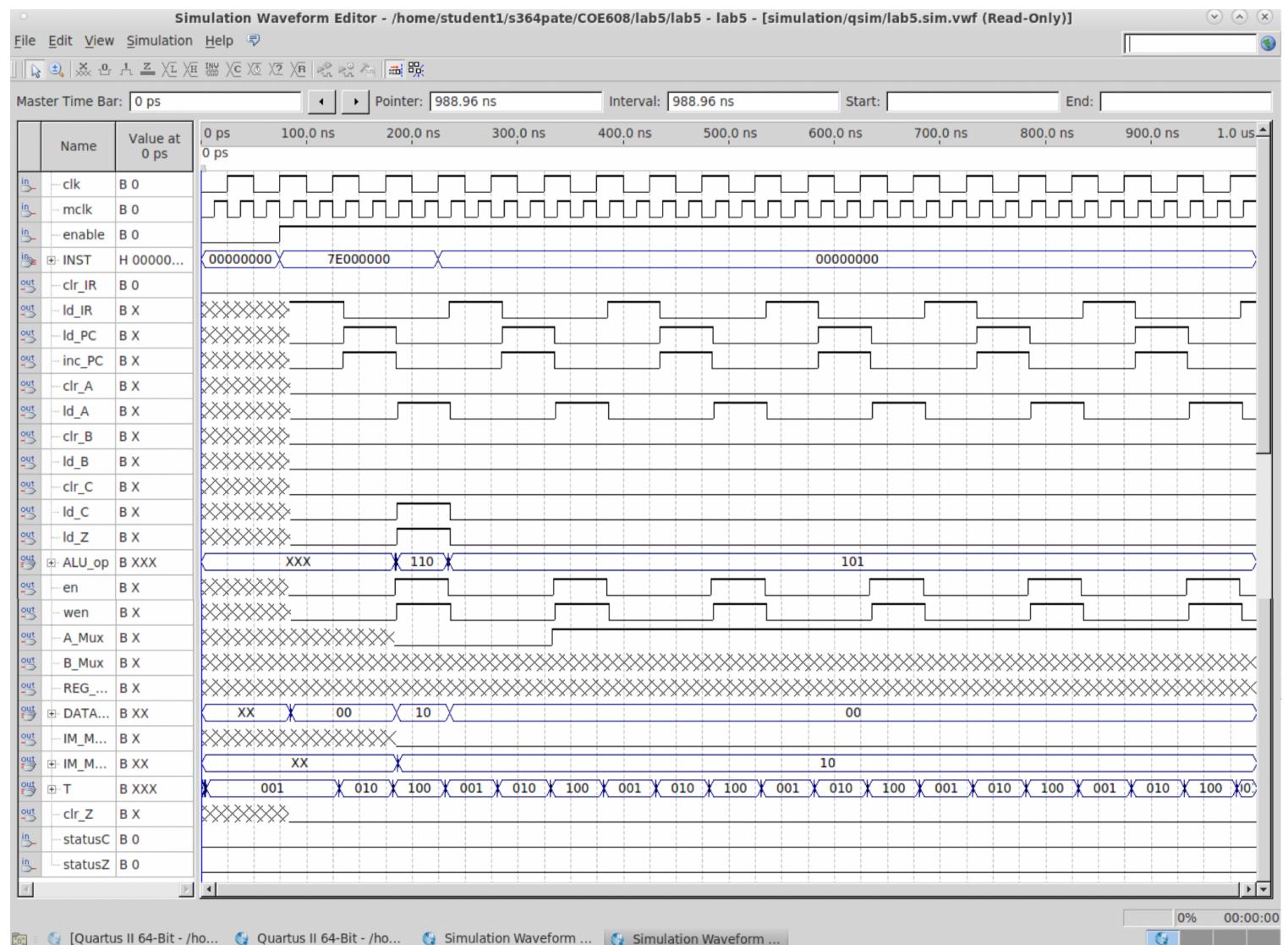
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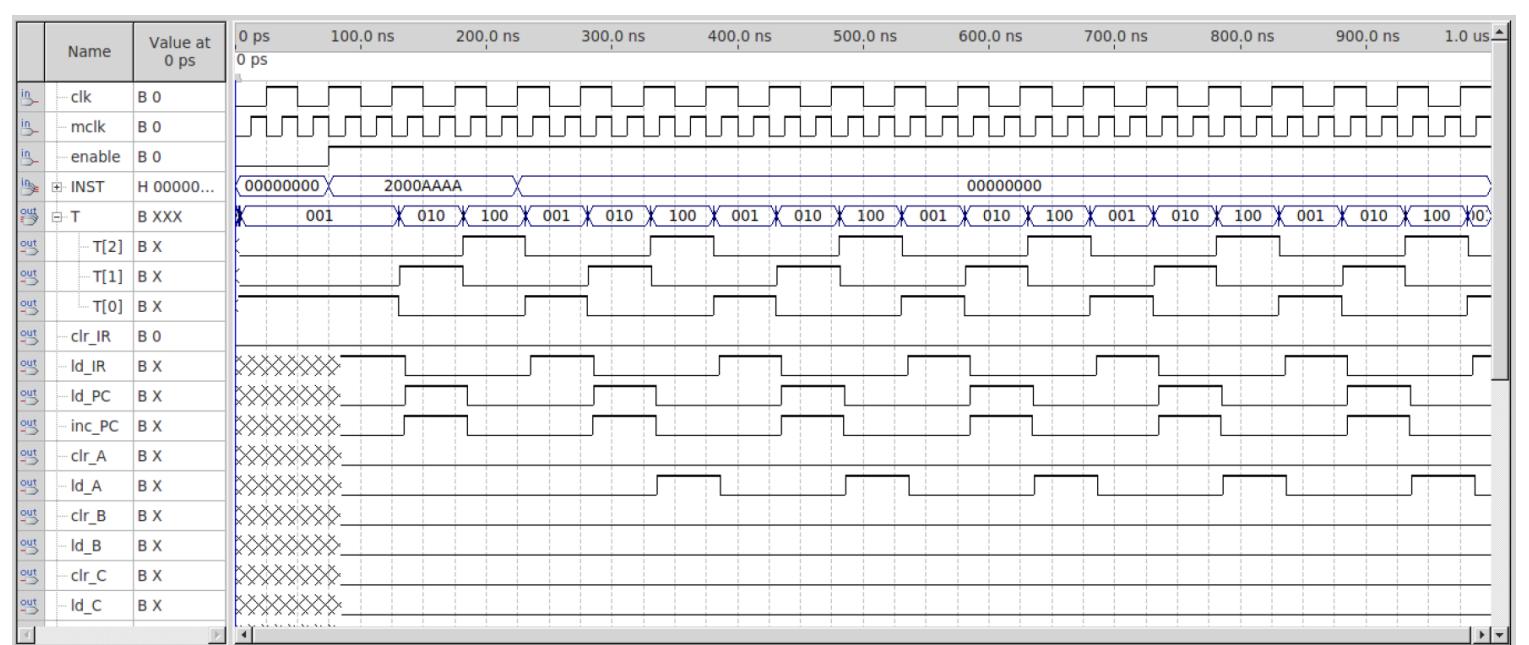
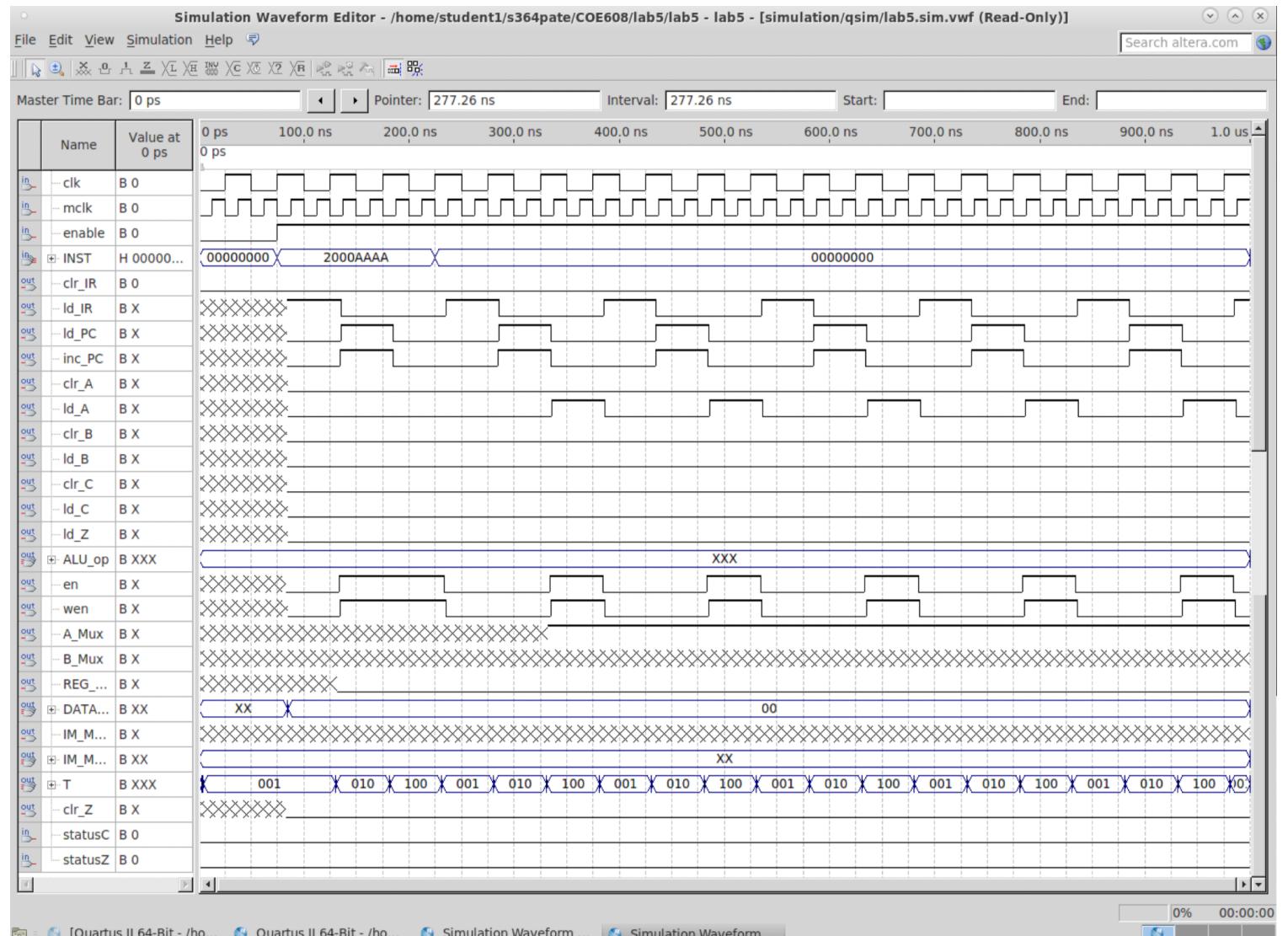
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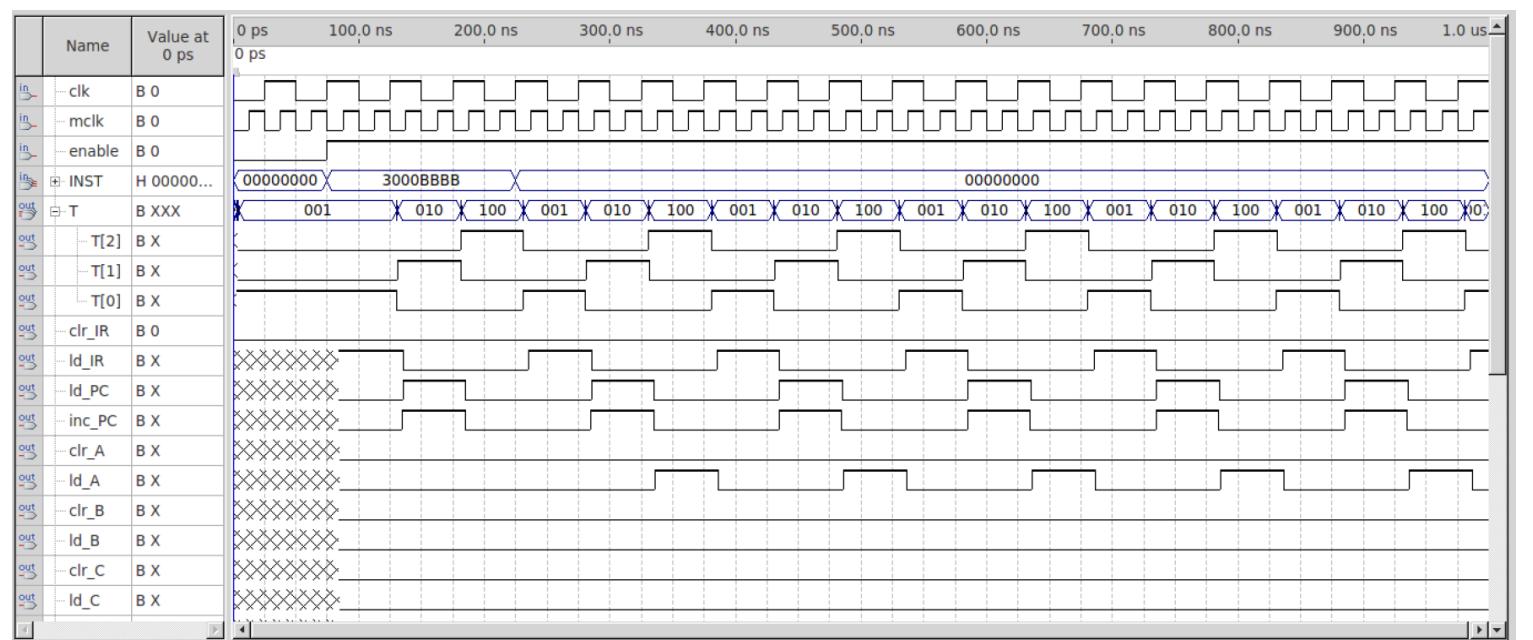
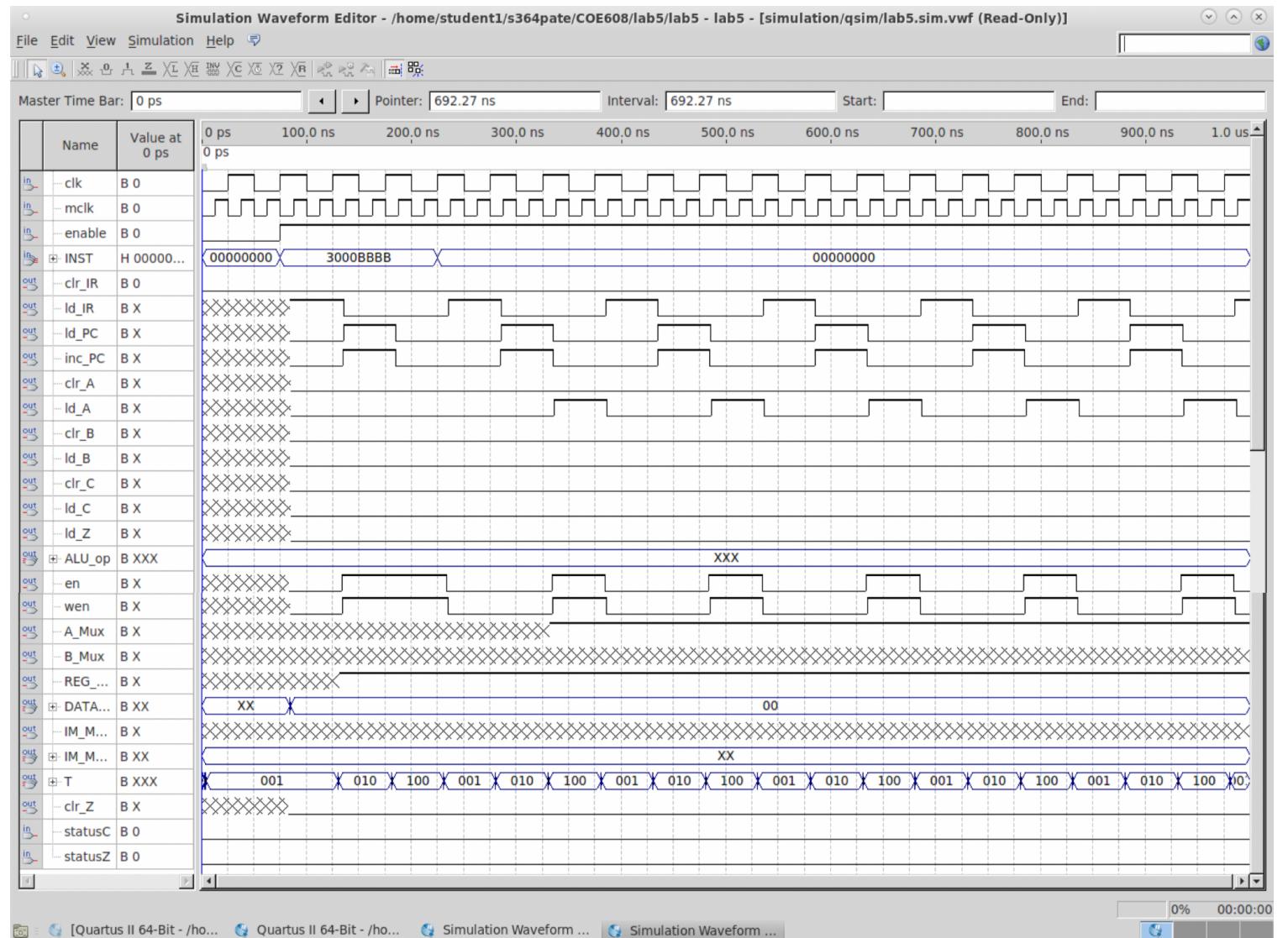
ROR



STA



STB



SUB

