

Course Title:	Computer Organization and Architecture
Course Number:	COE608
Semester/Year (e.g.F2016)	Winter 2023

Instructor:	Demetres Kostas
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Assignment/Lab Number:	6
Assignment/Lab Title:	The Complete CPU (Overall Project)

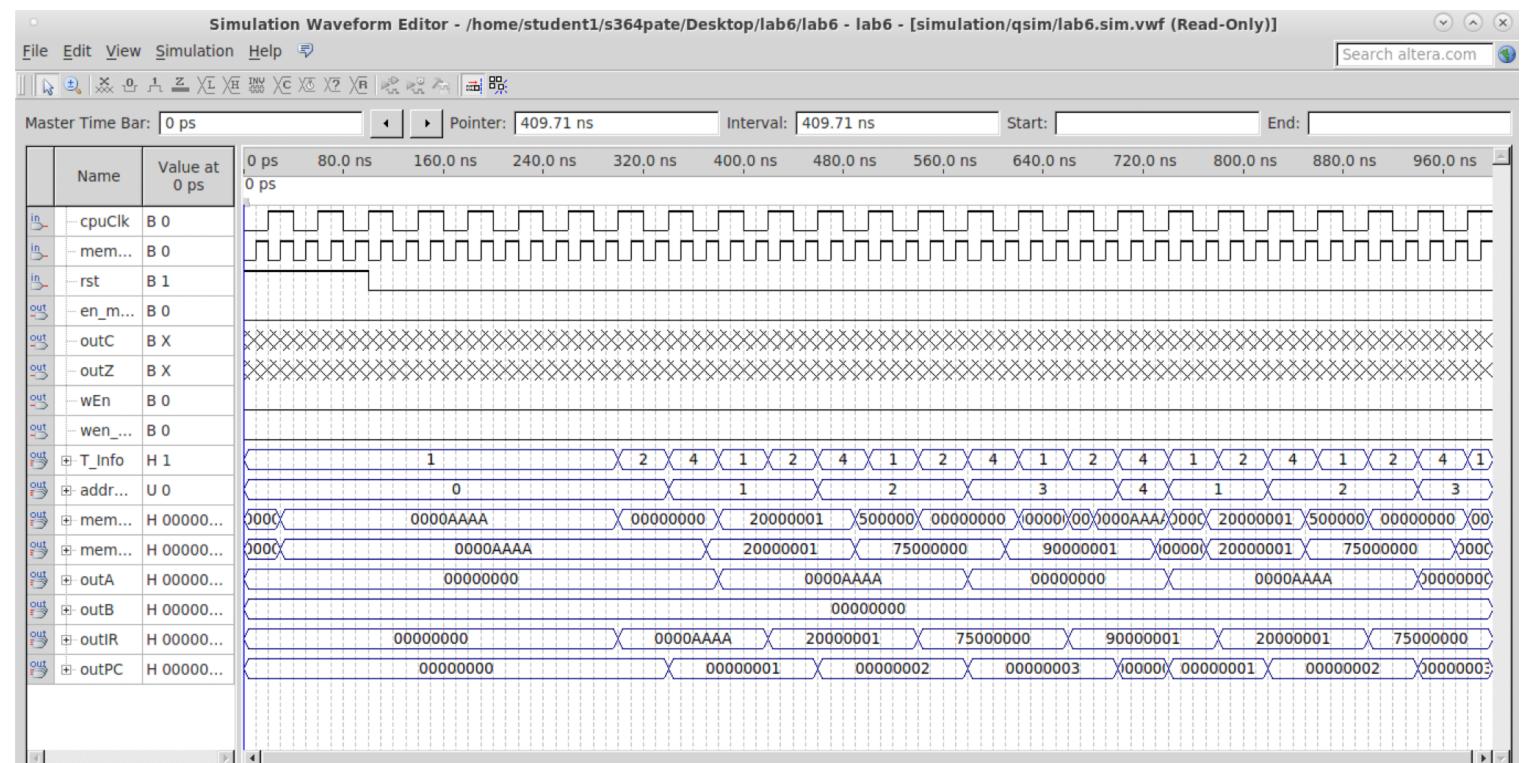
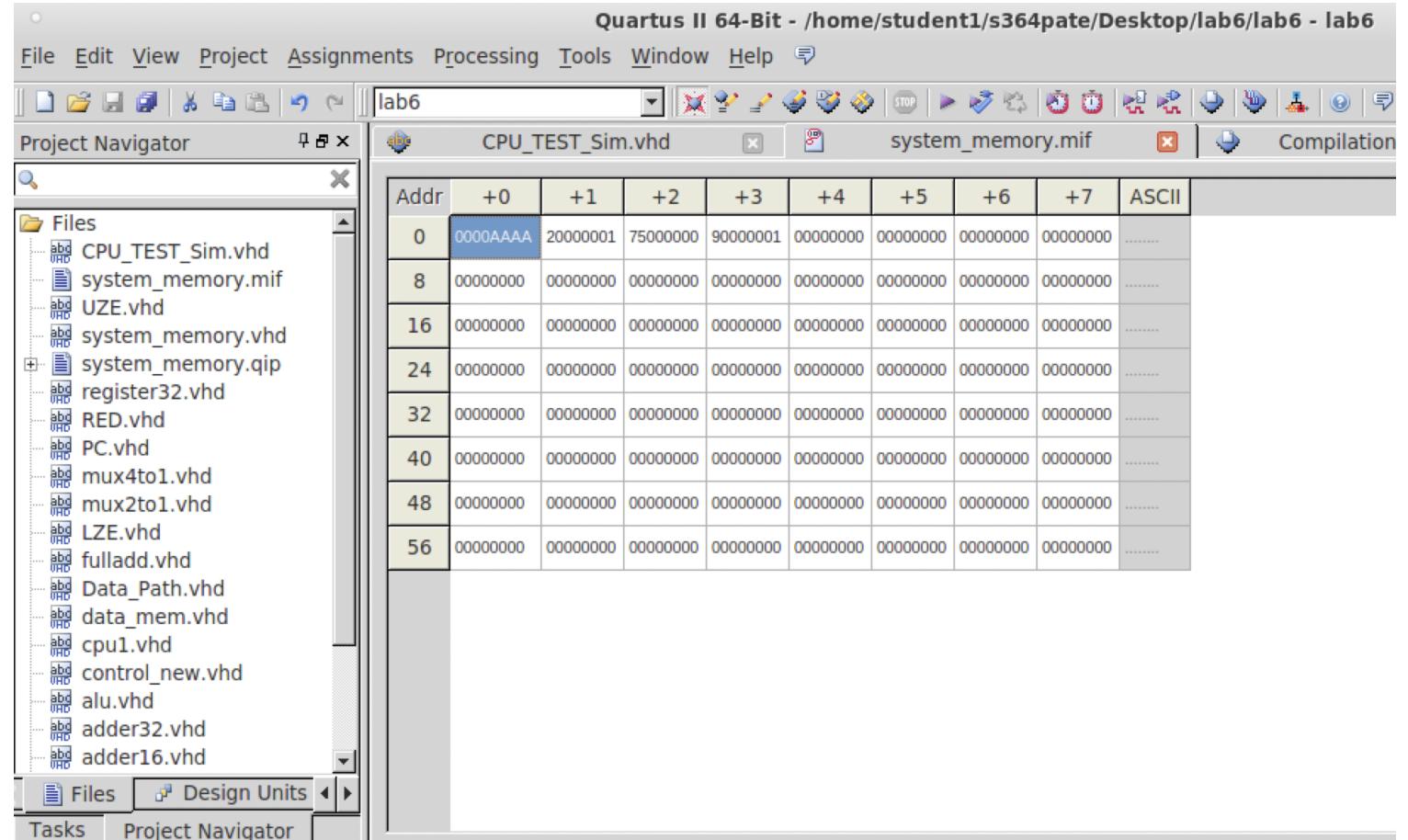
Submission Date:	Tuesday April 11 2023
Due Date:	Wednesday April 12 2023 3:00pm

Student LAST Name	Student FIRST Name	Student Number	Section	Signature*
Patel	Stuti		04	S.P

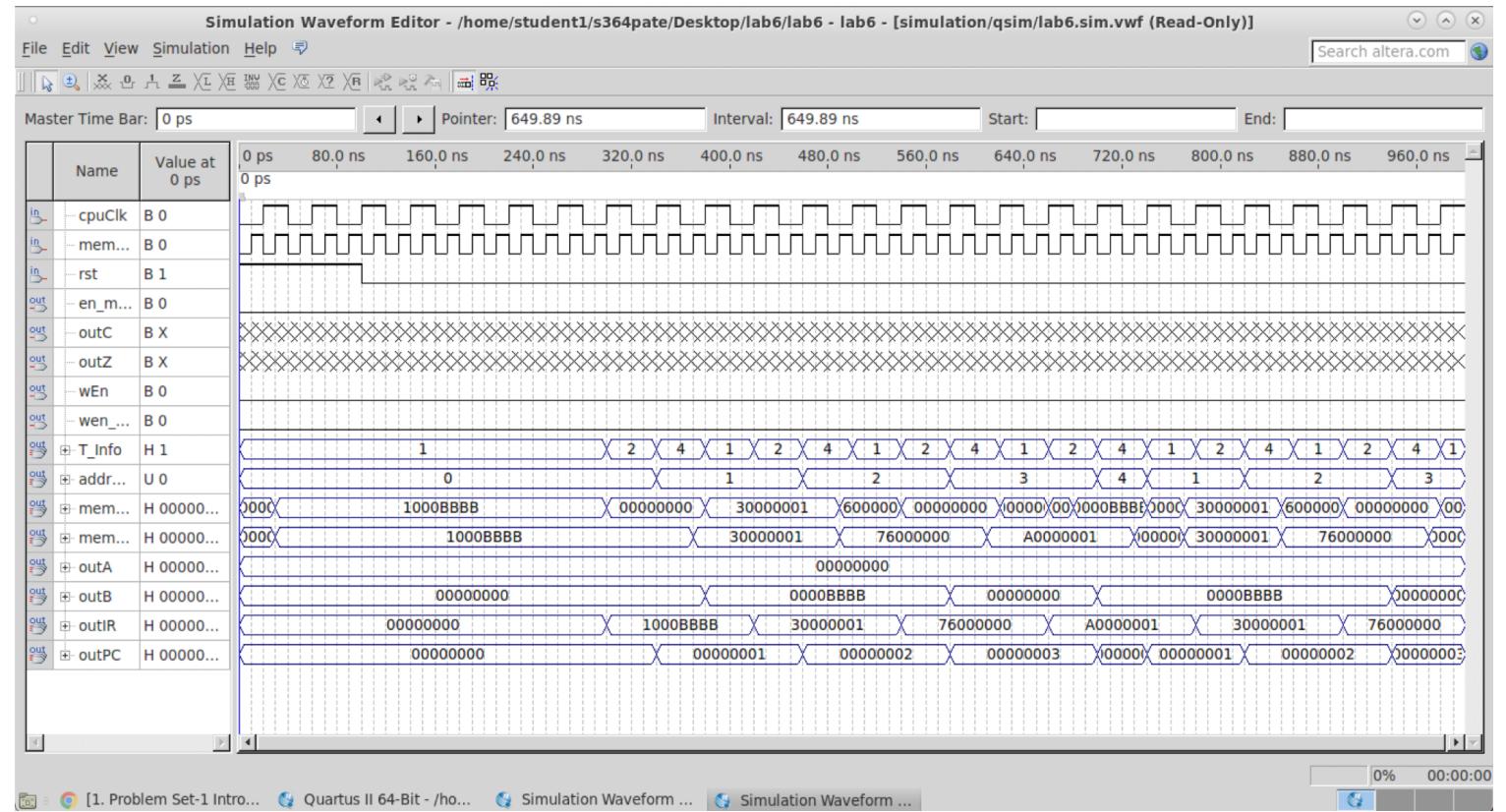
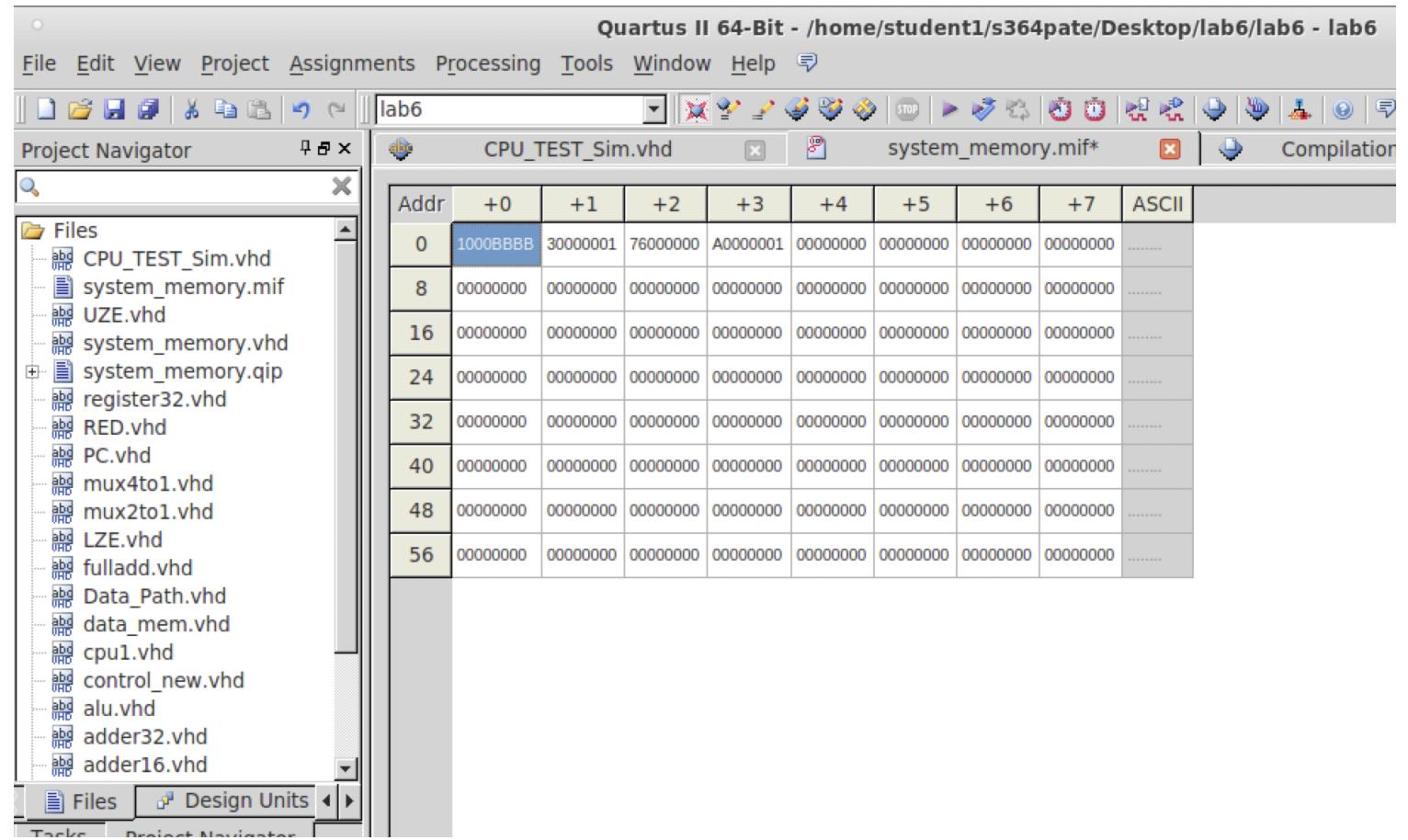
*By signing above you attest that you have contributed to this written lab report and confirm that all work you have contributed to this lab report is your own work. Any suspicion of copying or plagiarism in this work will result in an investigation of Academic Misconduct and may result in a "0" on the work, an "F" in the course, or possibly more severe penalties, as well as a Disciplinary Notice on your academic record under the Student Code of Academic Conduct, which can be found online at: <http://www.ryerson.ca/senate/current/pol60.pdf>

Functional Simulations

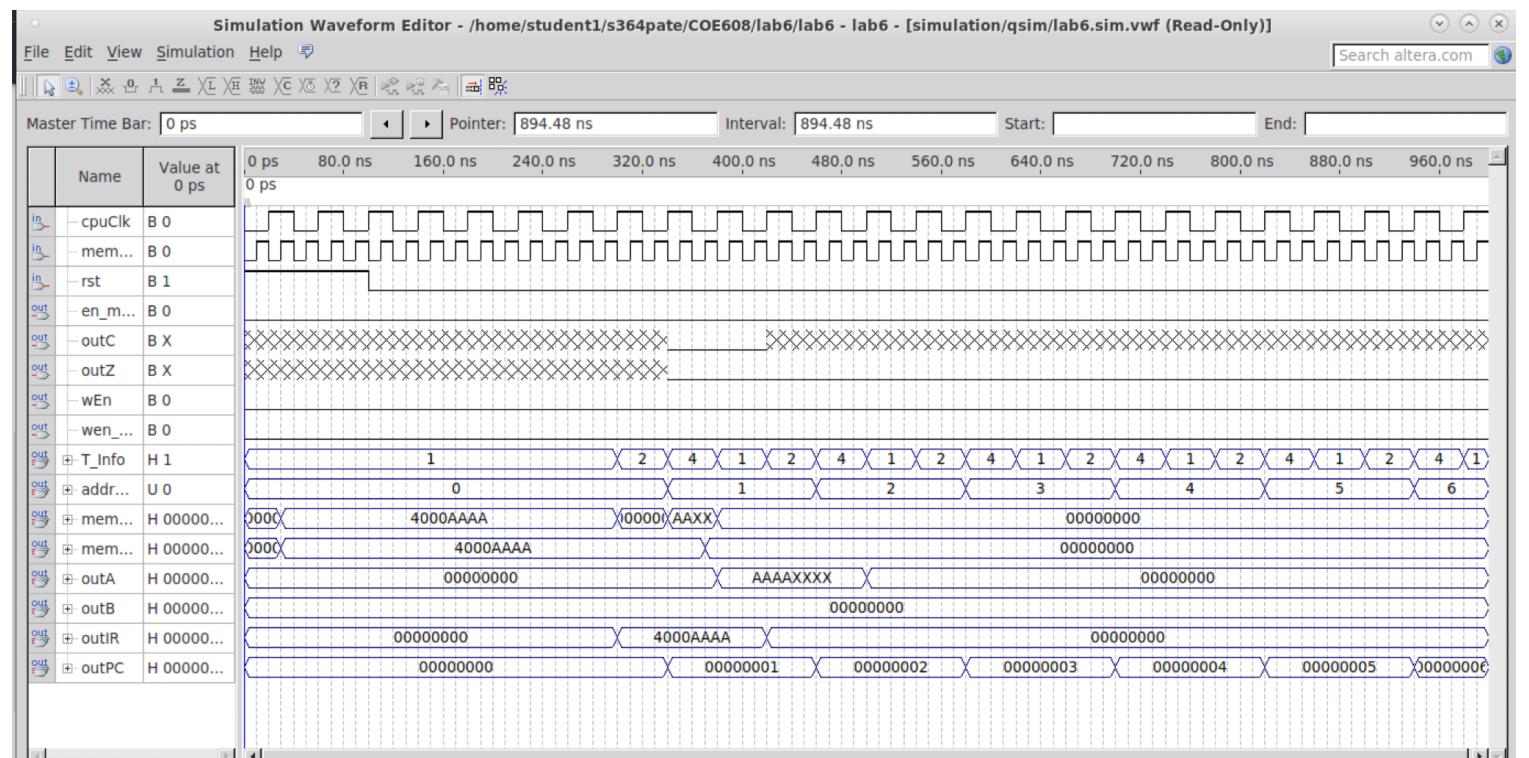
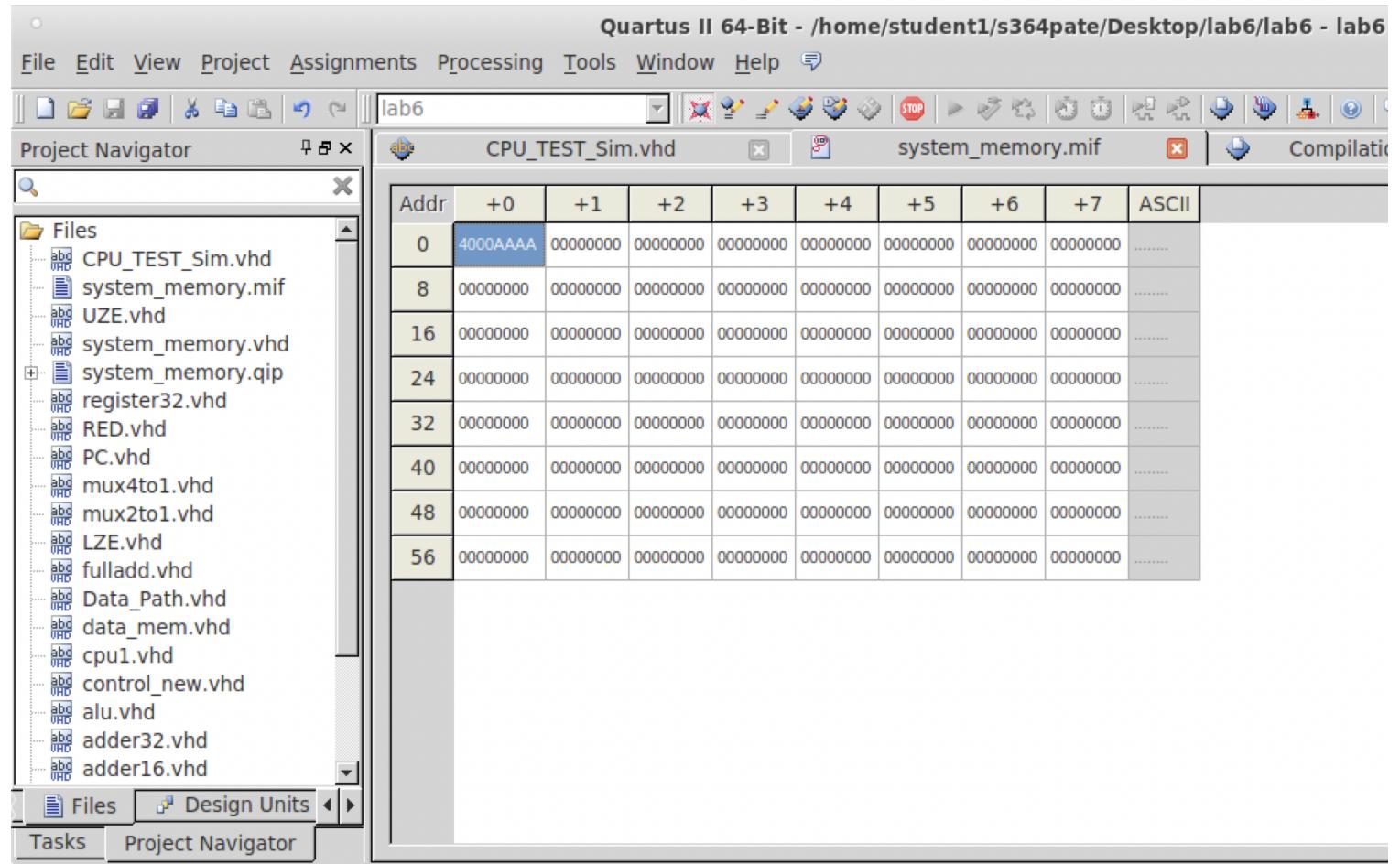
LDAI, STA, CLRA, LDA



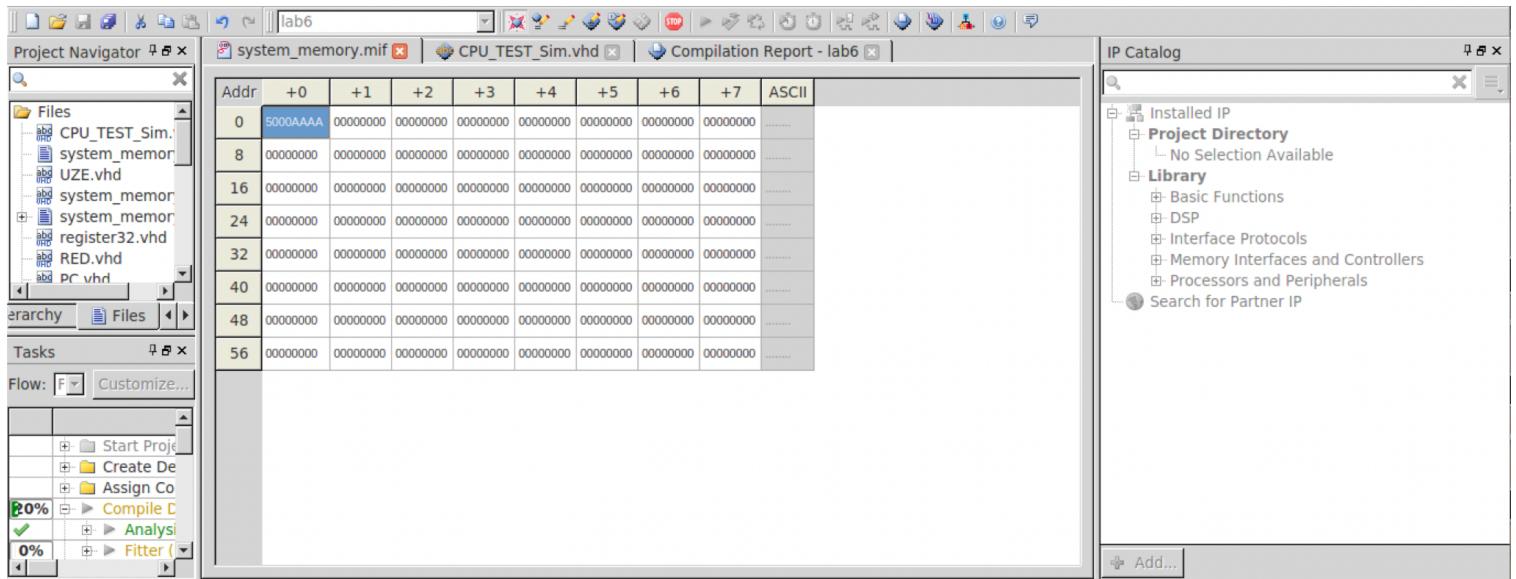
LDBI, STB, CLRb, LDB



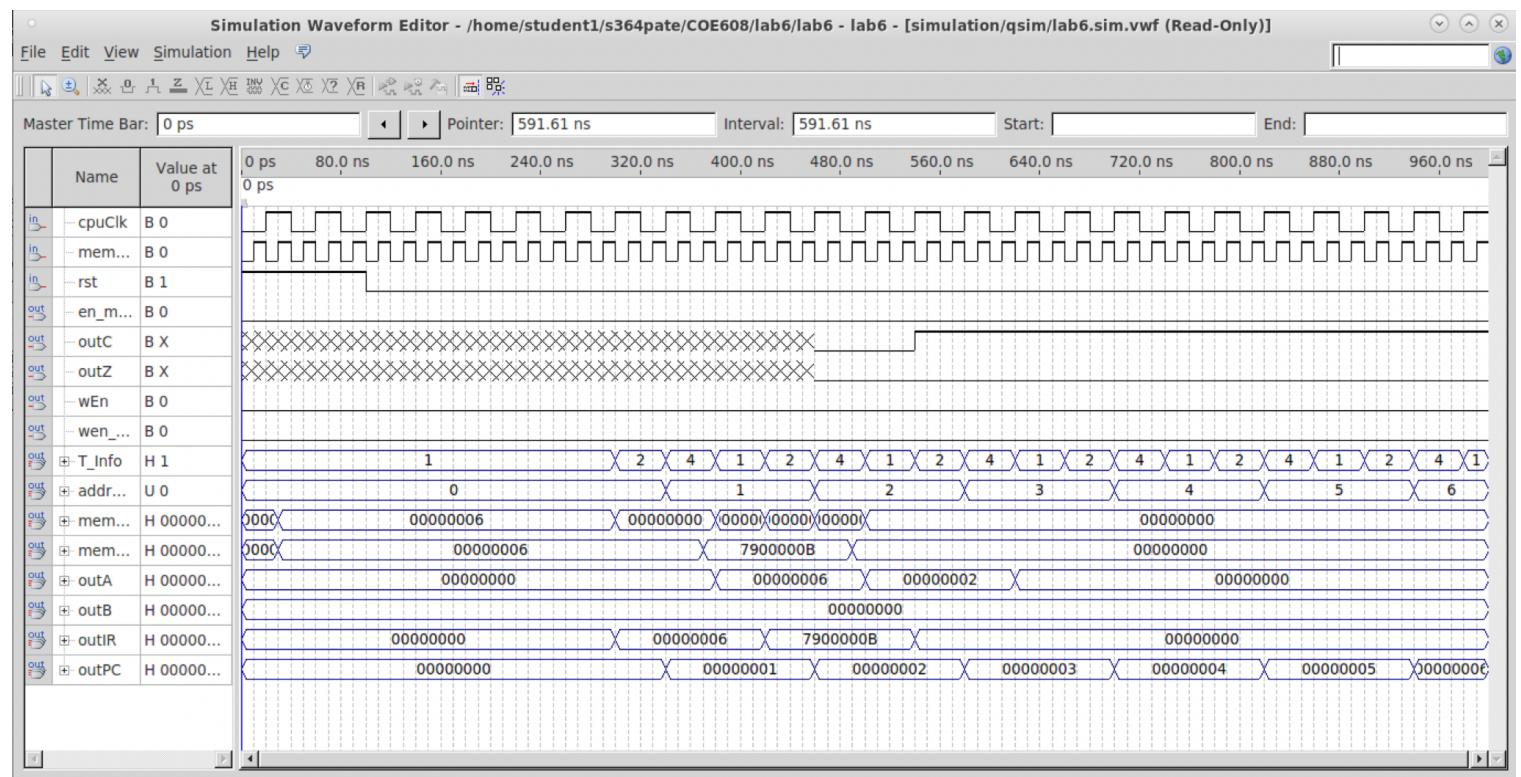
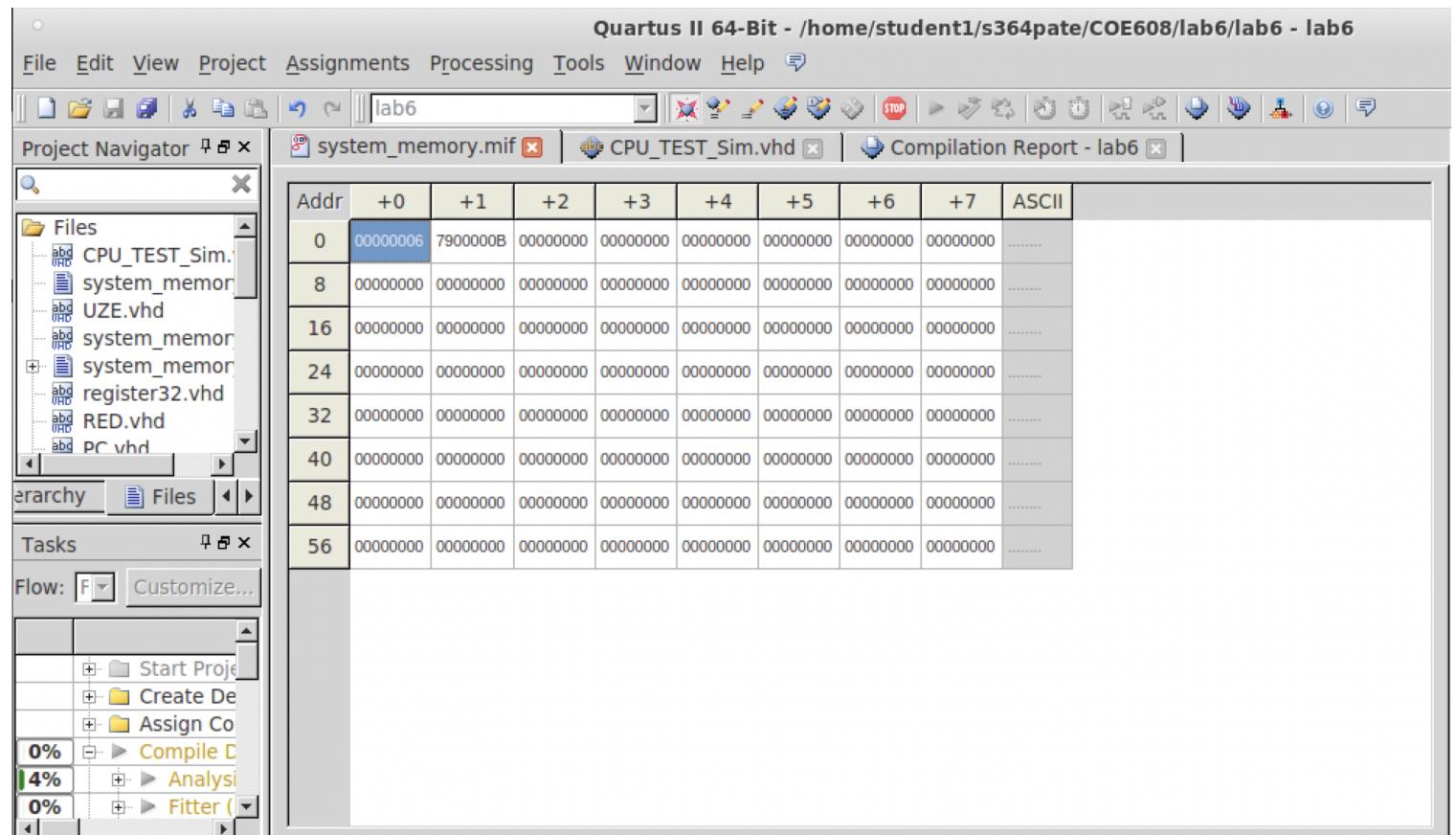
LUI



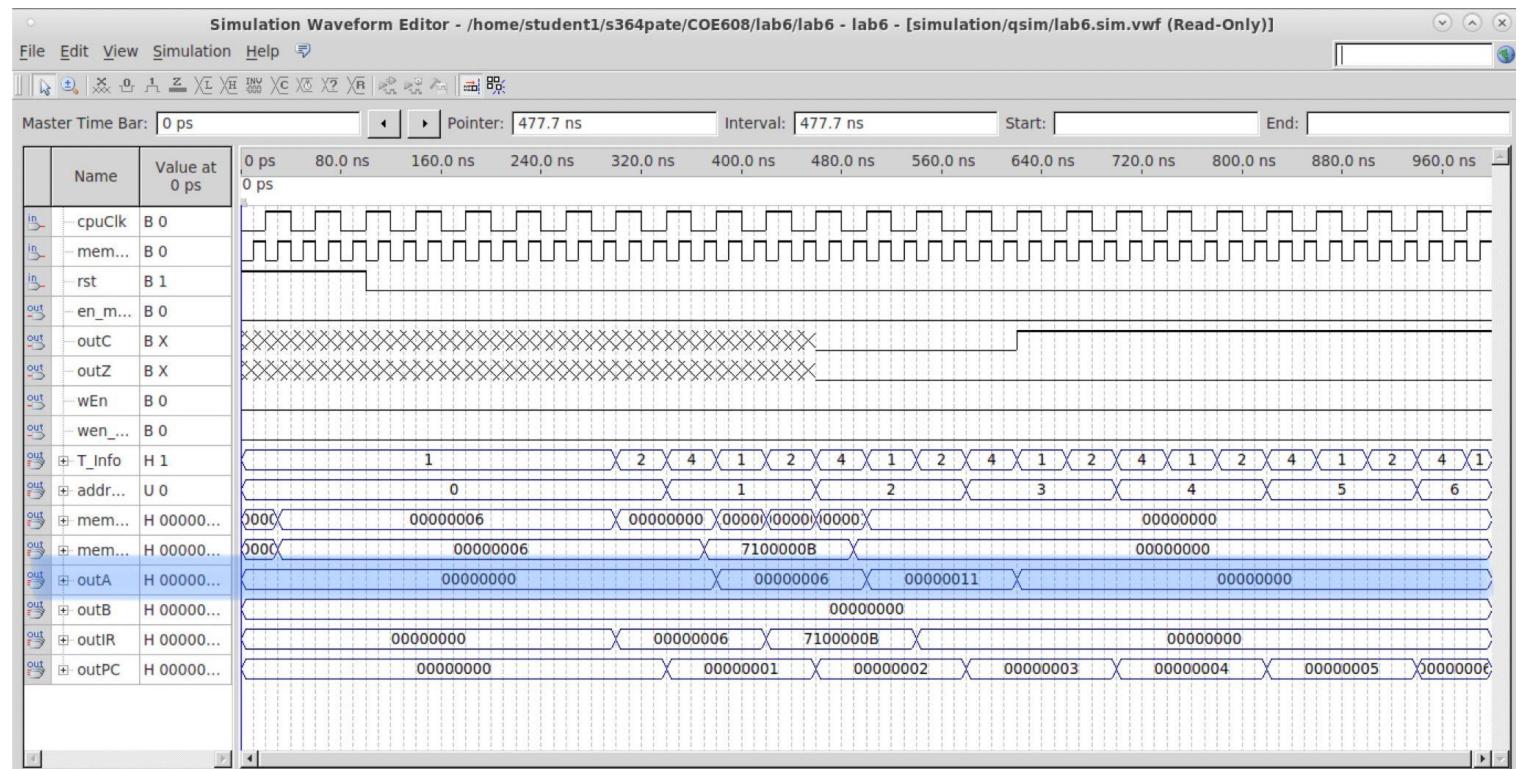
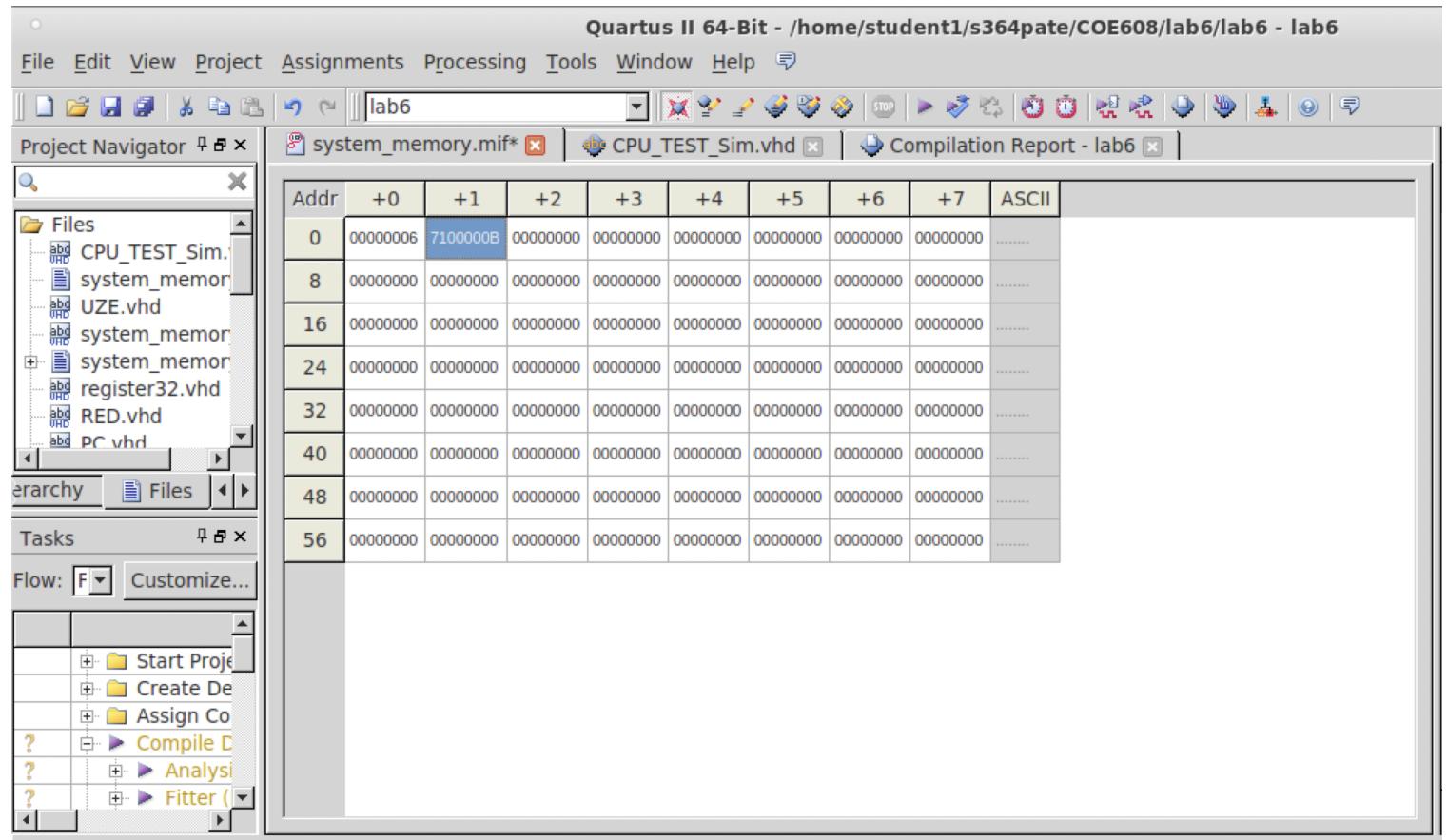
JMP



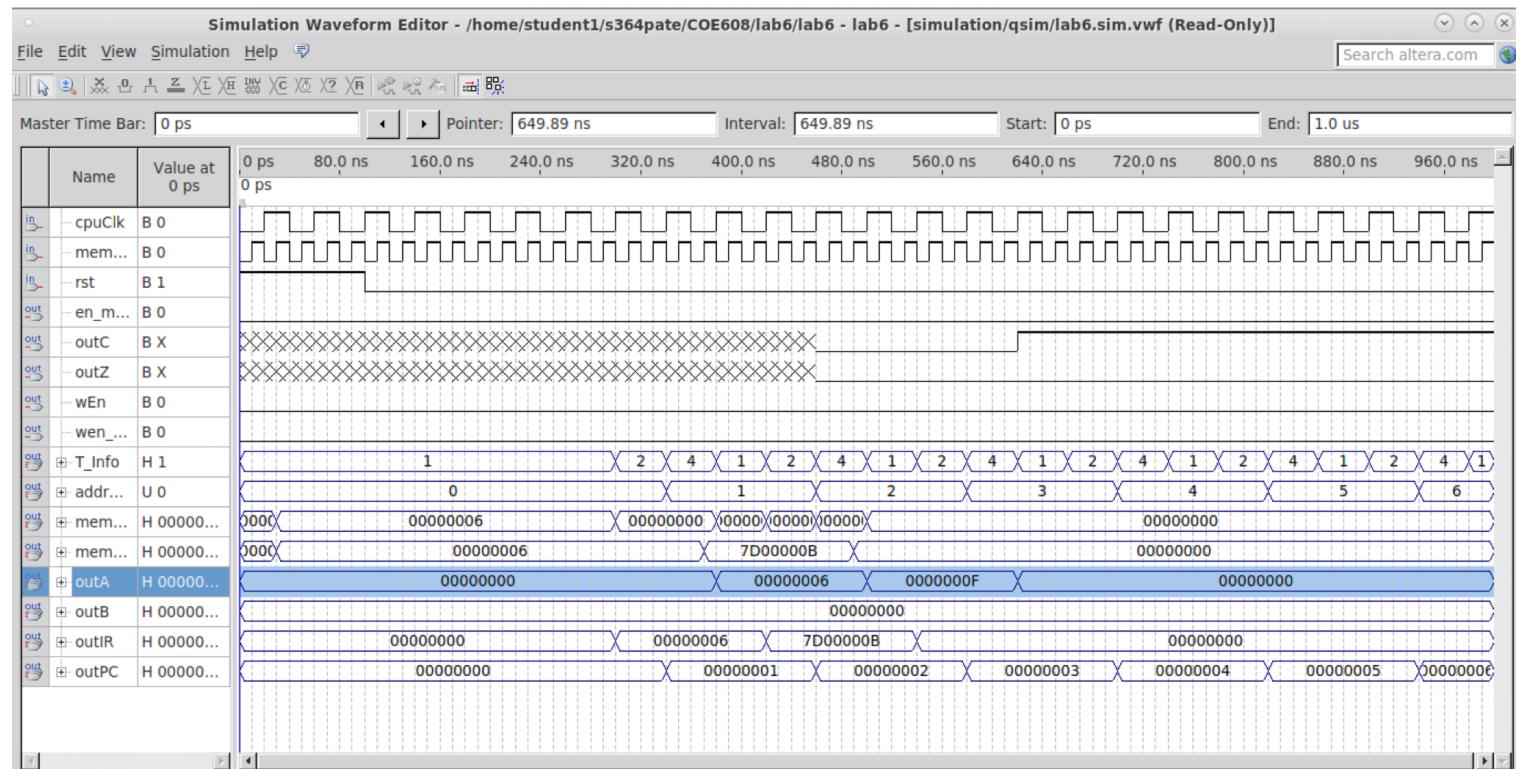
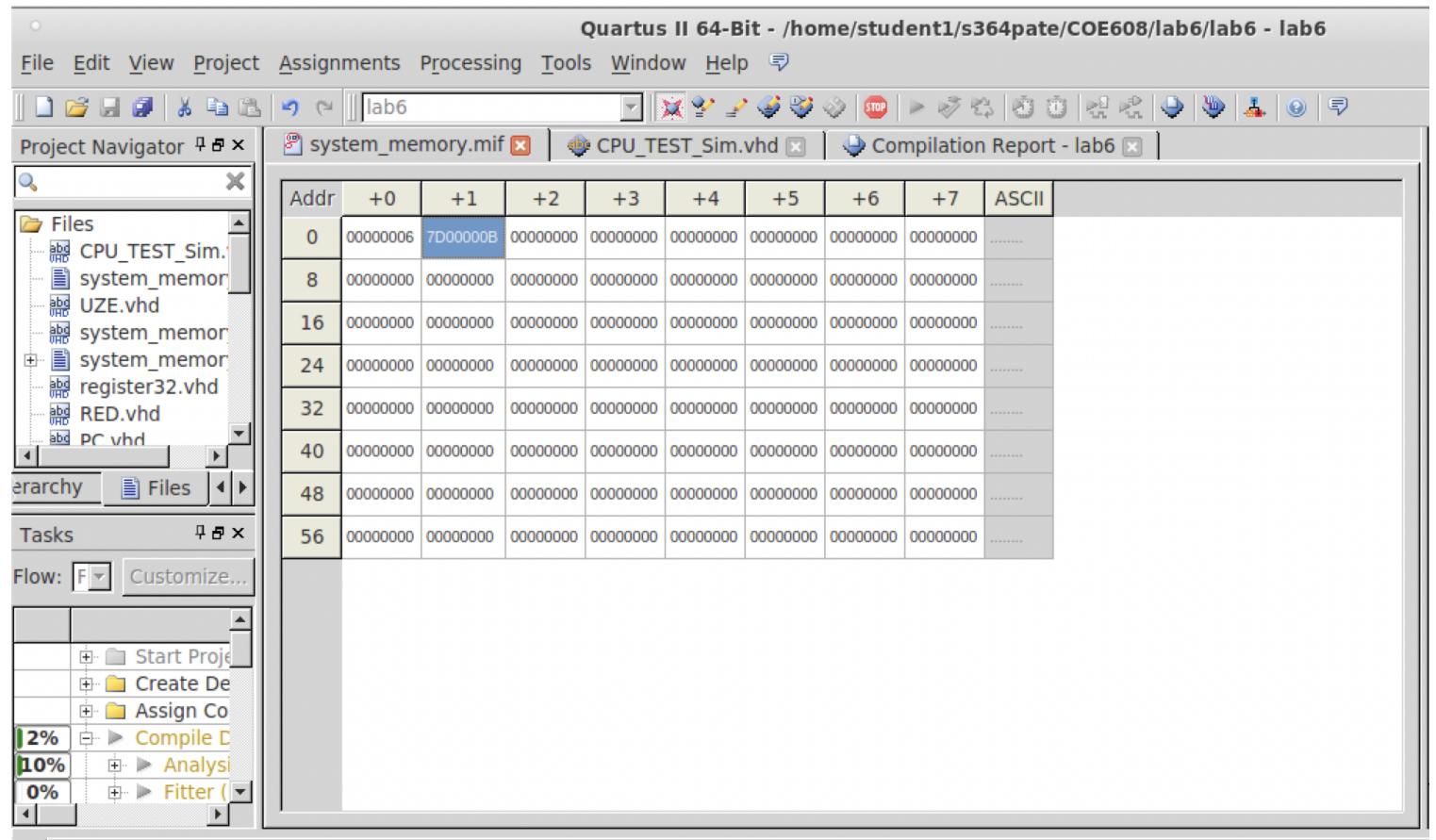
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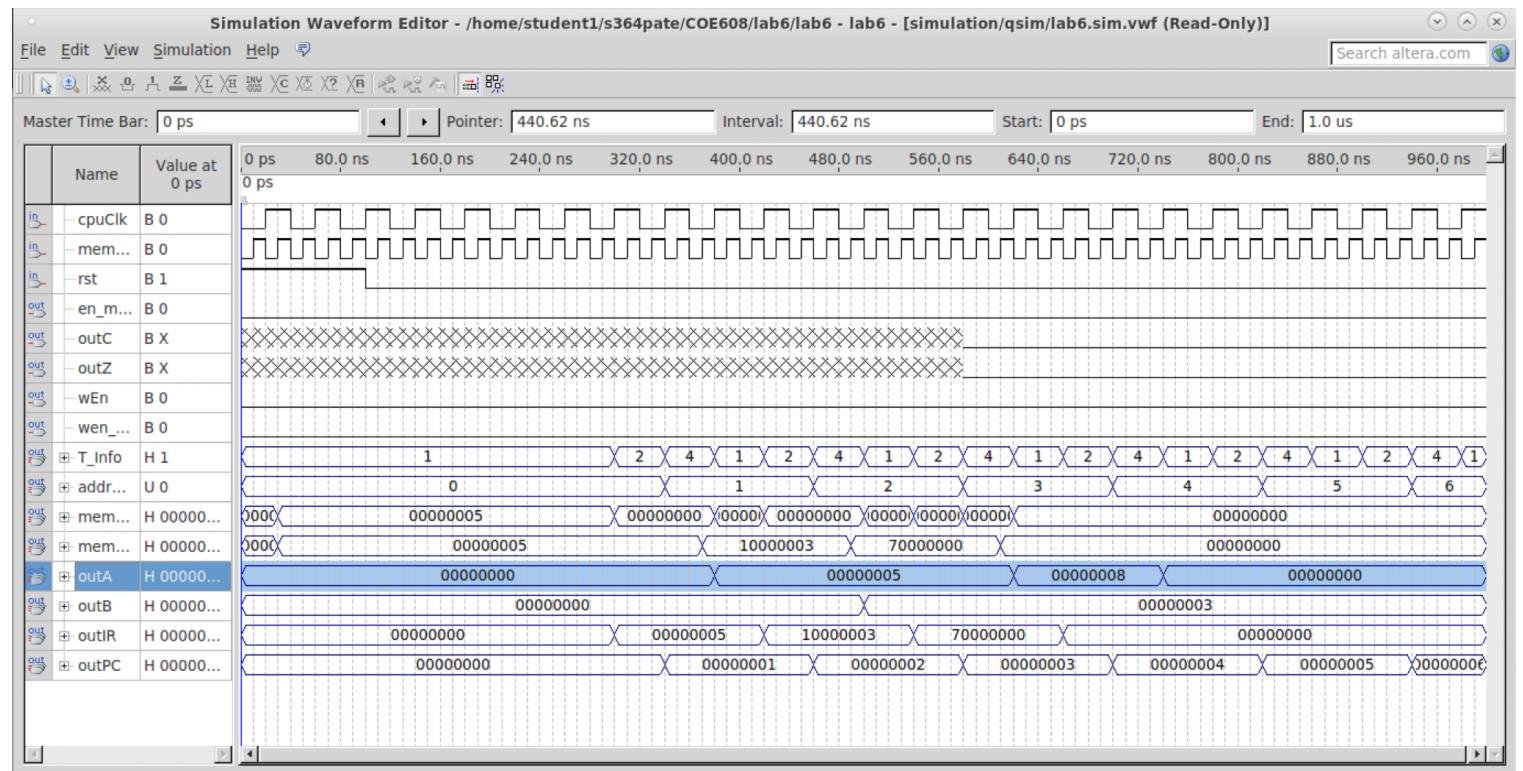
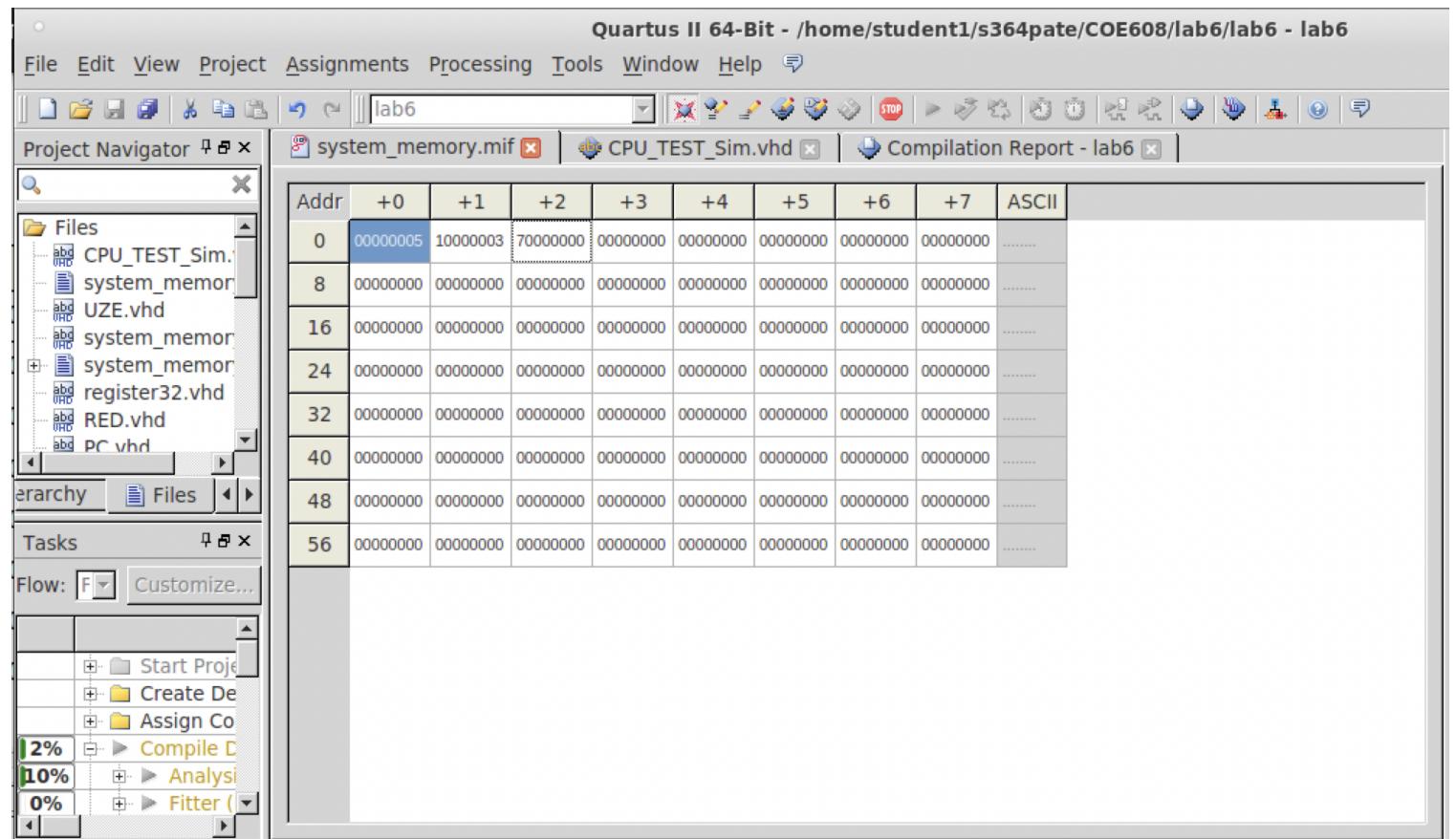
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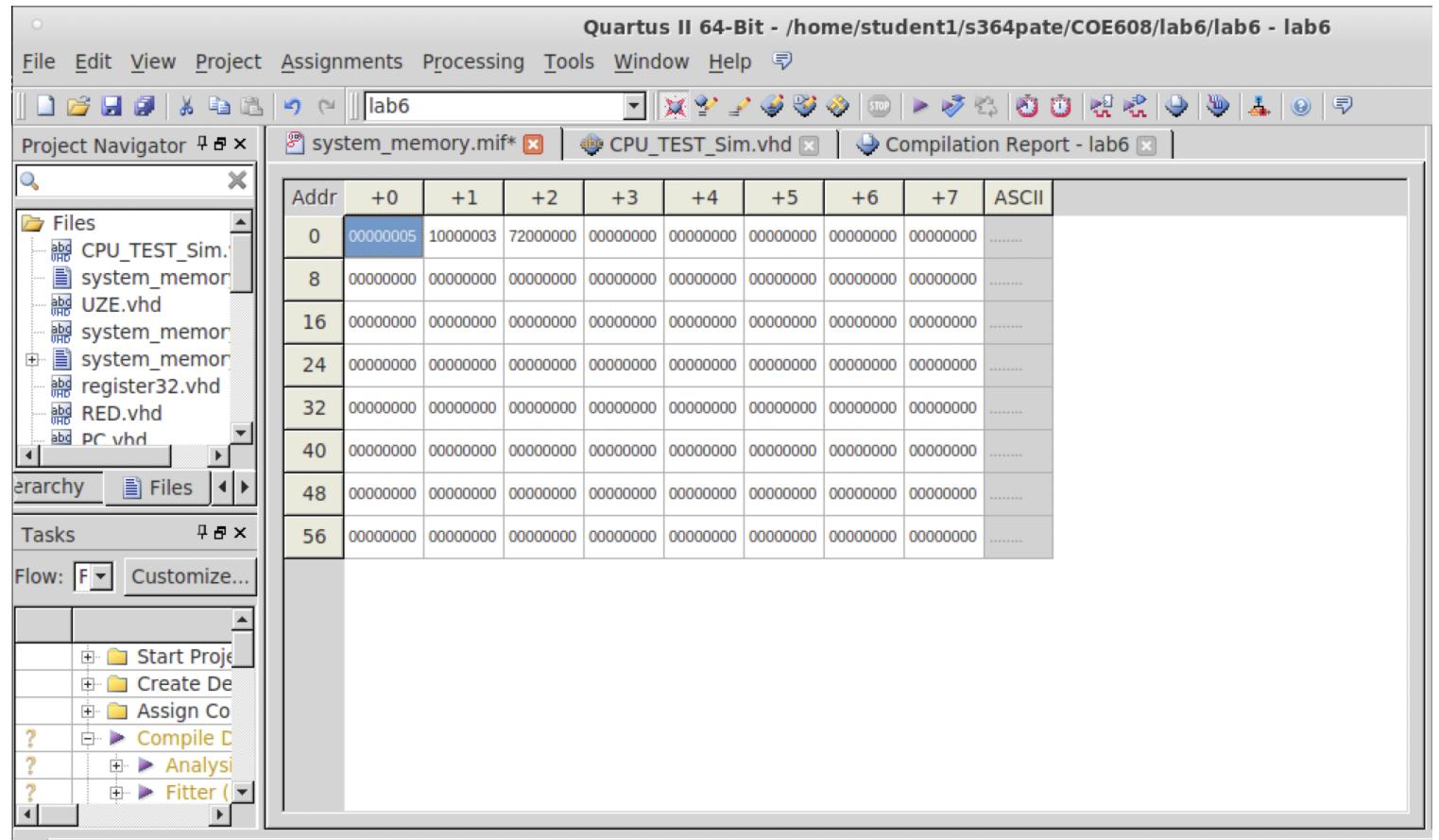
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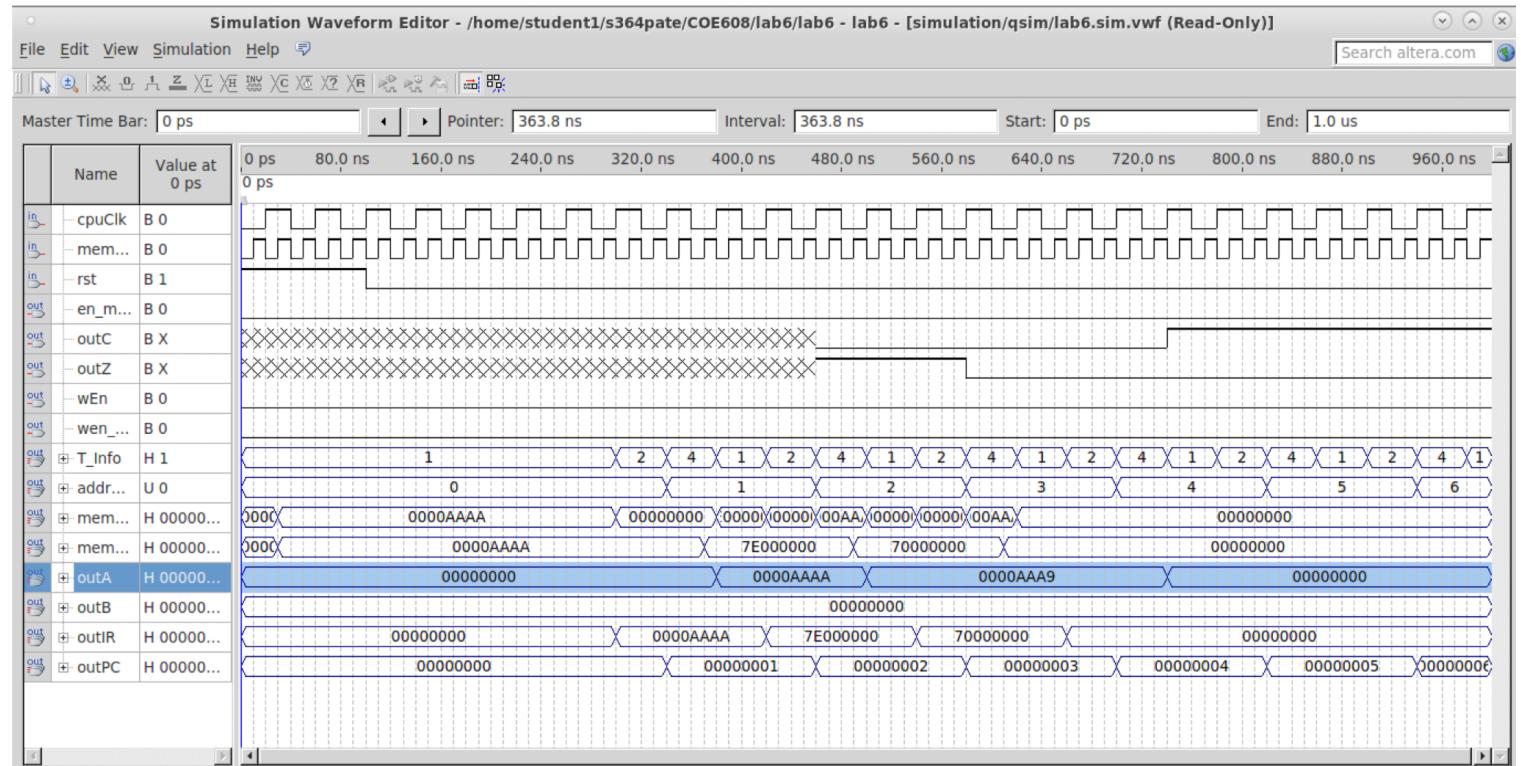
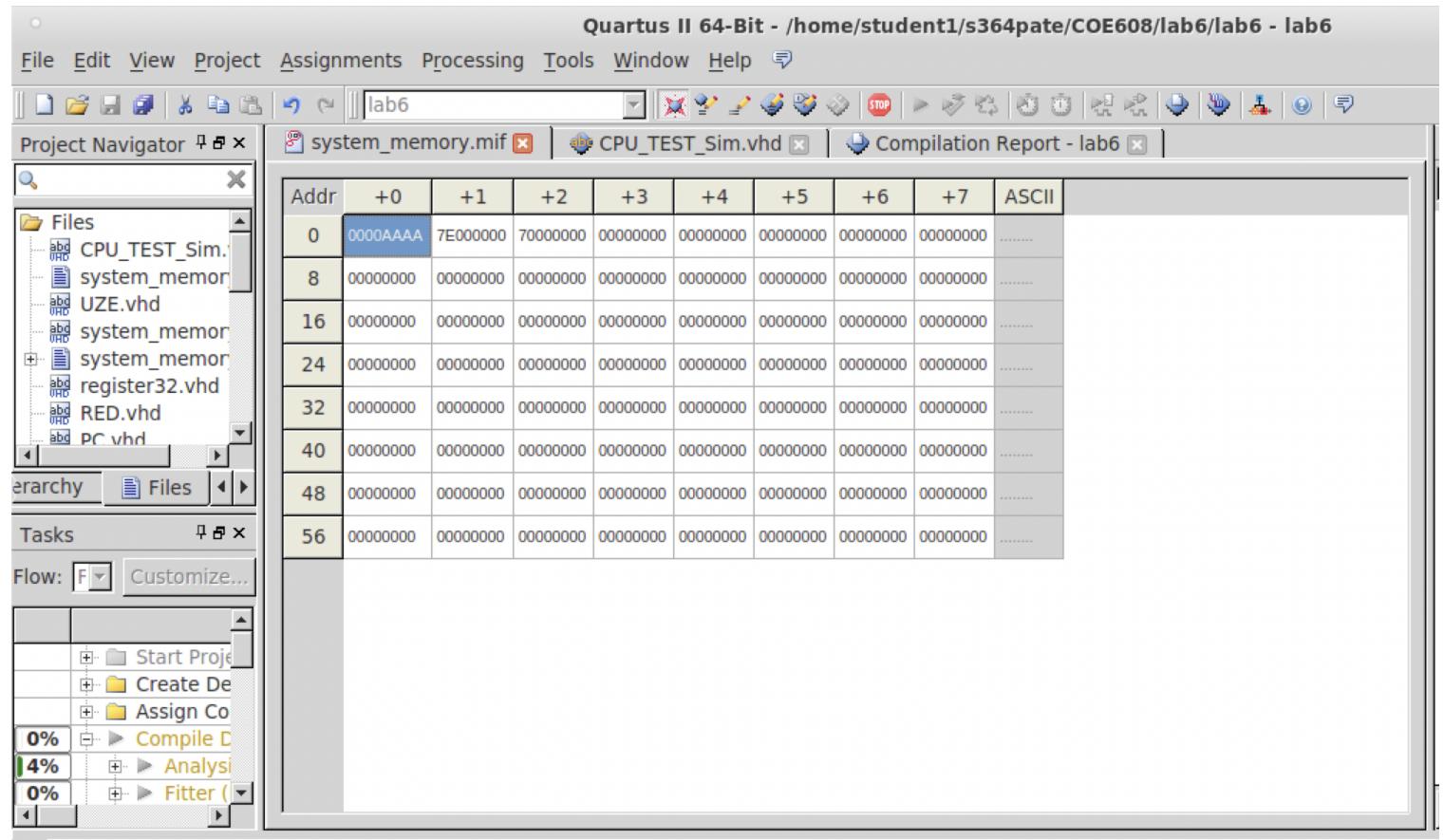
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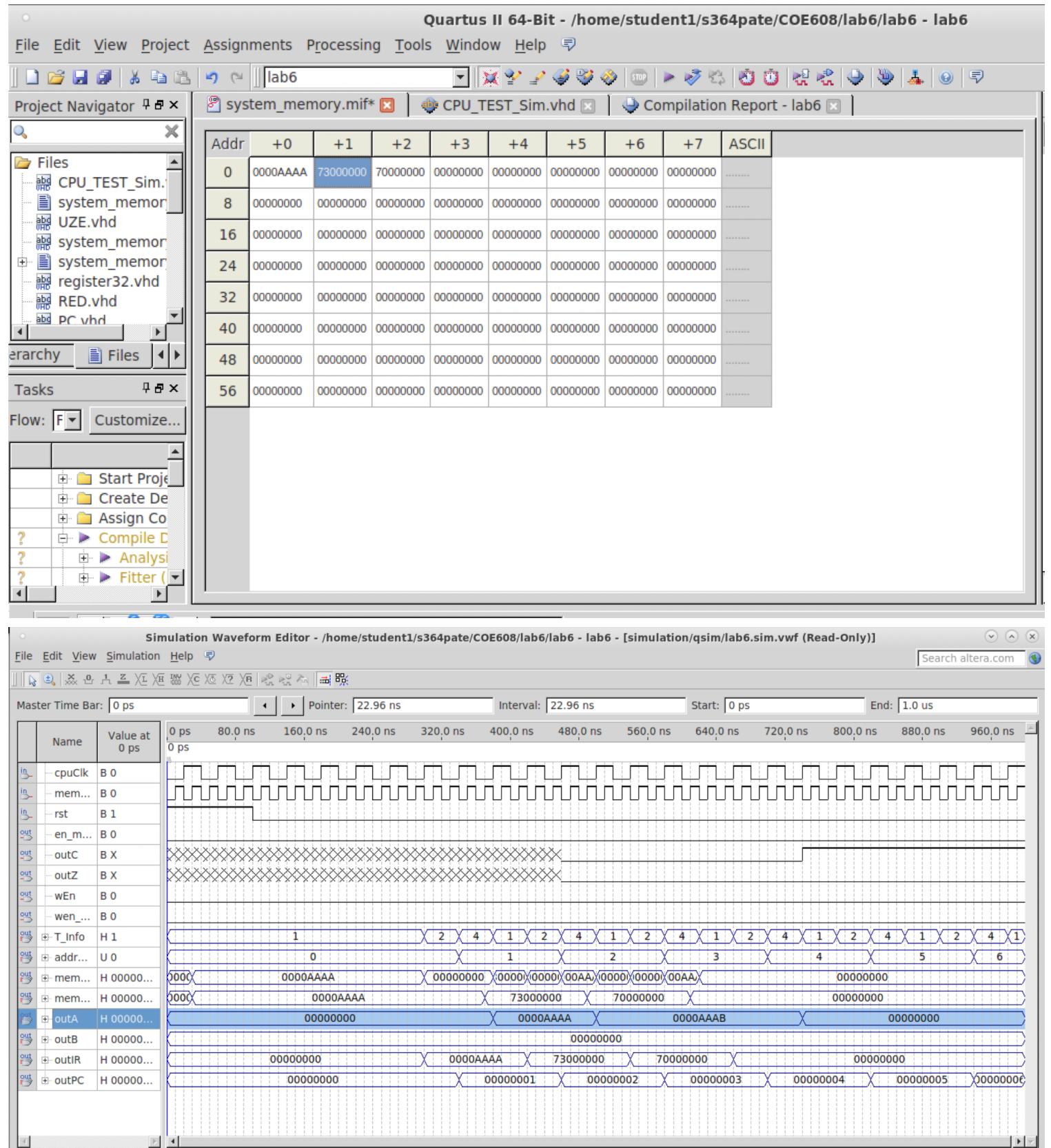
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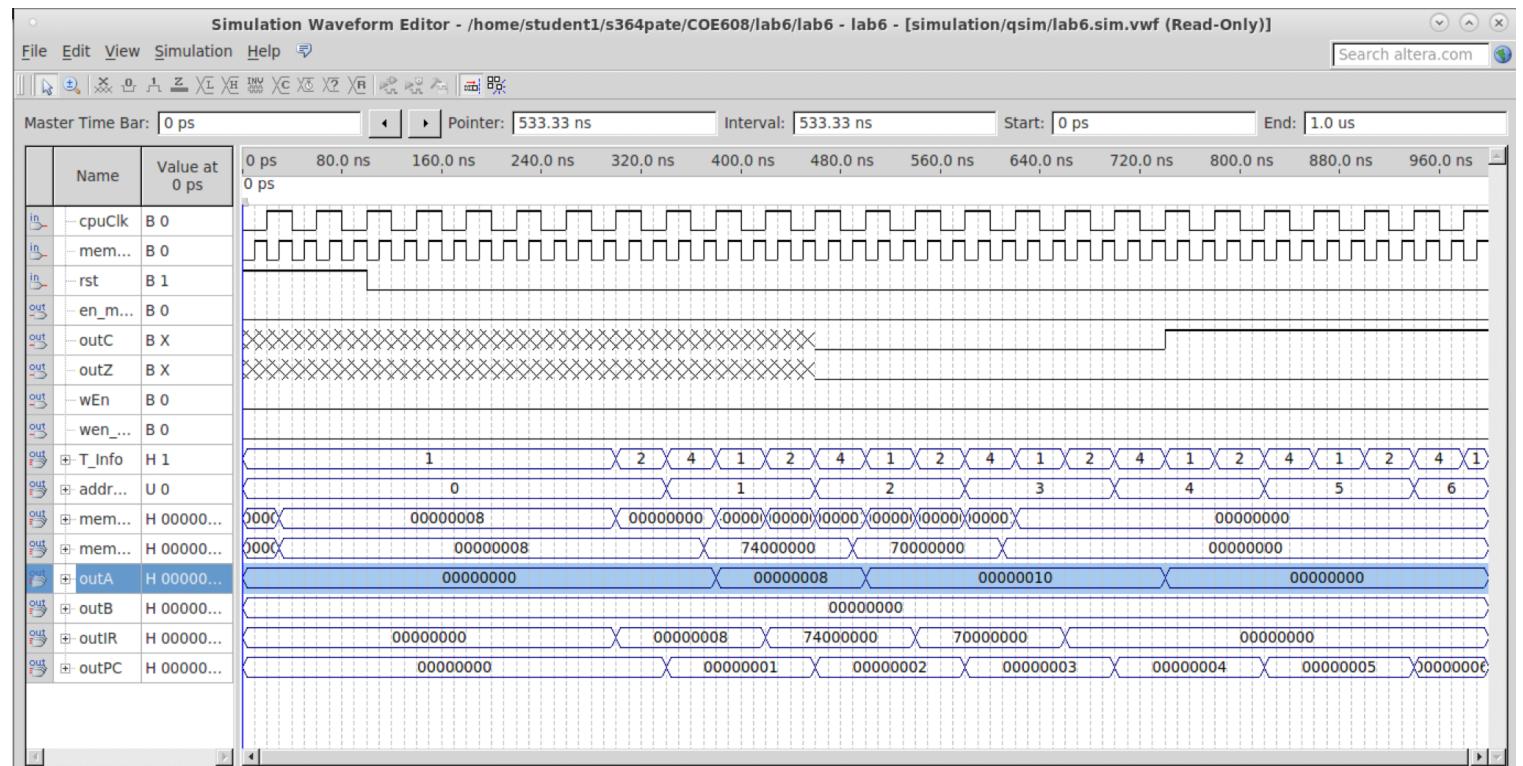
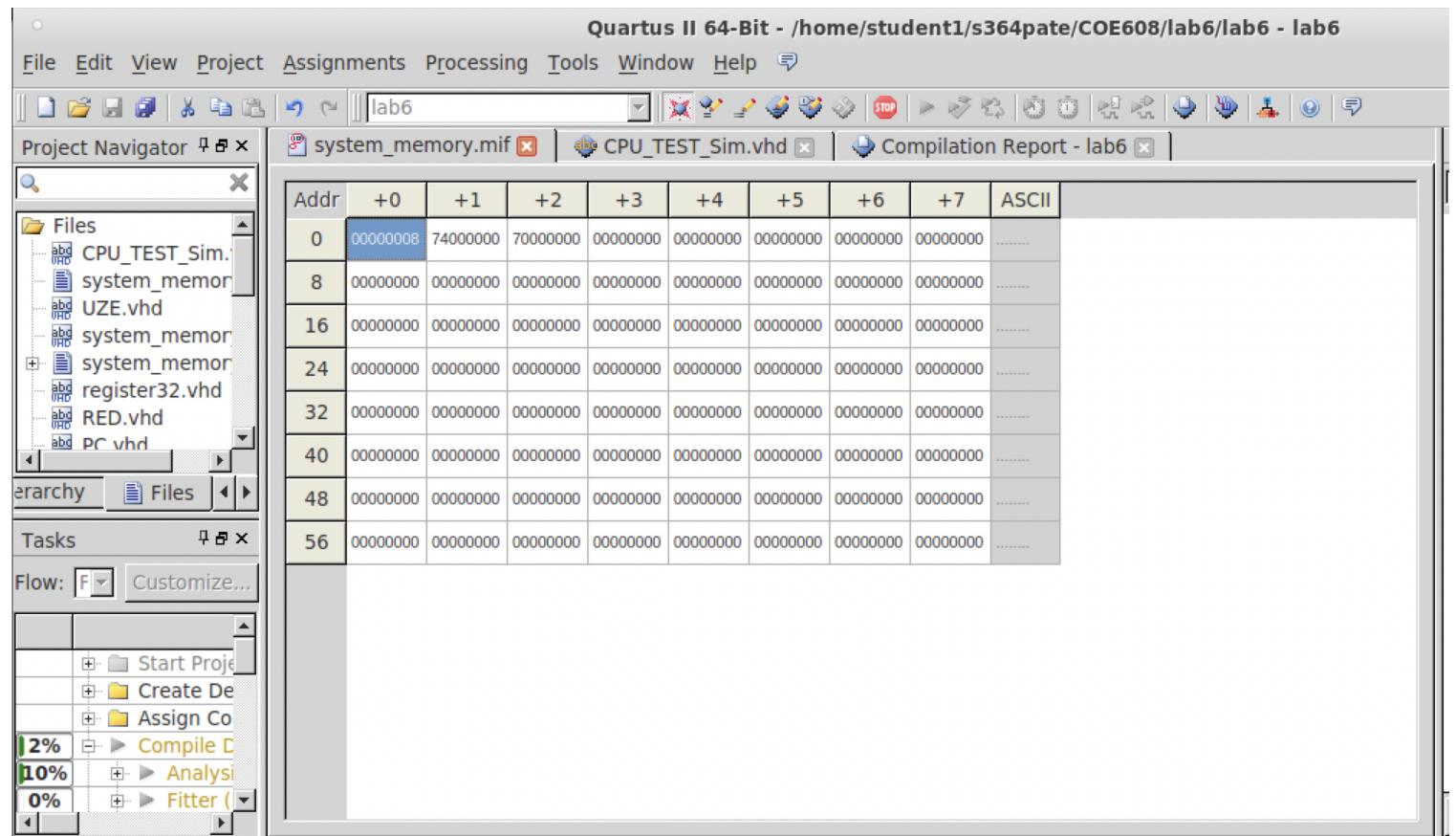
DECA



INCA



ROL



ROR

Quartus II 64-Bit - /home/student1/s364pate/COE608/lab6/lab6 - lab6

File Edit View Project Assignments Processing Tools Window Help

Project Navigator | system_memory.mif* | CPU_TEST_Sim.vhd | Compilation Report - lab6

Files

- CPU_TEST_Sim.vhd
- system_memory.mif
- UZE.vhd
- system_memory.mif
- system_memory.mif
- register32.vhd
- RED.vhd
- PC.vhd

Tasks

- Start Project
- Create Design
- Assign Constraints
- Compile Design
- Analysis
- Fitter

Flow: Customize...

26% Done

0% Done

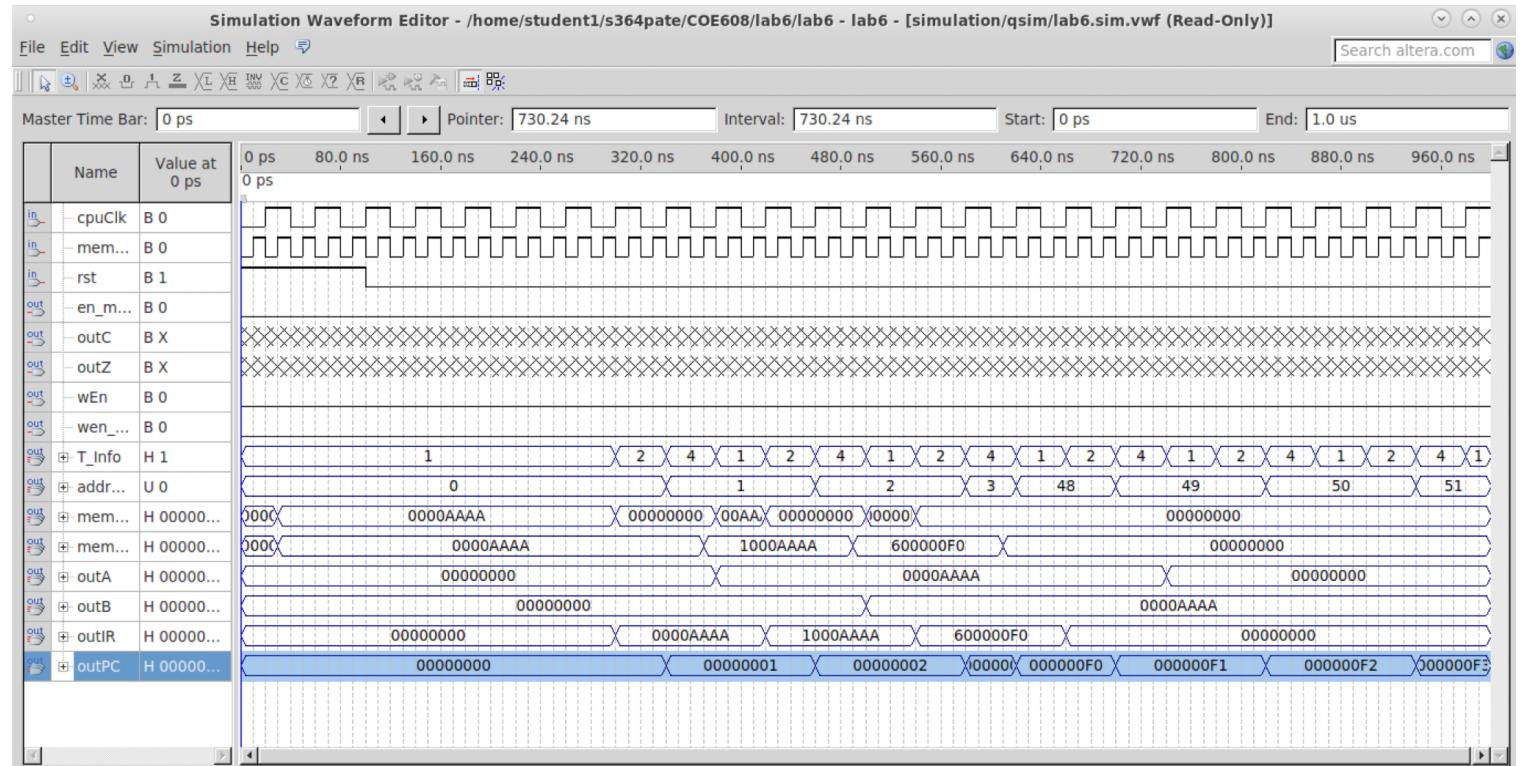
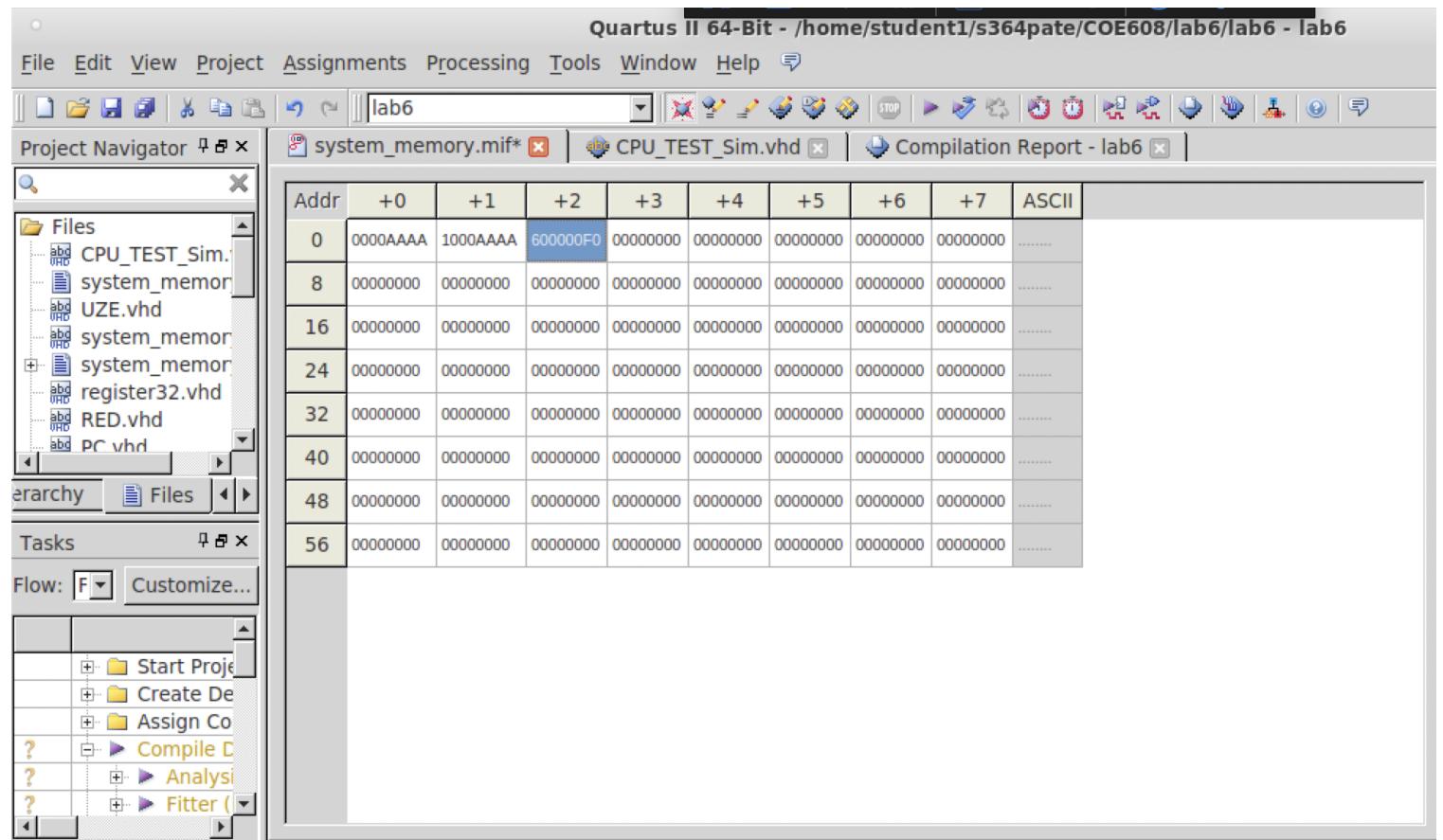
Simulation Waveform Editor - /home/student1/s364pate/COE608/lab6/lab6 - [simulation/qsim/lab6.sim.vwf (Read-Only)]

File Edit View Simulation Help

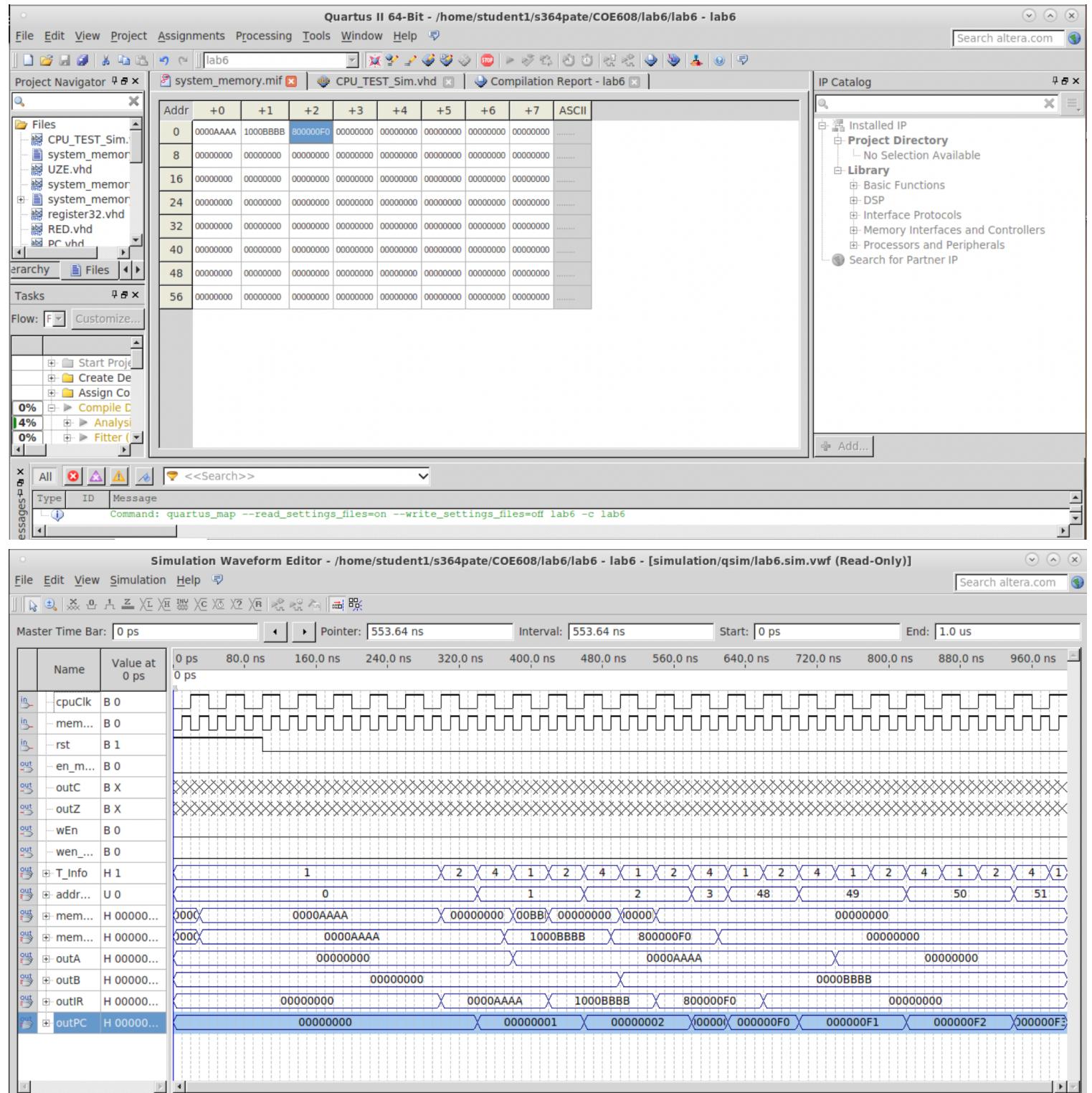
Master Time Bar: 0 ps Pointer: 350.55 ns Interval: 350.55 ns Start: 0 ps End: 1.0 us

Name	Value at 0 ps	0 ps	80.0 ns	160.0 ns	240.0 ns	320.0 ns	400.0 ns	480.0 ns	560.0 ns	640.0 ns	720.0 ns	800.0 ns	880.0 ns	960.0 ns
cpuClk	B 0													
mem...	B 0													
rst	B 1													
en_m...	B 0													
outC	B X													
outZ	B X													
wEn	B 0													
wen...	B 0													
T_Info	H 1	1	X	2	4	1	2	4	1	2	4	1	2	4
addr...	U 0	0	X	1	X	2	X	3	X	4	X	5	X	6
mem...	H 00000...	00000008	X	00000000	X	00000000	X	00000000	X	00000000	X	00000000	X	00000000
mem...	H 00000...	00000008	X	74000000	X	70000000	X	00000000	X	00000000	X	00000000	X	00000000
outA	H 00000...	00000000	X	00000008	X	00000010	X	00000000	X	00000000	X	00000000	X	00000000
outB	H 00000...	00000000	X	00000008	X	74000000	X	70000000	X	00000000	X	00000000	X	00000000
outIR	H 00000...	00000000	X	00000001	X	00000002	X	00000003	X	00000004	X	00000005	X	00000006
outPC	H 00000...	00000000	X	00000001	X	00000002	X	00000003	X	00000004	X	00000005	X	00000006

BEQ



BNE



Conclusion

In conclusion, this lab project aimed to implement a complete CPU system by combining the data path and control components designed in previous labs with a reset circuit. The reset circuit was designed to ensure proper functionality of the CPU by clearing the program counter and allowing the data surrounding the CPU to stabilize before operation begins.