Course Number	COE608
Course Title	Computer Organization and Architecture
semester/year	Winter 2023
Instructor	Demetres Kostas
TA Name	Tasnim Prova

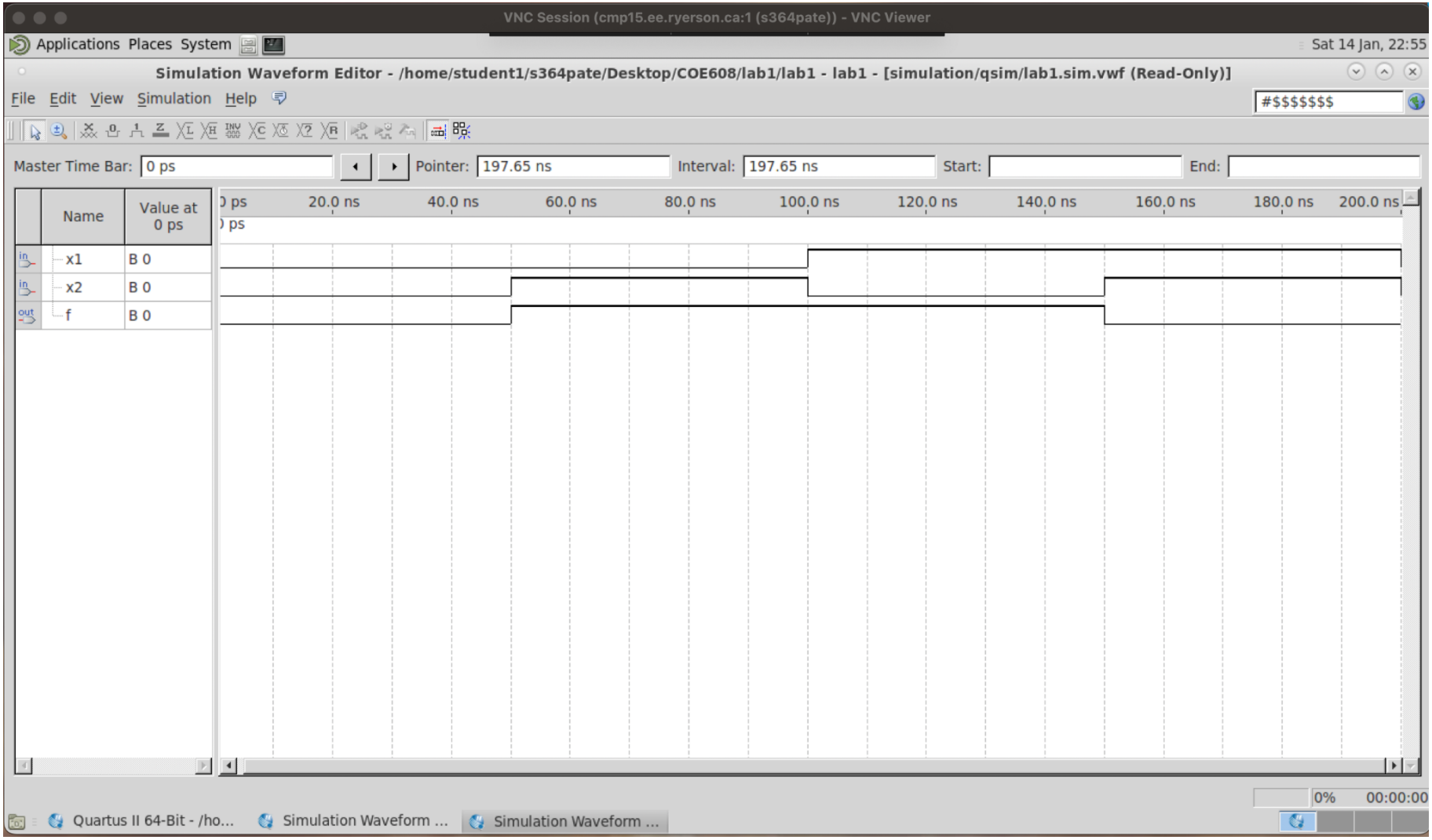
Lab report No.	1

Report Title	Introduction to Quartus-II by a VHDL Based Design

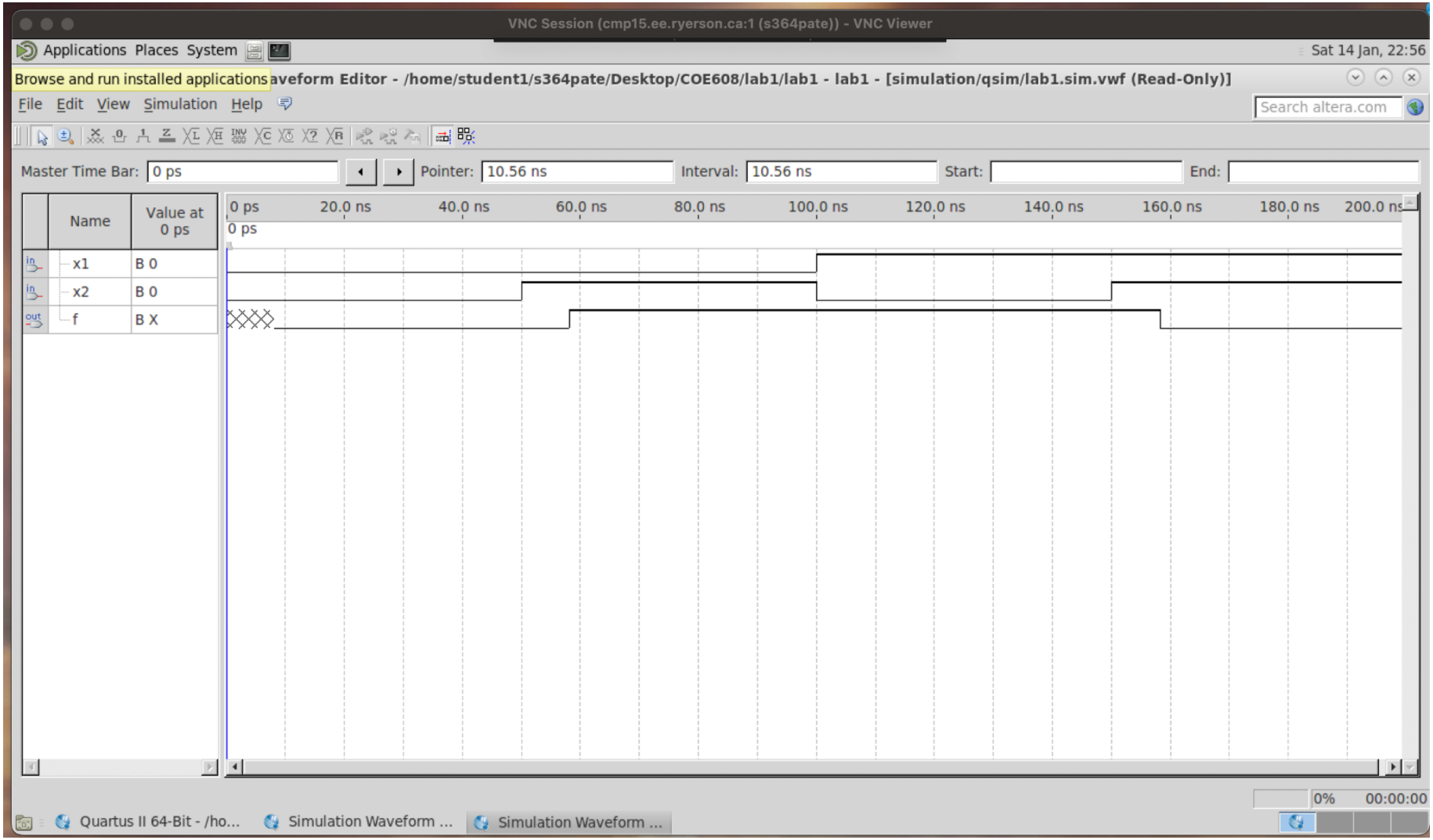
Section number	04
Submission date	
Due date	January 20 2023

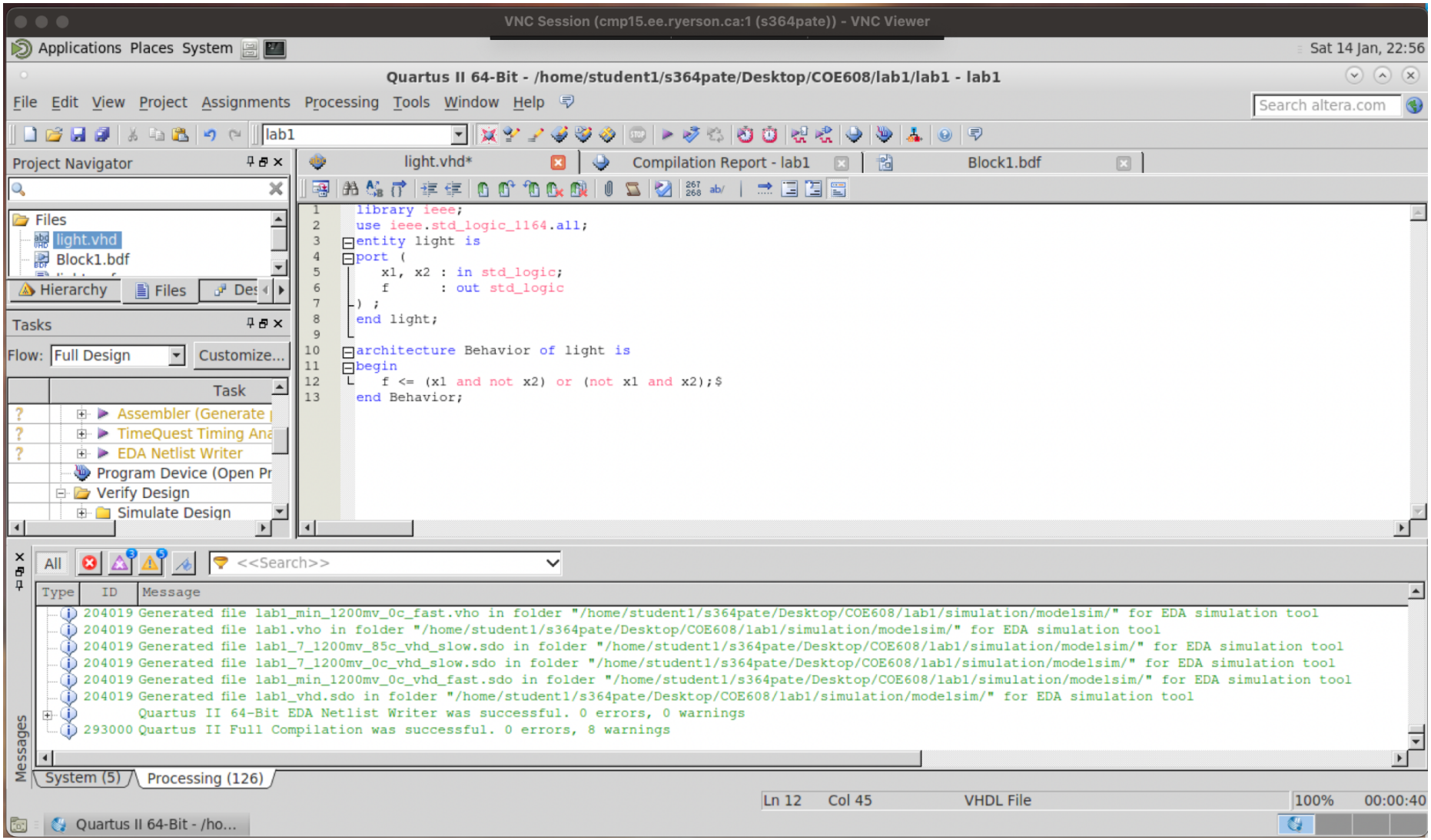
Student Name	Student ID	Signature/Initials
Stuti Patel		SP

Functional Diagram



Time Functional Diagram

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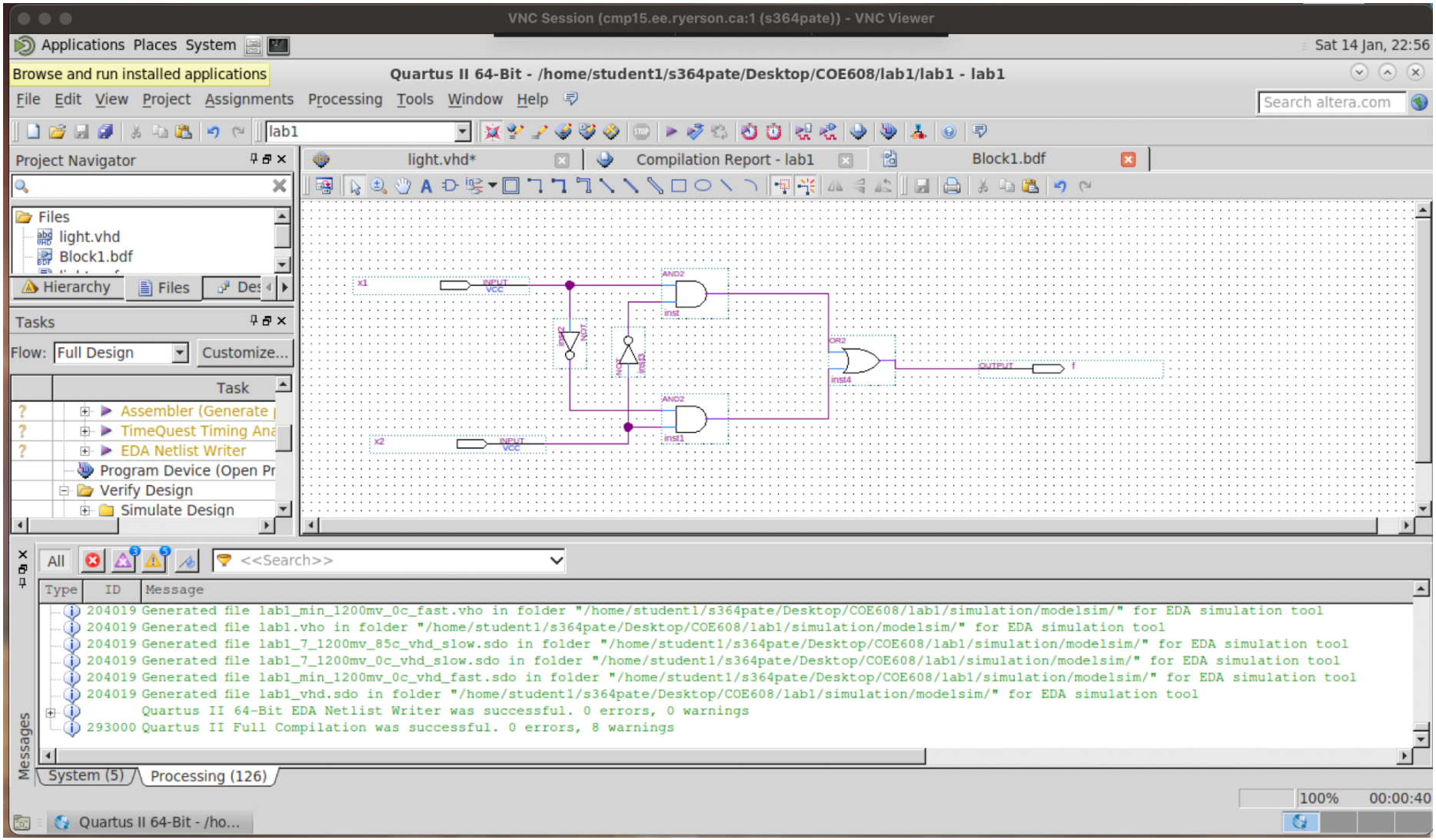
Applications Places System
Sat 14 Jan, 22:56
Quartus II 64-Bit - /home/student1/s364pate/Desktop/COE608/lab1/lab1 - lab1
File Edit View Project Assignments Processing Tools Window Help
Search altera.com
lab1
Project Navigator
Files
light.vhd
Block1.bdf
Hierarchy
Files
Tasks
Flow: Full Design
Customize...
Task
Assembler (Generate
TimeQuest Timing Ana
EDA Netlist Writer
Program Device (Open Pr
Verify Design
Simulate Design
light.vhd*
Compilation Report - lab1
Block1.bdf
1 library ieee;
2 use ieee.std_logic_1164.all;
3 entity light is
4 port (
5 x1, x2 : in std_logic;
6 f : out std_logic
7) ;
8 end light;
9
10 architecture Behavior of light is
11 begin
12 f <= (x1 and not x2) or (not x1 and x2);$
13 end Behavior;
All
<<Search>>
Type ID Message
204019 Generated file lab1_min_1200mv_0c_fast.vho in folder "/home/student1/s364pate/Desktop/COE608/lab1/simulation/modelsim/" for EDA simulation tool
204019 Generated file lab1.vho in folder "/home/student1/s364pate/Desktop/COE608/lab1/simulation/modelsim/" for EDA simulation tool
204019 Generated file lab1_7_1200mv_85c_vhd_slow.sdo in folder "/home/student1/s364pate/Desktop/COE608/lab1/simulation/modelsim/" for EDA simulation tool
204019 Generated file lab1_7_1200mv_0c_vhd_slow.sdo in folder "/home/student1/s364pate/Desktop/COE608/lab1/simulation/modelsim/" for EDA simulation tool
204019 Generated file lab1_min_1200mv_0c_vhd_fast.sdo in folder "/home/student1/s364pate/Desktop/COE608/lab1/simulation/modelsim/" for EDA simulation tool
204019 Generated file lab1_vhd.sdo in folder "/home/student1/s364pate/Desktop/COE608/lab1/simulation/modelsim/" for EDA simulation tool
Quartus II 64-Bit EDA Netlist Writer was successful. 0 errors, 0 warnings
293000 Quartus II Full Compilation was successful. 0 errors, 8 warnings
Messages
System (5)
Processing (126)
Ln 12 Col 45 VHDL File 100% 00:00:40
Quartus II 64-Bit - /ho...


VNC Session (cmp15.ee.ryerson.ca:1 (s364pate)) - VNC Viewer
Applications Places System
Sat 14 Jan, 22:56
Browse and run installed applications
Quartus II 64-Bit - /home/student1/s364pate/Desktop/COE608/lab1/lab1 - lab1
File Edit View Project Assignments Processing Tools Window Help
Search altera.com
lab1
Project Navigator
Files
light.vhd
Block1.bdf
Hierarchy
Files
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Flow: Full Design
Customize...
Task
Assembler (Generate
TimeQuest Timing Ana
EDA Netlist Writer
Program Device (Open Pr
Verify Design
Simulate Design
light.vhd*
Compilation Report - lab1
Block1.bdf
x1
x2
INPUT
VCC
AND2
inst
inst1
NOT
inst2
inst3
OR2
inst4
OUTPUT
f
All
<<Search>>
Type ID Message
204019 Generated file lab1_min_1200mv_0c_fast.vho in folder "/home/student1/s364pate/Desktop/COE608/lab1/simulation/modelsim/" for EDA simulation tool
204019 Generated file lab1.vho in folder "/home/student1/s364pate/Desktop/COE608/lab1/simulation/modelsim/" for EDA simulation tool
204019 Generated file lab1_7_1200mv_85c_vhd_slow.sdo in folder "/home/student1/s364pate/Desktop/COE608/lab1/simulation/modelsim/" for EDA simulation tool
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Messages
System (5)
Processing (126)
100%
00:00:40
Quartus II 64-Bit - /ho...