

컴퓨터공학실험II

FPGA의 소개와 이해



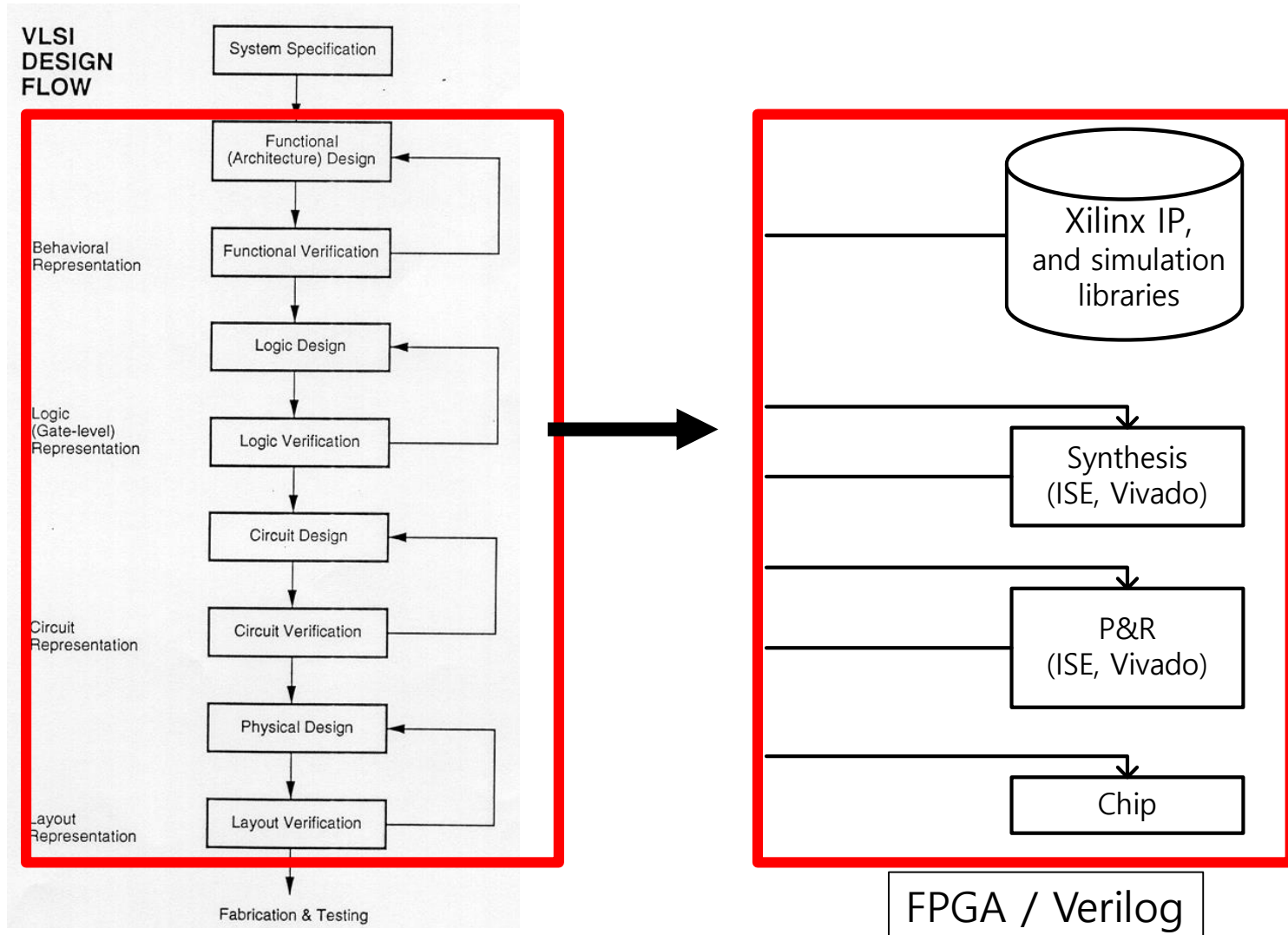
*Be as proud of Sogang
As Sogang is proud of you*

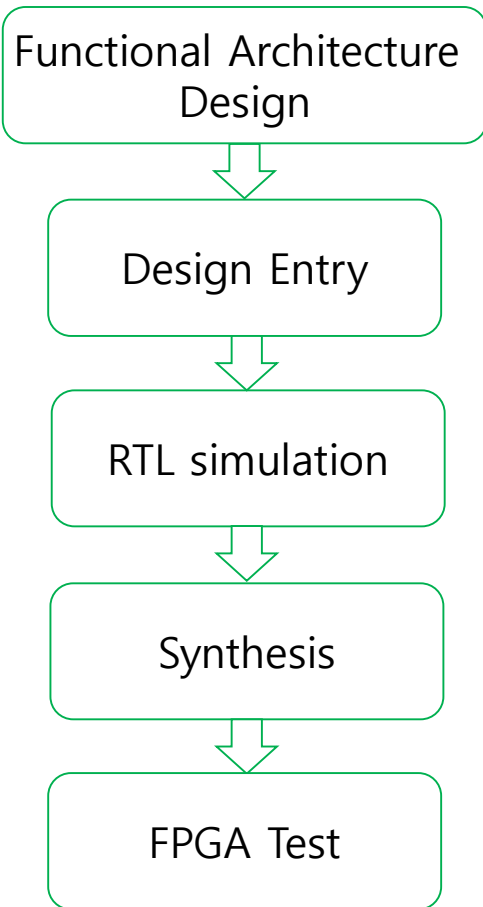
◆ FPGA(Field Programmable Gate Array)

- 이미 설계된 하드웨어를 반도체로 생산하기 직전 최종적으로 하드웨어의 동작 및 성능을 검증하기 위해 제작하는 중간 개발 물 형태의 집적 회로(IC)로, 프로그래밍을 할 수 있는 중간 형태의 비메모리 반도체의 한 종류입니다.
일반 반도체는 회로 변경과 프로그래밍이 불가능한 데 반해 프로그래밍이 가능합니다.
- 설계 가능 논리 소자는 AND, OR, XOR, NOT, 더 복잡한 디코더나 계산기능의 조합 기능같은 기본적인 논리 게이트의 기능을 복제하여 프로그래밍할 수 있으며,
대부분의 FPGA는 프로그래밍가능 논리 요소 에 간단한 플립플롭 이나, 메모리 블록으로 된 메모리 요소를 포함하고 있습니다.
- 활용 분야
 - 로봇제어(알파고)
 - 우주선, 인공위성 등

(압도적으로 빠른 하드웨어 프로그래밍을 요구로 하는 현장에서 주로 사용합니다.)

◆ 흐름도





◆ **Functional Architecture Design**

이론 및 스케메틱(schematic)을 통해서 디자인을 설계하는 단계.

◆ **Design Entry**

HDL(Hardware Description Language)로 설계하는 단계.

◆ **RTL simulation**

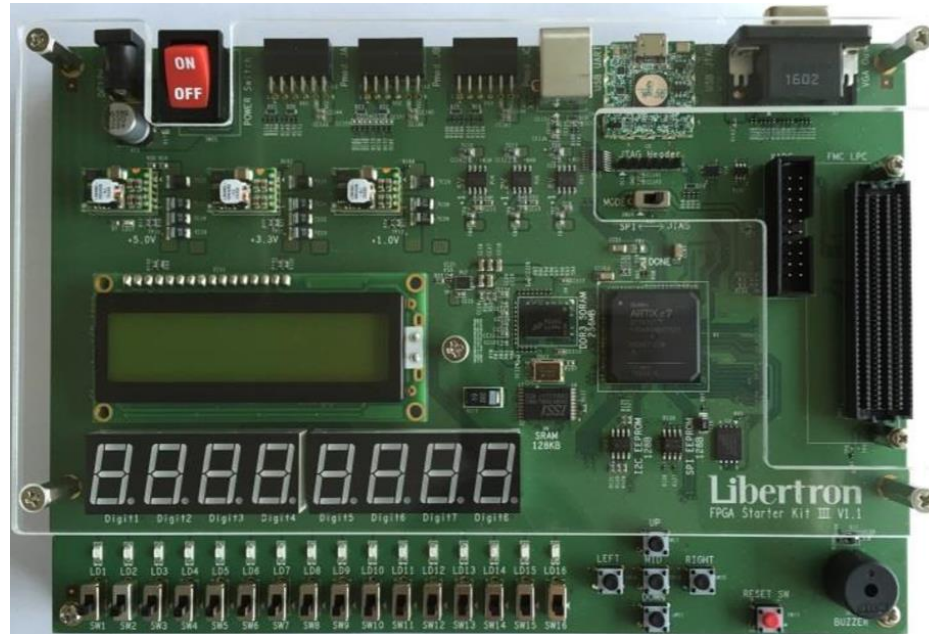
이전 과정인 design Entry에서 사용자가 구현한 것을 시뮬레이션으로 검증을 해보는 단계.

◆ **Synthesis**

합성과정은 유저가 구현한 High-Level한 디자인을 FPGA 보드가 이해 할 수 있는 Low Level로 바꿔주는 단계.

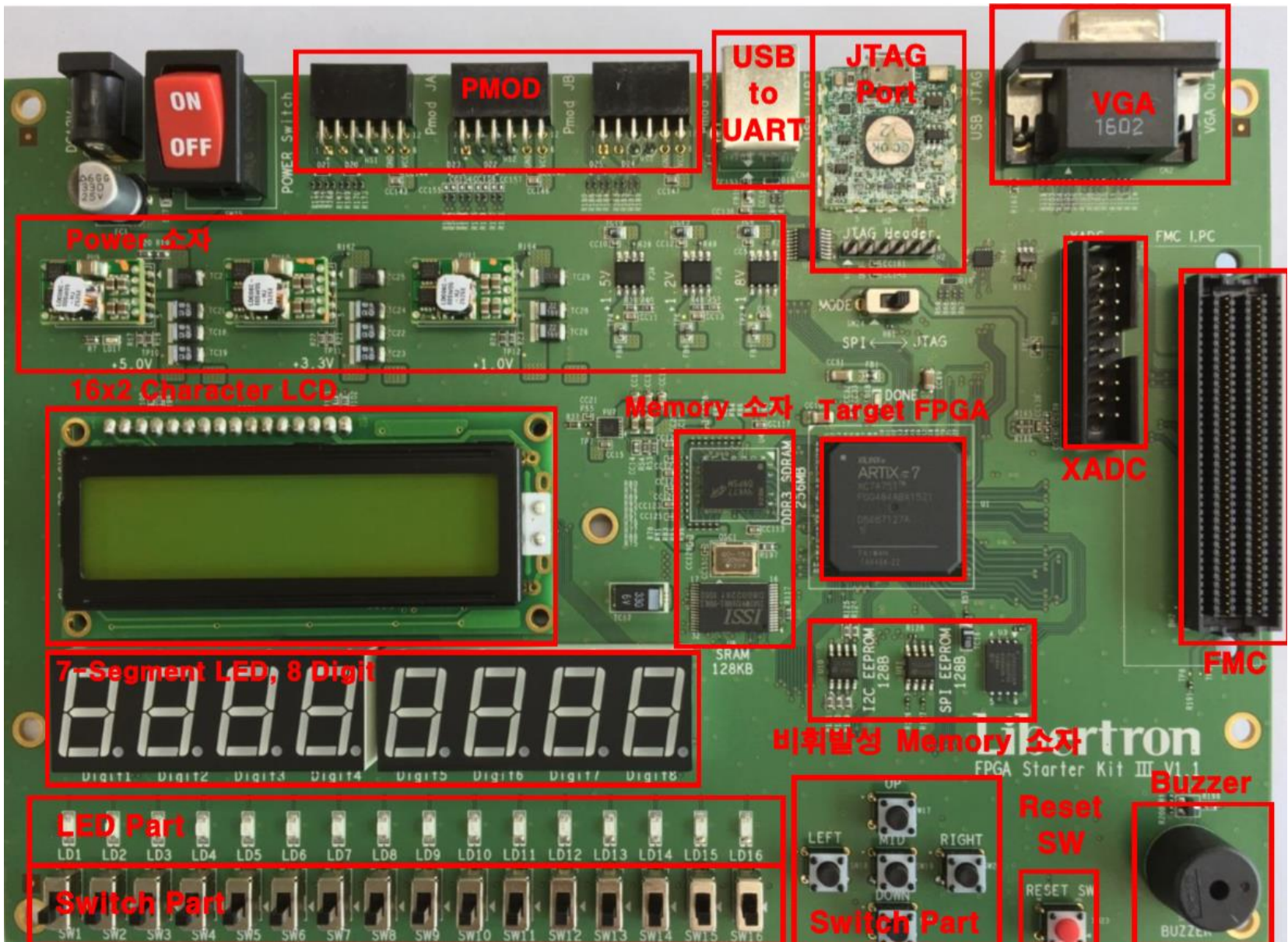
◆ **FPGA Test**

FPGA 보드를 통해 Test 해보는 단계.



- ◆ 실험장비 : FPGA Starter Kit III Board
- ◆ S/W : Xilinx Vivado
- ◆ Language : Verilog

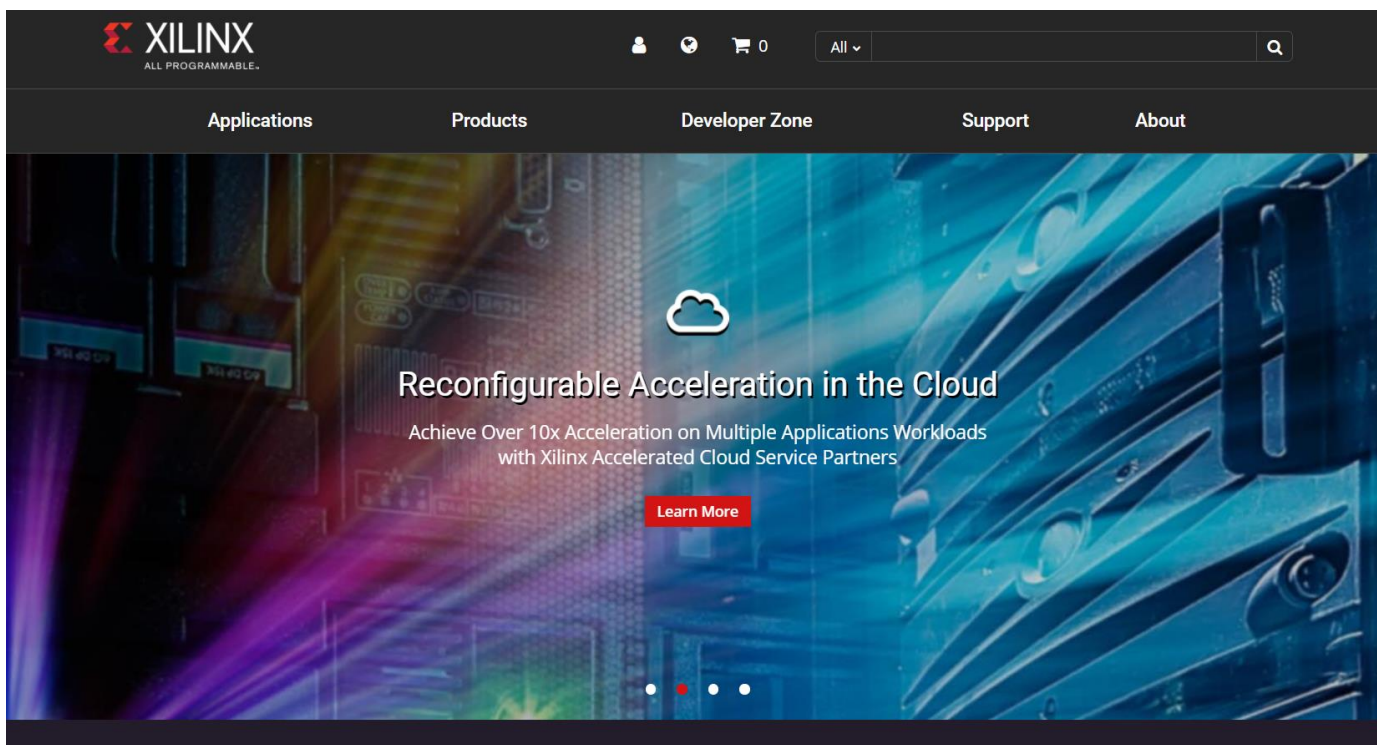
FPGA 장비 소개



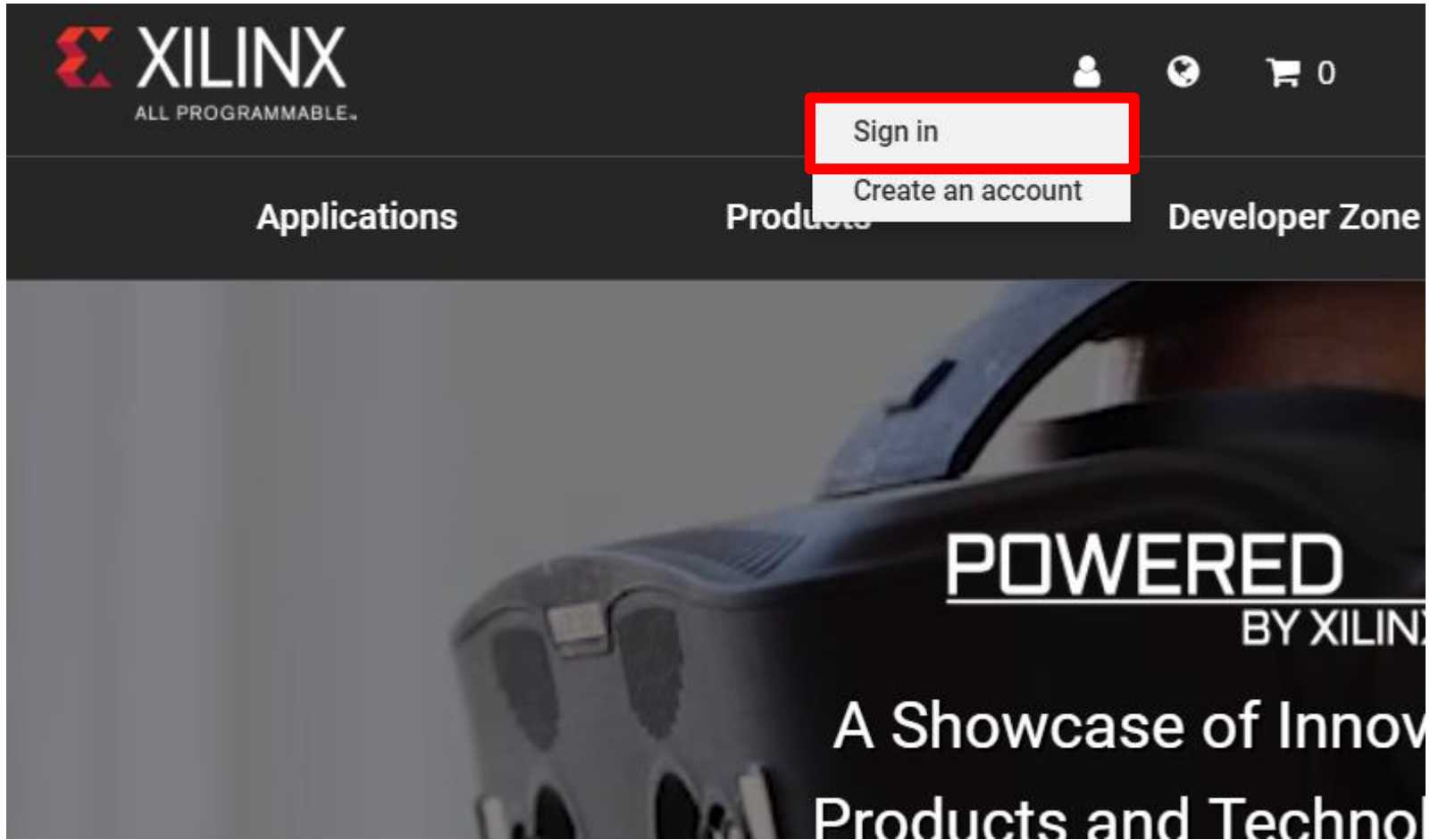
◆ Vivado 설치

www.xilinx.com 으로 접속합니다.



※ 이미 회원으로 등록되어 있으신 분은 가입 절차를 건너 뛰시기 바랍니다.



◆ Vivado 회원 등록



◆ Vivado 회원 등록


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Confirm Password *

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 e028a

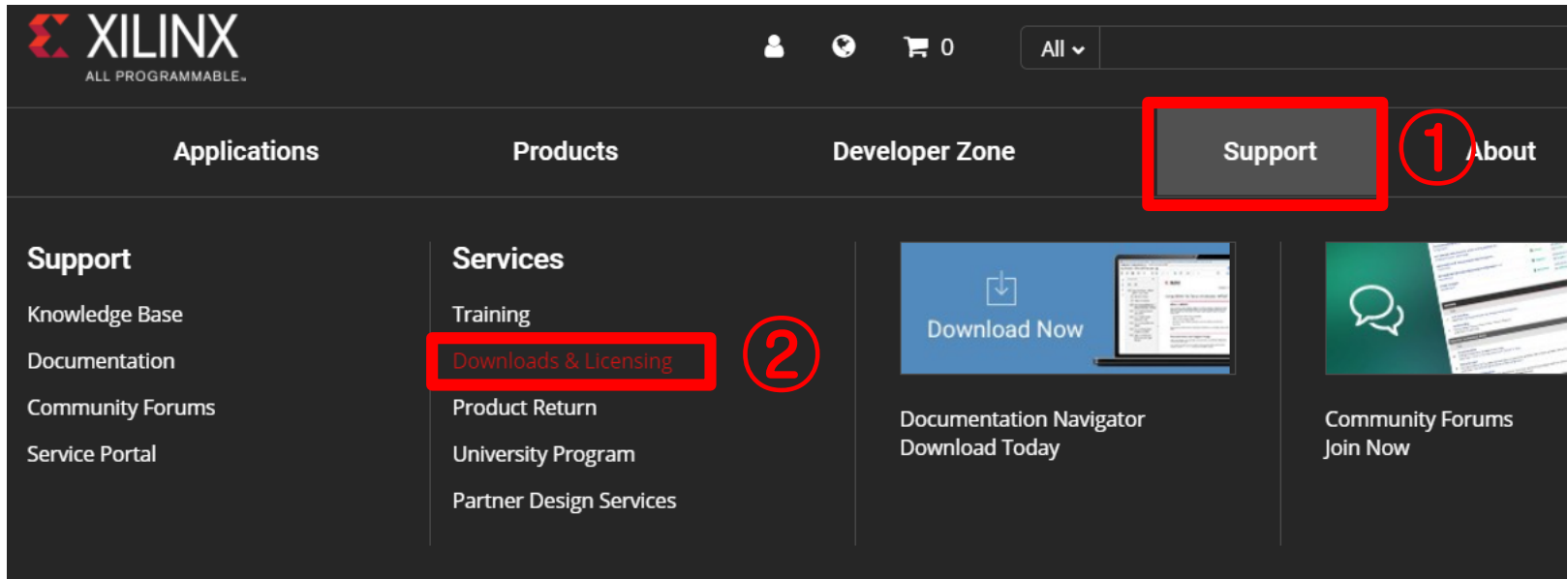
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Create Account

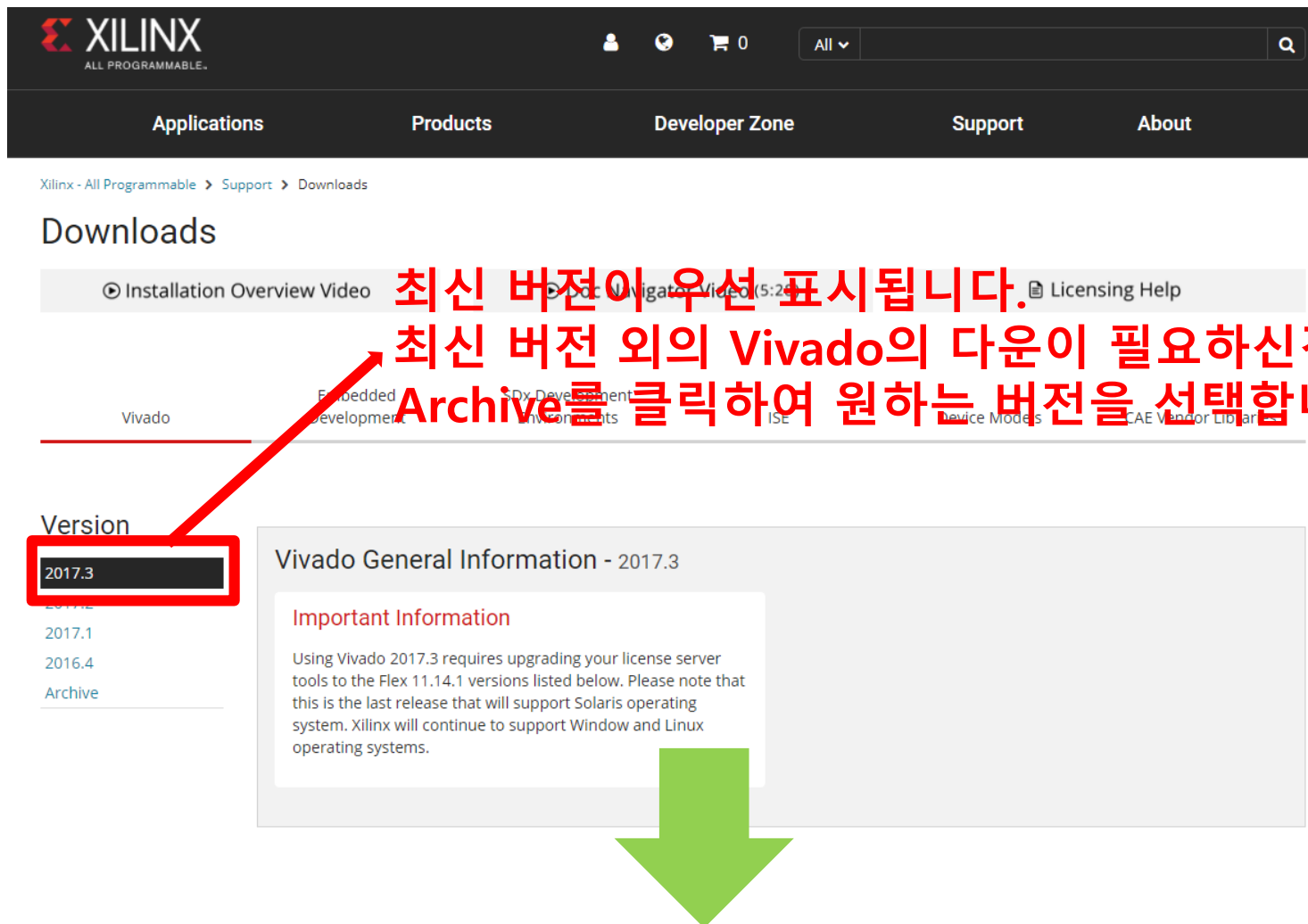
① 작성

②

◆ Vivado 설치



◆ Vivado 설치



The screenshot shows the Xilinx website's 'Downloads' section. A red arrow points from the '2017.3' version link in the 'Version' list to the 'Vivado General Information - 2017.3' section. A green arrow points down from the 'Important Information' box in the 'Vivado General Information' section.

Annotations:

- 최신 버전이 우선 표시됩니다. (The latest version is displayed first.)
- 최신 버전 외의 Vivado의 다운이 필요하신 경우 Archive를 클릭하여 원하는 버전을 선택합니다. (If you need to download Vivado other than the latest version, click Archive to select the version you want.)

◆ Vivado 설치

Vivado Design Suite - HLx Editions - 2017.3 Full Product Installation

Important

We strongly recommend to use the web installers as it reduces download time and saves significant disk space.

Please see [Installer Information](#) for details.

Download Includes

Vivado Design Suite HLx Editions (All Editions)

Download Type

Full Product Installation

Download Size

10.22 GB

Documentation

2017.3 - Release Notes

Enablement

License Solution Center

3가지 옵션 중에 자신에게 알맞은 파일을 선택하여 다운로드 합니다.

① Windows OS / 다운로드 및 설치가 가능한 자동실행 파일
- 설치 시 인터넷 연결 필수

② Linux OS / 다운로드 및 설치가 가능한 자동실행 파일
- 설치 시 인터넷 연결 필수

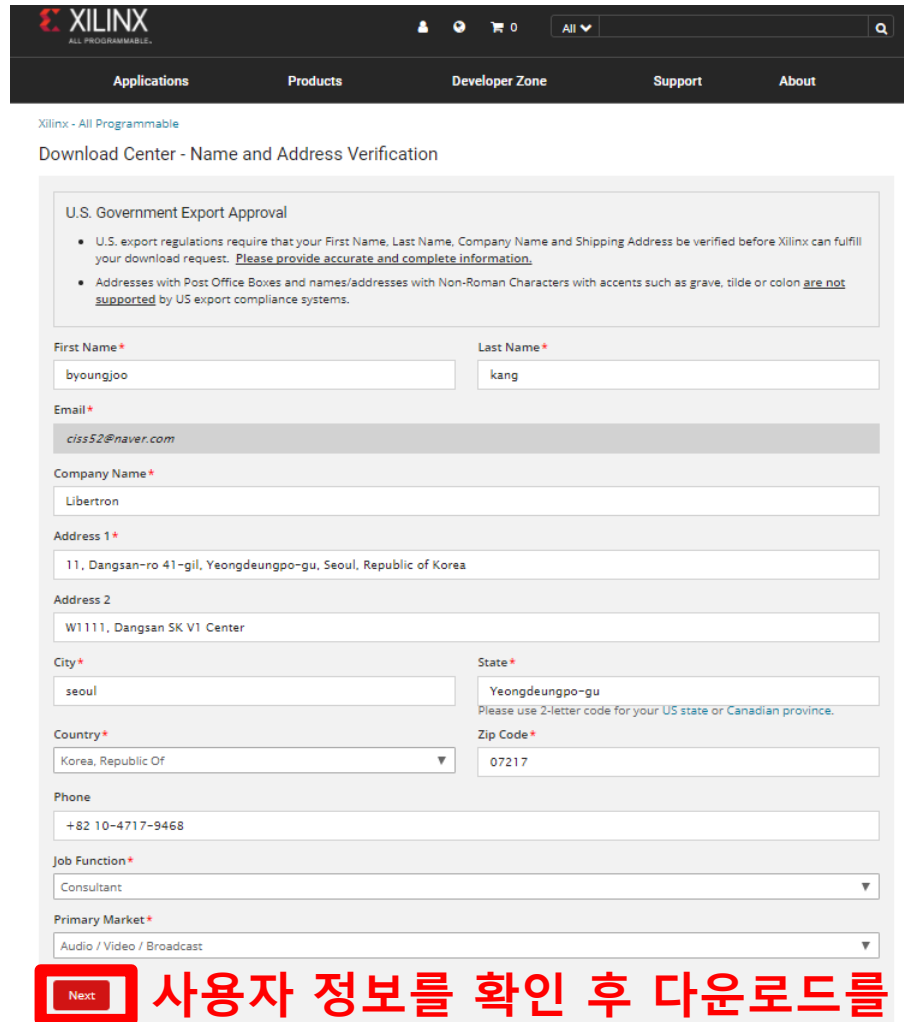
③ All OS / 다운로드 및 설치가 가능한 자동실행 파일
- 설치 시 인터넷 연결 필수

↓ Vivado HLx 2017.3: WebPACK and Editions - Windows Self Extracting Web Installer (EXE - 51.22 MB)
MD5 SUM Value: f25ec28dab1a3711dd1346dcab2640e8

↓ Vivado HLx 2017.3: WebPACK and Editions - Linux Self Extracting Web Installer (BIN - 100.61 MB)
MD5 SUM Value: d80a2721483fd5b1a6a77c481f98f988

↓ Vivado HLx 2017.3: All OS installer Single-File Download (TAR/GZIP - 16.23 GB)
MD5 SUM Value: d443f58d703ff691cebc59c2173ae782

◆ Vivado 설치



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Xilinx - All Programmable

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- U.S. export regulations require that your First Name, Last Name, Company Name and Shipping Address be verified before Xilinx can fulfill your download request. [Please provide accurate and complete information.](#)
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Address 1 *

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State *
Please use 2-letter code for your US state or Canadian province.

Country *

Zip Code *

Phone

Job Function *

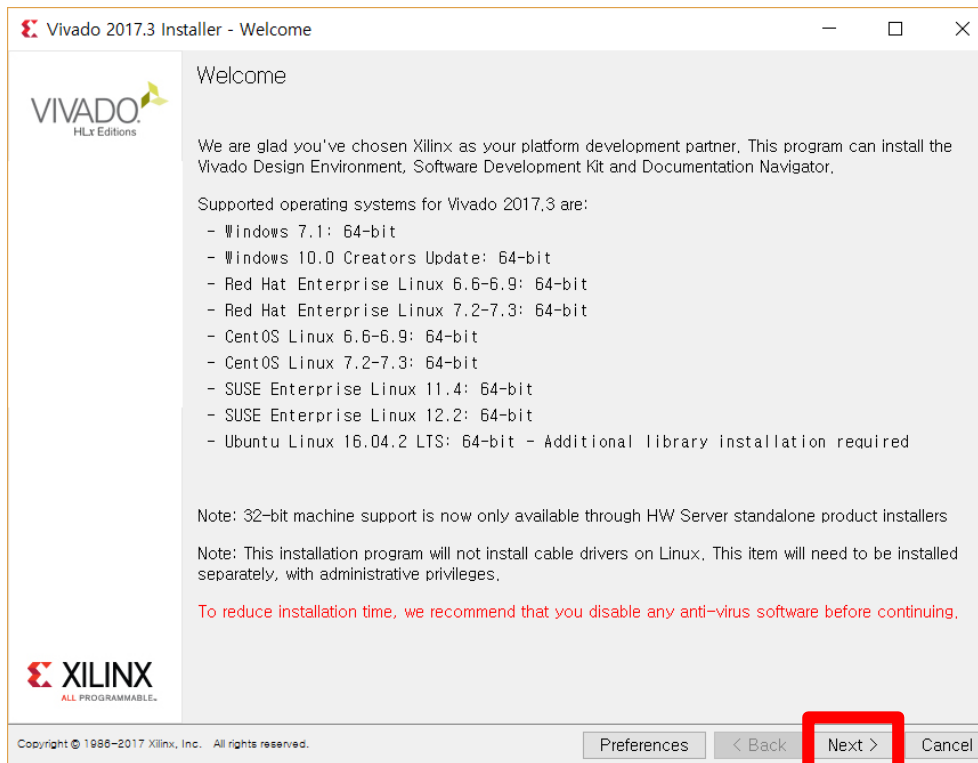
Primary Market *

Next 사용자 정보를 확인 후 다운로드를 시작합니다.

◆ Vivado 설치

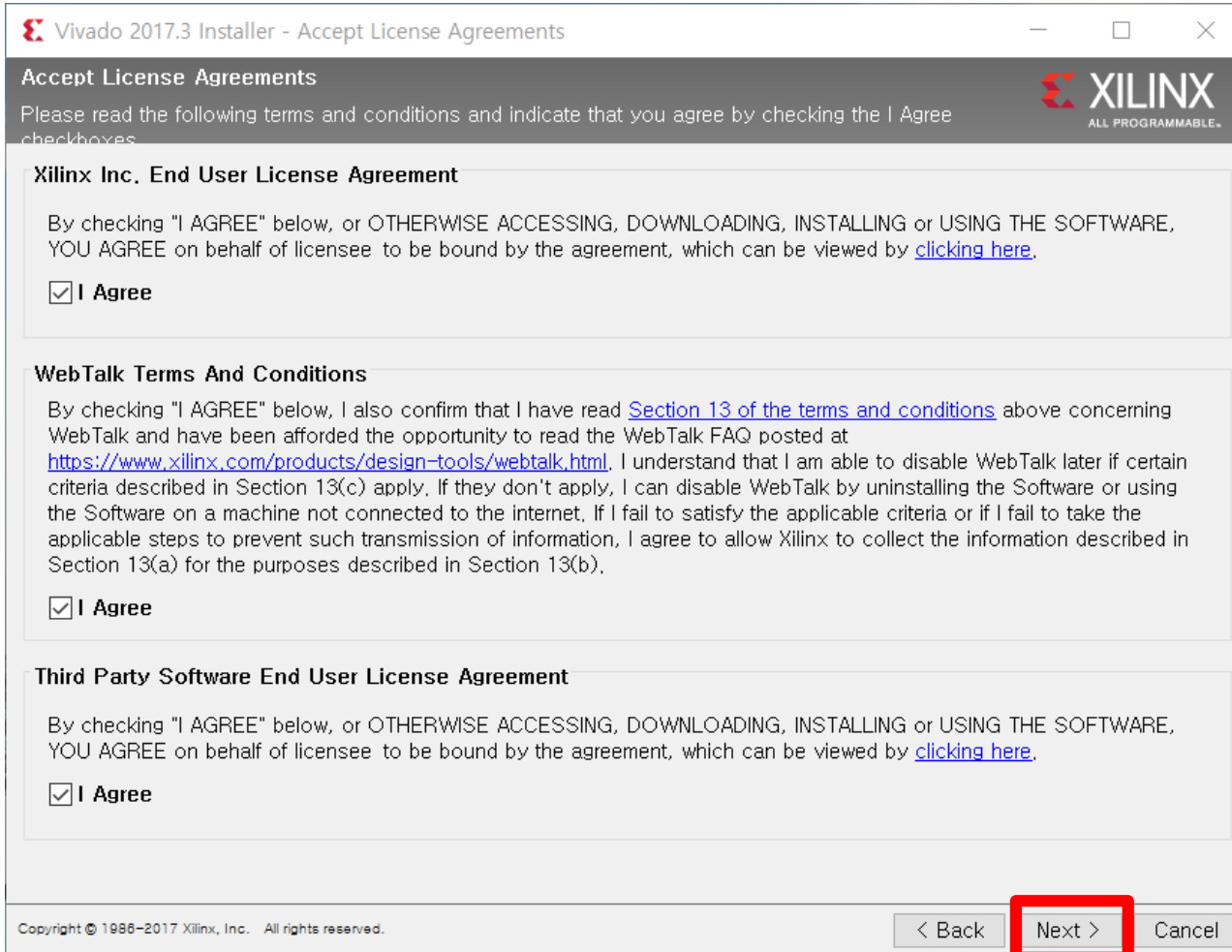


① 다운로드 완료된 파일을 실행하여 installer 를 시작합니다.



②

◆ Vivado 설치



Vivado 2017.3 Installer - Accept License Agreements

Accept License Agreements

Please read the following terms and conditions and indicate that you agree by checking the I Agree checkboxes.

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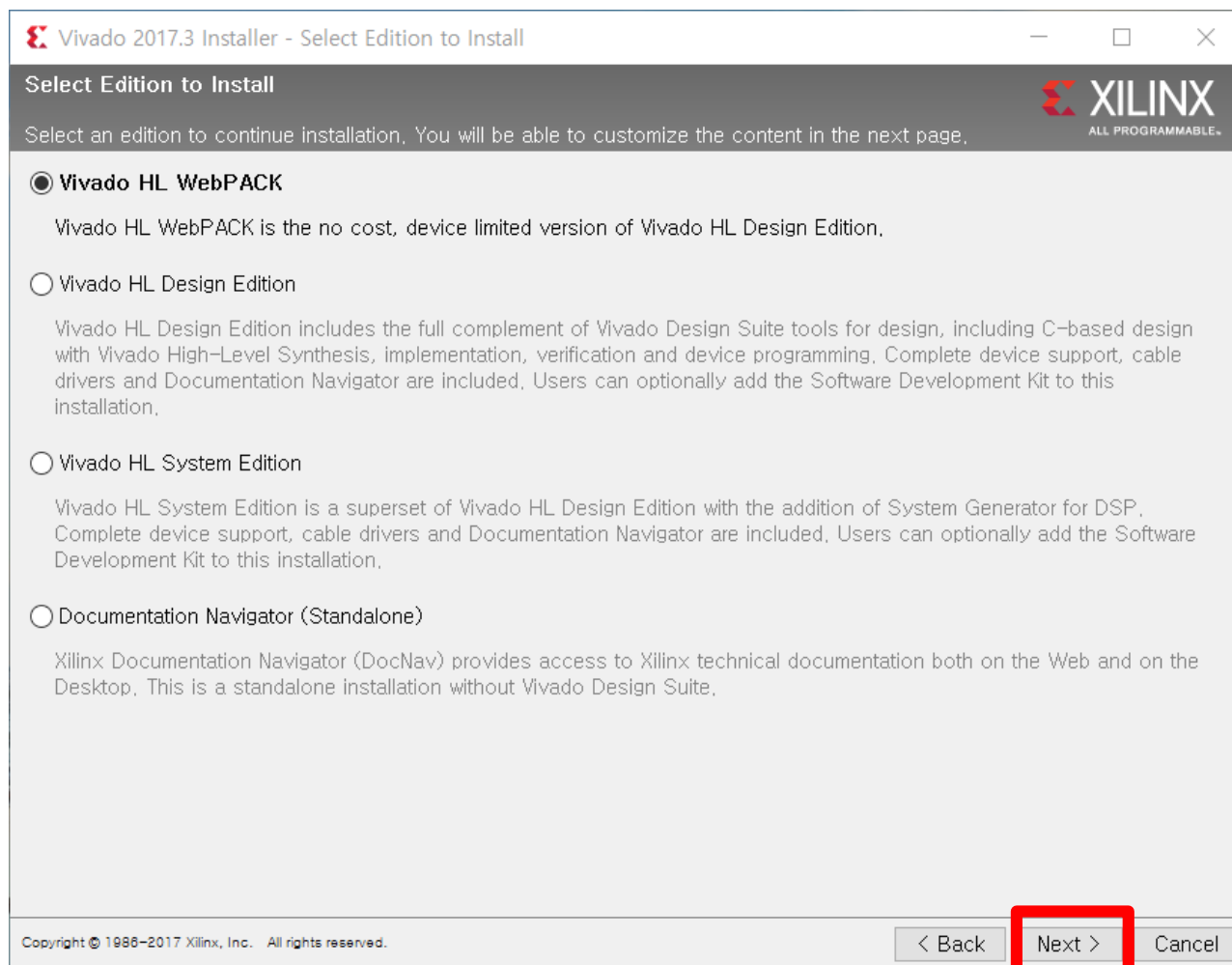
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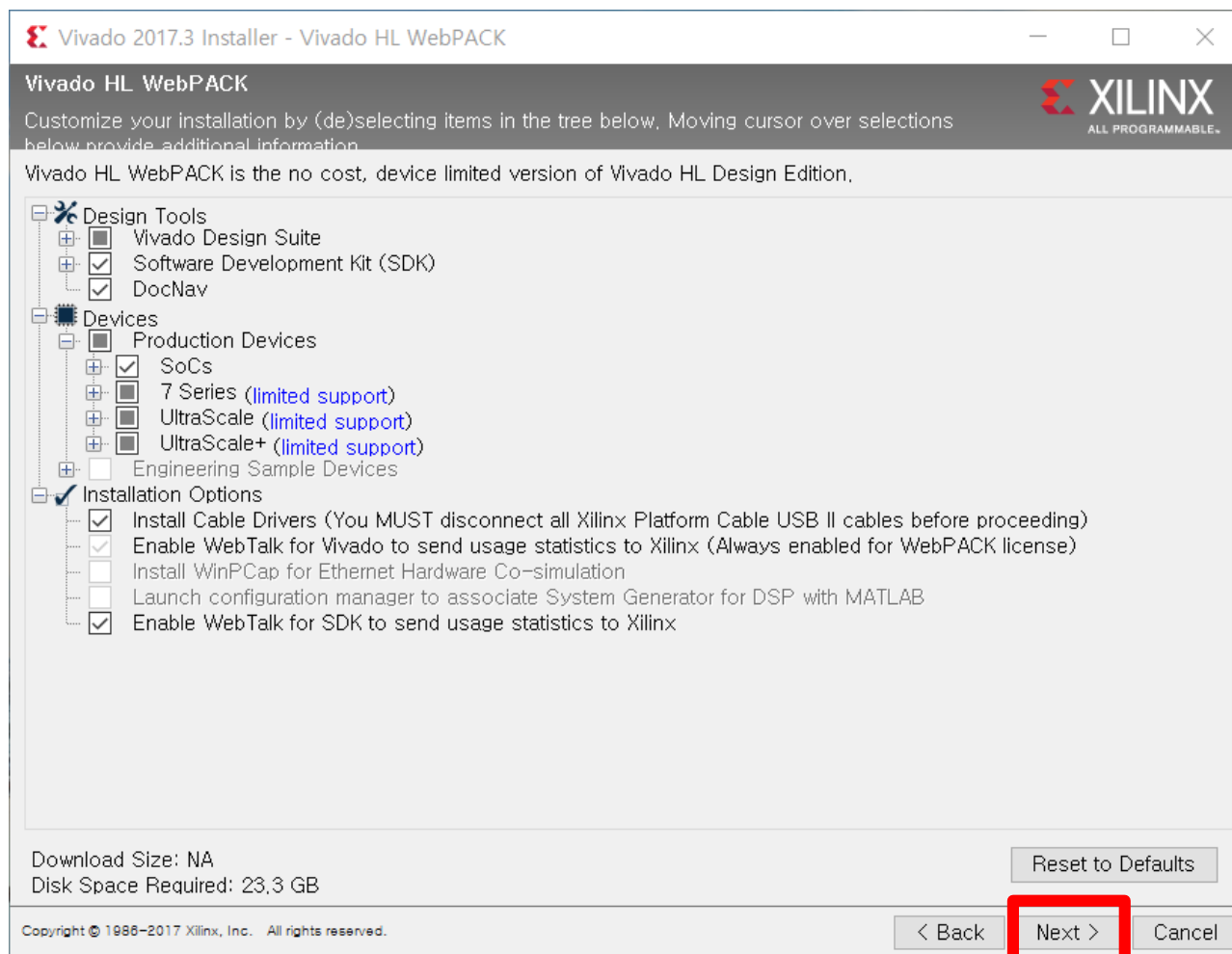
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< Back **Next >** Cancel

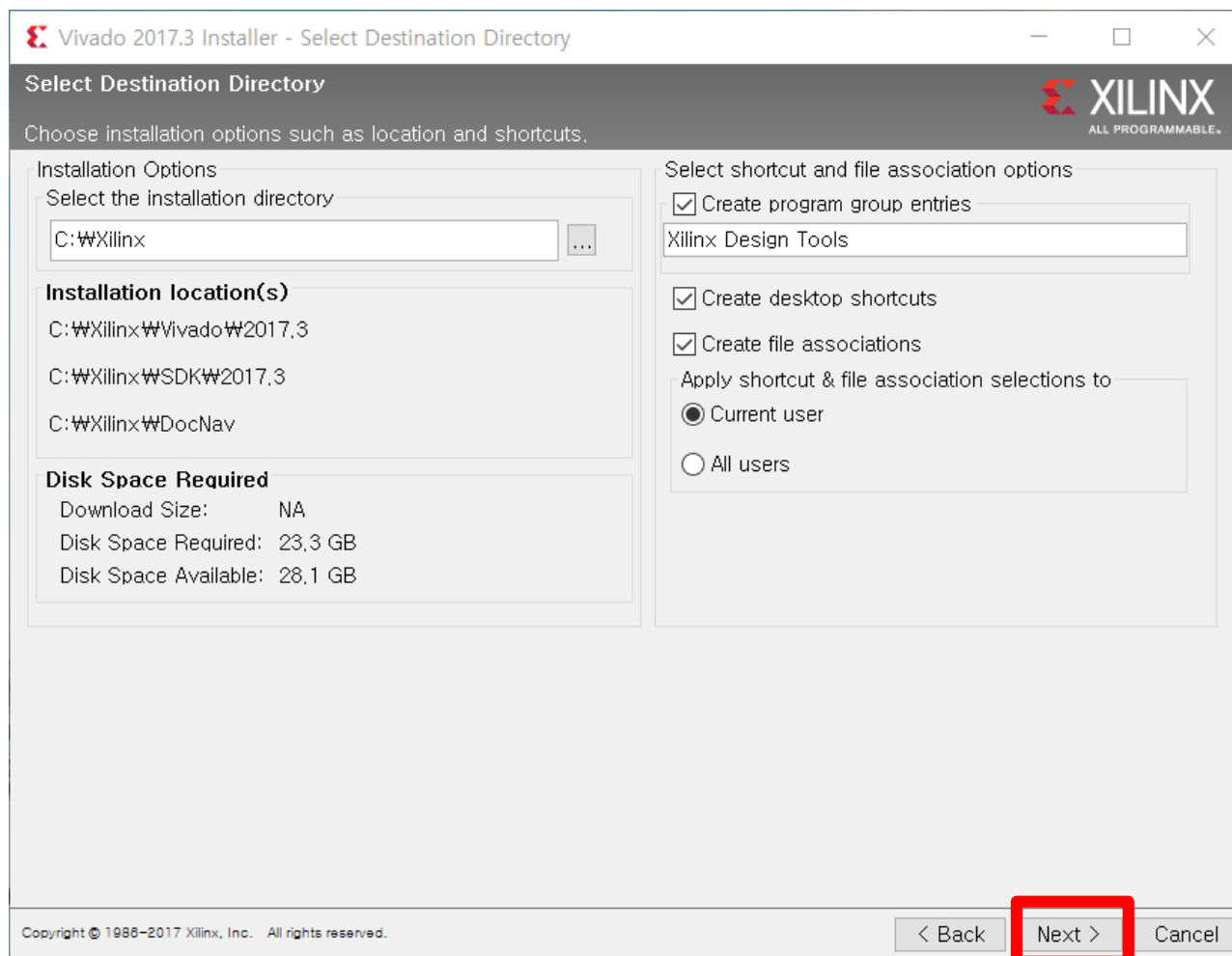
◆ Vivado 설치



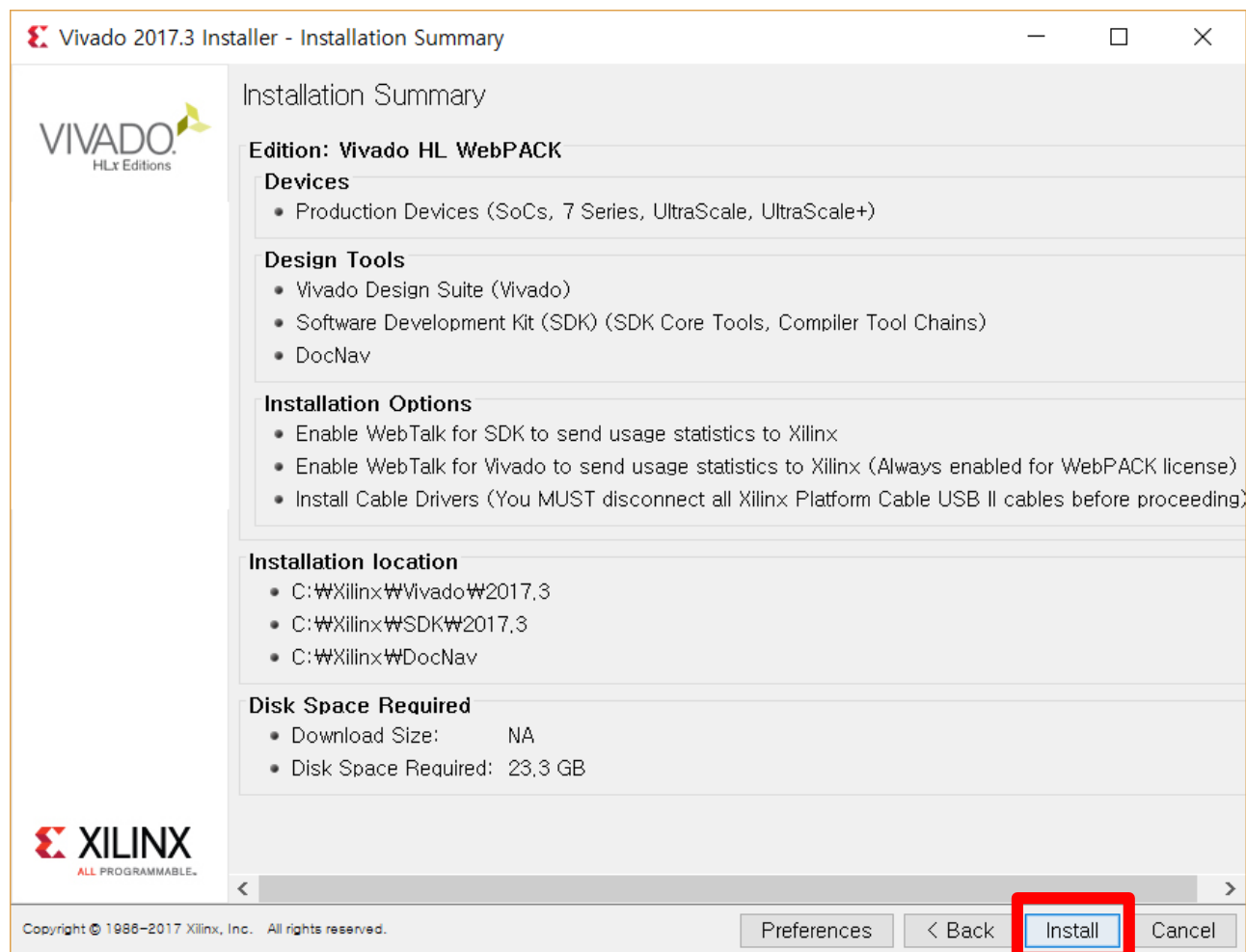
◆ Vivado 설치



◆ Vivado 설치



◆ Vivado 설치



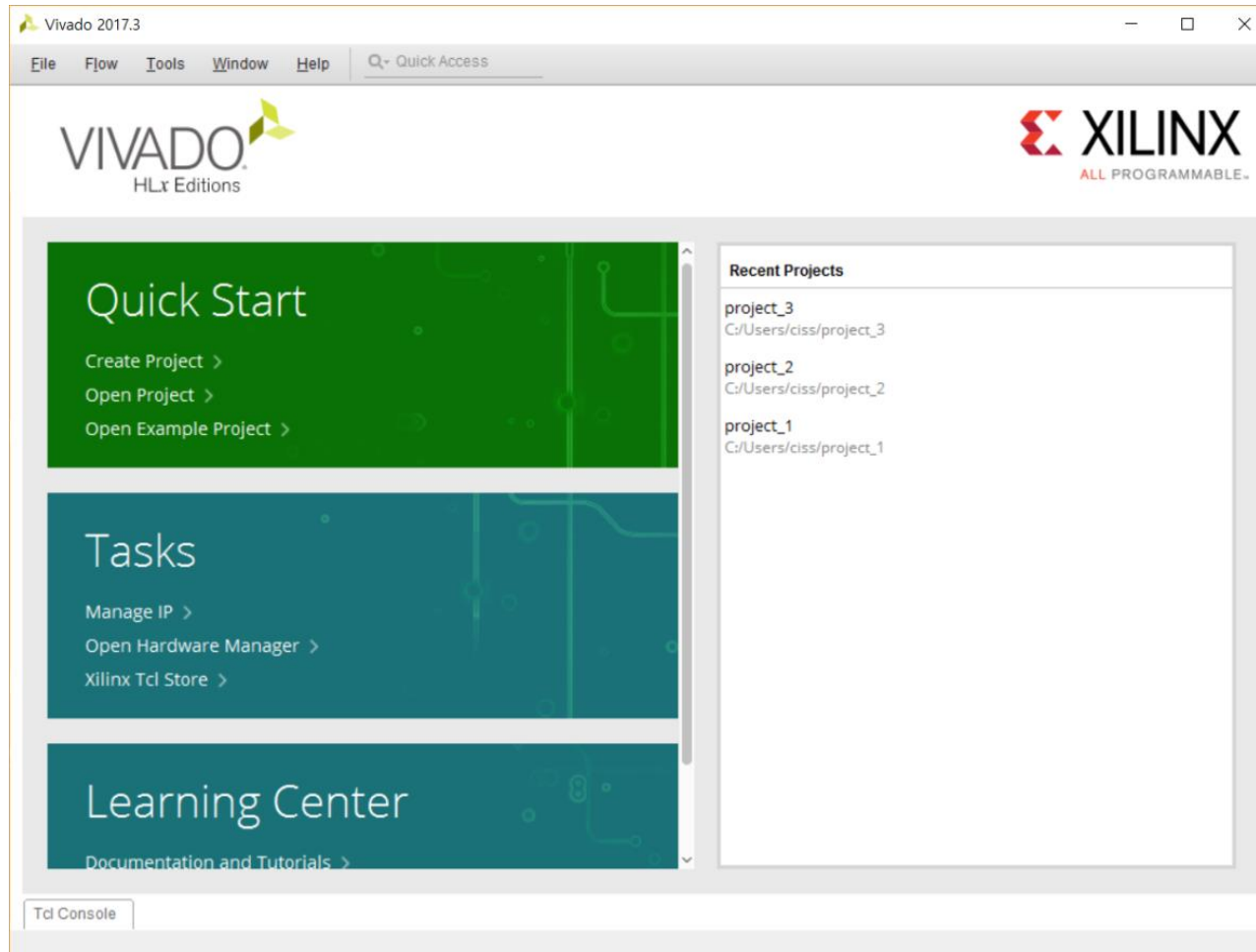
◆ Vivado 설치

파일 다운로드 및 설치가 시작됩니다.
수십분의 설치 진행후에 작업이 완료됩니다.



◆ Vivado 설치

정상적으로 설치가 완료되면 아래 와 같은
시작 화면을 보실 수 있습니다.



◆ Clock

Global Clock

Signal Name	FPGA Pin	I/O	Description
FPGA_CLK	R4	Input	FPGA Clock Input (100Mhz)

◆ Switch

Reset Switch

Signal Name	FPGA Pin	I/O	Description
FPGA_RSTB	U7	Input	FPGA Logic Reset Pin (Active 'L')

PUSH Switch

Signal Name	FPGA Pin	I/O	Description
PUSH_SW_UP	E21	Input	User Push Switch [4..0] (Active 'H')
PUSH_SW_LEFT	D21		
PUSH_SW_MID	G21		
PUSH_SW_RIGHT	G22		
PUSH_SW_DOWN	F21		

◆ Switch

DIP Switch

Signal Name	FPGA Pin	I/O	Description
DIP_SW<0>	J4	Input	User DIP Switch [15..0] (Active 'H')
DIP_SW<1>	L3		
DIP_SW<2>	K3		
DIP_SW<3>	M2		
DIP_SW<4>	K6		
DIP_SW<5>	J6		
DIP_SW<6>	L5		
DIP_SW<7>	L4		
DIP_SW<8>	Y16		
DIP_SW<9>	AA16		
DIP_SW<10>	AB16		
DIP_SW<11>	AB17		
DIP_SW<12>	AA13		
DIP_SW<13>	AB13		
DIP_SW<14>	AA15		
DIP_SW<15>	AB15		

◆ Display

Discrete LED

Signal Name	FPGA Pin	I/O	Description
LED<0>	F15	Output	User LED [15..0] (Active 'H')
LED<1>	F13		
LED<2>	F14		
LED<3>	F16		
LED<4>	E17		
LED<5>	C14		
LED<6>	C15		
LED<7>	E13		
LED<8>	AA10		
LED<9>	AA11		
LED<10>	V10		
LED<11>	W10		
LED<12>	Y11		
LED<13>	Y12		
LED<14>	W11		
LED<15>	W12		

◆ Display

7-Segment

Signal Name	FPGA Pin	I/O	Description
SEG_A	D20	Output	Segment [7..0] (Active 'H')
SEG_B	C20		
SEG_C	C22		
SEG_D	B22		
SEG_E	B21		
SEG_F	A21		
SEG_G	E22		
SEG_DP	D22		
DIGIT1	E14	Output	Digit [7..0] (Active 'H')
DIGIT2	E16		
DIGIT3	D16		
DIGIT4	D14		
DIGIT5	AB11		
DIGIT6	AB12		
DIGIT7	AA9		
DIGIT8	AB10		