Pokhara University
Faculty of Science and Technology

Course No.: xxx xxx
Course title: Digital Logic (3-1-2)
Nature of the course: Theory & Practical
Level: Undergraduate

Full marks: 100
Pass marks: 45
Time per period: 1 hour
Total Periods: 45
Program: BE

1. Course Description

This course covers the various concepts of digital logic systems. This course emphasizes on fundamental concept, principles and properties of Boolean algebra and its application in simplification, circuit analysis and gate implementation. It covers the use of flip flops in the design of synchronous and asynchronous sequential logic circuits. It also covers the ALU design.

2. General Objectives

This course provides basic knowledge of logic systems, introduces basic tools to design various digital logic circuits and enables the students to design a basic digital computer.

3. Methods of Instruction

Lecture, discussion, readings, Lab works, Project works

4. Contents in Detail

Specific Objectives	Contents
• Familiarize and compare analog and digital signal and system. • Familiarize and use the information representation in any number system.	**Unit 1: Introduction (2 hrs)** 1. Analog and digital signal 2. Analog and digital system 3. Numerical representation 4. Digital number system
• Familiarize with binary number systems and their conversions. • Understand the different codes to represent information.	**Unit 2: Number Systems and Codes (6 hrs)** 2.1 Number systems 2.1.1 Decimal 2.1.2 Binary 2.1.3 Octal 2.1.4 Hexadecimal 2.2 Number system conversion 2.3 Complements (radix and diminished-radix) 2.4 Subtraction using complements 2.5 Binary coding systems 2.5.1 Weighted codes (BCD, 8 4 -2 -1, and 2 4 2 1) 2.5.2 Non-weighted codes (Excess-3 and Gray) 2.6 Alphanumeric and instruction codes

• To trace the simplification process using Boolean Algebra. • To implement the simplified functions using logic gates.	**Unit 3: Boolean Algebra and Logic Gates (4 hrs)** 3.1 Boolean algebra (definition, properties, postulates and theorems) 3.2 Logic gates, truth tables and Boolean function 3.3 Duality principle and complements 3.4 Gate implementation 3.5 Universality of NAND and NOR gates
• Simplify the Boolean function using map method. • Help to identify and use don't care conditions while simplifying functions.	**Unit 4: Simplification of Boolean Function (5 hrs)** 4.1 Venn diagram 4.2 Canonical forms and standard forms 4.3 Karnaugh map up to 5 variables 4.4 Minimum realization 4.5 Don't care conditions 4.6 Simplification in SOP and POS using K-map
• Describe how to design various combinational logic circuits. • Help to analyze the designed combinational circuits.	**Unit 5: Combinational Circuit (4 hrs)** 5.1 Design procedure 5.2 Adder and subtractor 5.3 Code conversion 5.4 Analysis procedure 5.5 NAND and NOR implementation 5.6 Multilevel NAND and NOR gates 5.7 Parity generator and checker
• Describes different generations of IC technology. • Describe different MSI and LSI components, their design, internal logic diagram, operation and implementation.	**Unit 6: MSI and LSI Design (6 hrs)** 6.1 Introduction to Integration technology 6.2 Parallel adder and subtractor 6.3 Decimal / BCD adder 6.4 Magnitude comparator 6.5 Multiplexer and demultiplexer 6.6 Encoder and Decoder, 6.7 ROM and PLA
• Distinguish between synchronous and asynchronous logic and latch and flip flops. • Give knowledge of different flip flops and their use in sequential logic circuits. • Help to design and analyze sequential logic circuits.	**Unit 7: Sequential Circuits (6 hrs)** 7.1 Synchronous and asynchronous logic 7.2 Differences between Latch and fli-flop, Flip flops (RS, JK, D, T) and their truth table, excitation table and characteristic equation 7.3 Triggering of flip flops 7.4 State diagram and state table 7.5 State reduction and binary assignment 7.6 Design and analysis of clocked sequential circuit 7.7 Master-slave flip flops
• Describe about registers, shift registers and types with timing sequences. • Design synchronous, asynchronous and Mod	**Unit 8: Registers and Counters (6 hrs)** 8.1 Register, shift register and types of Shift register 8.2 Synchronous counters 8.2.1 up to 4-bit counters

counters.	8. 3 Asynchronous counters 8.3.1 BCD ripple counter, 8.3.2 Mod counter 8.4 Ring counter 8.5 Output hazard race
• Describe about read and write operation in RAM. • Design arithmetic circuit and logic unit. • Describe about the processor unit and its diagram.	**Unit 9: Memory Unit and ALU (6hrs)** 9.1 Random access memory 9.2 Design of arithmetic logic unit 9.3 Accumulator 9.4 Shifter and status register 9.5 Processor unit

5. Laboratory work

- Familiarization with logic gates.
- Familiarization with Boolean functions.
- Design of simple combinational circuits.
- Adder and subtractor
- Encoder and decoder
- Multiplexer and demultiplexer
- Design of flip flops.
- Registers and counters

6. List of Tutorials

The various tutorial activities that suits this course should cover all the content of this course to give student a space to engage more actively with the course content in the presence of instructor. Students should submit tutorials as assignments or class-works to the instructor for evaluation. The following tutorial activities of 15 hours should be conducted to cover all the content of course:

A. Discussion-based Tutorials: (3 hrs)
   1. Analog and digital signal and system.
   2. IC technology and parameters considered during fabrication
   3. Sequential circuits and types
   4. Output hazard races

B. Problem solving-based Tutorials: (12 hrs)
   1. Conversion of numbers among number systems
   2. Simplification of Boolean functions in SOP and POS using theorems and postulates.
   3. Simplification of Boolean function in SOP and POS using K Map.
   4. Logic gate implementation, used of NAND and NOR gates.
   5. Implementation of Boolean function using various MSI and LSI components.
   6. Design of various combinational circuits, code conversion circuits and parity generation and checking circuits.
   7. Design of synchronous sequential circuit from state diagram.
   8. Design of synchronous and asynchronous counters.
   9. Design of arithmetic and logic unit.

7. Evaluation system and Students' Responsibilities

Evaluation System

The internal evaluation of a student may consist of assignments, attendance, term-exams, lab reports and projects etc. The tabular presentation of the internal evaluation is as follows:

External Evaluation	Marks	Internal Evaluation	Weight	Marks
Semester-End examination	50	**Theory**		30
		Attendance & Class Participation	10%	
		Assignments	20%	
		Presentations/Quizzes	10%	
		Term exam	60%	
		Practical		20
		Attendance & Class Participation	10%	
		Project Report	10%	
		Viva	20%	
		Exam	60%	
		Total Internal		50
Full Marks: 50 + 50 = 100				

Student Responsibilities

Each student must secure at least 45% marks in internal evaluation with 80% attendance in the class in order to appear in the Semester End Examination. Failing to get such score will be given NOT QUALIFIED (NQ) and the student will not be eligible to appear the Semester-End Examinations. Students are advised to attend all the classes, formal exam, test, etc. and complete all the assignments within the specified time period. Students are required to complete all the requirements defined for the completion of the course.

8. Prescribed Books and References

Text Book

1. M. Morris Mano, *Digital Logic and Computer Design* Pearson India, 2017.

Reference Books

1. M. Rafiquzzaman, Steven A. McNinch, *Digital Logic*, John Wiley and Sons, 2019.
2. M. Morris Mano, *Digital Design, Prentice Hall of India, 1998.*