Available online at www.sciencedirect.com
ScienceDirect
Microelectronic Engineering 84 (2007) 1647–1651
MICROELECTRONIC ENGINEERING
www.elsevier.com/locate/mee

Fabrication and characterization of single electron transistor on SOI

Q. Wang [a], Y.F. Chen [b], S.B. Long [a], J.B. Niu [a], C.S. Wang [a], R. Jia [a], B.Q. Chen [a], M. Liu [a,*], T.C. Ye [a]

[a] *Institute of Microelectronics of Chinese Academy of Sciences, Beijing 100029, China*
[b] *Rutherford Appleton Laboratory, Chilton, Didcot, Oxon OX11 0QX, UK*

Available online 15 February 2007

Abstract

A novel technique, based on electron-beam lithography (EBL) and anisotropic reactive ion etch (RIE), was developed in this work for the fabrications of single electron transistors with ultra small junctions in silicon on insulator (SOI). Junction size as small as 10 nm has been achieved. Initial characterisation at low temperature has demonstrated clear Coulomb blockade gap in the measured *I–V* curves, indicating that such narrow junctions in silicon finally formed by RIE are still functional. This process eases the difficulty in EBL for 10 nm feature size by the controllable lateral dry-etch on the sidewall of the silicon thin layer, opening up a prospect for routine manufacture of single electronic devices and circuits on SOI, which possesses broad applications in meteorological measurement and IT technology.

Keywords: Single electron transistor; Silicon on insulator (SOI); Electron beam lithography; Reactive-ion etching; Coulomb blockade; Coulomb staircase

1. Introduction

It has been widely recognised that single electron tunnelling transistors (SETs), due to its high sensitivity to electronic charge, low power consumption [1–3] and high integration density, are of broad potential applications [4–8]. In the past decade this technique has successfully evolved from traditional metallic tunnelling junctions (MTJs) [9] to silicon based SOI SET technique. This advance exhibits a number of important advantages over the traditional technique. For example, the well developed silicon-based processing technique can be applied on the fabrications of single electronics so that the integration of single electronics and CMOS technology for new generation of devices and circuits [10] becomes feasible. However, there are still considerable challenges before reaching this milestone. One of them is to fabricate ultra small tunnelling junctions in silicon for high temperature operation. So far, the most common method is to use pattern dependent oxidation (PADOX) to reduce the junction size after EBL patterning [11]. This process might have a problem in the control of junction size. In this work, we proposed a novel process using EBL to pattern SET devices followed by a dry-etch on both the depth and the sidewall of the junctions to further reduce its size in a much more controllable method. Junctions as small as 10 nm can be readily achieved by this process. Initial measurement of *I–V* curves also proved that such small junctions are still functional.

2. Nanofabrications of SETs on SOI

2.1. Electron beam lithography to pattern small junctions

Fig. 1 demonstrates the process flow for the fabrication of SOI SET devices. The SOI substrate used has a n-type 50 nm thick Si capping layer on a (1 0 0) Si surface, sandwiched by a 300 nm thick buried oxide layer. The carrier density of the Si capping layer is $2 \times 10^{19}\,\mathrm{cm}^{-3}$ and the resistance is $3 \times 10^{-2}\,\Omega\,\mathrm{cm}$. A bilayer of PMMA resists (the molecular weight of 100k on the bottom and 350k

* Corresponding author. Tel.: +86 010 82995578; fax: +86 010 62055666.
E-mail address: LiuMing@ime.ac.cn (M. Liu).

0167-9317/$ - see front matter © 2007 Elsevier B.V. All rights reserved.
doi:10.1016/j.mee.2007.01.261

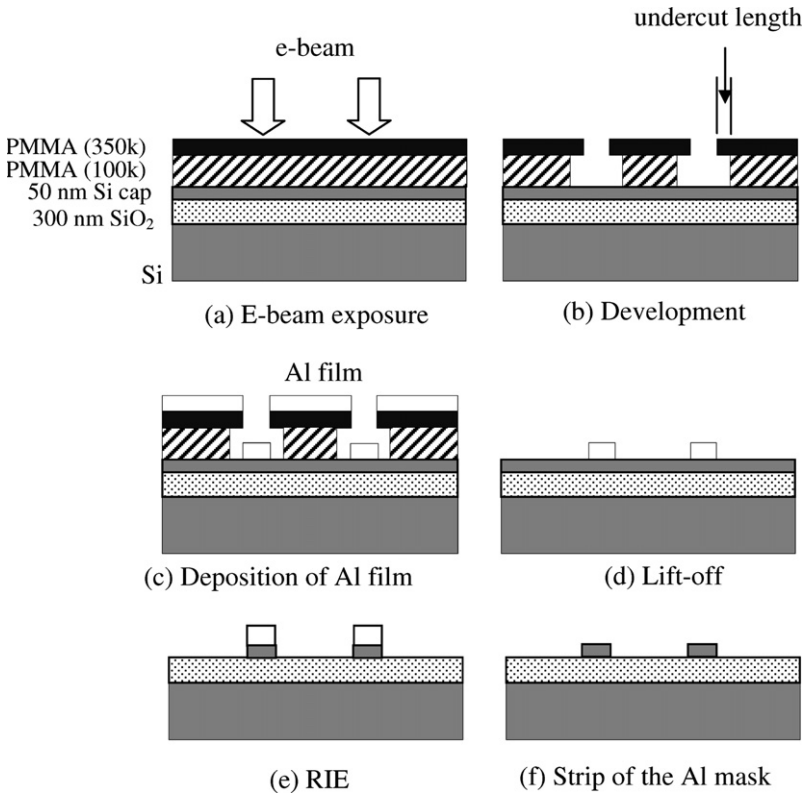

Fig. 1. Schematic diagram showing the process flow for the fabrication of SOI SETs. In this process, step (e) involves both vertical and horizontal etch which will be described in detail in Fig. 6 as well as in the text.

on the top) was first spin coated on the SOI substrate and baked at 180 °C for one hour in oven. A high resolution electron beam lithography system, VB6 HR from Leica Cambridge was used to write the SET patterns at the electron beam acceleration voltage of 100 kV and the beam current of 500 pA. Development was carried by a standard MIBK:IPA (1:3) developer at room temperature, followed by rinse in IPA for 30 s and finally blow dry by a compressed air. As shown in Fig. 2, a clear undercut profile in such a bilayer resist can be achieved, which is essential for the success of lift-off process after metallisation when the feature size is below 50 nm. This undercut was created due to the difference in e-beam sensitivities of these two layers as shown by their contrast curves in Fig. 3. Fig. 4 shows the junction size as the function of the exposure dose in the EBL. Apparently the reliable dose window locates in 2500–3500 mC/cm^2 where the slope is relatively lower, corresponding to 30–40 nm junction size. Based on this result, a further reduction of the junction size was attempted by developing a novel reactive ion etch (RIE) process, which will be discussed in the following section.

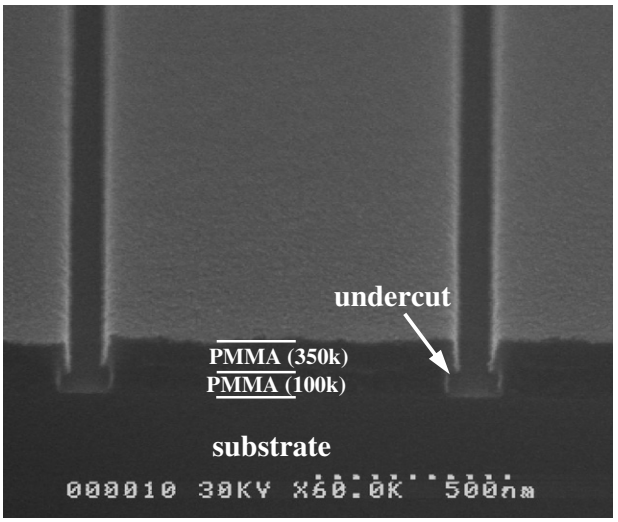

Fig. 2. A bilayer of PMMA(100k)/PMMA(350k) shows an undercut in the resist profile caused by the difference of e-beam sensitivity between the two resists during EBL process. This undercut is imperative to ensure the success of lift-off for nanometallic structures.

2.2. A reactive ion etch process for ultra small tunnelling junctions

As shown in Fig. 1, the step of metallisation was carried out by a deposition of 30–40 nm thick metal film after the EBL process. A Cr film was first chosen. Unfortunately it was found that the yield for successful lift-off was low when Cr was used. There was always some unwanted Cr remained in the central part of the SET pattern as indicated in Fig. 5a. However, when Al film was adopted, the resultant pattern was always clear (Fig. 5b). More importantly, the Al film can be slowly etched in the fluorine based

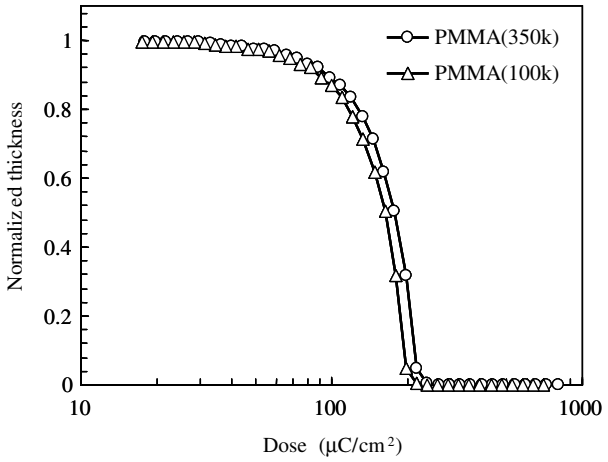

Fig. 3. The contrast curves of the two resists used in this work: PMMA(100k) symbolised by the open triangles and PMMA(350k) by the open circles. As can be seen that there is a clear difference in the sensitivity which was used for the form of undercut profile in this work.

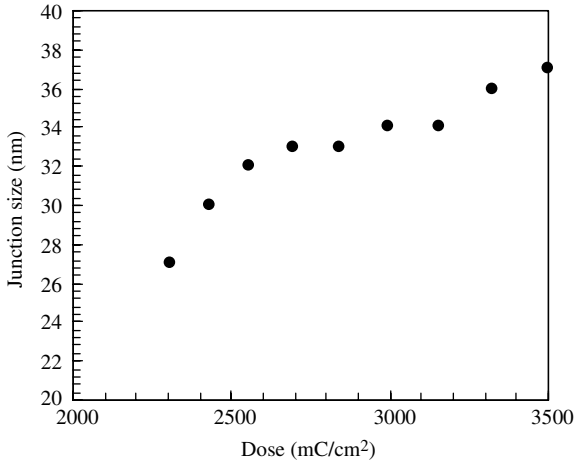

Fig. 4. The junction size as the function of exposure dose by electron beam in the EBL process. In the dose range of 2500–3500 μC/cm^2, the junction size changes relatively slowly with the dose, indicating a good CD control.

plasma, which offers us a good opportunity to reduce the junction size further by a controllable sidewall etch.

Fig. 6 schematically demonstrates how the junction was reduced horizontally when carrying out a vertical etch to transfer the SET pattern from the Al layer onto the 50 nm thick superficial silicon layer. In this dry-etch step, a SYS90 dry-etcher from the Oxford Plasma Technology (OPT) was used. The etching gas is the mixture of C_2F_6 and CHF_3, in which the C_2F_6 species does the etching and the CHF_3 does the passivation on the sidewall so that it is an anisotropic dry-etch. However, it was found that Al can be slowly etched in fluorine plasma, especially on the edge as illustrated in Fig. 6b. The erosion happening on the Al edge gradually reduces the feature size on the junction; consequently the junction becomes narrower and narrower. It is even possible that the erosion speed is faster than the etch rate on the Al top because etch happens on both the top and the sidewall of the Al edge. The etch rate on Si is measured to be 9–10 nm/min and the etch rate on Al is estimated to be slightly over 1 nm/min in contrast to that on Cr film (<0.5 nm/min). This etch property corresponds to the optimum condition: that is the ratio of C_2F_6 over CHF_3 is 2, the pressure is 30 mTorr and the rf power is 150 W. In the etch on the SOI for real SETs, 10 min etch time was used to make sure the 50 nm thick silicon layer was etched away and part of oxide was also removed to minimise the leakage current between the

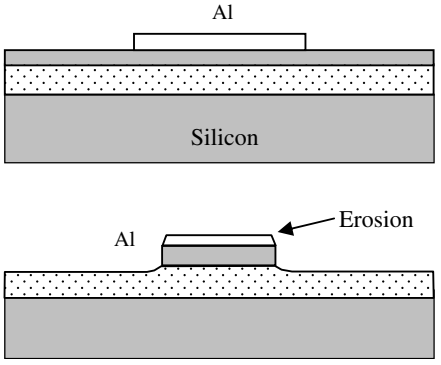

Fig. 6. A schematic demonstration of size reduction for the junctions during the RIE etch process. Due to the slow erosion of Al edge in fluorine gas the wire width in silicon is naturally and controllably shrunk. (a) The cross sectional view of the junction area before the RIE; (b) the junction is formed by a RIE etch in fluorine based plasma and meanwhile the junction size is reduced when the Al etch mask becomes narrower due to the erosion on the edge.

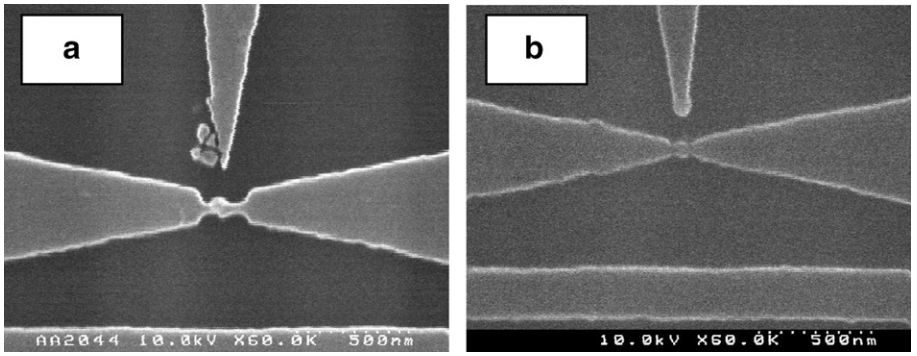

Fig. 5. The comparison of fabrication results using (a) Cr film and (b) Al film. The Al film gives rise to much higher yield in the lift-off process.

source and the drain. The total height of the mesa was measured as 90 nm by a Tancor Stepper. At the same time, the lateral size of the junction is reduced by 10–20 nm. Fig. 7 shows the central part of the fabricated SET device with both top view (Fig. 7a) and tilted view (Fig. 7b). The junction size is so small that the silicon looks transparent (Fig. 7b). We also undertook some over-etch tests and achieved break junctions with the spacing of less then 10 nm as shown in Fig. 7c.

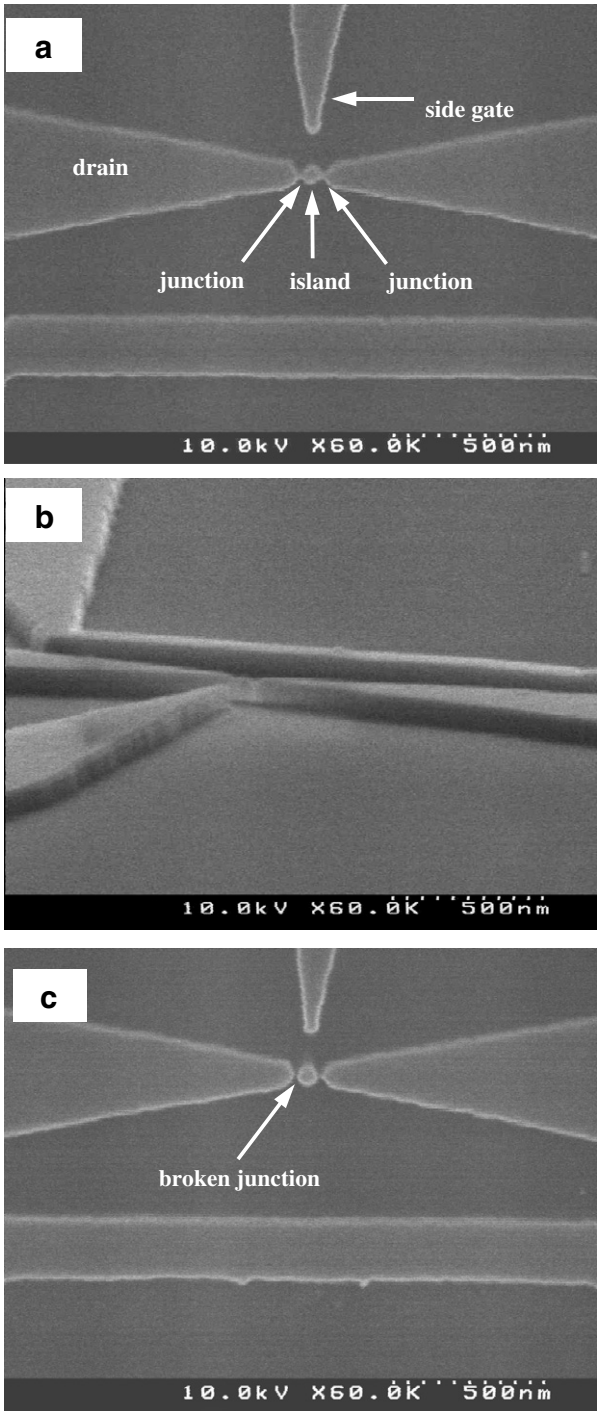

Fig. 7. Micrographs of scanning electron microscope for the fabricated SET device on SOI substrates. (a) The top view, (b) the tilted view and (c) the break junction under over etched condition.

3. Characterisation and discussion

One of the concerns in this process is whether the dry-etch process could cause damage to the silicon layer in the SOI substrate. To investigate the effect of the RIE on the electric transport property, initial characterisation was carried out on the fabricated SETs in a cryogenic system, using a Keithley semiconductor parameter analyzer. The I_{ds}–V_{ds} curve was measured as shown in Fig. 8. A clear Coulomb blockade gap corresponding to zero current was measured. Also demonstrated in Fig. 8 is the differential I_{ds}–V_{ds} curves which show some Coulomb staircases in I_{ds}. The Coulomb gap voltage, ΔV, of the SET is about 0.12 V. This result indicates that the fabricated SETs are functional and the RIE in this process did not damage the thin and narrow silicon line.

However, in the linear part of the I–V curves, the junction resistance is measured to be 1000 MΩ, which is higher than expected. There are many reasons causing high junction resistance. The electric property of the 50 nm silicon on insulator should be first responsible for the junction resistance. The mobility of the thin silicon layer could be low due to the boundary scattering of electrons localised in the thin layer, resulting in too high junction resistance. The edge roughness on the junction sidewall may introduce boundary scattering to the electrons, increasing the constriction resistance. A technique using oxidation/wet-etch process may offer a solution to smooth the etched junction. To improve the device performance, a high quality SOI material is definitely needed. To minimise the damage effect and sidewall roughness, lower power and lower pressure should be applied in the plasma dry-etch. Nevertheless, our results significantly indicate that the developed nano-fabrication technique is capable of manufacturing ultra small SET devices in SOI substrates.

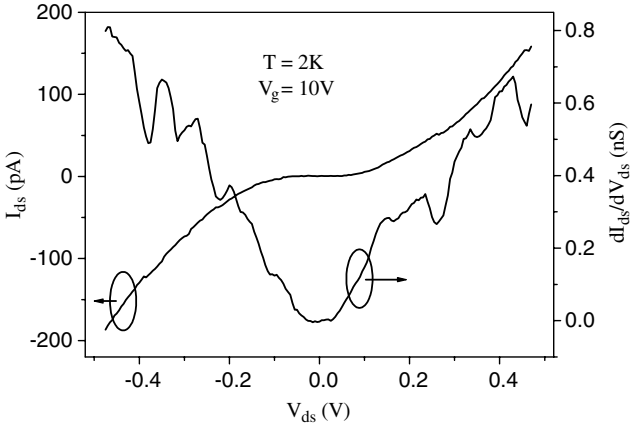

Fig. 8. The I_{ds}–V_{ds} and dI_{ds}/dV_{ds}–V_{ds} characteristics at $V_g = 10$ V, measured at the temperature of 2 K.

4. Conclusions

A novel process for the fabrications of SETs on SOI with 10 nm tunnelling junction size has been developed. This process has the advantages of being very simple, controllable, reliable and applicable for actual device manufacture. Initial characterisation of the fabricated SET devices at low temperature shows the device is functional. We believe that the device performance should be greatly improved when a high quality SOI substrate is used. The developed process for single electronics should have the prospect to combine with the existing CMOS technique for the fabrications of new generation devices and circuits in the future.

Acknowledgements

The authors thank Mr. Liwei Liu and Mr. Jinghai Fang of Institute of Physics, Chinese Academy of Sciences for the measurement of the electrical characteristics of the SET. The work was financial supported by the National Science Foundation (60506005) and National Basic Research Program (2006CB302706).

References

[1] Yukinori Ono, Yasuo Takahashi, Kenji Yamazaki, et al., IEEE Trans. Electron Dev. 47 (2000) 147.
[2] Lingjie Guo, Effendi Leobandung, Stephen Y. Chou, Science 275 (1997) 649.
[3] Henk W.Ch. Postma, Tijs Teepen, Zhen Yao, et al., Science 293 (2001) 76.
[4] K. Nakazato, R.J. Blaikie, J.R.A. Cleaver, H. Ahmed, et al., Electron. Lett. 29 (1993) 384–385.
[5] J.R. Tucker, J. Appl. Phys. 72 (1992) 4399–4413.
[6] R. Knobel, A.N. Cleland, Nature 424 (2003) 291–293.
[7] A. Cho, Science 299 (2002) 36–37.
[8] X.M.H. Huang, C.A. Zorman, M. Mehregany, M.L. Roukes, Nature 421 (2003) 496.
[9] T.A. Fulton, P.L. Gammel, D.J. Bishop, Phys. Rev. Lett. 63 (1989) 1307.
[10] K. Likharev, D.B. Strukov, Introducing Molecular Electronics, Springer LNiP, 2006, in preparation.
[11] K.S. Park, S.J. Kim, I.B. Back, W.H. Lee, J.S. Kang, et al., IEEE Trans. Nanotechnol. 4 (2005) 242.