VDTT (JVL/JVY) Admissions, IIT Delhi
Written screening, 2022

1. An ADC has a sampling rate of 10 kHz. The frequency of the analog input is 8 kHz. What is the fundamental frequency observed at the output of the ADC?

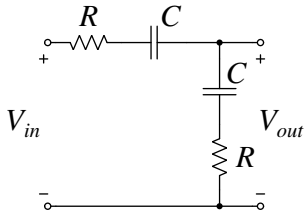
   A) DC

   B) 2 kHz

   C) 8 kHz

   D) 12 kHz

2. In the circuit shown in the figure below, what is the 3-dB bandwidth of V_{out}/V_{in}?



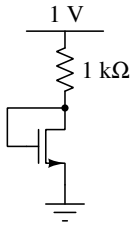
   A) $1/(RC)$

   B) $1/(2RC)$

   C) ∞

   D) $2/(RC)$

3. In the circuit shown in the figure below, the nMOS device has V_{TH} of 0.2 V, $\mu_n C'_{ox} W/L$ of 200 μA/V^2. What is the current in the nMOS device?



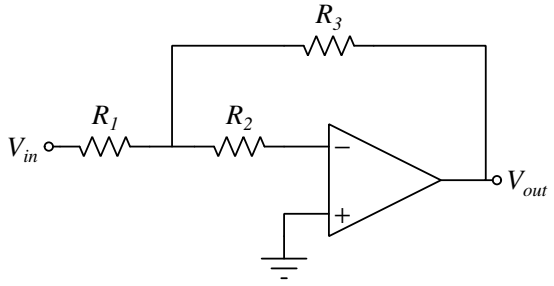
   A) 0.0554 mA

   B) 1 mA

   C) 0.707 mA

   D) 1 mA

4. In the circuit below, what is V_{out}/V_{in}?



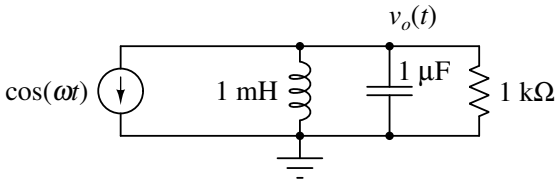
A) $-R_3/(R_1 + R_2)$

B) $-R_3/R_1$

C) $R_3/(R_1 \parallel R_2)$

D) $-(R_3 \parallel R_2)/R_1$

5. In the circuit below, ω is the resonant frequency of the RLC circuit. The highest value of $v_o(t)$ is:



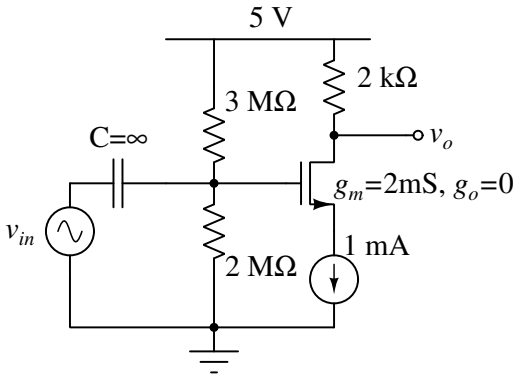
A) 1 mV

B) 100 mV

C) 10 V

D) 1 kV

6. What is the small signal gain, v_o/v_{in}, of the circuit shown in the figure below?



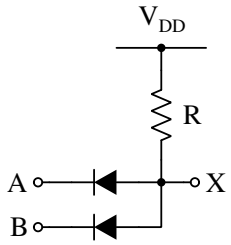
A) -2

B) 2

C) 0

D) ∞

7. The circuit shown in the figure below is a/an:



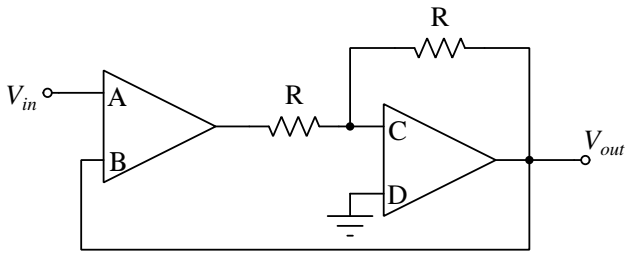
A) AND gate

B) NAND gate

C) OR gate

D) NOR gate

8. The voltage gain, V_{out}/V_{in}, of the circuit in the figure below is approximately 1. Which of the following statements is true?



A) A, C are negative; B, D are positive.

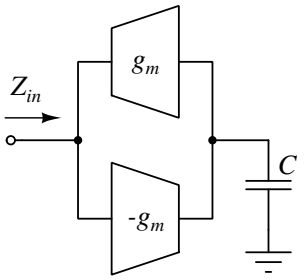
B) A, D are negative; B, C are positive.

C) B, C are negative; A, D are positive.

D) B, D are negative; A, C are positive.

9. Which of the following statements is true about the circuit shown in the figure below? Z_{in} represents the impedance of the circuit while

looking in the direction of the arrow.



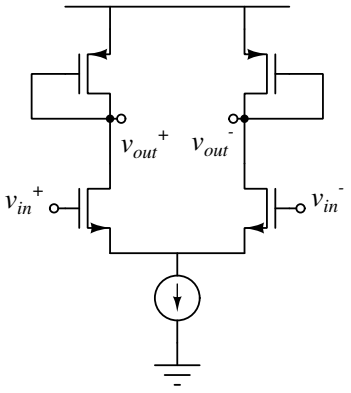
A) $Z_{in} = sC/g_m^2$ and the impedance behaves like an inductor.

B) $Z_{in} = g_m^2/sC$ and the impedance behaves like a capacitor.

C) $Z_{in} = g_m^2/C$ and the impedance behaves like a resistor.

D) $Z_{in} = g_m/sC$ and the impedance behaves like a capacitor.

10. In the circuit shown below the transconductances of of the nMOS and pMOS devices are the same. The output resistance of the nMOS and pMOS devices are the same. g_{mb} is 0. The differential voltage gain, $(v_{out}^+ - v_{out}^-)/(v_{in}^+ - v_{in}^-)$ is:



A) -1

B) 1

C) -1/2

D) 2

11. A Miller compensated OTA with a unity gain bandwidth of 20 MHz has a g_m of 250 μS in its first stage. The compensation capacitor used is approximately:

A) 1 pF

B) 2 pF

C) 3 pF

D) 5 pF

12. The source of a MOS device biased in saturation is terminated with a resistance R. The small signal incremental impedance looking into the drain of the circuit is:

A) $R + r_{ds} + g_m r_{ds}$

B) $\frac{r_{ds}+R}{1+g_m r_{ds}}$

C) $1/g_m$

D) $R + 1/g_m$

13. In a 2-stage cascode current mirror designed with pMOS devices, the maximum voltage tolerable at the output of the circuit, such that the circuit works as a current source, is:

A) $V_{DD} - 2V_{GST}$

B) $V_{DD} - V_{GST} - V_T$

C) $V_{DD} - 2V_{GST} - 2V_T$

D) $V_{DD} - 2V_{GST} - V_T$

14. An n-channel MOS device is biased at the edge of saturation (i.e., pinch-off.) The C_{gd} of the device is:

A) $2C_{ox}/3$

B) $C_{ox}/2$

C) $C_{ox}/3$

D) $C_{ox}/4$

15. Evaluate the following integral in a counter-clockwise loop given by $|z - 1| = 1$.

$$\oint \frac{2z}{z^2 - 1}\, dz$$

A) $4\pi j$

B) $2\pi j$

C) 0

D) $-2\pi j$

16. The setup time of a flip-flop is 10 ps, the hold-time is 50 ps, the delay of the flip-flop is 10 ps. The delay of logic circuits in feedback is 70 ps. What is the maximum frequency of the clock that can be used to operate the state-machine correctly?

    A) 7.1 GHz

    B) 7.7 GHz

    C) 11.1 GHz

    D) 14.2 GHz

17. A traffic light signal has a three-digit BCD seconds counter that can count down from 120 to 0 seconds. What is the minimum number of flip-flops that are required to operate this counter?

    A) 12

    B) 9

    C) 8

    D) 7

18. What is the asymptotic time complexity of the merge-sort algorithm?

    A) $O(N)$

    B) $O(N \log N)$

    C) $O(N^2)$

    D) $O(1)$

19. What is the best (fastest) way of finding the third-largest number in an unsorted array?

    A) Sort the array and then find the number that is the third from the top.

    B) Make a single pass on the array and use a small decision tree.

    C) Make two passes on the array.

    D) Make three passes on the array.

20. What is the advantage of the 2's complement notation?

    A) It has a single representation for 0.

    B) Multiplying two signed numbers is equivalent to multiplying their unsigned representations (in a 2's complement form).

C) Subtraction is easy.

D) All the options.