A 9 GS/s 2.1..2.2 GHz Bandpass Delta-Sigma Modulator for Class-S power amplifier

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***Abstract* — A tunable fourth-order bandpass delta-sigma modulator (BDSM) designed and fabricated in 0.25 um SiGe BiCMOS technology is presented. The input band can be tuned in a range of 2.1 to 2.2 GHz while clocking at 9 GHz. The modulator achieves 42-43 dB signal-to-noise ratio (SNR) in 10 MHz bandwidth with sine wave input over the tuning range consuming 270 mW from -3 V supply. Measurement results show that the circuit is well suited for Class-S power amplifier applications using WCDMA coding scheme. For a WCDMA modulated signal the modulator demonstrates less than 2.3 % of EVM over the full tuning range.**

***Index Terms* — bandpass ADC, sigma-delta modulation, continuous time, class-S, power amplifiers, WCDMA**

I. Introduction

Bandpass delta-sigma modulators (BDSM) are becoming very attractive for the analog-to-digital conversion in the receiver path because of high accuracy in a limited band and low power consumption. Early investigations were focused on the use of BDSMs for processing of the intermediate frequency signals in heterodyne receivers [1]. Only recently with the rapid development of the semiconductor technologies it is becoming possible to implement modulators for higher frequency. Recent investigations have led to use a modulator (as the component of a receiver which is closest to the antenna) at 2 GHz input frequency [2]. Applying a BDSM at this carrier frequency range is an significant step towards software defined radio in 3rd generation cellular networks. The same tendency could be observed in the transmitter path where a BDSM has also found its application. Highly efficient switching Class-S power amplifiers (PA) are using BDSM as an input stage that converts an analog input signal into a digital sequence, as shown in Fig. 1.

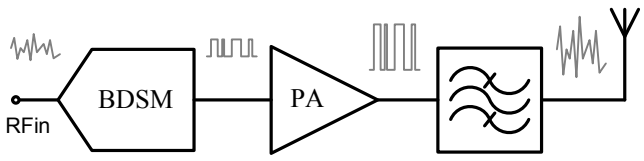

Fig. 1. Class-S BDSM-PA architecture

A Class-S system implementing a BDSM allows to process signals coded with non-constant envelope modulation schemes. Also using a BDSM in a Class-S PA relaxes the requirements to the switching stage in contrast to the same PA using pulse-width modulation (PWM-PA). For a PWM-PA the pulses at the input of an amplification stage could be very short which requires very high f_T to process a modulated signal. For a BDSM-PA the minimum pulse length at the input of an amplifier is just one clock period, which is a substantially less demanding constraint on the f_T of the PA. Thus BDSM appears to be the architecture of choice for class-S PAs at high clock rate.

II. Design strategy

Delta-sigma modulators at high frequency require a design procedure involving both system and circuit level. Modeling on transistor level takes into account realistic effects but suffers from the low simulation speed. System level design benefits by simulation time but does not provide sufficient simulation accuracy to predict the signal quality parameters. Only the synergy of both levels can lead to the most efficient design flow, as depicted in Fig. 2.

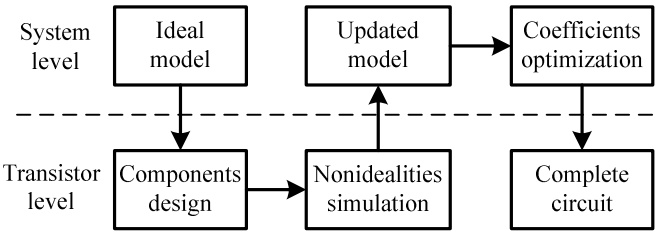

Fig. 2. BDSM design procedure

For the BDSM we have chosen 4th order $f_s/4$ LC architecture (Fig. 3) with RZ and HRZ pulses in a feedback path [3]. Fig. 3 shows the basic architecture, which had already been used in our previous BDSM for 450 MHz carrier frequency and 1.8 GHz clock. This BDSM was successfully implemented in a Class-S PA system [4]. For ideal model the transfer function (1) was used.

$$H_{BP}(z) = \frac{2z^{-2} + z^{-4}}{\left(1 + z^{-2}\right)^2} \qquad (1)$$

A continuous-time equivalent of (1) was obtained the way described in [5]. For an estimation of parasitic effects, the resonator, comparator, and DACs were designed and modeled on the circuit level. The jitter, excess loop delay and finite quality factor of the resonator are the main non-idealities that affect the performance of a BDSM. An estimation of those parameters will be discussed in detail in the next section. For taking real effects into account the transfer function has been changed and a coefficient optimization was done to improve the performance of the modulator.

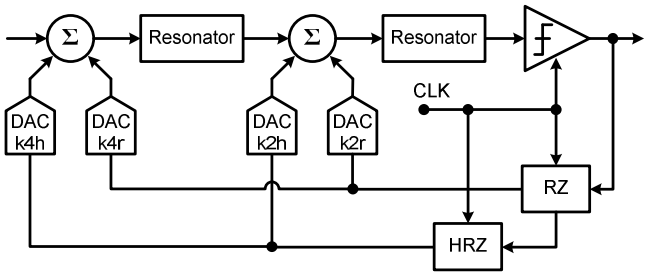

Fig. 3. Fourth order LC continuous-time BDSM architecture

All simulations were done in Cadence environment, allowing simultaneous use of behavioral and transistor-based models. For the system-level design component blocks were described in Verilog-A. Transient analysis was performed by the Cadence Spectre simulator.

III. Circuit design and non-idealities estimation

A fully differential circuit configuration was used to provide high common-mode noise rejection. All current sources were designed as CMOS circuits. This allows a low supply voltage without saturation of the transistors.

A. Resonator finite quality factor

The complete resonator structure consists of two gm-cells and an LC tank, including varactors (Fig. 4*a*). To improve the dynamic range of the resonator a gm-cell was designed as a multi-tanh structure (Fig. 4*b*). The linearity of the gm-cell can be controlled to some extent by unbalancing the differential pairs and the emitter degeneration. Since the supply voltage was fixed to 3 V it is possible to use effectively only one diode in the emitter. So only the tail current and emitter area ratio between left side and right side transistors were optimized.

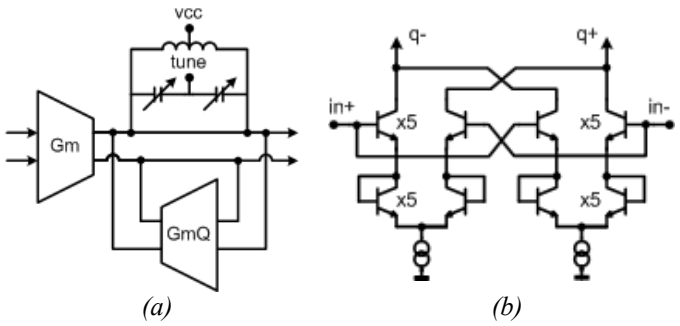

Fig. 4. (a) resonator sturcuture; (b) gm-cell schematic

The LC tank includes a symmetrical octagonal inductor and varactors to cover WCDMA base station transmitter frequency range (2.11..2.17 GHz). The octagonal inductor has an inductance of 4.7nH and consists of two thick layers connected in parallel in order to minimize resistive losses. Occupying an area of 220 x 220 um^2 the optimized coil has a quality factor of only 12 at 2.1 GHz. Since a low quality factor of the tank highly degrades an SNR it is necessary to compensate losses in the inductor. For this reason an additional gm-cell GmQ was connected as positive feedback (Fig. 4*a*). It is also based on the multi-tanh structure but uses four times bigger transistors and a 4-to-1 capacitive divider at the input. Both gm-cells have controlled currents to externally change gain and quality factor. The designed resonator has a maximum quality factor of 50. On the system level the transfer function of a resonator is described by (2).

$$H(s) = \frac{As}{s^2 + \frac{\omega_0}{Q}s + \omega_0^2} \qquad (2)$$

where ω_0 is the center frequency, A – constant gain factor, Q – quality factor of the resonator. Having a very high quality factor will bring the transfer function (2) to a form of an ideal resonator.

B. Comparator and DACs

A comparator was designed as a standard ECL master-slave latched circuit with preamplifier. The transistors in the latch were biased for peak f_T. The optimization of the recovery time of the comparator has lead to a load resistor of 100 Ohm at 200 mV output swing. In simulation the comparator has shown a sensitivity value of 1 mVpp at 2 GHz input frequency while clocking at 15 GHz.

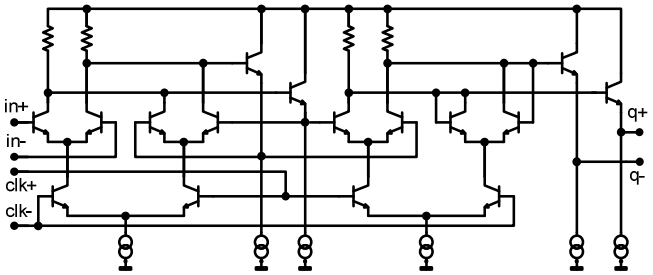

Fig. 5. Schematic of the RZ (HRZ) block.

RZ and HRZ blocks are clocked in anti-phase and based on the comparator structure. The difference is that in the slave part the cross-coupled latch transistors are replaced with diode-connected transistors [6] (Fig. 5). The DAC circuit is a simple differential pair with adjustable current in the range of 0.2 - 4 mA.

In simulation the estimated excess loop delay was $0.15T_S$. This value was taken into account in the system level model.

C. Jitter

The main source of jitter is the external clock signal generator. The measured peak-to-peak jitter value for the 9 GHz clock frequency was 2.9 ps. This corresponds to $\sigma = 4.3x10^{-3}T_S$ in the Gaussian distribution. Based on that value the jittered source was modeled and used in a system model. Using this clock source model an SNR degradation of 8.5 dB in a 10 MHz bandwidth was observed in comparison to the modulator clocked by a jitter-free source.

After the feedback coefficients tuning the final simulated maximum SNR was 53 dB in 10 MHz bandwidth. A simulation on transistor level has shown a maximum SNR of 40 dB in 80 MHz bandwidth. Scaling to 10 MHz we obtain an SNR value of 49 dB.

IV. Experimental Results

The modulator was fabricated in a 0.25 um SiGe BiCMOS process (f_T=180GHz) with three thin and two thick metal layers [7]. Fig. 6 shows the microphotograph of the BDSM. The occupied area is 1.4 mm^2.

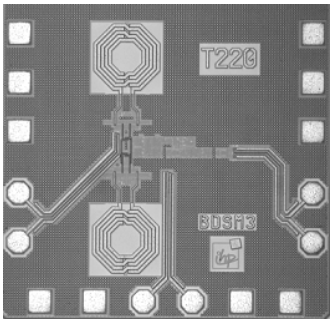

Fig. 6. Chip photo of the BDSM.

The BDSM consumes 90 mA current from -3 V supply voltage. The chip was mounted on the Rogers RO4003 printed circuit board with a thickness of 0.51 mm. Measurements were done under different conditions as described in the next subsections.

A. Sine wave input

For a sine wave input we estimated the modulator performance by measuring the SNR in a 10 MHz bandwidth. The output data have been captured from an oscilloscope controlled by Matlab and SNR values have been calculated.

For an estimation of the SNR 40 us of the output signal were saved and a Fourier transform was performed. To measure dynamic performance the input amplitude was changed and the corresponding SNR values were measured. Fig. 7 shows the measured SNR curves for 2.1 and 2.2 GHz input frequencies. For both measurements the modulator notch was tuned to the input frequency. The difference between simulated and measured SNR of about 5 dB can be attributed to layout parasitics, PCB imperfections and technology mismatches of the fabrication process.

A spectrum of the output signal obtained with a spectrum analyzer is shown in Fig. 8.

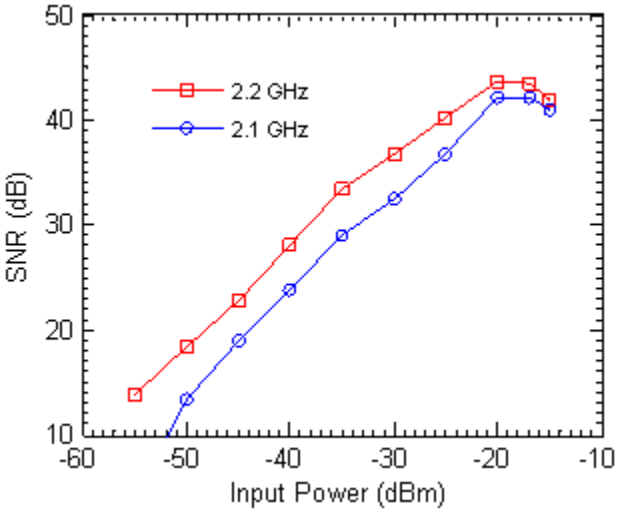

Fig. 7. Measured signal-to-noise ratio for sine wave input signal in 10 MHz bandwidth at 2.1 and 2.2 GHz input frequency and 9 GHz clock.

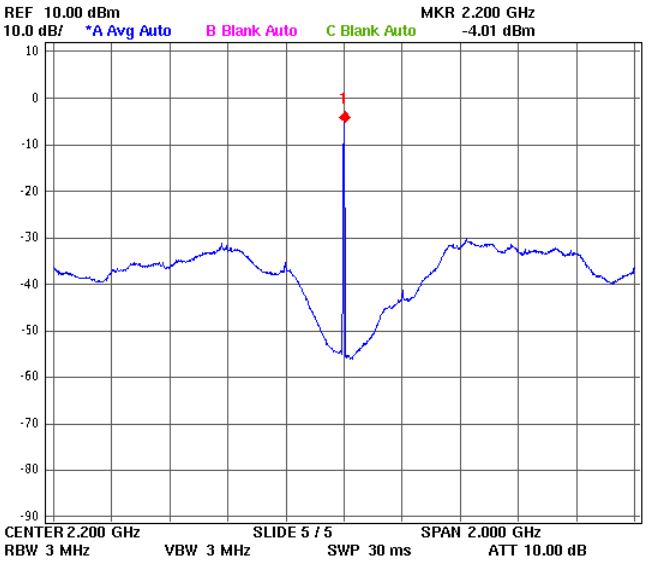

Fig. 8. Measured output spectrum of the BDSM at Pin = -20 dBm

B. WCDMA input signal

To define the conformance of a BDSM as a Class-S PA driver a real WCDMA signal must be applied and the error vector magnitude (EVM) value must be measured. The signal was generated according to the Test Model 5 [8]. This model is used to perform EVM measurements for base station

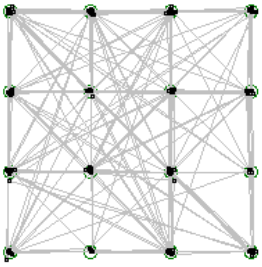

Fig. 9. Output signal constellation for WCDMA signal modulated by QAM16.

transmitters. We have used a model configuration which consists of 8 high-speed physical channels and 30 dedicated physical channels. Data in the high speed channels are modulated by 16QAM. Such a configuration allows measuring the BDSM under the most stringent conditions, since the peak-to-average ratio is maximal for such a signal and equals to 11.5. With a help of Agilent ADS the WCDMA signal was generated and uploaded to an ESG4433C signal generator. The output signal was captured and analysed by an Agilent Vector Signal Analyzer and VSA Software. The measured constellation diagram is shown in Fig. 9.

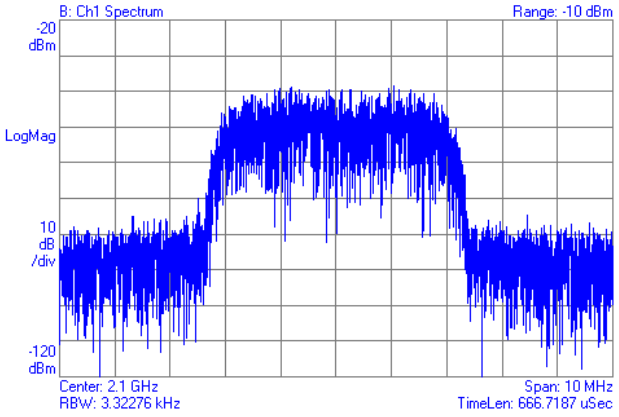

Fig. 10. Measured output spectrum of the WCDMA signal modulated by QAM16.

TABLE I
BDSM PERFORMANCE SUMMARY

Process	0.25 um SiGe BiCMOS
Notch frequency range	2.05..2.22 GHz
Sampling frequency	9 GHz
Supply Voltage	-3 V
Power Consumption	270 mW
Output swing, diff	0.8 V
Chip area	1.4 mm^2
DR	45 dB
SNRmax BW = 10 MHz	42 dB @ 2.1 GHz 43 dB @ 2.2 GHz
EVM (QAM16)	2.3% @ 2.1 GHz 1.7% @ 2.2 GHz

The designed bandpass delta-sigma modulator introduces lower than 2.3 % EVM at Pin = -30 dBm over the full tuning range. It is a very good value taking into account that a complete PA module must have the EVM lower than 12.5 % while transmitting WCDMA signal modulated by QAM16. The corresponding signal spectrum is shown in Fig. 10.

V. CONCLUSION

We have presented the design and measurement results of a tuned LC continuous-time BDSM for a class-S power amplifier. The modulator clocked at 9 GHz has a tuned notch in a 2.1-2.2 GHz frequency range. Non-idealities like jitter, finite quality factor of coils and excess loop delay were taken into account during the modeling phase. The successfully integrated and measured BDSM has demonstrated the ability to act as an input driver in a class-S power amplifier system for WCDMA signals. To the authors' knowledge this is the first BDSM for a switched-mode PA operating at 2 GHz.

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