A 16-mW 8-Bit 1-GS/s Subranging ADC in 55nm CMOS

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Abstract

An 8-bit subranging ADC was fabricated using a 55nm CMOS technology. To enhance speed, subranging is executed by activating comparators in the digital domain. To save power, comparators are latches with automatic offset calibration. Operating at 1GHz sampling rate, the ADC consumes 16mW from a 1.2V supply. The measured DNL is 0.8LSB and INL is 1.2LSB. The measured SFDR and SNDR are 55dB and 43.5dB respectively. The ADC occupies an active area of 0.2mm^2. Its FOM is 125fJ/conversion-step.
Keywords: Analog-digital conversion, subranging ADC, comparators (circuits), calibration.

Introduction

High-speed analog-to-digital converters (ADCs) can be realized in various architectures [1, 2]. A flash ADC consisting of only comparators can achieve high sampling rate. Its sampling interval can be as short as one comparison cycle. Its total number of comparators increases exponentially with the number of resolution bits. The subranging architecture can reduce the number of comparators by increasing the sampling time to two comparison cycles. Its speed is further hindered by the delay of the reference switching network. This reported ADC makes use of the subranging architecture but avoids the reference switching network. Its subranging function is executed by activating comparators in the digital domain. To save power, comparators are latches with automatic offset calibration. Although the proposed architecture does not reduce the number of comparators, it can achieve higher conversion rate while consumes less power.

Architecture

Fig.1 shows the 8-bit ADC block diagram. This ADC includes a coarse ADC (CADC) and a fine ADC (FADC). The CADC consists of 15 coarse comparators (CCMPs). It is supplied with 15 V_{RC} references that divide the ADC full input range into 16 subranges. Unlike conventional subranging ADCs, the FADC consists of 255 fine comparators (FCMPs). It is supplied with 255 V_{RF} references that spans the entire ADC input range. A resistor string generates both the V_{RC} and the V_{RF} references. There are no analog switches to select a subrange of V_{RF} references for the FADC. The speed of a subranging ADC is usually limited by delays of those switches.

As shown in Fig.1, the ADC operation is controlled by two non-overlapping global clocks, ϕ_1 and ϕ_2. Additional global clock ϕ_c controls the CADC. A track-and-hold (TAH) samples the ADC analog input V_i on the falling edge of ϕ_1. The resulting output is V_1. The CADC compares the sampled voltage V_1 with the V_{RC} references on the rising edge of ϕ_c in the ϕ_2 period. The subrange selector uses the comparison result

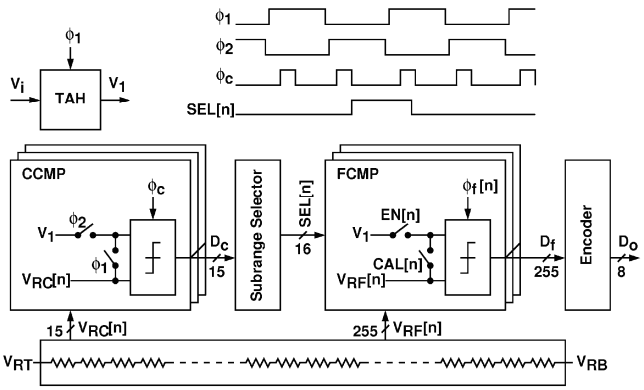

Fig.1. ADC block diagram.

D_c to determine which subrange V_1 is located in. Its outputs are 16 SEL[n] digital activation signals, where n is an integer between 1 and 16. The 255 FCMPs in the FADC is divided into 16 banks. The n-th bank is activated by SEL[n]. Only two banks, i.e., 32 FCMPs, are activated simultaneously each time. The overall input range of the activated FCMP banks covers the selected subrange and spans twice the subrange. This over-range protection relaxes the accuracy requirement for the CADC. For the disabled FCMPs, their digital outputs are set by SEL[n] directly, so that the entire 255 D_f outputs appears as a thermometer code. Finally, an encoder converts D_f into the ADC output D_o.

Circuit Implementation

The TAH shown in Fig.1 consists of a passive switch-capacitor track-and-hold followed by a voltage buffer. Bootstrapped switches are used to improve sampling speed and linearity. The two hold capacitors are metal-oxide-metal capacitors of 250fF. Two source followers function as a differential voltage buffer that drives both CADC and FADC.

Fig.2 shows the FCMP block diagram. To improve power efficiency, the comparator uses a single regenerative latch to provide the comparison function. It has no preamplifier. The offset of the latch is eliminated by an offset calibration charge pump. The FCMP is activated by a SEL signal from the subrange selector. Internal control signals such as EN, CAL, and ϕ_f are generated locally in each FCMP bank. The latch is triggered on the rising edge of ϕ_f. Upon the arrival of SEL=1, S1 is closed when EN=1. The latch makes a data comparison that compares V_1 with its V_{RF}. The comparison result is sent to the ADC encoder. After that, the S2 switch is closed when CAL=1. The latch makes an additional comparison with both inputs connected to V_{RF}. This comparison, called calibration comparison, detects the polarity of the latch offset and generates an up/down pulse, A_p/A_n, to charge/discharge capacitor C_b. The resulting voltage on the capacitor, V_c, adjusts the latch offset. Eventually, V_c will approach to a steady-state

value, making the latch offset approach zero asymptotically. Capacitor C_b is a low-leakage thick-oxide MOS capacitor of 0.5pF. The charge and discharge current, I_p and I_n, are about 1μA. The pulse width of Ap/An depends on the magnitude of the equivalent latch offset.

Fig.3 shows the schematic of the latch in FCMP. There are three input source-coupled pairs (SCPs). Two SCPs receive the differential input V_a and differential reference V_{RF}. The third SCP receives the difference between V_c and V_{CM}, where V_{CM} is a common-mode reference and V_c adjusts the latch offset. MOSFETs M3, M7, and M15 are added to control the conducting currents when the latch is turned on by ϕ_f. Kickback noises at the inputs of the latch are also reduced. The schematic of the coarse comparator (CCMP) shown in Fig.1 is identical to the FCMP shown in Fig.2 and Fig.3.

Experimental Results

The 8-bit subranging ADC is fabricated using a 55nm CMOS technology. Fig.4 shows the chip micrograph and performance summary. The active area is 0.2mm^2. The ADC digital output D_o is down-sampled by a ratio of 32 and then delivered off-chip to a logic analyzer. Fig.5 shows the measured differential nonlinearity (DNL) and integral nonlinearity (INL) at 1GS/s with 10MHz sine wave input. Before comparator offset calibration, the DNL is -1/+65LSB and the INL is -38/+42LSB. When the offset calibration is enabled, the DNL is improved to -0.8/+0.8LSB and the INL is improved to -1.2/+1.2LSB.

Fig.6 shows the measured ADC dynamic performance at different input frequencies. The achieved SNDRs at 1GS/s are 43.5dB and 39.2dB for 1MHz and 500MHz input respectively. The ADC consumes 16mW from a 1.2V supply. It achieves a FOM (Power/Fs×2^{ENOB}) of 125fJ/conversion-step.

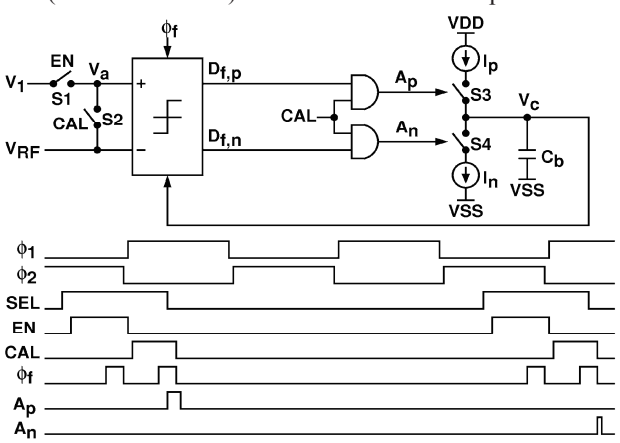

Fig.2. Fine comparator (FCMP) block diagram.

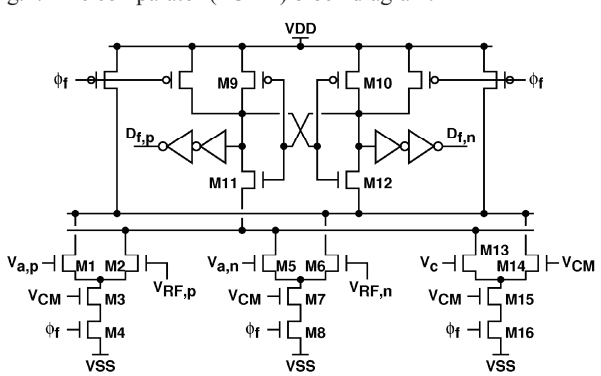

Fig.3. Schematic of the latch in fine comparator (FCMP).

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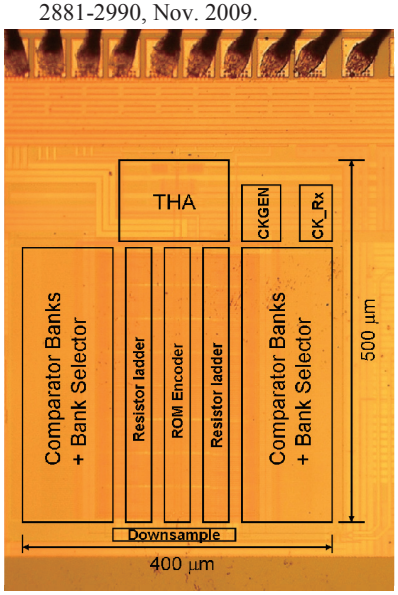

ADC Performance

Technology	55-nm
Resolution	8b
Sampling Rate	1 GS/s
Input Range	0.8 Vp-p
Input Loading	250 fF
SFDR	55 dB
SNDR	43.5 dB
DNL	0.8 LSB
INL	1.2 LSB
Supply	1.2 V
Power Dissipation	16 mW
ERBW	400 MHz
Active Area	0.2 mm^2
FOM	0.125pJ/conv-step.

Fig.4. Chip micrograph and performance summary.

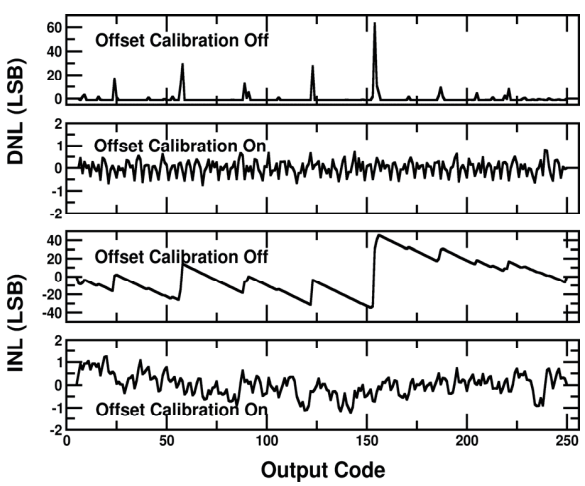

Fig.5. Measured DNL and INL.

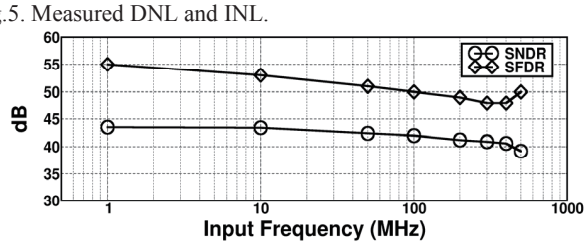

Fig.6. Measured dynamic performance vs. input frequency.