Analysis and Design of a High Speed Continuous-time $\Delta\Sigma$ Modulator Using the Assisted Opamp Technique

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***Abstract*—We apply the "assisted opamp technique" to the design of a 1 GS/s single-bit continuous-time $\Delta\Sigma$ modulator (CTDSM) that achieves 10 bit resolution in 15.625 MHz bandwidth. The enhanced linearity and speed of the first integrator of the modulator, necessitated by single-bit operation, are obtained in a power efficient manner using opamp assistance. However, timing-skew between the feedback and assistant DAC currents can be a potential problem at high speeds. We analyze and give intuition for the effects of timing mismatch in such CTDSMs, and show that opamp assistance is quite robust to timing errors. Measurement results from an implementation in a 0.13 μm CMOS process show that the modulator achieves a dynamic range of 67 dB in 15.625 MHz bandwidth while consuming 4 mW.**

***Index Terms*—Analog-to-digital converter (ADC), continuous-time circuit, continuous-time integrator, delta-sigma, distortion reduction, high speed, linearity enhancement, loop filter, oversampling, quantizer, sigma delta, 130 nm.**

I. Introduction

SEVERAL communication systems need medium resolution (9–12 bits) analog-to-digital converters (ADCs) with bandwidths in the tens of MHz range [1]–[3]. This combination of resolution and bandwidth were considered the exclusive forte of pipelined ADCs. Continuous-time Delta-Sigma modulators (CTDSM) are now being seen as attractive alternatives to pipelined converters in such applications. The latter family of ADCs needs high gain/speed operational amplifiers that are becoming increasingly difficult to realize in nanometer CMOS processes. Further, the switching input impedance of pipeline ADCs (or other ADCs employing switched-capacitor techniques) introduces additional challenges with respect to the circuitry driving the converter. These problems are avoided in a CTDSM, where the "burden" of having to achieve high loop-gain is distributed among several opamps. Since the modulator output depends on the waveform of the loopfilter output (as opposed to pipeline ADCs, which depend on settled values), opamp speed requirements are greatly relaxed. This enables the use of power efficient opamp topologies, which would not be appropriate in a pipelined ADC due to poor settling characteristics. The input impedance of a CTDSM is resistive, greatly simplifying the design of the drive circuitry. Further, with a proper design choice for the feedback DAC, these modulators have implicit anti-aliasing.

Several high performance converters reported recently [4]–[6] use multibit quantizers in the $\Delta\Sigma$ loop. A multibit design has several benefits—a more aggressive noise transfer function (NTF) can be chosen, resulting in a higher inband signal to quantization noise ratio (SQNR) for a given oversampling ratio (OSR). Put another way, a lower OSR can be used to obtain a desired in-band SQNR. If a non-return to zero (NRZ) DAC is used, the sensitivity of the converter to clock jitter is reduced. Further, since the loop filter processes only the shaped quantization noise (whose power is small due to the reduced LSB size), degradation of modulator performance due to loop filter nonlinearity is also reduced. The area occupied by the loop filter can be small, as smaller capacitors can be used while still avoiding integrator saturation.

Multibit operation also has a few drawbacks, especially at high speeds. The design of the quantizer, which is a cascade of a ADC and a DAC becomes increasingly difficult at high clock rates. This has led most designers to restrict the number of quantizer bits to four. The ADC is usually realized as a flash design to keep latency low. While a 4-bit flash ADC design may appear straightforward, one must note that the quantizer needs to provide an output well within one clock cycle [4]–[7]. This makes the design of the flash ADC very challenging, and requires significant power. This also increases the power dissipation of the loop filter, which needs to drive the flash converter.

The feedback DAC also presents its own share of problems. Mismatch in the DAC elements greatly degrades the inband signal to noise and distortion ratio (SNDR) and dynamic element matching (DEM) [7]–[10] is usually used to counter this. At high sampling rates, the delay introduced by the DEM logic can be unacceptable. Alternatively, calibration techniques [11] can be used, but this usually results in complex logic. Yet another approach is to design the DAC with inherently good matching [4], [12], but this results in increased loading and excess delay, and has to be addressed by increasing power dissipation. Due to the factors discussed above, it is often found that the quantizer consumes most of the power in a wideband CTDSM employing a multibit quantizer.

In this work, we investigate the use of a single-bit quantizer in a modulator, with the aim of obtaining 11-bit performance in a 15 MHz bandwidth. Traditionally SAR [13], [14] and pipelined ADCs [15], [16] are the architectures of choice to process such wideband signals with these resolutions. However, in recent years sigma-delta modulators [4], [6], [17] have evolved to the point that conversion of wideband signal with desired

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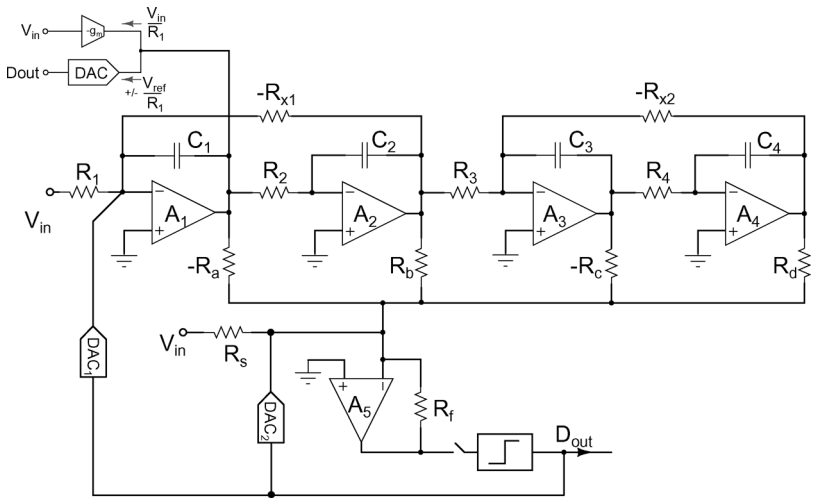

Fig. 1. Modulator architecture.

resolutions has become practically feasible. Compared to other ADC architectures (such as SAR and pipeline), continuous time sigma-delta modulators have an advantage that they relax requirements on anti-alias filters resulting in simplified system design, apart from the other favorable aspects mentioned earlier in this section. Furthermore, a single bit sigma-delta modulator design has several advantages. Due to the inherently linear feedback DAC, DEM is not necessary. This reduces excess loop delay, enabling a higher sampling rate (which is necessary anyway to obtain the desired SQNR). Thanks to the single-bit quantizer, only the sign of the loopfilter output is relevant—this enables the use of high speed, power efficient, feedforward compensated two stage opamps with a somewhat restricted output swing. Die area, and consequently, layout parasitics are small. However, single-bit feedback greatly increases the magnitude of the signal processed by the first integrator of the loop filter. The increased linearity requirement of the first opamp (assuming active-RC integrators) leads to higher power dissipation. In this work, we use the "assisted opamp technique" [18] to obtain the required linearity with a low power consumption. The efficacy of this technique has hitherto been demonstrated at low frequencies—here, we analyze nonidealities especially important in a wideband ADC. At high speeds, timing mismatch effects in the assisted integrator can be a potential problem. We give an analysis and simulation results to show that the performance of such an integrator is maintained with practical clock skews that can be expected on-chip. Experimental results from a 1 GS/s single-bit modulator show the improvements to be had at high sampling rates.

The rest of the paper, which is an extension of [19], is organized as follows. Section II describes the modulator architecture. In Section III, we analyze the effect of timing skew in assisted opamp integrators. Circuit design details are given in Section IV. Experimental results from a single-bit modulator testchip sampling at 1 GS/s are given in Section V. The prototype, fabricated in a 0.13 μm CMOS technology, achieves a dynamic range of 67 dB in a 15.625 MHz bandwidth, while consuming only 4 mW. Section VI concludes the paper.

II. Architecture Details

The architecture of the $\Delta\Sigma$ modulator is shown in Fig. 1. A single-ended diagram is given for simplicity, and negative values of the resistors indicate inversion of the signals in the fully differential version. The fourth order NTF is chosen to have maximally flat behavior with an out of band gain (OBG) of 1.5, as per Lee's rule [20]. The sampling rate is chosen to be 1 GHz, implying an OSR of 32. For enhanced noise shaping, complex zeroes are placed in the signal band—this results in a peak in-band SQNR of 77 dB, which is about 10 dB above the desired SNR of the converter. Interestingly, by using a 4-bit quantizer instead of a single-bit one, the same peak SQNR could have been achieved, but with a sampling rate of only 400 MHz (assuming the OBG of the NTF is increased to 2.5). However, this approach, which would need 15 comparators to realize the flash ADC and DEM logic, can be expected to dissipate more power than a single bit quantizer working at 1 GHz. As an example, the comparator in our design (along with associated clock drive circuitry) consumes about 450 μW when clocked at 1 GHz. 15 such comparators operating at 400 MHz are estimated to dissipate about 2.7 mW, not accounting for power in the DEM and other extra circuitry, rendering the quantizer power hungry.

The loop filter is implemented as a Cascade of Integrators with Feed Forward (CIFF) structure. A direct path is added from the modulator input to the loop filter output. Thanks to this, the loop filter processes only the quantization noise, and results in small values for the integrating capacitors. This, however, results in peaking in the signal transfer function (STF) and has to be addressed by appropriate prefiltering of the input. For low noise and high linearity, all integrators use active-RC designs. The first integrator, which uses a 10 kΩ input resistor, is implemented using the assisted-opamp technique (see the DAC and transconductor injecting current into the output of the first opamp). 40 kΩ resistors are used in subsequent integrators. Weighted addition of the integrator output is performed using a separate summing amplifier (A5). Capacitive feed-ins into the last integrator could have been used to accomplish summation (so that one opamp could be eliminated). Rather, a dedicated

summing amplifier is used to add the integrator outputs. In the capacitive summation approach, the fourth integrator would be in the high speed path of the modulator loop, and the feed-in capacitors needed to implement summation would result in increased delay when compared to the delay of a stand alone integrator. Hence, even though capacitive summation saves an opamp, simulations show that using a separate summing amplifier is a more power efficient solution. Finally, thanks to the single-bit quantizer, the output of the summing amplifier can be scaled without effecting the NTF. This simplifies the design of the summing opamp (A5), since its output does not have to accommodate a full-scale swing. Moreover, the parasitic pole caused by the feedback resistor and input capacitance of A5 occurs at a higher frequency (due to the smaller feedback resistor) thereby reducing delay.

There are several conceivable ways of implementing the feedback DAC. One choice is to use a switched-capacitor DAC, which makes the modulator performance robust to clock jitter. However, it can be shown [21] that the magnitude of the STF at the sampling frequency is approximately

$$|STF(j2\pi f_s)| = \frac{1}{1 + G_{m1}R} \tag{1}$$

where R is the input resistance of the modulator and G_{m1} is the transconductance of the opamp used in the first integrator. For instance, a $G_{m1}R$ of 10 (which is good enough to achieve noise shaping) results in an alias rejection of only 20 dB! Using a switched-capacitor DAC also results in increased in-band thermal noise due to aliasing effects. Further, the linearity needed of the first opamp is also increased due to the spikes of current resulting from the discharge of the feedback DAC capacitor. A return-to-zero (RZ) DAC is extremely sensitive to clock jitter. Based on the considerations above, a NRZ DAC (DAC_1) was chosen as the feedback DAC. An NRZ pulse shape can be implemented with a switched-resistor, but this reduces the loop gain around the first opamp, which in turn increases excess delay. The distributed parasitic capacitance of the resistor is also an issue. This led us to use a current steering DAC, though it is inherently more noisy than a resistive structure. Apart from enabling high speed operation, a current steering design also reduces the in-band noise contribution of the first opamp. The distortion contributed by the DAC is directly referred to the modulator input and has to be addressed by circuit techniques and careful layout, as discussed in Section IV. DAC_2 compensates for excess loop delay, which is about 55% of the clock period. The full scale voltage of the modulator is 2.4 V (peak-to-peak, differential).

All opamps are two stage designs that use NMOS input pairs (for high speed) and feedforward compensation, and are discussed in Section IV. The input referred noise of the loop filter is dominated by the thermal noise from the DAC and the first opamp. Due to opamp assistance, the first integrator is almost ideal. The finite bandwidth of the rest of the opamps, and excess delay (most of which is due to the latch) degrade the stability of the modulator. The NTF is restored to the desired response by the robust coefficient tuning technique of [22]. To counter RC time constant variations, the integrating resistors and capacitors are implemented as digitally tuned banks.

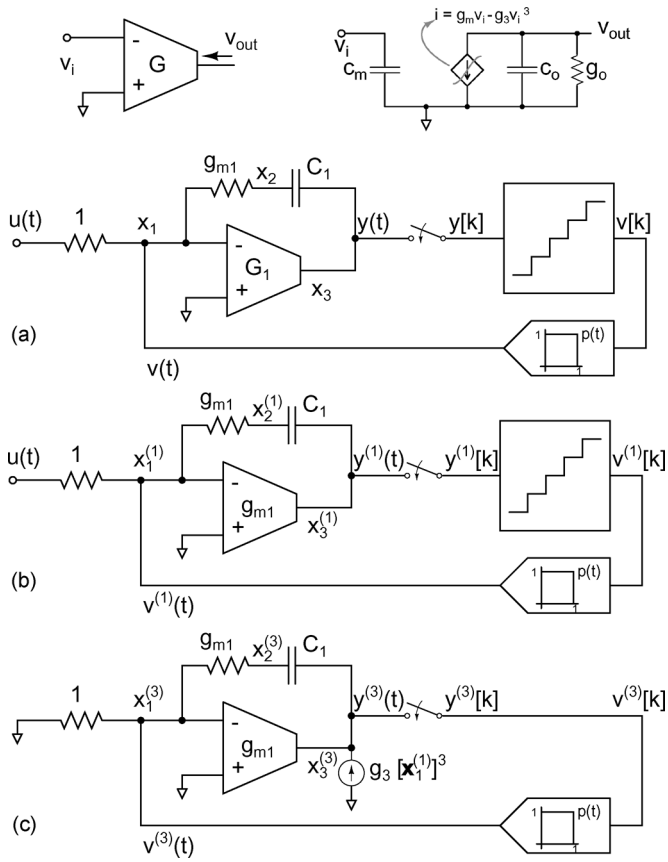

Fig. 2. Model to understand effects of weak loop filter nonlinearity in CTDSMs.

III. The Assisted Opamp Integrator and Timing Skew

To appreciate the motivation behind the assisted opamp integrator, and better understand the effects of timing mismatch, it is instructive to examine the mechanism behind distortion generation (due to weak nonlinearities in the loop filter) in CTDSMs. Fig. 2(a) shows a first order CTDSM with a nonlinear integrator. $p(t)$ denotes the pulse shape of the feedback DAC. The OTA in the integrator is assumed to be weakly nonlinear with an output current given by $i = g_m v_i - g_3 v_i^3$. The effect of OTA nonlinearity can be interpreted in the following manner. First, the output sequence $v^{(1)}[k]$ of a modulator with a linear loop filter, excited by the input $u(t)$ is determined (Fig. 2(b)). The OTA input voltage, assuming a linear loop filter, is denoted by $x_1^{(1)}(t)$. To determine the effect of nonlinearity on the modulator, the nonlinear current caused by the OTA, $g_3[x_1^{(1)}(t)]^3$, is injected into a *linear* modulator with the input nulled, and quantizer bypassed, as shown in Fig. 2(c). The output sequence of this linear system is denoted by $v^{(3)}[k]$. The true inband power spectral density (PSD) due to nonlinearity can be approximated by the PSD of $v^{(1)}[k] + v^{(3)}[k]$. This is an extension of the method of current injection [23] to CTDSMs [24]. The key points to observe are the following.

- Nonlinearity can be thought of as manifesting from the nonlinear currents injected into a linear system (see Fig. 2(c)). Thus, inband distortion can be reduced by reducing internal swings $x_1^{(1)}(t)$, or g_3, or both.

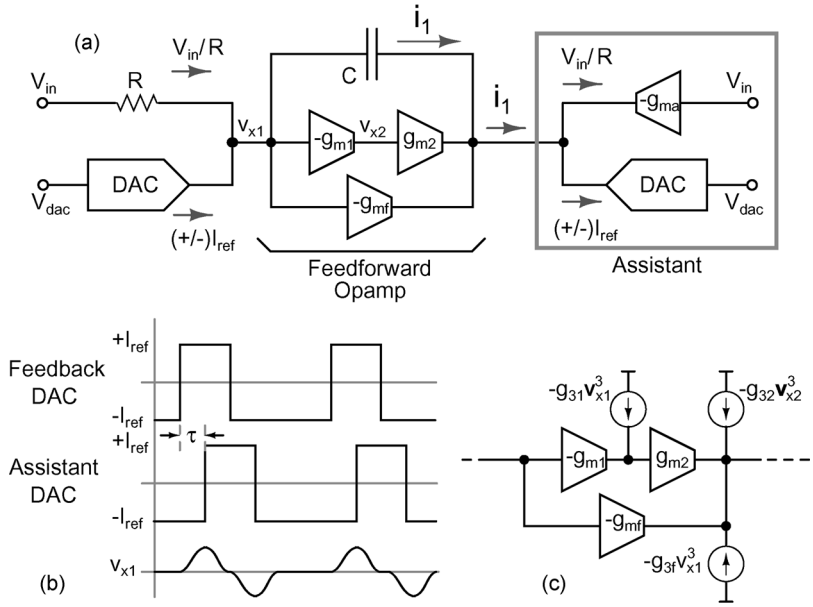

Fig. 3. (a) The assisted opamp integrator. (b) Waveforms in the presence of a timing skew (τ) between the feedback and assistant DACs. (c) Current-injection model to understand the effect of opamp nonlinearity on model performance.

- The PSD of the inband "noise" due to OTA nonlinearity is related to the PSD of $g_3[x_1^{(1)}(t)]^3$.

With this intuition in mind, we proceed to explain the basic idea behind the assisted opamp technique applied to an active-RC integrator, as in Fig. 3(a). The opamp is of the feedforward kind, with its phase margin dependent on g_{mf}. The current flowing through the integrating capacitor is $V_{in}/R \pm I_{ref}$. In a conventional integrator, this current would have to be sourced by the opamp, thereby causing large voltage excursions at its internal nodes ($v_{x1}(t)$ and $v_{x2}(t)$). These large swings cause nonlinear currents to be injected into the modulator, thereby increasing the in-band noise and distortion. Swings at the internal nodes of the opamp can be avoided by using "assistant" currents, enclosed in the grey box in Fig. 3(a). This way, the current through the integrating capacitor is absorbed by the assistant, and $v_{x1}(t)$ and $v_{x2}(t)$ are zero, resulting in improved integrator linearity. Further, since $v_{x1}(t) = 0$, the integrator is virtually ideal, with negligible excess delay. This feature is particularly useful in high speed designs such as the one described in this paper. Fig. 4 shows the NTF of the modulator with and without using opamp assistance for the first integrator. (Circuit details are given in the next section). Thanks to opamp assistance, integrator excess delay is reduced, resulting in a "less peaky" NTF. For a fair comparison, power dissipation is kept same in both cases. This is done by increasing the opamp output stage current in the case without assistance by an amount equal to that consumed by the assistant circuitry.

One potential issue with the assisted opamp integrator is timing skew between the feedback and assistant DAC currents, indicated as τ in Fig. 3(b). For the duration τ, the opamp has to supply the required current—causing $v_{x1}(t)$ and $v_{x2}(t)$ to be nonzero. Based on the intuition developed in Fig. 2, these swings cause nonlinearity, whose effect can be understood as nonlinear currents injected into a linear modulator (with input

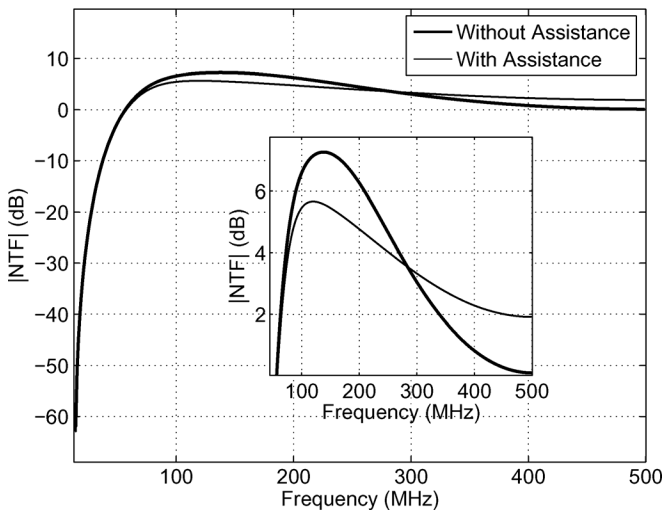

Fig. 4. Noise transfer functions with and without assistance in the first integrator. Power dissipation is same in both cases.

nulled and quantizer bypassed). These currents are proportional to $v_{x1}^3(t)$ and $v_{x2}^3(t)$, as shown in Fig. 3(c). However with weakly nonlinear opamps, these distortion components have very little power at low frequencies due to the following. Notice from Fig. 3(b), that whenever $v_{x1}(t)$ goes up for a duration τ at the rising edge of the DAC current waveform, it undergoes a largely similar excursion at the falling edge but in the opposite direction. This means that the cubes of these pulses that occur around the rising and falling edges are similar, but occur in opposite directions, indicating that their inband components are small. Clearly, for small τ, the amplitude of $v_{x1}(t)$ is proportional to τ, leading us to conclude that the (small) inband nonlinear components due to timing skew should be proportional to τ^3. One must also bear in mind that the analysis assumes weakly nonlinear operation of the opamp—this will not be true for large τ.

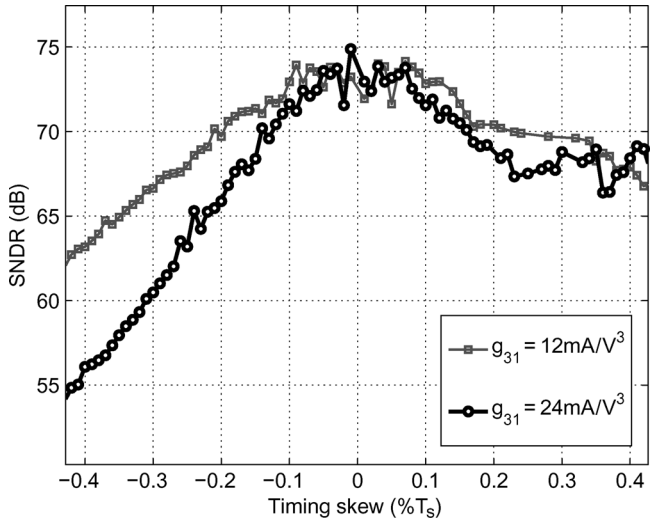

Fig. 5. Simulated inband SNDR as a function of timing skew between the feedback and assistant DACs using a macro-model of the first opamp for two levels of opamp nonlinearity.

To verify the above, macromodel simulations of the fourth order CTDSM, incorporating timing skew between the DAC and assistant were run. Every transconductor in the first opamp was modelled by a saturating nonlinearity which is an odd function of the differential input, as follows:

$$\begin{aligned} i &= -I_{max}, \quad v_i < -\sqrt{\frac{g_m}{3g_3}} \\ &= g_m v_i - g_3 v_i^3, \quad |v_i| \le \sqrt{\frac{g_m}{3g_3}} \\ &= I_{max}, \quad v_i > \sqrt{\frac{g_m}{3g_3}} \end{aligned} \tag{2}$$

where $I_{max} = (2g_m/3)\sqrt{g_m/3g_3}$. The coefficients in (2) were obtained by fitting the DC $i - v$ characteristic of the individual transconductors. Fig. 5 shows the inband SNDR as a function of timing skew for two levels of nonlinearity (different values of g_{31}). We see that the SNDR is dominated by quantization noise for skews between $-0.1T_s$ and $0.1T_s$. Beyond that, timing mismatch degrades the modulator performance. As expected, higher amounts of nonlinearity result in lower SNDR for a given timing error.

Interestingly, the SNDR-versus-skew curve is asymmetric about $\tau = 0$, and becomes more so with increased nonlinearity. It turns out that the primary reason for this phenomenon is the overlap capacitance in the second stage of the feedforward amplifier. To gain intuition, consider the waveforms in an assisted opamp integrator with a zero input, as shown in Fig. 6. For simplicity, the input resistor and the assistant transconductor that compensates for the input current are removed. C_m models the overlap capacitance of the second stage of the opamp. The feedback and assistant DAC currents are denoted by I_{DAC} and I_{asst} respectively. Without timing skew, it is easy to see that the current I_m through C_m is $I_{DAC}(C_m/C)$, which in turn, causes v_x to be $-v_{max} = -(I_{DAC}/g_{m1})(C_m/C)$. Thus, due to the parasitic C_m, the virtual ground node of the first opamp has a peak to peak swing of $2v_{max}$, and is shown in blue in Fig. 6(a), (b). In the discussion to follow, positive timing skew is defined as the feedback DAC pulse leading the assistant DAC pulse, and vice versa. Fig. 6(a) shows selected waveforms when the skew is $-0.15T_s$. For $t < t_1$, I_{DAC} is negative. This causes $v_{x1}(t) \approx -v_{max}$. At $t = t_1$, I_{asst} changes state early. This causes a net current of $2I_{DAC}$ to be drawn from the output node, leading to a negative going glitch in v_{x1}. For $t > t_2$, the virtual ground node will attempt to settle to $+v_{max}$. Since v_{x1} begins from a large negative value (just before $t = t_2$) and has to settle to $+v_{max}$, another large glitch is seen beginning at $t = t_2$. The glitches occur in the opposite direction when I_{asst} falls.

For a positive timing skew, the situation is quite different, as shown in Fig. 6(b). For $t < t_2$, $v_{x1} = -v_{max}$. For $t_3 > t > t_2$, a nett current of $2I_{DAC}$ is injected into the output node, since the assistant DAC has not changed state. This causes v_{x1} to increase (due to negative feedback action) causing a positive going glitch—however, for $t > t_3$, it attempts to settle to $+v_{max}$. This causes v_{x1} to fall, from a large positive value to $+v_{max}$. Thus, when compared to the case of negative skew (where v_{x1} has to start from a large negative value and settles to $+v_{max}$), the height and width of the glitch on the virtual ground node is much smaller. From the discussion at the beginning of this section, we saw that a larger/wider glitch on the virtual ground node results in higher nonlinear currents being injected and subsequently, a lower SNDR. This intuitively explains the asymmetry of the SNDR curve with τ.

The asymmetry of the SNDR-versus-τ curve is further accentuated by the nonlinearity of the common-mode detector employed at the output of the first stage of the opamp. Fig. 7 shows the inband SNDR of the CTDSM as a function of τ for three cases: (a) a nonlinear macromodel of the opamp, (b) a transistor level opamp implementation with ideal CMFB (linear common-mode detector) at the output of the first stage, and (c) a transistor level opamp implementation with transistor level CMFB. The details of the CMFB circuitry are given in the next section. Notice the increased asymmetry caused by the CMFB circuitry. However, we notice that the CTDSMs SNDR is quite tolerant of clock skews of up to ±10% of the clock period.

Finally, transistor level simulations were run to compare modulator performance with and without opamp assistance. For a fair comparison, the total power dissipation is kept the same in both cases (as mentioned earlier in this section). Fig. 8 shows the simulated PSD; the improvement to be had with opamp assistance is evident.

IV. Circuit Design

A. Operational Amplifiers and Quantizer

Opamps: The first integrator largely determines the noise and linearity of the modulator. The circuit schematic of the opamp used in the first integrator is shown in Fig. 9. It is a two stage design that uses feedforward compensation. Such an architecture is fundamentally more efficient when compared to a Miller compensated design, since power is not wasted in charging and discharging the compensating capacitors. The first stage consists of long channel devices M_1, M_2, M_3 and M_4 to lower the $1/f$ component of the input referred noise. The output common-

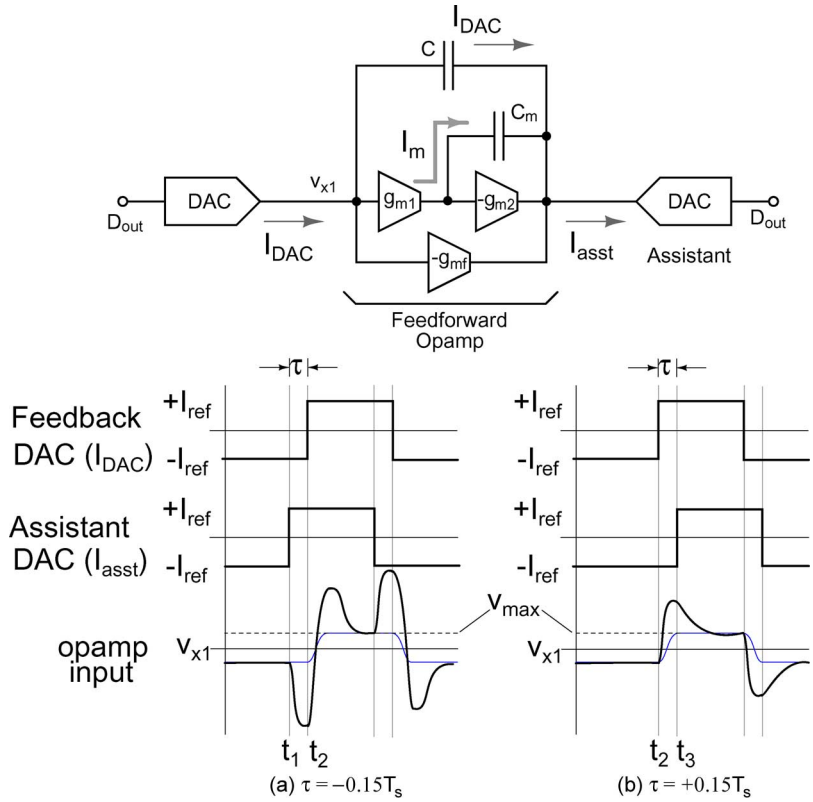

Fig. 6. Timing waveforms for (a) −15% timing skew ($\tau = -0.15\mathrm{T_s}$) and (b) +15% timing skew ($\tau = +0.15\mathrm{T_s}$).

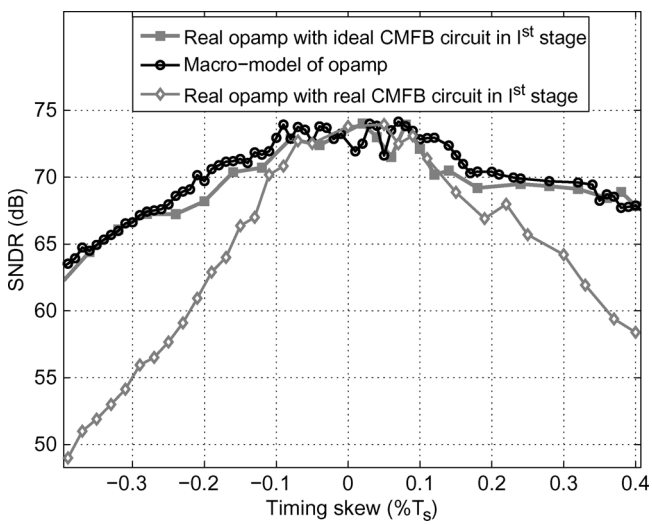

Fig. 7. Simulated inband SNDR as a function of timing skew between the feedback and assistant DACs for several cases. The nonlinear CMFB circuitry at the first stage output accentuates the asymmetry of the SNDR versus τ curve.

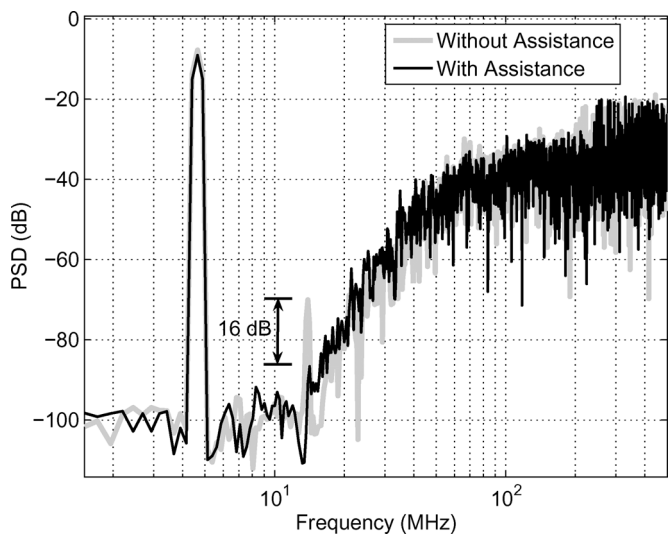

Fig. 8. Simulated performance with and without assistance. The power dissipation is the same in both cases.

mode of the first stage is established and stabilized using $\mathrm{M_5}$ and $\mathrm{M_6}$. These are minimum length devices, carrying a third of the first stage tail current. Since $\mathrm{M_{9,10}}$ and $\mathrm{M_{5,6}}$ have the same $\mathrm{V_{DS}}$, the quiescent current in the second stage is accurately set to 60 μA by choosing $\mathrm{M_9}$ to be six times wider than $\mathrm{M_5}$. As transistors detect the common-mode voltage at the output of the first stage, the DC gain is not degraded by the common-mode feedback mechanism. Further, the current density of $\mathrm{M_{3,4}}$ can be set in a manner independent of that of the output stage—this way, the input stage can be sized based on $1/f$ noise considerations, while $\mathrm{M_{5,6}}$ and $\mathrm{M_{8,9}}$ are optimized for speed. Note that the second stage current is reused to implement the compensating feedforward path. The total current drawn by the opamp is 190 μA. The opamps used in the subsequent integrators and the summing amplifier are similar to the first opamp, except that they are appropriately scaled to reduce power dissipation.

Latch and DAC: The CMOS latch shown in Fig. 10(a) is similar to the one used in [18], except that it has a reset phase.

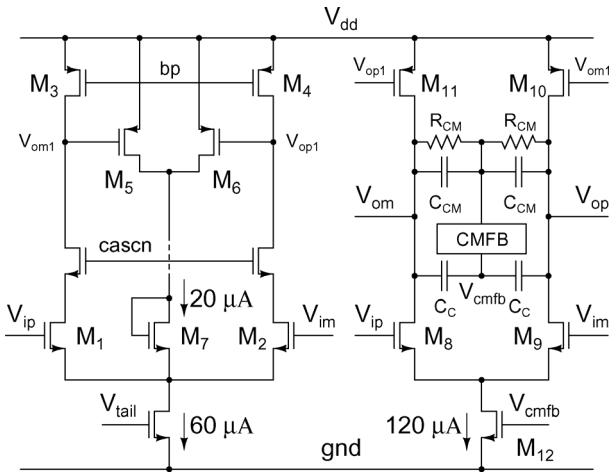

Fig. 9. Operational amplifier used in the first integrator.

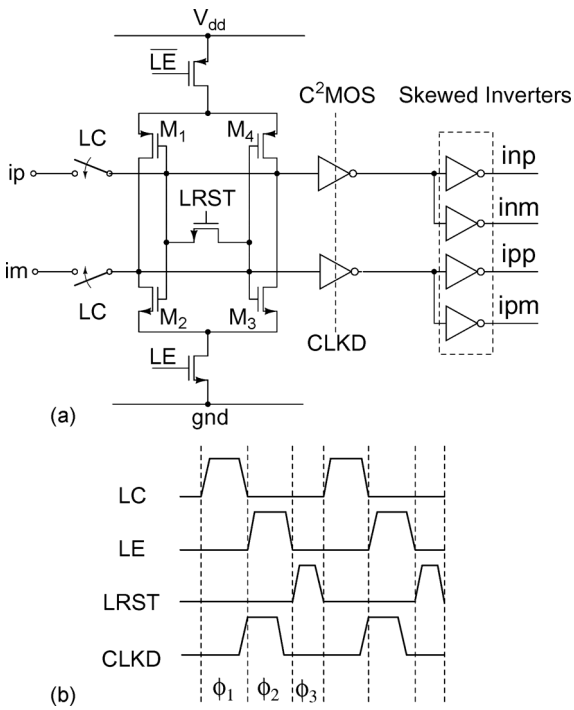

Fig. 10. (a) Comparator schematic and (b) clock waveforms.

The timing waveforms are shown in Fig. 10(b). During the reset phase (ϕ_3), the outputs of the latch are shorted. This causes the differential input of the latch to become zero at the beginning of ϕ_1, thereby reducing latch hysteresis. The latch output is sampled using $\mathrm{C^2MOS}$ buffers clocked by a delayed version of the clock (CLKD). This reduces the effect of data dependent jitter. The $\mathrm{C^2MOS}$ buffer drives the complementary NMOS/PMOS NRZ DACs used in the feedback and assistant paths. Using a rail-to-rail swing to drive the differential switches of the current steering feedback DACs causes distortion. Therefore, reduced swing inverters are used to generate the drive signals for the DACs.

Fig. 11 shows the schematic diagram of the feedback and assistant DACs. The feedback DAC carries 60 μA. Noise from the DAC bias circuitry RC-filtered so that it does not contribute

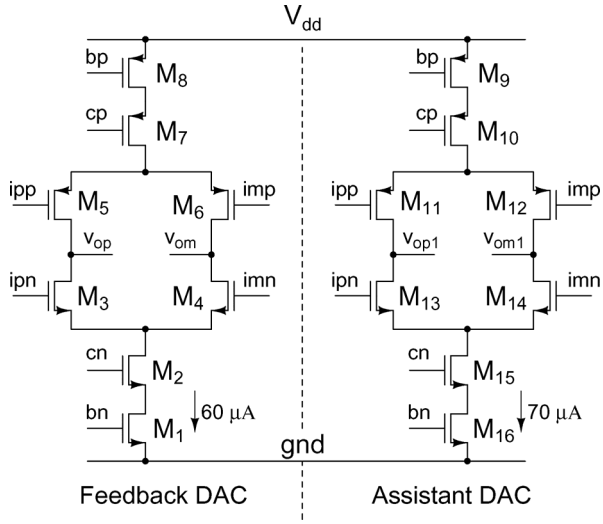

Fig. 11. Schematic of the feedback and assistant DACs.

significant noise. The input referred voltage noise spectral density contributed by the DAC is seen to be

$$S_n(f) = \frac{8kT(g_{mn} + g_{mp})R^2}{3} \tag{3}$$

where g_{mn} and g_{mp} denote the transconductances of the current sources $\mathrm{M_1}$ and $\mathrm{M_8}$. It is important to bias the current sources such that they have a large overdrive. However, a large overdrive reduces the headroom for the cascode device, which would necessitate a large transistor (with a higher parasitic capacitance), increasing distortion. Thus there is a tradeoff between noise and distortion caused by the DAC.

B. Assistant Circuitry

Assistant Transconductor: Fig. 12 shows the schematic of the assistant transconductor used to inject a current $\mathrm{V_{in}/R}$ into the opamp output. This circuit is similar to the assistant transconductor circuit presented in [18], but biased so as to have sufficiently large bandwidth. It is a class-AB design, comprising of complementary common gate stages $\mathrm{M_2}$ and $\mathrm{M_7}$, which carry 20 μA under no signal conditions. $\mathrm{R_1}$ is chosen to be 8 $\mathrm{k\Omega}$. $\mathrm{M_4}$ and $\mathrm{M_9}$ are of the same size as $\mathrm{M_3}$ and $\mathrm{M_8}$ respectively. Distortion components generated by this transconductor are attenuated by the gain of the first integrator, and are of little consequence, as shown in [18].

Assistant DAC: The assistant DAC, shown in Fig. 11, is a replica of the feedback DAC. It is implemented as cascoded 70 μA NMOS and PMOS current sources, steered using differential pairs. The additional current helps in compensating for the current flowing through the parasitic capacitances at the output of the first integrator.

V. Measurement Results

The fourth order continuous-time ΔΣ ADC was fabricated in a 0.13 μm CMOS process through Europractice. Fig. 13 shows the test board and the layout of the active area, which measures about 0.26 $\mathrm{mm^2}$. Including bypass capacitors, the area is about 0.38 $\mathrm{mm^2}$. The modulator output was demultiplexed

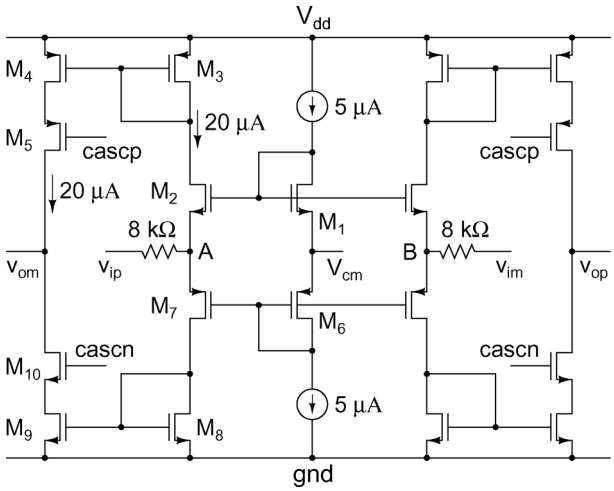

Fig. 12. Assistant transconductor.

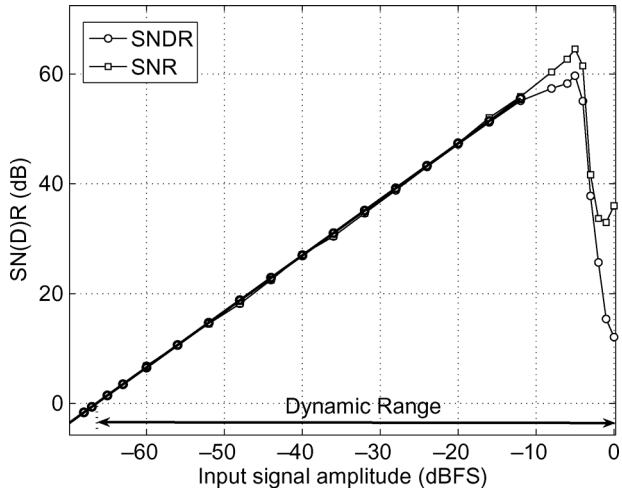

Fig. 14. Measured SNR and SNDR as a function of input amplitude.

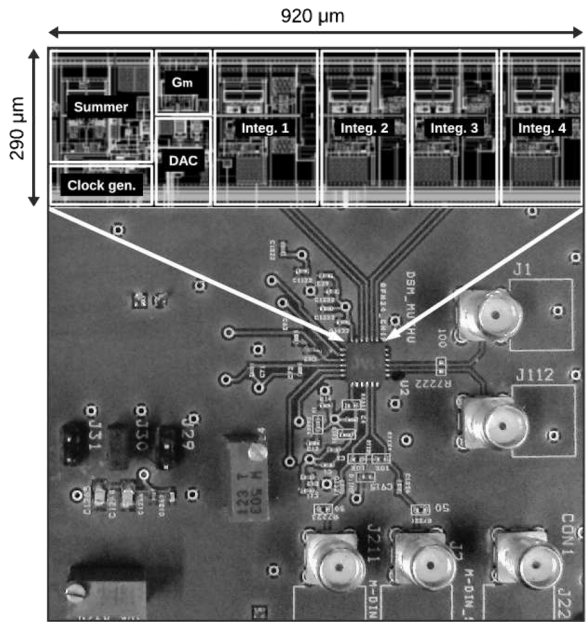

Fig. 13. Chip layout and photograph of the test board.

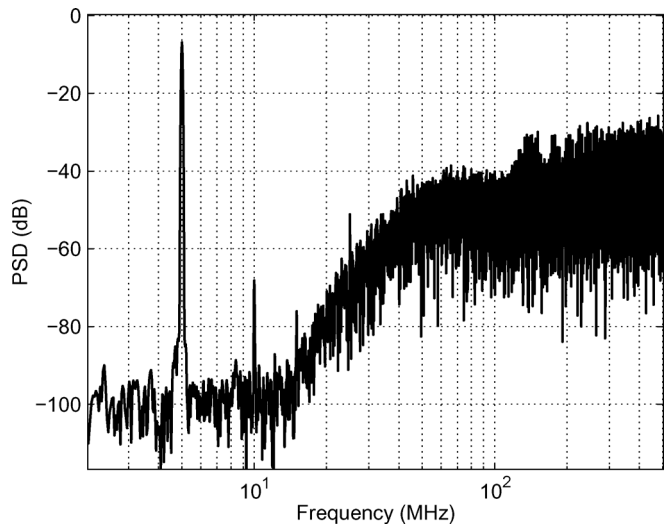

Fig. 15. PSD of the modulator output sequence for a −5 dBFS input sinusoid.

on-chip into two 500 Mbps streams, and brought out using two LVDS buffers. These waveforms were captured on a real-time high speed scope (Agilent DSO80204B), and subsequently processed on a computer. A 32 K Blackman-Harris window was used for spectral estimation. Fig. 14 shows the measured SNR and SNDR of the modulator. The SNR was determined using a 10 MHz sine wave input, while a 5 MHz tone was used for SNDR measurement. The peak SNR and SNDR are 64.5 dB and 59.8 dB respectively. The measured dynamic range of the modulator is 67 dB. Fig. 15 shows the spectrum of the output sequence when the converter is excited by a -5 dBFS tone at 5 MHz. The SNDR is limited by the second harmonic, and is believed to be from coupling of the high speed stream back to the modulator reference pin/clock through the package. In retrospect, it would have been better to avoid bringing data out at half speed, as the half rate clock opens up avenues for coupling of noise from $f_s/2$ into the signal band. The PSD also shows a third harmonic 69.8 dB below the fundamental—this has a negligible effect on the SNDR.

A. Intermodulation and Jitter Measurements

Two tone tests were made to determine the third order intermodulation distortion (IM_3). Fig. 16 shows the spectrum of the output sequence when two narrowly spaced sinusoids with frequencies 14.5 MHz and 15 MHz were used. The amplitude of each of the tones was -10.6 dBFS. The intermodulation products are -70.1 dB and -69.5 dB, sufficiently below the in-band noise specification of the modulator. Fig. 17 shows the variation in IM_3 with the average frequency f_{av} of the two tones, as f_{av} is swept through the signal band. We see that the intermodulation components are well below the noise level for f_{av} less than 8 MHz, and that the maximum value of IM_3 occurs when f_{av} is at the band edge.

To determine the performance of the CTDSM with jitter, the clock was FM modulated with a frequency of 96 MHz, using a Centellax-TG1B1 signal generator. The peak frequency deviation controls the magnitude of the injected jitter. Due to the

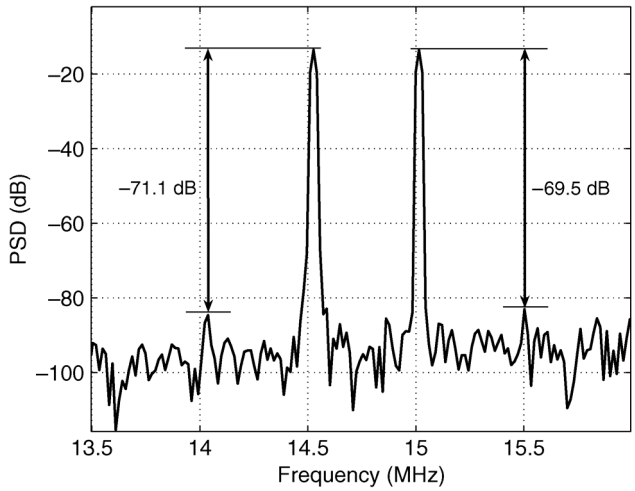

Fig. 16. Intermodulation components for a two tone test—each input tone has an amplitude of −10.6 dBFS.

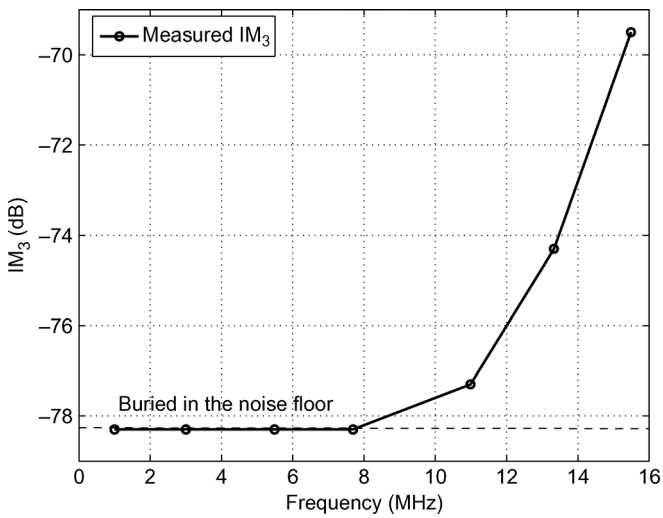

Fig. 17. Variation of $\mathrm{IM_3}$ with the average of the two tones.

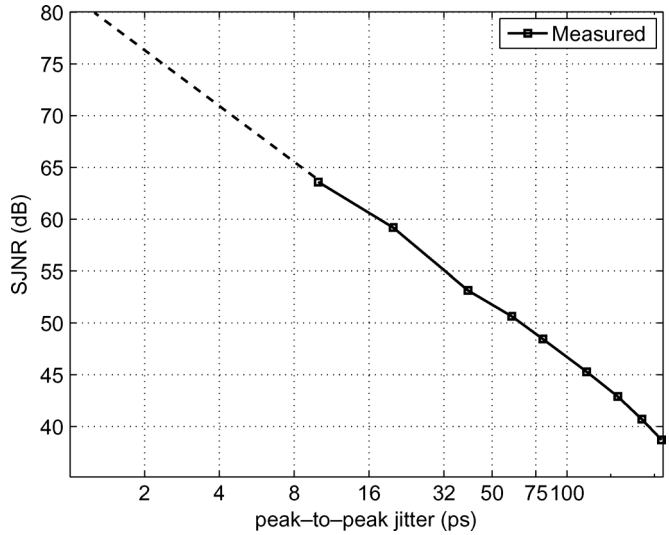

Fig. 18. Variation of signal to jitter noise ratio (SJNR) with peak-to-peak jitter.

TABLE I
SUMMARY OF MEASURED ADC PERFORMANCE

Signal Bandwidth/Clock Rate	15.6 MHz / 1 GHz
Full Scale	2.4 $V_{pp,diff}$
Input Swing for peak SNR	−4.6 dBFS
Dynamic Range/ SNR / SNDR	67.0 dB / 64.5 dB / 59.8 dB
Active area	0.38 mm^2
Process / Supply Voltage	0.13 μm CMOS / 1.3 V
Power dissipation (Modulator+References)	4 mW
Figure of Merit (SNR)	93 fJ/level
Figure of Merit (SNDR)	160 fJ/level
Figure of Merit (Schreier)	162.9

wideband modulation of the clock, noise from out-of-band frequencies folds into the signal band, degrading the in-band SNR. Fig. 18 shows the measured signal to jitter noise ratio (SJNR) as a function of peak-to-peak clock jitter. On extrapolating the results, we see that 4 ps peak-to-peak jitter results in about 70 dB SJNR, which is well above the thermal noise limited SNR.

A summary of the measured performance is given in Table I. The figure of merit (FOM) of the converter is determined using SNR and SNDR separately as given by (4) and (5), respectively.

$$\mathrm{FOM_{SNR}} = \frac{\mathrm{P}}{2\mathrm{f_B}2^{\frac{(\mathrm{SNR}-1.76)}{6.02}}}, \tag{4}$$

$$\mathrm{FOM_{SNDR}} = \frac{\mathrm{P}}{2\mathrm{f_B}2^{\frac{(\mathrm{SNDR}-1.76)}{6.02}}} \tag{5}$$

where P, $\mathrm{f_B}$, and SNR denote the power dissipation, signal bandwidth, and signal to noise ratio, respectively. Since the noise performance of the modulator is dominated by the thermal noise, it is also relevant to compute the FOM proposed by Schreier [25] given by

$$\mathrm{FOM_{DR}} = \mathrm{Dynamic\ Range_{dB}} + 10\log_{10}\left(\frac{\mathrm{BW}}{\mathrm{P}}\right). \tag{6}$$

Our modulator achieves $\mathrm{FOM_{SNR}}$ of 93 fJ/level and $\mathrm{FOM_{SNDR}}$ of 160 fJ/level and $\mathrm{FOM_{DR}}$ 162.9 dB.

Table II compares the performance of this design with that of several high speed ΔΣ modulators presented in the literature (alongwith some state of art SAR and pipelined ADCs). Thanks to opamp assistance, this work achieves 160 fJ/level and outperforms several converters targeting similar bandwidths and resolutions, but realized in more advanced processes.

VI. CONCLUSIONS

The assisted opamp technique, originally proposed to improve the linearity of low speed high resolution CTDSMs, was successfully applied to the design of a high speed single-bit modulator. At high clock rates, timing mismatch between the

TABLE II
COMPARISON WITH OTHER STATE-OF-THE-ART ADCS

Ref.	BW (MHz)	OSR	Type	SNDR/SNR/DR (dB)	Power (mW)	Tech. (nm)	V_{DD} (V)	FOM_{SNR} (fJ/level)	FOM_{SNDR} (fJ/level)	FOM_{DR} (dB)
[4]	20	16	CTDSM	74.0/76.0/80.0	20.0	130	1.2	97	122	170.0
[5]	15	20	CTDSM	64.2/67.2/70.0	20.7	180	1.8	368	521	158.6
[6]	10	32	CTDSM	82.0/-/87.0	100.0	180	1.8	273	486	167.0
[17]	20	8.5	CTDSM	69.0/71.0/77.0	56.0	90	1.2	482	608	162.5
[26]	10	47.5	CTDSM	72.0/86.0/90.0	40.0	130	1.2	122	615	174.0
[27]	20	22.5	CTDSM	78.0/81.2/-	87.0	130	1.5	231	331	164.8
[28]	20	23.75	CTDSM	60.0/62.0/68.0	10.5	65	1.3	255	321	160.8
[29]	10	32	CTDSM	65.0/-/67.0	6.8	90	1.3	185	234	158.7
[30]	20	10.5	DTDSM	70.0/72.0/-	28.0	90	1.2	215	271	160.5
[31]	10	15	CTDSM	62.5/68.2/70.2	5.32	110	1.1	126	244	162.9
[11]	25	10	CTDSM	63.5/64.0/70.0	8.5	90	1.2	131	139	164.6
[12]	125	16	CTDSM	65/65.5/70.0	260	45	1.1	676	716	156.8
[13]	20	1	SAR	55.1/55.8/63	1.21	65	1.1	60	65	165.1
[14]	20	1	SAR	53.3/-/-	0.82	90	1.0	55	-	-
[16]	25	1	Pipeline	58.2/66.0/66.0	9.9	180	1.2	121	298	160.0
[15]	25	1	Pipeline	62.0/62.0/72.0	4.5	90	1.2	87	87	169.0
This work	15.6	32	CTDSM	59.8/64.5/67.0	4	130	1.3	93	160	162.9

feedback and assistant DACs can be a potential problem. Intuition and analysis for the effect of timing skew was given, and it was shown that the performance of this ADC is quite tolerant of timing errors. A 11-bit single-bit modulator with a 15.625 MHz signal bandwidth (and a sampling rate of 1 Gsps) designed using this technique consumes only 4 mW and achieves a FOM of 160 fJ/lvl.

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