IEEE 2009 Custom Intergrated Circuits Conference (CICC)

A 1-GS/s 6-bit 6.7-mW ADC in 65-nm CMOS

Jing Yang, Thura Lin Naing, Bob Brodersen
Berkeley Wireless Research Center,
Department of Electrical Engineering and Computer Sciences,
UC Berkeley
2108 Allston Way, Suite 200, Berkeley, CA, USA
E-mail: yangjing, thura, bwb@bwrc.eecs.berkeley.edu

Abstract

An asynchronous 6bit 1GS/s ADC is achieved by time interleaving two ADCs based on binary successive approximation algorithm (SA) using a capacitive ladder. The semi-close loop asynchronous technique eliminates the high internal clocks and significantly speeds up the SA algorithm. One bit redundancy is implemented to compensate the process variation of parasitic and the MOM capacitance. Fabricated in 65nm CMOS with an active area of 0.11mm^2, it achieves a peak SNDR of 31.5dB at 1 GS/s sampling rate and has a power consumption of 6.7mW for the analog and digital processing.

Index Terms: Analog-to-digital conversion, asynchronous logic circuits, semi-close loop, binary successive approximation algorithm, time-interleaving, cognitive radios.

Introduction

In many high speed wireless communication systems, such as UWB, OFDM-based 60GHz receivers, and WPAN, medium-resolution, high-speed analog-to-digital converters (ADCs) is required to convert RF/IF signals to digital form for subsequent baseband processing [1][2].

Recent research [3][4] explores the application of high-speed (~GHz) medium-resolution (~6-bit) low-power ADCs to resolve high dynamic range problems in cognitive radios (CR) and software defined radios (SDR). Architectures composed of multiple ADCs as pipeline stages, coupled with the flexibility of digital processing facilitate the front-end circuitry design to provide extremely high dynamic range (~70dB), wider signal bandwidth, increased design flexibility and more cost effective system integration.

The low power constraint with such high speed ADC designs is especially challenging with the scaled supply voltage and increased transistor threshold voltage in a low leakage low-power (LP) CMOS processes. As a result, transistors are biased in sub-threshold region and the overdrive voltages are limited by the decaying headroom as the voltage supply scales down.

A conventional flash ADC could be the preferred choice, considering its low latency and high-conversion speed, one conversion is completed in a single clock cycle. However, flash ADCs suffer from an exponential dependence of power and area on resolution. Furthermore, the component variations of the parallel paths could be significant and thus it becomes expensive to calibrate, especially with increased resolution and process variation as technology scales. In comparison, a successive approximation algorithm only has a logarithmic dependence on resolution -- it spreads one conversion over several cycles, dissipating significantly less power while occupying a smaller area. This characteristic renders the architecture highly scalable and easier to calibrate.

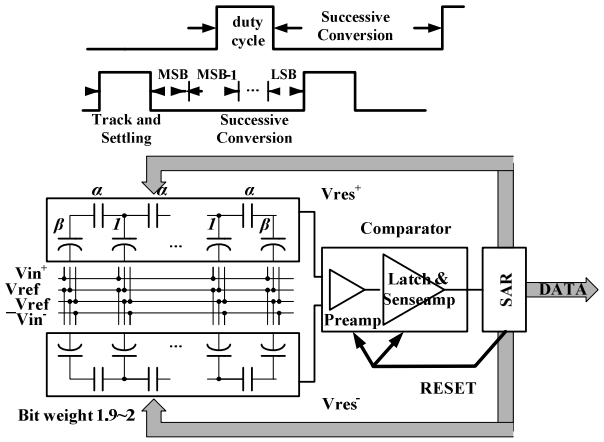

Fig. 1 Time interleaved asynchronous ADC architecture

This work presents strategies and techniques optimizing the power and area efficiency of a high speed ADC. We adopt power efficient semi-close loop successive approximation algorithm executed in an asynchronous manner. Particular attention is paid to increase the conversion speed of the asynchronous feedback loop. We use improved technology over previous implementations [5] and design a fast settling dynamic comparator with timing-optimized dynamic digital-decision logic.

The prototype design of a 6-bit 1GS/s ADC consumes a total power of 6.7mW in 65nm CMOS by interleaving two such asynchronous SA ADCs. Each ADC only occupies an area of 0.35x0.16mm^2.

Architecture

Fig 1. shows the proposed architecture. The external square-wave clocks initiate a tracking and settling phase followed by the successive approximation (SA) comparisons.

The input is sampled by the capacitor array with effectively low input capacitance. An alpha-beta low-input capacitive ladder network enables the high input bandwidth applications, such as cognitive radio receivers. The ladder network requires extra attention in layout because of the vulnerability to parasitic capacitors associated with the interconnects [5].

After tracking and settling phase, the asynchronous SA, instead of executing the conversion on several equally divided time slots, sequences through MSB to LSB, utilizing only one comparator. The single comparator design avoids the offset calibration between multiple comparators. The offset from the comparator therefore becomes a global offset that could be removed through digital processing. The comparator is also

required to reset itself after each comparison. The charge redistribution network formed by the capacitor array operates as a digital to analog converter (DAC) to subtract or add a fraction of the reference voltage. The voltage increment of the DAC output will be controlled by the previous comparison result. For instance, a "1" from the second comparison indicates a proper connection of the DAC switches, to minus a voltage of Vref/4 to the DAC output. The duration for each cycle is set so that the capacitor array is settled reliably for the successive comparisons to slice and latch the data. Contrary to synchronous processing, such an asynchronous approach does not have the suspension time between subsequent bits, therefore, substantially shortening the conversion time. This approach also eliminates the significant overhead of providing an internal clock with frequency higher than the sampling rate, which would easily go up to 10GHz in the previously mentioned applications. The absence of the clock distribution network allows the design to be significantly more power efficient in high speed operations. Dynamic logic is used to further assist the asynchronous process. Transistors are sized optimally using logical effort for dynamic gates.

The time-interleaved architecture with two opposite phase clocks is implemented to double the conversion speed, which is optimized for the maximum achievable rate of a single ADC. The clocks are provided on-chip for this prototype. Interleaving two ADCs using non-overlapping clocks achieves twice the sampling rate at twice the power and area with a slight additional penalty of power and area for the parallel path synchronization and calibration. Post digital processing reduces process variations from manufacturing, extracts the clock skew between two ADCs and compensates it through calibration.

Circuit Implementation

A. Comparator and Semi-close Loop Ready Generator

A pre-amplifier is presented at the input of the comparator as shown in Fig 2. The gain is set to be 6dB based on Monte-Carlo simulation, so that the pre-amplifier could accommodate the 3-sigma offset error due to process variation when the difference at input is 1LSB. Multi-finger poly-resistors provide good matching between outp and outn, and are therefore used for R_D's. The NMOS differential pair is sized to guarantee enough drive strength through the pre-amplifier. M3 and M4 are used to separate the pre-amplifier and the regenerative latch, so the charge from the data logic level injected to the input capacitor array is minimized. The charge difference built up on the R_D's results in an imbalanced charge between the equalizing transistor (M5) source and drain. After each reset phase, as the Eq signal goes

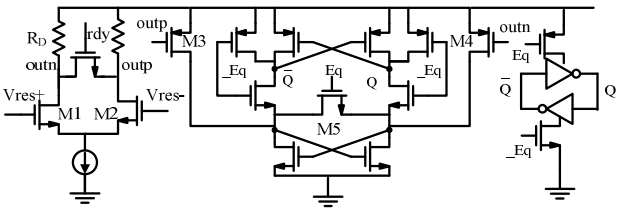

Fig. 2 Dynamic comparator circuit schematic. Pre-amplifier(left), Dynamic latch (middle) and Dynamic sense-amplifier (right).

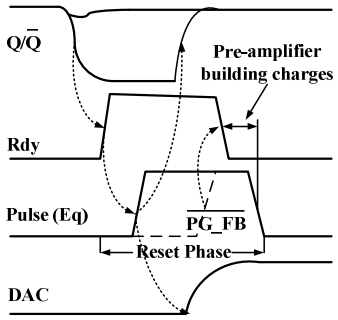

Fig. 3 Dynamic ready acknowledge signal generator, pulse generator schematics and semi-close loop timing diagram with extended reset phase.

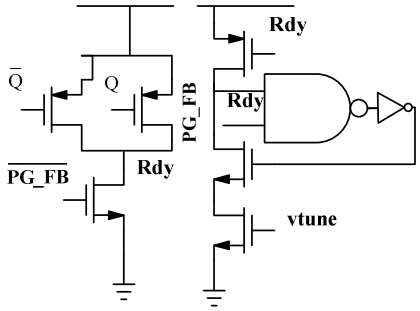

Fig. 4 Dynamic ready acknowledge signal generator and pulse generator schematics.

down, the charge will toggle one of the Q or $\overline{Q}$ to a logical level low. The dynamic sense-amplifier boosts the comparator gain during the dynamic transitions (Fig. 2). It significantly improves the settling time to sense small inputs, which are the bottle-necks of most of the previous comparator designs. The dynamic sense-amplifier switches between standby and wake-up modes, resulting in minimum static power consumption.

Upon the completion of the comparison, there are two critical delay paths involved in setting the DAC. First, in the signal path, the current bit of the comparator is latched into a register. Note the register buffers the bit before it is stored to a bit cache. Second, in the timing path, a dynamic ready acknowledge signal is generated after each comparison phase when the complementary data is available (Fig 3). The ready acknowledge signal triggers a rising edge, followed by a set of switch-controlled clocks. These multiple clocks, together with the registered data coming from the signal path are then used in the decision logic to determine charging or discharging the capacitor array before the next comparison. The asynchronous timing path is usually the longer critical delay path, since it is composed of several logic function delays. Optimizing the timing of the critical delay path, including the delay through the comparator, the timing path and the DAC settling time are crucial in designing the high-speed SA ADC. Moreover, in this design, particular care and effort are taken to merge these three timing pieces together by circuit implementations that explore the possible time overlapping between them within each cycle.

First, observing that both Q and $\overline{Q}$ are fully charged to VDD at the end of each reset phase, thus voltage drop in any or both of them would indicate the start of comparison. The ready acknowledge signal could be generated far ahead of when the

data becomes available. The circuit in Fig. 4 implements this novel idea. Detecting the start of the comparison shortens the overall delay of the critical path, thus facilitating increased speed without a power penalty. Second, both Q and $\overline{Q}$ are pulled down together by the regenerative latch to a level much lower than the supply voltage before one of them is charged back to VDD and the other discharged to GND. Therefore, both PMOS transistors are turned on during the pulling down transition, resulting in a significantly reduced delay from the complementary data to the ready acknowledge signal.

The ready signal triggers a pulse generator to create the reset phase for the comparator, enable the charge redistribution on the capacitor array and guarantee the DAC to settle down within 1LSB by the end of the reset phase. The circuit for generating the pulse is shown at the right of Fig. 4. A tunable gate voltage (Vtune) is used to control the delay from the equalizing clock (Eq) to the feedback node (PG_FB), varying the overall pulse width. In fact, if the settling error for the DAC is less than 1LSB, the decision will not be affected. The Vtune is set so that the converted output for a fixed input voltage doesn't change with Vtune. The tunable voltage could be further set automatically using a multiplying digital to analog converter (MDAC) controlled by a sensing circuit to the DAC's output. The complimentary pulse clock ($\overline{Eq}$) is used to reset the regenerative latch, charging both Q and $\overline{Q}$ to logical level high (Fig. 2). The feedback node (PG_FB) is further used to reset the ready signal shortly before the next comparison. The maximum Vtune is limited to avoid spurious short-circuit current from the supply when both the $\overline{PG\_FB}$ controlled NMOS and one of the PMOS transistors are on.

Because the ready signal controls the reset switches in the pre-amplifier, the recovery phase is extended by allowing extra time for the DAC to finish settling towards the end. During the extended reset phase, the pre-amplifier starts to track and sense the residue (Vres) and build enough charge to reduce the response time of the latch. This scheme not only enables the comparison instantaneously after the evaluation of the previous residue, especially at low Vres levels, but also helps to further reduce the memory effect of previous conversions, which could be substantial at large input signal levels. Therefore, in both cases, the comparison time is significantly reduced.

B. Binary Capacitive Ladder and Bit Weight Calibration

A binary capacitive ladder [3] is used to dramatically reduce the effective input capacitance to 84fF, which shorten the DAC settling time. The capacitor array (Fig 5.) is implemented with low-cost metal-oxide-metal capacitors and particular care must be taken to achieve adequate accuracy. The parasitic capacitance due to interconnect and the capacitor itself were carefully considered by iteratively estimating capacitance at floating nodes and the corresponding ratio of α and β. Each α cap is divided into two α /2 caps, located at the top and bottom of a column cell. By this means, it not only compensates for the vertical process variation, but also provides better differential matching by interleaving the positive-side and negative-side capacitor arrays. Dummy capacitances are placed on each side for matching purpose. α and β values are chosen such that the equivalent radix for the capacitive ladder is 1.9~2, essentially a binary network. One bit redundancy is implemented for testing and to avoid significant weight loss.

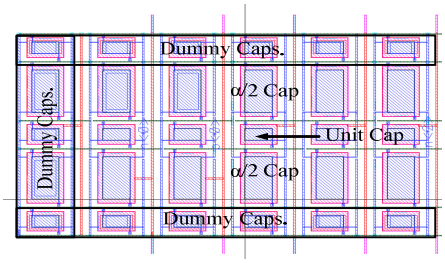

Fig. 5 Binary Capacitive Ladder with improved symmetry

The passive bottom plate sampling network is combined with the binary capacitive ladder. Relatively small switches could be used while still maintaining high input bandwidth of much more than 10GHz. The ratio between the switches is designed such that the equivalent RC constants are about the same for all bits.

The unpredicted parasitic variation and capacitor mismatch result in a change of the effective radix for each bit. The discrepancies cause the variation of the bit weights and lead to non-linearity of the ADC. This systematic error is compensated by foreground off-chip calibration by injecting a known full-range sinusoidal signal. The converted digital outputs are used to reconstruct the initial input signal. The bit weights are calibrated using an adaptive algorithm to minimize the mean-square error.

C. Opposite Phase Clocks with Tunable Duty Cycle

The internal non-overlapping sampling clocks with 180 degree phase shift are generated on-chip for this prototype. It is achieved using two off-chip square waves with 50% duty cycle. The clocks are buffered in the chip. The phase skew between two clocks is tunable, such that the duty cycle of the sampling clock is adjustable, when combined with an AND gate. This tunable duty cycle enables a flexible time allocation between tracking and conversion. Particular care was taken in the layout to generate and distribute the opposite clocks to ensure the 180 degree phase shift, because any imbalance from the two sampling clocks, as well as undesired clock jitter caused by the noise from the generation and distribution network will result

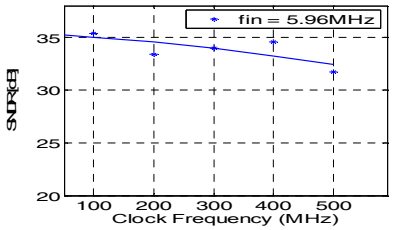

Fig. 6 Measured SNDR versus sampling freq. for single ADC

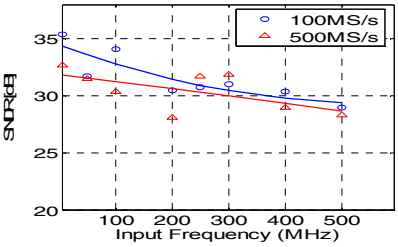

Fig. 7 Measured SNDR versus input frequency for single ADC

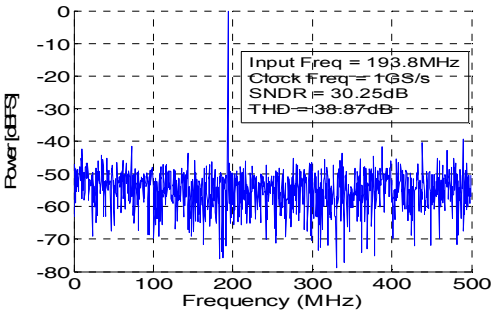

Fig. 8 Measured power spectrum and SNDR versus sampling frequency for interleaved ADC

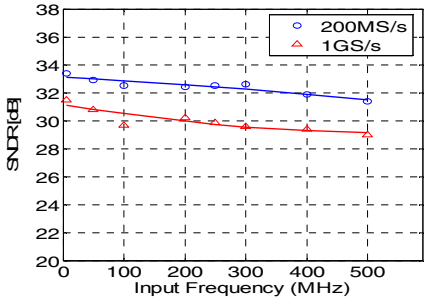

Fig. 9 Measured power spectrum and SNDR versus input frequency for interleaved ADC

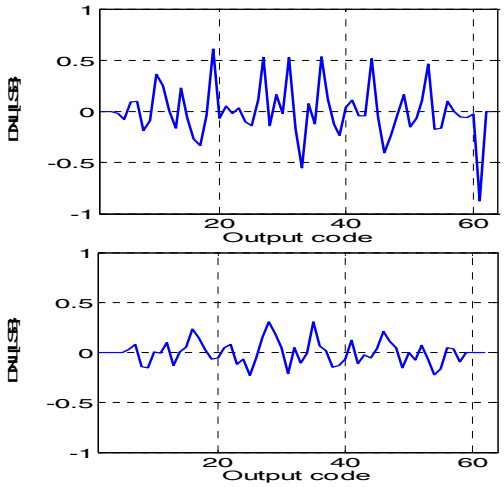

Fig. 10 DNL before and after calibration

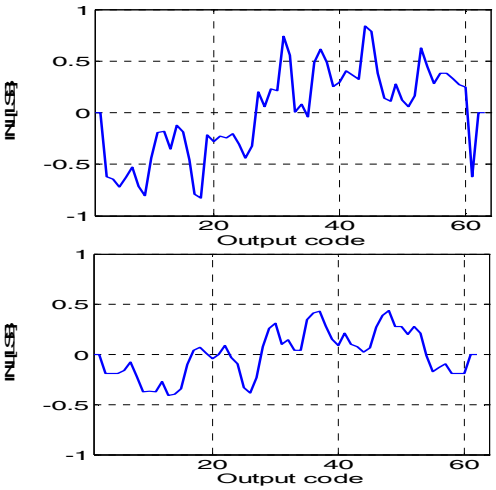

Fig. 11 INL before and after calibration

in distortion and degradation in interleaved ADCs performance.

Measurement Results and Conclusion

The converter is implemented in a 1.2-V 65nm Low-power CMOS process. Each ADC only occupies an area of 0.35 x0.16mm^2. The measured results show effective number of bits (ENOB) of a single ADC scales from 5.6b at 100MS/s to 5b at 500MS/s (Fig. 6), as well as the SNDR when input is above the Nyquist rate (Fig. 7), demonstrating the straight forward tradeoff between ENOB and conversion rate. Fig. 8 and Fig. 9 show the two time-interleaved ADC performance is increased to 1GS/s at twice the power and area. The static performance of the interleaved ADC is also characterized by DNL and INL measurements (Fig. 10, Fig. 11). After the digital calibration for the bit weights and the subtraction of the offset, DNL is improved by almost half LSB and INL is improved by more than 0.7LSB. The clock skew between two clocks at high frequencies is calibrated, resulting in only 0.7dB degradation in SNDR. The chip microphotograph is show in Fig 12. The total active area is 0.11mm^2. Analog, digital and clock consumes 1.51mW, 4.05mW and 1.16mW respectively at 1GS/s. With FOM defined as power/2^{ENOB}×fs, the interleaved ADCs achieve 0.21pJ/conversion. The total die size is 1.6×1.4mm^2.

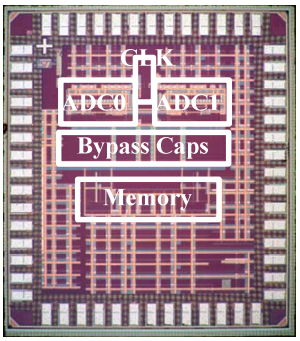

Fig. 12 Chip micrograph

Acknowledgements

The authors acknowledge the contributions of Mike Chen, the NSF Infrastructure Grant No. 0403427, wafer fabrication donation of STMicroelectronics, and the support of the C2S2.

References

[1] E. Alpman, H. Lakdawala, L.R. Carley, K. Soumyanath, "A 1.1V 50mW 2.5GS/s 7b Time-Interleaved C-2C SAR ADC in 45nm LP Digital CMOS", IEEE ISSCC 2009 Dig. Of Tech. Paper, pp. 65-77. Feb. 2009

[2] Y. Lin, S. Chang, Y. Liu, C. Liu, G. Huang, "A 5b 800MS/s 2mW Asynchronous Binary-Search ADC in 65nm CMOS

[3] J. Yang, R.W. Brodersen, "Spatial Channel Characterization for Cognitive Radios", MS thesis, 2004

[4] J. Yang, R.W. Brodersen, and D. Tse, "Addressing the Dynamic Range Problem in Cognitive Radios", *IEEE International Conference on Communications*, pp. 5183 - 5188, June, 2007.

[5] S. W. M. Chen and R. W. Brodersen, "A 6b 600MS/s 5.3mW Asynchronous ADC in 0.13 um CMOS," *IEEE, ISSCC 2006, Dig. of Tech. Papers,* pp. 574-575. Feb. 2006.