# A Digital-Intensive Multimode Multiband Receiver Using a Sinc$^2$ Filter-Embedded VCO-Based ADC

Jaewook Kim, *Student Member, IEEE*, Wonsik Yu, *Student Member, IEEE*, and SeongHwan Cho, *Senior Member, IEEE*

***Abstract*—In this paper, we present a 0.2–1.8-GHz digital-intensive receiver front-end using a voltage-controlled oscillator (VCO)-based analog-to-digital converter (ADC) running at 1.4 Gs/s in 90-nm CMOS. To improve the out-of-band rejection, we propose a second-order anti-aliasing Sinc filter that can be embedded in the ADC, which exploits the integrating nature of a VCO. the nonideal effect of the proposed architecture is analyzed with regard to the waveform imperfection due to device mismatch. The proposed receiver achieves −94 dBm of sensitivity at 1-MHz bandwidth and −6.8 dBm of IIP3, while providing 50-dB rejection of aliased signals.**

***Index Terms*—Anti-aliaising filter, digital-intensive, direct-conversion receiver, highly digitized, multimode multiband, Sinc$^2$ filter, software-defined radio, voltage-controlled oscillator (VCO)-based analog-to-digital converter (ADC).**

## I. Introduction

AS THE number of wireless communication standards increase, multimode multiband (MMMB) receivers that can cover multiple standards is garnering much attention. It is, however, difficult for a conventional analog receiver to achieve such versatility, since analog baseband circuits such as variable-gain amplifiers (VGAs) and low-pass filters (LPFs) are not easily programmable. In order to cope with this problem, a discrete-time MMMB receiver has been proposed in [1], where LPFs and VGAs are implemented using switches and capacitors. While such an architecture avoids the use of sophisticated analog circuits, thereby enabling higher programmability, the receiver itself is still based on analog signal processing and hence is vulnerable to device mismatch and PVT variations (see Fig. 1).

As an alternative solution to a discrete-time receiver, a digital-intensive MMMB receiver can be employed where a wide-dynamic range analog-to-digital converter (ADC) is used. The main advantages of this architecture are the removal of the VGA and the implementation of filters in digital domains, which not only offer high programmability but also provide better immunity to device mismatch and PVT variations.

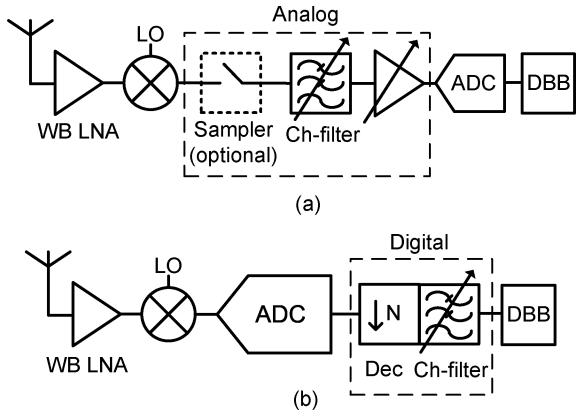


Fig. 1. Wireless RF MMMB receiver architectures. (a) Conventional analog-intensive receiver. (b) Proposed digital-intensive receiver.

With such advantage in mind, direct-RF digitizing receiver and digital intensive direct conversion receiver have been introduced. In a direct-RF receiver, the key component is the bandpass ADC that quantizes the desired signal located at RF. Unfortunately, RF bandpass ADCs based on $G_m$-*LC* filters are not widely tunable and consume a large amount of power and area [2], [3]. Furthermore, such an ADC is highly analog-intensive and is not suitable for future nanoscale CMOS processes. Although a widely tunable time-domain bandpass ADC that exploits fast switching time of advanced CMOS has been proposed in [4]–[6], it requires a highly tunable anti-aliasing filter at RF that is a very challenging component.

To avoid such complexity of direct-RF sampling, a passive mixer can be added between the LNA and the ADC, which relaxes the requirement of the ADC from a bandpass to a low-pass, allowing a conventional continuous-time (CT) $\Delta\Sigma$ ADC to be used. However, CT $\Delta\Sigma$ ADC suffers from stability issues and requires several operational amplifiers (op-amps) which are not suitable for deep-submicrometer CMOS process. Although such op-amps are replaced by switches and capacitors in the discrete-time $\Delta\Sigma$ ADC [7], a large amount of gain is required in the low-noise amplifier (LNA) due to the signal loss in the integration stages, when [7] applies to the receiver. In addition, a high-performance anti-aliasing filter is also required because interferers in odd harmonics of the sampling frequency are not rejected by the embedded filtering process.

A first-order noise-shaped voltage-controlled oscillator (VCO)-based ADC is a promising architecture because it can be implemented using ring VCOs and digital circuits, which

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J. Kim was with the Department of Electrical Engineering, Korea Advanced Institute of Science and Technology (KAIST), Daejon 305–701, Korea. He is now with the Electrical Engineering and Computer Science Department, Massachusetts Institute of Technology, Cambridge, MA 02139 USA (e-mail: jaeuk83@gmail.com).

W. Yu and S. Cho are with the Department of Electrical Engineering, Korea Advanced Institute of Science and Technology (KAIST), Daejon 305–701, Korea (e-mail: wonsik.yu@gmail.com; chosta@ee.kaist.ac.kr).

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are much more digital-friendly than conventional delta–sigma ADCs [8]. In addition, the VCO-based ADC provides an inherent first-order anti-aliasing Sinc filter from the integration nature of the VCO. In [9], a digital-intensive receiver exploiting the VCO-based ADC has been proposed, but its target was not a MMMB but a single-mode single-band (2.4-GHz) application. The extension of such an approach to an MMMB receiver is difficult because the first-order Sinc filter in the VCO-based ADC does not provide sufficient out-of-band rejection for MMMB receivers that do not have an RF pre-filter. Therefore, a higher order anti-aliasing filter is required.

In this paper, we propose a second-order anti-aliasing Sinc filter (Sinc$^2$ filter) that can be embedded in a VCO-based ADC [10]. There have been several research works about stand-alone VCO-based ADCs with regard to improving linearity or noise-shaping order [8], [11], [12]. In [11], a negative feedback loop is used to enhance the noise-shaping order and alleviate the effect of VCO nonlinearity. In [12] and [13], a background calibration technique is used to improve linearity by extracting the harmonic coefficients of VCO from the replica VCO-based ADC. In [8], a lookup table (LUT) and a ramp signal are used to store and calibrate the nonlinear characteristic of the VCO. However, none of the above works have looked into improving the embedded Sinc filter of the VCO-based ADC for a wireless RF receiver. In this paper, we present an MMMB RF receiver that employs VCO-based ADC with an embedded Sinc$^2$ filter [10]. In addition to providing an in-depth analysis of the architecture and its operation principle, we theoretically analyze the proposed Sinc$^2$ filter and investigate the nonideal effects from waveform approximation and errors from amplitude and phase.

This paper is organized as follows. First, the anti-aliasing property of the VCO-based ADC is briefly reviewed in Section II. Second, operation principle of the proposed Sinc$^2$ filter and its implementation in VCO-based ADC are explained in Section III. Third, nonideal effects of the proposed architecture are analyzed in Section III. Next, implementation of the MMMB receiver using the proposed VCO-based ADC is described in Section IV, and measurement results are shown in Section V. Finally, conclusions are drawn in Section VI.

## II. Background: VCO-Based ADC

### A. Quantization Noise Characteristic

In a VCO-based ADC, the VCO integrates the analog input signal as output phase and quantizes it in the form of rising or falling edges. The reset counter counts the number of edges during a sampling period and produces the digital output. The noise-shaping property of the VCO-based ADC can be explained by using phase-domain analysis as shown in Fig. 2 [8]. It can be seen that the residual phase (quantization noise $\phi_q[n-1]$) of the previous sampling period inherently becomes the initial phase $\phi_i[n]$ of the next period. Therefore, the output of the VCO-based ADC ($y[n]$) can be represented as

$$y[n] = \frac{N_{mp}}{2\pi}\left(\phi_x[n] + \phi_q[n-1] - \phi_q[n]\right) \tag{1}$$

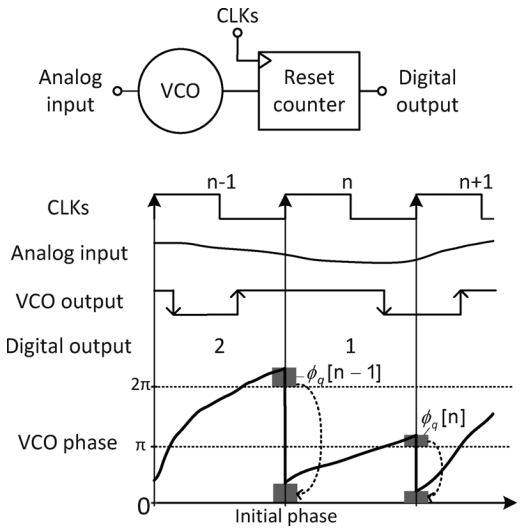


Fig. 2. Waveform of VCO-based ADC. $\phi_q[n]$ represents the amount of phase corresponding to quantization error in the $n$th sampling period.

where $N_{mp}$ is the number of the VCO phase and $\phi_x[n]$ is the VCO phase change due to the analog input. Since the $z$-transform of (1) produces $(1-\mathrm{z}^{-1})\mathrm{Q(z)}$, the quantization error of the VCO-based ADC is first-order shaped and, hence, is equivalent to a first-order delta–sigma modulator. The theoretical signal-to-quantization-noise ratio (SQNR) can be represented as [8]

$$\begin{aligned}\mathrm{SQNR} =& 6.02\log_2\left(\frac{f_{tune}N_{mp}}{f_s}\right) - 3.41 + 30\log \mathrm{OSR} \\ &+ 20\log\left(\mathrm{sinc}\left(\frac{1}{2\mathrm{OSR}}\right)\right)\end{aligned} \tag{2}$$

where $f_{\mathrm{tune}}$ is the tuning range of the VCO. When the VCO-based ADC is applied to a digital-intensive receiver based on an LNA-mixer-ADC configuration, it should have a large SQNR to compensate for the absence of VGA. Since the VCO-based ADC can be implemented by using mostly digital circuits and as it does not have any feedback loop, a high sampling frequency of several gigahertz can be easily achieved in advanced CMOS process. Therefore, despite low noise-shaping order, a large SQNR can be obtained due to high OSR.

### B. Signal Transfer Characteristic

From the input signal standpoint, the analog input signal is integrated, sampled, and then differentiated, which corresponds to the operation of a first-order Sinc filter. When the VCO-based ADC is used after the mixer in the digital-intensive receiver, there will be out-of-band interferers that are integer multiples of the sampling frequency apart from the desired signal, which will be aliased down to dc, as shown in Fig. 3. Fortunately, these interferers will be suppressed by the inherent anti-alias filter of the VCO-based ADC, and its rejection ratio can be described as

$$\mathrm{Rejection\ ratio} = 20\log\left(\mathrm{Sinc}\left(\frac{f_{\mathrm{int}}}{f_s}\right)\right) \tag{3}$$

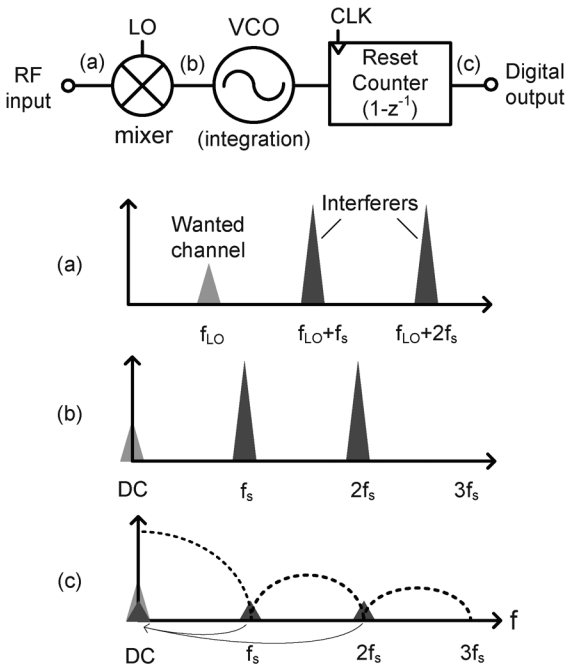


Fig. 3. Embedded first-order Sinc filter of VCO-based ADC.

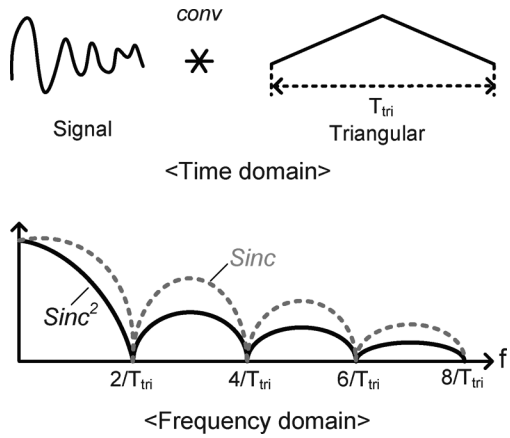


Fig. 4. Basic principle of Sinc$^2$ filter.

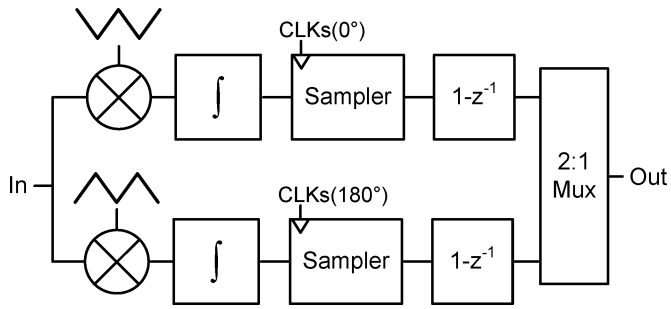


Fig. 5. Sinc$^2$ filter in the sampling system.

where $f_{\text{int}}$ is the frequency where the interferer is located. It can be seen that increasing the sampling rate improves the out-of-band rejection ratio by 20 dB/dec. While [9] may be sufficient for narrowband applications where there exists an RF prefilter, it is not enough for wideband applications where the RF prefilter is absent. For example, if 40 dB of additional filtering is to be achieved for a VCO-based ADC clocked at 400 MHz [9], the sampling rate must be increased by a factor of 100 to 40 GHz, which is not really feasible in a low-power implementation. Therefore, there is a strong motivation to increase the order of the Sinc filter to apply the VCO-based ADC for wideband applications.

## III. SINC$^2$ FILTER-EMBEDDED VCO-BASED ADC

### A. Operation Principle of Sinc$^2$ Filter

The rejection ratio of a second-order Sinc filter (Sinc$^2$ filter) is given by

$$\text{Rejection ratio} = 40\log\left(\text{Sinc}\left(\frac{f_{\text{int}}}{f_s}\right)\right) \tag{4}$$

where it can be seen that the rejection ratio is doubled compared with a first-order Sinc filter. Therefore, the required sampling frequency of a Sinc$^2$ filter can be ten times lower than that of a Sinc filter while meeting the same rejection ratio.

The basic principle of a Sinc$^2$ filter is shown in Fig. 4. A Sinc$^2$ function is a time-domain convolution of the input with a triangular waveform whose period is $T_{\text{tri}}$. The null location $(f_{\text{null}})$ of the Sinc$^2$ filter is related to the period of the triangular waveform (in a way that $f_{\text{null}} = 2/T_{\text{tri}}$). In our proposed receiver, Sinc$^2$ is followed by an ADC that has a sampling process. Hence, a Sinc$^2$ filter with sampling can be implemented as shown in Fig. 5, where the input is convoluted with a triangular waveform (i.e., multiplied by a triangular waveform and integrated) and sampled. As the first desired null location of the Sinc$^2$ filter is $1/T_s$, where $T_s$ is the sampling period of the ADC, the triangular waveform must have a period of $2T_s$ (i.e., $T_{\text{tri}} = 2T_s$). Therefore, a two-way time-interleaving is required for seamless operation of the Sinc$^2$ filter.

### B. Approximation of Triangular Waveform

In the proposed Sinc$^2$ filter, the triangular waveform is approximated to a staircase waveform to alleviate the analog efforts in its implementation. To investigate the effect of such approximation, let us consider the staircase waveform as a result of sampling and holding a triangular waveform as shown in Fig. 6(a). In order to denote how well a staircase approximates the triangular waveform, we introduce a term denoted as triangular waveform sampling ratio (TSR) described as

$$\text{TSR} = \frac{f_{s,\text{tri}}}{f_{\text{tri}}} \tag{5}$$

where $f_{\text{tri}}$ is the frequency of the triangular waveform and $f_{s,\text{tri}}$ is the frequency of the clock that samples the triangular waveform. Basically, (5) indicates how many times the triangular waveform is sampled per period. Hence, a staircase with higher TSR has stronger resemblance to a triangular waveform. The effect of sampling and holding the triangular waveform can be viewed in the frequency domain shown in Fig. 6(b). It can be seen that sampling results in aliasing, causing the nulls to disappear at integer multiples of the sampling frequency $(f_{s,\text{tri}})$. The holding operation results in Sinc filter that restores nulls at integer multiples of $f_{s,\text{tri}}$. However, the frequency response

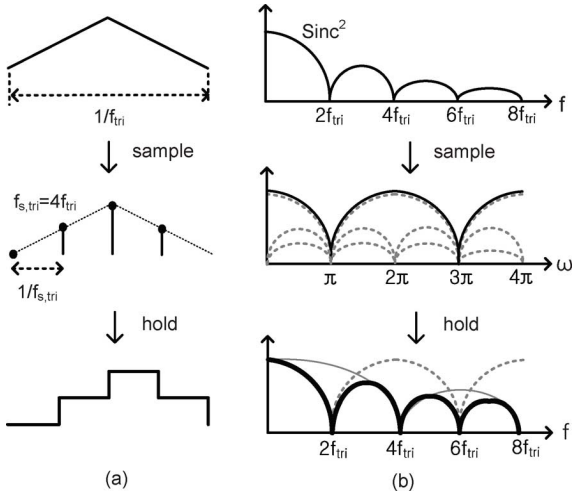


Fig. 6. Approximation of triangular waveform to staircase waveform. TSR= 4. (a) Time-domain view of staircase waveform. (b) Frequency-domain view of staircase waveform.

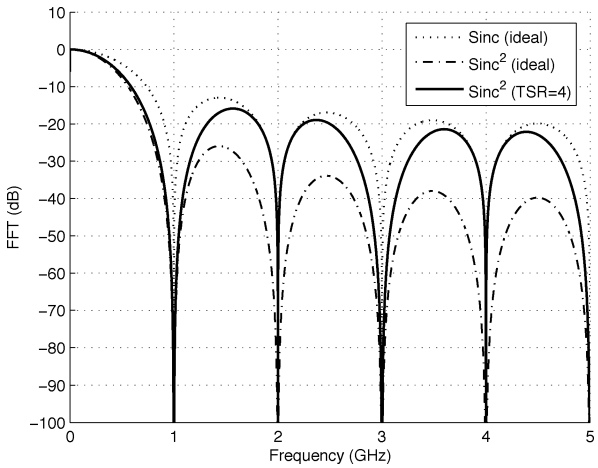


Fig. 7. Frequency response of Sinc$^2$ filter with $\mathrm{TSR} = 4$.

around $f_{s,\mathrm{tri}}$ is no longer Sinc$^2$ but Sinc. Therefore, the staircase approximation reduces the rejection ratio at the sampling frequency $f_{s,\mathrm{tri}}$ and its multiples.

The above analysis is verified in a MATLAB simulation shown in Fig. 7, for the case when $f_s = 1$ GHz, $f_{\mathrm{tri}} = 0.5$ GHz, and $f_{s,\mathrm{tri}} = 2$ GHz. It can be seen that the simulated output spectrum obeys the theoretical analysis shown in Fig. 6. The filtering property of Sinc$^2$ filter with a TSR of 4 follows that of a Sinc$^2$ filter at the odd multiples of $f_s$ and that of a Sinc filter at the even multiples of $f_s$. Fig. 8 shows the filtering properties of the Sinc$^2$ filter with TSRs of 4 and 8 when the simulation condition is kept the same. Increasing $f_{s,\mathrm{tri}}$ by a factor of two causes the filtering property to be more similar to an ideal Sinc$^2$ filter.

Although a larger TSR provides filtering that is closer to the ideal Sinc$^2$ filter, it also increases the implementation cost, that is, a circuit generating an approximated triangular waveform with a larger TSR requires a clock signal with a frequency of $f_{s,\mathrm{tri}}$ that is also higher. It means that it dissipates a larger current and its maximum operating speed limits the maximum sampling frequency ($f_s$) of the proposed Sinc$^2$ filter-embedded

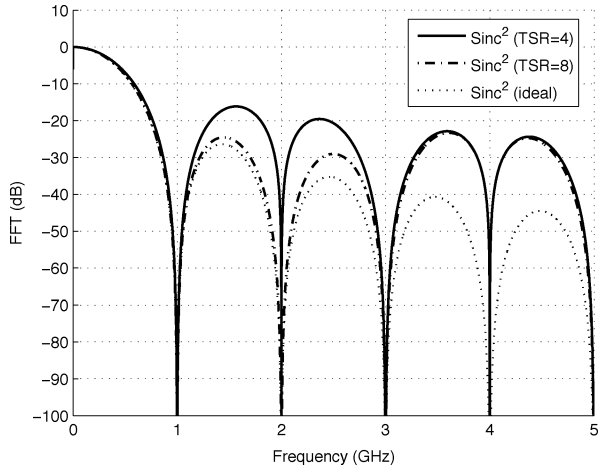


Fig. 8. Comparison between filtering properties when $\mathrm{TSR} = 4$ and $\mathrm{TSR} = 8$.

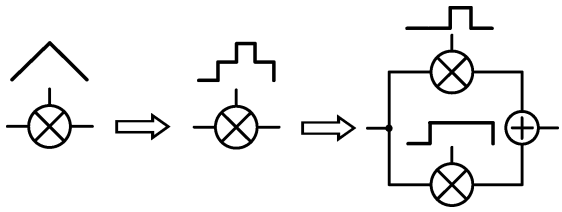

Fig. 9. Approximation of triangular waveform. Triangular waveform is approximated to staircase waveform that is realized by the addition of two rectangular waveforms.

ADC. In addition, a higher TSR increases the vulnerability of the approximated triangular waveform to implementation issues such as device mismatches, as it requires more staircases that should have even interval and height. In this paper, we set TSR to 4 such that $f_{s,\mathrm{tri}}$ becomes 2.8 GHz in our implementation, when the sampling frequency of the Sinc$^2$ filter-embedded ADC is 1.4 GHz.

### *C. Proposed Sinc$^2$ Filter Implemented Using VCO-Based ADC*

The staircase waveform can be realized by adding two rectangular waveforms with different duty cycles as shown in Fig. 9. Hence, multiplying the input by the staircase waveform can be implemented using mixers and adding their outputs.

While the Sinc$^2$ filter shown in Fig. 5 can be difficult to implement in conventional designs, it can be easily implemented by using a VCO-based ADC that operates in the time domain, that is, the integrator can be implemented by using a VCO that inherently integrates the input voltage to phase. The difference operator $(1 - z^{-1})$ is implemented by using a reset counter which quantizes the VCO phase by counting the rising edges of the VCO output during a sampling period.

Fig. 10 shows the detailed implementation of the proposed Sinc$^2$ filter. Note that two rectangular waveforms with different duty cycle are applied to the two multipliers and their outputs are summed in the adder. The adder is implemented in the current domain by using the transconductance of the delay cell in the ring VCO. The control transistors $\mathrm{M}_{C1}$ and $\mathrm{M}_{C2}$ converts the gate voltages into currents that are added at the tied drains. The multiplier receiving rectangular waveform and input

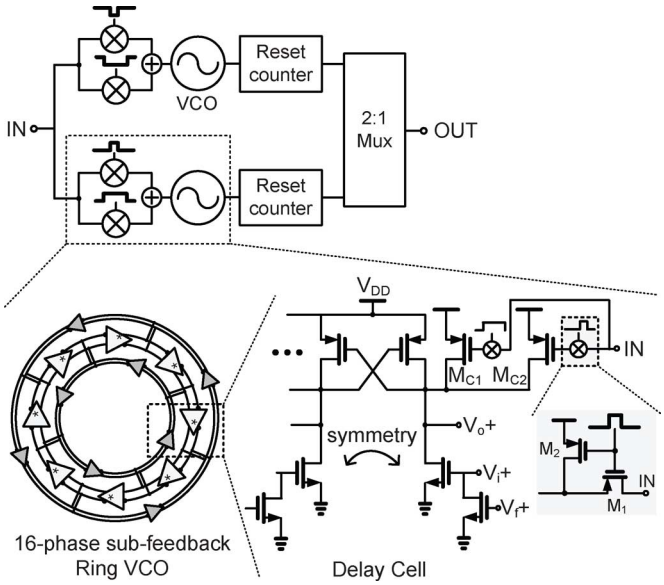


Fig. 10. Proposed Sinc$^2$ filter exploiting a VCO-based ADC.

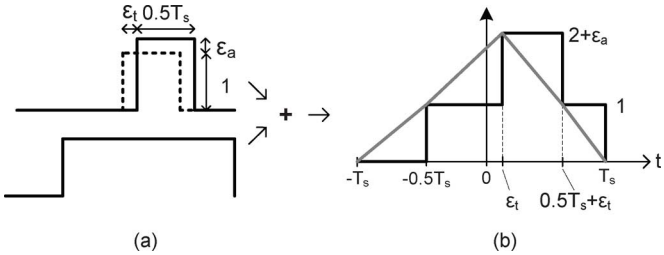


Fig. 11. Nonideal effect due to the amplitude and phase error.

signal is implemented as a single-balanced passive mixer. Compared with the VCO-based ADC with an embedded Sinc filter, the overhead in implementing the Sinc$^2$ filter-embedded VCO-based ADC is one control transistor and two passive mixers per each delay cell, two-way time-interleaving and rectangular waveform generator.

## IV. Nonideal Effect: Waveform Imperfection

An imperfect triangular waveform can degrade the performance of the proposed Sinc$^2$ filter. As shown in Fig. 11(a), the effect of waveform imperfection can be divided into amplitude mismatch and phase mismatch.

*1) Amplitude Error:* The triangular waveform can be distorted by the mismatch between the two transconductors $\mathrm{M}_{C1}$ and $\mathrm{M}_{C2}$ in Fig. 10. The strength difference between the two transistors will cause amplitude error in a staircase waveform as shown in Fig. 11(b). In order to analyze it without complexity, we will not consider a distorted staircase waveform (black line) but a distorted triangular waveform (gray line). The effect of approximation of the triangular waveform to the staircase waveform was described in Section III-B in detail. Defining the amplitude error as $\epsilon_a$, the Fourier transform of the distorted triangular waveform can be expressed as

$$H_{\epsilon,a}(\omega) = T_s\left(2\mathrm{Sinc}^2\left(\frac{f}{f_s}\right) + \frac{\epsilon_a}{2}\mathrm{Sinc}^2\left(\frac{f}{2f_s}\right)\right) \quad (6)$$

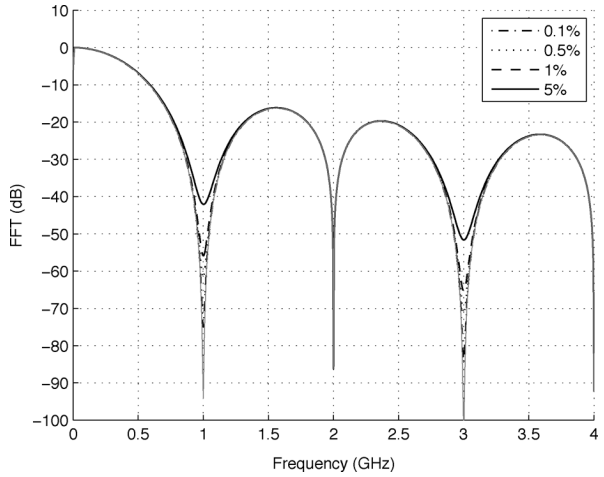


Fig. 12. Effect of amplitude error.

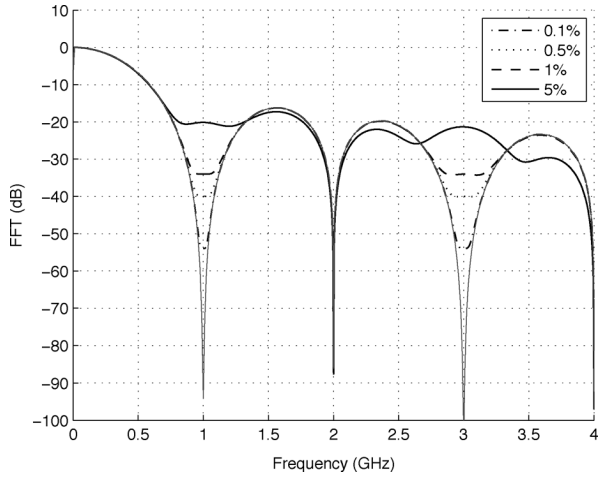


Fig. 13. Effect of phase error.

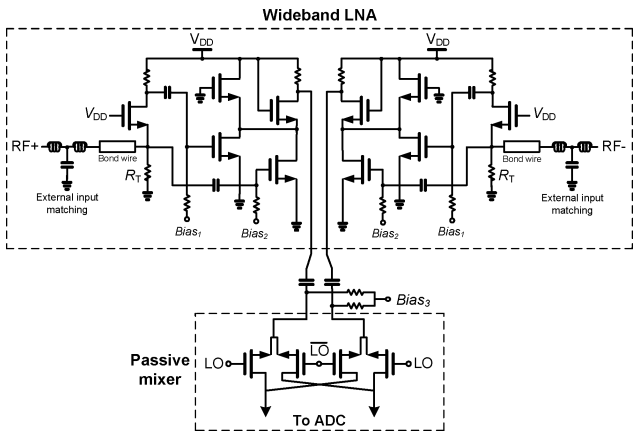


Fig. 14. Digital-intensive MMMB receiver using a Sinc$^2$ filter-embedded VCO-based ADC.

where it can be seen that amplitude mismatch adds a second term that has nulls only at even integer multiples of $f_s$. Therefore, as the amplitude mismatch is present, the rejection ratio of the Sinc$^2$ filter at the odd multiples of $f_s$ will be degraded. Fig. 12 shows the MATLAB simulation result of the proposed

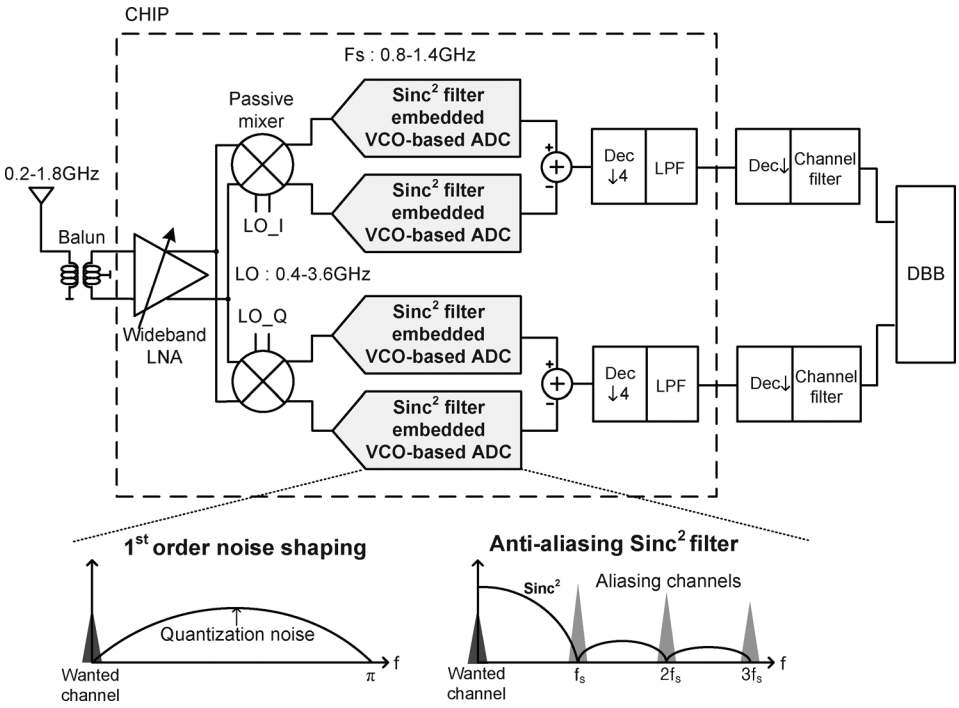


Fig. 15. Schematic of wideband LNA.

Sinc$^2$ filter with amplitude error of 0.1%–5% when the sampling frequency is 1 GHz. It shows that the simulation result corresponds to the analysis in (6). It also shows that the amplitude mismatch should be less than 5% in order to achieve 40-dB rejection at the first null.

*2) Phase Error:* The triangular waveform can also be distorted by the phase mismatch between the two rectangular waveforms as shown in Fig. 11. Denoting the phase error as $\epsilon_t$, the Fourier transform of the distorted triangular waveform can be expressed as

$$H_{\epsilon,p}(\omega) = \frac{4}{T_s\omega^2}\left(1-\cos(\omega T_s)\cos(\epsilon_t)\right) + j2\epsilon_t\cos(\omega T_s) + \frac{2\epsilon_t}{T_s}\left(2+e^{j\omega\left(\frac{T_s}{2}+\epsilon_t\right)}-e^{j\omega\frac{T_s}{2}}\right). \quad (7)$$

It can be seen that the first term would be exactly the same with the transfer function of the Sinc$^2$ filter if $\epsilon_t$ was zero. Considering that $\epsilon_t$ is about a few picoseconds in real implementation, the effect of $\epsilon_t$ is negligible in the first and second terms. In the third term, the difference of two exponential terms becomes a noticeable error even though $\epsilon_t$ is very small, that is, the exponential terms represent periodic signals in the frequency domain whose frequency is $2/(T_s+2\epsilon_t)$ and $2/T_s$, respectively. Unfortunately, the amplitude difference of these two periodic signals having slight frequency difference has peak values at the integer multiples of $f_s$, which are null frequencies of the Sinc$^2$ filter.

Fig. 13 shows the MATLAB simulation result of the proposed Sinc$^2$ filter with phase error of 0.1%–5% when the sampling frequency is 1 GHz. It can be seen that, for the same percentage errors, the phase error degrades the rejection property of the Sinc$^2$ filter much more than the amplitude error, as shown in Fig. 12. It corresponds to the above analysis in that the error due to phase mismatch has peak values at the nulls of the Sinc$^2$ filter. In order to achieve a rejection ratio above 40 dB at the first null, the phase mismatch should be less than 0.5%.

## V. MMMB Receiver

The block diagram of the implemented MMMB receiver using the proposed Sinc$^2$ filter-embedded VCO-based ADC is shown in Fig. 14. The receiver covers signals at 0.2–1.8 GHz with wideband LNA that amplifies the signal by 8 or 16 dB in low or high-gain mode, respectively. Four ADCs are required for differential I/Q signals, as the ADC receives single-ended input. The output of the passive mixer is directly connected to the input transistor of the proposed VCO-based ADC. An implicit first-order LPF is formed by the on-resistance of the switch transistor and the input capacitance of the ring VCO.

The tradeoff between linearity and noise in a generic receiver can be applied to the receiver using a VCO-based ADC in the same way. The nonlinear voltage-to-frequency characteristic of the VCO in a VCO-based ADC can degrade the linearity performance of the receiver such as IIP2 and IIP3. Note that IIP2 can be easily improved by exploiting a differential configuration in the VCO-based ADC, as shown in Fig. 14. In the case of IIP3, unless additional calibration techniques are used [8], [12], LNA gain should be adjusted to reduce the power of interferers that will generate a third-order intermodulation term (IM3) through the VCO nonlinearity. Based on the target noise figure of the receiver and the LNA gain which is set by the VCO nonlinearity, noise specification of the VCO-based ADC can be determined. In a generic receiver, improving the linearity by reducing the gain imposes a stringent requirement on noise. In this work, LNA gain in high-gain mode is determined as 16 dB based on the simulation result of IIP3 of the proposed VCO-based ADC, which is +12.5 dBm.

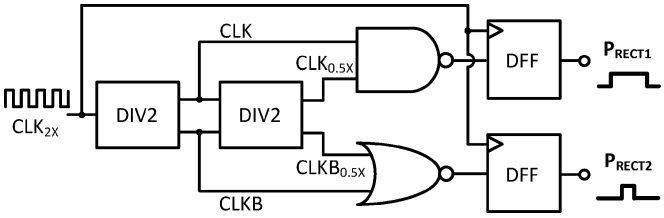


Fig. 16. Schematic of a rectangular waveform generator.

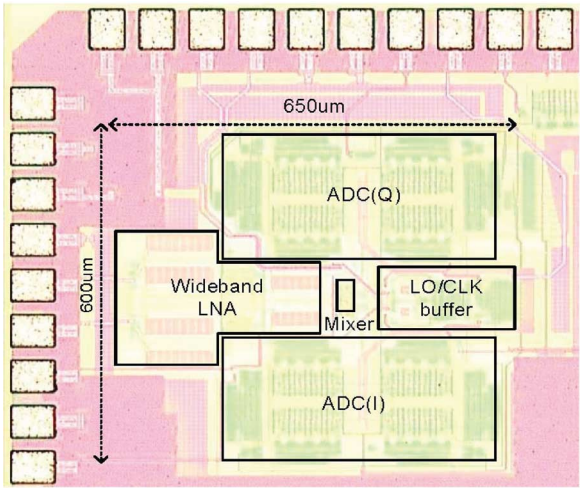


Fig. 17. Chip micrograph.

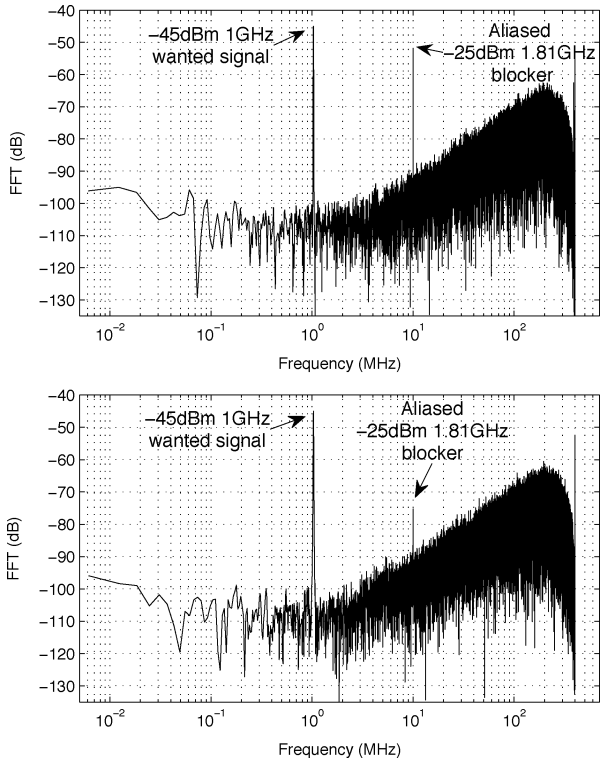


Fig. 18. Measured output spectra with the Sinc filter and the proposed Sinc$^2$ filter.

The wideband LNA is based on a noise-cancelling architecture using a common-gate and common-source amplifier, as shown in Fig. 15. In order to achieve wideband input impedance matching, an external *LC* ladder filter and a termination resistor $(R_T)$ is adopted.

The ADC employs a 16-phase subfeedback differential ring VCO so as to increase the tuning range while maintaining the frequency for enhanced time-resolution and high SNR. Depending on the target SNR, the sampling frequency can be changed from 800 MHz to 1.4 GHz, where the lower frequency is determined so as to allow one-bit quantization in the counter, i.e., so that the output of the counter is either one or zero [8]. The maximum frequency is determined by the maximum operating frequency of the following digital decimation filter. Scaling sampling frequency also enables scaling of power consumption, since the VCO-based ADC is implemented using mostly digital circuits. Note that the effect of PVT variation in the ring VCO c,an be significantly alleviated by exploiting a differential configuration of VCO-based ADC as shown in Fig. 14. The error due to the PVT variation in a ring VCO are rejected as a common-mode noise where the rejection is limited by the mismatch between two ring VCOs.

The schematic of the rectangular waveform generator for the proposed Sinc$^2$ filter is shown in Fig. 16. A clock signal $(\mathrm{CLK}_{2X})$ whose frequency is twice the sampling frequency of the ADC goes through two divide-by-two circuits. The outputs of the dividers are combined using logic gates and captured by D flip-flop to generate two synchronous rectangular pulses ($\mathrm{P}_{\mathrm{RECT1}}$ and $\mathrm{P}_{\mathrm{RECT2}}$) with duty cycles of 0.25 and 0.75, respectively.

## VI. Measurement Results

The die microphotograph of the proposed receiver front-end is shown in Fig. 17. The core area is less than 0.4 mm$^2$, where the LNA accounts for 0.06 mm$^2$ and the differential I/Q ADCs occupy 0.19 mm$^2$. A $-45$ dBm desired signal at 1.001 GHz and a $-25$ dBm out-of-band interferer at 1.810 GHz that will be aliased to 10 MHz after down conversion are applied to the input of the receiver that has 1-GHz LO and 800-MHz ADC sampling clock. The measured output spectrums with the Sinc filter and the proposed Sinc$^2$ filter are shown in Fig. 18(a) and (b), respectively. The conventional Sinc filter is obtained by bypassing the multiplier in the ring VCO. The proposed Sinc$^2$ filter achieves an out-of-band rejection ratio of 50.2 dB, which is almost twice as large as 25.5 dB of the Sinc filter. Note that the quantization noise nulls at dc and $\pi$ are seen due to the two-way time-interleaving of the VCO-based ADC. The rejection ratio of the Sinc filter and Sinc$^2$ filter when the frequency of the out-of-band interferer is changed from 1.8001 to 1.81 GHz is shown in Fig. 19, where the interferer is aliased to 100 kHz–10 MHz. It can be seen that the rejection ratio of the two filters are relatively constant even when the aliased frequency is close to dc. Simulation results show that the rejection ratio is limited by clock jitter and mismatch among the delay cells. The measured output spectrum with $-28$ dBm two-tone test is shown in Fig. 20, where it can be seen that the in-band IIP3 is $-6.78$ dBm. The SNDR as a function of the RF input power is shown in Fig. 21 when the LO frequency is 1 GHz, sampling frequency is 1.4 GHz, and the input bandwidth is 1 and 10 MHz, respectively. Assuming that the required system SNR is 10 dB, the proposed receiver achieves

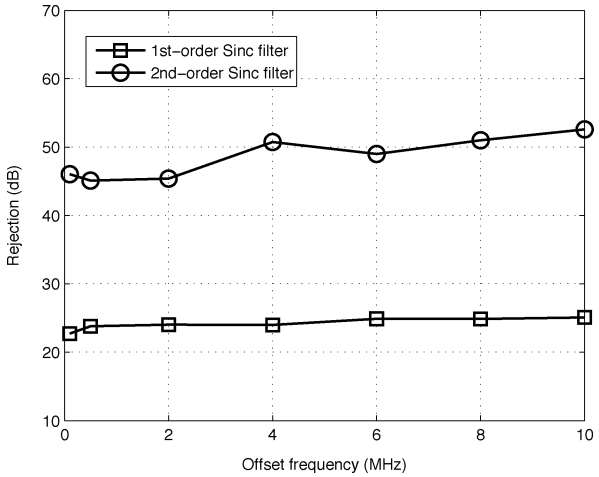


Fig. 19. Rejection ratio of the Sinc filter and Sinc$^2$ filter.

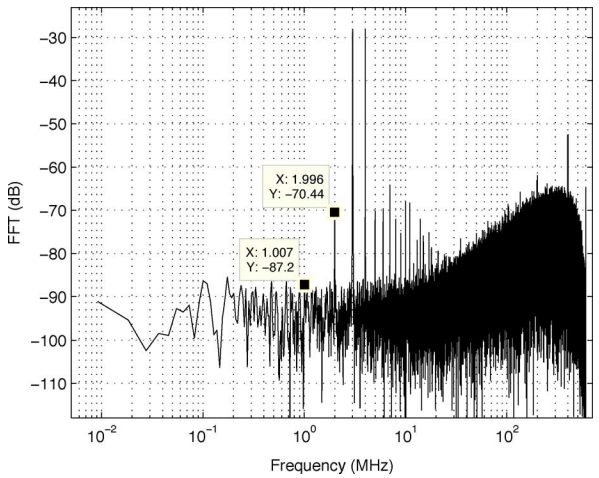


Fig. 20. Measured output spectrum with $-28$ dBm two-tone test.

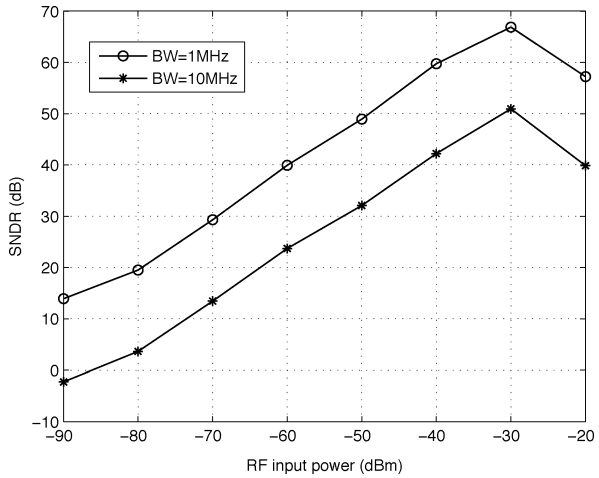


Fig. 21. SNDR as a function of the RF input power.

sensitivity levels of $-94$ and $-74$ dBm for 1- and 10-MHz bandwidth, respectively. The SNR versus RF carrier frequency from 0.2 to 1.8 GHz is shown in Fig. 22 for the case when the RF input power is $-35$ dBm and the sampling frequency is 1.4 GHz. The performance is summarized in Table I. The measured IIP2 is

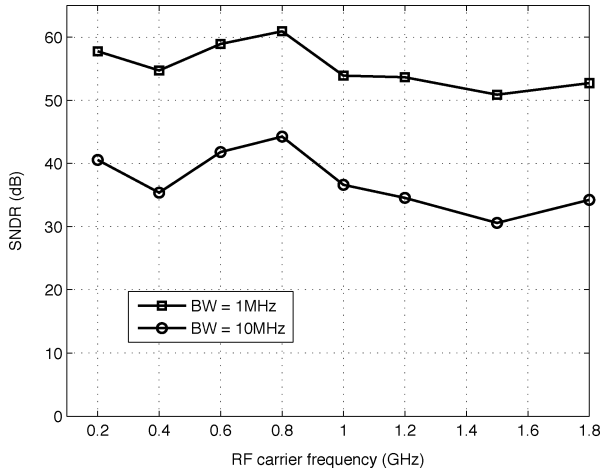


Fig. 22. SNR versus RF carrier frequency from 0.2 to 1.8 GHz.

TABLE I
PERFORMANCE SUMMARY

| | This work | [7]* | [9]* |
|---|---|---|---|
| Carrier frequency | 0.2-1.8GHz | 0.4-1.7GHz | 2.4GHz |
| Inband noise | -163dBm/Hz | -152dBm/Hz | -134dBm/Hz |
| IIP3 | -6.78dBm | +19dBm | +16.4dBm |
| IIP2 | +31.2dBm | +60dBm | +66dBm |
| S11 | $\leq$-8dB | N.A | N.A |
| Technology | 90nm CMOS | 90nm CMOS | 40nm CMOS |
| Supply voltage | 1.35V | 1.2V | 1.1V |
| Current | 31.1-36mA | 42mA | 11mA |
| Area | 0.4mm$^2$ | 0.8mm$^2$ | 0.07mm$^2$ |

* LNA is not included.

31.2 dBm. As the sampling frequency is changed from 800 MHz to 1.4 GHz, the current consumption of the ADC varies from 20.3 to 27.4 mA, where 9 mA of constant current is consumed in the VCO. The LNA dissipates 12 mA and the LO buffer dissipates 2.1 mA from a 1.35-V power supply.

## VII. CONCLUSION

In this paper, we present a 0.2–1.8-GHz digital-intensive receiver front-end using a VCO-based ADC running at 1.4 Gs/s in 90-nm CMOS. In order to achieve MMMB applications where a RF prefilter is absent, we propose a second-order anti-aliasing Sinc filter that can be embedded in the ADC, which exploits the integrating nature of a VCO. To alleviate the analog efforts in implementation, a triangular waveform is approximated to a staircase waveform and its effect is analyzed and verified. Non-ideal effect of the proposed architecture is analyzed with regard to the waveform imperfection due to device mismatch. The proposed receiver achieves $-94$ dBm of sensitivity at 1-MHz bandwidth and $-6.8$ dBm of IIP3, while providing 50-dB rejection of aliased signals. Since the overhead in implementing such a high-rejection Sinc$^2$ filter in the VCO-based ADC is a few transistors and a digital clock generator, the proposed receiver can be considered to be quite suitable for the future digital CMOS process.

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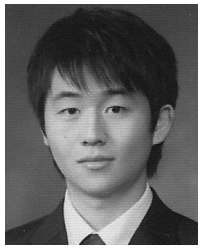


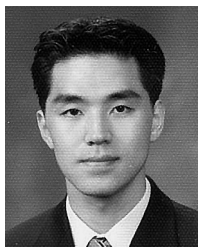
**Jaewook Kim** (A'06) received the B.S., M.S., and Ph.D. degrees in electrical engineering from the Korea Advanced Institute of Science and Technology, Daejon, Korea, in 2006, 2008, and 2011, respectively.

He is currently a Postdoctoral Associate with the Electrical Engineering and Computer Science Department, Massachusetts Institute of Technology, Cambridge. His research interests are time-based analog-to-digital converters, highly digitized RF receivers and DNA-protein circuits for systems and synthetic biology.

Dr. Kim was the corecipient of the 2009 IEEE Transactions on Circuits and System Society Guillemin–Cauer Best Paper Award.

**Wonsik Yu** (S'12) received the B.S. degree from Ajou University, Suwon, Korea, in 2010, and the M.S. degree from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea, in 2012, both in electrical engineering. He is currently working toward the Ph.D. degree in electrical engineering at KAIST.

His current research interests include time-based analog-to-digital converters, time-to-digital converters, and digital RF receivers



**SeongHwan Cho** (SM'10) received the B.S. degree in electrical engineering from the Korea Advanced Institute of Science and Technology, Daejon, Korea, in 1995, and the M.S. and Ph.D. degrees in from the Massachusetts Institute of Technology, Cambridge, in 1997 and 2002, respectively.

In 2002, he joined Engim, Inc., where he was involved in data converters and phased-locked loop (PLL) design for IEEE 802.11abg WLANs. Since November of 2004, he has been with the Department of Electrical Engineering, Korea Advanced Institute of Science and Technology (KAIST), Daejon, Korea, where he is currently an Associate Professor. His research interests include mixed-signal and analog circuits for low-power communication systems and bio/healthcare devices.

Prof. Cho was the corecipient of the 2009 IEEE Transactions on Circuits and System Society Guillemin–Cauer Best Paper Award. He serves on the Technical Program Committee on several IEEE conferences, including ISSCC, Symposium on VLSI, and A-SSCC. He has served as an associate editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS from 2010 to 2011 and guest editor of the IEEE JOURNAL OF SOLID-STATE CIRCUITS. He has twice received the Outstanding Lecturer Award from the Department of Electrical Engineering, KAIST.