A 3-GS/s 5-bit 36-mW Flash ADC in 65-nm CMOS

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***Abstract*— A 3-GS/s 5-bit flash ADC is fabricated for millimeter-wave communication systems in 65nm CMOS technology. The proposed foreground calibration method reduces the input-referred DC offset, achieving the resolution of 4.7 ENOB at 200MHz input frequency and keeping more than 4.3 ENOB even at Nyquist. The ADC consumes only 36.2mW including the power of the clock buffer and the resistor ladder from 1-V supply. The ADC has the FoM of 0.6pJ/conv at Nyquist.**

I. Introduction

In recent years, millimeter-wave broadband wireless systems have been developed by using deep-submicron CMOS process. In these systems, an ADC is required to achieve the sampling rate of multi GS/s and the resolution of 4-6 bits to digitize the wide baseband signal downconverted from RF signal with a few-GHz bandwidth. Flash archtecture is one of the most promising architectures for high speed and relatively low resolution.

In the finer CMOS process, the smaller transistor size facilitates the higher-speed operation of the ADC owing to the smaller parasitic capacitance. However, this increases the mismatch of the transistor, degrading the resolution of the ADC. Furthermore, since the available supply voltage becomes lower, the dynamic range of input analog signal becomes narrower, making the impact of the mismatch on the linearity more stringent. Therefore, it is a challenge to maintain the linearity of the high-speed ADCs in the finer process.

In this paper, a new foreground offset calibration is proposed for achieving the required linearity.

II. Architecture

Fig. 1 shows a main block diagram of this flash ADC. The ADC consists of track-and-hold circuits (T/Hs), a reference, 3-stage preamps, 2-stage comparators, an encoder and clock buffers. An input analog signal is sampled in the T/Hs. A low-power passive distributed configuration similar to [1] is employed in the T/Hs. The sampled signal is fed to the cascaded preamps. As shown in Fig. 1, the input signal is interpolated by a factor of 2 per stage in the preamps. The interpolation reduces the number of T/Hs by 9 and the number of the resistors in the reference by 8, saving the area and mitigating the error by timing skew between the T/Hs. In the ADC, the active interpolation by a 4-input preamp is employed to avoid interaction between the preamps. All the preamps have a reset switch connected between the differential outputs for fast recovery [2]. Fig. 2 shows the comparators in this ADC. The cascaded two dynamic comparators satisfy the operating speed of 3 GS/s with low power. The digitized signal by the comparators is passed through a quasi-gray encoder [3] and then converted into 5-bit binary.

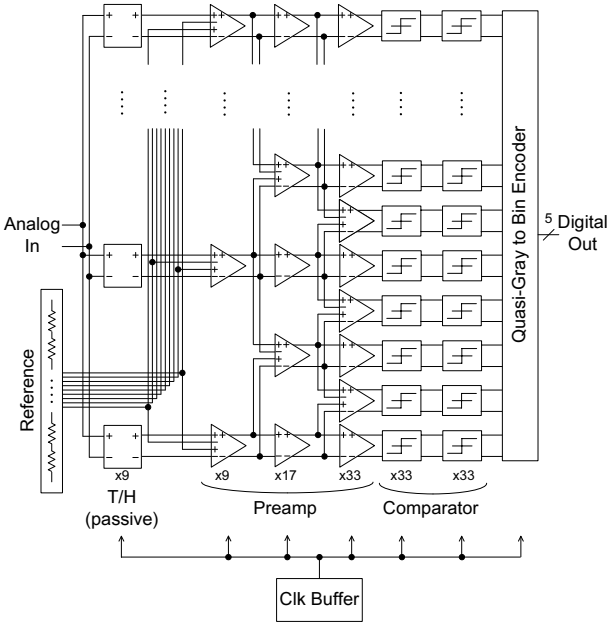

Fig. 1. Block Diagram of Flash ADC

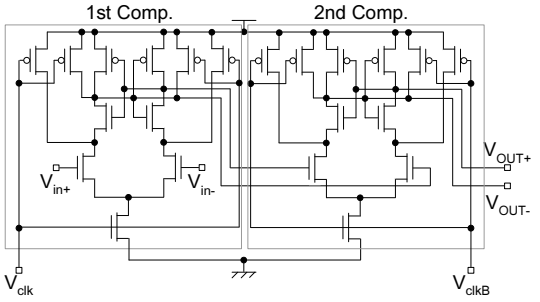

Fig. 2. Comparator

III. Conventional offset calibration

To ensure the linearity of a flash ADC with high yield, the input-referred offset originated in the preamps and the comparators should be suppressed within the standard deviation of

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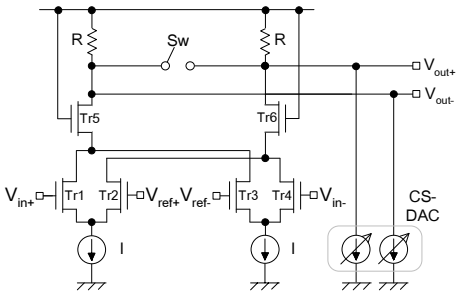

Fig. 3. 1st Preamp

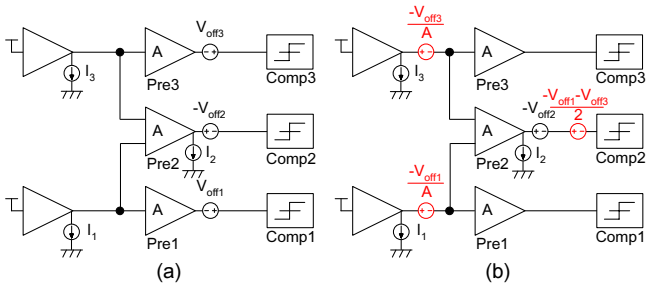

Fig. 4. Conventional Offset Cancellation Using CS-DACs

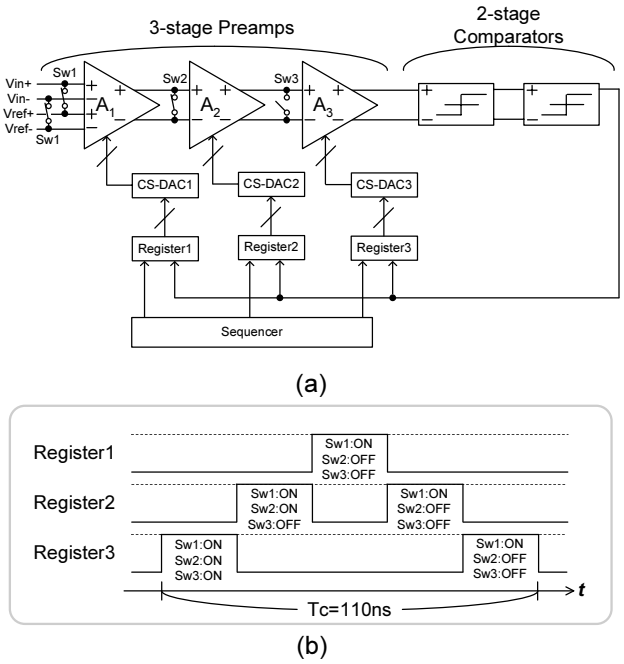

Fig. 5. Proposed Offset Calibration Scheme

0.1 LSB [4]. The calibration using current steering DAC (CS-DAC) is one of the effective methods to obtain the required linearity [1][5]. The current from the CS-DAC flows to a load resistance in the preamp and generates a trimming voltage. This generated trimming voltage cancels out the offset voltage. However, considering the gain in the 1st preamp is low and the interpolation technique may increase the offset voltage in the later preamps, it is inefficient for this ADC to adopt the conventional calibration scheme such as [1].

Fig. 3 shows the circuit diagram of the 1st preamp with two input differential pairs Tr1 to Tr4. Each differential pair in the 1st preamp receives one of input voltages $V_{in\pm}$ and one of reference voltages $V_{ref\pm}$. Because $V_{ref\pm}$ is fixed, only the half DC current I is used to amplify the input signal. Therefore, the transconductance to input signals in the 1st preamp is smaller than that of the preamp in the later stages. This lowers the voltage gain in the 1st preamp. Given the output parasitic capacitance of a few tens of fF, the load resistance in the preamps should be sufficiently reduced to obtain the wide bandwidth for operating the ADC at the high speed of 3 GS/s. Also, the addition of transistors Tr5 and Tr6 to surppress kickback noise narrows the available output signal range of the preamp to operate these transistors in the saturation region. For these reasons, it is difficult to lift up the voltage gain of the 1st preamp by increasing the DC current.

Fig. 4(a) illustrates the conventional calibration scheme such as [1]. For simplicity, single-ended and 2-stage preamps and comparators are shown in this figure. $Pre1$ to $Pre3$ are the preamps in the 2nd stage, V_{off1} to V_{off3} are the output-referred offset voltages at the outputs of them, A is their voltage gain of them, and $Comp1$ to $Comp3$ are the comparators connected to them. Ideally, if the conventional calibration is implemented, V_{off1} and V_{off3} are eliminated by $-V_{off1}/A$ and $-V_{off3}/A$ generated by trimming currents I_1 and I_3. In fact, the residual offset voltage remains in the output of the 1st preamp caused by the limited resoluton with the CS-DAC and by the current mismatch of the nonideal CS-DAC. Although total voltage gain of the 3-stage preamps is designed to be around 10 dB, the voltage gain in a 1st preamp is low and around 3 dB in this ADC. Owing to this low voltage gain with the 1st preamp, the input-referred residual offset voltage often exceeds 0.1 LSB.

In Fig. 4(a), there is no correlation between V_{off1} (or V_{off3}) referred at the output of 2-input preamp $Pre1$ (or $Pre3$) and $-V_{off2}$ referred at the output of 4-input preamp $Pre2$ in the same stage for interpolation. So, the calibration by I_1 and I_3 in the 1st stage may increase $-V_{off2}$ by $-(V_{off1}+V_{off3})/2$ as shown in Fig. 4(b). To calibrate this stacked offset voltage, the trimming current I_2 must be expanded. This lowers the input common-mode voltage of $Comp2$ connected to the output of $Pre2$. In Fig. 2, the inputs of the comparator are composed of NMOS transistors. Therefore, as the input common-mode voltage is lower, the transconductance of the comparator is smaller, slowing down its operation speed.

IV. Proposed Foreground DC Offset Calibration for High Resolution

To supress the input-referred residual offset voltage within 0.1 LSB, a new foreground calibration is proposed.

Fig. 5(a) shows the block diagram for the calibration. For simplicity, a series of the cascaded preamps and the comparators is illustrated in this figure. Each preamp has a

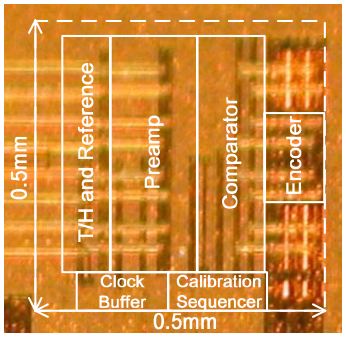

Fig. 6. Chip Photograph

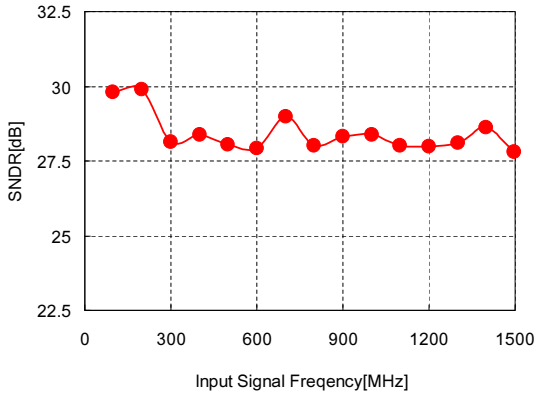

Fig. 7. SNDR versus Input Signal Frequency at 3 GS/s

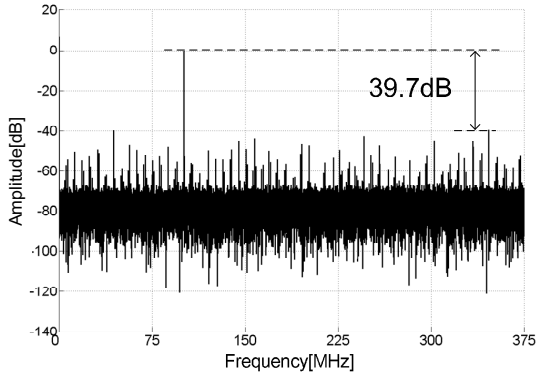

Fig. 8. Measured Spectrum of the ADC at 3 GS/s with 1399 MHz Input

CS-DAC and a register. The sequencer controls which switches and registers are operated.

Fig. 5(b) depicts the timing chart for the calibration. At the beginning, all the switches Sw1 to Sw3 are turned on. The input terminals of the 1st preamp are connected to the reference voltages and the differential inputs of the 2nd and 3rd preamp are set to zero. CS-DAC3 in the 3rd stage is operated by the sequencer, adjusting the offset due to the mismatch of the 3rd preamp and the comparators. Next, when Sw1 and Sw2 remain turned on and Sw3 is turned off, CS-DAC2 in the 2nd stage is operated. Only the offset voltage in the 2nd stage is compensated by CS-DAC2 because the offset voltages in the 3rd preamp and the comparator have already been corrected. After that, the calibration in the 1st preamp is executed in the same manner. By this calibration, the displacement of offset voltages from the 2-input preamps to 4-input preamp in the same stage is avoided.

In the next step, the residual offset voltages are replaced to the later stage. When Sw1 is switched on and Sw2 and Sw3 are off, CS-DAC2 is operated again. Both the output residual offset in the 1st preamp and the offset voltage in the 2nd preamp are corrected. After this step, the only remaining uncorrected residual offset voltage exists at the output in the 2nd preamp. Likewise, CS-DAC3 is operated at the end.

By executing the proposed calibration, the final residual offset voltage only stays in the output of the 3rd preamp. As a result, the input-referred offset voltage is diminished by total voltage gain with 3-stage preamps, suppressing it to within 0.1 LSB. This simple foreground calibration finishes in only 110 ns as shown in Fig. 5(b) and is much faster than conventional background calibration [1].

V. Measurement Results

Fig. 6 shows the chip photograph of this ADC. The test chip is fabricated in 65-nm 1-P 8-M CMOS technology and occupies the active area of 0.25 mm^2.

After calibration, the measured SNDR vs input signal frequency is shown in Fig. 7. The SNDR is 29.9 dB for 200-MHz input, corresponding to the effective number of bits (ENOB) of 4.7. The SNDR remains 27.8 dB with 1496-MHz input, respectively. It corresponds to the ENOB of 4.3. These results indicate that this ADC maintains the ENOB of over 4 and keeps the effective resolution bandwidth (ERBW) from DC to Nyquist.

Fig. 8 illustrates the FFT output spectrum for the input frequency of 1399 MHz at 3 GS/s when the output of the ADC is decimated by 4. The SFDR is 39.7 dB.

Fig 9 and Fig 10 show the DNL/INL after calibration. The measured DNL/INL is +0.36/-0.35 LSB and +0.41/-0.40 LSB.

At 3 GS/s, the total power of the ADC is only 36.2mW from the 1-V supply. The preamps, the comparators and encoder, the clock buffer and the reference ladder dissipate 13.2 mW, 10.7 mW, 11.7 mW and 0.6 mW, respectively.

In this ADC, the Figure of Merit (FoM) is 600 fJ/conv where the FoM is defined as

$$FoM = \frac{Power[J/conv]}{2^{ENOB@Nyquist} * Min(2 * ERBW, fs)}. \quad (1)$$

Table I compares the performances of the ADCs reported in recent years with the sampling rate around 3 GS/s. From this figure, it is obvious that this proposed ADC has an FoM below 1 pJ/conv and therefore is one of the best performances in the ADCs with several GS/s.

The performance of the chip is summarized in Table II.

VI. Conclusion

This paper presents the new foreground calibration method for Flash ADC. By executing the proposed calibration, the

TABLE I

PERFORMANCE COMPARISON OF ADCS OF AROUND 3-GHZ

	Deguchi [6] (JSSC'08)	Nakajima [1] (JSSC'10)	Alpman [7] (ISSCC'09)	Verbruggen [8] (ISSCC'10)	Park [9] (CICC'06)	Lin [10] (CICC'07)	Kijima [11] (CICC'09)	This work
Sampling Rate (GS/s)	3.5	2.7	2.5	2.2	3.5	3.2(4.2)	3	3
Supply (V)	0.9	1.0	1.1	1.1	1.8(1.4)	1.2	1.2	1.0
ENOB@Nyquist (bit)	4.9	5.3	5.4	4.9	3.6@1GHz	4.4(4.2)	5.3@500MHz	4.3
DNL (LSB)	+0.50/-0.48	0.50	±0.5	<0.8@1ch	+0.93/-0.83	0.60	±0.2	+0.36/-0.35
INL (LSB)	+0.96/-0.39	0.73	±0.8	<0.8@1ch	+0.88/-0.89	0.65	±0.2	+0.41/-0.40
ERBW (MHz)	1650	1350	1250	2000	-	1650(1750)	500	1500
Power (mV)	98	50(25)	50	2.6	227	180	90	36.2
FoM (pJ/conv)	0.95	0.47(0.25)	0.48	0.04	9.4@1GHz	2.51(2.80)	2.3	0.60
Technique	Averaging	Calibration	Calibration	Calibration	Calibration	Averaging	Calibration	Calibration
Technology(nm)	90	65	45	40	90	130	90	65

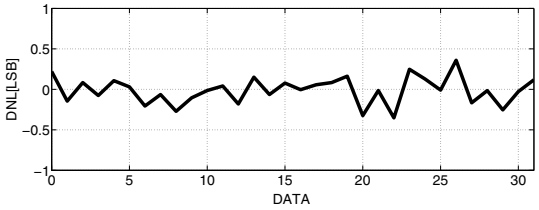

Fig. 9. DNL

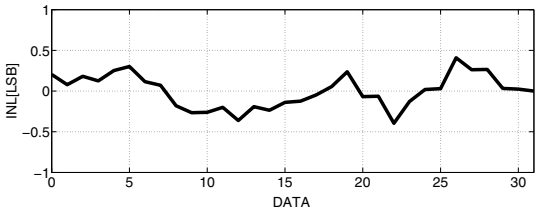

Fig. 10. INL

TABLE II

PERFORMANCE SUMMARY

Technology	65-nm 1-P 8-M CMOS
Supply Voltage	1 V
Full Scale	0.5 V_{p-p} (diff.)
Power	36.2 mW
Sampling Rate	3 GS/s
Resolution	5 bit
SFDR	43.1 dB @ 200 MHz input 39.6 dB @ 1496 MHz input
SNDR	29.9 dB @ 200 MHz input 27.8 dB @ 1496 MHz input
FoM	470 fJ/conv @ 200 MHz input 600 fJ/conv @ 1496 MHz input
DNL	+0.36/-0.35 LSB @ after calib.
INL	+0.41/-0.40 LSB @ after calib.
Area	0.25 mm^2 (0.5 mm × 0.5 mm)

input-referred DC offset is suppressed by total voltage gain with 3-stages preamplifiers, improving the resolution greatly.

The measurement results of the test chip verify that the fabricated ADC has the sufficient ENOB and ERBW required as a 3-GS/s 5-bit ADC from DC to Nyquist. The power consumption is only 36.2 mW at the 1-V supply voltage and the FoM with this ADC is comparable to those with the state-of-the-art ADCs.

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