Track and Hold for Giga-Sample ADC Applications using CMOS Technology

Marco Macedo, Gordon W. Roberts, Ishiang Shih
Integrated Systems Laboratory
McGill University
Montreal, Canada
marco.macedo@mail.mcgill.ca; gordon.roberts@mcgill.ca; ishiang.shih@mcgill.ca

***Abstract*—This paper presents a CMOS track and hold amplifier (THA) designed and fabricated in a 130 nm CMOS technology. It is intended for analog-to-digital converters (ADCs) used in radio receivers that sample in the Giga-Hertz region. At these data rates, it is extremely difficult for data converters to reach the desired performance levels using a single data path. Rather, ADCs operating in parallel at lower clock rates are becoming the norm. Such architectures require high-performance THAs capable of capturing the signal information at the desired sampling speed. Experimentally, this work will demonstrate a 2.5 GS/s THA capable of offering an SNR of almost 46 dB, SNDR of 42.4 dB and an ENOB of almost 7 bits.**

I. INTRODUCTION

The need for larger bandwidths in communication systems that supports higher data rates for consumer applications has virtually exploded in the last few years with the advent of smart phones and other technologies with multimedia capabilities. This drives the need for faster and higher resolution ADCs that can be integrated alongside other circuits in these high-speed communication devices. For integration reasons, it is preferable to construct these systems using CMOS processes as it is more economical and provides easier integration with other digital signal processing circuits.

The THA is the unit responsible for performing the continuous-time to discrete-time conversion in the ADC and provides a constant value to the ADC during the hold time so that the ADC can perform the conversion process. As a result, the THA is the main element of the front-end circuitry that establishes the performance limits of the ADC, such as speed, bandwidth, resolution and linearity.

This paper begins with an overview of the current track and holds topologies available for implementation in a CMOS process and outlines their advantages and disadvantages. In Section III, a fully differential THA design based on a switch source-follower is presented. This is followed by a discussion in Section IV on the non-idealities of the proposed THA. In Section V, the experimental results from an IC implementation in IBM 130nm CMOS process are provided..

II. SAMPLING CIRCUIT TOPOLOGIES

A. Passive CMOS THA

The simplest sampling topology for THA circuit is a passive topology consisting of a single MOSFET acting as a switch and a series capacitor to store the input voltage value [1]. Even though this structure looks very appealing from a realization point of view, it suffers from many drawbacks such as clock feed-through, charge injection and nonlinear on-resistance. Some techniques have been proposed to resolve these technical problems (e.g. clock boosting bootstrapping, switch dummies) [2]. Also, one important parameter of the THA that is difficult to achieve is the analog bandwidth requirement. In the context of a passive THA, the bandwidth of the circuit is dependent on only two parameters: on-resistance of the MOSFET switch and the series capacitor connected to it. Hence, the only way to increase the bandwidth of this topology is reduce the series on-resistance of the switch by increasing the width of the MOSFET and reducing its length. For example, in 130 nm CMOS process, the dimensions of the MOSFET switch will have to be 200 μm x 120 nm to provide an analog bandwidth of 1.25 GHz. However, this results in a significant capacitive load at the gate of the MOSFET switch, which in return reduces the clock edge rates to unacceptable levels.

B. Active CMOS THA (closed-loop and open-loop)

It is possible to implement a sampling topology with an active element, referred to as an active THA. The active element reduces the size of the switch and the load on the driver. An active THA can be implemented using an open or closed-loop topology. The closed-loop architecture makes use of high-gain Operational Transconductance Amplifiers (OTAs) and provides excellent linearity using relatively smaller sized MOSFETs. However at high sampling speeds, closed-loop architectures fail, as the OTA gain is reduced to very low levels and the benefits of the closed-loop operation are lost. Hence, the only suitable architecture for high-speed operation is an open-loop active THA, such as the differential switch source follower configuration shown in Fig. 1. It is

978-1-4673-0219-7/12/$31.00 ©2012 IEEE

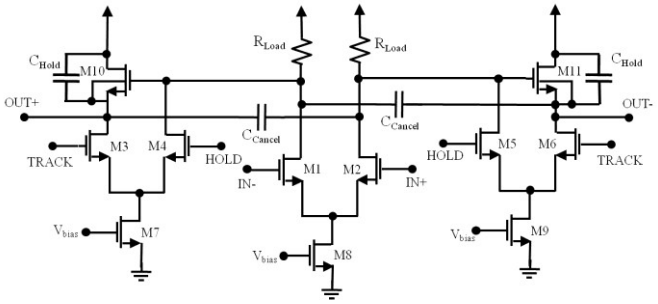

Fig. 1: Differential source-follower THA architecture.

interesting to note that this THA is a derivative from the popular diode sampling bridge found in many bipolar processes when Schottky diodes are available.

The differential THA circuit of Fig. 1 is composed of two main blocks: the analog input buffer (M_1, M_2 and M_8) and the two switched source-followers (M_3, M_4, M_7, M_{10} and M_5, M_6, M_9, M_{11}). This design employs a similar structure to what was presented in [3] except that in this design the use of inductors is eliminated. The inductors did not improve the bandwidth enough for this application to justify the added silicon area. Moreover, the elimination of the inductors allowed for a more compact layout; one that is less prone to mismatch effects.

The analog buffer has two main functions; one to restore any gain loss associated with the switched source-followers, and the other is to bias the subsequent switched source-follower stages for large dynamic range.

The two switched source-followers work in the following manner: During the tracking phase, i.e., when TRACK is high and HOLD is low, transistor M_3 is turned ON, M_4 is turned OFF and M_{10} is biased through M_3 such that it acts as a voltage buffer from its gate terminal to its source, forming the positive output of the THA. Similarly, M_6 is ON and M_5 is OFF and M_{11} acts as a source follower for the negative output of the THA. During the holding phase, i.e., when TRACK is low and HOLD is high, the two switched source-followers (M_{10} and M_{11}) are turned off and the state of the output voltage at the transition from track-to-hold is stored on the two storage capacitors C_{Hold}.

Finally, in order to reduce the hold-mode feed-through, two feed-forward capacitors C_{Cancel} are included. The charges on these two capacitors are of opposite sign to the charges on the gate-to-source capacitance of the two switched source-follower. Ideally, we should try to match this feed-forward capacitance to the gate-source capacitance of the source-follower. In practice, the hold-mode feed through cannot be completely eliminated because of device mismatches. Simulations were run multiple times with post layout circuit in order to select the best cancelation feed through capacitors (i.e., 120 fF).

III. Design Choices in IBM 130 nm Technology

The THA was designed for an IBM 130 nm CMOS process. This particular process technology offers several transistor options such as thick-oxide MOSFET with 3.3 V and 2.5 V supply voltages and a thin-oxide MOSFET with 1.2 V supply voltage. Keeping these components in mind, the first step in the design process was to determine how to maximize the input range while achieving an input bandwidth greater than 3 GHz. While a high-voltage MOSFET would enable a large input range to the THA, it does so at the expense of reduced bandwidth, as it requires a minimum transistor length of 500 nm. Spectre-RF simulations reveal that the THA could only reach a 3-dB bandwidth of 1 GHz in the best-case scenario. Since our target goal is a 3-dB bandwidth greater than 3 GHz, we are forced to use the low-voltage thin-oxide MOSFETs with smaller lengths of 120 nm, while accepting the limited input range that it causes.

Another important aspect of this design is the fact that the switched source-followers make use of NMOS triple-well MOSFETs. To maximize the output swing and reduce output distortion, the source and body terminals of this triple-well NMOS device are connected together so that its threshold voltage V_{TH} is minimized. This comes at the expense of a slower device, as an extra capacitance resulting from a parasitic reversed-biased diode connection is formed between the n-well bulk and substrate junction [4]. Nonetheless, the desired 3-dB bandwidth of 3 GHz is still met.

In order to test the chip and make measurements, an output buffer was added to the THA as shown in Fig. 2. The output buffer is designed to provide 50 ohms impedance matching to the external instrumentation.

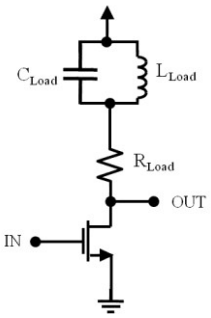

Fig. 2: Output buffer architecture.

IV. THA Non Idealities

There are six main sources of errors that degrade the performance of the THA: timing errors induced by clock jitter; hold-mode feed-through; settling time; pedestal error; droop rate, as well as offset errors due to the mismatches in the front-end buffer differential pair. While the last five sources of error are design dependent, and under the control of the THA designer in some manner, the errors caused by clock jitter must be eliminated through the application of clock cleaners, i.e., narrowband PLLs, and good routing of all clock signals.

A. Hold-Mode Feed-Through Errors

During the hold-mode, there is a portion of the input signal that appears at the output, as shown in the middle portion of Fig. 3. This is due to the fact that the switched source-followers have a parasitic capacitance path between the gate and the source ($C_{gs,10}$ and $C_{gs,11}$) during the off state [5]. The

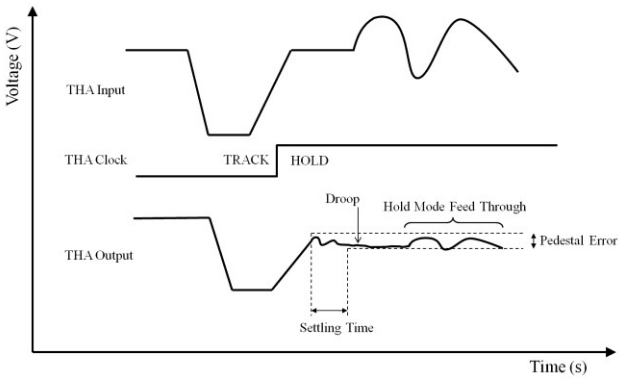

Fig. 3: Sources of THA errors.

addition of the cross-coupled capacitors label C_{Cancel} in Fig. 1 can help to reduce this effect. It is important to recognize that complete cancellation of the hold-mode feed-through is not possible because of device mismatches; it can only be minimized.

B. Settling Time and Pedestal Error

The settling time is the time it takes the output to settle to a constant level just after the track-to-hold transition. The pedestal error is the difference between the ideal output level and the output that results once the THA has settled down. Both these effects are illustrated in Fig. 3. The settling time error is due to the finite time it takes for differential pairs (M_3 and M_4) and (M_5 and M_6) to shut down the operation of the switched source-followers. The pedestal error is a result of the charge that is injected from the MOSFET forced in the off-state to the sampling capacitor. One possible way of reducing the settling time is to make use of wide devices in these differential pairs. However, larger devices lead to greater charge injection. Hence, there is a fundamental trade-off between the settling time and the accuracy of the charge transfer process associated with the THA.

C. Droop Rate

During hold-mode, the capacitor used to store the voltage starts to discharge or droop over time due to various MOSFET leakage effects (e.g., gate and substrate). The impact of this phenomenon can be observed from Fig. 3 towards the end of the holding phase.. The level of droop is a function of the amount of leakage and the size of the sampling capacitor. In order to minimize the droop rate, the design requires small-sized transistors in the switched source-followers, as well as a large sampling capacitor C_{Hold}. However, this reduces the settling time of the overall THA; therefore we are faced with a trade-off of speed versus accuracy.

D. Static Differential Mismatch Error

Any static mismatch in the differential signal path will result in second-harmonic distortion, unlike that which occurs in a passive THA. Adding some level of offset correction in the front-end differential pair can help to minimize this error.

V. EXPERIMENTAL RESULTS

For testing purposes, the bare die of the THA returned from fabrication was wired bonded directly onto a printed circuit board (PCB) made from Rogers RO4003C material and interfaced to various test equipment through SMA connectors and SMA coaxial cables. A die photograph of the THA fabricated in IBM 130 nm CMOS process is shown in Fig. 4. The THA occupies an active area of 200 μm x 240 μm. As the signal and clock generator available was single-ended, additional baluns manufactured by Mini-Circuits and TDK were added to the PCB to convert the single-ended signals to differential ones. The balun chosen for the analog input is model TC1-1-13MG2+ made by Mini-Circuits and the balun chosen for the clock input is the model HHM1517A made by TDK.

A wideband-matching network was designed for the analog input such that it provides good power transfer to the THA from the signal source in the frequency range between 500 MHz to 3.5 GHz. A 5th-order matching network was designed using the principles described in [4] and [6] and the resulting matching network is shown in Fig. 5. The matching network was built using surface mount components with a low ESL option manufactured by Murata.

To demonstrate the functionality of the THA, a sine wave at 500 MHz with a power level of -10 dBm was applied to the input of the balun connected to the THA. The continuous sine wave was sourced with an HP8647A signal generator. The THA was clocked with a Centellax TG1C1-A clock generator at 2.5 GHz. The output of the THA was observed on a LeCroy SDA6000 digital oscilloscope with a 20 GS/s sampling rate and is shown in Fig. 6. The tracking ability of the THA appears to be functioning correctly, as the general shape of the output signal is similar to a sine wave. The holding state of the THA is clearly present, although some settling, feed-through

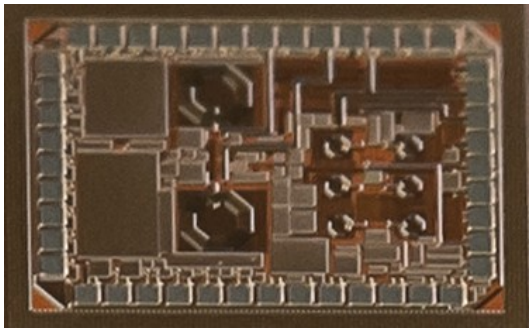

Fig. 4: Die photograph of the THA. Active area is 200 μm x 240 μm.

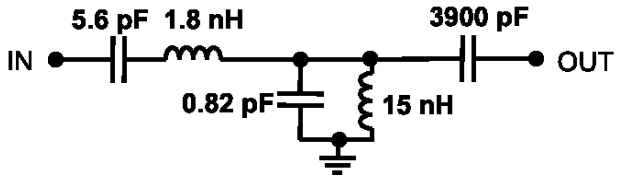

Fig. 5: A 5th-order wideband-matching network.

and droop is present. While one may be tempted to quantify these errors from the time-domain plot, it is important to note

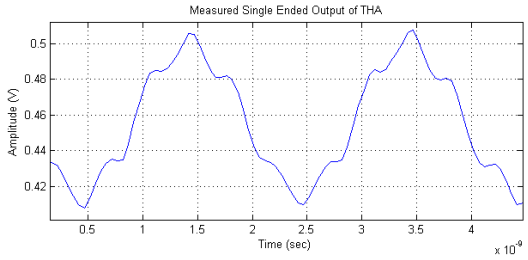

Fig. 6: Measured time-domain single-ended output for an input sine wave -10 dBm at 500 MHz (Oscilloscope sampling rate is 20 GS/s).

that the time-domain plot was obtained with a digital sampling scope and it contains quantization and reconstruction errors associated with digital sampling. In addition, large-sized high-speed inputs can also be affected by slew-rate limiting effects in the front-end stage of the oscilloscope. It is imperative that the performance of the THA be assessed with a spectrum analyzer.

Using an Agilent Technologies MXA N9020A spectrum analyzer, a frequency spectral plot corresponding to the THA output when its input is driven by a 500 MHz sine wave with a power level of -10 dBm and sampled at 2.5 GS/s is shown in Fig. 7. The output was measured single-ended on account of the equipment available, thus the spectral response contains greater levels of second-order distortion than that which would be measured with a fully differential spectrum analyzer.

Repeating the spectral test on the THA, the input power level was varied from -4 dBm to -20 dBm and the spectral response of the THA was collected and analyzed. Specifically, the peak SNDR was extracted to be 45.8 dB corresponding to an input power level of -10 dBm. Hence, this THA design can be used as part of the analog-to-digital conversion process with an effective number of bits (ENOB) of 6.8 taken single-ended, but the ENOB is expected to be at least 7.3 differentially.

TABLE I. SUMMARY OF THA CHARACTERISTICS

Process	IBM CMOS 130 nm
Supply Voltages	1.7 V (THA) and 1.2 V (Clock Buffer)
Analog Input Amplitude	0.285 Vpp (differential)
Clock Input Amplitude	0.3 Vpp (differential)
Sampling Rate	2.5 GS
Analog Bandwidth	>3 GHz
Peak SNDR at Fin = 500 MHz (up to 4th Harmonic)	42.4 dB
ENOB at Fin = 500 MHz	6.8 bits (single-ended) 7.3 bits (estimated differential)
Area for THA	200 um x 240 um
Chip Area	1.5 mm x 2 mm

VI. CONCLUSION

A 2.5 GS/sec THA capable of offering an SNDR of almost 46 dB, SNDR of 42.2 dB and ENOB of about 7 bits was designed and fabricated in 130 nm CMOS technology. The THA is a potential candidate for the front-end track and hold circuit needed in an ADC system intended for radio applications. The proposed THA does not rely on the use of inductors, thereby reducing its silicon footprint. The compact nature of this design is valuable for time-interleaved ADC integrated on a single die targeting radio application.

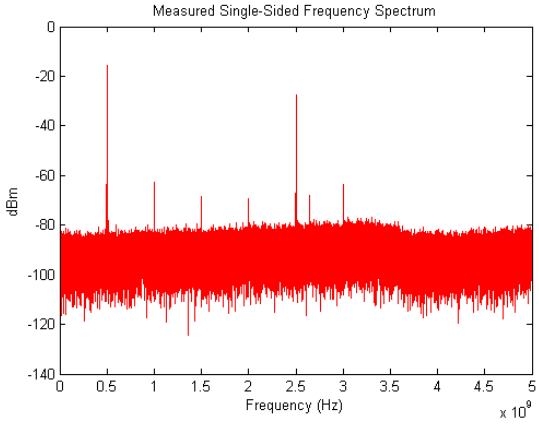

Fig. 7: Measured frequency spectrum for an input at 500 MHz with an input power level of -10 dBm corresponding to the peak SNDR situation. (Res BW = 100 kHz).

ACKNOWLEDGMENT

The authors would like to thank the Canadian Microelectronics Corporation (CMC) for providing chip fabrication.

REFERENCES

[1] Razavi, B.; , "Design of sample-and-hold amplifiers for high-speed low-voltage A/D converters," *Custom Integrated Circuits Conference, 1997., Proceedings of the IEEE 1997* , vol., no., pp.59-66, 5-8 May 1997

[2] Fayomi, C.J.B.; Roberts, G.W.; Sawan, M.; , "Low-voltage CMOS analog bootstrapped switch for sample-and-hold circuit: design and chip characterization," *Circuits and Systems, 2005. ISCAS 2005. IEEE International Symposium on* , vol., no., pp. 2200- 2203 Vol. 3, 23-26 May 2005

[3] Shahramian, S.; Voinigescu, S.P.; Carusone, A.C.; , "A 30-GS/sec Track and Hold Amplifier in 0.13-µm CMOS Technology," *Custom Integrated Circuits Conference, 2006. CICC '06. IEEE* , vol., no., pp.493-496, 10-13 Sept. 2006

[4] Bevilacqua, A.; Niknejad, A.M.; , "An ultrawideband CMOS low-noise amplifier for 3.1-10.6-GHz wireless receivers," *Solid-State Circuits, IEEE Journal of* , vol.39, no.12, pp. 2259- 2268, Dec. 2004

[5] R. van der Plassche, "Integrated Analog-to-Digital and Digital-to-Analog Converters", *Kluwer Academic Publisher*, 1994.

[6] Ismail, A.; Abidi, A.A.; , "A 3-10-GHz low-noise amplifier with wideband LC-ladder matching network," *Solid-State Circuits, IEEE Journal of* , vol.39, no.12, pp. 2269- 2277, Dec. 2004