A 0.47–1.6 mW 5-bit 0.5–1 GS/s Time-Interleaved SAR ADC for Low-Power UWB Radios

Pieter J. A. Harpe, Ben Büsze, Kathleen Philips, and Harmke de Groot

***Abstract*—This paper presents a 16-channel time-interleaved 5-bit asynchronous SAR ADC for UWB radios. It proposes 400 aF unit capacitors, offset calibration, a self-resetting comparator and a distributed clock divider to optimize the performance. The prototype in 90 nm CMOS occupies only 0.11 mm^2 including decoupling capacitors. Two relevant modes for UWB are supported: 0.5 GS/s at 0.75 V supply, and 1 GS/s at 1 V supply with 0.47 mW and 1.6 mW power consumption respectively. With an ENOB of 4.7 and 4.8 bits, this leads to energy efficiencies of 36 and 57 fJ/conversion-step. Compared to prior-art, state-of-the-art efficiency is achieved without relying on complex calibration schemes.**

***Index Terms*—ADC, analog-to-digital conversion, CMOS, successive approximation, time-interleaving.**

I. Introduction

WIRELESS communication standards using Impulse Radio UWB, like 802.15.4a WPAN or 802.15.6 WBAN, require low-resolution (3 to 6 bits), high-speed ADCs [1], [2]. Because of the high speed of operation, flash-based converters are often selected for this application [3], but alternatives based on pipelining [4] or SAR [5] are also being developed. Within this application range, a disadvantage of current state-of-the-art designs is that they strongly rely on calibration techniques to compensate for, e.g., comparator offsets, non-linearities and timing inaccuracies in order to achieve their performance. For example, [4] uses an external reference generator and requires 288 calibration steps, while [5] requires external generators and analyzers to characterize INL, THD, SNDR, offset, gain and time skew in order to calibrate the converter. Due to the complexity of the applied calibration schemes, an on-chip implementation is not straightforward. In order to overcome this problem, the goal of this work is to realize a highly power-efficient ADC for UWB radios, while minimizing calibration complexity to make an on-chip implementation feasible. Thus, a 16-channel time-interleaved SAR ADC is presented that only requires a simple calibration of the channel-offset, which can be integrated on-chip easily. Other error sources (such as time-skew errors) are minimized by intrinsic design rather than calibration.

While a sampling rate of 0.5 GS/s is sufficient for 802.15.4a UWB receiver architectures [2], ranging and localization applications benefit from higher sampling rates to achieve a better accuracy [6]. Therefore, the presented 5-bit ADC supports two relevant modes of operation: a 0.5 GS/s mode for communication applications, and a 1 GS/s mode for ranging applications. The proposed design uses 16 channels, each operating at 31.25 MS/s or 62.5 MS/s, which is a good compromise between chip-area and channel-speed.

Section II describes the design of a single 5-bit SAR converter, while Section III describes the design of the 16× time-interleaved array. Measurement results are shown in Section IV and conclusions are given in Section V.

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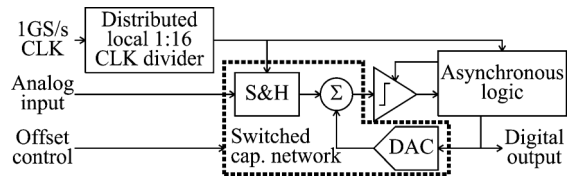

Fig. 1. One channel of the time-interleaved ADC: asynchronous SAR architecture with distributed clock divider.

II. Single Channel: Asynchronous SAR ADC

Fig. 1 shows a single channel of the 16× time-interleaved ADC. For an overall sample rate equal to f_s, each channel only needs a clock at $1/16 \times f_s$ because of the asynchronous architecture [7]. 0.5 GS/s and 1 GS/s modes are simply supported by adjusting the single external clock. While a 1 V supply is used at 1 GS/s, the supply can be reduced at 0.5 GS/s because of the relaxed speed requirements. As shown later, a 0.75 V supply is sufficient for the 0.5 GS/s mode. Since the complete design is based on dynamic circuitry, the power consumption is proportional to $f_s \mathrm{VDD}^2$, thus achieving a $0.5 \cdot 0.75^2 = 0.28\times$ power reduction at 0.5 GS/s when compared to the 1 GS/s mode. For simplicity of explanation, the remainder of this paragraph assumes that a 1 V supply is used. In case of a reduced supply, all voltage levels (e.g., LSB value, full-scale range) would be scaled proportional to the supply.

Apart from the typical blocks of a SAR converter, this design also includes a part of the clock divider and an offset correction mechanism, both of which are required to support the time-interleaved architecture.

A. Switched-Capacitor Network

The analog part is implemented by a switched-capacitor network (Fig. 2). The array of capacitors provides several functions, namely: sampling of the analog input signal (on the complete array), 5-bit DA conversion (capacitors $C_{d4\ldots0}$), attenuation of the signal range (capacitor C_a), a common-mode shift (capacitor C_b), and analog offset correction (capacitors $C_{b3\ldots0}$).

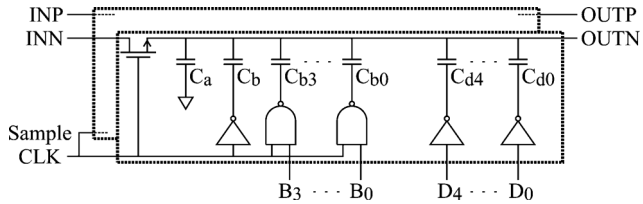

Fig. 2. Switched capacitor core of the ADC, including analog offset correction.

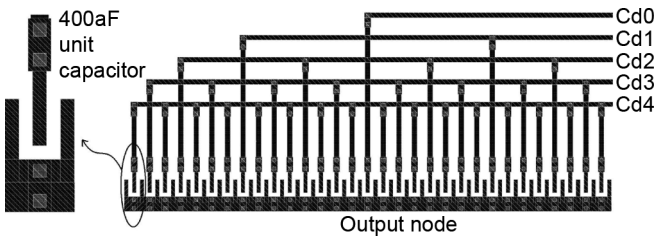

Fig. 3. Layout of the 400 aF unit capacitor and partial layout of the capacitor array.

TABLE I
EXTRACTED VALUES OF THE CAPACITORS

Capacitor	Value (fF)	Value (LSB)
C_{d4}	6.296	16
C_{d3}	3.148	8
C_{d2}	1.574	4
C_{d1}	0.787	2
C_{d0}	0.394	1
C_{b3}	3.147	8
C_{b2}	1.575	4
C_{b1}	0.788	2
C_{b0}	0.394	1
C_b	19.21	
C_a	24.87	
C_s (total)	62.18	

To optimize the efficiency for this low resolution ADC, in which noise and matching requirements are relaxed, the values of the capacitors need to be minimized. Thus, this work uses dedicated lateral metal-metal capacitors of 400 aF (Fig. 3) to compose the various capacitors in the array. In this way, a total equivalent sampling capacitance C_s of only 62 fF is achieved. Fig. 3 also shows a part of the layout of the capacitor array, revealing the common-centroid approach used for the binary-scaled DAC elements. Independently, a similar layout technique has been mentioned in [8]. Since the proposed capacitors are based on layout parasitics, the actual values are verified by RC-extraction. Table I gives an overview of the extracted values.

Using the proposed 0.4 fF capacitor elements, the 5-bit binary-scaled DAC ($C_{d4\ldots0}$) yields a total DAC capacitance C_{dac} of $31 \cdot 0.4 = 12.4$ fF. Since the DAC capacitors are switching between GND and VDD, a differential signal range of 2VDD is theoretically achieved. However, since the DAC is based on charge-redistribution, it is loaded by the overall capacitor array, and thus the effective value of the LSB is given by

$$V_{\mathrm{LSB}} = 2\frac{C_{d0}}{C_s}\mathrm{VDD}, \tag{1}$$

where the factor of two arises from the differential operation. Thus, the differential peak-to-peak range of this 5-bit ADC becomes

$$V_{\mathrm{fs,\ pp}} = 32V_{\mathrm{LSB}} = 64\frac{C_{d0}}{C_s}\mathrm{VDD}. \tag{2}$$

For a practical signal range of 0.4 V at 1 V supply (suitable to e.g., [9]), and given $C_{d0} = 0.4$ fF, this implies C_s needs to be around 62 fF. For that reason, attenuation capacitor C_a is included: after dimensioning the other capacitors, C_a is added to achieve an overall C_s of 62 fF.

Externally, a low common-mode voltage of 0.2 V is used to allow the use of a single NMOS device of $1.5\ \mu\mathrm{m}/0.1\ \mu\mathrm{m}$ as sampling switch. The simple structure of the switch and the small dimensions enable a lower complexity and lower power consumption in the clock circuitry. However, since the comparator in this ADC is not designed to operate at such a low common-mode level, a common-mode shift is required after sampling. This is implemented by capacitor C_b (19.2 fF), which shifts the common-mode level after sampling by an amount of

$$V_{\mathrm{CM,\ shift}} = \frac{C_b}{C_s}\mathrm{VDD} \tag{3}$$

which equals $19.2/62 \cdot 1 = 0.3$ V, thus reaching a common-mode level of 0.5 V.

Since offset-mismatch between the channels in a time-interleaved converter results in spurious tones, an offset calibration technique is used in this design. For that reason, an analog offset correction method is implemented by the array of binary-scaled capacitors C_{b3} (3.2 fF) to C_{b0} (0.4 fF). These capacitors can be programmed digitally through bits $B_{3\ldots0}$. Note that when B_i is low, the output of the associated NAND-gate is fixed to a high-level, and thus the corresponding capacitor C_{bi} is never activated. When B_i is high, the NAND-gate inverts the CLK signal, and thus C_{bi} is driven by the same signal as C_b. In this way, the activated part of $C_{b3\ldots0}$ adds up to the common-mode shift. However, since each half of the differential structure can be programmed separately, it can actually add an offset to the sampled signal. The added offset is given by

$$V_{\mathrm{offset}} = \sum_{i=0}^{3}\frac{B_i C_{bi}}{C_s}\mathrm{VDD}\ \text{with}\ B_i \in \{0,1\}. \tag{4}$$

With the given capacitor values, this leads to a programmable offset correction in the range of ± 7.5 LSB with 0.5 LSB steps. Since the quantization step of the offset correction equals 0.5 LSB, the post-calibration offset is ideally distributed within ± 0.25 LSB.

B. Self-Resetting Comparator

The dynamic comparator (Fig. 4) is implemented similar as in [7], [10], but optimized for a higher speed and a lower accuracy.

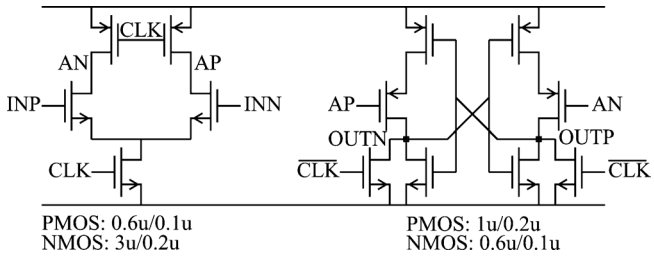

Fig. 4. Dynamic comparator.

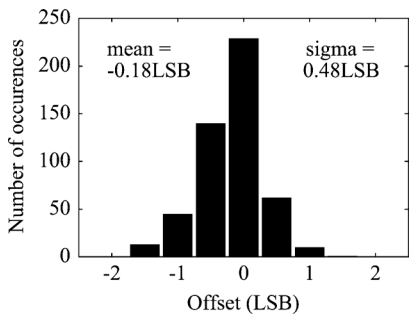

Fig. 5. Simulated comparator offset (500 Monte-Carlo runs).

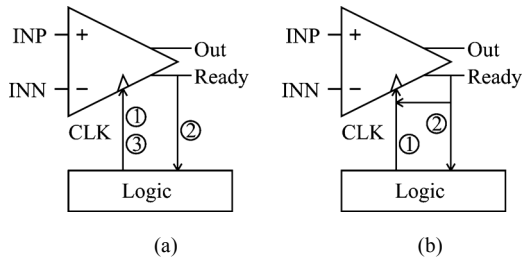

Fig. 6. Comparator control (a) without and (b) with self-reset.

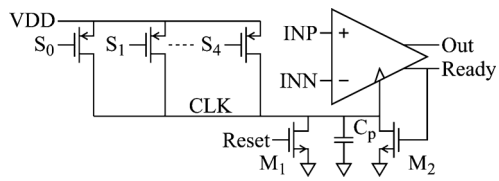

Fig. 7. Dynamic control logic and self-reset for the comparator.

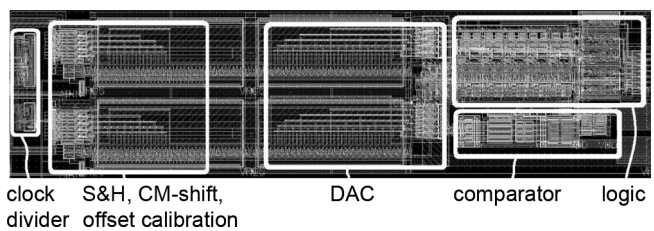

Fig. 8. Layout view of a single channel of the ADC, occupying 96×24 μm.

Since the offset performance of the comparator is important for the time-interleaved ADC, the offset is simulated with Monte-Carlo simulations. As shown in Fig. 5, an offset with $\sigma = 0.48$ LSB is achieved. Since 4σ is well within the offset correction range of ± 7.5 LSB, the comparator offset can be effectively calibrated down to the calibration granularity.

To minimize the power consumption of the digital logic and to prevent the need for an oversampled clock, the logic in this ADC is implemented with asynchronous dynamic logic, which has been described in detail in [7]. However, while [7] uses mostly dynamic logic, the comparator control logic is still implemented with standard CMOS logic. In this work, the comparator control is also implemented with dynamic logic. Moreover, to slightly increase the speed of operation, a self-resetting loop is created around the comparator to reduce the reset-time: Fig. 6 shows the difference between the original approach and the proposed self-resetting scheme. In the original case, the logic would request a comparison by enabling the clock to the comparator first (1). Then, as soon as the comparator is ready, this will be indicated by a *Ready* flag from the comparator to the logic (2). At that moment, the logic will proceed by disabling the comparator clock (3). In this approach, phase (3) is unnecessarily delayed after phase (2), due to the gate-delay introduced by the logic. For high-speed operation, it is beneficial to minimize this delay. This is done by the self-resetting scheme which shortens the loop to reset the clock as shown in Fig. 6: the *Ready*-flag is now used to reset the clock immediately instead of passing through the state-machine of the main logic.

The detailed implementation of the comparator control logic is shown in Fig. 7. First, before the conversion takes place, a *Reset* discharges the parasitic capacitance C_p through transistor M_1, thus disabling the comparator clock (*CLK*). Then, during the 5-bit conversion process, the logic will request a total of five comparisons. Each comparison is requested by a low level on one of the five inputs S_i (one for each bit cycle). When one of these inputs is low, one of the PMOS devices will be enabled, which charges C_p and creates a high level on *CLK*, thereby initiating a comparison. Compared to complementary logic (requiring several layers of CMOS gates to generate *CLK* from the five inputs S_i), the proposed dynamic PMOS logic reduces the delay and the power consumption. Furthermore, the self-reset can be implemented simply by a single transistor M_2: as soon as the comparator is finished, the *Ready* output will go high, thereby enabling transistor M_2, which discharges C_p and thus disables the comparator.

C. Layout

To minimize power loss due to layout parasitics and to facilitate integration into a time-interleaved system, a small form-factor layout is necessary. Fig. 8 shows the layout of a single channel including clock-divider. The small area of only 96×24 μm in 90 nm CMOS can be achieved because of the small-area capacitors, the dynamic logic (which reduces the number of transistors), by putting the supply decoupling capacitors below the signal capacitors and by careful layout.

III. 16-Channel Time-Interleaved ADC

Time-interleaved converter arrays are widely used to increase the speed of operation while maintaining power-efficiency [5],

[11]. However, channel mismatches result in undesirable spurious components. Thus, either sufficient matching needs to be achieved by intrinsic design or otherwise calibration or correction techniques are required to compensate for these errors. The three main types of mismatch are: offset mismatch, gain mismatch and time-skew, as analyzed in a.o. [11]. Gain mismatch can be neglected in this time-interleaved SAR architecture, as the gain is determined by precise capacitor ratios. On the other hand, the offset mismatch and time-skew need to be taken into account, and are therefore discussed in the following sections.

A. Offset Mismatch and Calibration

Each individual ADC in a time-interleaved array might have a different input-referred offset, resulting in offset mismatch between the channels. In the proposed SAR ADC from Section II, the offset is dominated by the random offset of the comparator, which has been simulated to have a standard deviation σ_{offset} of 0.48 LSB. As described in [11], a random channel-offset with a standard deviation of σ_{offset} for each channel leads to spurious tones with a total power of

$$P_{\text{offset}} = \sigma_{\text{offset}}^2. \tag{5}$$

To prevent substantial degradation of the ENOB due to offset mismatch, P_{offset} should remain small compared to the quantization noise power. As the latter one is given by

$$P_q = \frac{1}{12}\text{LSB}^2, \tag{6}$$

this implies that the offset matching should be better than

$$P_{\text{offset}} \ll P_q \Rightarrow \sigma_{\text{offset}} \ll 0.289\text{LSB}. \tag{7}$$

Since the intrinsic design achieves a σ_{offset} of 0.48 LSB, offset calibration is required to fulfill (7). The proposed offset calibration scheme is composed of a digital measurement algorithm and an analog correction technique. The measurement is performed off-chip at start-up. Since it is a start-up method, it does not affect the power consumption during normal operation. The correction is performed on-chip in the analog domain (as described in Section II) since it leads to a low power consumption.

The post-calibration offset performance is determined by two parameters: the accuracy of the offset measurement and the accuracy of the offset correction. First, the analog offset correction as described in Section II is considered. Since the implemented method has a step size of 0.5 LSB, truncation errors within ± 0.25 LSB can be expected. Assuming a normal distribution within this range, the post-calibration offset performance is ideally characterized by

$$\sigma_{\text{offset, post, ideal}} = \sqrt{\frac{1}{12}\left(\frac{1}{2}\text{LSB}\right)^2} = 0.144\text{LSB}, \tag{8}$$

showing that the matching requirement (7) can be achieved.

Next, the performance of the offset measurement needs to be validated. To avoid additional power consumption during normal operation, a start-up calibration technique is used. A straightforward method to measure channel-offset is to short the analog input (i.e., apply a zero input), and to determine the digital output code. For each channel, the output code corresponds to the digitized offset, and can be used to determine the required correction value. Since a zero input can be provided easily on-chip, while no additional signal sources or analyzers are needed for this method, it can be implemented in a straightforward manner. However, due to the quantization process of the ADC, the measured offset has an inaccuracy equal to the quantization error of the ADC (6), which thus limits the post-calibration performance to $\sigma_{\text{offset}} = 0.289$ LSB.

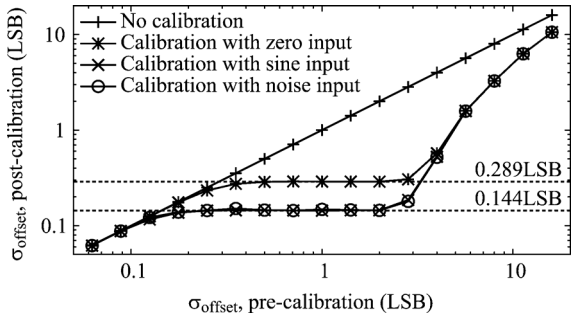

Fig. 9. Offset calibration performance for various test signals, using 10000 Monte Carlo simulations.

The offset measurement precision can be improved by randomizing the quantization errors and applying averaging. For example, the quantization errors can be randomized by applying an AC-tone or white noise at the input of the ADC. In both cases, the applied signal needs to have a sufficient magnitude to be able to decorrelate the quantization errors, while sufficient averaging is needed to reduce the total noise below the accuracy target. Before investigating these properties, a first set of simulations is used to confirm the performance of the three measurement methods: zero input, sine input and noise input. Fig. 9 shows the achieved post-calibration performance as a function of the pre-calibration performance for each of these methods, using Monte Carlo simulations on a high-level ADC model. The model assumes an ideal 5-bit quantizer with a random input-referred offset and an offset correction with $\pm 7.5\text{LSB}$ range and 0.5 LSB steps. For this test, the number of points for averaging is fixed to 2048. The sine-tone is set at $-\text{dBFS}$ to achieve sufficient randomization of the quantization errors while preventing saturation, and the noise input is set to $\sigma_{\text{noise}} = 0.5\text{LSB}$. Several conclusions can be drawn from Fig. 9: first, when the intrinsic σ_{offset} is already better than the calibration accuracy or when it is beyond the calibration range, the post-calibration performance will approach the pre-calibration performance, as the calibration is not effective in these cases. Second, within the effective range, the zero input case achieves a constant post-calibration performance around $\sigma_{\text{offset}} = 0.289$ LSB, as predicted before. At the same time, the sine and noise inputs achieve a post-calibration performance around $\sigma_{\text{offset}} = 0.144$ LSB, corresponding to the limit given in (8). This is understandable since the large amount of averaging (2048 samples) suppresses the quantization errors sufficiently in the measurement phase. In more detail, the performance as a function of the signal strength and the amount of averaging is investigated for the noise input

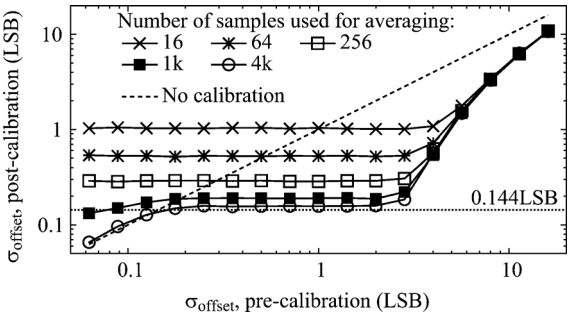

Fig. 10. Offset calibration performance for various amounts of averaging, using 10,000 Monte Carlo simulations.

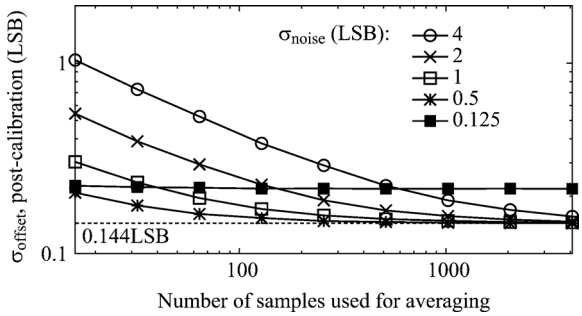

Fig. 11. Offset calibration performance versus amount of averaging for various amounts of noise, using 10,000 Monte Carlo simulations.

case. Considering the amount of noise applied to the input of the ADC is given by σ_{noise}. Under the assumption that

$$\sigma_{\mathrm{noise}}^2 \gg P_q, \tag{9}$$

the quantization errors will be decorrelated. At the same time, since σ_{noise} is assumed to be dominant over the quantization error, the measurement inaccuracy for a single observed output sample can be approximated by σ_{noise}. Then, assuming k samples are averaged to determine the channel offset, the measurement inaccuracy $\sigma_{\mathrm{measurement}}$ is given by

$$\sigma_{\mathrm{measurement}} = \frac{\sigma_{\mathrm{noise}}}{\sqrt{k}}. \tag{10}$$

To be able to approximate the best possible calibration performance (8), the measurement inaccuracy $\sigma_{\mathrm{measurement}}$ needs to be negligible compared to the correction accuracy (0.144 LSB), thus:

$$\sigma_{\mathrm{measurement}} \ll 0.144\mathrm{LSB} \Rightarrow k \gg 48\sigma_{\mathrm{noise}}^2. \tag{11}$$

Using Monte Carlo simulations, the effect of averaging is shown in Fig. 10 for $\sigma_{\mathrm{noise}} = 4$ LSB. For small numbers of averaging, the performance is indeed limited by the measurement accuracy (10), e.g., for $k = 16$, (10) predicts $\sigma_{\mathrm{offset}} = 1$ LSB after calibration, which is confirmed by the simulation. Also, corresponding to (11), the post-calibration performance approaches 0.144 LSB when $k \gg 768$. Fig. 11 shows the Monte Carlo simulation results for various levels of noise and various amounts of averaging for a fixed pre-calibration σ_{offset} of 1 LSB. It can be seen that as long as the requirements for noise-level (9) and number of averaged samples (11) are fulfilled, the post-calibration performance will approximate the limit of 0.144 LSB. In case the noise-level is too small to allow decorrelation of the quantization errors, the performance approximates 0.289 LSB regardless of k, corresponding to the zero input case.

Having investigated the effects of offset mismatch and the requirements in terms of correction and measurement precision, the overall offset calibration procedure can be summarized as follows: first, at start-up, the offset for each channel is determined. Considering this ADC is used in a wireless receiver, the noise generated by the preceding block (e.g., VGA) can be used to improve the measurement precision. As the input-referred noise of the total system is typically dominated by the earlier stages, requirement (9) can be fulfilled easily. After the measurement phase, the correction values can be calculated at once and loaded into the calibration register that controls the programmable capacitors $C_{b3\cdots0}$. After that, no additional processing is required as the correction is performed in the analog domain. Since the proposed calibration method does not require specific signal sources or analyzers, it can be implemented on-chip easily.

The calibration time at start-up is dominated by the measurement time. Assuming a realistic case where $\sigma_{\mathrm{noise}} = 1$ LSB, the number of averaged samples should be at least 48 according to (11). Taking (with some margin) for example 128 samples and noting that there are 16 channels to be measured, the total measurement time at a sample rate of 500 MS/s becomes $16 \cdot 128/500 \cdot 10^6 = 4.1$ μs. The power consumption of the measurement logic is dominated by the accumulator, required for averaging. Assuming 128 5-bit samples to be averaged, 12-bit accumulators are required. While not implemented in this chip, a simulated schematic-level 12-bit accumulator consumes 0.25 pJ per operation, thus leading to a total energy consumption of 0.5 nJ for averaging 128 samples for each of the 16 channels. This indicates that the power consumption for the measurement method will be small, and moreover, it only occurs temporarily at start-up.

B. Time-Skew Mismatch

Next to offset mismatch, time-skew mismatch can reduce the performance of a time-interleaved ADC. As analyzed in [11], the error power due to random time-skew for each channel can be approximated by

$$P_t = \frac{(A2\pi f_{\mathrm{in}}\sigma_t)^2}{2} \tag{12}$$

where A is the amplitude and f_{in} the frequency of the input signal, and σ_t is the standard deviation of the time-skew. For an N-bit Nyquist-rate converter, the maximum amplitude equals $A = 2^{N-1}$ LSB, while the maximum input frequency is given by $f_{\mathrm{in}} = 1/2f_s$, with f_s the sample rate of the time-interleaved ADC. Under these assumptions, and requiring the error power due to time-skew to be small compared to the quantization noise, the following requirement for time-skew can be derived:

$$P_t \ll P_q \Rightarrow \sigma_t \ll \frac{2}{\pi\sqrt{6}} \cdot \frac{1}{2^N f_s}. \tag{13}$$

For the 5-bit 1-GS/s ADC considered in this work, this yields

$$\sigma_t \ll 8.1 \text{ ps}. \tag{14}$$

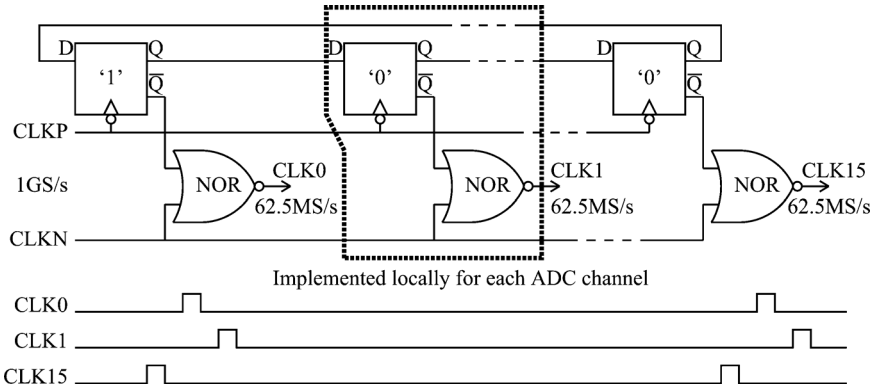

Fig. 12. Distributed local clock divider and generated non-overlapping output clocks.

Instead of applying calibration techniques to achieve the required timing accuracy, a design approach is proposed that has sufficient intrinsic performance. The following section discusses the design and implementation of the clock divider and the global signal connections, which are key to achieving sufficient timing accuracy.

C. Clock Divider and Global Signal Distribution

The clock divider in Fig. 12 uses a ring of 16 flip-flops clocked at 1 GS/s, one of which is preloaded with '1', while the others are preloaded with '0'. In this way, 16 62.5-MS/s clock phases are generated; one for each channel of the time-interleaved ADC. NOR-gates are added to post-synchronize the generated clocks by the original 1 GS/s input clock (CLKN) and to generate non-overlapping clocks. Note that these NOR-gates drive the NMOS sampling switches directly (Fig. 1). Since the actual sampling takes place on the falling edge which is triggered by the rising edge of CLKN, only the NOR-gates contribute to time-skew, while the flip-flops have no influence.

With this implementation composed of 16 flip-flops and 16 NOR-gates, a single flip-flop and NOR gate can be implemented locally for each channel (see Fig. 8), instead of using a single global clock divider. In that way, only the 1 GS/s clock needs to be distributed to the various channels, instead of distributing 16 different 62.5 MS/s clocks.

Time-skew errors can be classified in two categories: random and systematic errors. The first type originates from random mismatch of the components in the clock divider and the sampling network, while systematic errors can be caused by the layout topology. Considering random variations, a Monte Carlo simulation on the clock buffer and sampling structure was carried out, resulting in an expected time-skew with a standard-deviation σ_t equal to 1.0 ps.

For the systematic time-skew performance, the layout of the time-interleaved array has to be considered: systematic irregularities in the global clock and signal paths can cause systematic time-skew for the different ADC channels. For that reason, the global clock and signal paths in a time-interleaved ADC are usually designed for equal delay (e.g., a tree structure as in Fig. 13(a)). However, since four signals (differential clock and differential signal) need to be implemented precisely, this results in a complex layout and increased wiring length and chip area, especially in case of highly-interleaved ADCs. To alleviate these problems, a *matched-delay* approach is used to minimize time-skew instead. The layout sketch in Fig. 13(b) shows the distribution of the clock and input signal to the 16 channels: the channels are placed in a single column, while the global connections are implemented with straight vertical wires. The time-skew between the channels is minimized by matching the clock-delay and signal-delay for each channel: e.g., the analog input signal for channel I will be delayed by Δ_a as compared to channel A. At the same time, the clock for channel I is delayed with an amount Δ_c. By matching the signal and clock delays, they can cancel out each other, effectively suppressing the systematic time-skew.

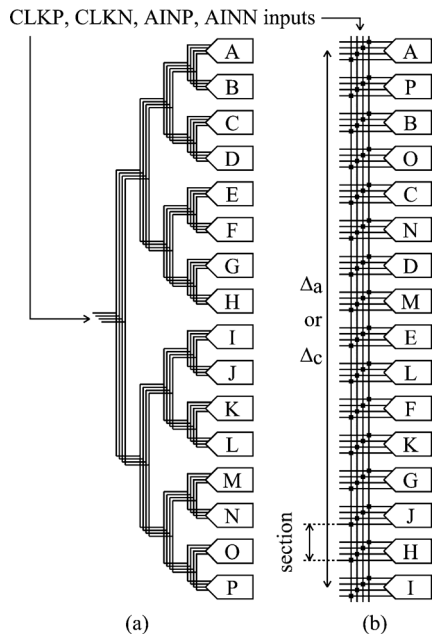

Fig. 13. Layout diagram for clock and signal distribution: (a) tree structure and (b) proposed matched-delay layout.

To analyze the systematic time-skew, the delay of the global signal connections is modeled. First, the global clock connection is considered as shown in Fig. 14. The model is composed of p sections, where p is equal to the number of channels in the time-interleaved array. For clarity, a single section of the global wiring is indicated in Fig. 13. Each section (composed of R_0 and C_0) models the parasitic resistance and capacitance

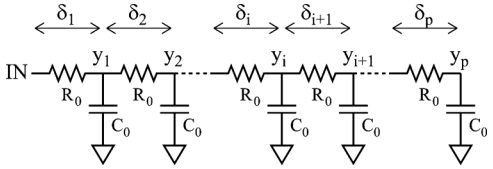

Fig. 14. Model of the systematic channel-dependent delay due to the layout.

of a section of the global wire. Moreover, the input capacitance to the clock buffer inside each channel can be included in C_0 as well. The outputs from the global wire to the p channels are indicated by y_1 up to y_p, while the delay from one section to the next is denoted by δ_i for each section i. Since the global wire needs to have a bandwidth beyond the frequencies of interest, it can be assumed that $R_0 \ll 1/2\pi f C_0$. Thus, the delay δ_i for each section can be expressed as RC, where R is equal to the resistance from the input to the output of one section (R_0), and C is the load capacitance at the output of each section, which can be approximated by $(p-i+1)C_0$ as $R_0 \ll 1/2\pi f C_0$. Then, the cumulative delay $\Delta_{c,i}$ from the global input clock to each channel output y_i is given by

$$\Delta_{c,i} = \sum_{j=1}^{i} \delta_j = \frac{1}{2}(2p-i+1)iR_0C_0. \tag{15}$$

While the model for the global analog connection is mostly similar to the one for the clock, there is one important difference: the analog wire is loaded by the sampling capacitors. However, only 1 out of the p sampling capacitors is connected at a time, since the capacitors are tracking the input in a time-interleaved fashion. Thus, assuming channel i is active, an additional contribution C_s due to the sampling capacitance needs to be added to node y_i in Fig. 14. For that reason, the section delays δ_j prior to node y_i will experience an additional delay of R_0C_s, while the other section delays remain unchanged. Since there are i sections prior to node y_i, a total delay of iR_0C_s is experienced, thus the analog signal delay for channel i can be expressed as

$$\Delta_{a,i} = \Delta_{c,i} + iR_0C_s \tag{16}$$

leading to an effective systematic time-skew of

$$\Delta_i = \Delta_{a,i} - \Delta_{c,i} = iR_0C_s. \tag{17}$$

Therefore, the channel-dependent time-skew varies with equidistant steps from R_0C_s to pR_0C_s. Even though this is a deterministic error, it can be expressed with an equivalent σ_t of $0.289pR_0C_s$. pR_0 can be rewritten as L/WR_{sh}, where W and L are the total length and width of the global wire, and R_{sh} is its sheet resistance, leading to the following relation for the systematic time-skew:

$$\sigma_t = 0.289\frac{L}{W}R_{sh}C_s. \tag{18}$$

In the implemented design, where $C_s = 62$ fF, $R_{sh} = 0.05\Omega$, $W = 1$ μm, and $L = 384$ μm (16 channels with 24 μm height), a σ_t of 0.34 ps is expected. Similar to this result, an RC-extracted simulation on the time-interleaved structure predicts $\sigma_t = 0.38$ ps. Both results agree that the required timing precision of 8.1 ps from (14) can be achieved with the proposed

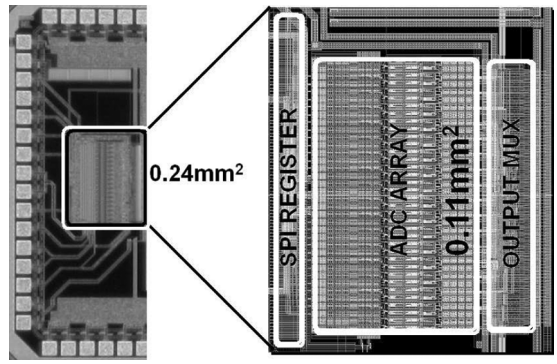

Fig. 15. Die photo and layout view of the ADC in 90 nm CMOS.

structure. More generally, since the predicted timing precision is substantially better than the requirement, the proposed matched-delay approach could be further extended towards higher resolution and speed, as well as higher interleaving factors.

D. Overall Implementation and Layout

Fig. 15 shows the realized ADC in 90 nm CMOS, which occupies 0.11 mm^2 including decoupling capacitors. The naked die is wirebonded to a PCB. An SPI interface controls the offset-calibration register. The digital logic required for the start-up offset measurement is implemented off-chip.

To be able to get all data off-chip without decimation, the 16 5-bit outputs are multiplexed to four channels of 5 bits. In this way, a 20-bit digital bus operating at 250 MHz can be used for interfacing the data off-chip to an FPGA board for realtime data-capturing. Thus, a data-multiplexer is included on-chip as well as a set of LVDS buffers (not shown in the figure). The analog input of the ADC is connected to the bondpads without any buffer but with an on-chip 100 Ω termination resistor. Thanks to the small size of the sampling switches (1.5 μm wide), the kickback effects are negligibly small in this case.

The supply for the switched-capacitor network has dedicated pins to prevent direct crosstalk with other on-chip blocks. The bonding wires and on-chip decoupling capacitors provide some filtering of noise from the external supply. On the PCB, a single standard linear regulator is used to provide all supplies to the ADC, including the supply for the switched-capacitor network.

IV. Measurement Results

The ADC was measured at 0.5 GS/s with 0.75 V supply and 1.0 GS/s with 1.0 V supply. The measured power consumptions are 0.47 mW and 1.6 mW, respectively. In both cases, the power consumption is distributed as follows: 33% in the clock divider and sampling-switch buffers, 10% in the switched-capacitor network and 57% in the comparator and ADC logic.

Fig. 16 confirms that the channel-offset can be tuned in steps of 0.5 LSB over a range of 15 LSB. Before calibration, the offset of the 16 channels ranges from -1.51 LSB to $+0.29$ LSB (Fig. 17). After calibration, all offsets are reduced to within ± 0.25 LSB, which matches with the 0.5 LSB calibration steps. Since this ADC is implemented as a stand-alone chip, the calibration is performed with a sine tone at the input, and 2048 samples per channel are averaged. However, as detailed in Fig. 9, an equivalent performance should be feasible with a noise input.

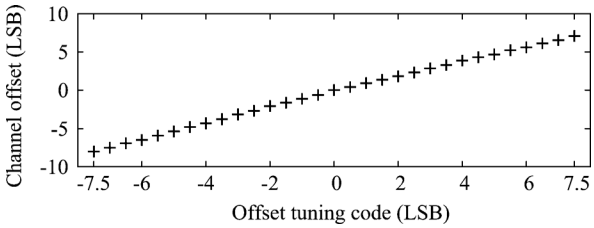

Fig. 16. Measured offset tuning range.

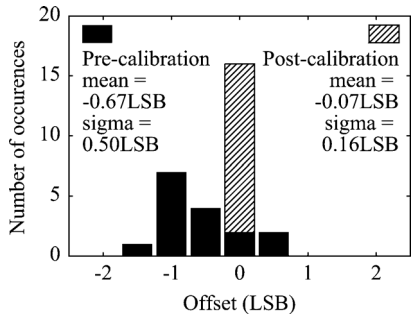

Fig. 17. Measured pre/post calibration offset (with sine-tone calibration).

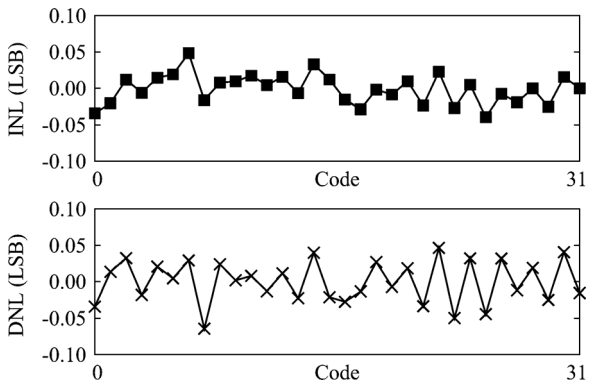

Fig. 18. Measured INL and DNL.

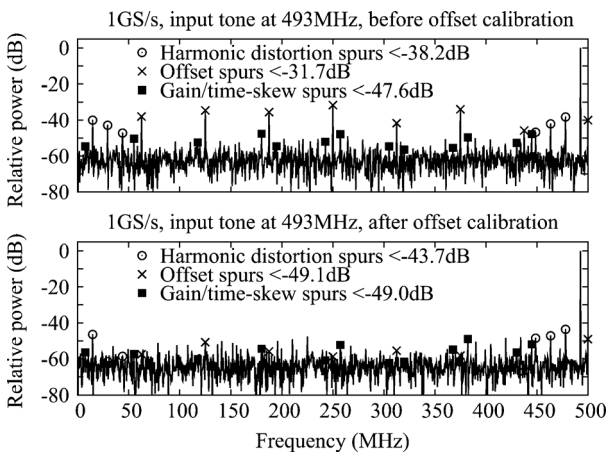

Fig. 19. Measured spectrum before and after offset calibration at 1 GS/s with 493 MHz input tone.

The measured INL and DNL (Fig. 18) are well below 0.1 LSB. Fig. 19 shows the output spectrum for a near-Nyquist tone at 1 GS/s both before and after offset calibration. Before calibration, the linearity is limited by offset mismatch. After calibration, the offset-spurs are reduced to -49.1 dB which is negligible for 5-bit accuracy. The figure also confirms that gain

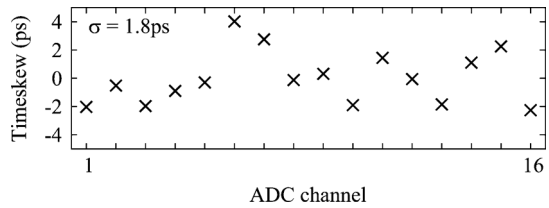

Fig. 20. Analysis of time-skew at 1 GS/s with 2.414 GHz input tone.

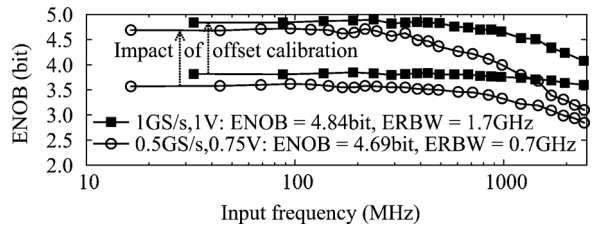

Fig. 21. Measured ENOB before and after offset calibration at 0.5 GS/s and 1 GS/s, using 0.75 V and 1.0 V VDD, respectively.

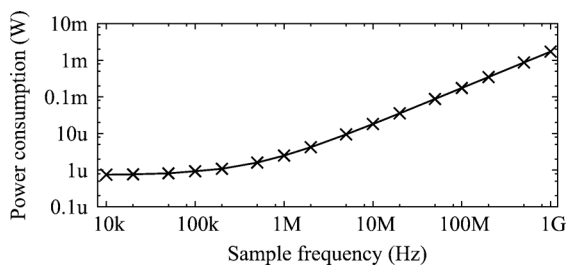

Fig. 22. Measured power consumption versus sample rate at 1 V supply.

and time-skew errors are negligible in this design (-49.0 dB). From the measurement at 1 GS/s with $f_{\rm in} = 2.414$ GHz, the time-skew performance for each channel was determined. As shown in Fig. 20, the time-skew is within -2 to $+4$ ps, with a σ_t of 1.8 ps. Since no systematic pattern in the time-skew analysis can be observed, it is most likely to be dominated by random time-skew rather than systematic time-skew.

Fig. 21 shows the ENOB for both sampling rates, before and after offset calibration. After calibration, an ENOB of 4.7/4.8 bits is achieved, while the ERBW is far beyond Nyquist. Using the FoM:

$$\text{FoM} = \frac{\text{Power}}{2^{\text{ENOB}} \cdot \min(f_s, 2\text{ERBW})},$$

power efficiencies of 36 fJ and 57 fJ/conversion-step are achieved at 0.5 GS/s and 1 GS/s, respectively.

Since this ADC is purely based on dynamic circuitry, the power consumption scales proportional to the sample frequency down to a leakage level below 1 μW, as shown in Fig. 22. Note that in this case, the supply is fixed to 1 V; a further power reduction at reduced samples rates is feasible by reducing the supply.

A summary of the measured performance is given in Table II. Compared to prior-art converters with a similar speed/accuracy target, this work achieves state-of-the-art efficiency without complex calibration schemes, despite the use of an older technology. Since most components in the presented design are limited by technology dimensions, the power consumption

TABLE II
MEASURED PERFORMANCE SUMMARY AND COMPARISON

	[4]	[5]	This work	
Resolution	6bit	5bit	5bit	
Supply	1.1V	0.8V + 1.2V	0.75V	1.0V
Power consumption	2.6mW	1.2mW	0.47mW	1.6mW
Sample frequency	2.2GS/s	0.25GS/s	0.5GS/s	1.0GS/s
ERBW	2GHz	≈0.2GHz	0.7GHz	1.7GHz
ENOB	4.9bit	4.4bit	4.7bit	4.8bit
FoM	40fJ/step	240fJ/step	36fJ/step	57fJ/step
Technology	40nm	65nm	90nm	
Area	0.03mm^2	2.3mm^2	0.11mm^2	
Calibration	Complex		Simple	

and chip area can be further reduced when scaling to a newer technology.

V. CONCLUSION

In this work, an ultra-low-power 5-bit time-interleaved SAR ADC for UWB radios was presented. The ADC is composed of power-efficient, area-minimized SAR sub-converters, using 400 aF unit capacitors, asynchronous logic and a self-resetting comparator. The time-interleaved structure is optimized by simplifying the layout of clock and signal connections. The prototype in 90 nm occupies 0.11 mm^2 and achieves a FoM of 36 fJ/conversion-step at 0.5 GS/s with 0.75 V supply or 57 fJ/conversion-step at 1.0 GS/s with 1.0 V supply.

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