A 1mW 4b 1GS/s Delay-Line based Analog-to-Digital Converter

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Abstract— **In this paper we introduce a novel Analog-to-Digital architecture for high speed applications that is compatible with digital CMOS and surpasses the issues with traditional voltage conversion techniques. The quantization method is based on the delay-to-digital concept as a means to quantize a variable delay line. A 4bit 1GS/s ADC with 1mW power consumption is designed in 65nm CMOS based on the proposed architecture. The new architecture is highly scalable with CMOS technology and because of its delay-line-based core, the ADCs performance enhances with further CMOS scaling and provides a promising method for the trend toward more digital implementation of circuits.**

I. Introduction

The emergence of high speed wireline and wireless protocols combined with the increase in low cost CMOS technology which is widely in favor of digital processing has put a high desire toward more digitally-assisted high speed applications. These applications vary from UWB standards and RF signal sensing in wireless transceivers to wireline signal conditioning and data acquisition [1]-[6]. Analog-to-digital converters are the major challenge for these digitally-assisted applications. Because of the nature of these applications an ultra high speed ADC with a relatively low number of bits is required. Even though the accuracy is low but because of the high speed required for processing the analog signal, the power consumption of these blocks become extremely important.

The conventional architectures for this range of ADCs are mostly high speed flash ([1]), folding flash([6]) and also time interleaved versions of Successive Approximation (SAR) Converters and Pipeline structures([3]-[5]). As mentioned in [8], in general, Analog-to-Digital conversion is performed in three steps: signal difference amplification, a zero crossing detector and a succeeding logic encoder. The analog signal difference amplification in all mentioned architectures are performed by amplifying the analog voltage (current) level by a voltage (current) amplifier. Due to the voltage and device scaling in the mainstream CMOS technology, both amplification and comparison are becoming more and more challenging mainly because the devices should be large and power hungry for large gain and low offset. In this paper, we use delay amplification as a different solution for signal difference amplification that shows significantly better performance for the high speed low resolution end of the ADC application spectrum. An applied pulse is propagated in a variable delay line and its delay is quantized after a certain time. The delay based ADC has the advantage of being highly digitally oriented, thus the scaling of CMOS which gives smaller delay steps is a fundamental advantage to it as opposed to traditional analog circuits.

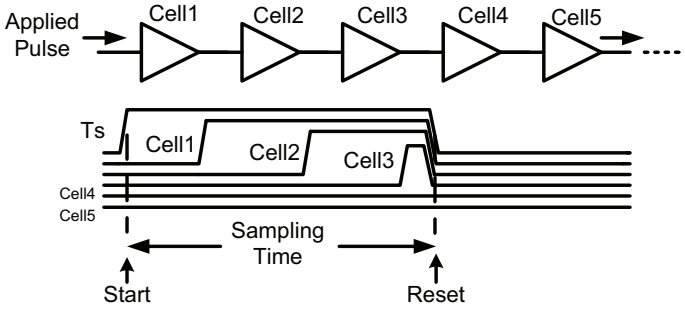

Fig. 1. Delay line based analog-to-digital conversion

The organization of the paper will be as follows. In section II the system will be described and the requirement for the delay cells will be discussed. Then in section III The delay cell will be introduced it's circuit issues will be addressed and the simulation results will be compared to the state-of-the-art high speed ADCs.

II. Delay-Line based ADC

The idea of delay amplification has been utilized traditionally for time-to-digital conversion with applications in phase locking and jitter measurements [7],[9]-[11]. The idea is to apply a pulse to a delay loop and measure the distance in terms of number of delay cells the signal passes in a certain amount of time. This number is proportional to the time window. There are also variations to this basic structure including using a variable delay and a constant time window. In ADC applications, the slope-based ADCs are well known as ADCs based on a delay depending on the input signal [11]. These analog-to-digital conversions are based on a small variation in the delay and giving a sufficient amount of time. Their target is relatively high accuracy but slow sampling rates. In Fig.1, the concept of the quantization method is shown. A digital pulse is applied to a chain of delay cells and the pulse propagates in the chain. After a fixed time window (T_s) the pulse has propagated to some extent and the number of the delay cells is a measure of the amount of delay for each cell. In these architectures, in order to get high accuracy the signal propagates several times in the line and a counter counts the

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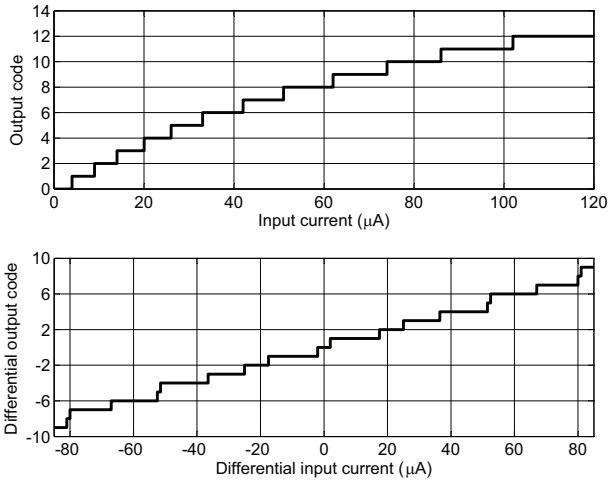

Fig. 2. Quantizer transfer function for single delay line (top) and differential delay line (bottom)

number of circulations. As opposed to the conventional delay to digital loop, in order to design a high speed ADC we only send the signal once in the line and watch the number of cells that are activated in a fixed time window. In this case, the delay cell dynamic range becomes crucial because the time is very limited and each delay cell is used once in each single sampling. It is instructive to observe what delay dependence is required in the delay line for a linear quantizer. Assuming $T(X_{in})$ is the delay dependence to the input X_{in}, after a time window of T_s, the number of cells in which the pulse has passed would be N:

$$NT(X_{in}) \geq T_s \Rightarrow N = \left\lfloor \frac{T_s}{T(X_{in})} \right\rfloor \quad (1)$$

Thus, for N as the output of the quantizer to be proportional to the input, from (1) the delay should have an inversely linear proportionality to the input. Unfortunately, this is an ideal case and in reality it would be quite hard to design a delay cell which has arbitrary small delays for some big inputs. In section III, we will see that a more realistic delay cell would have a characteristic as

$$T(X_{in}) = T_0 + \frac{A}{X_{in}} \quad (2)$$

Where T_0 and A are constants. This is mainly because there is always a minimum delay T_0 for every delay circuit. In this case the quantizer will deviate from the linear curve. In order to compensate the non-ideal effects we use a differential structure. In the differential structure we use the same non-ideal delay cells in two parallel paths and look at the differential output as the overall quantizer output. It can be seen that in this case the linear range of the quantizer increases significantly. The effect of using a differential structure compared to a single path can be clearly seen in Fig.2. From (1) the effective number of bits for the ADC would be proportional to the number of delay cells which will be 2N for the differential case.

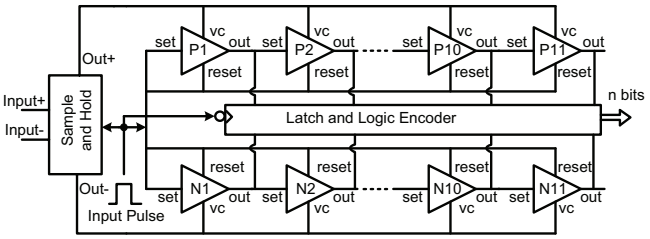

Fig. 3. Proposed differential Delay-Line ADC structure with P and N paths

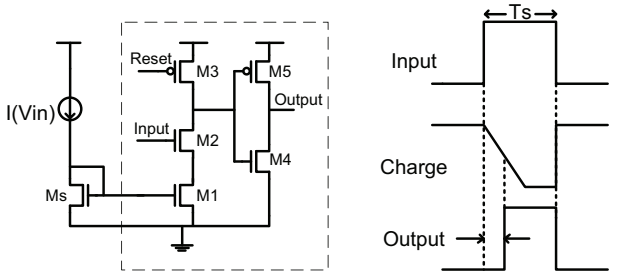

Fig. 4. The delay cell concept and circuit

III. Circuit Implementation

In this section, we propose the design procedure for designing a prototype ADC using the proposed architecture. Fig.3 captures the basic building blocks of the delay based ADC. The input Sample and Hold (SHA) samples the input and sets the delay of the cells. Then the pulse propagates in the delay line and afterwards, the digital encoder outputs the digital value. The delay cell is the core of the ADC and its function determines the overall performance. In the following, we will go through the circuit details of the delay cells, the sample and hold and the rest of the circuit issues, followed by the simulation results of the overall ADC.

A. The Delay Cell

As mentioned, the delay line as the core of the ADC is of the most interest, so we start from possible ways to implement a delay line. Different variable delay architectures have been proposed in the literature but usually the delay lines proposed previously did not have to have a wide dynamic range because the delay measurement was based on multiple loop counting that compensated for the small delay dynamic range ([9]-[12]). A suitable way to implement the delay line is to use the same concept used previously in variable slope ADCs.

As in Fig.4, a current source charging some capacitive node is changed proportional to the input signal changing the overall rising and falling time of the node. The charging node has a slope proportional to the input current and the output will be a delayed version of the input. According to Fig.4, one can write the introduced delay as:

$$T_D = C\frac{V_T}{I(V_{in})} + T_{inv} \quad (3)$$

where $I(V_{in})$ is assumed to be a linear function of the input V_{in}, C is the total capacitive load seen in the drain of M2 and

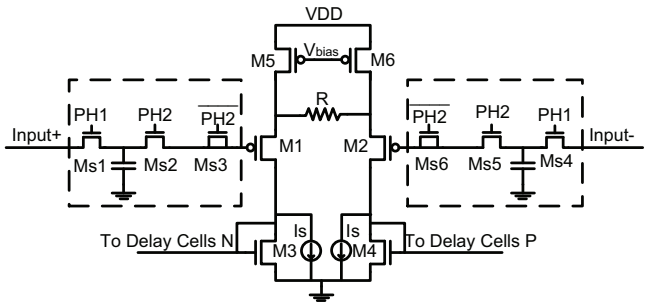

Fig. 5. Front End SHA and Voltage-to-Current converter

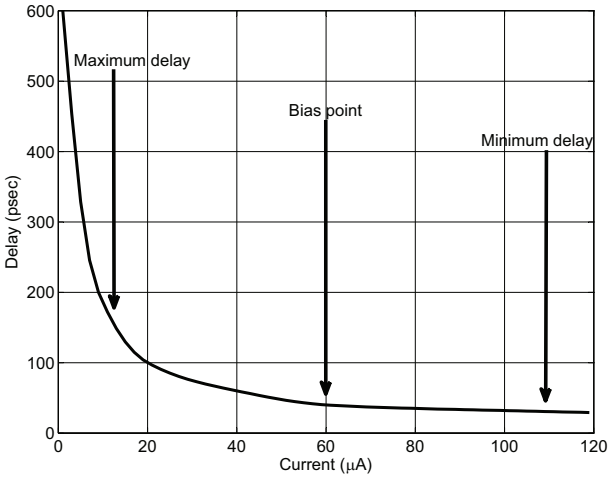

Fig. 6. Delay Cell delay vs. input current

V_T is the inverter threshold voltage. The term T_{inv} is added because there will always be a constant delay associated with the inverter (see (2)). In this circuit, M1 is the current source and is controlled by the current mirror M_s coming form the Sample and Hold. When the input of the cell becomes high, M2 turns on and the input capacitance of M4 and M5 is charged to the point that the output goes high with the delay described in (3). In order to get the highest delay and the lowest offset T_0, the capacitive node should be as small as possible. Also the inverter should be fast that requires M4 and M5 to be large, thus there is an optimum size for the inverter sizes to get minimum delay. Also M3 is used to reset the cell after the time window ends.

The delay cell output is latched by a fast latch composed of a switch and a buffer. The output is processed by a logic encoder that calculated the difference of the two input codes of the two differential paths and produces the final output bits.

Another notable property of this delay cell is that its power consumption is constant regardless of the input current because the power is roughly $T_D I(in)$ where T_D is almost inversely proportional to $I(in)$. Since the delay cell has no static power consumption, the delay line can be designed arbitrarily long so that for high sampling rates we get low number of bits, while for lower sampling rates where the the time window is wider, the pulse propagates in more cells and more quantization levels are achieved.

B. Front End SHA and Voltage-to-Current converter

The front end sample-and-hold circuit is shown in Fig.5. The input switching network marked by the dashed area is composed of two non-overlapping clock phases generated by the clock phase generator and samples the input differential signal. Devices $Ms3$ and $Ms6$ are dummies to reduce the common mode change caused by the charge injection of the switches. The sampled signal is converted to two differential current sources using the differential pair and the source degenerated resistor. The current is copied to all the delay cells producing the input dependent delay relation required for the delay line operation.

M5 and M6 are current sources which determine the bias current. In order to get a linear transconductance gain we should have: $g_{m_{M1,M2}} \gg R$. The current mirrors M3 and M4 are biased around the middle point in the delay cell swing as shown in Fig.6. In this case the differential current of M3 and M4 will be:

$$I_{DELAY_{P/N}} = I_{M4/M3} = I_b \pm \frac{\Delta V_{in}}{R} \tag{4}$$

Where, I_b is the common mode current of the cell. The settling time of the sample and hold is extremely important and directly affects the effective number of bits. In order to get maximum number of bits the delay line time window (T_s) should be a significant part of the sampling time, so the remaining for the settling of the SHA is small. The time constant of the settling equals to $\tau = C_{load}/g_{m_{M1,M2}}$. Where C_{load} is the total capacitive load at the gates of M3 or M4 which is the total delay cell current source which should be set in the settling phase. In this design 200ps of the 1ns sampling time is accommodated for the settling of the SHA. The sizing of the current mirrors and current sources in the delay blocks should be proper to meet the settling time.

C. Simulation Results

In this section we go through the simulation results for the designed ADC. The delay cell characteristic is shown in Fig.6. The delay cell is biased at $60\mu A$ and swings between $10\mu A$ and $110\mu A$ for the input voltage swing. The delay characteristic shifts up or down by around 10 percent over the corners which can be compensated by shifting the bias point. For the 1GSample/sec, of the 1nsec time, 800psec is designated for the pulse propagation phase, thus according to the delay characteristic the number of quantized levels would be $2N$ where N is the maximum number achievable in each delay line that is $N = \lfloor 800ps/35ps \rfloor = 22$, thus theoretically 44 levels are available for this time window. However in order to get reasonable linearity we only use 16 levels (4 bits) for this ADC. The DNL and INL of the ADC is shown in Fig.7. As it can be seen the INL is within the 0.5bit limit for 4 bits. The spectrum of the ADC output for a sinusoidal input is simulated and plotted in Fig.8. The performance of the ADC is summarized in Table I. The power consumption is 1mW that

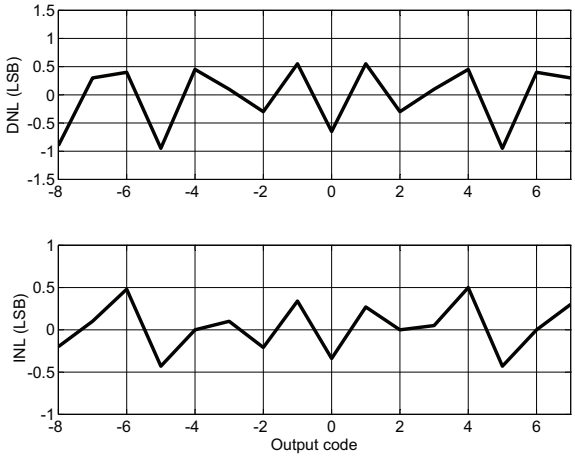

Fig. 7. Simulated DNL(top) and INL(bottom) of the ADC

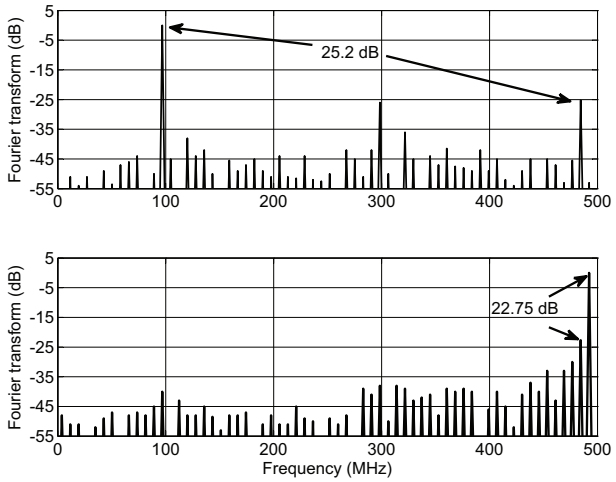

Fig. 8. 128 point FFT for 100MHz input (top) and 500MHz input (bottom)

almost half of it is from the delay line and the rest of it comes from the sample and hold. Because the sample and hold works at only one fifth of the total clock period, by turning it off in the hold mode, we can get even lower power consumption. With the simulated values and using the calculation of [6]:

$$FOM = \frac{power}{2^{ENOB} \times min(2 \times f_{in}, f_{sample})} \quad (5)$$

the ADC yields a FOM of 126fJ/conversion step. The comparison of this design to other high speed ADCs in Table II shows it's superior performance compared to most of the conventional structures.

IV. Future Work and Conclusion

In this paper we introduced a new approach for low power and high speed ADCs using delay lines that are highly compatible with digital CMOS process. The ADC can be easily scaled for higher sampling rate or higher number of bits. As a case study a 1 GS/s 4 bit ADC was designed. Due to the purely digital core, the delay based ADC is highly integrated and is a good fit for applications which require a fast ADC with low number of bits in a small area.

TABLE I

Performance Summary

Technology	65nm CMOS
Voltage	1.2
Sampling Rate	1GS/s
Number of Bits	4
Input Swing	$1V_{pp}$ Differential
SNDR @ 100MHz	21.3dB
SNDR @ 500MHz	19.9dB
SHA Power	$490\mu W$
Core Power	$530\mu W$
Total power	1.02mW

TABLE II

Performance Comparison of State of the Art ADCs

Ref.	Architecture	Power	F_s	Res.	Energy/Conv.
[1]	Flash	3.6 W	10G	5-bit	4700 fJ
[2]	Flash	2.5mW	1.25G	5-bit	160 fJ
[3]	TI-Pipeline	250mW	1G	11-bit	500 fJ
[4]	TI-SAR	1.8mW	500M	5-bit	440 fJ
[5]	Pipelined Flash	23.7mW	2.5G	4-bit	923 fJ
[6]	Folding Flash	2.2mW	1.75G	5-bit	50 fJ
This Work	Delayline	1.02mW	1G	4-bit	126 fJ

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