A 50-GS/s 5-b ADC in 0.18-µm SiGe BiCMOS

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ABSTRACT — **A 5-b 50-GS/s time-interleaved ADC is presented in 0.18-µm SiGe BiCMOS. The two-channel interleaved flash architecture is used to increase the conversion rate. The front-end three-stage distributed track-and-hold amplifier is devised to improve the dynamic performance. The ADC features SNDR as high as 23.1 dB with 20 GHz sine wave input at 50 GS/s conversion rate, and the third harmonic distortion is -36.5 dBc. It shows the measured resolution bandwidth of 18 GHz and the FOM of 9 pJ per conversion step with power consumption of 5.4 W.**

Index Terms **— Analog-to-digital converter, distributed track-and-hold amplifier, interleaved flash, millimeter-wave radio, optical transmission receiver.**

I. INTRODUCTION

Huge capacity-growth forecasts have lead to the development of technology for the next-generation transmission rate such as millimeter-wave radio or 100 Gb/s optical transmission. For instance, in a single wavelength approach, polarization-multiplexed quadrature phase-shift keying (PM-QPSK) modulation with a coherent receiver is one of leading architectures. Due to ultra high speed operations, significant research on DSP and ADC technology is required. A PM-QPSK coherent system requires four 50-GS/s ADCs in a receiver for *I/Q* and *X/Y* components, combined over 4 effective bits with the resolution bandwidth exceeding 16 GHz. Several high-speed ADCs have been designed recently [1-3], but their performance are not adequate for target applications. In this paper, as the first design step, a 5-b 50-GS/s ADC is presented in a 0.18-µm SiGe BiCMOS process. This ADC features SNDR and SFDR as high as 23.1 dB and 27.8 dBc respectively, with 20 GHz sine wave input at 50 GS/s sampling rate.

II. ARCHITECTURE

The time-interleaved flash ADC architecture, shown in Fig. 1, employs two 5-b flash ADC channels. The use of front-end interleaved sample-and-hold function relaxes the maximum clock skew between the interleaved channels. Fully differential input signal is first sampled by a distributed track-and-hold amplifier (DTHA) at a full sample rate (f_{FS}), and subsequent track-and-hold amplifiers (STHAs) in each channel are able to resolve the full input signal bandwidth of 20 GHz. The sampled signals are delivered to the two ADC

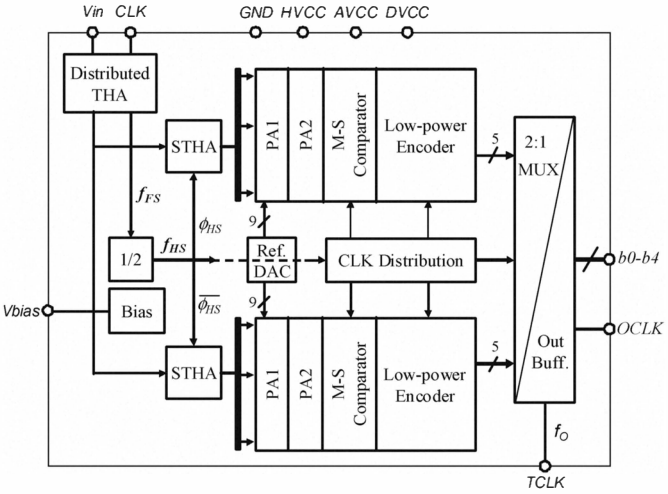

Fig. 1. Time-interleaved flash ADC architecture.

channels, alternatively quantized at a half sample clock (f_{HS}). Each ADC channel consists of two-stage preamplifier for double amplification and interpolation, master-slave comparator for fast regeneration operation, error-compressed low-power Gray encoder, and pipelined exclusive-OR based binary encoder. The selection of ADC channel from which the digital output will be provided is achieved through a high-speed 2:1 multiplexer (Mux) driven by a half clock period.

III. DISTRIBUTED TRACK-AND-HOLD

The speed and accuracy of the ADC at high input frequencies are largely determined by the performance of front-end THA. Interleaved sampling architecture is deployed to suppress the timing mismatch between two ADC channels without extra digital calibration. The main THA is a three-stage distributed track-and-hold topology, similar to the design in [4], but is implemented with a fully distributed topology (Fig. 2). The DTHA utilize a bank of identical three active switch circuits (SWO), where the input and output of each SWO is connected to the tap point of transmission lines. Here, input transmission lines of the distributed switches form the output transmission lines of the distributed input buffers, which enable higher driving capability. The track signal is made by adding the delayed parallel output voltages, while the hold signal is formed by adding the delayed parallel hold

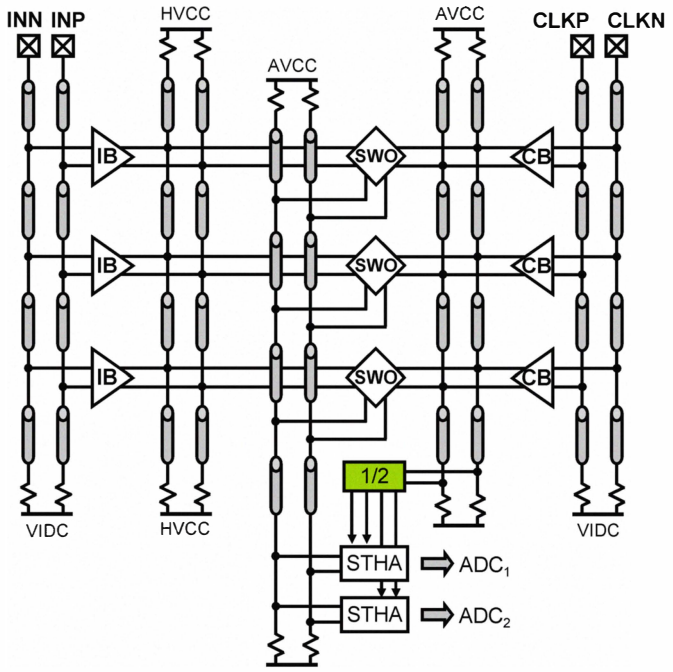

Fig. 2. Schematic of three-stage distributed THA. IB and CB denote input buffer and clock buffer, respectively.

signals sampled by delayed parallel control signals. So, the delay of input lines and clock lines should be matched through the selection of propagation constant and length of the two lines as such the output signals from each individual switch circuit sum in phase. The DTHA shows simulated gain of -0.7 dB and small signal track-mode bandwidth over 40 GHz. The DTHA output is connected to two STHAs, which is similar to the THA in [3], controlled by alternate half clocks. The STHA shows 24 GHz track-mode bandwidth and over 41 dBc SFDR with a full-scale 20 GHz sine wave input in simulations.

IV. CIRCUIT DESIGN

The static performance of the ADC is constrained by the error on reference voltage and device mismatch (i.e., offset voltage) of the bipolar transistors, as well as gain and offset error between two channels. Digitally controlled reference voltage generation is a powerful technique to alleviate the impact on amplifier array. The reference voltage is produced by an 8-b current-steering DAC, as shown in Fig. 3. The 6-b unary MSBs are used for generating 8 different reference voltages (V_{R1}-V_{R8}, and V_{R9} = AVCC), while the two binary LSBs are used for the compensation of offset variation. The nine reference voltages are shared with two ADC channels to suppress the offset error between them. In addition, the output common-mode voltage of each STHA is aligned with a half of

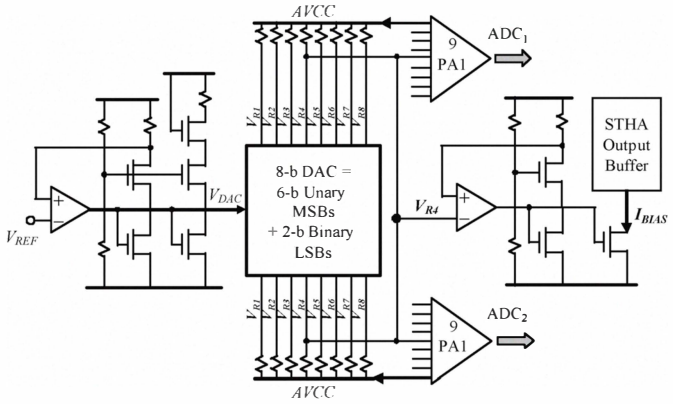

Fig. 3. Schematic of a shared reference voltage generation.

the full-scale input range by controlling the bias of the STHA output buffer with the middle-point of the reference (= V_{R4}).

The 31 thermometer outputs (T_0 – T_{30}) are converted to 5-b Gray encoder. Fig. 4 illustrates a scheme of low-power Gray encoder. It features the combination of cascaded folded differential logic (FDL) [5] and wired-OR logic. This scheme can reduce the error rate and the number of logic circuits. In order to avoid the degradation of data transfer rate, the number of comparators connected into a FDL are limited to four. High-speed wired-OR logic is added after the FDL to generate

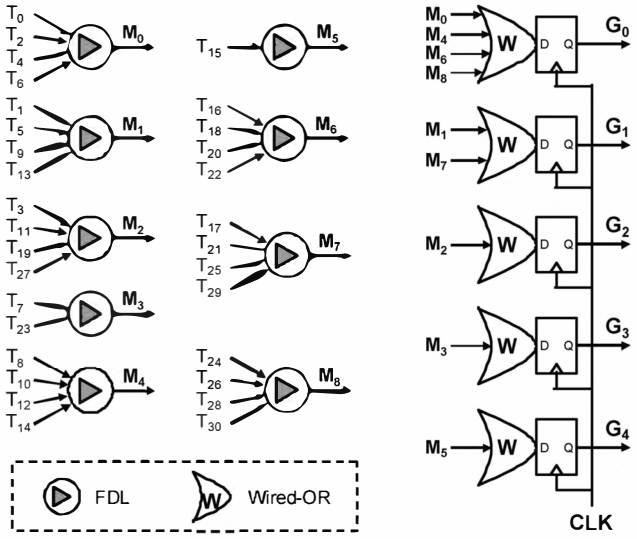

Fig. 4. Schematic of a modified FDL + Wired-OR based low-power Gray encoder logic.

Gray code (G_0 – G_4). The pipelined exclusive-OR gates finally convert the Gray code into 5-b binary code.

V. MEASUREMENT RESULTS

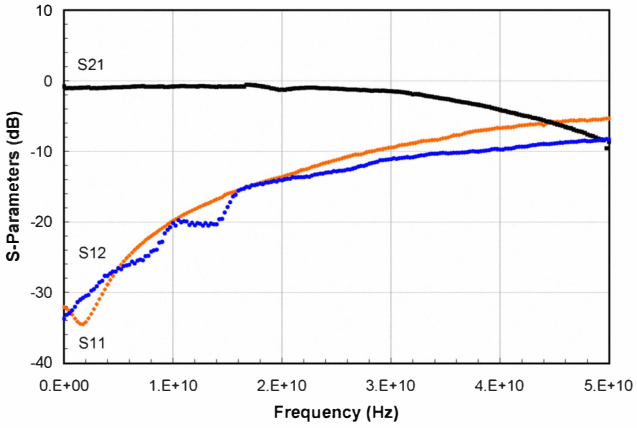

Fig. 5. On-wafer S-parameters measurements of a 3-stage distributed THA.

Along with the ADC prototype, a separate test chip was fabricated for testing a 3-stage DTHA. On-wafer probe testing was carried out using 150 µm pitch probes. Two supply voltages are used: 3.8 V (V_{CCH}) for the front-end THA and 3 V (V_{CC}) for the output buffer. At the clock frequency of 56 GHz, the THA power dissipation is 480 mW. The S-parameter data is measured with an Agilent 67GHz network analyzer, as shown in Fig. 5. The small-signal bandwidth (S21) in track mode exceeds 38 GHz with flat passband gain of -0.8 dB. Measured input return loss S11 is well below -7 dB up to 50 GHz. Two-tone intermodulation tests are performed with 20 GHz and 20.001 GHz at the input power of -5 dBm. It shows the measured 3rd-order intermodulation distortion of about -42 dB below the fundamental.

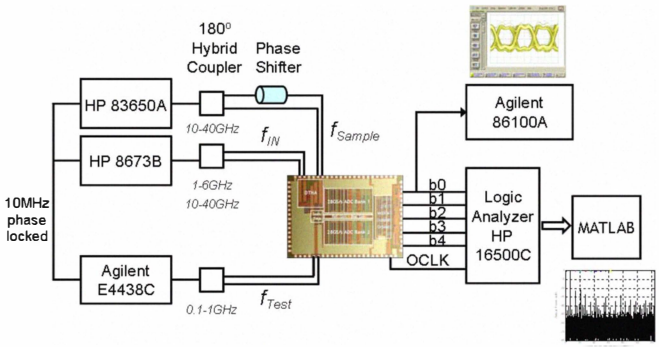

Fig. 6. ADC test set-up.

The measurement of the ultra-high-speed ADCs is always troublesome in the design phase. It has been using backend digital processing [2], on-chip DAC [1], or integrated frequency decimation using dividers and flip-flops [3]. In this design, the ADC output is subsampled with external frequency decimation such that the output data rate is decimated with test frequencies at f_{test} = 250/500 MHz in a test mode. The maximum sampling frequency is observed to 50 GHz, limited by test setup in Fig. 6 (sampling clock synthesizer < 50 GHz, 180° hybrid coupler < 40 GHz, K-connector < 40 GHz, etc).

The ADC has been implemented in 0.18-µm SiGe BiCMOS process offering BJT f_T/f_{max} = 200 GHz and six layers of metals. The chip occupies 3.78 x 2.7 mm^2 silicon area. Multiple power supplies are used: HVCC = 3.8 V for THAs, AVCC = 3 V for analog blocks, and DVCC = 3 V for digital blocks. At the sampling clock of 50 GHz, peak power dissipation is about 5.4 W. More than 50 pads of 78 bonding pad counts are dedicated to power and ground networks to supply sufficient current with low bondwire inductance. Approximately 2.1 nF of decoupling capacitance is arranged between power and ground networks. The ADC is mounted in a ceramic substrate via epoxy glue, which is then recessed into a circuit board. The substrate is carefully mounted on heat sink to minimize thermal resistance between the substrate and heat sink. At 42 GS/s, measured DNL and INL are below 0.65 LSB and 1.04 LSB, respectively. Fig. 7 shows an output spectrum measured with 19.986 GHz sine wave input at f_s = 42 GS/s. With f_{test} = 250 MHz, the fundamental spectrum is

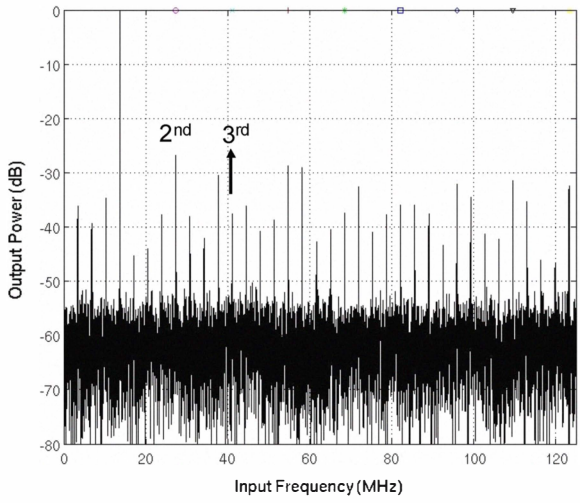

Fig. 7. Output spectrum measured with 19.986 GHz input signal frequency at 42 GS/s sampling rate (16384 FFT).

located at 14 MHz. The second harmonic distortion is -27.2 dBc and the third is -36.5 dBc. The SNDR is 23.5 dB and effective number of bit (ENOB) is 3.6-bit.

Fig. 8 shows the measured SFDR and SNDR at 50 GS/s operation. The SNDR is better than 22 dB up to Nyquist frequency. The SNDR degradation at high input frequencies is mainly determined by signal-frequency-dependent spurious tones and aperture jitter of 400 fs (i.e., RMS jitter of clock source in ADC test setup). The effective resolution bandwidth

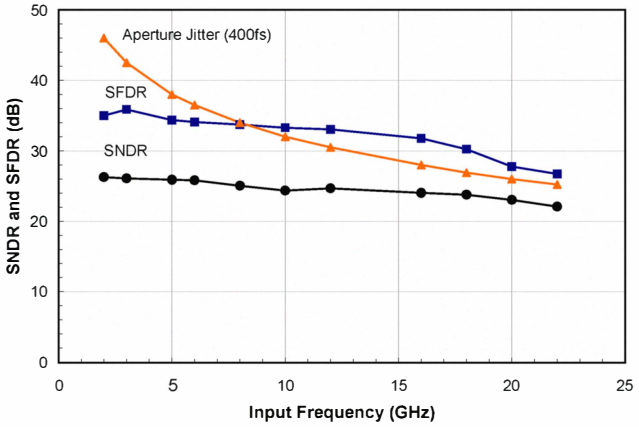

Fig. 8. Measured SNDR and SFDR versus input signal frequencies at 50 GS/s.

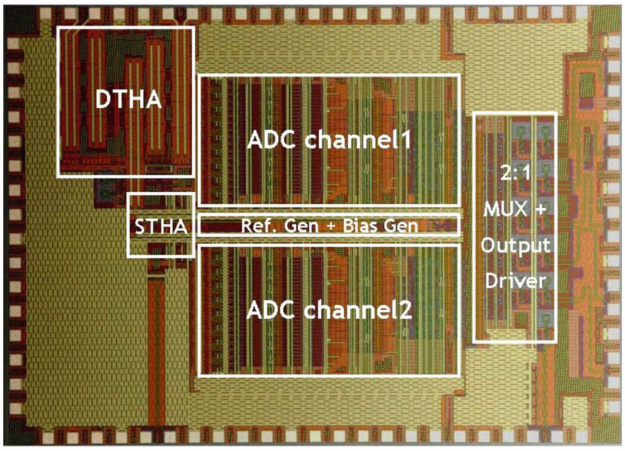

Fig. 9. ADC micrograph.

exceeds 18 GHz, and the figure of merit (FoM) of energy per conversion step is 9 pJ. The die micrograph of the ADC is shown in Fig. 9.

VI. Conclusion

Time-interleaved flash ADC that can digitize input signals up to 20 GHz has been demonstrated in 0.18-µm SiGe BiCMOS. A fully distributed 3-stage distributed THA, sampled at clock frequencies up to 56 GHz, has been used to perform wideband digitization with high dynamic performance. Power-efficient comparator and Gray encoder contribute to achieve low-power consumption of 5.4 W. The ADC demonstrates 18 GHz resolution bandwidth and the FoM is only 9 pJ/conversion step (to the author's knowledge, this ADC is the best resolution bandwidth and FoM over prior arts). This ADC potentially expands the range of applications in which high sampling rate is required such as 100 Gb/s optical transmission receiver [6], wideband data acquisition system, fast digital oscilloscope, millimeter-wave radios, or electronic warfare systems.

TABLE I
PERFORMANCE SUMMARY

Input bandwidth	> 20 GHz
Sampling frequency	> 50 GHz
Static linearity (DNL/INL)	+/- 0.7/1.1 LSB
SNDR @ fin = 2 GHz	26.3 dB
SNDR @ fin = 22 GHz	22.1 dB
Resolution bandwidth	18 GHz
Power dissipation	5.4 W @ 3/3.8 V
Figure of Merit	9 pJ/cs
Chip area/core area	3.78 x 2.7 mm^2
Technology	0.18-µm SiGe BiCMOS

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