Utilizing Process Variations for Reference Generation in a Flash ADC

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***Abstract*—This brief presents an experimental study on how to take advantage of the increasing process variations in nanoscale CMOS technologies to achieve small and low-power high-speed analog-to-digital converters (ADCs). Particularly, the need for a reference voltage generation network has been eliminated in a 4-bit Flash ADC in 90-nm CMOS, with small-sized comparators. The native comparator offsets, resulting from the process-variation-induced mismatch, are used as the only source of reference levels, and redundancy is used to acquire the desired resolution. The measured performance of the 1.5-GS/s ADC is comparable to traditional state-of-the art ADCs and dissipates 23 mW.**

***Index Terms*—Flash analog-to-digital converter (ADC), high-performance design, parameter variation.**

I. Introduction

As CMOS technologies continue to scale down deeper into the nanometer regime, the process variation has become an ever-increasing problem for the design of any VLSI circuit [1]. The within-die variations of random dopant fluctuations and process imperfections related to the subwavelength lithography cause large variations of circuit parameters such as the transistor threshold voltage [2], [3]. According to the International Technology Roadmap for Semiconductors [4], the relative threshold voltage variations for minimum-size transistors will continue to increase with technology scaling. Therefore, the accuracy control of analog and mixed-signal circuits implemented with small device sizes will pose increasingly greater challenges.

The aim of this brief is to provide an experimental study on how to take on a new approach toward process variations. There exist several studies on how to design circuits that are more tolerant to the increasing problem related to the process parameter variations, such as [1]. The approach in this brief is to view the process variations as a source of diversity and opportunistically utilize this to provide a stochastic distribution of the design metrics of individual building blocks. This idea is explored through the case study presented in this brief with the realization of an analog-to-digital converter (ADC) with the references generated by mismatch-induced comparator offsets.

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High-speed low-resolution ADCs are required in both wire transmission, such as gigabit Ethernet, and wideband wireless receivers. The integration of the front end and the back end requires the ADCs to be implemented in nanoscale CMOS processes, where the process variations cause a significant overhead in terms of power and complexity.

Traditionally, accuracy in ADCs has been achieved by sizing in the analog domain together with calibration and trimming methods to combat the large process variations and mismatch. In [5], redundancy was used to relax the accuracy constraints of the comparators in the ADC. In [6], a combination of redundancy and calibration was used to lower the power dissipation through minimizing the power used by the redundant circuits.

There exists various calibration methods employed in Flash ADCs, and a majority of them are foreground calibration methods that adjust or trim reference voltages or comparator trip points. When redundant circuits are used, the calibration methods first characterize the existing circuits, followed by the selection of an optimal set. There are also background calibration techniques employed such as the technique reported in [7].

Despite the significant achievements reported in the past, the design of ADCs still involves tradeoffs between sizing and accuracy. This has lead to considerable power and area overheads compared with theoretical bounds [8], which will increase as technology scales deeper into the nanometer regime.

In the experimental study of this brief, we present an ADC that utilizes the existing process variations by generating the reference levels through the random distribution of comparator offsets caused by the mismatch. Increased variations would even improve the performance as the input range would increase, and magnitudes of the comparator mismatch up to $10\times$ the current variations would be beneficial. Redundancy is used to provide enough statistical spread in the comparators while at the same time allowing minimum-size transistors, leading to low power dissipation and better utilization of the technology. This highly scalable architecture will continue to benefit from reduced feature sizes, with increasing sampling rates and lower power dissipation, while not being limited by the increasing process variations.

This brief is organized as follows: Section II describes how stochastically distributed references should be treated. In Section III, the ADC architecture is presented together with the subblocks. Section IV shows the measurement results, followed by conclusions in Section V.

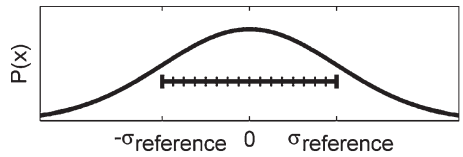

Fig. 1. Distribution of reference levels in relation to the ideal locations of a 4-bit ADC.

II. Distribution of Reference Levels

In the design of an n-bit Flash ADC, the $2^n - 1$ reference levels should be equally spaced, with a least significant bit size of $V_{\rm FS}/(2^n - 1)$. This is traditionally implemented by the division of the full-scale range using a resistor ladder. Through the mismatch in both the comparator circuits and the reference generation network, these reference levels will shift. However, to achieve the desired n-bit functionality, the static errors must be kept sufficiently small.

In the proposed architecture, no reference network is needed, and all comparators are identically designed. The native comparator offsets, resulting from the process-variation-induced mismatch, are then used as the only source of reference levels. If we consider the zero-crossing of the differential input signal as the reference midpoint, the reference levels of individual comparators will be shifted due to the native offsets. The offsets of the entire comparator array will then form a set of reference levels. If a subset of these comparator trip points, corresponding to the ideal reference levels, can be selected from the full set, then the target transfer characteristic of an n-bit ADC will be met.

Since all comparators will be designed to detect the input zero-crossing, they can be implemented based on regular sense amplifiers. As the threshold voltage variations are approximately normally distributed [1], the offsets, and therefore the reference levels, will be normally distributed with zero mean and a certain standard deviation $\sigma_{\rm reference}$. If we consider a full-scale input range of $\pm\sigma_{\rm reference}$, which will further be explained at the end of this section, the probability density function of the normally distributed reference levels is shown in Fig. 1 and compared with their ideal location within the full-scale range.

The achievable resolution depends on the outcome of the distribution of offsets, i.e., the reference levels. It would then be desirable to find how the expected effective resolution, which is achieved for 99.9% of the devices, varies as a function of the number of comparators. This is done by performing Monte Carlo simulations with a fixed number of comparators, where each comparator suffers from a randomly distributed static offset with a standard deviation of $\sigma_{\rm reference}$. Each statistic outcome results in a set of reference levels; out of these levels, the subset that gives the maximum signal-to-quantization-noise ratio is chosen. This corresponds to the calibration performed on the fabricated ADC, where only the comparators that contribute to an increase in the resolution are used. By performing 1000 such Monte Carlo simulations and analyses, the expected effective number of bits (ENOB) and the respective standard deviation are acquired for the fixed number of comparators. This procedure was then repeated for an increased number of comparators. By sweeping from 4 to 10 ideal number of bits,

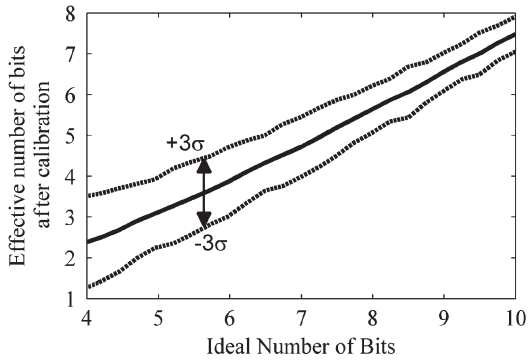

Fig. 2. ENOB assuming only static errors, achieved for an ADC with normally distributed reference levels.

where the number of comparators is given by $2^{\rm ENOB,ideal} - 1$, the expected number of bits is acquired as a function of the ideal resolution. Fig. 2 plots the result of these simulations. A first-order fit of the -3σ limit gives the expected minimum ENOB that is achieved for 99.9% of the devices and is expressed as

$$\text{ENOB} = 0.96 \cdot \text{ENOB}_{\rm ideal} - 2.64. \tag{1}$$

As an example, an ADC with 255 comparators, corresponding to an ideal resolution of 8 bits, would result in at least 5 effective bits with a probability of 99.9%. The -3σ fit also shows that an increase in the ideal resolution results in approximately the same increase in the effective resolution, making the required redundancy fixed. Note that for this ADC, with the references being randomly generated, the ideal resolution does not correspond to the case of no mismatch or process variations as for traditional ADC architectures. Without the presence of any process variations, the proposed architecture will only generate one effective bit, whereas the ideal resolution could only be reached if all reference levels, through random variations, end up at the ideal locations.

The full-scale input range of $2\sigma_{\rm reference}$ is chosen for resulting in the maximum number of bits in the Monte Carlo simulations. As the input range is directly determined by the process variations, it must be sufficiently large such that the thermal noise does not dominate. A thermal noise analysis of regenerative comparators is given in [9], with the noise voltage given by

$$V_{\rm noise}^2 = \frac{2kT}{C}. \tag{2}$$

Equating this noise to the quantization noise as in (3), we get an estimation of how large the mismatch-induced offsets must be, i.e.,

$$\frac{V_{\rm FS}^2}{12} 2^{-2n_{\rm effective}} = \frac{2kT}{C}. \tag{3}$$

Solving this equation for $V_{\rm FS}$, with $n_{\rm effective} = 4$ and $C = 10$ fF, gives $V_{\rm FS} = 50$ mV. This corresponds to $\sigma_{\rm reference} = 25$ mV, which can easily be expected, considering just the $V_{\rm th}$ variations in 90-nm CMOS.

An advantage with the proposed architecture lies in the higher resolution domains, which are becoming increasingly

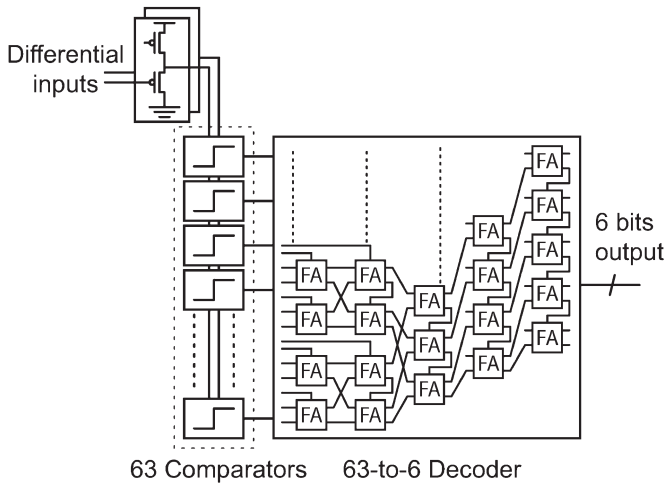

Fig. 3. Architecture of the Flash ADC.

attractive for Flash ADCs due to their ability to utilize technology scaling [10]. At these resolutions, the traditional resistor ladder reference will dissipate a significant portion of the total power. Increasing the number of bits by 1 will double the power in the comparator array, decoder, and clock circuitry. The accuracy requirement on the resistor ladder will double [11], but the number of comparators that inject kickback charge also doubles. Therefore, the impedance required to control the transients would be reduced by more than a factor of 2, increasing the relative contribution of power dissipation. By using the proposed power efficient architecture, the reference generation power is eliminated, and the Flash topology becomes more attractive for larger resolutions as well.

III. ADC Architecture

To prove the concept of an ADC without a reference network, a test chip was manufactured. The ADC was designed with 63 comparators, corresponding to 6 ideal number of bits.

Fig. 3 shows the block diagram of the ADC architecture. The differential input signal is buffered through two single-ended source follower circuits shown in the same figure. The buffer is used to reduce kickback effects, control the common-mode voltage, and drive the bank of 63 small-sized low-power comparators. As the reference levels are randomly distributed, there will be no internal order of the comparators, preventing the use of traditional decoder techniques. Therefore, a summing decoder is used to efficiently convert the output array into binary.

To reject the unwanted reference levels, the calibration method has been implemented by disabling the comparators with undesired offsets. This will set the comparator output to zero independent of the input signal. The entire output array is then summed in the decoder, implemented as a pipelined 6-bit Wallace tree decoder.

A. Decoder

The Wallace tree decoder, as shown in Fig. 4, is used to generate a binary representation of the output from the comparator

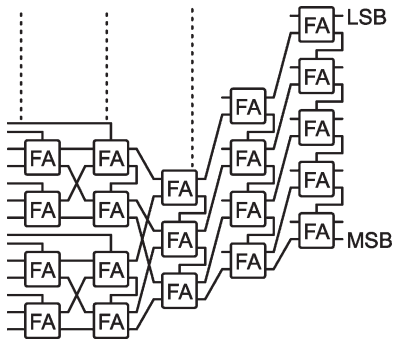

Fig. 4. Wallace tree decoder (63-to-6 bits).

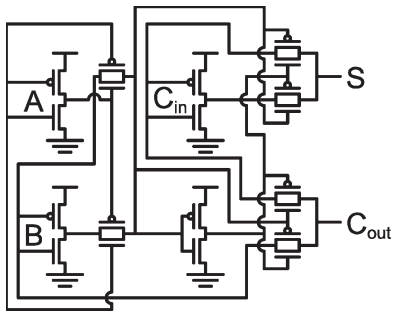

Fig. 5. Transmission gate full-adder cell.

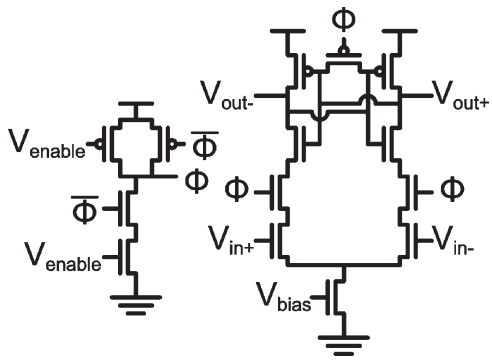

Fig. 6. Sense-amplifier-based comparator.

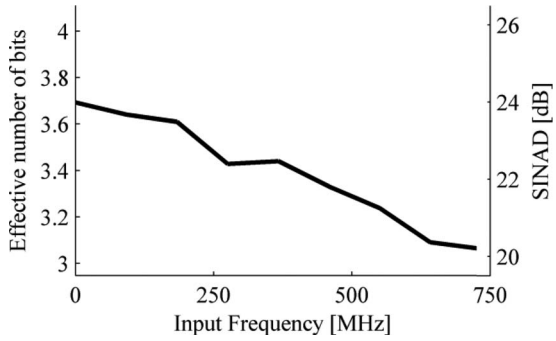

Fig. 7. ENOB/SINAD versus input frequency.

array by counting the number of 1s. As the critical path of a 6-bit Wallace tree decoder is nine full adders [12], the decoder is pipelined to handle the throughput of a multigigasample/second ADC [13].

The full adders used for this purpose are transmission-gate-based full adders, as shown in Fig. 5. These have been chosen

TABLE I
PERFORMANCE COMPARISON

Author Year	Effective Number of Bits (ENOB)	Sampling Frequency (fs)	Effective Resolution Bandwidth (ERBW)	Process	Power Dissipation (P)	$FoM1 = \frac{P}{2^{ENOB} \cdot f_s}$	$FoM2 = \frac{P}{2^{ENOB} \cdot 2 \cdot ERBW}$
[10] 2008	6.9	1.25 GS/s	1.3 GHz	90 nm CMOS	207 mW @ 1 V	1.38 pJ/Conv-Step	0.67 pJ/Conv-Step
[13] 2007	3.9	4 GS/s	100 MHz	0.18µm CMOS	608 mW @ 1.8 V	10.2 pJ/Conv-Step	20.4 pJ/Conv-Step
[16] 2008	5.44	1.6 GS/s	800 MHz	0.13µm CMOS	180 mW @1.5 V	2.61 pJ/Conv-Step	2.61 pJ/Conv-Step
[17] 2007	3.25	3.0 GS/s	1.5 GHz	0.18 µm CMOS	43 mW @ 1.8 V	1.51 pJ/Conv-Step	1.51 pJ/Conv-Step
This Work	**3.69**	**1.5 GS/s**	**600 MHz**	**90 nm CMOS**	**23 mW @ 1.2 V**	**1.18 pJ/Conv-Step**	**1.47 pJ/Conv-Step**

because of resulting in the best power–performance tradeoff for the entire pipelined decoder.

B. Comparator

The comparator used in the ADC is a sense-amplifier-based comparator, as shown in Fig. 6. The mismatch in the input pairs, as caused by process variations, results in native comparator offsets forming the set of reference levels. As the mismatch in differential pairs degrades the common-mode rejection ratio, special care has been taken to reduce common-mode variations at the input. At the beginning of the evaluation phase, any charge at the source and drain terminals of the input transistors will be discharged to ground. This causes a common-mode kickback to the input that could affect subsequent samples. By inserting the clocked transistors in between the cross-coupled inverter pair and the input transistors, the precharge of these internal nodes is prevented, and the common-mode kickback is reduced [14].

Not being limited by the mismatch, the transistors used in the comparator can be small to reduce the power dissipation. The minimum transistor sizes used will then only be determined by the required operating speed, eliminating the sizing–accuracy tradeoff. For this comparator design, only sizes smaller than 1 μm, which is 10$\times$ the minimum width, were used.

C. Calibration

For calibration, each comparator is characterized with a reference level using a sine-wave input through the histogram method [15]. A similar calibration method was implemented on-chip in [6], where a DAC searches for the individual comparator trip points, which shows that the method is efficient and does not rely on external measurements and exact trimming of trip points or reference levels. The number of comparators resulting in the maximum performance is enabled; the rest are disabled using clock gating to save power. The local clock-gating circuit is implemented as a NAND gate to emphasize the rising edge. This will keep the disabled comparators in the latching state, and changes in the input signal will not affect the output or dissipate power due to switching. For the disabled comparators not to count toward the output, the enable signal is used as a reset in the subsequent latch. This architecture allows any number of comparators to be enabled to achieve the maximum resolution.

IV. MEASUREMENT RESULTS

The ADC was designed and manufactured in 90-nm CMOS. For testing, the chip was directly bonded on a PCB to reduce the package loss. To test the ADC at high sampling rates, the decoder output was downsampled by a factor of 64 to guarantee the signal integrity needed for measurements.

Fig. 7 plots the ENOB and signal-to-noise-and-distortion ratio (SINAD) versus the input frequency at a sampling rate of 1.5 GS/s. At low input frequencies, the effective resolution was 3.69 bits, and the effective resolution bandwidth (ERBW) was 600 MHz. The maximum absolute integral and differential nonlinearities were below 0.53 and 0.38 bits, respectively. At a supply voltage of 1.2 V, the power dissipation was 23 mW, including the input buffers, clock generation, and driver circuits.

The best performance was measured using an input range of 100 $\mathrm{mV_{p\text{-}p,diff}}$, which would indicate a comparator mismatch deviation $\sigma_{\mathrm{reference}} \approx 50$ mV. This also shows why this ADC will actually benefit from larger variations as the full-scale input range would then increase, whereas traditional architecture utilizing calibration would have to increase the range for which calibration is possible at the cost of an increased power dissipation overhead.

Table I summarizes the measured performance of the ADC together with recently published Flash ADCs that do not require extensive calibration, showing that the proposed design achieves a performance comparable to that of previously reported state-of-the-art ADCs. The micrograph of the fabricated ADC is shown in Fig. 8, with an active area of 0.04 $\mathrm{mm^2}$.

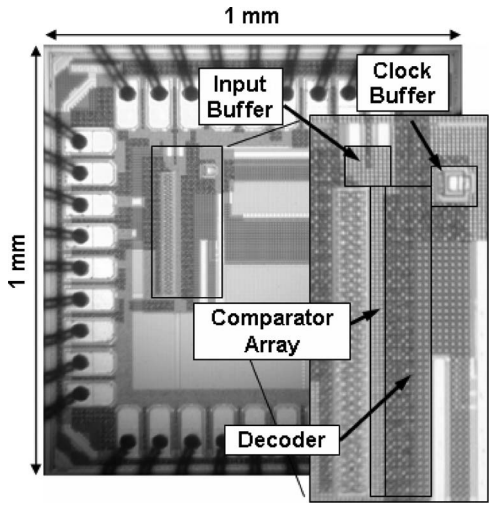

Fig. 8. Micrograph of the fabricated ADC.

V. Conclusion

This brief has demonstrated a new approach to take advantage of process variations by utilizing them as a source of diversity rather than being viewed as strictly detrimental to circuit performance. The concept has been explored through the experimental study of an ADC that uses the inherent mismatch-induced comparator offsets to generate the reference levels, removing the need for a resistor ladder. The manufactured test chip in 90-nm CMOS achieves an effective resolution of 3.69 bits at 1.5 GS/s while dissipating 23 mW, which is comparable to state-of-the-art ADCs.

Although the presented ADC is not a commercially viable architecture in the presented form, it offers a new view on how the challenges of nanoscale CMOS technologies can be utilized instead of being combated. As technology scales deeper into the nanometer regime, new solutions will be needed to retain and further increase the power efficiency of mixed-signal circuits and to fully utilize the benefits offered at these technology nodes.

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