A 10-GS/s Multibit Delta-Sigma Analog-to-Digital Converter in an InP HBT Technology

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***Abstract* — Continuous time delta-sigma (CTΔΣ) analog-to-digital converters (ADCs) are capable of sampling at much higher rates than discrete time ΔΣ converters. This makes heterojunction bipolar transistor (HBT) technologies excellent candidates for the implementation of fast CTΔΣ ADCs. Due to linearity considerations, all HBT-based ΔΣ ADCs known to us incorporated a single-bit digital-to-analog converter (DAC). Here, we present a multibit lowpass ΔΣ ADC based upon the InP HBT technology, which incorporates an internal resolution of 2 bits. The ADC was clocked at 10 GHz, its total power consumption was 1.9 W, and it obtained a signal-to-noise ratio (SNR) of 44.1 dB at signal bandwidth of 312.5 MHz.**

***Index Terms* — Analog-digital conversion, bipolar integrated circuits, delta-sigma modulation, heterojunction bipolar transistors.**

I. Introduction

High speed continuous time delta-sigma analog-to-digital converters (ΔΣ ADCs) have become widespread in state-of-the-art communications systems and radars. The simplicity of the ΔΣ converter enables to design and fabricate it in fast technologies, e.g. SiGe and III-V heterojunction bipolar transistors (HBTs), despite the limit on transistor count usually set by those technologies due to yield requirements.

Contemporary HBTs sport cutoff frequencies in excess of 500 GHz [1], while commercial and semi-commercial processes reach 300 GHz [2]. As a result, very fast HBT-based ΔΣ ADCs have been demonstrated, sampling at several GS/s. Due to transistor count limitations, all of them are of the continuous time type. The converters include both lowpass [3],[4] and bandpass [5]–[7] that consist of the basic 2nd and 4th order structures, respectively. A high complexity 10th order bandpass ADC also has been reported [8], as well as tunable bandpass converters that can shift the center frequency of the band [9]–[11]. Among the above, two ADCs sample at 10 GS/s or faster [4], [6].

As the linearity of the internal DAC of the ΔΣ ADC must be sufficiently high to support the final resolution of the ADC [12]–[14], and digital methods of nonlinearity correction are too complex for HBT technologies, all HBT-based ΔΣ ADCs known to us, including the above mentioned, incorporated a single-bit DAC, which is linear by definition [3],[6]. Here, we present a multibit ΔΣ ADC based upon the InP HBT technology, which incorporates an internal resolution of 2 bits. The ADC consists of a 2nd order modulator, which makes use of op amps rather than simple transconductance amplifiers.

II. Implementation

A. Architecture

The ADC consists of a lowpass second order ΔΣ modulator, incorporating a 2-bit quantizer. A block diagram of the ADC is shown in Fig. 1, featuring two loop filters, a quantizer, and additional DAC and buffer that serve as measurement auxiliary circuits.

The dominant noise contributors are the input-referred noise of the first filter and the output noise of the DAC, as both are introduced at the modulator's input. The DAC noise consists of the noise current generated by the transistors, and noise caused by clock and data jitter. To alleviate the effect of data jitter, the comparators of the flash ADC consist of the master-slave structure [15],[16], in which the output is well synchronized with the sampling clock. However, the master-slave comparator delays its output by one half of the clock period. This delay introduces excess loop delay at the ΔΣ feedback path. Instability of the modulator caused by the delay must therefore be corrected using compensation methods [17].

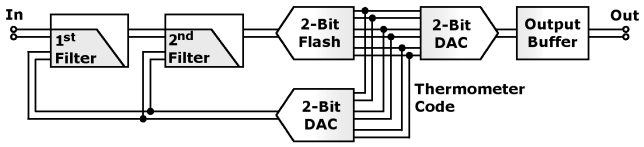

Fig. 1. Block diagram of the second order ΔΣ ADC. The decimation filter is replaced by an additional DAC and output buffer.

The loop transmission of the modulator is given by the expression $-H_q H_2 (1 + H_1)$, where H_1, H_2, and H_q are the transfer functions of the first and second loop filters and the quantizer, respectively. The above expression implies that if a zero exists in H_2 the loop transmission inherits the very same zero. Hence, we have added a zero to the second filter, as will be explained in the next section.

The converter was designed to work with over-sampling ratio (OSR) of 16, hence the maximum achievable signal-to-noise ratio (SNR) is 58.6 dB, equivalent to an effective number of bits (ENOB) of 9.4. The supply voltage of the whole ADC is 6 V to enable high gain of the loop filters' op amps.

B. Loop Filters

Each filter consists of a fully differential op amp connected as a summing integrator (Fig. 2). The resistors denoted R_Z introduce a zero to the transfer function, and exist only in the second filter.

The goal of the zero is to compensate the loop gain, as mentioned above.

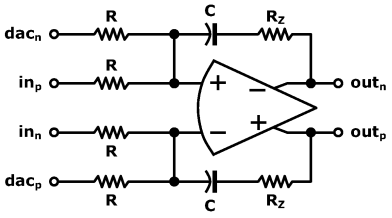

Fig. 2. Schematic diagram of the loop filter.

The key parameters of the op amp are low frequency (LF) gain and linearity. High LF gain improves the noise shaping at low frequencies and reduces the nonlinear phenomena of dead bands and idle tones [14], which are undesirable. Linearity of the op amp in the first integrator is critical to the linearity performance of the ΔΣ ADC, as this distortion is referred back directly to the input of the ADC. Linearity of the second integrator, on the other hand, is less critical.

Schematic diagram of the op amp is shown in Fig. 3. The circuit incorporates two gain stages with standard Miller compensation. An additional class-A common-collector stage serves as an output stage. The first stage is degenerated by a resistance of 20 Ω to improve the linearity of the amplifier, at the expense of 8 dB in gain. However, since the linearity of the second integrator is less critical, no degeneration was applied to the op amp of the second integrator, to regain the 8 dB-gain lost in the first integrator. In order to avoid latch up problems during start up, the common mode feedback circuit controls only half of the current of the second gain stage, while the other half is fixed current.

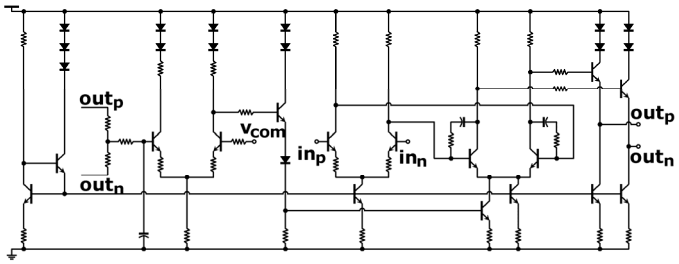

Fig. 3. Schematic diagram of the op amp.

The op amp uses the global 6 V supply voltage of the ADC and consumes 50 mA (excluding any load current). The output common mode voltage is 2.5 V, and so is the input DC voltage.

C. 2-Bit Quantizer

The quantizer includes a differential 2-bit flash ADC and current steering DAC. Control over the quantizer gain is available via the reference voltage of the flash ADC. Since noise and linearity of the DAC are critical for the performance of the complete ΔΣ ADC, no external control is connected to the DAC.

Shown in Fig. 4 is a schematic diagram of the flash ADC. The voltage at V_{REF} controls the dynamic range of the flash. The ratio between the dynamic ranges of the flash ADC and the DAC sets the total gain of the quantizer. Each of the 3 comparators comprises a preamplifier and master-slave latch. The preamplifier improves the sensitivity and alleviates the effect of clock kickback. Illustrated in Fig. 5, it consists of a cascode stage followed by two emitter follower stages. The preamplifier has a separate biasing circuit to prevent the clock transients from interfering via the current sources. The master-slave latch is based upon the standard ECL topology. Here, clock kickback effect is reduced by degeneration of the clock switching pair. The latching pair includes emitter followers to increase its speed by neutralizing the Miller effect. Finally, the speed of the master latch is enhanced by the introduction of peaking inductors. The schematic diagram of the complete master-slave latch is depicted in Fig. 6. Simulated sensitivity of the comparator is below 0.1 mV when clocked at 10 GHz, which means, in practice, that the sensitivity is limited by noise. Total current consumption of the flash ADC is 173 mA.

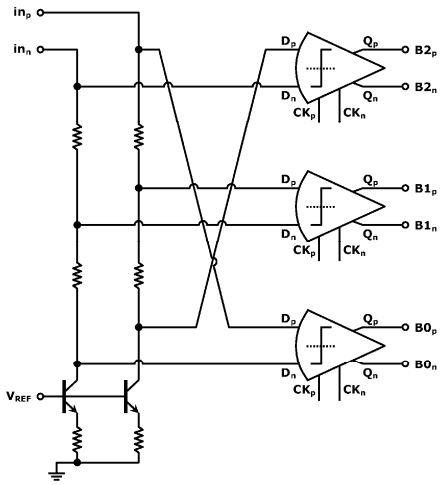

Fig. 4. Schematic diagram of the differential 2-bit flash ADC.

The DAC is based upon the standard differential current steering architecture, as shown in Fig. 7. The digital input is provided by the flash ADC in the thermometer coding format; hence, the switched current sources (I0–I2) are identical. The differential pairs forming the current switches are slightly degenerated in order to reduce output overshoots caused by sharp input transients. The differential pairs and the current sources are matched using the method reported by us in [18], which demonstrated a DAC with linearity of 9.2 bits. The DAC is loaded by the two integrators, which together introduce a 150 Ω resistance to ground at each side. The total current consumption, when loaded by the integrators, is 15 mA.

D. Clock Distribution

As explained before, the comparators of the flash ADC consist of the master-slave structure, which delays its output by one half of the clock period. This results in excess loop delay, which may result in instability of the ΔΣ modulator. To alleviate the effect of excess loop delay we have reduced the quantizer delay to slightly less than half clock period. This was done by implementing an uneven clock distribution manifold. The manifold comprises longer transmission lines leading to the master latches than the lines leading to the slaves. The delay difference between the two paths sums up to about 2.5 psec. This delay difference results in shorter comparator delay at the expense of small degradation in

sensitivity, as the masters have shorter time for making a comparison.

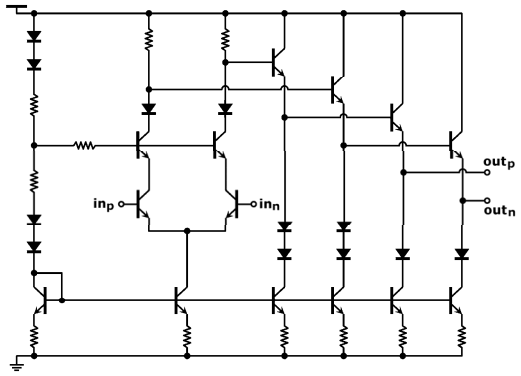

Fig. 5. Schematic diagram of the comparator's preamplifier.

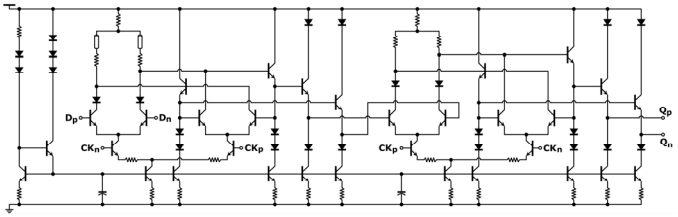

Fig. 6. Schematic diagram of the comparator's master-slave latch.

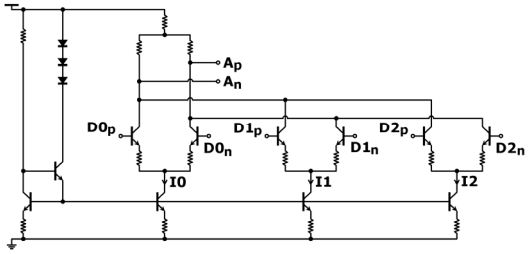

Fig. 7. Schematic diagram of the 2-bit DAC.

E. Measurement Auxiliary Circuits

A common method of measurement of ΔΣ ADCs is by feeding the bit stream coming from the output into a logic analyzer that logs the digital data in a file. Then data are processed off-line by a mathematical software [8]. This method is limited by the speed of the logic analyzer, usually several hundred MHz. In addition, the number of probes required for such a measurement equals, at least, to the number of bits of the quantizer. Acquisition speed can be slowed down by buffering the output in a shift register, but the bit number is then multiplied accordingly [3],[9]. If the ADC loop resolution is 1 bit, the digital output can be treated as an analog signal and fed directly into a spectrum analyzer, to obtain SNR and linearity [19]. Since our loop resolution is 2 bits, a different method of measurement is required. The method proposed by us is explained below.

Due to the high sensitivity of the modulator performance to the DAC's output, we have located the probing point at the digital signal connecting the flash's output with the DAC's input. The signal is fed to an additional DAC, which is identical to the internal DAC, and then buffered by a high current common collector stage (Fig. 1). Finally, the signal is introduced at the input of a spectrum analyzer.

F. Layout and Fabrication

All the above blocks were put together to form the layout of the whole ΔΣ ADC. The number of transistors sums up to 378 transistors, with the following distribution: 31 transistors in each of the op amps, 245 transistors in the flash ADC (where each comparator includes 81 transistors), 32 transistors in each of the DACs, and 7 transistors in the output buffer.

The ADC was fabricated using the 1-μm emitter InP DHBT technology of Fraunhofer Institute for Applied Solid State Physics (IAF) [2]. A microphotograph of the circuit is shown in Fig. 8. Total die area was 2.25x2.25 mm^2.

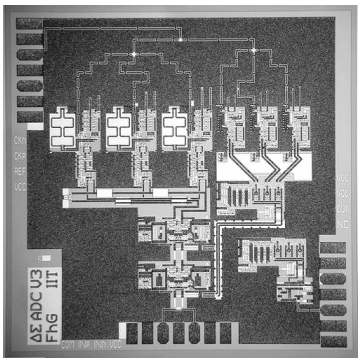

Fig. 8. Microphotograph of the ΔΣ ADC.

III. Experimental Results

The ADC was characterized by introducing a sine wave at the input and measuring SNR at the output. The clock signal was generated by a Wiltron 68337B signal generator, and the input signal by a Wiltron 68177B. The analog output was sampled by an Agilent E4440A spectrum analyzer. The supply voltage was 6 V, the DC voltage of the inputs was 2.5 V, and the reference voltage of the flash ADC (V_{REF}) was 1.7 V. All DC voltages were provided by Hameg HM 8142 power supplies. The total power consumption was 2.26 W, where the ADC itself consumed 1.89 W, and the output driving circuits 370 mW.

The circuit was tested with a clock frequency of 10 GHz, signal frequency of 310.779 MHz, and signal power of 1.2 dBm (from which 2 dB should be subtracted due to cable attenuation). Spectrum of the output is shown in Fig. 9. Noise shaping is clearly evident in the figure. Using the adjacent channel power (ACP) function of the spectrum analyzer, the noise and signal powers were integrated and the SNR was 44.1 dB. This value is equivalent to an ENOB of 7.01.

The waveform of Fig. 9 shows significant harmonies, a result of nonlinearity somewhere in the system. The nonlinearity can originate either by the ADC itself or in the probing circuit (output DAC and buffer). Two additional measurements were carried out in order to diagnose this phenomenon: two-tone linearity test and time domain measurements using an oscilloscope. Results of both measurements show severe nonlinearity in the output driving circuit, probably due to the use of a common collector output stage and long lines towards the output DAC. We have therefore

concluded that the linearity of the ADC itself cannot be characterized.

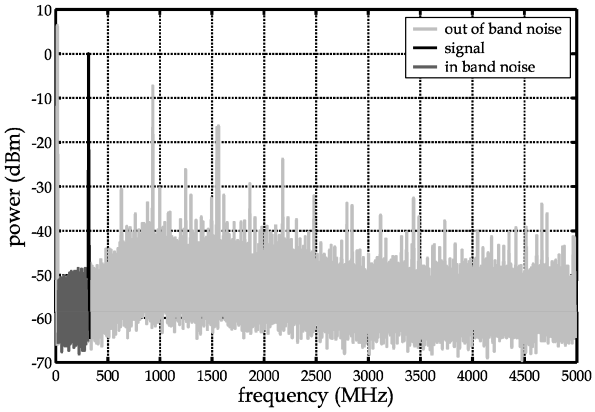

Fig. 9. Measured spectrum of the ADC's output.

IV. Conclusion

Table I summarizes the performance of the ΔΣ ADC. A continuous time multibit lowpass ΔΣ ADC, clocked at 10 GHz, was demonstrated. The Converter consumes 1.89 W and exhibits SNR of 44.1 dB. Linearity could not be characterized. This work is compared to other works in Table II. To our knowledge, this is the first multibit ΔΣ ADC implemented in an HBT technology.

TABLE I
Summary of ADC Performance

Modulator type	continuous time lowpass 2nd order
Technology	Fraunhofer IAF InP DHBT
No. of transistors	378
Supply voltage	6 V
Power consumption	1.89 W
Clock frequency	10 GHz
OSR	16
SNR	44.1 dB
SNDR	N/A
Figure of Merit	23.5 pJ/conv

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References

[1] E. Lind et al, *DRC 2007*, June 2007.
[2] R. Driad et al, *IEEE TED*, 58, pp. 2604–2609, August 2011.
[3] S. Krishnan et al, *IEEE TMTT*, pp. 2555–2561, December 2003.
[4] A. Hart et al, *RFIC 2008*, pp. 181–184, June 2008.
[5] J.A. Cherry et al, *IEEE TCAS–II*, pp. 518–530, June 2000.
[6] T. Chalvatzis et al, *IEEE JSSC*, pp. 1065–1075, May 2007.
[7] B.K. Thandri et al, *IEEE JSSC*, pp. 269–279, February 2007.
[8] M. Inerfield et al, *IEEE JSSC*, pp. 1524–1532, September 2003.
[9] A.E. Cosand et al, *IEEE JSSC*, pp. 1633–1639, October 2004.
[10] M. Schmidt et al, *RFIC 2009*, pp. 153–156, June 2009.
[11] P. Ostrovskyy et al, *MTT-S 2009*, pp. 1129–1132, June 2009.
[12] G.I. Bourdopoulos et al, *Delta-Sigma Modulators: Modeling, Design and Applications*, Imperial College, 2003.
[13] S.R. Norsworthy et al, *Delta-Sigma Data Converters: Theory, Design, and Simulation*, Wiley–IEEE Press, 1997.
[14] R. Schreier and G.C. Temes, *Understanding Delta-Sigma Data Converters*, Wiley–IEEE Press, 2005.
[15] R.E.J. van de Grift et al, *IEEE JSSC*, pp. 374–378, June 1984.
[16] T. Wakimoto et al, *IEEE JSSC*, pp. 1345–1350, December 1988.
[17] W. Gao et al, *ISCAS 1997*, pp. 65–68, June 1997.
[18] S. Kraus et al, *IPRM 2010*, pp. 317-320, June 2010.
[19] S. Krishnan et al, *MTT-S 2003*, pp. 1063–1065, June 2003.

TABLE II
Recently Published HBT-Based ΔΣ ADCs

Reference & Year	[5] 2000	[3] 2003	[8] 2003	[9] 2004	[6] 2007	[7] 2007	[4] 2008	[10] 2009	[11] 2009	This Work
Technology	SiGe HBT	InP HBT	InP HBT	InP HBT	SiGe BiCMOS	SiGe BiCMOS	SiGe BiCMOS	SiGe BiCMOS	SiGe BiCMOS	InP HBT
Architecture	CTΔΣ Bandpass	CTΔΣ Lowpass	CTΔΣ Bandpass	CTΔΣ Tunable Bandpass	CTΔΣ Bandpass	CTΔΣ Bandpass	CTΔΣ Lowpass	CTΔΣ Tunable Bandpass	CTΔΣ Tunable Bandpass	CTΔΣ Lowpass
Loop Order	4th	2nd	10th	4th	4th	4th	2nd	4th	4th	2nd
Quantizer Resolution	1 bit	1 bit	1 bit	1 bit	1 bit	1 bit	1 bit	1 bit	1 bit	2 bits
Power	450 mW	1.8 W	6 W	3.2 W	1.6 W	75 mW	350 mW	1 W	270 mW	1.89 W
Clock Frequency	4 GHz	8 GHz	8 GHz	4 GHz	40 GHz	3.8 GHz	35/37/40 GHz	7.5 GHz	9 GHz	10 GHz
Signal Bandwidth	20 MHz	62.5/125 MHz	40/80 MHz	1/60 MHz	60/120 MHz	1 MHz	100/500/1000 MHz	20 MHz	10 MHz	312.5 MHz
OSR	100	64/32	100/50	2000/33	333/167	1900	175/37/20	188	450	16
ENOB	6.3	8.9/7.7	13.7/12.0	12.7/8.0	8.8/8.3	9.5	8.5/7.1/5.9	7.3	6.9	7.0*
Figure of Merit	143 pJ/conv	30/35 pJ/conv	5.6/9.2 pJ/conv	240/104 pJ/conv	30/21 pJ/conv	52 pJ/conv	4.7/2.6/3.0 pJ/conv	159 pJ/conv	113 pJ/conv	23.5 pJ/conv

* ENOB of this work is derived from SNR since SNDR is not available