APPLYING LOW POWER CONSUMPTION SUPERCONDUCTIVE DEVICE TECHNOLOGY TO REAL-TIME WAVEFORM MONITORING FOR PHOTONIC NETWORK

Mutsuo Hidaka, Michitaka Maruyama, and Hideo Suzuki

Superconductivity Research Laboratory, International Superconductivity Technology Center

ABSTRACT

A superconductive single flux quantum (SFQ) circuit is an ultimate low-power consumption electrical device. It can operate at a more than 100-GHz clock frequency with less than 1-μW power consumption per gate. A promising application of the SFQ circuit in the near future is a real-time oscilloscope. With a real-time monitoring method, non-periodical waveforms can be observed. This method is indispensable for future network monitoring, and a higher sampling clock will be demanded. Commercially available semiconductor real-time oscilloscopes have extended input bandwidth and sampling clocks due to hardware and software interleaves. On the other hand, an SFQ circuit may increase those aspects without any interleaves because it can help implement a high-speed and high-reliability analog to digital converter (ADC) with its high-speed and periodic characteristics. We propose a new SFQ ADC and confirm its high sampling clock of over 150 GS/s by computer simulations.

Keywords—Superconductive device, single flux quantum circuit, real-time oscilloscope, AD converter, sampling clock

1. INTRODUCTION

Superconductive single flux quantum (SFQ) circuits [1] have the ability to operate at a more than 100-GHz clock frequency with less than 1-μW power consumption per gate because the operation voltage is less than 1 mV, which is three orders smaller than that of semiconductor circuits. Low thermal noise at cryo-temperatures enables us to use such small signals. Therefore, SFQ circuits can implement high-speed and low power consumption large-scale integrated (LSI) circuits. Moreover, superconductive microstrip transmission lines that are capable of transferring a picosecond SFQ pulse over centimeters at the speed of light are available. We previously developed a fabrication process [2], circuit design [3], and packaging [4] technologies for Nb-based SFQ circuits that operate at around 4 K. A prototype system of an SFQ 4×4 switch with a scheduler successfully demonstrated DVD data transfer among 4 PCs [5]. We also demonstrated a 40-Gbps serial switch operation using another SFQ switch prototype system [6].

Although becoming a large-scale network switch is a good target for SFQ circuits because the simple configuration by serial processing and the low-power nature of an SFQ device results in an ultimate low-power system, a lot of time is needed to make it commercially available. Thus, we chose a flush type analog to digital converter (ADC) used in a real-time oscilloscope as an SFQ circuit application because it is a relatively simple system and can be implemented in the near feature. Moreover, the high-speed and periodic characteristics of SFQ devices are effectively utilized in it [7].

In this article, we describe the operational principle and a state of the art Nb-based SFQ technology, current status of semiconductor high-speed real-time oscilloscopes, and expected performance of a real-time oscilloscope using a proposed SFQ ADC.

2. SFQ TECHNOLOGY

Magnetic flux is quantized in a superconducting loop. The minimum unit is the SFQ, whose value is 2.07×10^{-15} Wb. We define one SFQ in the superconducting loop as logical "1" and no SFQ in the loop as logical "0" (Fig. 1). An SFQ cannot go through a superconductor. Thus, we use a Josephson junction (JJ) as a gate. A JJ is a device in which two superconductors are weakly coupled. When the supply current exceeds the critical current of the JJ, the JJ switches to a voltage state and superconductivity is broken. At that moment, a SFQ can go in and out of the loop.

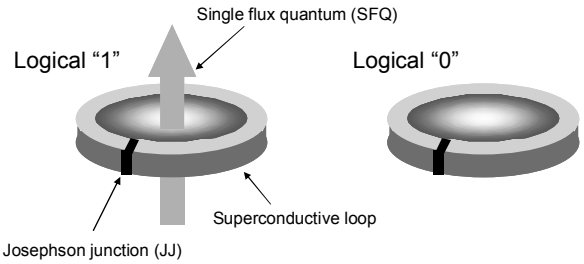

Figure 1. Schematic of SFQ device in the case of logical "1" and logical "0".

An example of an SFQ circuit is shown in Fig. 2 (× represents a JJ). An ordinary SFQ loop has two or three JJs. In SFQ circuits, such loops are connected to each other and

978-0-7695-3297-4/08 $25.00 © 2008 IEEE
DOI 10.1109/SAINT.2008.41

SFQ pulses can be propagated, stored, divided, and joined in the circuits. We can make all Boolean logic gates from combinations of these operations.

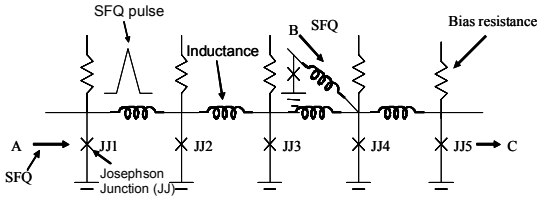

Figure 2. SFQ circuit example in which SFQ loops are connected with various forms.

When an SFQ enters a superconducting loop through a JJ, pulse shape voltage is generated. Thus, SFQ propagation can be considered voltage pulse propagation. Therefore, SFQ circuits are pulse logic ones. The SFQ pulse has a constant area in time-voltage plain of 2.07 mV-ps.

We have two fabrication processes: the standard process (SDP) and advanced process (ADP). The SDP uses four Nb layers for a ground plane and three wiring layers. The minimum JJ and line sizes are 2×2 and 1.5 μm, respectively. The critical current density (J_c) of a JJ is 2.5 kA/cm^2 and corresponds to a 40-GHz switch operation. The ADP can increase the Nb layers to 9 by using a planarized method, and the planarized Nb surface enables us to obtain a better photolithography resolution, resulting in a smaller JJ (1×1 μm) and line (0.8 μm) sizes. The J_c is increased to 10 kA/cm^2 and corresponds to an 80-GHz switch operation. An 8-bit shift register with a 120-GHz clock frequency and only a few μW power consumption per gate (which has a more than three order advantage including cryo-cooler power consumption compared with same speed semiconductor devices), a one-million SQUID array with no open or short circuits, and 16-kbit RAM including 80,768 JJs were fabricated using the ADP and successfully tested [2].

We have adopted a cell-based design methodology in which circuits are constructed from tile-shaped basic cells, for example, an AND cell and OR cell. We developed an SFQ cell library including about 250 cells [3]. We and our collaborators have developed many SFQ circuits consisting of up to 11,000 JJs and successfully operating at several tens of GHz clock frequency [8]-[11].

A superconductive multi-chip module (MCM) was developed in which SFQ chips were flip-chip bonded to an MCM carrier with 30-μm diameter solder bumps. The MCM carrier has superconductive wiring and an SFQ pulse can propagate to other chips at over 100 Gbps [12]. We also developed a cryocooled system for mounting the MCM. It had 32 10-Gbps ports through which high-speed signals were transferred between room temperature instruments and the SFQ chips [4].

By integrating elemental technologies, we implemented a 4×4 SFQ network switch prototype system. The system's core is composed of two SFQ chips. One is a 4×4 switch chip with a scheduler driven by a 40-GHz on-chip clock generator. The other is a 6-channel SQUID driver chip that amplifies the outputs of the switch chip. Each chip contains about 2,200 JJs. They were flip-chip bonded on a 16×16 mm MCM carrier. The carrier was then installed in the cryocooled system, which was cooled by a two-stage 4-K 1-W cryocooler. We measured the bit error rates (BER) through all the input and output channels of the SFQ switch. They were in the order of 10^{-13} for a 10^{23}-1 pseudo-random bit sequence at 10 Gbps. The BER is low enough for communication applications. We also implemented a four-port SFQ ethernet local area network (LAN) switch through which DVD data were transferred. All the modules were installed in a standard 19-inch rack [5] as shown in Figure 3. To demonstrate 40-Gbps serial processing by an SFQ system, we also developed another prototype system in which a 2×2 switch with 4:1 MUX and 1:4 DEMUX was mounted [6].

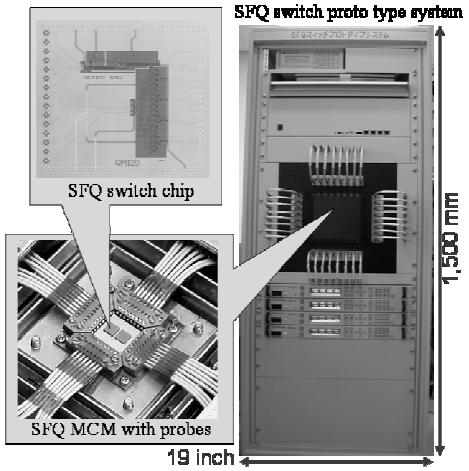

Figure 3. SFQ switch prototype system in standard 19-inch rack. SFQ MCM and SFQ switch chip insets. Compressor of cryocooler not shown.

3. SEMICONDUCTOR REAL-TIME OSCILLOSCOPES

A real-time oscilloscope is able to monitor non-periodical waveforms, which is indispensable for future photonic network monitoring. An ADC is a key component and determines the input bandwidth and sampling clock of the oscilloscope. TeKtronix, Agilent, and LeCroy are leading companies supplying real-time oscilloscopes. The catalog specifications for the bandwidth and sampling clock are 16 GHz and 50 GS/s for TeKtronix [13], 12 GHz and 40 GS/s for Agilent [14], and 18 GHz and 60 GS/s for LeCroy [15], respectively.

Hardware and software interleave methods are used in such high-speed real-time oscilloscopes to extend their temporal performance. The hardware interleave principle in a case where two ADCs are used is explained in Fig. 4. One ADC is clocked with a half cycle delay compared with the

other ADC (Fig. 4(a)). An equivalent twice sampling clock is achieved by superimposing the measurement results of the two ADCs, as shown in Fig. 4(b). The measured waveform, however, is distorted if the characteristics of the two ADCs do not exactly coincide or the clock delay is not aligned with high accuracy. This distortion is one of the main reasons for reduced effective number of bits (ENOB) in an interleaved ADC.

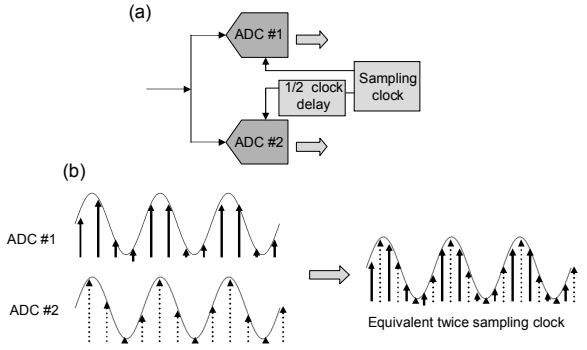

Figure 4. (a) Block diagram of hardware interleave using two ADCs. (b) Schematic of its interleave principle.

The highest sampling clock in a semiconductor ADC is 24 GS/s, which was achieved by an interleaved CMOS device. Although its vertical resolution was 6 bits, the ENOB was >4.1 up to 8 GHz and >3.5 up to the Nyquist frequency [16].

4. SFQ ADC FOR REAL-TIME OSCILLOSCOPE

High performance real-time oscilloscopes with higher sampling clocks will become more important in future photonic networks. They will be used for monitoring 100-Gbps ethernet performance and the transient phenomena of optical switches, analyzing the operation of ultra-high-speed photonic devices, and so on. Therefore, we are developing a flush type high-speed ADC using SFQ technology. This ADC could also be used in a digital coherent receiver [17].

We believe that an SFQ circuit is suitable for implementing in an ADC. First, it has a quite high-speed nature. Second, a superconductive quantum interference device (SQUID), which has almost the same configuration as an SFQ loop, has periodic input current characteristics, which results in a smaller number of comparators in the ADC. For instance, an *n*-bits SFQ ADC can be constructed with *n* comparators. On the other hand, a semiconductor device requires 2^n-*1* comparators to implement the *n*-bits ADC. In the case of 6 bits, an SFQ ADC needs at least 6 comparators but a semiconductor ADC requires 63. Third, it is quite easy to input an optical signal to SFQ circuits because an SFQ circuit is a low-impedance current-driven device.

A quasi-one-junction SQUID (QOS) has been used as a comparator in conventional SFQ ADCs [18]. A circuit diagram of the QOS and its input current versus output voltage characteristics is shown in Fig. 5. The output is periodically modulated by every SFQ going in and out of the QOS loop. The input signal current is divided by a resistance ladder, and each current enters an n^{th} bit QOS comparator, as shown in Fig. 6. For forming an ADC, some SFQ processing elements are added to the QOS comparators to process QOS output data, for example, an error correction circuit to eliminate the gray zone in a QOS threshold curve [19]. Kaplan et al. demonstrated an SFQ ADC with a 30-GS/s sampling clock without any interleaves [20].

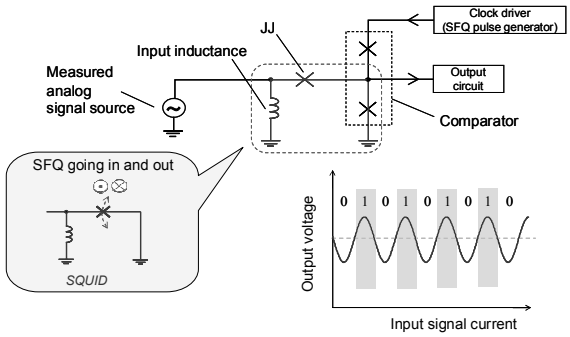

Figure 5. Schematic circuit diagram of superconductive comparator (QOS) and its input current versus output voltage characteristics.

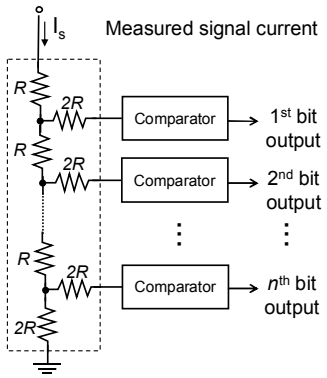

Figure 6. Schematic circuit configuration of *n*-bits SFQ ADC.

The conventional SFQ ADC has the drawbacks of non-linearity and asymmetry. We proposed a new design comparator that can solve these problems [21]. We investigated the performance of this new-type comparator using computer simulations. The resultant sampling clock dependence on J_c is shown in Fig. 7. The sampling clock and input bandwidth of the SFQ ADC were improved by increasing J_c. Kaplan et al. used a J_c of 2.5 kA/cm^2, but by introducing the new comparator design and increasing the J_c to 40 kA/cm^2, we improved the sampling clock to more than 150 GS/s without any interleaves. This sampling clock enables us to achieve a real-time oscilloscope that can monitor 40-Gbps digital waveforms with high accuracy.

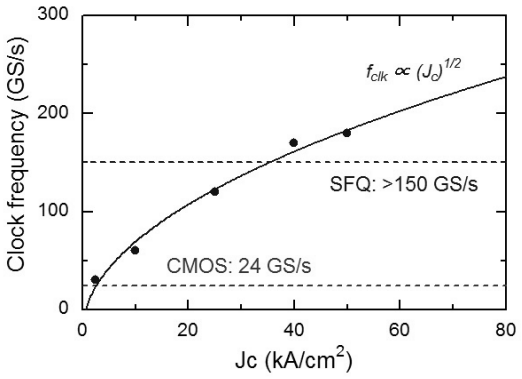

Figure 7. Sampling clock of SFQ ADC on J_c estimated by computer simulations.

5. CONCLUSION

Superconductive SFQ circuits are ultimate low-power consumption devices and will contribute remarkably to future photonic networks. A real-time oscilloscope is an attractive application for small-scale SFQ circuits. An SFQ ADC is the key component of this oscilloscope. The ADC is able to achieve more than 150 GS/s without any interleaves, estimated by computer simulations, and monitors 40-Gbps digital signals with high accuracy. On the other hand, the maximum sampling clock of a semiconductor ADC is 24 GS/s with interleaves. Moreover, the small number of comparators in the SFQ ADC will result in higher precision measurements, and high-rate output data from comparators can be processed by high-speed SFQ circuits. Superconductive devices have great potential for enabling breakthrough performances when applied in measurement instruments.

ACKNOWLEDGEMENTS

This work was supported by the New Energy and Industrial Technology Organization (NEDO) as a Development of Next-Generation High-Efficiency Network Device Project.

REFERENCES

[1] K. K. Likharev and V. K. Semenov, "RSFQ logic/memory family: A new Josephson-junction technology for sub-terahertz-clock frequency digital systems," *IEEE Trans. Appl. Supercond.*, 1, pp. 3–28, 1991.

[2] M. Hidaka, S. Nagasawa, K. Hinode, and T. Satoh, "Improvements in fabrication process for Nb-based single flux quantum circuits in Japan," *IEICE Trans. Electron.*, E91-C, pp. 318–324, 2008.

[3] S. Yorozu, Y. Kameda, H. Terai, A. Fujimaki, T. Yamada, and S. Tahara, "A single flux quantum standard cell library," *Physica*, C372-376, pp. 1471–1474, 2002.

[4] Y. Hashimoto, S. Yorozu, T. Miyazaki, Y. Kameda, H. Suzuki, and N. Yoshikawa, "Implementation and experimental evaluation of a cryocooled system prototype for high-throughput SFQ digital applications," *IEEE Trans. Appl. Supercond.*, 17, pp. 546–551, 2007.

[5] Y. Kameda, Y. Hashimoto, and S. Yorozu, "Design and demonstration of a 4x4 SFQ network switch prototype system and 10-Gbps bit-error-rate measurement," *IEICE Trans. Electron.*, E91-C, pp. 333–341, 2008.

[6] Y. Hashimoto, S. Nagasawa, T. Satoh, K. Hinode, H. Suzuki, T. Miyazaki, M. Hidaka, N. Yoshikawa, H. Terai, and A. Fujimaki, "Superconductive single-flux-quantum circuit/system technology and 40Gb/s switch system demonstration," Extended abstract on ISSCC 2008.

[7] H. H. Zappe, "Ultrasensitive analog to digital converter using Josephson junctions," *IBM Tech. Disc. Bull.*, 17, pp. 3053–3054, 1975.

[8] Y. Hashimoto, S. Yorozu, Y. Kameda, A. Fujimaki, H. Terai, and N. Yoshikawa, "Implementation of a 4x4 switch with passive interconnects," *IEEE Trans. Appl. Supercond.*, 13, pp. 535–538, 2003.

[9] M. Tanaka, T. Kondo, N. Nakajima, T. Kawamoto, Y. Yamanasi, Y. Kamiya, A. Akimoto, A. Fujimaki, H. Hayakawa, N. Yoshikawa, H. Terai, Y. Hashimoto, and S. Yorozu, "Demonstration of a single-flux-quantum microprocessor using passive transmission lines," *IEEE Trans. Applied Supercond.*, 15, pp. 400–404, 2005.

[10] H. Terai, Y. Hashimoto, S. Yorozu, A. Fujimaki, N. Yoshikawa, and Z. Wang, "The relationship between bit-error rate operating speed and circuit scale of SFQ circuits," *IEEE Trans. Applied Supercond.*, 15, pp. 364–367, 2005.

[11] K. Fujiwara, N. Nakajima, T. Nishigai, M. Ito, N. Yoshikawa, A. Fujimaki, H. Terai, and S. Yorozu, "Error rate test of large-scale SFQ digital circuit systems," *IEEE Trans. Applied Supercond.*, 15, pp. 427–430, 2005.

[12] Y. Hashimoto, S. Yorozu, T. Satoh, and T. Miyazaki, "Demonstration of chip-to-chip transmission of single-flux-quantum pulses at throughput beyond 100Gbps," *Appl. Phys. Lett.*, 87, pp. 022502–022504, 2005.

[13] http://www.tek.com/

[14] http://www.home.agilent.com/

[15] http://www.lecroy.com/

[16] P. Schvan, J. Bach, C. Falt, P. Flemke, R. Gibbins, Y. Glreshischev, N. Benhamida, D. Pollex, J. Sitch, S-C. Wang, and J. Wolczanski, "A 24 GS/s 6b ADC in 90 nm CMOS," Extended abstract on ISSCC 2008.

[17] D. S. Ly-Gagnon, S. Tsukamoto, K. Katoh, and K. Kikuchi, "Coherent detection of optical quadrature phase-shift keying signals with carrier phase estimation," *Journal of Lightwave Technol.*, 24, pp. 12–21, 2006.

[18] H. Ko and T. Van Duzer, "A new high-speed periodic-threshold comparator for use in a Josephson A/D converter," *IEEE J. Solid-State Circuits*, 23, pp. 1017–1021, 1988.

[19] S. V. Rylov and V. K. Semenov, "Wide-margin Josephson-junction A/D converter using redundant coding," *Electronics Letters*, 21, pp. 829–830, 1985.

[20] S. B. Kaplan, P. D. Bradley, D. K. Brock, D. Gaidarenko, D. Gupta, W.Q. Li, and S. V. Rylov, "A superconductive flash digitizer with on-chip memory," *IEEE Trans. Appl. Supercond.*, 9, pp. 3020–3025, 1999.

[21] Japanese patent 2007-340949.