A 6-Bit 1.6-GS/s Low-Power Wideband Flash ADC Converter in 0.13-μm CMOS Technology

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***Abstract*—In this work, a new termination technique for the averaging network of the flash analog-to-digital converter (ADC) input preamplifiers is devised. The proposed technique eliminates the over-range voltage headroom consumed by the dummy preamplifiers and therefore, the input capacitance and power dissipation of the ADC is reduced. This technique is applied to the design of a 6-bit 1.6-GS/s flash ADC in 0.13-μm CMOS technology. The measured peak INL and DNL are 0.42 LSB and 0.49 LSB, respectively. The ADC achieves an effective resolution bandwidth (ERBW) of 800 MHz and an SNDR of 30 dB at 1.45-GHz input signal frequency while consuming 180 mW.**

***Index Terms*—Analog-to-digital converters, averaging termination, CMOS analog integrated circuits, flash converter, offset averaging, resistor averaging network.**

I. Introduction

FLASH ADCs targeting optical communication standards were reported using SiGe BiCMOS technology in [1]–[3]. CMOS implementation of such designs involves two challenges. The first is to achieve a high sampling speed given the lower gain-bandwidth (lower f_t) of CMOS technology. The second is to handle the high bandwidth of the input signal with a certain accuracy. While the first problem can be relaxed using the time-interleaved architecture [4]–[7], the second problem remains as a main obstacle to CMOS implementation. Thus, the feasibility of a CMOS implementation of ADCs for such applications or other wideband applications depends mainly on achieving a very small input capacitance (large bandwidth) at the desired accuracy.

In the flash architecture, the input capacitance directly trades with the achievable accuracy. This tradeoff gets tighter with technology scaling as explained later. An effective way to relax this tradeoff is to use resistive offset averaging [8]. However, the resistor network used for averaging causes systematic nonlinearity at the ADC transfer characteristics edges. The common solution to this problem is to extend the preamplifiers array beyond the input signal voltage range [9]–[11]. However, this demands a corresponding extension of the flash ADC reference-voltage resistor ladder. Since the voltage headroom of the reference ladder is considered as the main bottleneck to the implementation of flash ADCs in deep-submicron technologies with reduced supply voltage [12], extending the reference voltage beyond the input voltage range is highly undesirable. Also, the elimination of this over-range voltage allows a larger least-significant bit. As a result, a higher input referred offset is tolerated and a significant reduction in the ADC input capacitance and power dissipation is achieved.

The triple-cross connection method proposed in [13] eliminates the over-range voltage of the reference ladder. However, it introduces negative transconductance at the preamplifiers array edges and produces a relatively large residual mean integral nonlinearity (INL) value, unless pre-distorted reference voltages are used.

In this paper, a termination technique that maintains the linearity of the ADC at the transfer characteristics edges is proposed. The proposed technique is based on using two interface amplifiers that get connected to the in-range reference ladder voltage taps, but has a shifted zero-crossing point. Thus, this termination technique does not require any over-range voltage headroom and does not introduce negative transconductance.

This paper is organized as follows. In Section II, a formulation of the bandwidth-accuracy tradeoff of flash ADCs is driven and the effect of technology scaling is discussed. The problem of averaging network termination is discussed in Section III, while in Section IV, the new termination technique is proposed. The design of a 6-bit 1.6-GS/s flash ADC that uses the proposed technique is presented in Sections V and VI. Finally, measurement results are reported in Section VII.

II. The Bandwidth-Accuracy Tradeoff of Flash ADCs

The bandwidth of high speed flash ADCs is mainly determined by the track-and-hold (T/H) circuit at its input [14]–[16]. Thus the input capacitance of the ADC preamplifiers array that load the T/H circuit should be reduced for wideband applications. The input referred static offset RMS value of the flash ADC preamplifiers is given by [17]

$$\sigma_{\text{offset}} \approx \frac{A_{\text{Vt}}}{\sqrt{W \cdot L}} \tag{1}$$

where A_{Vt} is the mismatch coefficient for FET threshold voltage, and W and L are the width and length of the preamplifier input differential pair transistors, respectively. Equation (1) reveals that to reduce the offset of the preamplifiers, the area of the FET transistors needs to be increased. This would increase the input capacitance of the preamplifiers, and hence would result in a reduction of the input signal bandwidth. Therefore, the offset-area tradeoff leads to a bandwidth-accuracy tradeoff.

The averaging technique can ease this bandwidth-accuracy tradeoff. In this technique, adjacent preamplifiers outputs are connected with resistors. The amount of offset reduction due

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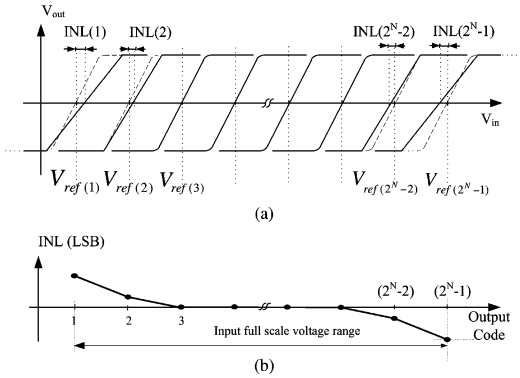

Fig. 1. Preamplifiers array edge problem. (a) Transfer characteristics of preamplifiers. (b) INL versus output code.

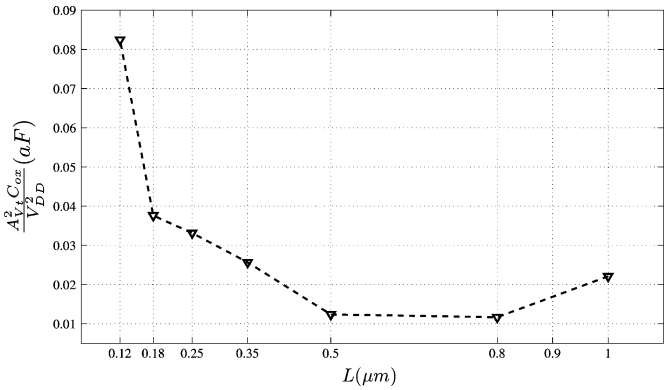

Fig. 2. $(A_{\rm Vt}^2 C_{\rm ox}/V_{\rm DD}^2)$ versus technology minimum feature size (L).

to averaging, ξ, depends on the ratio of the averaging resistor value, R_1, to the preamplifier output resistance, R_0. Decreasing (R_1/R_0) leads to more reduction in the RMS value of the offset voltage. However, the zero-crossing points of the preamplifiers at the array edges are pulled by the averaging resistors towards the array. This results in an increase in the mean values of INL(j) at the two edges of the array (Fig. 1). To mitigate this effect, dummy preamplifiers are added at the two edges of the preamplifiers array beyond the input signal range. However, the over-range dummies reduce the available voltage headroom for the input signal. The loss in the voltage headroom due to dummies can be expressed as

$$\eta = \frac{V_{\rm sig}}{V_{\rm sig-max}} \tag{2}$$

where $V_{\rm sig}$ is the available voltage headroom for the input signal and $V_{\rm sig-max}$ represents the signal voltage headroom plus the over-range voltage. In a previous design, the over-range voltage is about 28% of $V_{\rm sig}$ [9].

Based on (1)–(2), a measure for the accuracy of an ADC that uses averaging is derived as

$$\left(\frac{\sigma'_{\rm offset}}{\Delta}\right)^2 \approx \frac{A_{\rm Vt}^2}{W \cdot L}\frac{2^{2N}}{V_{\rm DD}^2}\frac{1}{\eta^2\alpha^2\xi^2} \tag{3}$$

where $\sigma'_{\rm offset}$ is the preamplifier input referred offset RMS values after averaging, Δ represents the least-significant-bit (LSB), and α accounts for the voltage headroom consumed by the biasing circuit of the reference ladder.

The input capacitance of such an ADC is given by

$$C_{\rm in} \approx \frac{2}{3}C_{\rm ox}WL\frac{1}{\rho m}(2^N - 1). \tag{4}$$

In (4), $C_{\rm ox}$ is the gate capacitance per unit area, m represents the interpolation factor and is equal to one if no interpolation is used, while ρ is the number of preamplifiers within signal range divided by the total number of preamplifiers including dummies. Equation (3) and (4) can be combined together, yielding a representation of the *bandwidth–accuracy* tradeoff of flash ADCs

$$\begin{aligned}\kappa &\equiv C_{\rm in}\left(\frac{\sigma'_{\rm offset}}{\Delta}\right)^2 \\ &\approx \left(\frac{A_{Vt}^2 C_{\rm ox}}{V_{\rm DD}^2}\right)\left(\frac{2}{3}\frac{2^{2N}(2^N-1)}{\eta^2\rho\alpha^2(\xi^2 m)}\right).\end{aligned} \tag{5}$$

For many applications, minimizing the input capacitance at the same target accuracy (minimizing κ) is a main design objective. An example of such application is flash ADCs designed for wideband communication systems, where large input bandwidth (and hence small $C_{\rm in}$), in addition to a certain accuracy, are dictated by system specifications.

The maximum sampling rate of flash ADCs is limited by its preamplifiers and comparators overdrive recovery time [9], which is a function in the gain–bandwidth (GBW) offered by the technology. Therefore as technology minimum feature size scales to lower values, higher sampling rates are achieved at a given power consumption [18]. On the other hand, the effect of technology scaling on the bandwidth-accuracy tradeoff (κ) can be studied by plotting $(A_{\rm Vt}^2 C_{\rm ox}/V_{\rm DD}^2)$ for different CMOS technologies (Fig. 2). Typical values for $A_{\rm Vt}$, $t_{\rm ox}$ and $V_{\rm DD}$ can be found in [19]. The rest of the parameters in the RHS of (5) are technology independent.[1] Fig. 2 shows that for technologies with minimum feature size less than 0.5 μm, κ increases with technology scaling. The reason behind this is that the continuous reduction in the supply voltage of technologies beyond 0.5 μm almost cancels out the improvement expected due to the enhancement in the matching properties of the FET transistor as both $A_{\rm Vt}$ and $V_{\rm DD}$ scale nearly with the same factor. Since accuracy depends on the *ratio* of the offset voltage to the LSB, approximately the same FET area is needed in different submicron technologies to achieve a certain accuracy. Thus, the increase in the value of $C_{\rm ox}$ with scaling would lead to a net increase in κ. Hence, as technology scales, a tighter bandwidth-accuracy tradeoff is obtained and optimizing the technology-independent terms in (5) becomes crucial.

Equation (5) reveals that the higher the value of η, the lower the input capacitance at the same accuracy. This fact is exploited in this work to reduce κ as the averaging network is terminated without consuming over-range voltage, and hence $V_{\rm sig}$ is equal to $V_{\rm sig-max}$.

III. Coping With the Lower Supply Voltages in Deep-Submicron Technologies

The loss of signal swing due to over-range dummy preamplifiers makes averaging less suited to low-voltage designs [20]

[1]The parameter α has a slight dependence on technology, but this can be ignored for simplicity.

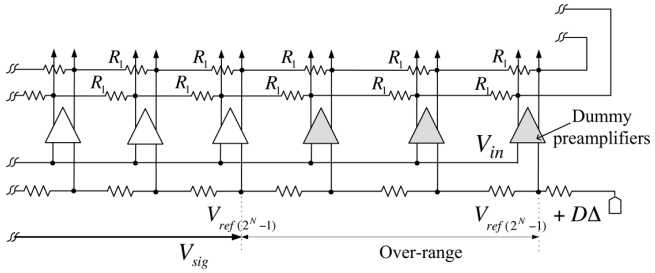

Fig. 3. Averaging network termination using dummy preamplifiers.

or ultra-deep-submicron technologies that have a low nominal supply voltage. Thus, different solutions have been proposed to reduce this voltage over-range penalty.

The art in [13] uses triple cross-connection and two interface amplifiers together with pre-distorted reference voltages, generated using digitally controlled current sources. This method reduced the peak mean value of INL from 5 LSB to 0.3 LSB according to simulations reported in [13]. The triple cross-connection technique does not need over-range voltage. However, the pre-distorted reference ladder increases the design complexity. In [16], the pre-distorted reference ladder was eliminated, and triple cross-connection, in addition to interface amplifiers were used. Nevertheless, the resulting peak mean value of INL obtained by simulation was dropped from 4.5 LSB, in the case of abrupt termination, to 0.5 LSB only. This value is relatively high as random variations would still add to it to give the total INL error value.

A major drawback of the triple cross-connection method is that the differential output of the interface amplifier is cross-connected to the outputs of the regular array preamplifiers through the averaging network. Hence, the interface amplifier introduces negative transconductance at the preamplifiers array edges. As a result, the effective transconductance, gain, and gain-bandwidth of the preamplifiers at array edges are lowered. To alleviate this effect, the zero-reference point used for interface amplifier in [16] is chosen to be three steps away from the end of the reference ladder. Nonetheless, this limits the amount of residual INL reduction that can be achieved.

A different solution is proposed in [21], where the value of the over-range voltage needed is reduced by altering the values of the edge resistors in the averaging network. For the design reported in [21], a 20% over-range voltage was consumed and a supply of 1.95 V was used for the analog part of the ADC in 0.18-μm CMOS technology. Thus, the supply voltage is still higher than the technology nominal supply voltage.

The termination technique presented in the next section is a modification to that reported in [21]. It neither consumes over-range voltage headroom nor introduces negative transconductance and therefore, provides an efficient solution to the problem of averaging network termination.

IV. The Proposed Termination Technique

The concept of the proposed termination circuit is introduced in Section IV-A, while the details of the circuit implementation are presented in Section IV-B.

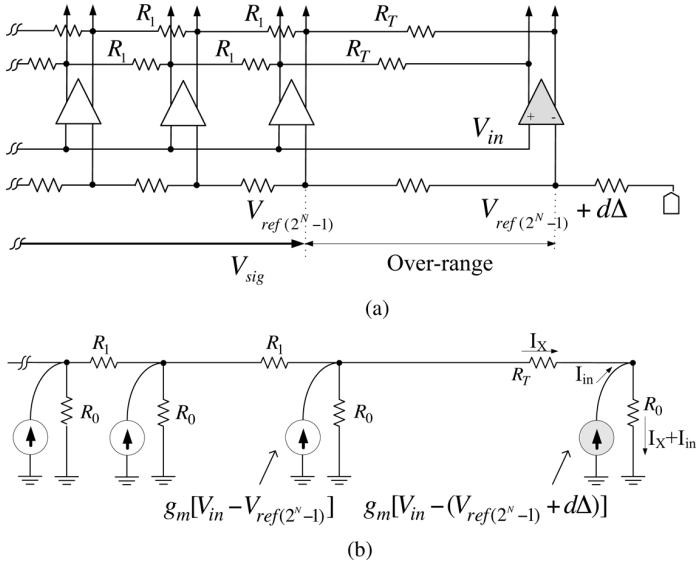

Fig. 4. The Termination technique of [21]. (a) Actual circuit. (b) Simplified model.

A. Concept

In Fig. 3 only one edge of the preamplifiers array is shown, and it is assumed that D number of dummy preamplifiers per edge are used to eliminate the edge problem. The number of needed dummy preamplifiers is reduced by altering the value of the averaging resistors at the edge, as suggested in [21] [Fig. 4(a)]. The output voltage of the dummy amplifier in Fig. 4(a) is described as [Fig. 4(b)]

$$V_{\text{dummy}} = [g_m[V_{\text{in}} - (V_{\text{ref}(2^N-1)} + d\triangle)] + I_x]R_0 \quad (6)$$

where $V_{\text{ref}(2^N-1)}$ is the maximum *in-range* reference voltage, I_x is the differential current following through the termination resistors R_T, and d is an integer less than D. To eliminate the over-range reference voltage $(V_{\text{ref}(2^N-1)} + d\triangle)$, the interface amplifier of Fig. 5(a) together with the in-range reference voltage $(V_{\text{ref}(2^N-1)} - d\triangle)$ are used instead. The output voltage of the interface amplifier is given by [Fig. 5(b)]

$$\begin{aligned} V_{\text{interface}} &= [g_m[V_{\text{in}} - V_{\text{ref}(2^N-1)}] \\ &\quad + g_m[(V_{\text{ref}(2^N-1)} - d\triangle) - V_{\text{ref}(2^N-1)}] + I_x]R_0 \\ V_{\text{interface}} &= [g_m[V_{\text{in}} - (V_{\text{ref}(2^N-1)} + d\triangle)] + I_x]R_0. \end{aligned} \quad (7)$$

So $V_{\text{interface}}$ is equal to V_{dummy} in (6) and an interface amplifier with the connectivity shown in Fig. 5 can replace the structure of Fig. 4.

Unlike the work in [16] and [13], the output of the interface amplifier, $V_{\text{interface}}$, does not decrease with the increase in V_{in}. That is to say, the proposed interface amplifier does not add negative transconductance. The interface amplifier principal of operation is to shift its zero-crossing point by adding a constant voltage to its output.

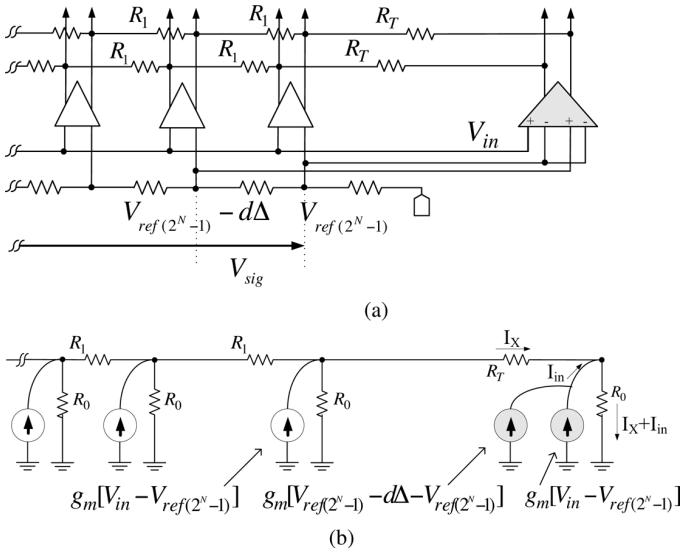

Fig. 5. The proposed termination scheme. (a) Actual circuit. (b) Simplified model.

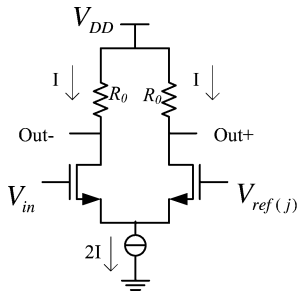

Fig. 6. The preamplifier.

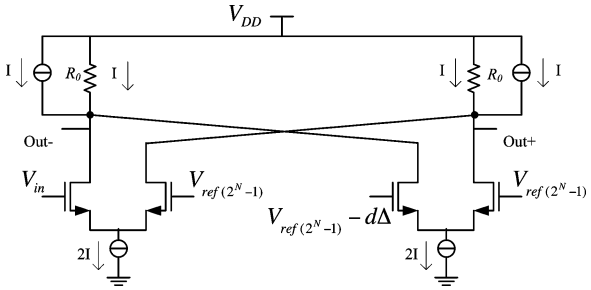

Fig. 7. The interface amplifier.

B. Circuit Level Implementation

Flash ADC preamplifiers are usually implemented as a simple differential pair with resistive loads (Fig. 6) [20], [21]. The interface amplifier shown in Fig. 7 should have the same output impedance, gain, GBW, and output common mode voltage as that of the array preamplifiers. Therefore, (W/L) of the input differential pair and the tail current sources of the interface amplifier are set equal to that of the preamplifiers. As a result, both the preamplifiers and the interface amplifier would have equal transconductance (g_m). The current source connected in parallel to the load resistor R_0 is designed to have a much larger output impedance than the load resistor R_0. Hence, both circuits would have nearly the same output impedance (R_0) and gain $(g_m R_0)$. Assuming that the load capacitance is dominated by the input capacitance of the next stage, the two circuits would have approximately equal bandwidth. The DC current flowing through (R_0) in both circuits is I, so the output common mode voltage of both circuits is equal to $V_{\rm DD} - IR_0$.

Typically, the input referred RMS offset value of the interface amplifier of Fig. 7 would be $\sqrt{2}$ times the offset value of the regular preamplifier, if they are designed to have the same input capacitance. This would degrade the input referred offset at the preamplifiers array edges. Therefore, in actual implementation the interface amplifier differential pairs are sized such that

$$\left(\frac{W}{L}\right)_{\rm interface} = \left(\frac{\sqrt{2}W}{\sqrt{2}L}\right)_{\rm preamp}. \tag{8}$$

Hence, the interface amplifier would have the same RMS offset as the regular preamplifier but double its input capacitance.[2]

The circuits shown in Figs. 6 and 7 assumed single-ended input signal for simplicity. In actual implementation, all the circuits are fully differential.

V. The Analog Front-End

A. Track-and-Hold Circuit and the Reference Voltage Resistor Ladder

An open-loop T/H circuit is incorporated in the analog front-end to enhance the dynamic performance of the ADC. The T/H circuit consists of an NMOS sampling switch, a dummy switch and a 153-fF MIM capacitor. The input voltage range of the flash ADC is set to 0.84 $V_{\rm p-p}$ differential, while the common mode voltage of the input signal is set to 0.27 V to lower the T/H sampling switch resistance. A source follower buffer proceeding the T/H circuit is used to shift the input common mode voltage to 0.88 V. A replica source follower is used to bias the N-well of the source follower main PMOS transistor as in [13]. The pseudo differential source follower buffer consumes 10 mA and achieves 3rd harmonic distortion (HD3) of -53 dBc.

The reference voltages of the flash ADC are generated using an 80-Ω serpentine structure of Metal 3. The low resistance of the resistor ladder reduces the reference ladder signal feedthrough problem.

B. Preamplification Stages

In order to maximize the bandwidth of flash ADCs preamplification stage, it is commonly realized using low gain amplifiers. A cascade of two to four stages of these low-gain amplifiers is usually needed to suppress the relatively large dynamic offset of the comparators [13], [21], [22]. In this design, four preamplification stages were used. A $\times 2$ averaging interpolating network connects consecutive stages as shown in Fig. 8. For every stage, the value of the averaging resistors R_1 is selected 1.5 times larger than the value of the preamplifier load resistance R_0. For the first preamplifiers stage R_T is set equal to $(R_1 - R_0)$ [21]. Table I lists the voltage gain, 3-dB bandwidth, input referred offset RMS value, and the offset reduction ratio for each of the

[2]The interface amplifier used in triple cross-connection method also has a larger input capacitance than that of the regular preamplifiers [13].

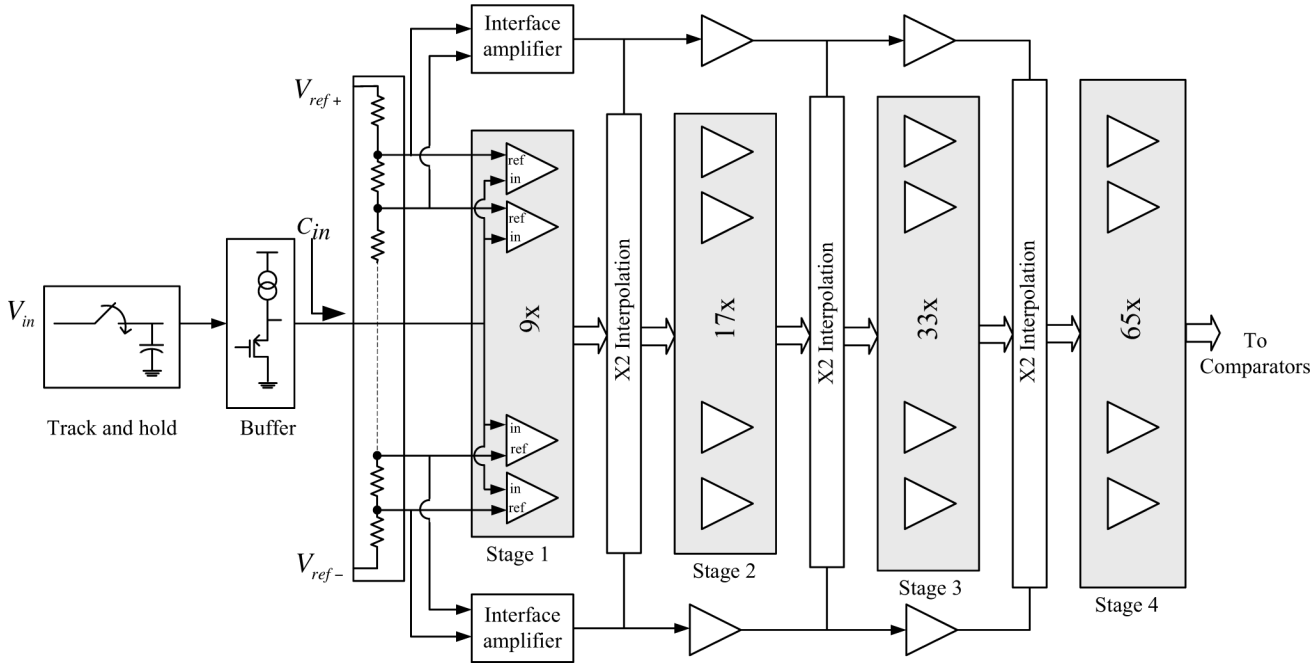

Fig. 8. Analog front-end of the ADC.

TABLE I
VOLTAGE GAIN, 3-dB BANDWIDTH, INPUT REFERRED OFFSET, AND OFFSET REDUCTION FACTOR OF EACH PREAMPLIFIERS STAGE

	Voltage gain (A)	3-dB bandwidth in GHz	Input referred offset RMS value without averaging (σ) in mV	Offset reduction ratio due to averaging (ξ)
First Stage	2.7	3.7	3.94	1.6
Second stage	3.2	6.1	6.51	1.6
Third stage	2.9	7.7	11.92	2
Fourth stage	2.9	5.2	15.37	–

four stages. The total input capacitance of the preamplification stage is 380 fF, while the total input referred offset RMS value due to the four preamplifiers stages and the digital back-end comparators is equal to

$$\sigma'_{\text{offset}-\text{total}} = \sqrt{\frac{\sigma_1^2}{\xi_1^2} + \frac{\sigma_2^2}{\xi_2^2 . A_1^2} + \frac{\sigma_3^2}{\xi_3^2 . \prod_{i=1}^{i=2} A_i^2} + \frac{\sigma_4^2}{\prod_{i=1}^{i=3} A_i^2} + \frac{\sigma_{comp}^2}{\prod_{i=1}^{i=4} A_i^2}} = 3.1\ \text{mV}_{\text{rms}} \quad (9)$$

where σ_i and A_i are the input referred RMS offset and voltage gain of the ith preamplifiers array, respectively, σ_{comp} is the dynamic offset of the comparators, and ξ_i is the offset reduction ratio due to offset averaging of the ith preamplifiers array.

Simulations show that the proposed termination technique limits the maximum mean value of INL to 0.15 LSB (compared to 4.13 LSB in the case of abrupt termination). So over-range voltage is eliminated without deteriorating the linearity of the ADC.

For this design, the reference voltage ladder needs to extend along the 9 preamplifiers of the first stage, while the technique proposed in [21] requires the reference ladder to extend along 11 preamplifiers (the 9 preamplifiers processing the input signal $+2$ dummy preamplifiers). Therefore, the increase in η due to over-range voltage elimination is equal to $(11/9)$. The LSB, as well as the target $\sigma'_{\text{offset}-\text{total}}$, are increased by the same value keeping the ADC accuracy unaltered. It follows from (1) and (9) that the input capacitance of each of the preamplifiers arrays is reduced by a factor of $(9/11)^2$. Hence, a 33% reduction in the input capacitance of the second, third and fourth preamplifiers arrays is achieved. For the first stage, the interface amplifier has double the input capacitance of the preamplifiers. Hence, the net reduction in input capacitance of the first stage due to the proposed technique is 20% compared to the averaging termination technique of [21]. Since each preamplifier array represents the load of the preceding array, lowering the input capacitance of the preamplification stages results in an increase in the GBW of these stages at the same power dissipation[3]. In other words, the target GBW can be obtained with less power. Thus, the proposed technique not only reduces the ADC input capacitance, but also reduces the power consumption of the analog front-end.

VI. THE DIGITAL BACK-END

A block diagram for the digital back-end is shown in Fig. 9. The output of the last preamplification stage is fed to an array of low kick-back latched comparators [22] followed by two arrays of CMOS latches [23]. The latch of each comparator stage

[3]This is achieved by reducing the value of W and L with the same ratio keeping W/L the same.

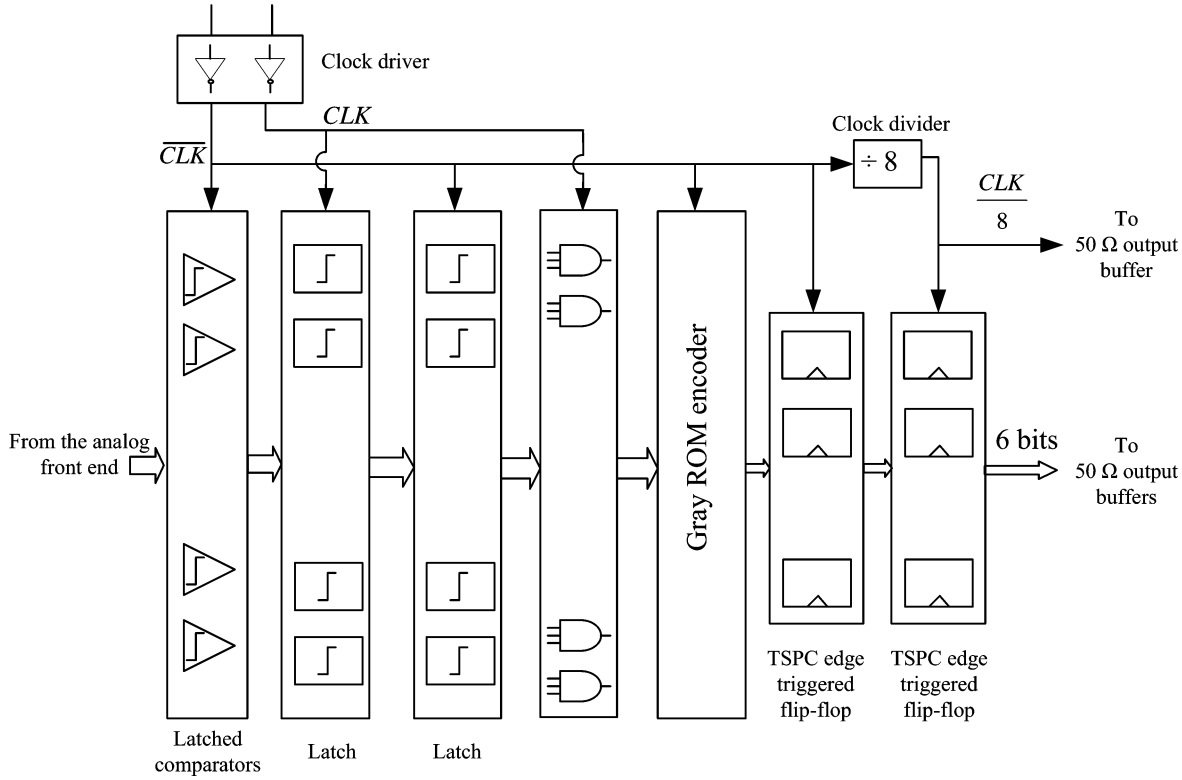

Fig. 9. Digital back-end of the ADC.

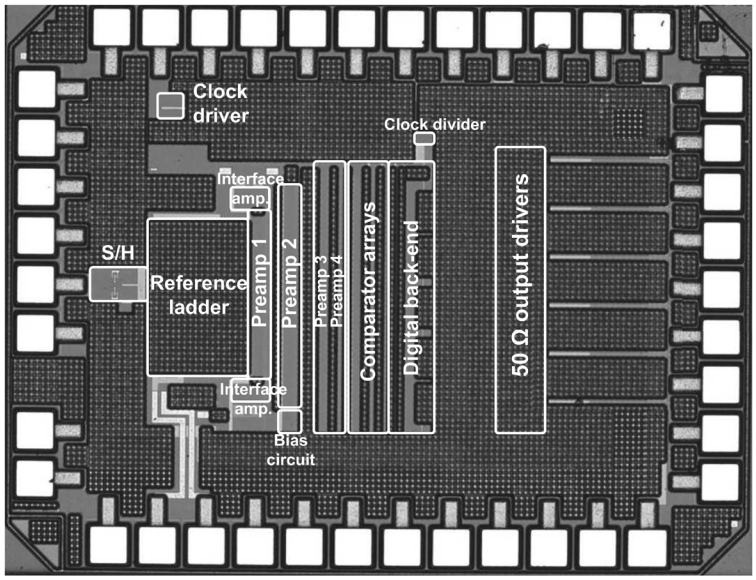

Fig. 10. Microphotograph of the chip.

has a GBW approximately equal to 16 GHz. Cascading latches provides a power efficient way to increase the available time for regeneration, and hence reduce metastability errors [24].

A three-input clocked NAND gate is used for first order bubble suppression and to transform the thermometer code to 1-of-*N* code that selects one word of a pre-charged Gray ROM encoder. The output of the ROM is held by a true single phase clocked (TSPC) flip-flop for a whole clock period.

The output digital stream is down-sampled by a factor of 8 to allow acquisition by the logic analyzer. The divide by 8 clock is generated on-chip to avoid sampling uncertainty due to supply bounce.

VII. Measurements

The designed ADC was fabricated in 0.13-μm 8-metal single-poly CMOS technology. A microphotograph of the chip

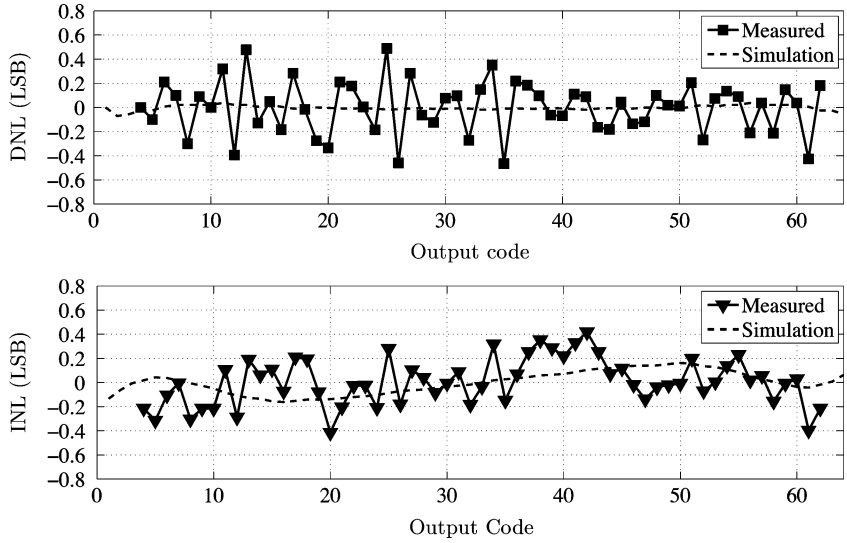

Fig. 11. Measured INL and DNL at 1.6 GS/s.

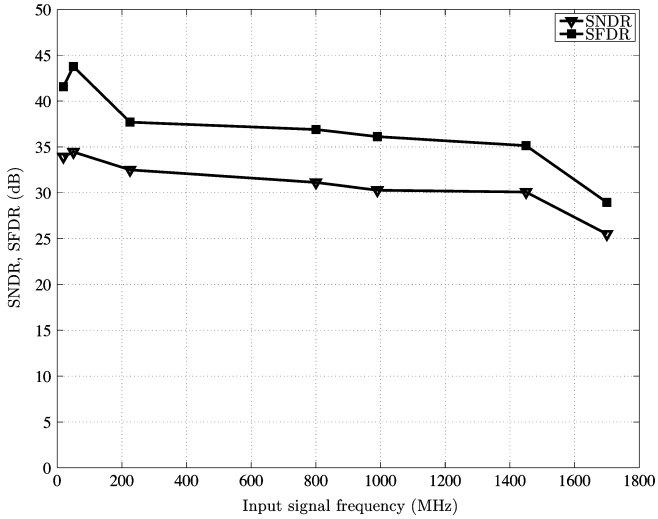

Fig. 12. Measured SNDR and SFDR at 1.6 GS/s.

is shown in Fig. 10. The active area of the design occupies 0.42 mm^2. On-chip 0.12-nF and 0.4-nF capacitors are added to decouple the analog and digital supplies, respectively. The analog front-end is surrounded by guard ring connected to the analog ground to isolate it from the digital noise. The chip was mounted on a standard 4-layer PCB and directly wire-bonded to the board for testing. The differential clock and input signal are generated using phase splitters and terminated on-chip with 50-Ω poly resistors.

The ADC nonlinearity is measured using the histogram method at 1.6 GS/s. Fig. 11 shows the measured INL and differential nonlinearity (DNL) values for a typical chip together with the simulation results for the mean values. The maximum INL and DNL errors are found to be 0.42 LSB and 0.49 LSB, respectively.

The dynamic performance of the ADC at 1.6 GS/s is shown in Fig. 12. The ADC achieves an SNDR of 34.5 dB at 50-MHz input signal. The effective resolution bandwidth (ERBW) is equal to 800.04 MHz. However, the SNDR remains higher than 30 dB until an input signal frequency of 1450 MHz. The whole ADC operates from a 1.5-V supply. The analog portion of the ADC consumes 81 mA, while the digital circuitry consumes 35.8 mA. The total power dissipation of the ADC including reference ladder is 180 mW. Therefore, the ADC achieves a figure-of-merit

$$(\mathrm{Power}/(2^{\mathrm{ENOB,DC}} \cdot 2 \cdot \mathrm{ERBW})) = 2.6\mathrm{pJ/conv}. \quad (10)$$

Fig. 13 plots the input signal frequency at 5 effective number of bits (ENOB) versus sampling frequency for previously reported 6-bit flash ADCs together with the ADC of this work, while Fig. 14 compares the figure-of-merit of these ADCs. It can be concluded from Figs. 13 and 14 that the designed ADC achieves a superior dynamic performance combined with low power dissipation.

VIII. Conclusion

The limited supply voltage offered by future technologies will outweigh the accuracy improvement due to its superior MOS matching properties. Therefore, optimizing the bandwidth-accuracy tradeoff of flash ADC is essential to advance its state of the art.

A technique to cancel out the over-range voltage headroom of the flash ADC reference ladder has been proposed. This permits a larger value for the ADC LSB, and thus, the matching requirements of the preamplifiers arrays are relaxed. As a result, a reduction in ADC input capacitance and power dissipation is achieved. Eliminating the over-range voltage also makes flash ADCs more amenable for integration in deep-submicron technologies.

A 6-bit 1.6-GS/s flash ADC that incorporates the proposed technique is implemented in 0.13-μm CMOS technology. The ADC achieves an ENOB of 5.44 bits at low input frequencies and a FOM of 2.6 pJ/conv.

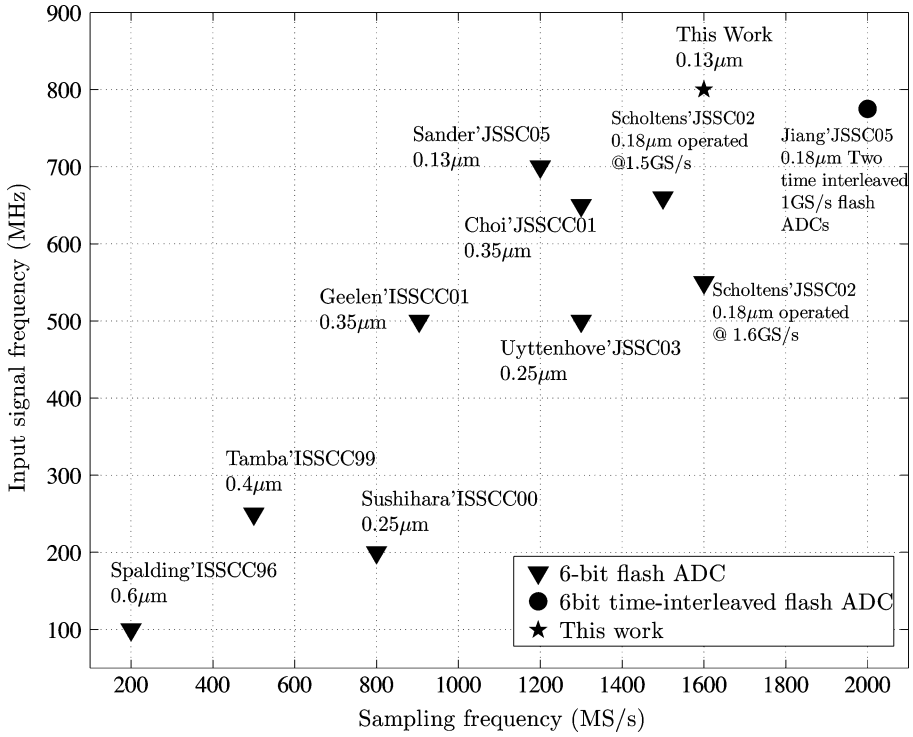

Fig. 13. The input signal frequency at 5 ENOB versus sampling frequency for previously reported 6-bit flash ADCs and this work.

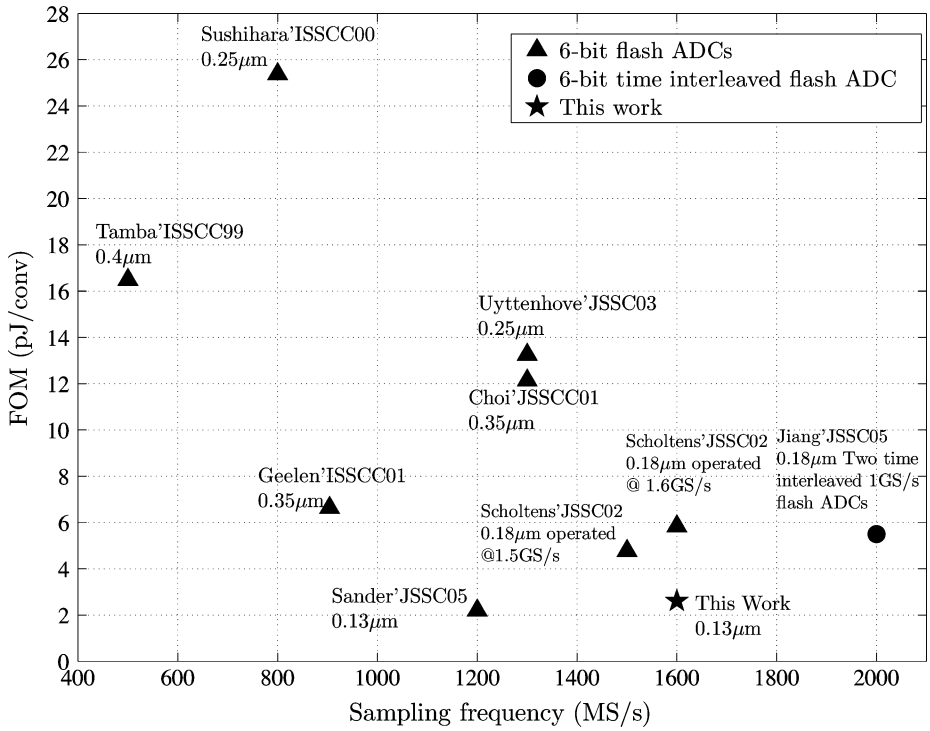

Fig. 14. Figure-of-merit for previously reported 6-bit ADCs and this work.

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