A 90 nm CMOS Broadband Multi-Mode Mixed-Signal Demodulator for 60 GHz Radios

Kevin Chuang, *Student Member, IEEE*, David Yeh, *Member, IEEE*, Francesco Barale, *Student Member, IEEE*, Patrick Melet, *Member, IEEE*, and Joy Laskar, *Fellow, IEEE*

***Abstract*—In this paper, a low-power high-speed fully integrated mixed-signal quadrature demodulator with an embedded multi-gigabit modem in 90 nm CMOS technology is presented. A wide dynamic-range automatic gain control (AGC) is implemented to avoid clipping distortion experienced by the baseband ADCs. By reusing the power detector circuit within the AGC, analog signal processor is introduced to recover OOK modulated signals up to 2.5 Gb/s for an additional power consumption of 7.5 mW. Integrated with ultra-low-power, 3 mW, 3 GS/s, 3-bit ADCs and high-speed digital modem, the system requires neither external synchronization controls nor processing to demodulate BPSK modulated signals up to 3.5 Gb/s and DBPSK modulated signals up to 1.3 Gb/s. The baseband modem incorporates a mixed-signal, timing-recovery loop to sample the symbols at the optimum SNR based on a high-speed Gardner timing-error detector for an additional power consumption of 14 mW. The analog front-end consists of IQ mixers, a 13 GHz QVCO, frequency synthesizers, and a baseband AGC for an overall power consumption of 52 mW. The entire receiver chip occupies an area of 1.275×1.19 mm^2. To the best of authors' knowledge, this demonstrates the maximum throughput at the minimum power budget and highest level integration among all published wireless multi-gigabit, multi-mode, mixed-signal CMOS receivers.**

***Index Terms*—90 nm, ADC, AGC, bit synchronizer, BPSK, CMOS, DBPSK, high-Speed, low-Power, mixed-signal, modem, multi-gigabit, OOK.**

I. Introduction

INCREASED consumer demands and technological improvements have made radio-based electronic devices essential in our society. With the rapid advancements in semiconductor technologies, CMOS wireless communication transceivers in the millimeter-wave regime have recently become more versatile, portable, and inexpensive [1]–[3]. However, plagued by the short lifetime of batteries, low-power consumption has become an extremely important specification in developing mobile communication devices [4], [5]. Such systems generally require both low-power broadband demodulator and high-speed ADCs for portable multi-gigabit applications.

One of the key advantages of millimeter-wave communication technology is the large amount of spectral bandwidth available, which is enough to transmit a gigabit of data even with the simplest modulation schemes, such as on-off keying (OOK), binary phase-shift keying (BPSK), or differential BPSK (DBPSK). In 2001, the Federal Communications Commission (FCC) allocated a continuous block spectrum of 7 GHz in the 60 GHz band for license-free operation in the United States [6]. For the first time, sufficient spectrum has made possible multi-gigabit radio frequency (RF) links. This is attractive for security applications because oxygen molecules absorb electromagnetic energy in this band [7]. The additional oxygen absorption loss in addition to the free space path loss allows multiple 60 GHz data links to operate in close proximity with each other. Shortly after that, in 2003, the FCC opened up E-band (known as the 71–76, 81–86, and 92–95 GHz for carrier-class point-to-point digital backhaul applications) for licensed operation [8].

This paper expands our previous work [9] by describing, analyzing, and developing a fully integrated CMOS broadband quadrature demodulator with embedded mixed-signal signal processors that are compatible with OOK, BPSK, and DBPSK modulation schemes. Section II of this paper introduces system-level architecture and explains the requirements of the ADC resolution based on desired modulation scheme. Section III discusses each individual component in further details. The measurement results are discussed and analyzed in Section IV, followed by a conclusion in Section V.

II. System Architecture

A. Modulation Scheme

The required performance of a wireless receiver is determined by the intrinsic and extrinsic noise sources. Typically, the extrinsic sources include TX noise leakage in RX band, intermodulation distortion, quantization noise, and imperfectly filtered interference [10]. The noise figure (NF) of a receiver is normally determined by the low-noise amplifier (LNA) following the on-chip antenna in any radio environment. To realize a low-cost, single-chip, 60 GHz transceiver, the state-of-the-art millimeter-wave, front-end components are first reviewed. The results in Table I indicate that a millimeter-wave 90 nm CMOS receiver front-end, consisted of a LNA, mixer, and frequency synthesizer, is able to output a conversion gain of 22 dB and

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K. Chuang is with the School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA 30308 USA (e-mail: kevinchuang@gatech.edu).

D. Yeh, F. Barale, P. Melet, and J. Laskar were with the School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA 30308 USA. D. Yeh and P. Melet are now with the Samsung Design Center, Atlanta, GA 30308 USA.

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TABLE I
60 GHz MILLIMETER-WAVE FRONT-END COMPONENTS

Component	Specification	Parameter	Units	Ref
LNA	Gain	20.4	dB	[11]
	Noise Figure	8.6	dB	
RX	Gain	22	dB	[12]
	Noise Figure	8.4	dB	

DSB NF of 8.4 dB at 61.5 GHz. The receiver minimum sensitivity, related to this information, can be expressed as

$$P_{\mathrm{MIN}} = 10\log(kT \cdot BW) + NF + LM + SNR_{\mathrm{MIN}} \quad (1)$$

where k is the Boltzmann constant, T is the absolute temperature in Kelvin, BW is the bandwidth occupied by the RF signal, NF is the noise figure of the receiver, LM is the link margin, and SNR_{MIN} is the minimum signal-to-noise ratio (SNR) required for the chosen modulation. To achieve a specific level of reliability in terms of bit-error rate (BER), the baseband SNR required for a suitable modulation scheme can be calculated as

$$SNR_{\mathrm{ADC}} = P_{\mathrm{IN}} - 10\log(kT \cdot BW) - NF \quad (2)$$

where P_{IN} is the received input power level. A raw BER before error correction of 1E-06 is typically desirable for wireless communication systems [13]. For BPSK modulation, the theoretical SNR required for a BER of 1E-06 is 10.5 dB. Considering a RF bandwidth of 3.5 GHz, zero link margin, and a RX NF listed in Table I, the receiver minimum sensitivity is computed as -59.7 dBm. The ADC resolution required for a given modulation scheme is then derived using (2). In this case, P_{IN} is assumed the minimum sensitivity of a receiver. Therefore, the required baseband SNR would be 10.5 dB, which requires a minimum ADC resolution of 2 bits. For an uncompressed high definition multimedia interface (HDMI) video streaming, a BER of 1E-08 is acceptable.

Figs. 1 and 2 show the BER simulation versus ADC resolution with mixed-signal synchronization architectures for both coherent and non-coherent demodulators. As mentioned in [9] the coherent digital signal processor (DSP) estimates and corrects the phase and frequency offsets between the intermediate frequency (IF) local oscillator (LO) and the modulated IF input carrier. On the other hand, the proposed non-coherent demodulator first synchronizes the ADC sampling clock to the middle of baseband symbols by incorporating a timing-recovery loop. When the baseband SNR is optimized, the DSP differentially demodulates DBPSK by complex multiplication. Here, a theoretical BER curve is plotted against various BER curves obtained using different ADC resolutions. As seen from the graphs, BER degradation due to the quantization noise and nonlinearity of 3-bit and 4-bit ADCs are similar and can be negligible. The trade-off between power and speed conveys 3-bit architecture over any higher resolution systems. In addition, a review of state-of-the-art 6-bit ADCs with sampling speeds above 3 GS/s has shown a power budget of more than 200 mW when operating two 6-bit ADCs in a quadrature receiver [14]. As demonstrated in Section III, a 3-bit, 3-GS/s ADC can be implemented with significantly lower power dissipation

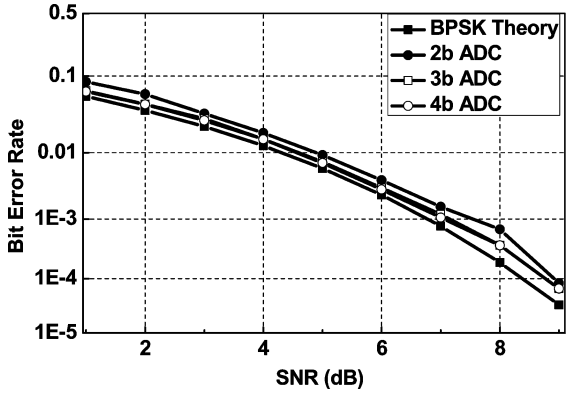

Fig. 1. BER simulation versus ADC resolution for a mixed-signal coherent demodulator.

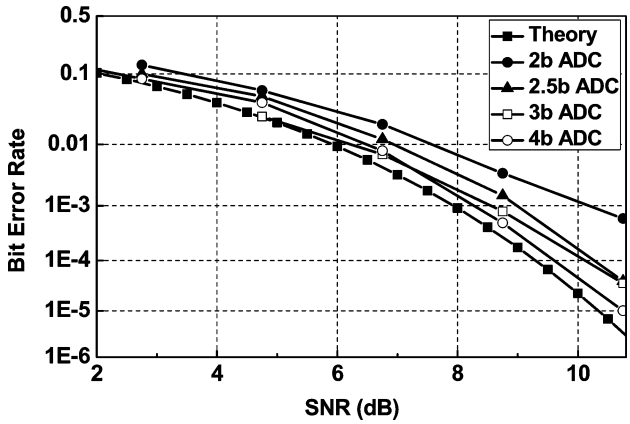

Fig. 2. BER simulation versus ADC resolution for a mixed-signal non-coherent demodulator.

(3 mW) and integrated with a baseband modem to offer a novel, low-power, multi-gigabit demodulator solution.

B. Receiver Architecture

As shown in Fig. 3, the quadrature demodulator is implemented to downconvert a modulated IF carrier at 13 GHz to baseband using double-balanced passive mixers. The LO is generated by the quadrature voltage-controlled oscillator (QVCO) integrated with a frequency synthesizer. Baseband variable-gain amplifiers (VGA) are implemented with automatic gain control (AGC) and DC-offset compensation. The analog signal processor (ASP) reuses the power detector circuit within the AGC loop to detect the OOK signal. The signal path between the differential-to-single-ended amplifier and the ADC is AC-coupled. AC-coupling is chosen to minimize the possible ADC linearity degradation due to the IQ imbalance and DC offset. This requires a biasing voltage through a shorted inverter or an 8-bit current-steering DAC, whose inputs are digitally controlled through serial peripheral interface (SPI). The AGC setting for a desired baseband power level is also digitally set via SPI from a 6-bit current-steering DAC. This prevents the baseband signal from over-driving the ADC and the IQ-gain mismatch from exceeding the least significant bit (LSB) of ADC. To extend sampling rate aggressively, the ADC is time-interleaved and implemented with 14 parallel

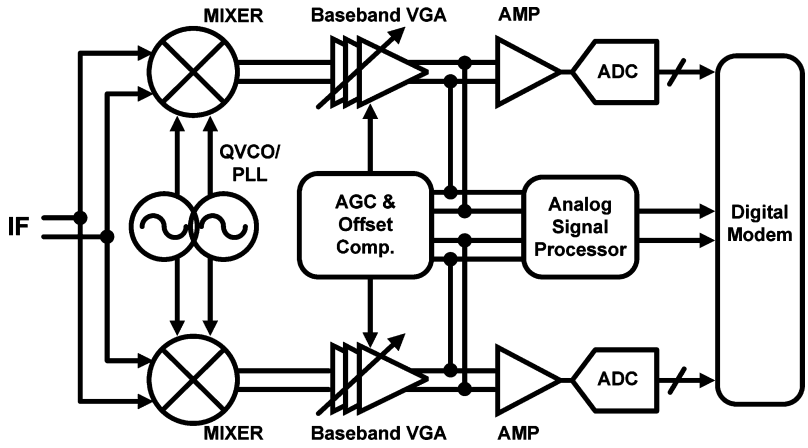

Fig. 3. Demodulator block diagram.

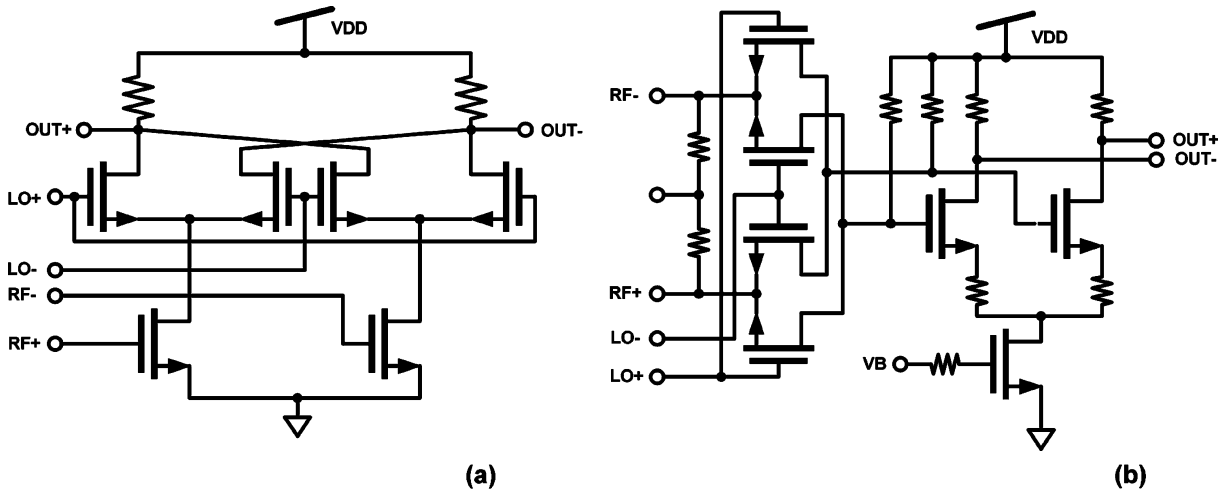

Fig. 4. (a) Schematic of the double-balanced Gilbert mixer. (b) Schematic of the double-balanced passive mixer.

comparators in each channel. This contributes a total loading capacitance of 80 fF. Therefore, the differential-to-single-ended amplifier, designed to drive a large capacitive loading, employs RC-degenerative bandwidth-extension technique to mitigate insufficient bandwidth after three cascaded high-gain VGAs. The output of the ADC contains two 3-bit data streams: each data stream is latched at falling-edge and rising-edge, respectively. The digitized signals are then fed to a digital baseband modem, performing either BPSK or DBPSK demodulation operation using mixed-signal synchronization architectures. The ADC and DSP are time-interleaved throughout digital back-end to meet the stringent timing constraints on such a large-scaled digital system for its multi-gigabit operations. This paper presents the first fully integrated quadrature receiver with embedded analog and digital signal processors in deep-submicron CMOS technology.

III. Circuit Implementation

A. IQ Mixer

The input to the quadrature demodulator is a modulated IF carrier and is downconverted to the baseband frequency. The conventional double-balanced Gilbert-cell mixer [shown in Fig. 4(a)] is not suitable for low-voltage, 1-V operation due to the trade-off between linearity and conversion gain [15]. Since the maximum allowable output swing directly depends on the available voltage headroom across the output load resistor given that the RF transistors need to be in the saturation region, a conventional mixer pays the penalty for low conversion gain in a standard 1-V supply, consequently poor linearity. Therefore, the proposed double-balanced passive mixer shown in Fig. 4(b) utilizes a passive mixing core of RF transistors followed by a differential output buffer to compensate the conversion loss due to the passive mixing. Linearity is preserved in this design because the output buffer requires only two-transistor stacking.

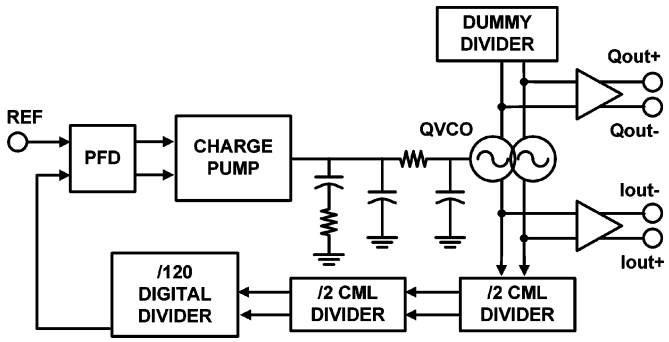

Fig. 5. Block diagram of the IF frequency synthesizer.

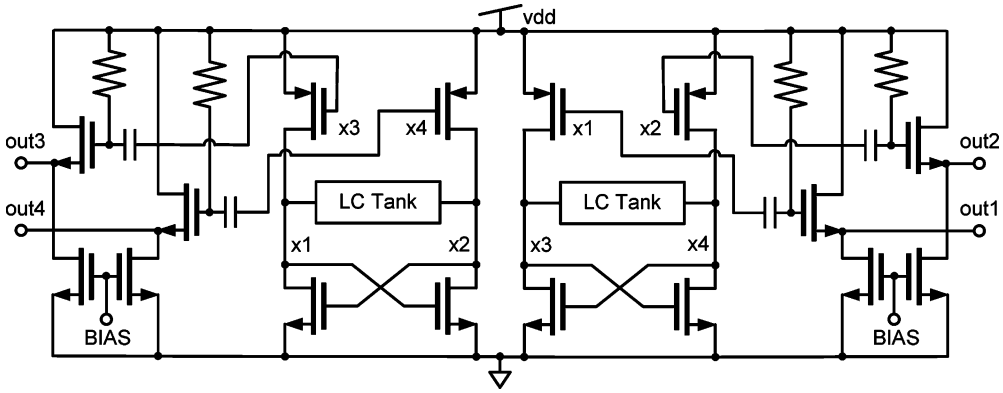

Fig. 6. Schematic of the QVCO.

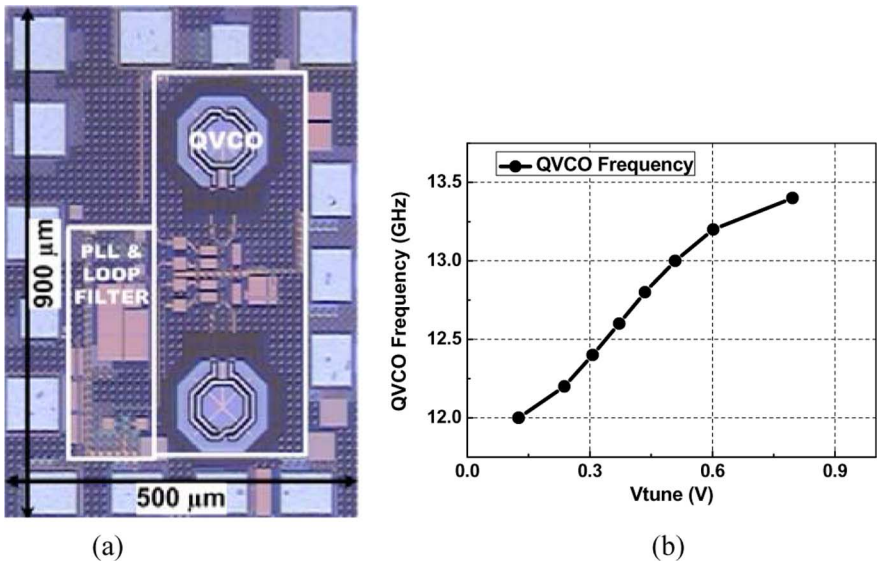

Fig. 7. (a) Microphotograph of the QVCO/PLL test structure. (b) Oscillating frequencies at various tuning voltages.

The mixer provides a conversion gain of 3 dB with a bandwidth greater than 4 GHz and has a power consumption of 3 mW.

B. Quadrature Voltage-Controlled Oscillator (QVCO)

The IF phase-locked loop (PLL) is designed to lock the free-running QVCO to 13 GHz. This frequency synthesizer features an integer-N, type-II, fourth-order architecture with a division ratio of 480 [16]. As seen in Fig. 5, the first two cascaded divide-by-two frequency dividers are implemented using current-mode logic topology. The remaining low frequency dividers are implemented as true single-phase clock (TSPC) counters, featuring a division ratio of 120. The IF PLL shares the same 27 MHz crystal oscillator as the baseband PLL. To realize an on-chip loop filter, the loop bandwidth is chosen to be 2 MHz with a locking time less than 2 μs. The schematic of the cross-coupled LC-QVCO is shown in Fig. 6, where the varactor diodes and inductor form a LC-tank resonator. The mechanism of the parallel cross-coupled pairs forces two differential outputs to be 90 degrees out of phase [17]. The output buffer of the QVCO is a source-follower stage and provides a differential voltage amplitude of 840 mV peak-to-peak with a 3-dB bandwidth of 24 GHz at a current consumption of 2.4 mA.

The QVCO and PLL are first characterized separately on a test structure, occupying an area of $500\ \mu\text{m} \times 900\ \mu\text{m}$, as shown in Fig. 7. The free-running QVCO exhibits a tuning range from 12 to 14 GHz and has a phase noise of -95 dBc/Hz at 1 MHz offset. The KVCO in the center of tuning voltage is 2.9 GHz/V. The total power consumption is 15 mW.

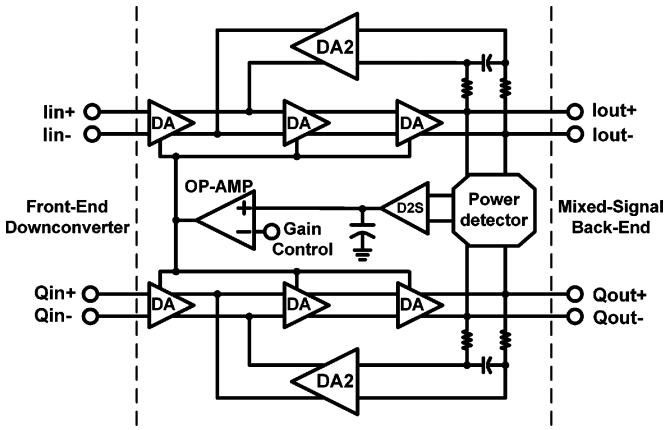

Fig. 8. Block diagram of the VGA with AGC and DC compensation.

C. VGAs With AGC and DC Offset Compensation

The baseband VGAs in each I and Q path are implemented with AGC and DC offset compensation loops as shown in Fig. 8.

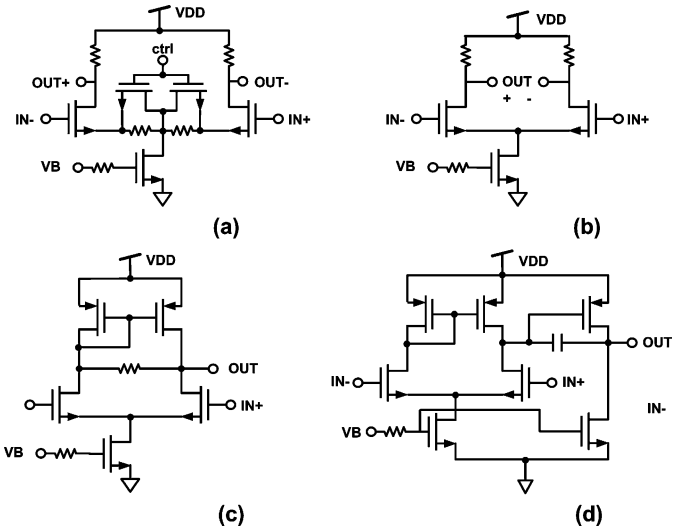

Fig. 9. (a) Variable-gain amplifier schematic. (b) Differential amplifier schematic. (c) Differential-to-single-ended amplifier schematic. (d) Operational amplifier schematic.

Each of the quadrature signal paths consists of three cascaded amplifiers to provide a maximum gain of 24 dB with a continuous gain variation of 27 dB. The schematic of one VGA is shown in Fig. 9(a). Its gain variation and high linearity are achieved using variable source degeneration. Since the VGAs are high-gain amplifiers, any experienced DC offset in the path would lead to erroneous calculations for subsequent quantizers. Therefore, a DC offset compensation feedback loop is required to minimize this offset. It is achieved by connecting the differential output of the third VGA in opposite polarity to the differential output of the first VGA in a low-frequency feedback loop. The accuracy of the DC offset compensation depends on the voltage gain of the differential amplifier, and its schematic is shown in Fig. 9(b).

To avoid clipping distortion to the baseband ADCs, AGC is required to keep the output power of the VGAs constant. It can be realized using a power detector, a differential-to-single-ended amplifier, a low-pass filter, and an op-amp. The schematics of the differential-to-single-ended amplifier and op-amp are shown in Fig. 9(c) and (d). For faster settling response, the cut-off frequency is chosen in the low megahertz range. The output power of the VGA can be digitally controlled and set to a desired value through a 6-bit current-steering DAC. The total power consumption of the baseband VGAs with AGC and DC compensation is 30 mW.

D. Power Detector and On-Off Keying

The power detector circuit (shown in Fig. 10) serves two purposes: to detect the output power from the VGAs and demodulate an OOK-modulated signal. It consists of two double-balanced Gilbert-cell mixers with a common differential load. Each Gilbert-cell mixer performs the squaring function by connecting the gates of the upper-stack and lower-stack transistors to the same input signal. The output of the power detector is the summation result of squared quadrature signals (I^2+Q^2). While operating as an OOK demodulator, a high-speed comparator chain

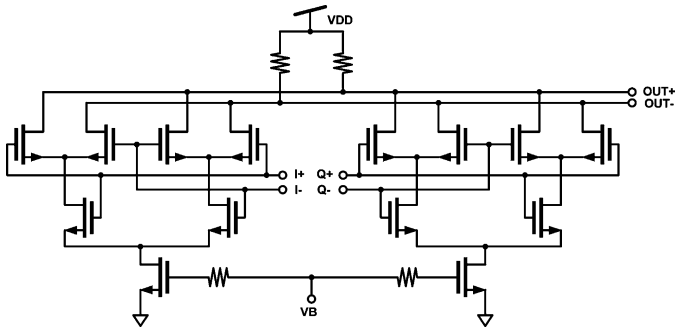

Fig. 10. Schematic of the power detector featuring $I^2 + Q^2$ operation.

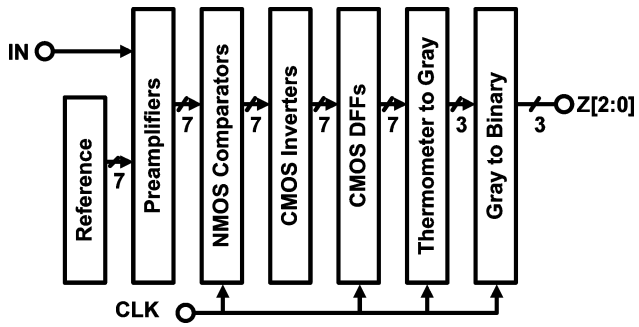

Fig. 11. Block diagram of the high-speed 3-bit ADC.

is enabled to improve the overall minimum sensitivity for a total power consumption of 7.5 mW.

E. High-Speed Analog-to-Digital Converter

Unlike conventional architectures, the ADC performs ultra-low-power processing by removing track-and-hold amplifier [18], [19]. The ADC block diagram is shown in Fig. 11. First, seven comparators sample the data and compare with its own voltage reference to generate the output in thermometer code. Next, the outputs are converted to gray code and then to binary code. The entire operation requires only a single-phase clock and is also time-interleaved to achieve a high conversion rate at a low-power budget. The schematic of the high-speed mixed-signal data path is shown in Fig. 12. In this circuit, the input is first compared with a voltage reference, $V_{\rm ref}$ using the differential pair M_1–M_2. The comparison result is then transferred to the output latch by current mirrors M_3–M_5 and M_4–M_6. When clk is low, M_9 is off and the latch senses the decision of $V_{\rm in}$ and $V_{\rm ref}$. In this phase, when $V_{\rm in} > V_{\rm ref}$, $I_{\rm M1}$ is greater than $I_{\rm M2}$, thus decreasing the voltage at $V1$. Then, at the output node, the drain current of M_5 quickly charges up the negative impedance cross-coupled pairs and brings the output node voltage close to VDD (or *GND* when $V_{\rm in} < V_{\rm ref}$). On the other hand, when clk goes high, M_9 is turned on to short the outputs to equal value and speeds up regeneration. The overload recovery time is determined by M_9, the output parasitic capacitance and the transconductance of M_7–M_8. Furthermore, to guarantee a metastability error due to the undefined comparator outputs, sampling frequency is derived in (3) as a function of a desired metastability probability ($P_{\rm meta}$) and regenerative time constant (τ_R) assuming a single dominant pole at the output cross-coupled pairs. For simplicity, assuming half of

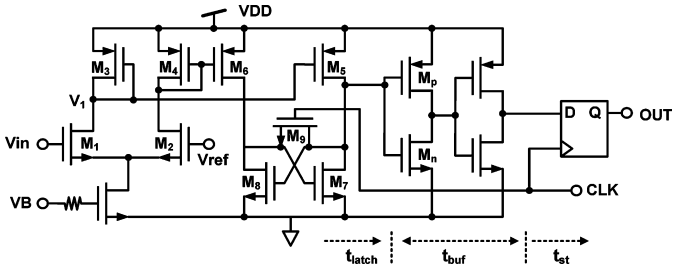

Fig. 12. High-speed mixed-signal data path.

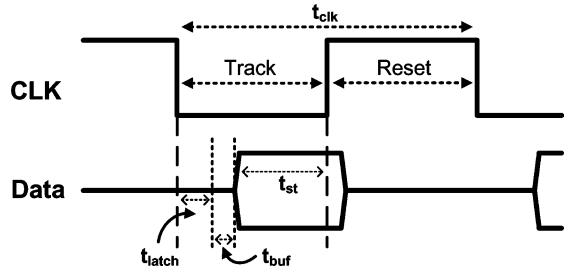

Fig. 13. Critical timing diagram for high-speed data path.

the sample period is used for latch phase and the maximum sampling frequency can be approximated as

$$f_s \propto \frac{1}{2\tau_L} \propto \frac{-1}{2\tau_R \ln\left(\frac{p_{\rm meta} V_{\rm in} A_v}{V_o}\right)} \tag{3}$$

where

$$p_{\rm meta} = \frac{V_o}{V_{\rm in} A_v} e^{-\tau_L/\tau_R} \tag{4}$$

$$\tau_R = \frac{C_L}{g_m} \tag{5}$$

where A_v is the voltage gain of the preamplifier, $V_{\rm in}$ is the down-converted signal voltage swing, V_o is the output voltage swing required for valid logic levels, τ_L is the maximum settling time, C_L is the output capacitance, and g_m is the transconductance of $M_{7\text{-}8}$. To avoid missing codes, the comparator must maintain valid output level for $V_{\rm in}$ larger than half LSB. That is to have its metastability probability less than a given $p_{\rm meta}$ for $V_{\rm in} = V_{\rm FS}/2^{n+1}$ and $V_o = V_{\rm FS}$, where $V_{\rm FS}$ is the input full-scale range with n-bit resolution. Acquiring parameters $A_v = 6$, $g_m = 300\,\mu$S and $C_L = 5$ fF from the simulation, the calculated maximum frequency is 1.55 GHz for a $p_{\rm meta}$ of 1E-08. Therefore, this ADC has to be time-interleaved to guarantee 3 GHz of sampling frequency.

Fig. 13 shows the timing diagram of the interface between high-speed latched comparator output and digital data path. $t_{\rm latch}$ is the data propagation delay due to the latched comparator, $t_{\rm buf}$ is the delay of two CMOS inverters, and $t_{\rm st}$ is the required setup time by the D flip-flop (DFF). Since the propagation delays of the comparator $(t_{\rm latch})$ and buffer $(t_{\rm buf})$ constitute sufficient margin for hold time, the only possible error is caused by the inadequate margin of setup time. From the simulation, the worst case delay from each path is: $t_{\rm latch} = 90$ ps, $t_{\rm buf} = 20$ ps and $t_{\rm st} = 75$ ps, this corresponds to a maximum conversion rate of 2.7 GHz. The

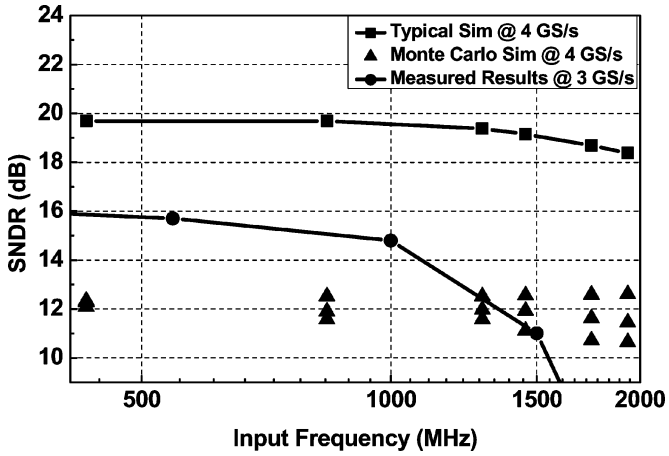

Fig. 14. Measured ADC dynamic performance versus simulation.

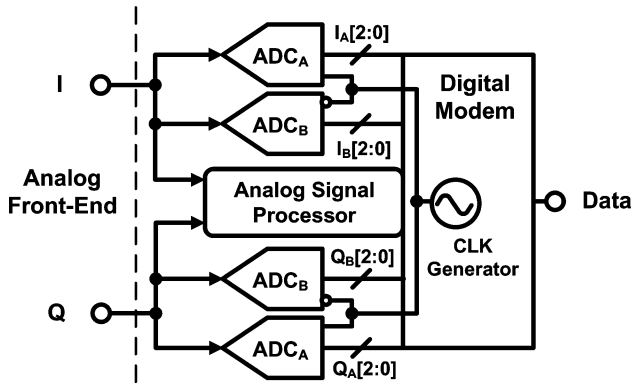

Fig. 15. Block diagram of the mixed-signal back-end.

dynamic performance of the ADC is further simulated in a Monte Carlo mismatch condition and over-clocked at 4 GS/s as shown in Fig. 14. When transistors are plagued by device mismatch and insufficient bandwidth, the signal-to-noise and distortion ratio (SNDR) is limited to 12 dB at 4 GS/s. Toward high input frequencies, the simulations show a larger variation in SNDR. The measured SNDR at a nominal sampling rate of 3 GS/s is also plotted, indicating a SNDR of 15 dB up to 1 GHz input frequency. Overall, this ADC occupies an area of 120 μm $\times$ 90 μm, and has a measured power consumption of 3 mW at 3 GS/s.

F. Baseband Sampling and Clock Generation

The block diagram of the mixed-signal back-end is shown in Fig. 15. The 3-bit time-interleaved ADC in each channel produces a total of 6 bits (3 bits on rising edge and 3 bits on falling edge of the baseband clock) to the digital modem. The positively and negatively latched bits are denoted by subscripts A and B, respectively. The digital modem consists of a mode select block, coherent DSP demodulator, bit synchronization, and non-coherent DSP demodulator. A mode select block is designed to reduce the power consumption by controlling and disabling circuit components that are not required for a specified modulation scheme. The clock signal to the ADC and DSP is generated from a baseband VCO whose control voltage is shared by PLL

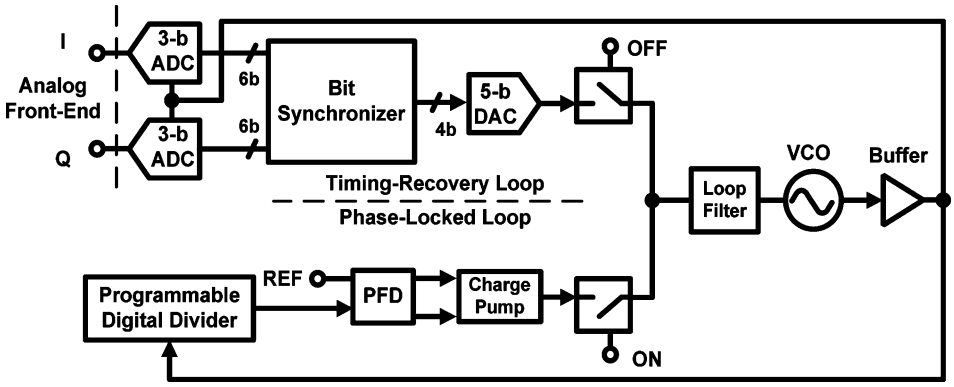

Fig. 16. Block diagram of the baseband frequency synthesizer and bit synchronization, sharing the same loop filter.

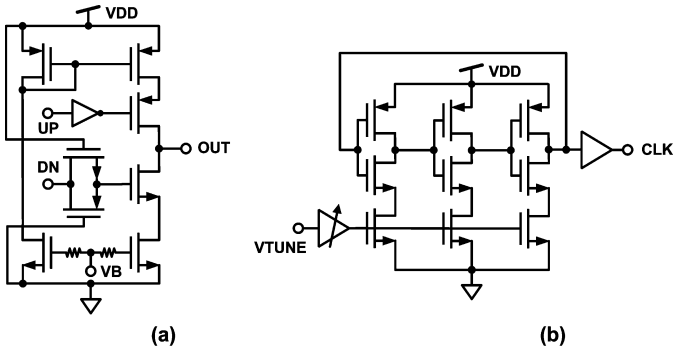

Fig. 17. (a) Charge pump schematic; (b) Schematic of the three-stages ring oscillator.

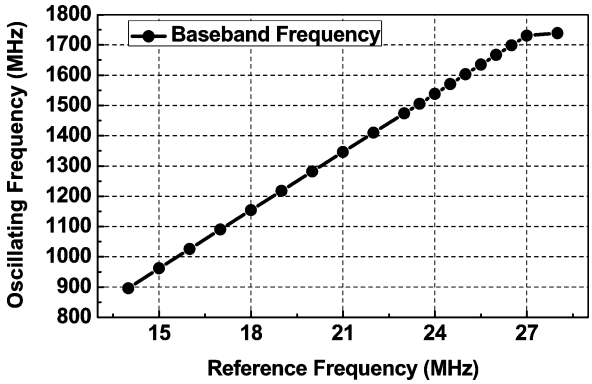

Fig. 18. Measured baseband oscillating frequency ranges.

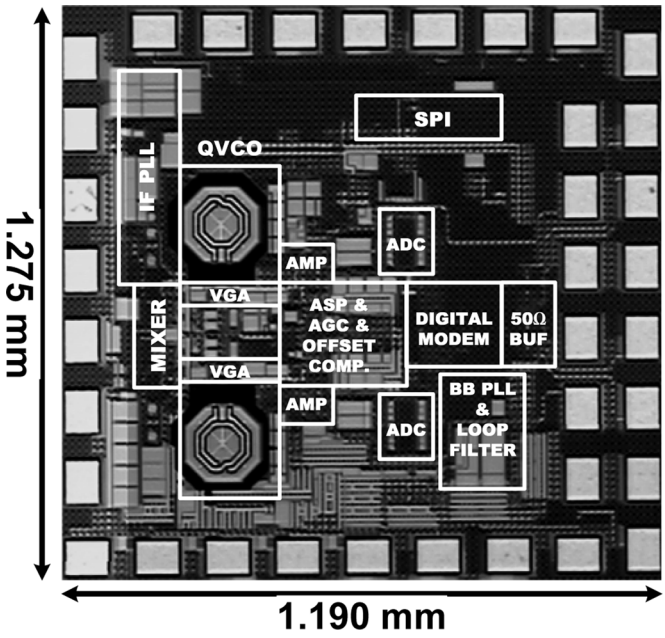

Fig. 19. Microphotograph of the mixed-signal receiver.

and a timing-recovery loop as shown in Fig. 16. In the operation of coherent DSP demodulator, the clock is generated by the baseband frequency synthesizer, comprising a three-stage ring oscillator and featuring a third-order, type-II, integer PLL. This PLL locks on to a 27 MHz crystal oscillator at a nominal rate of 1.485 GHz with a division ratio of 55. Programmable division ratio is also available to select different data rates, such as 432 MHz, 864 MHz, 1.485 GHz, and 1.728 GHz.

The phase detector is implemented as a linear Hogge structure [20], the charge pump schematic is shown in Fig. 17(a), consuming 300 μA, and the loop bandwidth is chosen 2 MHz range to avoid using large external capacitor. The schematic of the three stages current-starved topology based VCO is shown in Fig. 17(b). Since the ring oscillator has higher gain and poor linearity between the output frequencies with respect to the control voltage, an input conditioning block, an attenuator, is designed to linearize the frequency characteristics. The use of a wideband loop filter worsens the phase-noise performance; thereby requires the clock jitter (Δt) to satisfy the following condition:

$$\Delta t < \frac{1}{2^N \pi \cdot f_{\text{in}}} \tag{6}$$

where f_{in} is the input sinusoidal frequency, and N is the resolution of the ADC. When frequency scales up, the quantizing error due to the jitters becomes significant. Considering an input frequency of 1.5 GHz and 3-bit resolution, the required clock jitter should be less than 26.5 ps. The baseband frequency synthesizer is measured to have a RMS phase jitter of 12.78 ps at 1.485 GHz while consuming 3 mW. By varying reference frequencies, the baseband VCO covers a frequency range from 900 MHz to 1750 MHz as shown in Fig. 18.

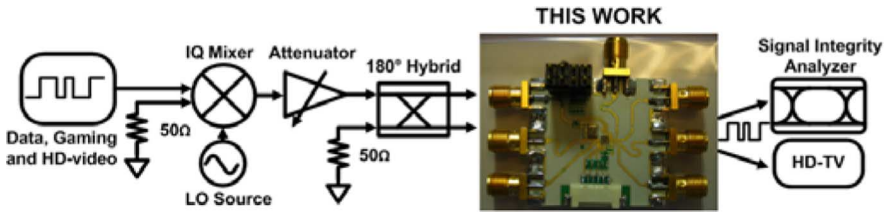

Fig. 20. Measurement setup and test module.

G. Digital Modem

Using the sampled baseband signal, a low-power mixed-signal symbol timing-recovery loop is designed for reliable data detection in modern digital communications system [21]. In the operation of timing-recovery loop, the baseband frequency synthesizer loop is disabled because the bit synchronizer shares part of the baseband VCO loop as seen in Fig. 16. Its implementation is based on a 3-bit Gardner timing-error detector (GTED) without using any digital multiplication. The Gardner loop method is developed for BPSK and QPSK symbol synchronization [22]. It basically detects the zero crossing point of the symbols, and corrects the gradient using neighboring sample values [23]. The recursion process is performed to reduce the error for timing recovery, and a timing tone is recovered though convergence. To avoid the interpolation operation needed to estimate the correct sampling instance, a 4-bit digital timing-error signal is converted to analog domain using a 5-bit high-speed current-steering DAC as shown in Fig. 16. Then, the timing-error signal is filtered by a passive loop filter at a loop bandwidth of 2 MHz. This error signal controls the phase of the baseband VCO. The digital timing-error detector block is capable of handling high data rate at low power consumption; it does not require any digital multiplier and utilizes 657 gates (2163 μm^2) to perform a 6-bit input error calculation. When the GTED loop finally settles for the optimum sampling, its output becomes only the 3-bit input samples following on rising edge of the clock. The 3-bit on falling edge of the clock are discarded, being the symbols at zero crossing. The non-coherent DSP demodulator can work at only one sample by symbol, when the loop is locked, and works at the maximum SNR on I and Q inputs. Its measured power consumption is 14 mW at a data rate of 1.25 Gb/s, which is also the maximum error-free transmission speed.

IV. Measurement Results

The quadrature receiver chip is fabricated using a standard 90 nm digital one-poly seven-metal (1P7M) CMOS process and occupies an area of 1.275 mm $\times$ 1.19 mm (shown in Fig. 19). For measurement purposes, the chip is mounted onto a FR-4 based module using wirebonding as shown in Fig. 20. The measurement setup modulates either an uncompressed HDMI video streaming or PRBS pattern generator with the LO (13 GHz) through the off-the-shelf IQ mixer followed by a 30 dB attenuator. Then, the single-ended modulated signal is converted to differential signals through a 180 degrees hybrid to feed the mixed-signal quadrature receiver with a modulated signal. The data output is measured by a signal integrity analyzer for eye-diagram captures. In addition, it is connected to a high definition TV featuring a real-time uncompressed video streaming.

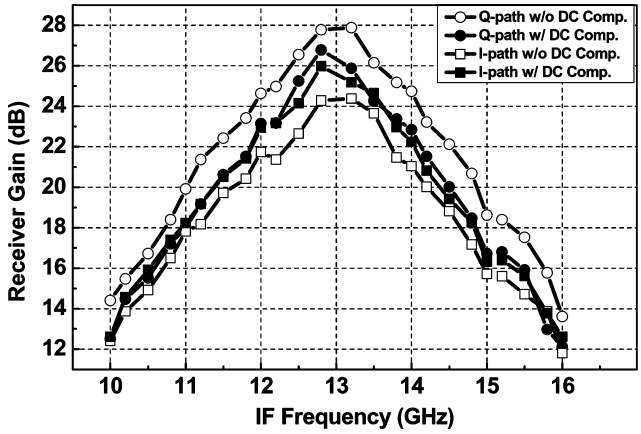

Fig. 21. Measured downconversion gain versus IF frequencies.

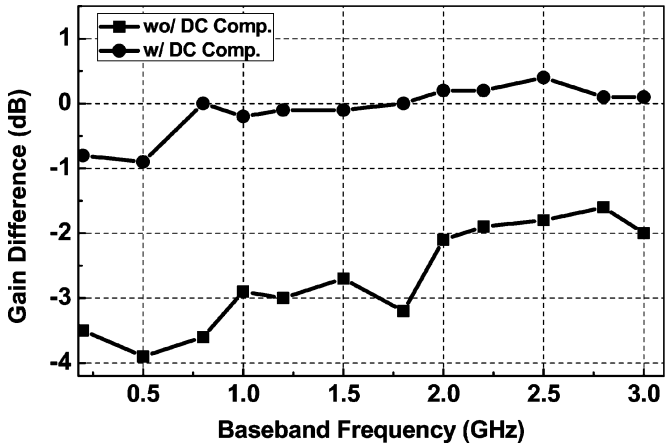

Fig. 22. IQ gain imbalance versus baseband frequencies.

A. Analog Front-End Performance

Fig. 21 shows the gain response of the analog path with and without DC offset compensation at various IF frequencies. The lines with circle symbols indicate the analog gain at different IF frequencies in Q-path. Similarly, the analog gain of the I-path is labeled with square symbols. The maximum measured gain with DC offset compensation is 26 dB at the center of the designed local oscillating frequency, and achieves a double sideband bandwidth of 2.4 GHz. The IQ gain imbalance is further plotted in Fig. 22. This is done by subtracting the measured gain

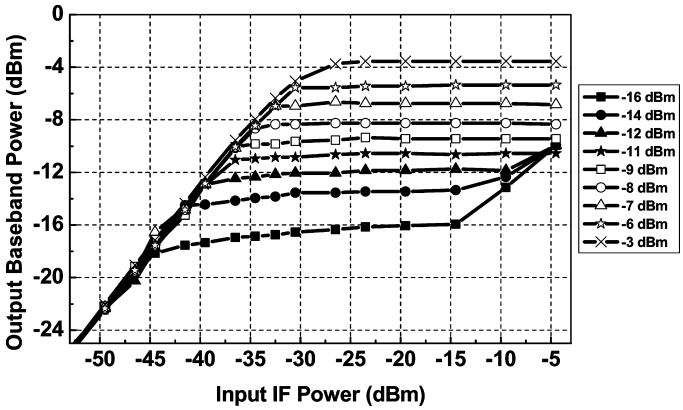

Fig. 23. Measured baseband power level at various AGC settings.

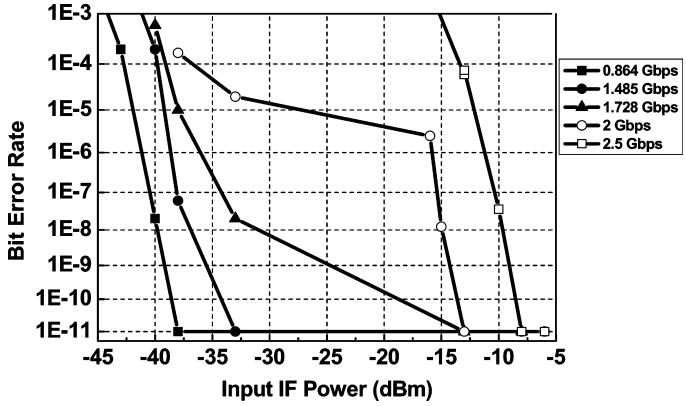

Fig. 24. Measured OOK BER at various data rates.

in the I-path by the gain in the Q-path. When the DC offset compensation is enabled, the gain difference between I and Q channels is less than 1 dB across all baseband frequencies. From 750 MHz to 3 GHz, the gain imbalance is even less than 0.4 dB. On the other hand, when the DC offset compensation is disabled, the IQ gain mismatch can be as high as −4 dB at a baseband frequency of 500 MHz. As expected, the gain mismatch attenuates at higher baseband frequencies.

The AGC system is next characterized. Fig. 23 shows an input dynamic range from −44 dBm to −17 dBm with a measured baseband power level from −16 dBm to −3 dBm at various closed loop gain setting. Sharing the same power detector within the AGC, the performance of the OOK demodulator is verified at a maximum gain setting. Fig. 24 shows the measured BER at different input IF power levels for various data rates. It achieves minimum sensitivities of −36 dBm, −33 dBm, and −13 dBm at 864 Mb/s, 1.485 Gb/s, and 1.728 Gb/s, respectively. The minimum sensitivity for 1.728 Gb/s and 2 Gb/s data rates both occurs at −13 dBm due to the insufficient analog front-end bandwidth. To solve this issue, high-bandwidth mode is enabled to push the bandwidth at the expense of lower baseband amplifier gain. At different data rates, the measured input IF power level for maintaining error-free transmission ranges from −38 dBm to −6 dBm, resulting a dynamic range of 32 dB.

B. Mixed-Signal Back-End Performance

In the operation of DSP, the baseband power level is set to −10 dBm, which corresponds to a 200 mV peak-to-peak voltage swing at the input of ADC. The coherent BPSK demodulator performance is first characterized. Fig. 25 displays the sensitivity of the mixed-signal demodulator by varying the input DC voltage of the ADCs in both I and Q channels together. This test is conducted using a $2^{31}-1$ PRBS signal at a data rate of 1.485 Gb/s for an input IF power level of −33 dBm. The demodulator is robust against the DC bias variation and remains error-free demodulation from the ADC input bias voltages of 465 mV to 555 mV. Furthermore, a measured minimum sensitivity is shown in Fig. 26. Wide synchronization ranges occur at higher input IF power levels. When the input IF power level is sufficiently strong (i.e., >-33 dBm), the synchronization range can be achieved better than 40 MHz. At −39 dBm power level, the range drops down to only 20 MHz.

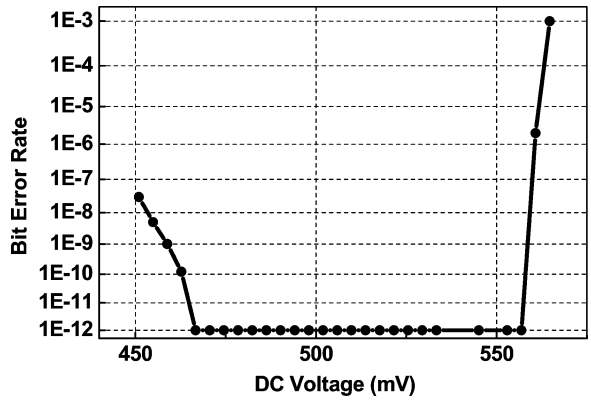

Fig. 25. Measured BPSK BER versus ADC input bias at 1.485 Gb/s.

It should be noted that the BER is not affected at saturated baseband power level and maintains error-free demodulation up to 2.5 Gb/s. Therefore, the performance will not deteriorate if the gain of AGC loop is set to maximum. Hence, the dynamic range of the demodulator is greater than the 27 dB provided by the AGC and better than 33 dB. In Fig. 27, the synchronization ranges with corresponding BER are measured at various data rates from 432 Mb/s to 3.5 Gb/s. This DSP achieves synchronization range of 51 MHz at 864 Mb/s and 15 MHz at 3.5 Gb/s, respectively. In the same plot, error free data transmission is maintained up to 2.5 Gb/s data rate, and 1E-09 up to 3 Gb/s. The highest achieved operating data rate is 3.5 Gb/s with BER of better than 1E-08 measured at an input power level of −33 dBm. The overall power consumption of the BPSK demodulator is 2 mW.

In the operation of non-coherent DBPSK demodulator, symbol timing-recovery loop is first enabled, taking over the loop shared with the baseband frequency synthesizer. Fig. 28 indicates that the bit synchronizer achieves a baseband measured locking range of 19 MHz while maintaining error-free transmission from 1.24 Gb/s to 1.259 Gb/s. When fixing the baseband clock and data rate, the bit synchronizer tolerates an IF carrier offset up to 35 MHz. Fig. 29 shows the measured BER at a data rate of 1.25 Gb/s for various ADC input biases: 510 mV, 514 mV, 518 mV, 522 mV, and 525 mV. Unlike the BPSK demodulator, it is very sensitive to the ADC input bias. For example, to achieve a maximum dynamic range of 32 dB at

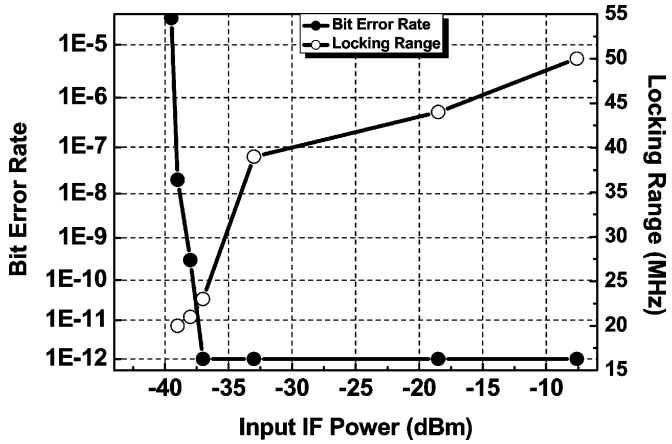

Fig. 26. Minimum sensitivity of the BPSK demodulator at 1.485 Gb/s.

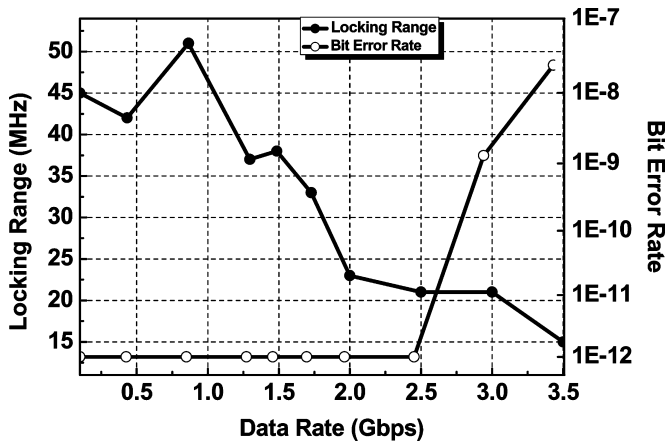

Fig. 27. Locking range and BER of the BPSK demodulator versus data rates.

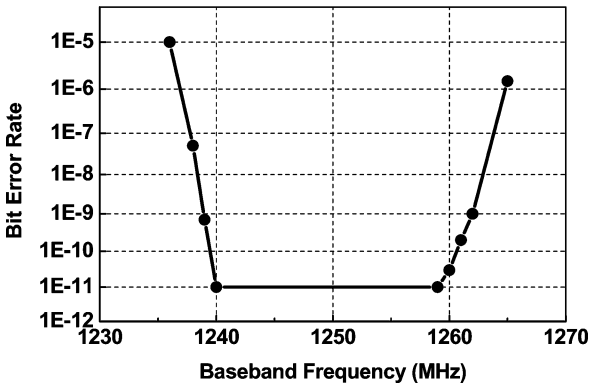

Fig. 28. Measured bit synchronizer locking range.

error-free transmission, the ADC input bias is set to 518 mV. Adjusting the bias to 525 mV, the dynamic range drastically shrinks to 15 dB (from −33 dBm to −18 dBm input IF power levels). The level of sensitivity to the bias voltage variation highlights the importance of DC offset compensation loop and AC-coupling in the operation of a non-coherent DSP. The sensitivity of the demodulator is further tested by varying the baseband power level. Fig. 30 contains 4 curves for different baseband power levels: −10 dBm, −7 dBm, −5 dBm, and −3 dBm. When the baseband power level is set to −10 dBm,

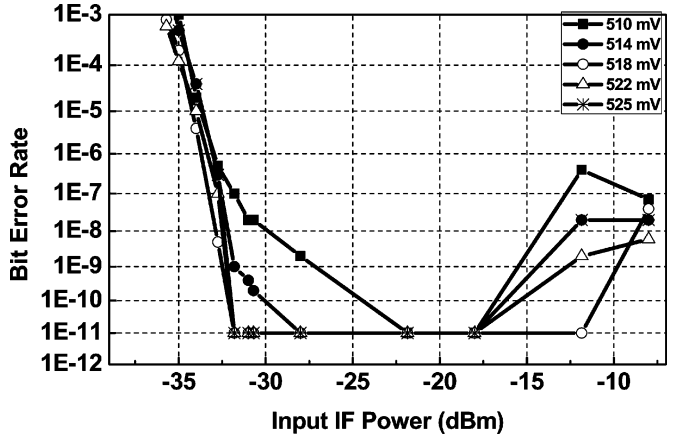

Fig. 29. Measured DBPSK BER at various ADC input bias at 1.25 Gb/s.

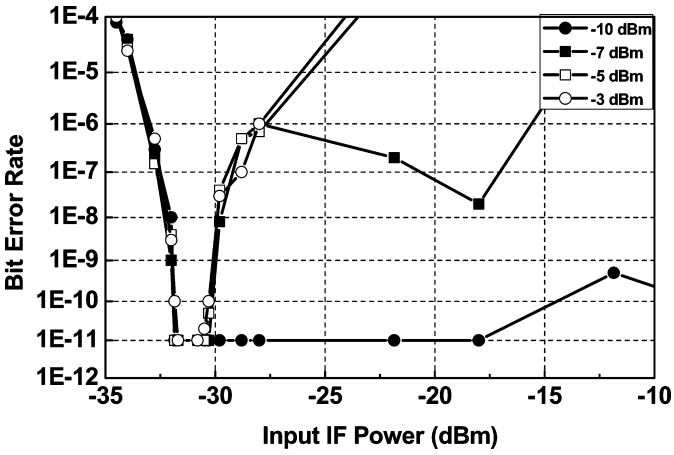

Fig. 30. DBPSK BER at various baseband power levels at 1.25 Gb/s.

the designed value, it achieves the maximum dynamic range as expected. However, saturating the baseband ADCs creates a drastic reduction in the dynamic range. For baseband power levels, such as −7 dBm, −5 dBm, and −3 dBm, the DSP can only maintain error-free transmission from −33 dBm to −30 dBm input IF power levels. This suggests that the DBPSK DSP will have trouble demodulating if there is no AGC loop to fix the baseband power level to −10 dBm.

C. Performance Summary

The performance summary of quadrature receiver is shown in Table II, featuring OOK, BPSK, and DBPSK demodulators. The coherent BPSK DSP demodulator achieves 6 dB better in the minimum sensitivity compared to that of the non-coherent OOK ASP and DBPSK DSP demodulators. However, the synchronization range of OOK demodulator is as 10 times wider than that of the BPSK demodulator. The power consumptions of OOK, BPSK, and DBPSK demodulators are 7.5 mW, 2 mW, and 14 mW, respectively. Finally, the demodulated eye-diagrams are shown in Fig. 31. This broadband quadrature receiver demodulates OOK modulated signal up to 2.5 Gb/s, BPSK modulated signal up to 2.5 Gb/s, and DBPSK modulated signal up to 1.25 Gb/s, while maintaining error-free transmission. The ripples on these eye-diagrams indicate the noise level generated from each signal processor. Clearly, the analog signal processor generates

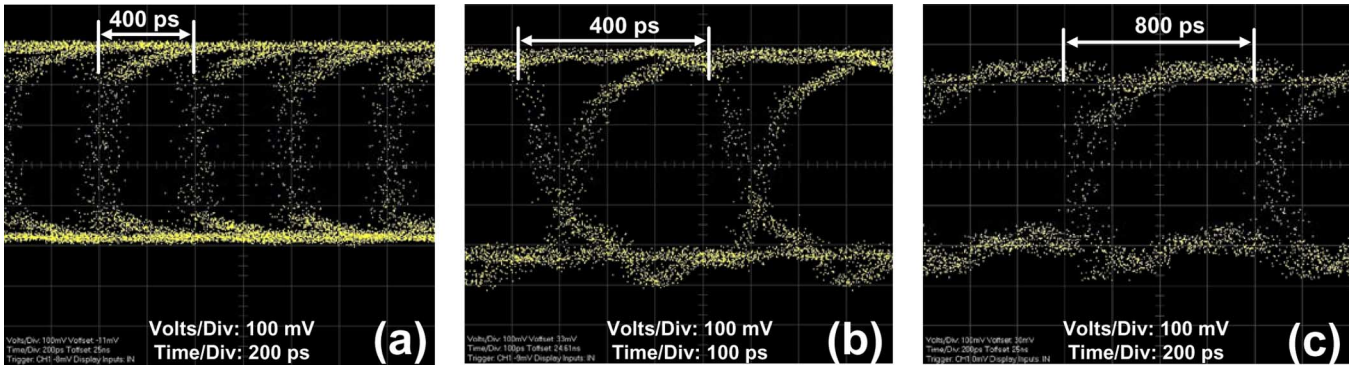

Fig. 31. (a) Demodulated eye-diagram of the non-coherent ASP demodulator at 2.5 Gb/s. (b) Demodulated eye-diagram of the coherent DSP demodulator at 2.5 Gb/s. (c) Demodulated eye-diagram of the non-coherent DSP demodulator at 1.25 Gb/s.

TABLE II
PERFORMANCE SUMMARY OF THE QUADRATURE RECEIVER

COMPONENT	Power Consumption	UNIT	PARAMETER	OOK	BPSK	DBPSK	UNIT
IQ Mixers	6	mW	Voltage Supply	1	1	1	V
IF PLL	15	mW	Signal Processor Power Consumption	7.5	2	14	mW
VGAs with AGC & DC comp.	30	mW	Maximum Speed	2.5	3.5	1.3	Gbps
ASP	7.5	mW	Dynamic Range	32 @ 1.485 Gbps	33 @ 1.485 Gbps	32 @ 1.25 Gbps	dB
Baseband PLL	3	mW	Minimum Sensitivity	-33	-39	-33	dBm
IQ ADCs	6	mW	Maximum Locking Range	500 @ IF	51 @ IF	35 @ IF 19 @ BB	MHz
Digital Modem	16	mW	Bit-Error Rate	< 1E-12 < 1E-12 < 1E-5	< 1E-12 < 1E-12 < 1E-09	< 1E-12 ---- ----	up to 1.25 Gbps up to 2.5 Gbps up to 3.0 Gbps

the least amount of noise in its supply line, where as in the digital signal processor, its eye-diagrams have clear undershoot response, indicating a higher noise contribution to the supply line. The majority of digital noise power is generated by the switching activity of baseband clock.

V. CONCLUSION

A mixed-signal broadband quadrature receiver with an embedded modem in 90 nm CMOS technology is presented in this paper, which leverages unique boundaries between analog and digital circuits to realize a high-performance IC design with compact area and low-power dissipation. A high-speed digital ASIC chip integrated with analog front-end is successfully demonstrated and performs desired multi-gigabit demodulation operations. The proposed architecture presents a fully integrated system that simultaneously achieves multi-gigabit modem functionality and maintains the overall power budget in sub-Watt regions. With a minimum sensitivity of −39 dBm and a dynamic range of 33 dB, the mixed-signal demodulator can perform a multi-gigabit BPSK demodulation up to 3.5 Gb/s data rate. With a minimum sensitivity of −33 dBm and a dynamic range of 32 dB, the mixed-signal demodulator can perform multi-gigabit OOK and DBPSK demodulations and maintains error-free up to 2.5 Gb/s and 1.25 Gb/s data rates, respectively. This demonstrates for the first time a unique multi-gigabit solution for low-power 60 GHz radios.

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Kevin S. Chuang (S'07) was born in Taipei, Taiwan, in 1985. He received the B.S. degree with high honors in electrical engineering from the University of California, Santa Barbara, in 2007, and the M.S. degree in electrical and computer engineering from the Georgia Institute of Technology, Atlanta, in 2009, where he is working toward the Ph.D. degree.

He is currently with the School of Electrical and Computer Engineering at the Georgia Institute of Technology. His research interest includes RF, mixed-signal, and data-conversion integrated CMOS circuits, and CMOS millimeter-wave transceiver development.

Mr. Chuang was the recipient of the 2007 Joseph J. Sayovitz Scholarship for outstanding achievement in electrical engineering at the University of California, Santa Barbara. He is also a member of Tau Beta Pi, Eta Kappa Nu, and the National Society of Collegiate Scholars.

David A. Yeh (S'99–M'10) was born in Taipei, Taiwan. He received the B.Eng. degree (first class honor) in electrical and electronic engineering from the University of Auckland, Auckland, New Zealand, in 2001, and the M.S. and Ph.D. degrees in electrical and computing engineering from the Georgia Institute of Technology, Atlanta, in 2004 and 2010.

His current areas of research include transceiver architecture, gigabit modem, system and circuit design for millimeter-wave gigabit wireless system. From 2001 to 2002, he was employed by Broadcast Communications Limited, Auckland, New Zealand, as an engineering consultant, working on the national deployment of a BWA (Broadband Wireless Access), a pre-WiMAX network. While pursuing his master degree, he held a RF Engineer position at Broadcom Corp., Duluth, GA, where he gained experience in noise modeling and distortion analysis for Cable Modem Termination System. During summers of 2005 and 2006, he held an internship positions at Motorola Labs, Tempe, AZ, working on the practical implementation of a millimeter-wave imaging system. Since 2010, he is a Research Staff at the Samsung Design Center, Atlanta, GA, and he is currently the RF group leader for low-power millimeter-wave IC design.

Francesco Barale (S'07) was born in Viareggio, Italy, in 1982. He received the B.S. (*cum laude*) and M.S. (*cum laude*) degrees in electronics engineering from the University of Pisa, Pisa, Italy, in 2004 and 2006, respectively, and the Ph.D. degree in electrical and computing engineering from the Georgia Institute of Technology, Atlanta, in 2010.

His research interests include the design of multi-GHz phase-locked loop frequency synthesizers and clock-data recovery circuits for multi-Gb/s CMOS integrated wireless transceivers.

Patrick Melet (M'10) received the M.S. and Ph.D. degrees in electrical engineering from Paul Sabatier University, Toulouse, France, in 1997 and 2001, respectively.

His primary research interests include digital signal processing for wireless application and digital spread spectrum demodulation and synchronization (CDMA-DSSS). From 2003 to 2007, he worked as a Research and Development engineer at DM Radiocom on different aspects of digital demodulation: IF under-sampling, digital linear FM demodulation, digital IF Costas loop for PSK demodulation, DQPSK-DSSS demodulation, NRZ bit synchronizers with high military constraints. From 2008 to 2010, he worked at Georgia Institute of Technology on multi-gigabit digital demodulation including symbol synchronization, for low-power CMOS applications. Since 2010, he is a Research Staff at the Samsung Design Center, Atlanta, GA, and he is currently the baseband group leader for low-power millimeter-wave IC design.

Joy Laskar (S'84–M'85–SM'02–F'05) received the B.S. degree in computer engineering with math/physics minors (*summa cum laude*) from Clemson University, Clemson, SC, and the M.S. and Ph.D. degrees in electrical engineering from the University of Illinois at Urbana-Champaign.

Prior to joining Georgia Tech in 1995, he was a Visiting Professor at the University of Illinois at Urbana-Champaign and an Assistant Professor at the University of Hawaii at Manoa. At Georgia Tech (currently on leave) he has held the Joseph M. Pettit Professorship of Electronics and the Schlumberger Chair in Microelectronics in the School of Electrical and Computer Engineering. He is also the Founder of the Georgia Electronic Design Center, and has graduated 41 Ph.D. students and raised more than $45M in extramural research funding since 1995. He has authored or coauthored more than 550 papers and five books, and has more than 50 patents awarded or pending. Dr. Laskar and his research team have founded four companies to date: an advanced WLAN IC company, RF Solutions, which is now part of Anadigics, a next-generation analog CMOS IC company, a next-generation collaborative analog signal CMOS IC company (now the Analog Center of Excellence for Intersil), Sayana Wireless (part of Georgia Tech's Venture Lab), which has developed single chip battery powered solution for multi-gigabit wireless, and Wi-Rider (part of Georgia Tech's Venture Lab), a mobile communications software start-up for broadband white space applications.

Dr. Laskar was elected an IEEE Fellow in 2005 and served as General Chairman of the IEEE International Microwave Symposium in 2008. He currently serves as an elected member of the IEEE MTT-S Administrative Committee and Chair of the IEEE MTT-S Education Committee.