A 6 bit 25 GS/s Flash Interpolating ADC in 90 nm CMOS Technology

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***Abstract*—A 25 GS/s 6 bit flash interpolating ADC in 90 nm CMOS technology with an analog input bandwidth of 14 GHz is presented. The ADC is realized in a fourfold parallelized structure to increase the sampling rate and to increase the available settling time in the single ADCs. To improve the linearity several calibration methods are implemented in the circuit. The power consumption of the whole ADC is 2.3 W, resulting in a FOM of 1.9 pJ/step. The converter core area is 0.75 mm^2.**

***Index Terms*—Analog-to-digital converter (ADC), CMOS, flash ADC, reference ladder calibration, interpolation**

I. INTRODUCTION

In the near future multi-level modulation methods have to be realized to fulfill the highly increasing data transmission needs in fiber optical and wired networks. This is due to the spectral inefficiency of on-off keying and its susceptibility to chromatic dispersion.

Promising methods like OFDM [1] are based on more than one carrier frequency or on phase shift keying like for QPSK. The advanced modulation methods require a complex and fast digital signal processor. E.g. for OFDM this results in two or more separate transmission paths. Each of them consists of a large digital signal processing core, preceded by two ADCs in the receiver and followed by two DACs in the transmitter. If the DSP and the converters are implemented in different semiconductor technologies (i.e. CMOS and SiGe-Bipolar), the packaging and assembly costs and the power consumption for the chip-to-chip interface will be very high. Since the resolution requirements for the ADCs are not too high, a possible solution for this problem is to realize the ADCs together with the digital core on a single CMOS chip.

A twofold 25 GS/s 6 bit approach is presented in [2] and a fourfold 20 GS/s 3 bit approach is presented in [3]. In this design the dynamic performance is improved by implementing a new reference ladder calibration method, a calibrated input amplifier stage and a new error tolerant thermometer-to-binary converter. The number of time-interleaved channels is increased by a factor of two compared to the previous design in [2]. This is due to bandwidth limitations in the single channels being a limiting factor for the effective resolution.

II. ADC DESIGN

Fig. 1 shows the block diagram of the presented fourfold ADC concept. The analog input signal is sampled by a first time-interleaving track and hold circuit (T&H) in the center of the chip. A second track and hold circuit in the master and slave building blocks operates at a quarter of the sampling rate. It delivers a constant signal to a single Flash-ADC for one clock period. Each Flash-ADC consists of a 3 bit coarse flash structure which uses three interpolation stages with active interpolation amplifiers [4] to increase the resolution up to 6 bit. This structure is found to be a good trade-off between power, bandwidth and linearity considerations of the single components and the overall design. Furthermore each ADC has its own reference voltages which can be shifted by current sources in the respective differential reference ladder. The final decision is taken by flip-flops at the interface to the thermometer-to-binary-converter (THBI). The THBI is build up in a new MUX-like structure, reducing the impact of bubble errors of the analog part to a minimum of 2 LSB [5].

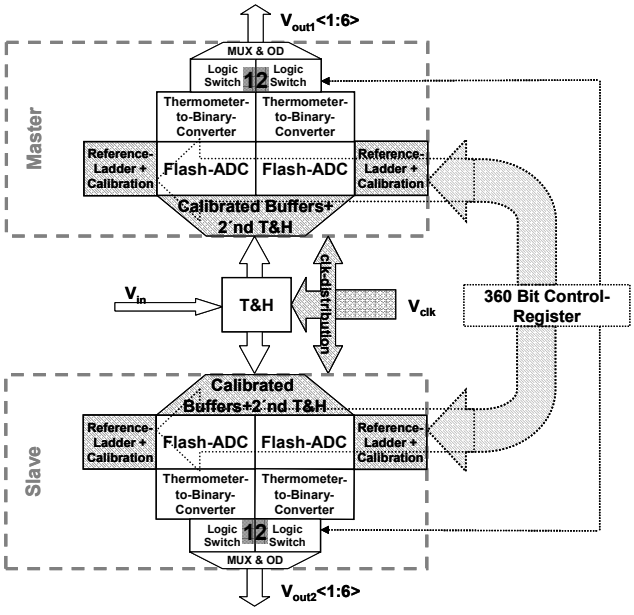

Figure 1. Block diagram of the 6 bit interpolating ADC.

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Two related ADC output signals are multiplexed to a single output to reduce the number of pads and the power dissipation of the output drivers (OD). For synchronization purposes with the test environment there is a half-rate PRBS generator with two blocks number 1 and 2 [6]. The output signals can be switched to the outputs of the corresponding ADC-channel. The combination of these two signals at the MUX results in the desired PRBS of length 1.

A. Analog Front-end

The analog front-end is a very critical part regarding the input bandwidth and the sampling speed of the circuit. In the case of a pure flash converter [3] there is a large capacitive load at the input, since there are 2^{n-1} comparators connected directly to the analog input signal. To reduce this effect, the presented 6 bit ADC implements an active 3-stage interpolation structure from 3 to 6 bit [2], combined with a calibrated frontend structure as shown in Fig. 2a). It is a tree like amplifier structure which reduces the input load and is shorted at the outputs to reduce mismatch effects over the chip.

The amplifiers (Fig. 2b)) are linearized with resistive source degeneration and have a gain of about one to keep the signal linear. By accurate dimensioning of the amplifier stages and the possibility of calibration, the large load of $C_{1\text{-}9}$ is reduced with every stage of the tree. This results in a higher input bandwidth. The T&H is implemented with a differential transfer-transistor structure. It is compensated both at the in- and output to reduce clock feedthrough on the signal itself and on the parallel working channels.

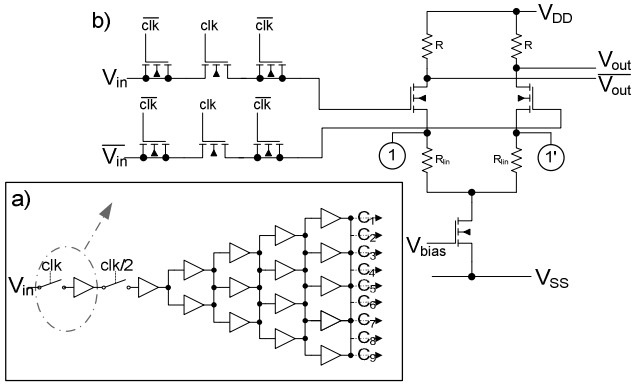

Figure 2. a) Block diagram of the sampler and amplifier in front of the coarse comparators $C_{1\text{-}9}$, b) Track and Hold T&H and a linearized amplifier used in a).

The clock signal for the second T&H is generated by an inductively peaked clock-divider. The clocking network for the T&Hs is connected to a second higher supply voltage VDD_{ovdr} which allows an output swing of the inductively peaked differential amplifiers of 1 V. This allows a lower on-resistance of the transfer transistors.

B. Calibration Circuits

In the case of a parallel structure the linearity is not only affected by the individual mismatch in each channel. If the output signals of the different channels do not match, the overall effective resolution of the converter is reduced [7]. Therefore two different calibration methods are implemented in the presented ADC to overcome in-channel and inter-channel-gain- and offset-mismatch. Timing mismatch is neglected here due to a symmetric and compact layout and design, resulting in very small time differences.

The first calibration scheme is shown in Fig. 3a). The zero crossings of the comparators shown in Fig. 3c) can be corrected by shifting the reference voltages that are generated in the reference ladder (Fig. 3a)). This is realized by binary weighted current sources connected to every node in the reference ladder (Fig. 3b)). A node-voltage can be shifted upwards by feeding an additional current into the corresponding node. To prevent that the surrounding nodes are shifted too, the same current has to be detracted from other nodes. Half the current has to be detracted from the node above and the other half from the node below the node that has to be shifted. This is realized with two different switchable binary weighted current sources and current mirrors for feeding and detraction of the exact currents. The maximum current value of the correction current can be derived from Monte Carlo simulations of the comparators. The result and the value of the reference ladder resistors determine the resolution of the binary weighted current source array according to the accuracy needed. There are similar current sources at the top and the bottom of the reference ladder to shift the voltages of one reference ladder all together or to scale the voltage headroom. This enables an appropriate adjustment of the channels to each other.

The second calibration scheme is shown in Fig. 2b). The linearization is implemented with two separate resistors. Mismatch effects in CML-amplifiers are mainly caused by the two separate current paths in the NMOS transistor pair at the input and the two resistors. Calibration currents can be extracted at the nodes 1 and 1' (Fig. 2b)) to cancel the mismatch. This offers the possibility to shift the zero crossing of the amplifier and to decrease or increase the voltage swing at both sides individually. The size of the current sources can be derived again from Monte Carlo simulations and a desired accuracy. The binary weighted current source array is similar to the one used in approach one with one bit more resolution.

Each current source of the two approaches is controlled by its own register. Since there are four ADCs with calibrated reference ladders and amplifier chains, a 356 bit register is needed which can be programmed by a 3-wire bus. The register will be programmed for the two calibration approaches iteratively by analyzing the output signal channel by channel with respect to static linearity for a ramp-wise input signal.

III. LAYOUT

The layout and the fabrication of the test circuit are done in the general purpose 90 nm CMOS technology of TSMC. The master-slave-architecture of Fig. 1 is directly reproduced in the layout to ensure symmetric channels. Fig. 4 shows the symmetric structure of the converter core with the four time-interleaved ADCs and their corresponding calibrated reference ladders and input amplifier arrays. The clock paths are depicted for the single 25 GS/s domain and the two 12.5 GS/s domains. The input signal is routed with a differential 100 Ω-line to the

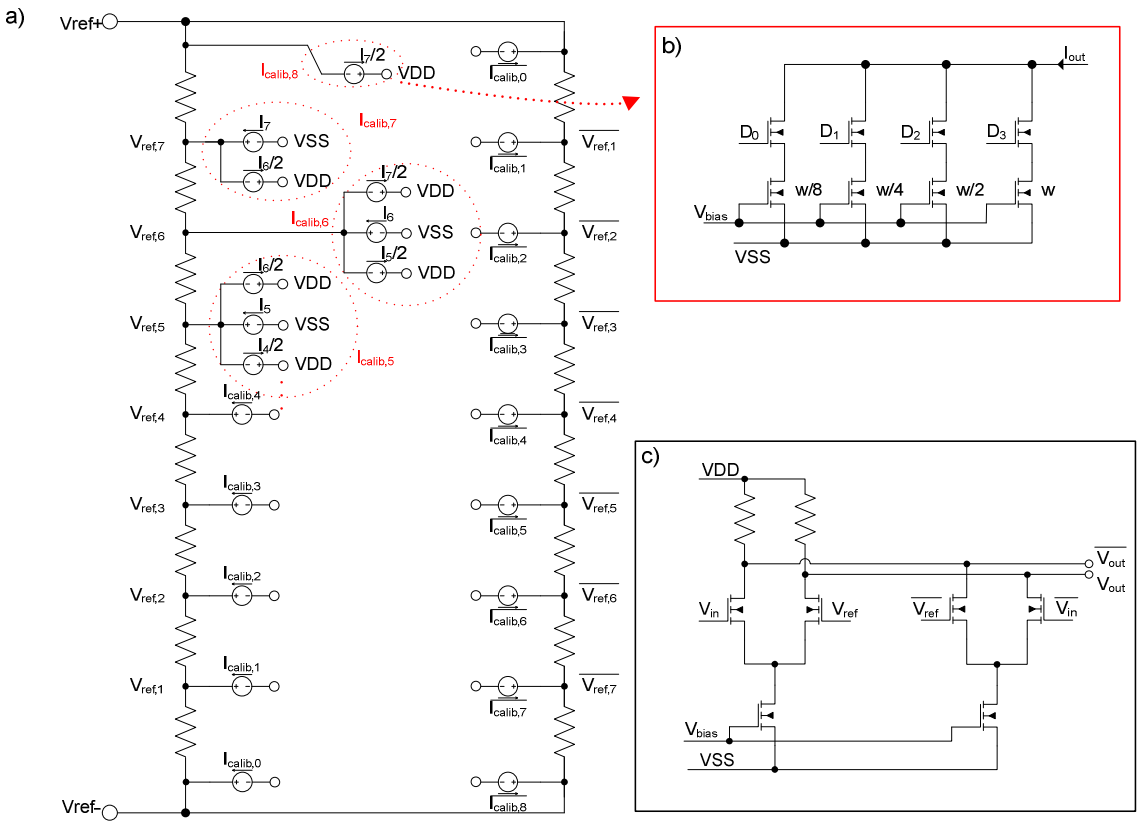

Figure 3. a) Calibration scheme implemented in the reference ladder, b) binary weighted current sources, c) differential CML-amplifier for the coarse quantization stage.

center of the chip to meet with the fast sampling-clock signal at the sample and hold circuit (S&H).

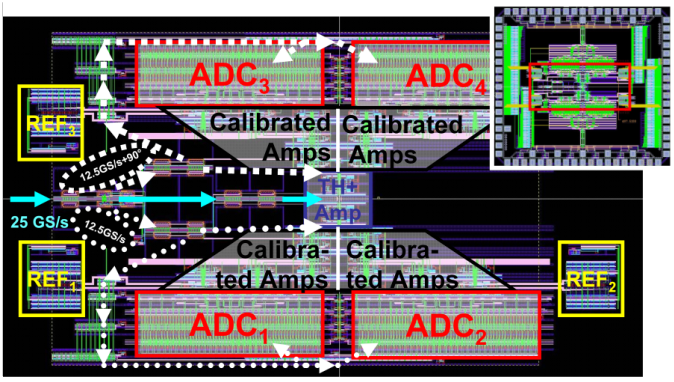

Figure 4. Layout picture of the ADC-core in the center of the die.

IV. Simulation Results

The simulated signal to noise and distortion ratio (SNDR) and the spurious-free dynamic range (SFDR) at a sampling rate of 25 GS/s are depicted in Fig. 5 versus the input signal frequency from 0 Hz to 20 GHz. The simulations are done for each frequency individually in the time domain with noise effects according to the IEEE standard [8]. They include layout RC- and coupling parasitics. The simulation shows an effective resolution of more than 5 bit up to the Nyquist frequency.

The basic functionality of the calibration circuits is verified by insertion of mismatch-sources in the single block simulations and the overall circuit simulations. The simulated characteristics at room temperature and for typical transistor parameters without mismatch are given in Table 1.

TABLE I. ADC Characteristics and State Of The Art

	[10] CHAIS	[11] SAR	[3] Flash	This Work Flash
Technology	65 nm	65 nm	65 nm	90 nm
Publication	2009	2010	2009	2011
Vdd (V)	± 1.2, 3.3	1	1.55	1.25, 1.75
Sampling rate (GS/s)	56	40	20	>25
Resolution (bit)	8	6	3	6
-3dB BW (GHz)	>15	?	10	>14
ENOB (@Hz)	5.7@17G	4.5@10G 3.9@18G	2.3 @ 10G	5.5@DC 5.0@12.5G
Input Range (Vpp diff)	1	?	0.8	1
Power Chip (W)	2	1.5	3	2.3
Core Size (mm^2)	16	?	0.16	0.75

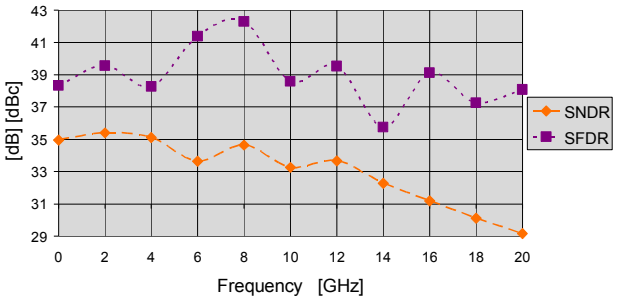

Figure 5. SNDR and SFDR over the frequency range 0-20 GHz at f_S=25 GS/s (simulated).

V. Realization and Test Setup

The ADC-Chip has been fabricated in a 90 nm general purpose technology in 12/2010. A micrograph of the chip is given in Fig. 6 and first tests on a wafer prober affirmed the basic functionality. The pad-configuration is a GSSG-structure with 19 Pads at the top and the bottom and 17 pads at the left and right side, resulting in a chip size of 2.1 x 1.9 mm^2. The six differential digital output signals of the master and the slave are routed to the pads at the top and the bottom of the chip. The analog input signal and the clock signal are routed from the middle of the right and left side to the center of the die. The remaining pads are used by the three-wire-bus, reference voltages and power supply. Additional pads are placed in a second row. They are mainly used for a more symmetric power supply and can only be connected when the ADC is mounted on a printed-circuit-board (PCB).

For testing the chip will be mounted together with four 3:6 DEMUX-chips on a 4.4x4.2 cm^2 thinfilm substrate to reduce the data rates at the outputs (Fig. 7). The DEMUX-chips are implemented in the same technology and work up to 14 Gbit/s. The thinfilm substrate will be mounted on a Taconic RF60A substrate. The digital 50 Ω output-lines of the thinfilm substrate are connected by bond-wires directly to the corresponding 50 Ω-lines on the Taconic-substrate. All the digital lines are connected to a FPGA-board [9] with SMP-plugs in a star-structure around the thinfilm-board on the Taconic-board. This setup ensures the testability with a FPGA with a maximum data rate of 6.5 Gbit/s per channel.

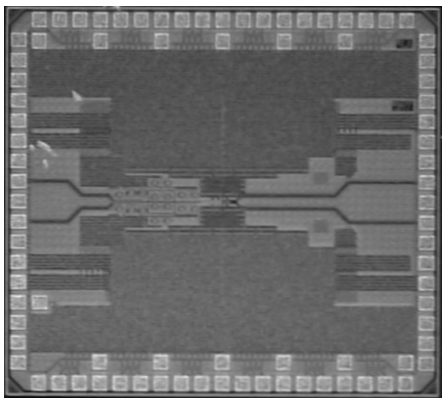

Figure 6. Micrograph of the fabricated ADC chip.

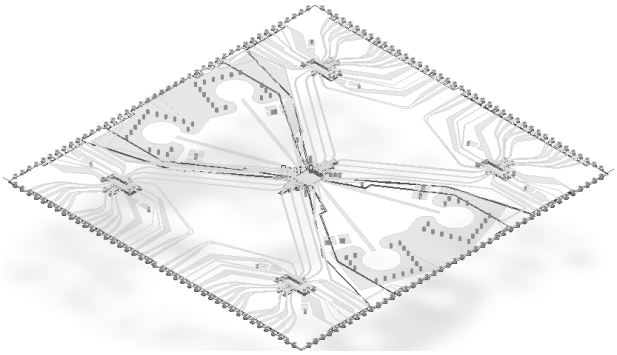

Figure 7. 3D graph of the thinfilm test board with the ADC in the center and a DEMUX-chip in each corner

VI. Conclusion

A 6 bit flash interpolating ADC structure with two calibration schemes is presented. It has a simulated effective resolution of more than 5 bit up to the Nyquist frequency. The power dissipation of the fabricated die is 2.3 W including output drivers and some extra testing logic. The core size is 0.75 mm^2 in a 90 nm CMOS process. Thus the ADC is well suited for integration with large digital logic blocks.

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