A 4.23-bit, 12.5 GS/s Comparator for High Speed Flash ADC in BiCMOS Technology

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***Abstract*-A 4.23-bit, high speed comparator for high-speed flash analog-to-digital converter and X-band applications that can work at a sampling rate of 12.5GS/s is presented in this paper. This fully differential comparator consists of three stages using a new structure to improve its performance. The offset voltage of the designed comparator has been reduced by means of an active positive feedback. The BiCMOS positive feedback and a new structure as output circuit are used to improve sampling rate and performance of comparator. The analyses and simulation results were obtained by using BiCMOS parameters. The comparator can operate with a 1 V peak-to-peak input range consuming 1.09 mW. The predicted performance is verified by analyses and simulations using HSPICE tool.**

***Keywords:* Analog-to-digital converter (ADC), comparator, flash, high speed, preamplifier.**

I. INTRODUCTION

Flash analog-to-digital converters (ADC) with X-band frequency sampling rates are critical components for applications such as radar, signal capture, satellite, digital oscilloscopes and waveform recorders [1]. Today researchers and the industry have extended the requirement for higher frequency and higher sample rate. Flash ADCs can generally achieve the higher sampling rates, with the comparator limiting the maximum achievable sampling speed. In addition, this comparator can be used for UWB and X-band technology that offer a lot of capability for the design of communications devices requiring very high performance and low power consumption. The comparators published in recent years [2][3][4] still have relatively high power consumption and operate with sampling rate lower than the expected future requirement.

In this paper a new BiCMOS positive feedback is proposed to increase the speed of track and hold (T/H) of the comparator. A new structure is also proposed to achieve the overall high speed for the comparator. The comparator design incorporates various techniques to lower its power consumption and improve its overall performance.

The comparator architecture is described in Section II. The preamplifier design, T/H and output domino logic are presented in Section III. Section IV shows the simulation results, and finally SectionV is the conclusion.

II. ARCHITECTURE

The architecture of the comparator is shown in Fig. 1. The comparator structure is fully differential and consists of preamplifier, T/H and output circuits. The first stage is a low gain classical differential amplifier with resistive loads (RD), which isolates the latches from reference voltages. The comparator with resistive loads shows better linearity, offset and gain response in comparison with amplifiers with active or diode loads. Low noise amplifier (LNA) is utilized to reduce the input referred offset of the comparator. The second stage is a BiCMOS T/H with BJT positive feedback and use of inductor and current source to reduce regenerative time. The domino output circuit that is new our suggestion circuit as shown in Fig.5 is used instead of SR Latch to support the comparator in high sampling rate.

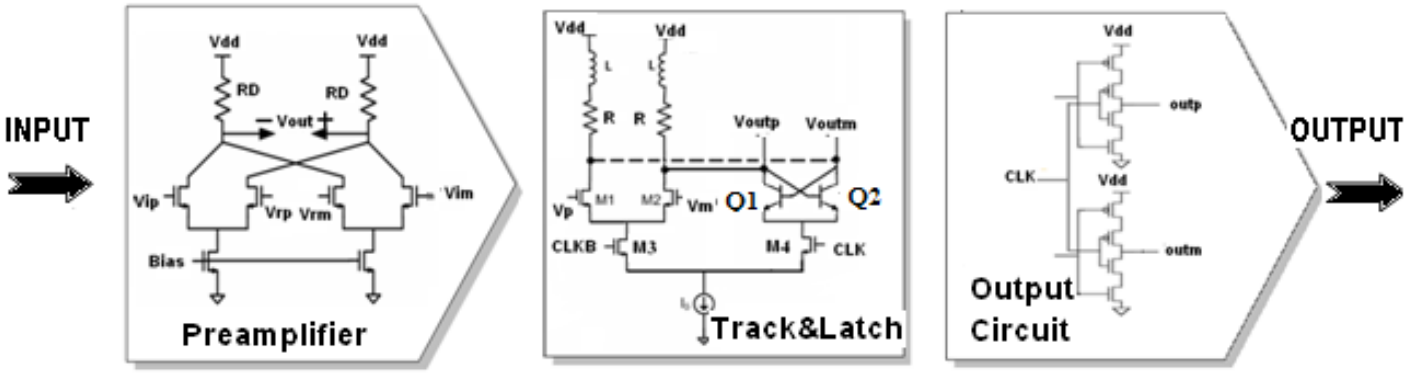

Fig.1 Schematic of comparator

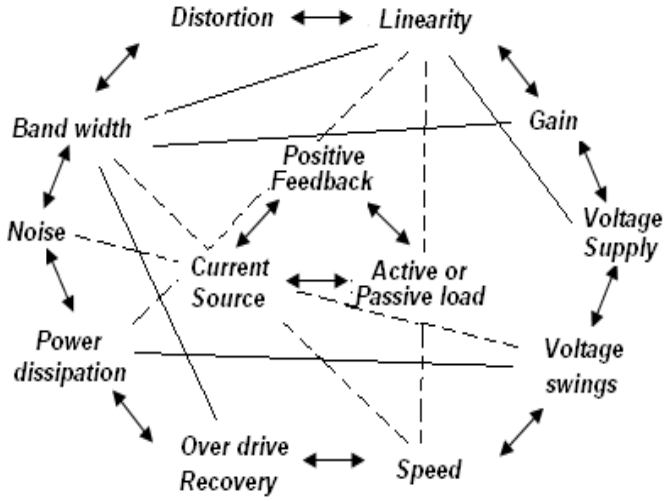

Fig.2 Relationship between comparator design parameters

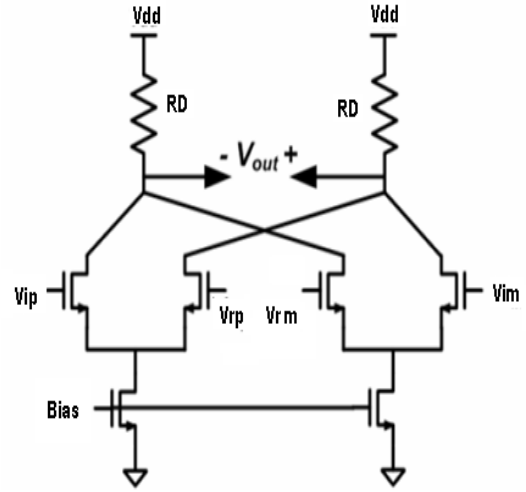

Fig.3 Preamplifier

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In practical implementation, any random or systematic imbalance of the circuit creates an offset in the comparator. Offsets are classified as static or dynamic according to their origins. The fully differential comparator has many advantages to prevent supply and kickback noise and therefore, achieves a big dynamic range. There is a question. What aspects of the performance of comparator are important? In addition to power dissipation and speed, such parameters as supply voltage, gain, voltage swings, band width, distortion, input offset, linearity and overdrive recovery may be important. In practice, most of these parameter trade with each other, making the design a multi-dimensional optimization problem. Illustrated in Fig.2 such trade-off present many challenges in the design of high quality comparator for flash ADC, requiring intuition and experience to arrive at an acceptable compromise.

III. COMPARATOR DESIGN

A. Preamplifier

The LNA preamplifier is shown in Fig. 3. The main role of LNA is to reduce the input referred offset of the comparator. The preamplifier acts as an isolator between voltage reference and T/H to improve bandwidth and decrease input offset. The preamplifier has two inputs for differential analog signal and two inputs for voltage reference. There is a relation between offset and W/L of the preamplifier that is equal to:

$$V_{\text{OFFSET}} = \Delta Vt + \frac{1}{gm}\left(\frac{\Delta w1}{w1} + \frac{\Delta L1}{L1} + \frac{\Delta w2}{w2} + \frac{\Delta L2}{L2} + \ldots + \frac{\Delta wn}{wn} + \frac{\Delta Ln}{Ln}\right) \quad (1)$$

where Vt is threshold voltage and gm is transconductanc W and L are width and length respectively[6][7].

Equation (1) indicates that with increase of transistor size (W) offset will be reduced, but this increase depends on the design. In addition, swing, bandwidth, output capacitance and linearity are important factors to choose the load of preamplifier. The linearity and frequency response of the preamplifier with passive load is better than preamplifier with active load. It is important to note that, with increasing LNA gain, the bandwidth is also decreased.

B. Comparator core (T/H) and Output circuit

The comparator core is shown in Fig. 4. The load is formed by the series combination of a resistor and an inductor. V_{ip} and V_{im} are the differential analog inputs signal from the preamplifier. It has input differential pairs (MI and M2) that turn on when the clock is low and track the input from the previous stage. When the clock is high, the comparator goes into hold mode. In this paper BiCMOS positive feedback is used to improve speed of comparator and reduce the regenerative time in latching mode. The passive inductor peaking technique is also employed in the T/H circuit to enhance the bandwidth [8] [9] [10]. The comparator core is designed using new structure. This type of design is the most efficient in terms of speed and very low swing signal operation. Therefore, it's reduced output swing and hence low-power dissipation. In other words, the domino output circuit as shown in Fig.4 is used instead of SR Latch to support the comparator in high sampling rate operation. The combination of T/H and output circuit creates a fast structure for the comparator [11]. Domino logic as output circuit operates in two phases, the precharge phase and the

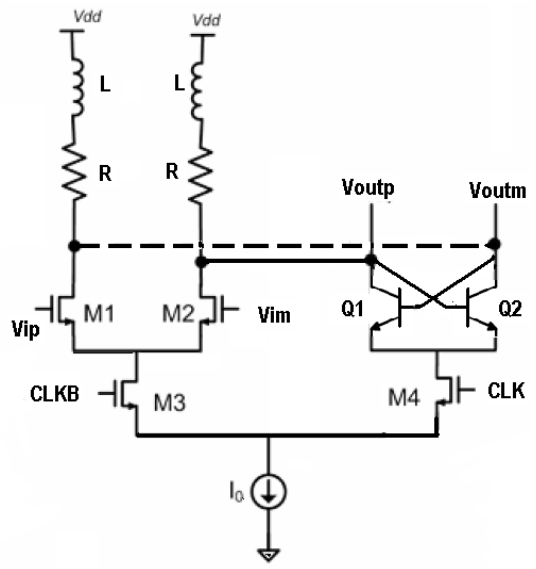

Fig.4 Comparator core (Track/Hold)

evaluation phase. In the precharge phase, output is precharged from low to high, while in the evaluation phase, output will either be discharged from high to low or remain high.

IV .SIMULATION RESULTS

The proposed comparator structure is designed using 0.12 µm BiCMOS technology. Simulation result was obtained by using HSPICE tool Table I shows the summary of comparator performance, in comparison with the designs in [2] and [3]. The new comparator dissipates only 1.09mW at 12.5GS/s. Fig.6 shows the output wave of comparator with1GHz analog input signal and clock frequency of 12.5Gs/s. The FFT of the signal is shown in Fig.7.

TABLE I
PERFORMANCE COMPARISON

Item	[3]	[2]	This work
Supply voltage	1v	2.2v	2v
Power consumption	3.6 mW	--	1.09mW
ENOB	4	3	4.23
Sampling frequency	4 Gs/s	11 Gs/s	12.5Gs/s
process	90nm CMOS	0.12 µm BiCMOS	0.12 µm BiCMOS
year	2007	2008	2010

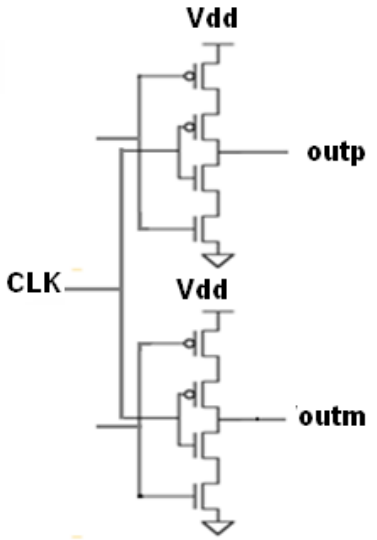

Fig.5 Output circuit of comparator

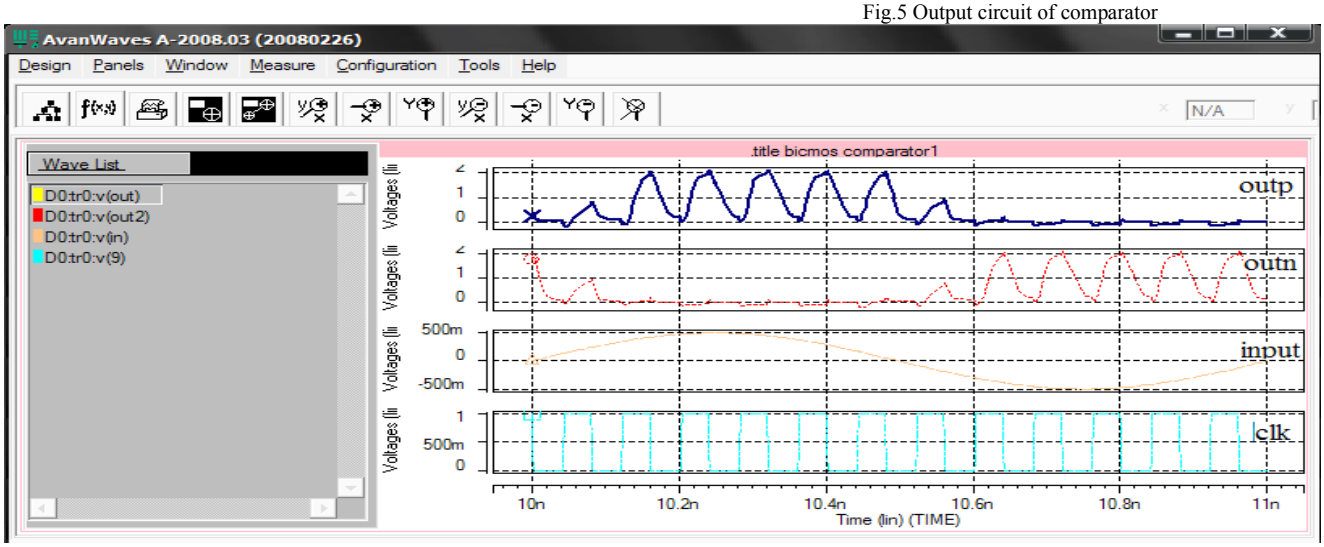

Fig.6 shows output wave of comparator at Fin=1GHz, Fclk=12.5Gs/s

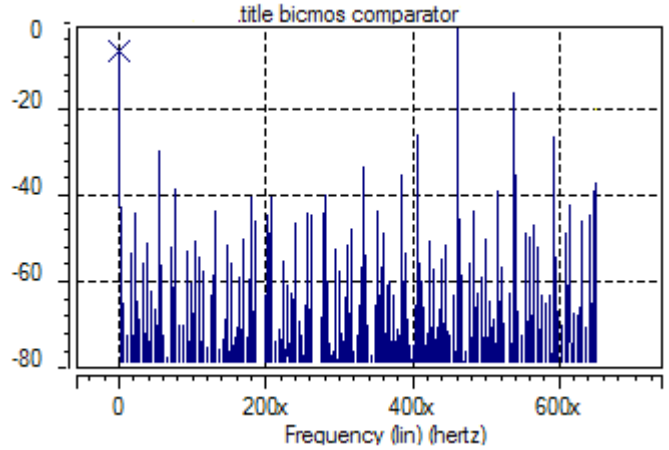

Fig. 7 FFT at input frequency of 4 GHz and sampling rate of 12.5Gsample/s

V. CONCLUSION

In this paper, a 0.12µm BiCMOS X-band comparator for high speed low power flash ADC is proposed. BiCMOS positive feedback and a new structure as output circuit are used to improve sampling rate and performance of comparator**.** We have used new core structure and domino logic circuit to speed up, reduce crosstalk and save power consumption of comparator. The measured ENOB is 4.23 bits at 12.5 GS/s with a 4 GHz sine input signal.

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