6-b 1.6-GS/s Flash ADC with Distributed Track-and-Hold Pre-Comparators in a 0.18μm CMOS

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Abstract— **This work presents a novel flash analog-to-digital converter (ADC) with distributed track-and-hold pre-comparators (THPCs). Utilizing the proposed architecture, the loading capacitances of the ADC front-end sampling sub-circuits can be markedly reduced, thereby improving operation speed. In a standard 0.18μm CMOS process, a 1.6GS/s 6-bit flash ADC is implemented to demonstrate the feasibility of the proposed distributed THPC architecture. The equivalent input capacitance of each input port of the proposed flash ADC is only 400fF, which is an easily driven interface. Furthermore, clocked timing buffers are inserted in the encoder to accelerate the operational speed of the proposed flash ADC.**

Post-layout simulation results demonstrate that the proposed ADC achieves an SNDR of 35.81dB, which is 5.66 ENOB at 1.6GS/s with a 793.8MHz input signal frequency. The proposed ADC consumes 300mW from a 1.8-V supply at full operating speed.

I. INTRODUCTION

High-speed analog-to-digital converters (ADCs) are critical blocks in some systems, such as the read-write channel in a disk drive system and receivers in ultra-wide band (UWB) communication systems, which require a high sample rate and medium-to-low resolution. Among these high-speed ADCs, the flash ADC has become a mainstream research topic due to its superior high-speed performance.

The track-and-hold amplifier (THA) is essential in flash ADCs. Several methods have been developed to ensure that the THA has the desired dynamic performance with a broadband input signal [1–4]. However, regardless of which approach is applied, the trade-offs between linearity, speed, area and power consumption must be considered carefully. For instance, Choi *et al.* increased THA bandwidth by inserting a shunt-peaking inductor [1]; however, this increases chip area. Geelen developed a THA that combines interpolation and averaging techniques [2]. Jiang *et al.* proposed an open-loop THA with replica-based "well-biasing" combined with averaging and interpolation techniques [3]. Although the averaging and interpolation techniques can reduce non-ideal effects caused by offset voltage and generate additional output signals, the requirement of amplifier linearity must still be considered carefully and thus induces a limiting factor on the operation speed.

This work presents a novel flash ADC architecture that utilizes distributed track-and-hold pre-comparators (THPCs) that reduce loading capacitance of ADC front-end sampling sub-circuits, thereby simplifying design methodology and minimizing device sizes of THPCs to achieve high-speed operation. Implemented using standard 0.18μm CMOS technology, the equivalent input capacitance of each input port of the proposed flash ADC is only 400fF due to the relaxed requirement for linearity of the THPC. Digital gate delay caused by logic parts, such as an encoder, also limits flash ADC operating speed. This work overcomes speed limitations by inserting clocked timing buffers into the encoder circuits. Section II introduces the new ADC architecture and THPC circuit. Section III describes the modified encoder topology. Section IV presents post-layout simulation results, which demonstrate the feasibility of the proposed ADC architecture. Section V provides conclusions.

II. FLASH ADC WITH DISTRIBUTED TRACK-AND-HOLD PRE-COMPARATORS

Figure 1 presents the front-end block diagram of the proposed flash ADC with the distributed THPC architecture. The proposed ADC consists of 65 one-bit ADCs. Each one-bit ADC is composed of a THPC, a comparator, and a differential CMOS latch. Since only one comparator is connected to each THPC, the loading capacitance of THPC is reduced significantly, thereby accelerating operating speed. To reduce the non-linearity errors caused by the "end-point" amplifiers, the averaging termination technique is applied to the top and bottom comparators [5].

Figure 2 presents a schematic diagram of the proposed THPC. When all MOS switches—M3, M4, M5, M6, M13 and M14 (Fig. 2)—are on, the THPC functions as a pre-amplifier. When the THPC operates in "hold" mode, it only needs to determine whether the input signal is higher or lower than the reference voltage at the end of the previous tracking period and keep the charges in the parasitic capacitors associated with the output nodes being held correctly. Thus, the linearity requirements of the THPC are more relaxed than those of a conventional pre-amplifier in a flash ADC. Furthermore, all MOS devices in the proposed THPC can be designed with minimal channel length. Using standard 0.18μm CMOS technology, the equivalent input capacitance of each input port of the proposed flash ADC is only 400fF due to minimized device size of the THPC, thereby accelerating operating speed and increasing bandwidth.

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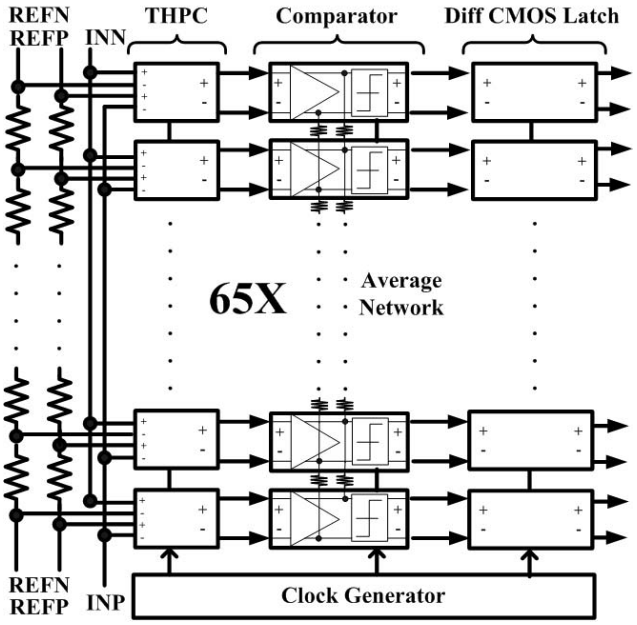


Figure. 1. Front-end block diagram of the proposed ADC architecture

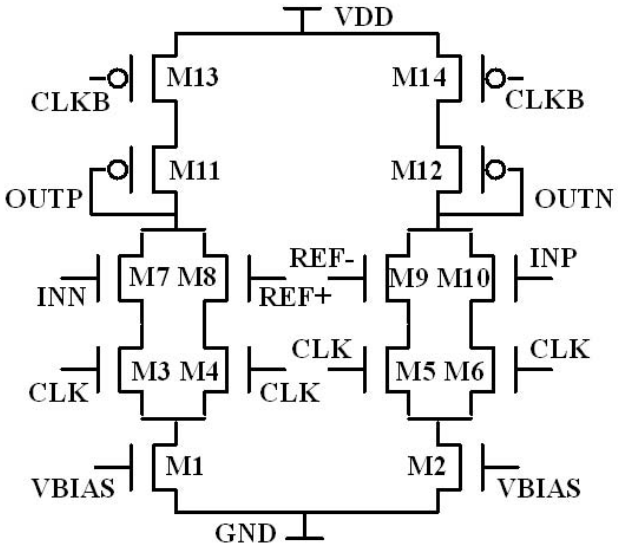


Figure. 2. Schematic of the THPC

Parts of the circuits in Fig. 2 are redrawn as Fig. 3 to show why two MOS switches are below the differential pairs (M7-M8 and M9-M10). Figure 3a shows a conventional one-switch topology. When the THPC works during the hold period, M7 and M8 form a closed-loop path. When the input signals of M7 and M8 are changed during the hold period, the charges in M7 and M8 are redistributed through this closed-loop path; thus affects the output hold voltages. Figure 3b shows the proposed two-switch topology. When the two MOS switches are off, the charge redistribution path no longer exists; thus, output voltages can be "held" correctly during the hold period.

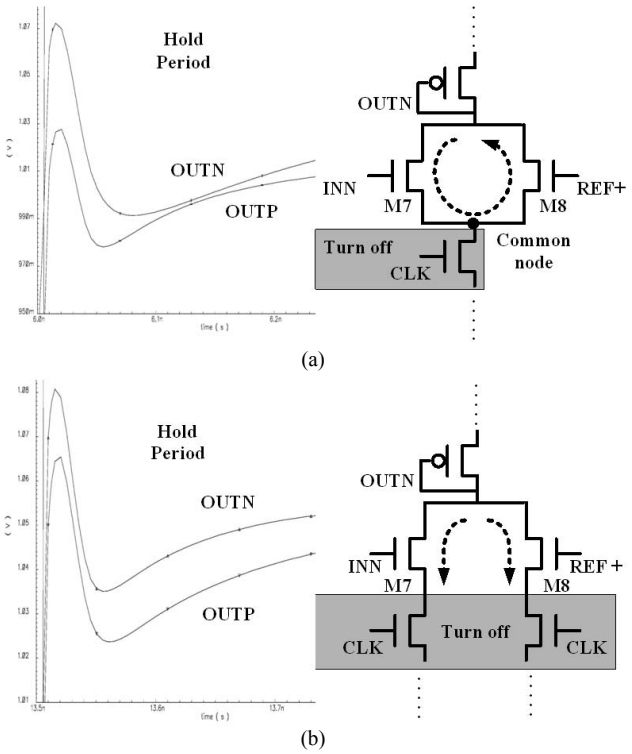


Figure. 3. Charge redistribution path for (a) the topology with one MOS switch (b) and that with two MOS switches

Figures 4 and 5 show the schematics of comparator and differential CMOS latch. To reduce the loading capacitance of previous sub-blocks and ensure high operating speed, all MOS devices in the comparator and the differential CMOS latch are designed with minimal channel length. Both M7 and M8 are added to the comparator to enhance output swing when the comparator is in latch mode.

III. The Modified Encoder with Clocked Timing Buffers

For high-speed flash ADCs, a bubble error is a major cause of bit errors and a critical problem to be solved. This work adopts a "clustering principles" encoding algorithm proposed by Yeh *et al.* to suppress bubble errors [6]; however, Yeh's algorithm still suffers propagation delay of digital gates. To overcome the gate delay limitation, clocked timing buffers are inserted between the clustering processing and the MSB/LSB encoder as shown in Fig. 6. Figure 7 presents an example timing diagram that explains the gate delay problem in detail. When the sum of gate delay time of the clustering process and MSB/LSB encoder exceeds the clock period, "stable outputs" are absent; that is, the encoder cannot convert correct outputs at this clock rate (Fig. 7a). When clocked timing buffers are inserted (Fig. 7b), the MSB/LSB encoder can convert "stable outputs" because the MSB/LSB encoder is separated from the clustering process by the clocked timing buffer such that both output signals of them have sufficient timing margin to settle

down. Post-layout simulation results demonstrate that sampling rate up to 1.6GHz can be achieved when clocked timing buffers are used in the modified encoder.

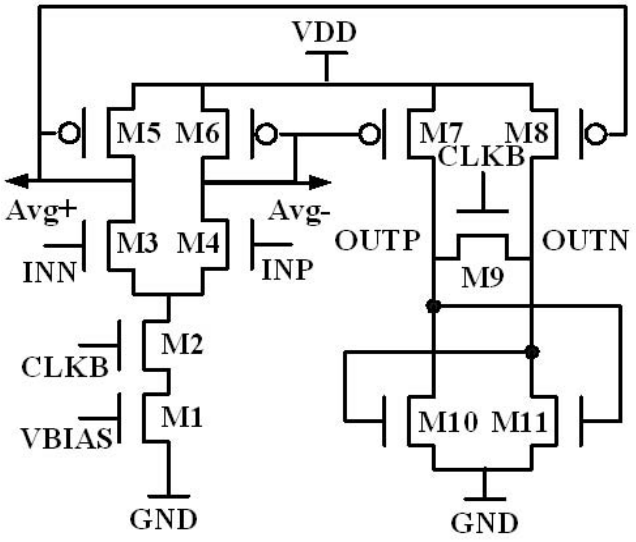


Figure. 4. Schematic of the comparator

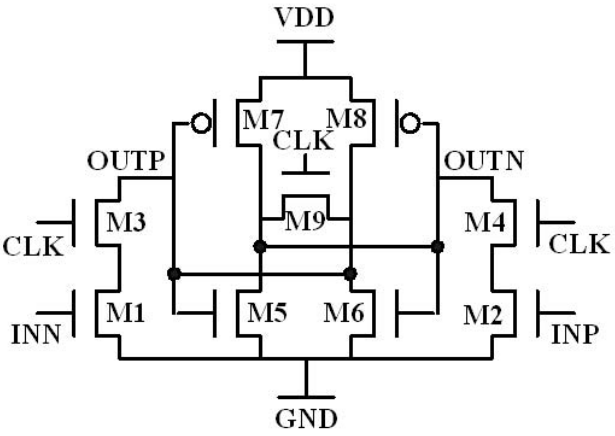


Figure. 5. Schematic of the differential CMOS latch

IV. Simulation Results

The proposed flash ADC was designed using the standard 0.18µm CMOS process and simulations were done using Spectre. Figure 8 shows the physical layout of the proposed flash ADC. The active area is 0.5x0.4mm^2. The DNL and INL shown in Fig. 9 are simulated with an input ramp signal sampled at 1.6G samples/s. The peak DNL and INL are 0.26 LSB and 0.23 LSB, respectively.

Figure 10 illustrates the output spectrum at 1.6Gsamples/s and a 793.8MHz input signal frequency. Figure 11 plots the simulated spurious free dynamic range (SFDR) and signal-to-noise-and-distortion ratio (SNDR) *versus* input signal frequency.

At a low input frequency of 13MHz, the SNDR and SFDR are 37.08dB and 46.71dB, respectively. With input signal frequencies up to 793.8 MHz, the SNDR and SFDR are 35.81dB and 43.24dB, respectively. The ENOB is 5.66 bits. The complete ADC consumes 300mW from a 1.8-V supply while operating at 1.6G sample/s with input signal frequencies up to 793.8MHz.

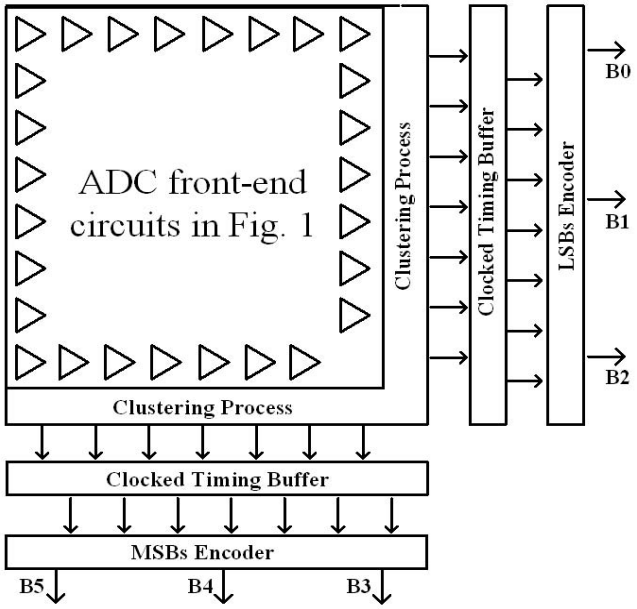


Figure. 6. Modified encoder block diagram with the clocked timing buffer

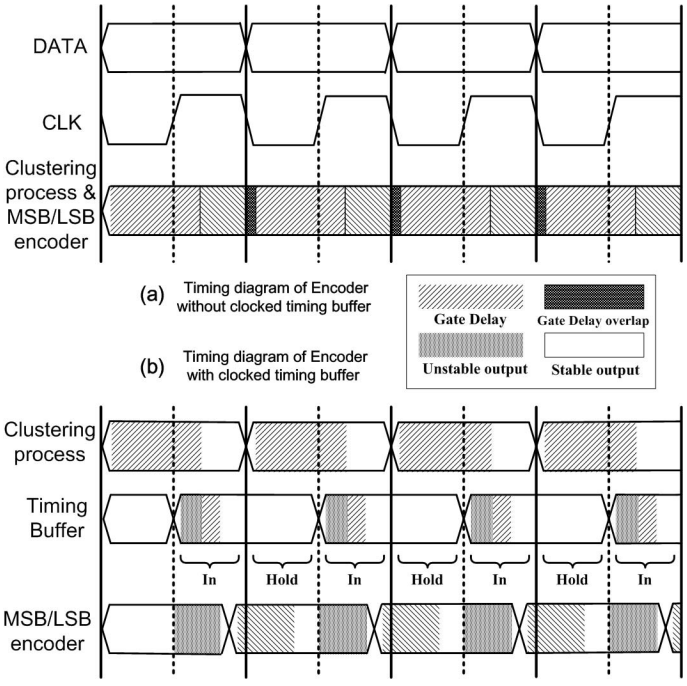


Figure. 7. Timing diagram of the clustering process and MSB/LSB encoder (a) without and (b) with the clocked timing buffer

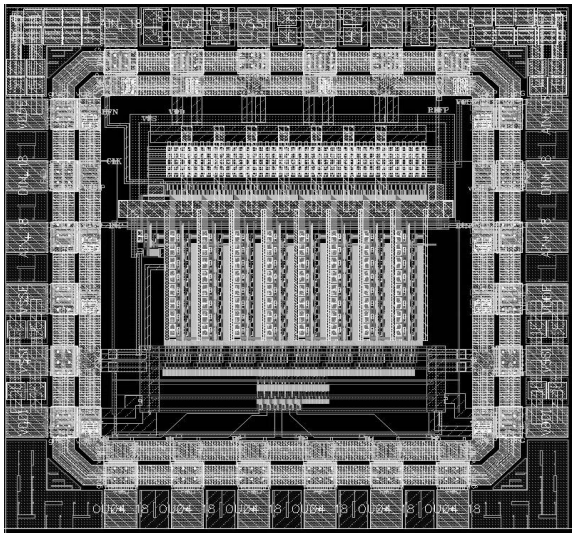
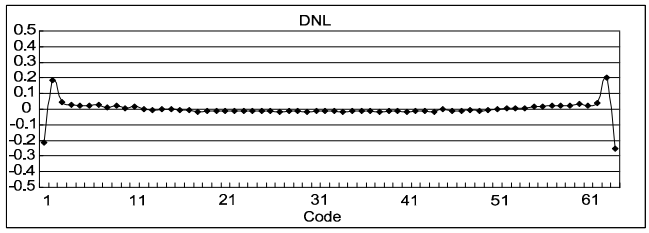
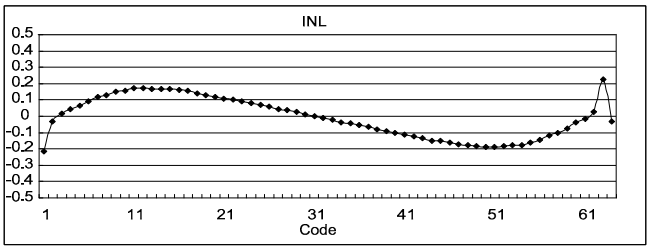


Figure 8. Chip layout of the proposed ADC



DNL(LSB)



INL (LSB)

Figure. 9. Simulated DNL and INL of the proposed ADC

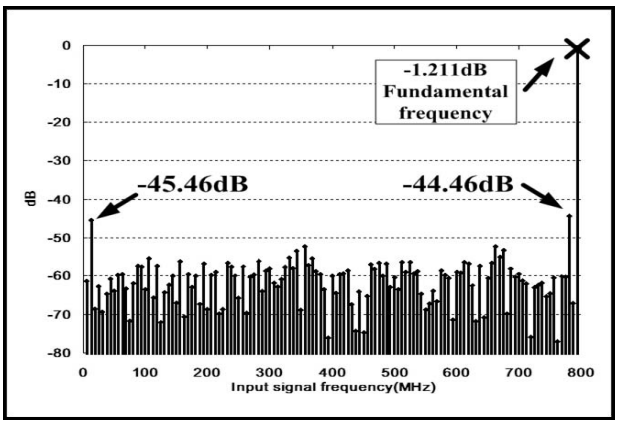


Figure. 10. Output spectrum of a 793.8MHz input signal at 1.6 GS/s

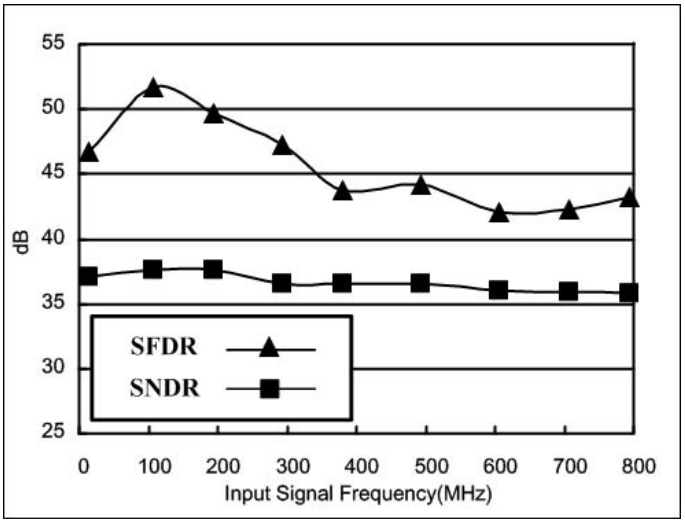


Figure. 11. Simulated SFDR and SNDR *vs*. input signals sampled at 1.6 GS/s

V. CONCLUSIONS

This work presents a novel flash ADC architecture with distributed THPCs. Post-layout simulation results with a standard 0.18μm CMOS process model show that an ENOB of 5.66 bits can be achieved with an input frequency of 793.8MHz at 1.6G samples/s while consuming 300mW from a 1.8-V supply. The equivalent input capacitance of each input port of the proposed ADC is only 400fF, which is an easily driven interface.

VI. ACKNOWLEDGEMENT

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