A 2.4 GS/s, Single-Channel, 31.3 dB SNDR at Nyquist, Pipeline ADC in 65 nm CMOS

Timmy Sundström, *Student Member, IEEE*, Christer Svensson, *Fellow, IEEE*, and Atila Alvandpour, *Senior Member, IEEE*

***Abstract*—This paper presents a high-speed single-channel pipeline analog-to-digital converter sampling at 2.4 GS/s. The high sample rate is achieved through the use of fast open-loop current-mode amplifiers and the early comparison scheme. The bounds on the sub-ADC sampling instance are analyzed based on sufficient settling for a decision as well as metastability. Implemented in a 65 nm general purpose CMOS technology the SNDR is above 30.1 dB in the Nyquist band, being 34.1 and 31.3 dB at low frequency and Nyquist, respectively. This shows that multi-GS/s pipeline ADCs are feasible as key building blocks in interleaved structures.**

***Index Terms*—Analog-to-digital converter (ADC), CMOS analog integrated circuits, current-mode, data converter, foreground digital calibration, high speed, low power, pipeline.**

I. Introduction

THE ever-increasing demands on communication capacity leads to a need for very high sample rate analog-to-digital converters (ADCs). For optical networks, with wavelength division multiplexing, data rates of 100 Gb/s per channel are under development. For such systems, more advanced modulation schemes requires moving from slicers (1-bit ADCs) to multi-bit ADCs with the least stringent ADC requirement being 27 GS/s sample rate at 6-bit resolution [1]. In order to reduce cost by relaxing fiber requirements, also 10 Gb/s optical links will need ADCs [2]. Even for radio links data rates of 10 Gb/s or more are strived for [3]. ADCs with sample rates of 10+ GS/s are implemented by interleaving sub-ADCs with lower rate. The sub-ADCs are of various types, e.g. flash [4], successive approximation (SAR) [5]–[7] or pipelined [2], [8], [9]. Flash converters typically have a large input capacitance, which puts severe constraints on the driving capacity of the pre-driver. SAR converters, on the other hand, perform binary search in a serial manner, thus being relatively slow and requiring a larger number of interleaved sub-ADCs. This leads to both higher complexity of the interleaving function and large demands on pre-driver capacity. In contrast, pipeline ADCs constitute both low input capacitance and high sample rate, whereas the power efficiency is often lower than for SAR ADCs.

The use of a high-speed pipeline sub-ADC for interleaving thus results in a lower aggregate input capacitance and a reduced interleaving factor, which offer benefits of reduced power dissipation and complexity of the interleaving process. The input capacitance is bound only by thermal noise constraints [10] and high speed can be achieved, as we will show in this paper. Together with better energy efficiency than what is traditionally achieved in high-speed pipeline ADCs, these benefits would make the high-speed pipeline ADC architecture suitable for interleaving to facilitate the high sample rates needed in 10, 40, and 100 Gb/s transmissions.

This test-chip of a 2.4 GS/s single-channel 8-bit pipeline ADC [11] explores the possibilities to achieve very high sample rates with the pipeline architecture The high sample rate is achieved through a fully differential, open-loop current-mode amplifier with common-mode balancing, which allow fast settling times and easy integration of the DAC. The use of the early decision scheme [12] removes the comparator latency from the critical path and the resulting sample rate of 2.4 GS/s is, to the authors' best knowledge, significantly faster than any previously reported single-channel pipeline ADC [2], [8], [13].

In Section II, the ADC architecture is described together with an analysis of the timing bounds on the early decision scheme. Section III presents the detailed circuit implementations, describing the design of the input stage, sample-and-hold (S/H), MDAC stages and the comparator. The digital calibration principle and measurement results are presented in Section IV and the paper is concluded in Section V.

II. ADC Architecture

The pipeline ADC, shown in Fig. 1, comprises a double-sampling sample-and-hold (two time-interleaved track-and-hold (T/H) stages), six pipeline stages and a flash ADC with all stages being differential. The T/H stage keeps the input signal to the first pipeline stage constant during one clock cycle. Each pipeline stage, shown in Fig. 2, consists of a 1.5-bit sub-ADC (two comparators followed by latches), two double-sampling S/H stages and a differential MDAC. The MDAC stage (see Fig. 8) is a time-continuous, open-loop, current-mode amplifier performing common-mode balancing, signal gain and subtraction of the DAC values. The double-sampling S/H samples the input signal once per clock period while simultaneously holding the previously sampled data constant at the output throughout the entire clock period T. As the MDAC is implemented with an open-loop amplifier, double-sampling is required to process data the entire clock period.

A. Comparator Timing

If the time used in one clock period is shared between the comparator decision time and the settling time of the MDAC,

Manuscript received November 10, 2010; revised January 26, 2011; accepted March 01, 2011. Date of publication May 23, 2011; date of current version June 24, 2011. This paper was approved by Guest Editor Angel Rodriguez-Vazquez.

The authors are with the Department of Electrical Engineering, Linköping University, 581 83 Linköping, Sweden (e-mail: timmy@isy.liu.se; chs@isy.liu.se; atila@isy.liu.se).

Digital Object Identifier 10.1109/JSSC.2011.2143811

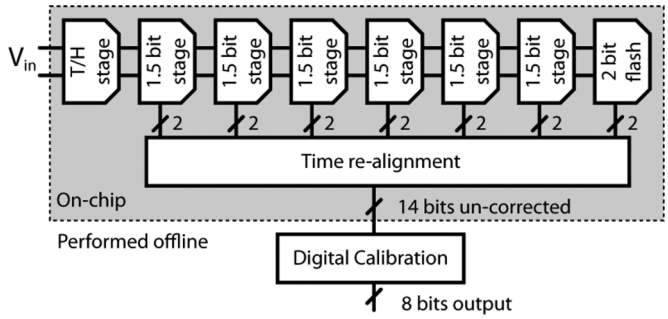

Fig. 1. Architecture of the pipeline ADC.

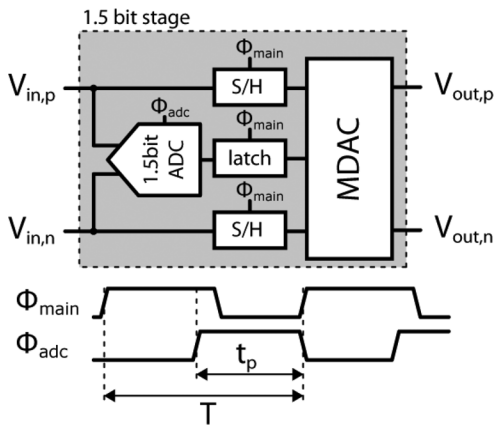

Fig. 2. 1.5-bit pipeline stage with the associated timing diagram.

the actual time used for the MDAC settling would depend on the input signal, as the comparator decision time is signal dependent [8]. As long as the outputs settle to the desired accuracy this is not a problem. However, when operating at gigasample-per-second rates this would lead to incomplete settling, which causes variations in the stage gain depending on the decision time of the comparator. This can be circumvented by the use of the look-ahead technique [2], [8], [14] where a sub-ADC with a higher resolution is used to determine the digital output of the subsequent stage. This will make sure that the comparator decision is available at the start of the clock period. The early decision scheme [12], used in this work, uses a sub-ADC with nominal resolution, placed in front of the S/H, that will take its decision on the incompletely settled output from the previous stage at a time $\mathrm{t_p}$ before this data is sampled.

At the rising clock edge the S/H circuit samples its input and feeds it to the MDAC. As the sub-ADC is clocked earlier, the digital outputs from the comparators can be latched at the same clock-edge as the S/H. This makes both the analog and digital inputs available to the MDAC at the start of the clock period. The MDAC then has the entire sample period, T, available for settling. After time $\mathrm{T} - \mathrm{t_p}$, the outputs have settled enough to be used by the sub-ADC in the following stage. Finally, at time T the output is latched by the following stage. The entire clock period is then used as follows. For the analog-to-digital path, it is used for limited MDAC settling plus comparator decision time. The time during limited settling (0 to $\mathrm{T} - \mathrm{t_p}$) is also used for comparator reset. For the analog signal path, the full clock cycle is used for MDAC settling.

Redundancy in pipeline ADCs, explained in Fig. 3, is achieved by overlapping the transfer functions for the different ADC decisions. This allows for offset in the sub-ADC comparators within the redundancy margin, without overdriving the MDAC output. In this design the redundancy margin budget is divided between allowed comparator offset and what is used to allow the comparators to take their decision on the incompletely settled MDAC outputs. The time from the end of the clock period to when the comparators are clocked, $\mathrm{t_p}$, can now be bound upwards. Fig. 4 shows the settling output of an MDAC stage during one clock period. This waveform corresponds to the worst-case scenario, which will determine how early the comparators can be clocked. The settled voltage shown in the figure will result in an out of range MDAC output if a wrong comparator decision is taken. Therefore, before the sub-ADC can be clocked, the voltage needs to have settled sufficiently in order to have crossed the actual threshold as given by the nominal threshold plus comparator offset. By budgeting half of the redundancy margin to the offset of the comparators, the required settling time, $\mathrm{t_{settled}}$, can be expressed in terms of the settling time constant of the MDAC, τ_{MDAC}, through the equation for linear settling:

$$\frac{V_{\mathrm{FS}}}{8} = \frac{3}{2} V_{\mathrm{FS}} e^{-\frac{\mathrm{t_{settled}}}{\tau_{\mathrm{MDAC}}}}. \tag{1}$$

Here $\mathrm{V_{FS}}/8$ corresponds to the difference between the worst-case threshold and the final voltage value. $3\mathrm{V_{FS}}/2$ is the worst-case voltage difference between the initial voltage and the final settled voltage, a smaller difference can not result in out of range errors and a larger difference will settle faster. Solving for $\mathrm{t_{settled}}$ then gives

$$\mathrm{t_{settled}} = 2.5\tau_{\mathrm{MDAC}}. \tag{2}$$

B. Metastability Analysis

Besides the limit on how early the comparators can be clocked, there is also a bound on how late they can be clocked. This bound is determined by the probability and impact of metastable outputs of the comparator. Metastability [15], as exemplified in Fig. 5, occurs when the comparators does not have enough time to regenerate a small input level to sufficient digital voltage levels. The problem with metastability is that the comparator output can be interpreted differently when several gates are connected to the output. In the specific case of the pipeline MDAC, the comparators control the DAC output level. Metastability could result in an unknown DAC output level and as a large random component is then added to the analog output, the signal information in the analog output of the pipeline stage is destroyed.

In [16], metastability was analyzed for SAR ADCs, developing a model to quantify the effect of metastability by calculating the resulting signal-to-metastability-error ratio (SMR). The metastability analysis is adapted here to pipeline ADCs and it consists of two parts, the probability for a metastable event to occur and the impact of such an error when it occurs.

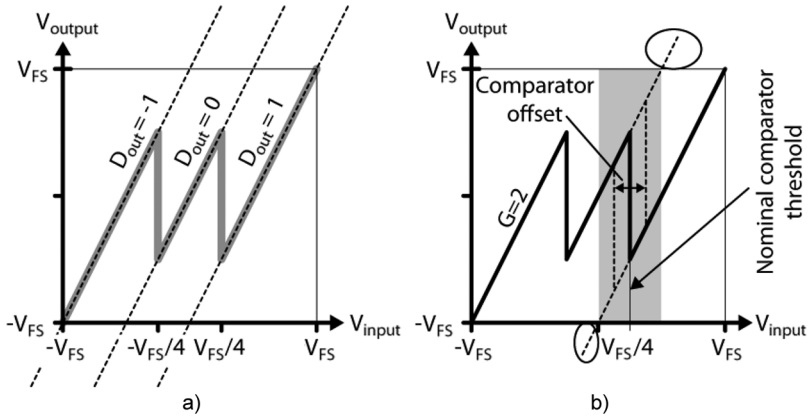

Fig. 3. Redundancy in the pipeline stages with (a) the transfer functions (dashed lines) for the three possible digital inputs and corresponding DAC levels as well as the aggregate transfer function (thick grey) when using comparators with the nominal threshold voltages. (b) The effect of offset in the comparators and the redundancy margin shown in grey. Highlighted with circles are the input/outputs that can cause out of range voltages when having comparator offsets larger than what is tolerated by the redundancy.

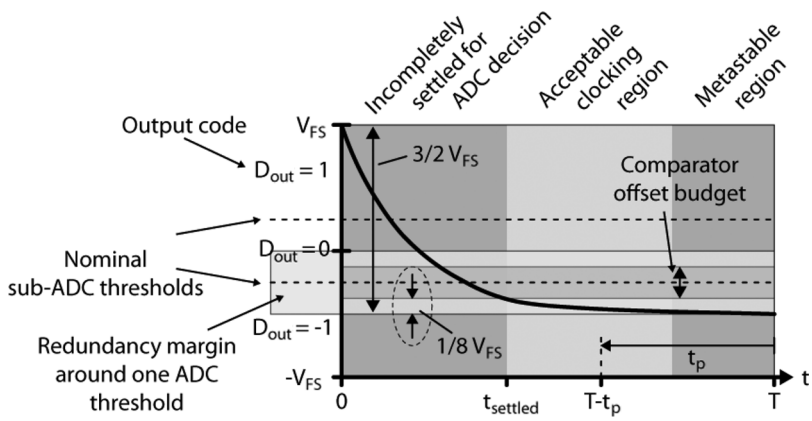

Fig. 4. The worst-case settling output, which determines how early the comparators can be clocked. $t_{settled}$ is determined by when the output is guaranteed to have crossed the sub-ADC comparator thresholds, which is restrained by the offset budget.

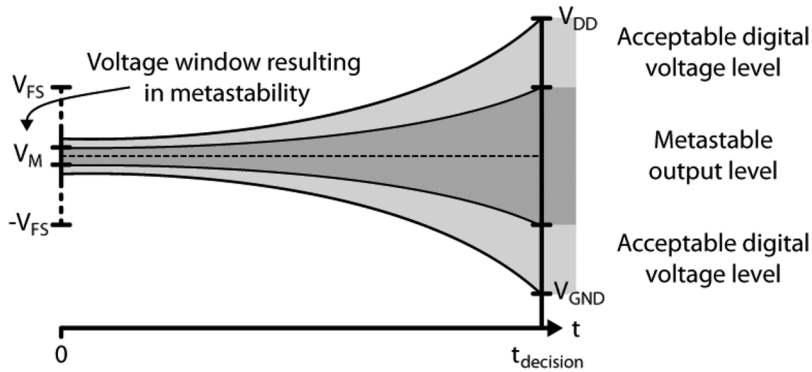

Fig. 5. Metastability occurs when the comparator does not have enough time to amplify a small voltage difference at the input to acceptable voltage levels for digital logic.

The voltage difference at the input of the comparator will be exponentially amplified by the comparator latch, as was shown in Fig. 5. If the resulting differential output fails to reach acceptable logic levels, defined as, e.g., $|\mathrm{V_{diff}}| > 0.5\mathrm{V_{dd}}$, the latch following the comparator will take too long time to regenerate the output to full swing, making the output metastable. The relative input range that cause metastability, $\mathrm{M_W}$, is the ratio between the metastability voltage window and the differential input voltage range, $2\mathrm{V_{FS}}$. Based on the allowed comparator decision time $\mathrm{t_{decision}}$, comparator time constant τ_{comp}, supply voltage and full-scale input range, $\mathrm{M_W}$, can be expressed as

$$M_{\mathrm{W}} = \frac{1}{2V_{\mathrm{FS}}} \frac{V_{DD}}{2} e^{-\frac{\mathrm{t_{decision}}}{\tau_{\mathrm{comp}}}}. \quad (3)$$

The probability for metastability can then be approximated as $2M_W$ as there are two comparators in each stage.[1]

Metastability could result in the addition of a large noise component at the analog output of the pipeline stage. Therefore, when metastability occurs in pipeline stage i (where the first stage corresponds to $i = 1$), the digital output of that stage contains only one useful bit and the following stages do not contain any information of the signal. In stage i, the input signal is close to a reference level, which gives the input-referred maximum amplitude error as

$$A_{M,i} = \frac{\frac{3}{4}V_{FS}}{G^{i-1}}. \quad (4)$$

$3V_{FS}/4$ comes from the difference between an input voltage near a threshold and the worst case produced output. As one bit still contains useful information this is given by the difference between the nominal thresholds, $V_{FS}/2$, plus the redundancy margin for each threshold, $V_{FS}/8$. Using a gain of two, the total metastability error power can then be expressed as

$$P_M = \sum_{i=1}^{n} 2M_W(A_{M,i})^2 = \sum_{i=1}^{n} \frac{9}{2}M_W V_{FS}^2 2^{-2i}. \quad (5)$$

SMR is defined as the ratio between the power of a full-scale sinusoidal signal to the metastability error power. Using the asymptotic value of the sum, this can be simplified to

$$\mathrm{SMR} = 10\log\left(\frac{\frac{V_{FS}^2}{2}}{P_M}\right) \approx 10\log\left(\frac{1}{M_W}\right) - 5\ \mathrm{dB}. \quad (6)$$

Fig. 6 plots SMR versus comparator decision time for the time constants acquired through simulating the extracted comparator layout in the nominal, fast and slow process and temperature corners. Shown in this figure is also the 49.9 dB limit, which corresponds to 8 effective bits of SNDR, as well as the minimum decision times, $t_{decision,min}$, required for the SMR to be larger than this limit.

The required timing constraints and potential operating frequency, given by the simulated time constants in the different process corners is summarized in Table I. The actual comparator decision time before the sampling edge, t_p, is then bound by the required settling time and the minimum comparator decision time:

$$t_{decision,min} < t_p < T - t_{settled}. \quad (7)$$

In this case we have used SMR as the determining criterion on how to limit the comparator decision time. In some applications, bit error rate (BER) at the ADC level should be used to determine minimum comparator decision times [1], [2], [5].

The actual hardware implementation of the MDAC has an impact on the effect of metastability. The presented analysis of the induced error is only valid for the proposed implementation. If the DAC levels are shared between the pipeline stages there is a possibility that metastability affects several samples in time as the pipeline stages simultaneously process different time instances of the signal, lowering SMR and causing consecutive bit errors in serial links.

[1]This is based on two assumptions, that the probability density function (PDF) is uniform and that the PDF of the input signal is the same for all pipeline stages. The PDF can be approximated as uniform in a vicinity of the reference levels for both sinusoidal and wideband signals with sufficiently large signal swings. In the presence of redundancy, the output PDF will be different from the input PDF due to superposition near the references. Both an analytical model with a uniform PDF and Monte Carlo simulations with sinusoidal inputs show that the impact on the SMR is about 1 dB.

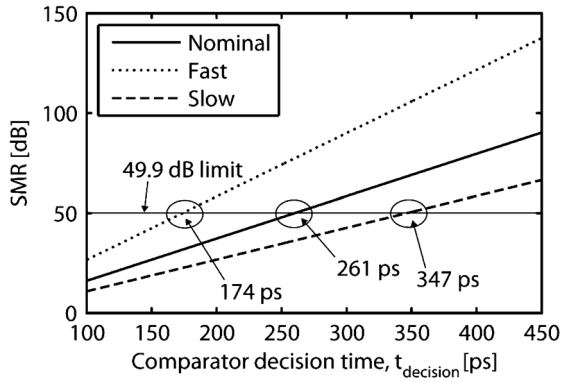

Fig. 6. SMR versus comparator decision time for the nominal, fast and slow process corners with the time constants from simulating the extracted layout. Also shown is the 49.9 dB limit, which corresponds to 8 effective bits of SNDR.

TABLE I
SUMMARY OF THE COMPARATOR TIMING REQUIREMENTS FOR THE DIFFERENT PROCESS CORNERS TOGETHER WITH THE SIMULATED TIME CONSTANTS INCLUDING EXTRACTED PARASITICS

Process corner	τ_{MDAC}	τ_{comp}	$t_{settled}$	$t_{decision,min}$	$F_{max} = 1/(t_{settled}+t_{decision,min})$
Fast	35 ps	13.7 ps	88 ps	174 ps	3.8 GS/s
Nominal	40 ps	20.5 ps	100 ps	261 ps	2.8 GS/s
Slow	80 ps	27.3 ps	200 ps	347 ps	1.8 GS/s

III. CIRCUIT IMPLEMENTATION

With the sub-ADC of the first pipeline stage being located in front of the S/H, an additional input T/H stage that was shown in Fig. 1 is needed in order not to have the input signal vary from the time instant of the sub-ADC decision to the time the pipeline stage S/H samples the data. The T/H employs double-sampling [17] and buffers are implemented using pMOS source followers. The distortion caused by these buffers is partially compensated in the digital calibration.

A single-ended clock enters the chip and through a current-controlled buffer chain the duty cycle can be tuned. The non-overlapping clock signals are then generated from this buffered clock while the comparator clock signals are generated by delaying the clock through another current-starved buffer, so that the comparator delays can be tuned for the measurement. The clock generation is close to the front-end S/H and is then distributed to the other stages.

A. Sample-and-Hold

Each pipeline stage should process a data sample each clock cycle. Because the entire clock period is dedicated to the MDAC settling time, double-sampling is used as shown in Fig. 7. The

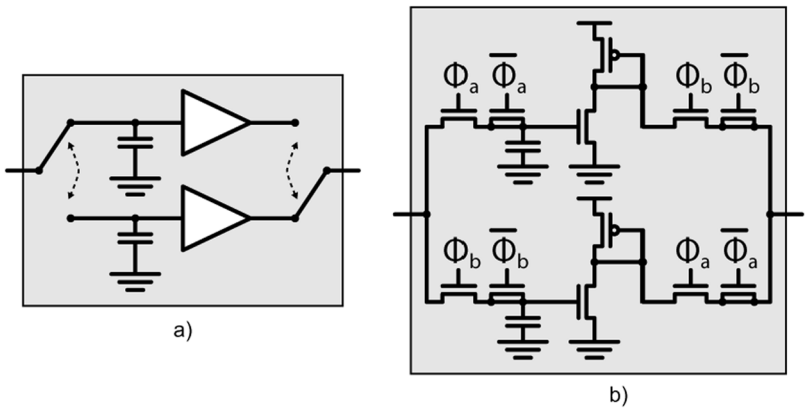

Fig. 7. Double-sampled S/H: (a) illustration and (b) circuit implementation.

S/H stage includes four nMOS switches and two current-mode buffer stages. These buffers serve two purposes. The first is to prevent harmful charge sharing between the sampling capacitance and the input capacitance of the MDAC while the second is to convert an nMOS signal level, at the input, to a pMOS signal level, at the output. If the output pMOS is driving another pMOS with the same size, the gain is nominally one, as the currents in the two cases are the same. In order to control the common-mode level disturbance caused by clock feedthrough and channel charge injection of the switch transistors, dummy transistors clocked with the opposite phase are used. The switches are controlled by non-overlapping clock signals.

B. MDAC

The differential MDAC is shown in Fig. 8. Here we use a differential input signal ($\mathrm{V_{SH,p}} = \mathrm{V_{CM}} + \Delta\mathrm{V}$, $\mathrm{V_{SH,n}} = \mathrm{V_{CM}} - \Delta\mathrm{V}$) at pMOS levels, driving a p-to-n-stage, where the pMOS levels are converted to nMOS levels, making both available. In the following stage, $\mathrm{M_{3p}}$ adds a current from $\mathrm{V_{in,p}}$ to the output node and $\mathrm{M_{5p}}$ subtracts a current from $\mathrm{V_{in,n}}$ from the same node. Therefore we create $\mathrm{V_{in,p}} - \mathrm{V_{in,n}} = 2\Delta\mathrm{V}$, the input signal doubled with common-mode removed. Furthermore, $\mathrm{M_{4p}}$ and $\mathrm{M_{6p}}$ act as a DAC and can add or subtract an appropriate current to the output node. The gate voltages of these are either connected as the secondary side of a bias current mirror or to the supplies, depending on the sub-ADC decision. The use of both nMOS and pMOS DAC transistors allows a differential voltage to be both added and subtracted to the output while leaving the common-mode level unchanged. $\mathrm{M_{7p}}$ is used to set the output common-mode level while $\mathrm{M_{8p}}$ finally constitutes the load of this stage, creating an output voltage with nMOS levels.

Due to the use of minimum channel length transistors in a nanoscale CMOS process, which is required to achieve a high $\mathrm{f_T}$, the output conductance of the transistors is large, i.e., $\mathrm{g_m}/\mathrm{g_{ds}}$ is low. This affects the gain of the pipeline stage and the relative width of the transistors is sized in order to achieve the nominal gain of two. As the relative transistor widths has a direct impact on the stage gain their absolute value needs to be increased to reduce mismatch. For transistor widths of 10 to 60 μm in the MDAC, the standard deviation of the gain, simulated through Monte Carlo analysis of the extracted layout, is $\sigma_{\mathrm{gain}} = 0.2$.

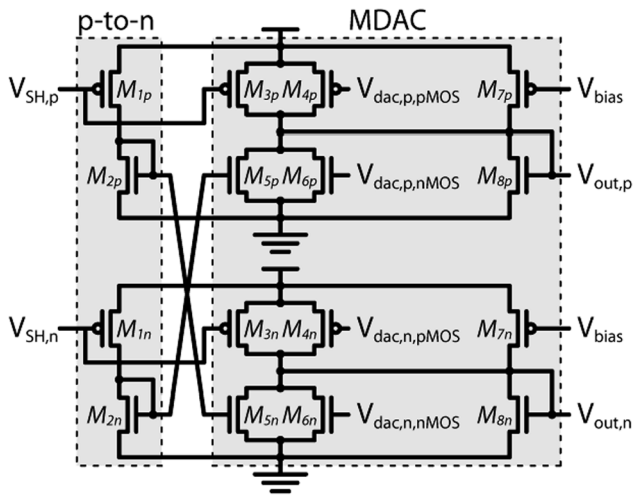

Fig. 8. Differential MDAC implementation.

The output conductance also has an impact on the common-mode rejection. The simulated common-mode attenuation for one MDAC stage is between 5 to 10 dB within full-scale input range, which prevents the common-mode level from being amplified throughout the pipeline chain.

C. Voltage Swing

The voltage swing in this design is limited by the fact that we need to bias the transistors above a minimum gate voltage ($\mathrm{V_G} > \mathrm{V_M}$) and also to keep them in saturation. Consider for example the low input voltage, $\mathrm{V_L}$, to the nMOS $\mathrm{M_{5p}}$. Its gate voltage thus needs to exceed $\mathrm{V_M}$, given by the minimum required $\mathrm{f_T}$ of the transistor. For the high input voltage, $\mathrm{V_H}$, symmetry and having an identical input range for all stages, will cause the output voltage over the MDAC load to be equal to the low voltage $\mathrm{V_L}$. The transistor terminal voltages must be such that the transistor still remains in saturation. Simulations indicate that an nMOS DC level of 350 mV with a single-ended swing of 240 mV provides reasonable performance while not dissipating an excess of static power.

D. Comparator

The comparator used in the sub-ADC is shown in Fig. 9. It is a differential-pair comparator based on the StrongARM

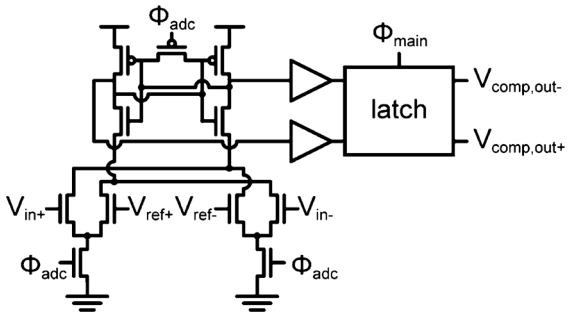

Fig. 9. Differential pair comparator based on the StrongARM sense-amplifier latch.

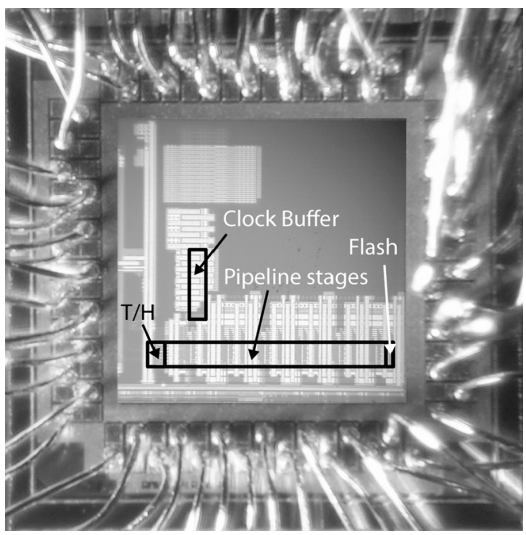

Fig. 10. Chip micrograph.

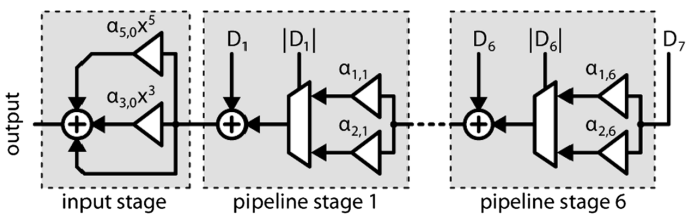

Fig. 11. Digital calibration principle.

sense-amplifier latch [18]. The important design criteria for the comparator are the mismatch-induced offset and speed. As the comparator was allocated half of the redundancy margin budget for the offset it needs to be kept within ±30 mV. The standard deviation of the offset was kept low by increased device sizes and careful layout. The regeneration time constant of the comparator is mostly determined by the process; using minimum size buffers means that the comparator speed is kept high. The latches following the comparator are clocked. As the digital outputs needs to be available at the beginning of the next clock period no additional time is given to these latches to suppress metastability.

E. Noise Analysis

Following the studies in [10], the sampling capacitor is dimensioned according to the thermal noise requirements.

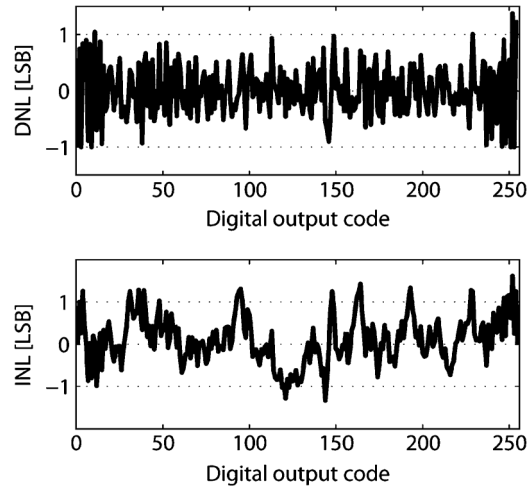

Fig. 12. Measured DNL and INL.

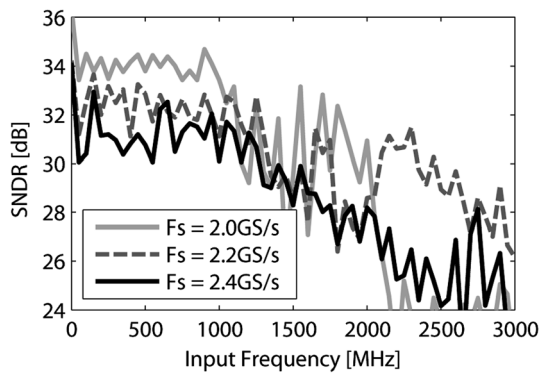

Fig. 13. Measured SNDR vs. input frequency for sample rates up to 2.4 GS/s.

The first sampling capacitor, in the T/H stage, is driven by two transistors, each with transconductance g_{mTH} and an output impedance of $1/g_{mTH}$. The noise current squared into the load is $2 \cdot 4\gamma kTg_{mTH}B$, where γ is the transistor noise factor (assumed 1.5 [19]) and B is the noise bandwidth. With $B = g_{mTH}/4C_s$ this leads to a noise voltage squared at the output of $2\gamma kT/C_s$, which can be seen as an equivalent input-referred noise voltage as the gain of this stage is 1. The next sampling capacitor (in the S/H of the first pipeline stage) is driven by the output buffer of the T/H circuit, leading to another equivalent input-referred noise voltage squared of $2\gamma kT/C_s$. The third sampling capacitor (in the second stage S/H) is controlled by the MDAC output, which is driven by the S/H buffer. This means that we have eight transistors generating noise current to this capacitor (assuming both DAC transistors off). Assuming that they have about the same g_m, they will give rise to a noise current squared of $8\gamma kTg_mB$. With a load impedance of $1/g_m$ (MOS diode M_{8p}) and noise bandwidth of $g_m/4C_s$ the noise voltage squared is $8\gamma kT/C_s$. Note that there is a gain of 2 in this stage, so the equivalent input-referred noise voltage squared is $2\gamma kT/C_s$. For the further stages in the chain, the equivalent input-referred noise voltage is reduced by $4\times$ due to their gain, making their importance small. Totally we estimate the equivalent input-referred noise voltage squared to $6\gamma kT/C_s$. With a voltage swing of $V_{FS} = 240$ mV

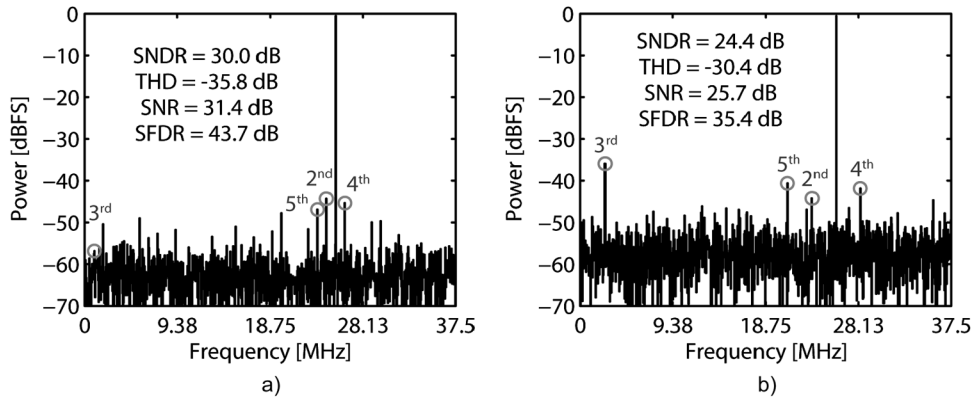

Fig. 14. Measured 2 K-point FFT spectrum, sampled at 2.4 GS/s and down-sampled a factor 32. The spectrum corresponds to the data points of a) $\mathrm{F_{in}} = 550\ \mathrm{MHz}$ b) $\mathrm{F_{in}} = 2350\ \mathrm{MHz}$ from Fig. 13 with the harmonics indicated by circles.

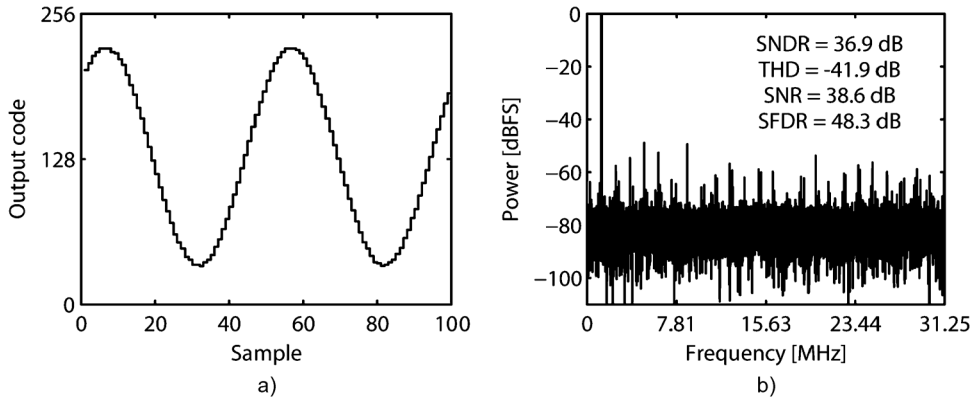

Fig. 15. Measured output sampled at 2.0 GS/s and down-sampled a factor 32 with $\mathrm{F_{in}} = 1.25\ \mathrm{MHz}$ showing a) waveform indicating only minor disturbances and b) 16 K-point FFT spectrum.

(single-ended) we have a quantization noise voltage squared of $\mathrm{v_q^2} = \mathrm{V_{FS}^2} 2^{-2\mathrm{n}}/12$. Equalizing the quantization noise and the estimated thermal noise for $\mathrm{n} = 8$ bits gives $\mathrm{C_s} = 510$ fF for the single ended case. For the differential case, noise squared is doubled and $\mathrm{V_{FS}^2}$ is quadrupled, making $\mathrm{C_s}$ half of the above value, 255 fF. We have chosen to implement $\mathrm{Cs} \approx 250$ fF (including parasitics).

IV. Evaluation and Measurement Results

The prototype pipeline ADC has been designed and fabricated in a general purpose 65 nm CMOS process and the die photo is shown in Fig. 10. The active area of the ADC core occupies 0.65×0.07 mm^2. A full implementation will require additional area, particularly for the digital calibration logic but also for reference generation, which, for this test-chip, is performed off-chip. The references are decoupled on the PCB as well as on-chip before being buffered to provide the necessary driving impedance.

A. Digital Calibration

As the gain of the pipeline stages are hard to control and will vary from process variations and mismatch, calibration and correction of the errors is performed. For this prototype ADC, it is not performed on-chip but implemented offline. The calibration principle is shown in Fig. 11 and follows a concept similar to [20]. The calibration works by correcting for gain errors in the pipeline stages as well as nonlinear distortion in the input T/H stage. Each pipeline stage is modeled by two parameters, one estimating the gain for the stage when the DAC is either adding or subtracting current ($\mathrm{D_{out}} = -1$ or 1) and another parameter for when DAC does neither ($\mathrm{D_{out}} = 0$). As the MDAC is the dominant source of gain errors the buffers in the time-interleaved S/H are, together with the MDAC, treated as one channel. In the input stage, the nonlinear distortion is modeled using two parameters, compensating for the 3rd and 5th order distortions. Working backwards, the digital output of the flash stage, $\mathrm{D_7}$, is multiplied by the two gain parameters, corresponding to the reciprocal of the gains from stage 6. Depending on the digital output of that stage (which indicates the DAC output) one of these two outputs is chosen by a multiplexer and the digital output from stage 6 is added. This continues to the input stage, where the partial result, taken to the power of 3 and 5, are multiplied with their respective coefficient and summed with the original output from stage 1 to generate the final output. The resolution of the calibration parameters were set to eight bits for the input and first stage, seven bits for the second stage down to three bits for the last pipeline stage.

B. Measurement Results

For the measurement, the chip was bare-bonded on to the PCB, and the digital output signals are down-sampled by a

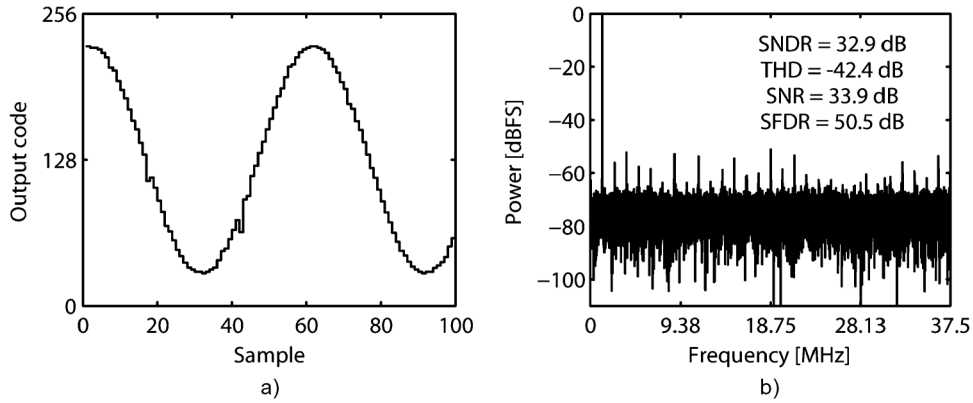

Fig. 16. Measured output sampled at 2.4 GS/s and down-sampled a factor 32 with $F_{in} = 1.25$ MHz showing a) waveform with visible metastability-induced impulse noise and b) 16 K-point FFT spectrum.

factor of 32 for increased signal integrity. This down-sampling factor is programmable between 1 and 32.

First, the value of the calibration parameters are estimated using a low-frequency input signal, based on maximizing the SNDR of the measured output data. For a 2.4 GS/s data set, the SNDR increased from 23.5 to 34.1 dB after calibration. Based on 2 chip samples the stage gains had a mean value of 1.89 and a standard deviation of 0.12. Although based on a small sample size, this could be compared to the simulated standard deviation of 0.2.

The resulting DNL and INL after calibration are shown in Fig. 12. Using these parameters Fig. 13 shows the SNDR versus input frequencies for sample rates up to 2.4 GS/s while operating at a supply voltage of 1.0 V.

At 2.4 GS/s, the SNDR, measured at a low input frequency, is 34.1 dB. The SNDR stays above 30.1 dB throughout the Nyquist band and is 31.3 dB at the Nyquist frequency. The higher resolution at low input frequencies can be explained by the fact that it is at these frequencies that the calibration was performed. The power dissipation of the entire ADC including output buffers is 318 mW and is measured for a Nyquist rate input signal. Out of this, 94 mW is used for clocking, 181 mW for the pipeline chain, 34 mW for the input stage and 9 mW for driving the outputs. Part of the high clock power is a result of an oversized buffer for the digital clock network. This will be able to support the pipeline registers needed for implementing the digital calibration logic at 2.4 GS/s. However, the extra clock load and the switching power that will be dissipated in the calibration logic are not included and will therefore increase the total power for a full implementation.

Fig. 14 shows the FFT spectrum associated with the measurement points that has the lowest SNDR in the first and second Nyquist zones for the sample rate of 2.4 GS/s. It can be seen that the harmonic distortion is significant. However, the dominant source of error is noise. The thermal noise level is then estimated by measuring the SNDR versus input amplitude at a low input frequency. It is measured to be more than 50 dB below the full-scale input power, which corresponds well to the theoretical level discussed in Section III. Simulations with better models of the ground and power network indicate that the performance is limited by coupling through the substrate and supplies, generating signal dependent distortion and inter-sample interference, degrading both total harmonic distortion (THD) as well as signal-to-noise ratio (SNR). The increased noise floor is also the source for the significant SNDR degradation for some measurement points of Fig. 13.

TABLE II
PERFORMANCE SUMMARY

Technology	65nm CMOS
Supply voltage	1.0 V
Sample rate	2.4 GS/s
SNDR	>30.1 dB up to F_{in}=1.2 GHz 34.1 dB at F_{in}=0.1 MHz 31.3 dB at F_{in}=1.2 GHz
SNR	36.0 dB at F_{in}=0.1 MHz 32.9 dB at F_{in}=1.2 GHz
THD	-38.6 dB at F_{in}=0.1 MHz -36.3 dB at F_{in}=1.2 GHz
SFDR	43.8 dB at F_{in}=0.1 MHz 40.7 dB at F_{in}=1.2 GHz
Max DNL	+1.4 / -1.0 LSB
Max INL	+1.6 / -1.3 LSB
Analog core power dissipation	Clock 94 mW Pipeline Chain: 181 mW Input Stage: 34 mW Output buffers: 9 mW Total: 318 mW
ADC analog core area	0.6 mm x 0.07 mm

At increased sample rates, the probability for metastability increases, which can be seen in Fig. 15 and Fig. 16 showing the output waveforms and associated FFT spectrum, sampled at 2.0 GS/s and 2.4 GS/s, respectively. At 2.4 GS/s, metastability

TABLE III
COMPARISON TO STATE-OF-THE-ART PIPELINE ADCS

Author/ Year	Architecture	CMOS Process	Sample Rate (GS/s)	Channel Rate (GS/s)	SNDR @ DC	$SNDR_{min}$ DC-Nyquist	Power Dissipation (mW)
Shen [13] JSSCC-07	Pipeline	0.18µm	0.8	0.8	33.7	31.5	105
Varzaghani [8] JSSCC-09	Interleaved Pipeline	0.13µm	4.8	1.2	30.4	30.0	300
Nazemi [2] VLSI-08	Interleaved Pipeline	90nm	10.3	1.3	36.6	32.4	1600
This Work	**Pipeline**	**65nm**	**2.0** **2.2** **2.4**	**2.0** **2.2** **2.4**	**36.4** **34.2** **34.1**	**33.4** **31.1** **30.1**	**294** **310** **318**

has a significant impact on the noise level, and above this sample rate, it vastly reduces SNDR.

The measurement results are summarized in Table II and a comparison with state-of-the-art pipeline ADCs with high channel rates is done in Table III. It can be seen that this ADC achieves a sample rate almost twice that of previously reported single-channel pipeline ADCs. The power dissipation indicates a figure-of-merit (FoM), defined as, for example, $\mathrm{FoM} = \mathrm{P}/(2^{\mathrm{ENOB@Nyquist}} \cdot \mathrm{f_S})$, slightly worse than other high-speed pipeline ADCs. However, the addition of the digital calibration logic will increase the power dissipation and therefore reduce the energy efficiency.

V. CONCLUSION

A test-chip of a single-channel 8-bit pipeline ADC with a sample rate of 2.4 GS/s has been presented. The high sample rate is achieved through a fully differential, open-loop current-mode amplifier with common-mode balancing, which allow fast settling times and easy integration of the DAC. In addition, the use of the early decision scheme removes the comparator latency from the critical path. The sample rate of the proposed pipeline ADC is, to the authors' best knowledge, faster than any other reported CMOS single-channel pipeline ADC. The actual implementation demonstrated the expected thermal noise level, but other noise sources limit SNDR to about 30 dB throughout the Nyquist band. Simulations indicate that these sources are due to crosstalk over substrate and supply. Measurements show that the sample rate is limited by metastability noise. The open-loop MDAC requires relatively large transistors to achieve reasonable gain accuracy, leading to a relatively large power consumption of 318 mW and a need for digital calibration.

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Timmy Sundström (S'07) received the M.Sc. degree in applied physics and electrical engineering from Linköping University, Linköping, Sweden, in 2005, where he is currently working toward the Ph.D. degree in electrical engineering in the Department of Electrical Engineering.

Since March 2006, he has been a Member of the electronic devices research group of the Department of Electrical Engineering, Linköping University. His research interests include process-variation-tolerant high-speed low-power analog-to-digital converters.

Christer Svensson (M'97–F'03) was born in Boras, Sweden, in 1941. He received the M.S. and Ph.D. degrees from Chalmers University of Technology, Gothenburg, Sweden, in 1965 and 1970, respectively.

From 1965 to 1978, he was with Chalmers University of Technology, where he researched on MOS transistors, nonvolatile memories, and gas sensors. Since 1978, he has been with the Department of Electrical Engineering, Linköping University, Linköping, Sweden, where since 1983, he has been a Professor of electronic devices. He initiated a new research group on integrated-circuit design. He pioneered the fields of high-speed CMOS design in 1987 and low-power CMOS in 1993. He founded several companies, for example, Switchcore (publ.) and Coresonic, where he also serves as the Director. He has published more than 180 papers in international journals and conferences. He is the holder of 15 patents. His present interests include high-performance and low-power analog and digital CMOS circuit techniques for computing, wireless systems, and sensors.

Dr. Svensson is a member of the Royal Swedish Academy of Sciences and the Royal Swedish Academy of Engineering Sciences. He was the recipient of the Solid-State Circuits Council 1988–1989 Best Paper Award.

Atila Alvandpour (M'99–SM'04) received the M.S. and Ph.D. degrees from Linkoping University, Sweden, in 1995 and 1999, respectively.

From 1999 to 2003, he was a senior research scientist with Circuit Research Lab, Intel Corporation. In 2003, he joined the Department of Electrical Engineering, Linköping University, as a Professor of VLSI design. Since 2004, he is the head of the Electronic Devices division. He is also the coordinator of the Linköping Center for Electronics and Embedded Systems (LINCE). His research interests include various issues in design of integrated circuits and systems in advanced nanoscale technologies, with a special focus on efficient analog-to-digital data converters, wireless transceiver front-ends, sensor interface electronics, high-speed signaling, on-chip clock generators and synthesizers, low-power/high-performance digital circuits and memories, and chip design techniques. He has published about 100 papers in international journals and conferences, and holds 24 U.S. patents.

Prof. Alvandpour is a senior member of IEEE, and has served on many technical program committees of IEEE and other international conferences, including the IEEE International Solid-State Circuits Conference (ISSCC) and the European Solid-State Circuits Conference (ESSCIRC). He has also served as a guest editor for the IEEE Journal of Solid-State Circuits.