A 2.4GHz 40mW 40dB SNDR/62dB SFDR 60MHz Bandwidth Mirrored-Image RF Bandpass ΣΔ ADC in 90nm CMOS

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***Abstract*—A 6th order RF bandpass ΣΔ ADC operating on the 2.4GHz ISM band is presented. The bandpass loop filter is based on digitally programmable Gm-LC resonators. By using a mirrored-image sampling technique, the clock frequency is reduced to 3GS/s, thereby reducing the power consumption. Implemented in a standard 90nm CMOS process, the IC achieves 40dB and 62dB of SNDR and SFDR respectively on a 60MHz bandwidth with 40mW of power consumption.**

I. Introduction

Steered by CMOS scaling, wireless radios are becoming increasingly digital intensive. This evolution has revived the suggestion of shifting the signal conditioning of the analog receiver chain to the digital domain by placing a high speed ADC as close as possible to the antenna [1]. By digitizing at RF, this architecture naturally becomes a native software radio, nicely scaling with CMOS technologies. Obviously, the very high speed and the large dynamic range required make the design of the ADC very challenging.

Flash ADCs can operate today at GHz speeds but their resolution remains limited to a few (~5-6) bits [2]. By placing the flash converter in a ΣΔ loop, the oversampling ratio and the order of the loop filter provide a higher resolution in a limited bandwidth. Therefore, a bandpass ΣΔ (BP–ΣΔ) ADC centered at the desired RF input signal appears as an ideal candidate for an RF ADC architecture. Moreover, the bandwidth of the converter can be made large enough to capture a complete RF band at once and allow multiple channels to be simultaneously processed. Several RF BP–ΣΔ ADC have been proposed in the literature [3-5] but they suffer from very high power consumption and are not implemented in a standard CMOS process. Both of these aspects limit their potential for competing with classical receiver architectures.

In this work, we propose the design of an RF BP–ΣΔ ADC realized in a standard 90nm CMOS technology and consuming only 40mW. Several techniques are used to achieve this low power consumption. First we exploit the mirrored-image technique [6] which allows a reduction of the clock frequency. This technique has been a major enabler for this order of magnitude reduction in power consumption w.r.t. published designs. Next, the bandpass loop filter is based on LC resonators that implement the desired bandpass characteristic at low power. Finally, the high speed requirements on the flash converter are alleviated by interleaving the quantizer sampling operation. The proposed RF BP–ΣΔ ADC operates at 2.4GHz with a 3GS/s sampling clock and a bandwidth of 60MHz almost covering the entire ISM band. The SNDR and SFDR performance integrated over the band are 40dB and 62dB respectively. The performance, although not yet sufficient to substitute a classical receiver, prove the feasibility of RF digitization at low power in standard CMOS implementations.

The paper is organized as follows: Section II discusses the ADC architecture, Section III describes the circuit details of the implementation, measurement results are provided in Section IV and Section V concludes the paper.

II. RF bandpass Sigma-Delta Architecture

A. Mirrored-image sampling

Traditionally, BP–ΣΔ ADCs are centered on integer fractions of the sampling clock below the input signal Nyquist frequency (e.g. Fs/4, Fs/5, …). However, it is important to realize that, because of the discrete-time nature of the ΣΔ loop, the noise shaping actually occurs at all aliases of the bandpass center frequency. This means that the loop filter center frequency can be positioned on for example the first alias above the Nyquist frequency (e.g. 3Fs/4, 4Fs/5, …). This technique is sometimes referred as the mirrored-image technique and Fig. 1 shows the example of a 4Fs/5 operation.

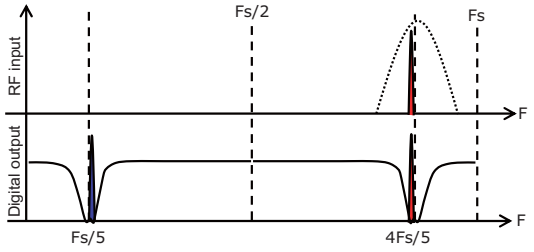

Figure 1. Mirrored-image sampling scheme with filter placed at 4Fs/5. Note that noise shaping is also observed at Fs/5.

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A clear advantage of this technique is the reduction of the sampling frequency, which in this example is four times lower than with the RF band centered on Fs/5. In our implementation, the filter center frequency of 2.4GHz is positioned at 4Fs/5 such that the clock frequency is 3GHz.

B. Filter architecture

The choice of the 6th order bandpass loop filter is based on a cascade of Gm-LC resonators as proposed in [7]. The filter architecture is shown in the top of Fig. 2 and a resonator cell in the bottom. A negative Gm (-R) is incorporated in each resonator to compensate for the low Q of on-chip inductors.

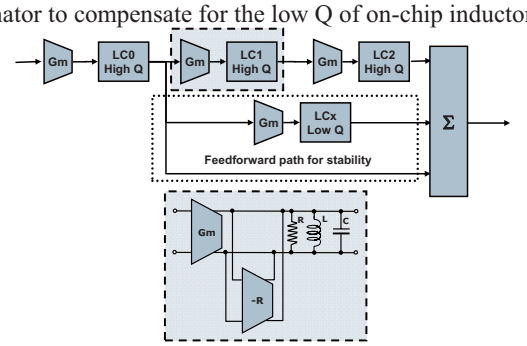

Figure 2. Bandpass loop filter architecture (top) and resonator cell (bottom).

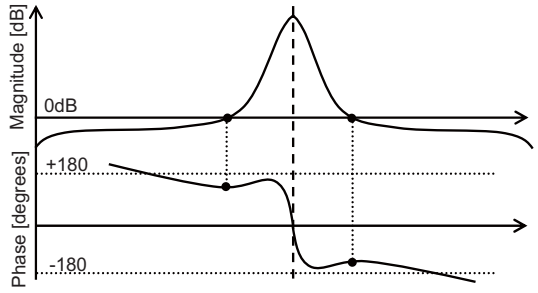

Figure 3. Frequency response of the loop filter incl. loop delay. The 0dB crossing points must experience less than 180 degrees phase shift for stability.

The filter consists of a high quality high gain path (Gm-LC1, Gm-LC2), ensuring sufficient noise shaping in the useful band, stabilized by a feedforward path with a lower Q (1+Gm-LCx). The stability of the loop can be evaluated on the filter frequency response including loop delay in the S-domain. As shown in Fig. 3, the phase rotation of the filter needs to be lower than +/-180 degrees at the 0dB crossing points. Gm-LC0 is centered at 2.4GHz but Gm-LC1 and Gm-LC2 are detuned to spread the NTF zeros.

C. Complete BP–ΣΔ ADC architecture

The architecture of the complete ADC is shown in Fig. 4. The feedback signal is injected as a current in the first resonator tank such that the first Gm stage lies outside the ΣΔ loop. A direct feedback path F adds the quantized signal directly to the quantizer input compensating for loop delay.

The single-bit quantizer is made of two interleaved comparators clocked at half the speed. This reduces the power consumption in the comparator. Both outputs are then multiplexed to produce the output bit stream.

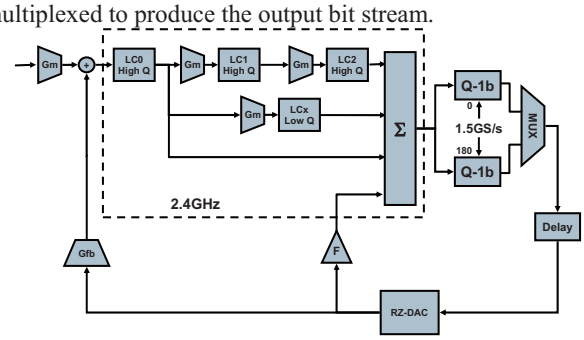

Figure 4. Complete RF BP–ΣΔ ADC architecture.

The feedback path operates at relatively high speed (3GS/s). Therefore, the delay in the feedback path becomes extremely critical. The ΣΔ loop is stable if the feedback phase rotation is a multiple of (2n+1) π at the center frequency of the loop filter (2.4GHz). In order to allow sufficient time for the quantizer and the multiplexing operations, the phase rotation in the feedback path is set to 3π, which corresponds to a feedback delay of 1.875Ts=625ps. Since the ΣΔ stability is very sensitive to this delay value, it is necessary to provide external calibration of the delay.

III. CIRCUIT DESIGN

A. LC resonator design

Each resonator (Fig. 5) is programmable by means of digitally tunable Gm-cells, negative-Gm cells and MOS-capacitors.

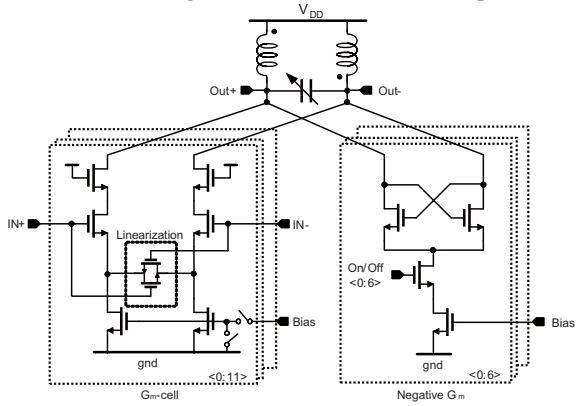

Figure 5. Circuit schematic of the fully-programmable resonator cell.

The Gm-cell cell consists of a cascode amplifier – for improved isolation – with active degeneration for linearization. Every transconductor consists of digitally selectable unit cells in parallel. Both the current through each cell (via the Bias input) and the number of active cells can be

changed individually. The Gm unit drives an inductor load, resonating with a capacitor bank. The inductor is a 4.6 nH differential 4-turn inductor in top metal. The capacitor bank consists of a binary weighted array of MOS varactors, digitally selectable in a binary weighted fashion. For improved isolation as well as to bias the following stage, each resonator output is buffered by a source follower. The negative Gm-cell consists of an array of cross-coupled pair. The gain of each resonator can be tuned from 0 to 20dB, their center frequency can be varied from 2GHz to 3GHz and the quality factor can be tuned up to 40. An array of parallel resistors is added to the low-Q resonator Gm-LCx allowing to reduce the Q down to 3.

B. Quantizer design

The high-speed single-bit quantizer is implemented with two interleaved comparators running at Fs/2 (1.5GS/s) (Fig. 6).

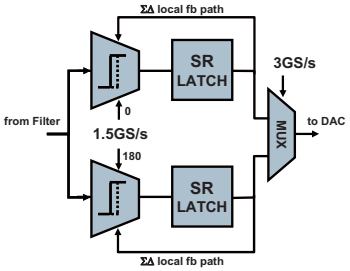

Figure 6. Interleaved single-bit quantizers with embedded local feedback.

The comparator's outputs are stored in SR latches that are multiplexed at 3GS/s rate. The direct feedback compensating for excess loop delay must be applied with a delay of approximately 2 clock phases. This extra feedback path has been incorporated into the quantizer as follows: the comparator threshold is shifted, controlled by the previous comparator decision. Because of the interleaving, this implements a 2 clock cycle delayed input signal which is the inverse of the threshold shift. By controlling the amount of shift, the DAC function is obtained. This technique reduces complexity in the analog part of the ΣΔ (no DAC, and input to the adder), while only marginally increasing the quantizer complexity and power consumption.

The comparator is based on the StrongARM latch (Fig. 7). To reduce power consumption, the size of the comparator has been aggressively reduced and the resulting increase of mismatch is corrected by calibration [2]. This calibration is implemented by variable capacitors on the internal nodes of the comparator as indicated in Fig. 7 [2]. This threshold calibration feature is also exploited to implement the local feedback path, which is as explained before equivalent to a DAC operation. The only additional circuitry required are AND gates controlling the variable capacitor bank.

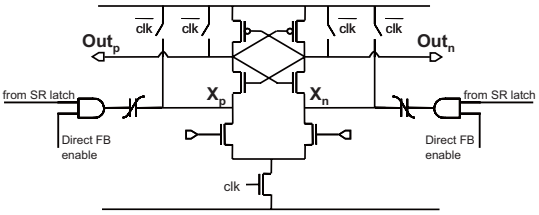

Figure 7. StrongARM latch based comparator.

At runtime the comparator is first calibrated for zero offset at its input and next, the appropriate amount of direct feedback is enabled ('Direct FB enable' in Fig. 7). The comparators drive a cross-coupled NAND SR latch, which in turn drives a MUX consisting of tri-state inverters.

The interleaved implementation runs at 3GS/s with low power due to the relaxed speed requirements. The comparators have about 300ps to decide, which is easily achievable. Doubling their speed would require disproportionally more power.

C. RZ-DAC

The RZ-DAC (Fig. 8) consists of a switched current source. The RZ signals are created by gating the data signal with the 3GS/s clock. This ensures low jitter edges being provided to the DAC, where jitter is of utmost importance. The clock signal is also used as a dump signal in order to ensure that the DAC current source remains continuously in saturation.

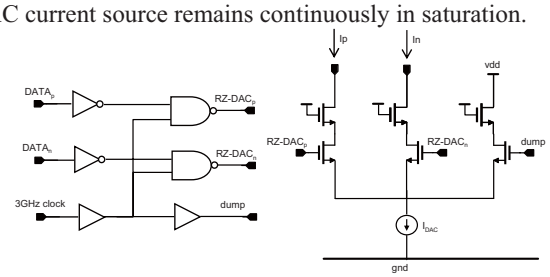

Figure 8. RZ DAC and its logic control circuit.

IV. MEASUREMENT RESULTS

The ΣΔ has been processed on a standard 1P9M 90nm CMOS technology and the chip microphotograph is given in Fig. 9.

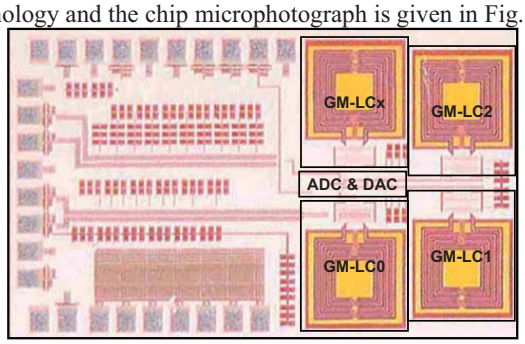

Figure 9. Chip microphotograph

Fig. 10 shows the spectrum plot of a 2.41GHz RF signal applied to the input of the ΣΔ clocking at 3GS/s. Note that the spectrum is plotted around the image frequency at 600MHz (3GHz–2.4GHz).

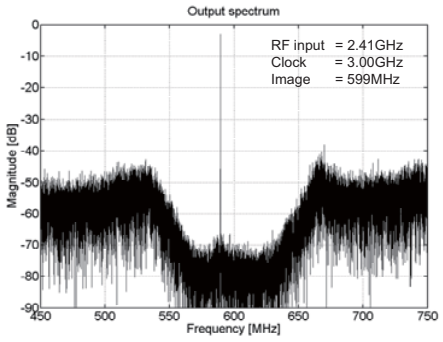

Figure 10. Spectrum of the output digital bit stream around the image (Fs/5).

This spectrum was obtained by capturing the digital bit stream on a 40GS/s scope and plotting the FFT around the image at Fs/5. Fig. 11 shows the result for two tones being applied to the converter. The measured IIP3 is -9dBm. The SNDR and SFDR are plotted as a function of the input power in Fig 12.

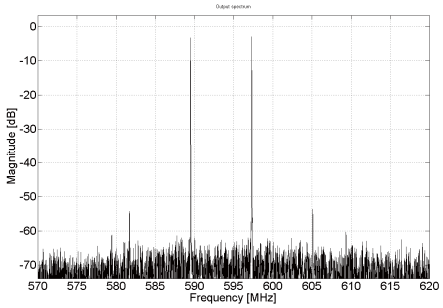

Figure 11. Output spectrum for two tones being applied to the input.

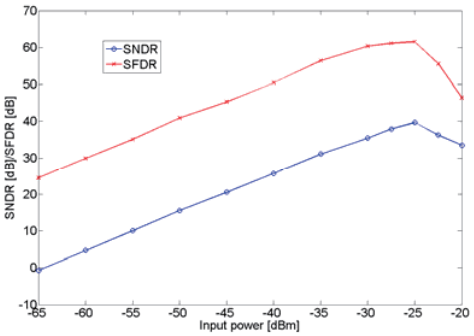

Figure 12. SNDR and SFDR as a function of input power. Note that input power is given in dBm. -25dBm = -6.4dB$_{FS}$

The maximum SNDR integrated over 60MHz is 40dB and is reached with a -25dBm input level (-6.4dB$_{FS}$). The SFDR is 62dB at maximum SNDR. The maximum SFDR is the limit in resolution that can be obtained when narrowing the channels in the digital front-end. The SNDR obtained is 12dB lower than predicted by circuit simulations. There are indications that the higher in-band noise would be due to signal dependent clock jitter being generated on-chip by the clock network.
The power consumption from 1V supply is 40mW including clock buffers. This design yields the highest FOM ($2^{ENOB}.2.B_w/P_{DC}$), while implemented in a CMOS process.

TABLE I. TABLE OF PERFORMANCE AND COMPARISON WITH SOA

Parameters	[3]	[4]	[5]	This work
Center frequency	2 GHz	950 MHz	1 GHz	2.4 GHz
Clock frequency	40 GHz	3.8 GHz	4 GHz	3 GHz
SNR (Bandwidth)	52 dB (120 MHz)	59 dB (1 MHz)	40 dB (20 MHz)	40 dB (60 MHz)
Power consumption	1600 mW	75 mW	450 mW	40 mW
Technology	0.13µm SiGe BiCMOS	0.25µm SiGe BiCMOS	0.5µm SiGe HBT	90nm CMOS
Active area	~1 mm²	1.08 mm²	1.36 mm²	0.8 mm²
FOM [GHz/W]	49	19.4	7	245

V. CONCLUSION

This IC demonstrates the feasibility of RF digitization at low-power in standard CMOS implementations. The performance obtained is not sufficient to replace a receiver chain but paves the way towards RF sampling. Indeed, several techniques could be employed to further improve the resolution, such as the use of multi-bit quantizers and cascaded ΣΔ loops.

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