A Single-Channel, 1.25-GS/s, 6-bit, 6.08-mW Asynchronous Successive-Approximation ADC With Improved Feedback Delay in 40-nm CMOS

Tao Jiang, *Student Member, IEEE*, Wing Liu, Freeman Y. Zhong, Charlie Zhong, Kangmin Hu, *Member, IEEE*, and Patrick Yin Chiang, *Member, IEEE*

***Abstract*—A single-channel, asynchronous successive-approximation (SA) ADC with improved feedback delay is fabricated in 40 nm CMOS. Compared with a conventional SAR structure that employs a single quantizer controlled by a digital feedback logic loop, the proposed SAR-ADC employs multiple quantizers for each conversion bit, clocked by an asynchronous ripple clock that is generated after each quantization. Hence, the sampling rate of the 6-bit ADC is limited only by the six delays of the Capacitive-DAC settling and each comparator's quantization delay, as the digital logic delay is eliminated. Measurement results of the 40 nm-CMOS SAR-ADC achieves a peak SNDR of 32.9 dB and 30.5 dB, at 1 GS/s and 1.25 GS/s, consuming 5.28 mW and 6.08 mW, leading to a FoM of 148 fJ/conv-step and 178 fJ/conv-step, respectively, in a core area less than 170 um by 85 um.**

***Index Terms*—Analog-to-digital converter (ADC), asynchronous logic, binary successive-approximation (SA) algorithm, single-channel ADC.**

I. Introduction

MULTIGIGAHERTZ, low-to-medium-resolution analog-to-digital converters (ADCs) are critical for a growing number of high-speed applications, including ultra-wideband (UWB) radios [1]–[3], mm-wave radios, serial link transceivers [4], [5], next-generation Ethernet [6], and digital oscilloscopes [7], [8]. Flash ADCs are commonly employed because they exhibit a fast conversion rate for a single quantization bit. However, the power and effective resolution suffer as the sampling rate increases [1]–[3], [6]. More recently, time-interleaved ADCs (TI-ADCs) have seen growing popularity due to their low power and high-sample rate. As each subchannel of a TI-ADC critically limits the total power consumption, the successive-approximation (SA) architecture has been widely used due to its improved power efficiency when compared with other approaches. Combined with time-interleaving, the SA architecture has recently shown sample rates up to 30–50 GS/s [9]–[11], therefore surpassing its flash counterpart, whose power consumption and area increases exponentially with the resolution.

In order to increase the conversion rate of the conventional SAR ADC, several techniques have been proposed that improve upon the traditional architecture. An asynchronous SA algorithm was first proposed in [12], where the triggering of the internal comparisons from MSB to LSB occurs in a ripple-like fashion, such that the quantization time allocated to each bit is no longer limited by the slowest conversion bit but the average quantization time, therefore improving throughput over a synchronous architecture. This algorithm was further improved by addressing the metastability issues in the comparator by post-processed calibration, thereby accounting for the slowest conversion bit time [13]. Recently, in order to obtain the benefits of the fast conversion speed of flash with the low power consumption of a SAR, a 2-b/step flash-SAR structure was proposed [14]. Compared with a normal SAR architecture, this structure theoretically improves conversion time by 50%, at the cost of consuming 50% more power. To achieve 6-bit resolution, only three steps were needed, with three quantizations per step. A nonbinary series network was designed in [12] to improve the capacitive digital-to-analog converter (DAC) settling time, resulting in two improvements: a nonbinary radix relaxed the DAC settling accuracy, thereby significantly saving the *RC* delay settling time, while a series network reduced the total DAC capacitance size, minimizing the absolute *RC* delay itself. A digital calibration scheme based on the least-mean-square (LMS) algorithm was used to overcome systematic errors due to capacitance mismatches and uncertainties in capacitive DACs [12]. Finally, several methods have been proposed to reduce the delay of the digital SAR logic, such as employing flip-flop bypass SAR logic [14] and a semiclosed digital loop [13]. The former technique removes a D-flip-flop between the comparator outputs and the capacitive network, but still requires a mux to select different control bits depending on the state machine. The latter technique enables some overlapping between the comparison time and the SA logic processing time, so that the total conversion time can be reduced.

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T. Jiang and P. Y. Chiang are with the School of Electrical Engineering and Computer Science, Oregon State University, Corvallis, OR 97331 USA (e-mail: pchiang@eecs.oregonstate.edu).

W. Liu was with LSI Corporation, Milpitas, CA 95035 USA. He is now with Altera Corporation, San Jose, CA 95134 USA.

F. Y. Zhong is with LSI Corporation, Milpitas, CA 95035 USA.

C. Zhong was with LSI Corporation, Milpitas, CA 95035 USA. He is now with Nvidia Corporation, Santa Clara, CA 95050 USA.

K. Hu was with the School of Electrical Engineering and Computer Science, Oregon State University, Corvallis, OR 97331 USA. He is now with Broadcom Corporation, Irvine, CA 92617 USA.

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The motivation for this work is to explore an alternative solution for improving the sub-ADC for time-interleaved multigigahertz ADCs. For time-interleaved structures, the number of channels and the operating speed of each sub-ADC need to be determined judiciously. A larger number of subchannels requires larger area and higher complexity for maintaining multiphase timing accuracy, especially in the first-stage time-interleaved T/H switches [7], [8]. A smaller number of subchannels relaxes the clocking complexity of these distributed T/H stages, but adds significant power and complexity to the higher performance sub-ADCs.

In a previously reported 1.2-W, 24-GS/s, 6-bit, 16-channel TI-ADC [9], a single 1.5-GS/s sub-ADC consumes 25 mW. Hence, all 16 sub-ADCs consume only 400 mW, meaning the T/H and clock generation circuits consume more than twice the power of the sub-ADCs. Each of these sub-ADCs must be able to handle a sampling rate of 1.5 GS/s, which leads to three possible options. First, a conventional dlash ADC can be employed [4], [5], [16], but is not preferred due to poor power efficiency and large area compared with a SAR structure, when the target resolution is high [22]. Second, each ADC can be further time-interleaved with several even more power-efficient SAR-ADCs running at even lower frequency [9]–[11]. In [9], each sub-ADC was further decomposed into ten SAR-ADCs running at 150 MS/s. Unfortunately, additional clock generation and channel calibration is required, as well as inter-stage voltage buffers, increasing power and system complexity. The third possibility is to design a single-channel, 6-b SAR-ADC that can run up to 1.5 GS/s. This is challenging even with continued CMOS scaling, as the state-of-the-art fastest single-channel ADC known to the authors can achieve 5 b at 800 MS/s [15], using a binary-search technique proposed in [23]. Although this technique improves the feedback delay without consuming higher power consumption, it employs $2^N - 1$ comparators (where N is the resolution), increasing the area and difficulty for floor planning and wire routing. Therefore, a fundamental architectural innovation needs to be developed in order to improve the sampling rate of conventional delay-limited SAR-ADCs.

This paper describes a chip prototype of a single-channel, 6-b 1.25-GS/s asynchronous SAR-ADC with improved feedback delay that is area-efficient, thereby enabling a large number of subchannels to be integrated into a TI-ADC. Section II briefly reviews the architecture of a conventional SAR-ADC and then introduces this proposed work. The circuit implementations of each individual block are provided in Section III, while measurement results are shown in Section IV. The final conclusion will be discussed in Section V.

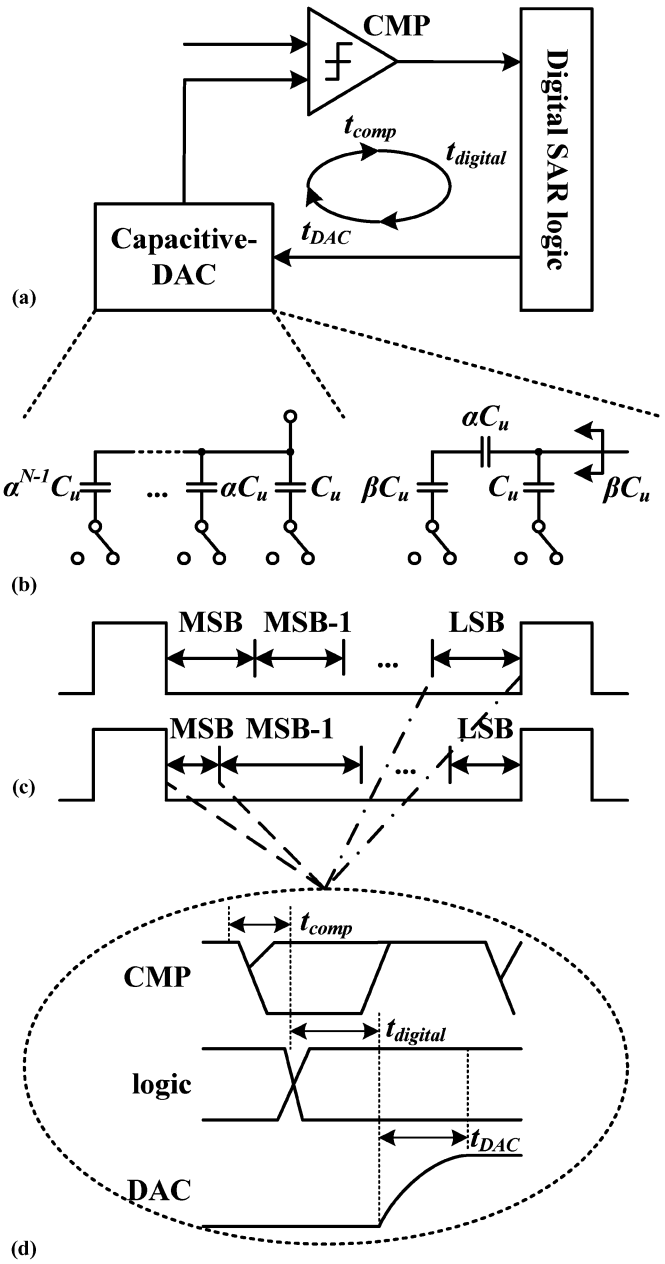


Fig. 1. (a) Conventional SAR-ADC architecture. (b) Parallel (left) and serial (right) connection of the capacitive DAC, with binary ($\alpha = 2$) and nonbinary ($\alpha < 2$) radix. (c) Synchronous and asynchronous algorithm. (d) Critical path for a one-bit conversion of a conventional SAR-ADC architecture.

II. SAR-ADC Architecture

A. Conventional SAR-ADC Approach

The conventional architecture of high-speed SAR ADCs is illustrated in Fig. 1, which consists of a single comparator to quantize the analog signal bit by bit, a capacitive network (DAC) to generate the successively approximated analog signal, and digital logic that both decodes the corresponding comparator outputs and controls the switching of the capacitive DAC. The comparator operating at this high frequency is typically a dynamic latch-based structure with either foreground [17] or background [14] calibration implemented to minimize offset. Several architectural possibilities exist for the capacitive DAC: binary [13], [18] and nonbinary [12] by radix, or parallel [18] and serial [12], [13] by connection style. While the conversion can be performed in a synchronous or asynchronous fashion, the critical path in a single bit of conversion always consists of the time required for the comparator to resolve the current bit $t_{\rm comp}$, the digital delay through the SA algorithm digital logic $t_{\rm digital}$, and

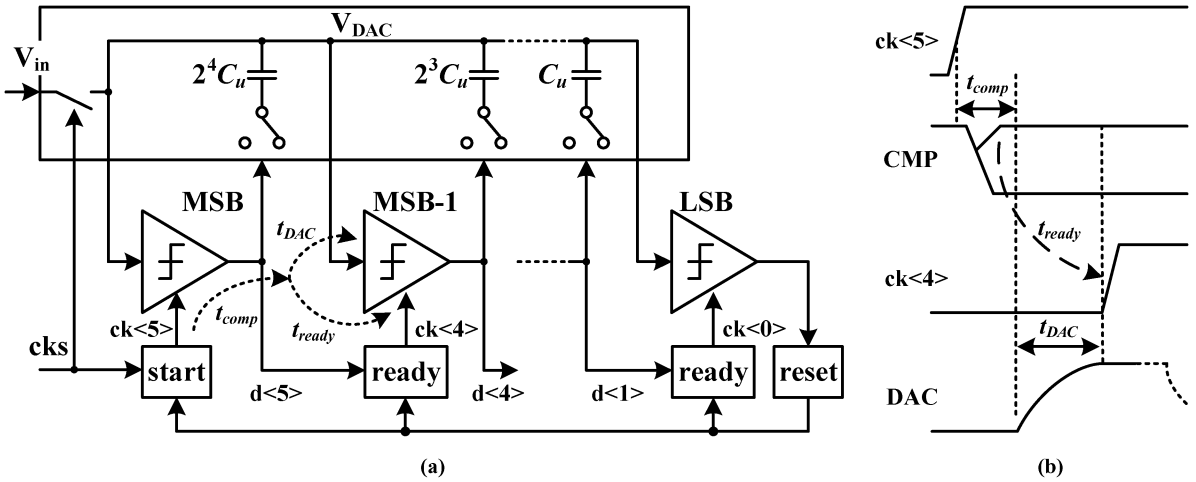


Fig. 2. (a) Proposed architecture of the asynchronous SAR-ADC with improved feedback delay. (b) Critical path for a one-bit conversion of the proposed SAR-ADC architecture.

the settling time for performing the charge sharing within the capacitive DAC $t_{\rm DAC}$:

$$T_{\rm critical} = t_{\rm comp} + t_{\rm digital} + t_{\rm DAC}. \tag{1}$$

$t_{\rm comp}$ is expressed as follows for a typical StrongARM-type dynamic comparator [13]:

$$t_{\rm comp} = \underbrace{\frac{2C_L V_{\rm thp}}{I_o}}_{t_o} + \underbrace{\frac{C_L}{g_{m,\rm eff}} \ln\left(\frac{1}{V_{\rm thp}}\sqrt{\frac{I_o}{2\beta}}\frac{\Delta V_{\rm out}}{\Delta V_{\rm IN}}\right)}_{t_{\rm latch}} \tag{2}$$

where $\Delta V_{\rm IN}$ represents the input difference and $\Delta V_{\rm out}$ represents the voltage swing at the proceeding output, C_L is the loading capacitance at the outputs of the comparator, I_o is the operating current determined by the tail transistor during the discharge phase at the beginning of the regeneration, $g_{m,\rm eff}$ is the effective transconductance of the input device, and the threshold voltage $V_{\rm thp}$ and β are technology-related constants. If C_L is determined by the following stage, and the input capacitance of the transistors is not too large, the straightforward method to reduce comparator delay is to increase the operating current I_o. Unfortunately, this will also cause the direct-path current to increase and impact the total energy efficiency. Therefore, there exists a lower limit for the value of $t_{\rm comp}$ for a given power budget. Even if the power budget can be ignored, the value of $t_{\rm comp}$ is still bounded by the intrinsic parasitic capacitance contained in C_L.

The settling time of the capacitive DAC is also similarly constrained, once the radix and the capacitor DAC connection style are determined. This is derived as below, assuming $R_{\rm eff}$ and $C_{\rm eff}$ are the effective on-resistance of the MOS switches and capacitance of the capacitive network. For the minimum amount of accuracy $V_{\rm LSB}$ required, sufficient settling time must be allocated such that the residual error is small:

$$t_{\rm DAC} = R_{\rm eff} C_{\rm eff} \ln \frac{|V_{\rm step}|}{V_{\rm LSB}} \tag{3}$$

where $V_{\rm step}$ is the voltage step size required for the current stage to settle, and $V_{\rm LSB}$ is the LSB voltage determined from the full-scale input swing, the required resolution, and the radix. With improved technology, the unit capacitance can be made extremely small (<1 fF in [26]). However, this trend of decreased capacitor size is constrained by thermal noise, as well as layout complexity and uncertainty in parasitic capacitances.

Finally, the digital SAR logic is employed to process the results of the current quantized bit, and then controls the switches within the capacitive DAC based upon its state machine, thereby generating the corresponding analog signal for the comparator to resolve its next bit. This digital logic requires that the switches that have been previously set must maintain their state until the end of the entire conversion period; otherwise, the final generated digital output will be incorrect. Depending on the internal digital structure, this digital logic delay can be quite large. For example, the work in [14] shows that this logic gate delay consumes up to 75% of the cycle time, thereby limiting any possibility for future speed improvements required for multigigahertz sampling rates.

B. Proposed Work: Asynchronous SAR-ADC With Improved Feedback Delay

In the conventional structure, the aforementioned three SAR operations occur successively in time. Because the comparator must wait for the capacitive DAC to be fully settled before it can start the comparison, $t_{\rm comp}$ and $t_{\rm DAC}$ cannot occur simultaneously. However, the digital logic processing does not necessarily require separate time durations other than $t_{\rm comp}$ and $t_{\rm DAC}$. In order to explore the timing benefits of performing the digital SAR algorithm at the same time while the C-DAC is settling, an asynchronous SAR ADC with improved feedback delay is proposed, as shown in Fig. 2.

The proposed SAR-ADC architecture features two new techniques. Unlike a conventional architecture that uses a single comparator followed by digital logic to determine, store, and transfer the comparison results, the new architecture uses N

comparators for N-bit conversion, storing each comparison result into the digital output of each comparator. These digital outputs are utilized simultaneously in two parallel paths: one is directly to the capacitive DAC, such that the DAC can respond to the results promptly and generate the successively approximated analog signal quickly without being delayed by any digital logic; the other is to a digital clock generator that detects the completion of the current quantization and then generates a "ready" signal to clock the next quantization. Both paths occur simultaneously, such that the critical path is reduced to

$$T_{\text{critical}} = t_{\text{comp}} + \max[t_{\text{ready}}, t_{\text{DAC}}] = t_{\text{comp}} + t_{\text{ready}}. \quad (4)$$

In order to improve the conversion as much as possible, any unnecessary buffer delays are to be avoided. Therefore, all digital logic gates were customized using logical effort [25] to optimize the gate delay and power consumption. Note that the time delay required for generating the ready signal must be made adequately longer than the settling time of the DAC. Compared with (1), the critical path in the proposed design is significantly improved over a conventional SAR-ADC.

Second, the proposed structure makes it natural to employ asynchronous processing [12], [13], taking advantage of the average quantization delay as opposed to the worst-case delay, as there will only be one quantization when the input level is less than 1/2 LSB due to the binary SAR algorithm. After the completion of the front-end sample/hold, which is determined by the global periodic clock cks, the quantization of the MSB cell is initiated, followed by the proceeding quantizations from MSB-1 to LSB, triggered like dominoes from the outputs of the ready logic. The $reset$ signal, generated from the LSB cell, will then precharge all of the comparators and the capacitive DAC, preparing the entire SAR-ADC for the next conversion. One additional benefit of the proposed architecture is that the resolution of the SAR ADC can be easily digitally programmed by disabling the last LSB cell, using the $ready$ signal of the LSB-1 cell as the $reset$ signal. This programmability may be useful for applications where higher sampling rate is preferred over higher resolution.

Signal voltages for a typical conversion period of the 6-b SAR ADC are simulated and shown in Fig. 3. After the falling edge of the cks signal, the clocks that trigger the comparison from MSB to LSB are generated sequentially. These clocks will maintain their logic high state until the $reset$ signal is generated to pull them down to a logic low value. The final $reset$ signal will be disabled at the beginning of each period so as not to impact normal operation.

Besides the features previously discussed, there are some other important considerations. First, each of the six comparators starts its own quantization triggered by the preceding $ready$ signal, but all quantizers are precharged and reset only when the LSB comparison is completed. During every conversion period, each of the six comparators only makes one quantization, and afterwards they each hold the comparison results for the rest of the period to ensure that the DAC performs correctly. In comparison, a conventional 6-b SAR ADC consists of only one comparator, but that comparator performs quantization six times. Therefore, the energy consumption in the above two cases is comparable, as the static energy consumption for a dynamic comparator is negligible at this sample rate. Second, the comparison results of each comparator will be passed through an R-S latch which is not within the critical path, with all six outputs retimed as the final digital bits.

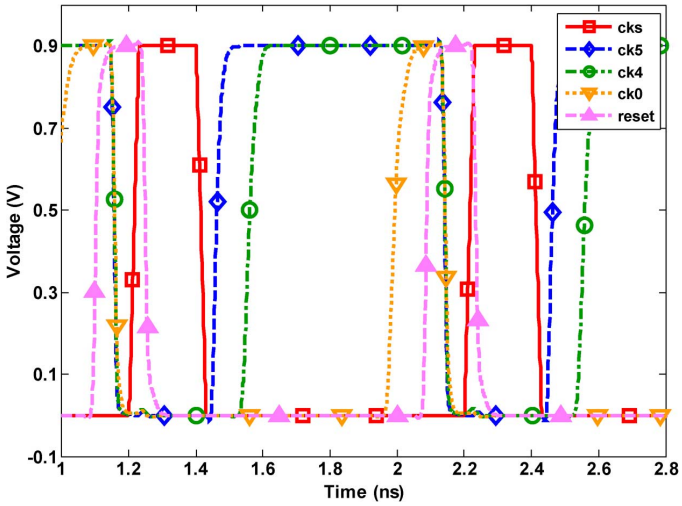


Fig. 3. Simulated waveforms for one single conversion period of the proposed SAR ADC.

III. Circuit Implementation

A. Capacitive DAC and Bootstrapped Switch

A conventional binary parallel-connected capacitive DAC (Fig. 4) [18] is employed, except with one minor change—the capacitor directly connected to ground is made $17C_u$ rather than C_u. Considering the parasitic capacitance ΔC contributed by the six paralleled comparators is considerable, the real reference voltage should be adjusted as follows:

$$V_{\text{ref}} = 1.5 \times V_{\text{FS}} \times (1 + \Delta C/48C_u). \quad (5)$$

In this way, the reference voltage is deliberately set to be over 750 mV, while the full-scale input voltage is 500 mV as defined by the system specifications. The bottom plates of the binary weighted capacitors are connected to ground through nMOS switches and to the reference voltage through pMOS switches, such that parasitic MOS switch capacitances do not affect the final accuracy of the DAC settling. Each pair of the MOS switches is gated by the same control signal which is either the positive or negative output of a corresponding comparator, so that the connection is similar to an inverter with the reference voltage as its supply. The reference voltage is preferred to be made large in order to improve the switching speed of the PMOS. To reduce design complexity, all the switches were designed to be the same size, even though the binary-weighted capacitors they connected varied significantly in size. For an improved future design, power consumption can be further reduced if both the switches and the corresponding comparators are sized accordingly based on the different capacitor values. One drawback of the DAC used in the design, however, is that only one

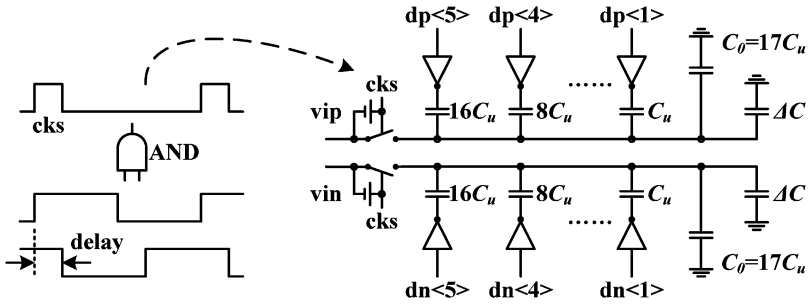


Fig. 4. Schematic of the capacitive DAC and generation of the sampling clock.

of the positive and negative outputs of the DAC is increased by the ratio of the reference voltage, making the overall differential output change up or down. Hence, while the differential voltage is generated correctly, the common-mode voltage may actually drift. This will cause the comparator offset to vary for different input common-mode values, leading to uncompensated offset for particular input voltage levels.

Given the limited time to perform data conversion when the frequency is high, the time allocated for signal sampling and conversion has to be compromised. Depending on the number of bits needed to be resolved, the on-resistance of the T/H switch R, and the loading capacitance C, the required time taken for adequate sampling can be estimated. Unfortunately, due to process variations the exact values of RC delay cannot be known, so that it is necessary to provide some calibration of the clock pulse externally. This optimized pulsewidth can be selected at startup, when the best SNDR performance is evaluated and then statically set.

Bootstrapped switches are employed (Fig. 5) in the sampling circuit in order to achieve both smaller on-resistance and minimal signal-dependent sampling distortion. As was previously illustrated in [20], when the sampling clock cks is low, the switch M_0 is shorted to ground and the capacitor is charged to near the supply voltage. When cks is high, the large voltage difference across the capacitor will be added to the input signal and then applied to the gate of the pass switch, making the gate-source voltage of the nMOS close to that high voltage constantly. In order to reduce the on-resistance of the bootstrapped switch such that the T/H circuit can meet the hard timing requirement, a 1.2-V external supply voltage is used for charging the capacitor. This circuit is carefully designed so that no voltage difference between any two nodes of a single MOS transistor is larger than the nominal voltage of 1 V for the technology.

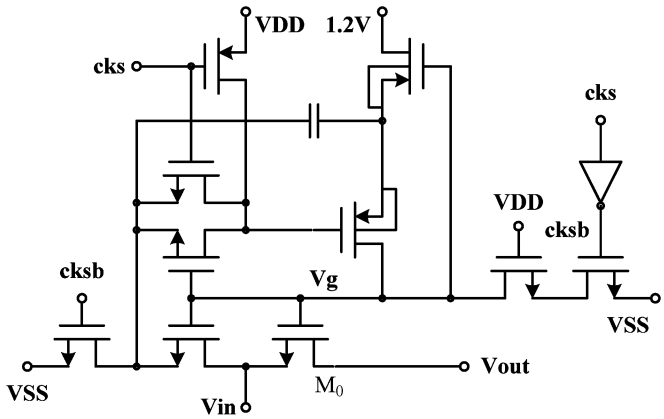


Fig. 5. Bootstrapped switch used in the capacitive DAC.

B. Comparator Design and Offset Cancellation Scheme

Six StrongARM comparators with offset cancellation [17] (Fig. 6) are used for the entire 6-b quantization. When the clock ck is reset to ground, both the positive and negative outputs are shorted to the supply voltage, shorting all the bottom plates of the capacitors in the DAC to ground. Clocked by the ready signal from the preceding conversion, each comparator evaluates the analog input signal and the corresponding differential outputs begin to split to the supply voltage and ground, respectively. Buffered by two stages of inverters, the regenerated outputs are directly sent to the switch gates of the capacitive DAC, and are kept high until reset occurs at the end of the 6-b conversion. The two inverters are sized such that they can provide sufficient drive ability while minimizing the loading seen by the regeneration nodes. To mitigate hysteresis during the quantization, all the internal nodes are also shorted to the supply voltage during the precharge phase. Unlike a conventional structure where only one comparator is used, each of the six comparators exhibit a different mismatch such that the offset is no longer a systematic error that can be subtracted during postprocessing. Therefore, foreground offset calibration for each comparator is performed at startup, where an offset cancellation circuit composed of two sets of 7-b binary current sources is used [30]. Since this 6-b ADC has a relatively large LSB (approximately 15 mV), the calibration requirements are not very strict. During calibration, the ADC is fed with the differential voltages that cause metastability to a specified comparator. The corresponding comparator digital output is monitored on the oscilloscope, and the control bits are tuned until metastability is observed. Current imbalance using a digitally controllable current mirror is used, such that the effect on the regeneration speed due to the added capacitance is minimized. In addition, pseudocommon-gate isolation reduces the effect of parasitic loading on the comparator speed. In this design, the transistors in the comparator were sized large, such that the three-sigma Monte Carlo offset was simulated to be within 50 mV. In the simulation, offsets ranging from 1 to 50 mV can be cancelled when turning ON and OFF co-responsive current sources. Although there will be some static current through the offset-cancellation circuit during the precharge

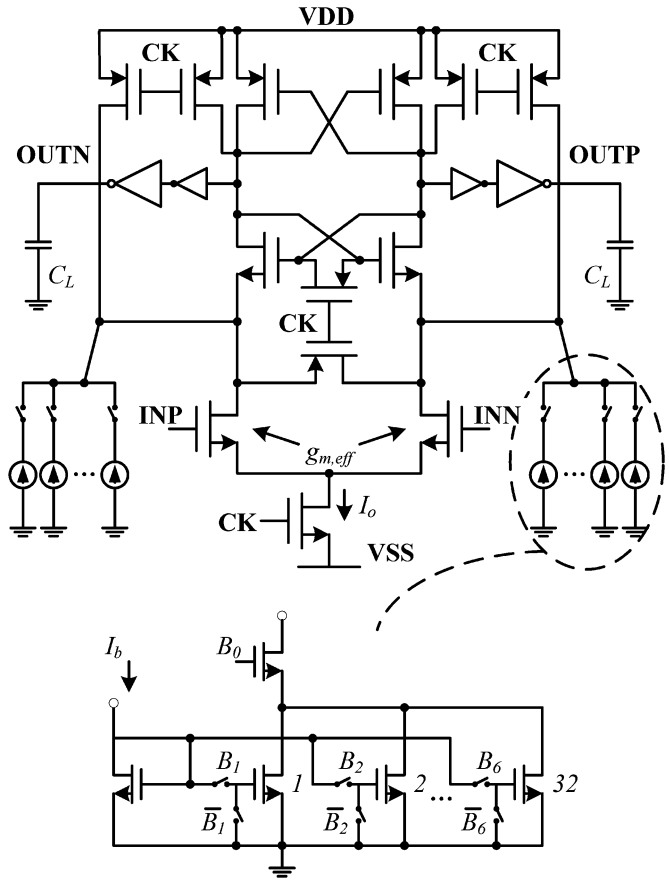
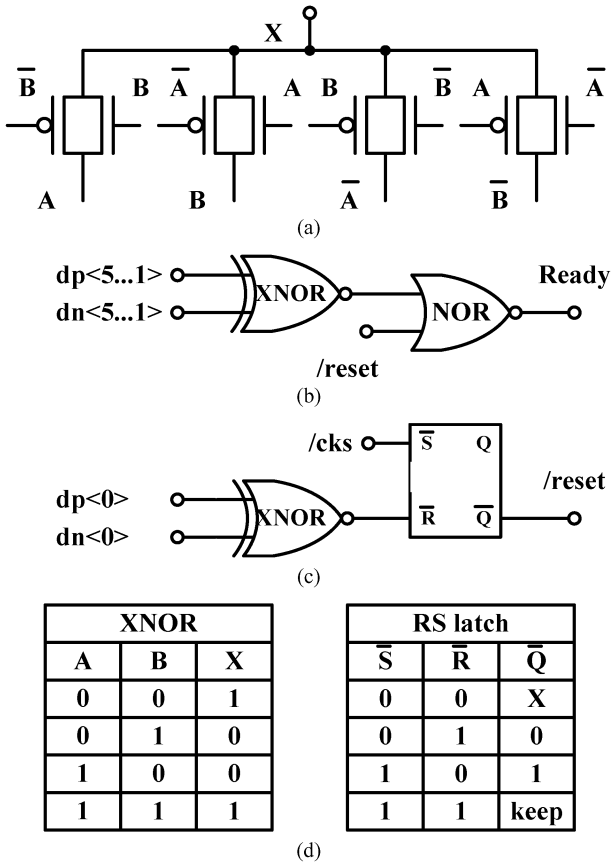


Fig. 6. Comparator design with current steering offset cancellation circuit.



XNOR		
A	B	X
0	0	1
0	1	0
1	0	0
1	1	1

RS latch		
$\overline{S}$	$\overline{R}$	$\overline{Q}$
0	0	X
0	1	0
1	0	1
1	1	keep

(d)

Fig. 7. (a) Schematic of the DPL XNOR gate. (b) The "ready" signal generation circuit. (c) The "reset" signal generation circuit. (d) Truth tables of the XNOR and RS latch.

phase since the current mirror is pulled up to supply, the injected current is minor and negligible. According to simulations, the LSB value in the binary current source is around 2 μA for cancelling the offset voltage.

C. Digital Logic Circuits

As shown in Fig. 2, each of the six comparators is followed by a digital detection circuit that determines if the current quantization is complete, followed by generation of an asynchronous clock to trigger the next quantization. The comparator in the first MSB cell is triggered by the falling edge of the sampling clock cks, while the other five comparators are triggered by the $ready$ signals from each preceding cell. The LSB cell generates a $reset$ signal that is used to reset all of the six comparators, shorting the bottom plates of the capacitors in the capacitor network to ground during the next sampling phase.

Since the comparator is precharged to the supply voltage every reset interval, its differential outputs can only exhibit "11" to "10" or "01." In a time-constrained system such as a high-speed ADC, a NAND gate for the ready logic might be preferred due to its single-stage delay. However, the NAND must be carefully designed in order to minimize the probability of making a wrong decision. For example, if the comparator is metastable, it will take a long time for its differential outputs to split, such that it is possible for both differential outputs to briefly become lower than the threshold voltage. Hence, the comparator outputs will be "00," and therefore erroneously generate the $ready$ signal, even if the comparison is far from complete. On the other hand, an XOR gate, typically formed by two cascaded stages of NAND gates, may be more robust since it will not generate a clock under the "00" situation, but suffers from relatively long delay. Therefore, a double pass-transistor logic (DPL) circuit, generated by only one stage of pass-gates, is employed to reduce the gate delay while making the correct decisions. The final ready logic is designed according to De Morgan's law and shown in Fig. 7. Instead of using an XOR and an AND gate, an XNOR and NOR gate are used to remove one-stage of delay. The output of the XNOR and the complementary/ $reset$ signal are passed through the NOR gate, generating the trigger signal for clocking the next quantization. The generation of the $/reset$ signal is slightly different. The $/reset$ signal should only be pulled up until all the $ready$ signals are reset to zero. Since all of the differential outputs of the comparators are precharged to the supply voltage, the outputs of all of the XNOR gates are reset to the supply voltage, and the $/reset$ signal must be pulled down again. Otherwise, the $ready$ signals will be always kept low. Therefore, an RS latch is used, using the supplementary sampling clock $(/cks)$ to reset the $/reset$ signal at the beginning of each period.

IV. Measurement Results

The SAR-ADC is fabricated in a 1-V, 40-nm CMOS process, with the die photograph and measurement setup shown in Fig. 8.

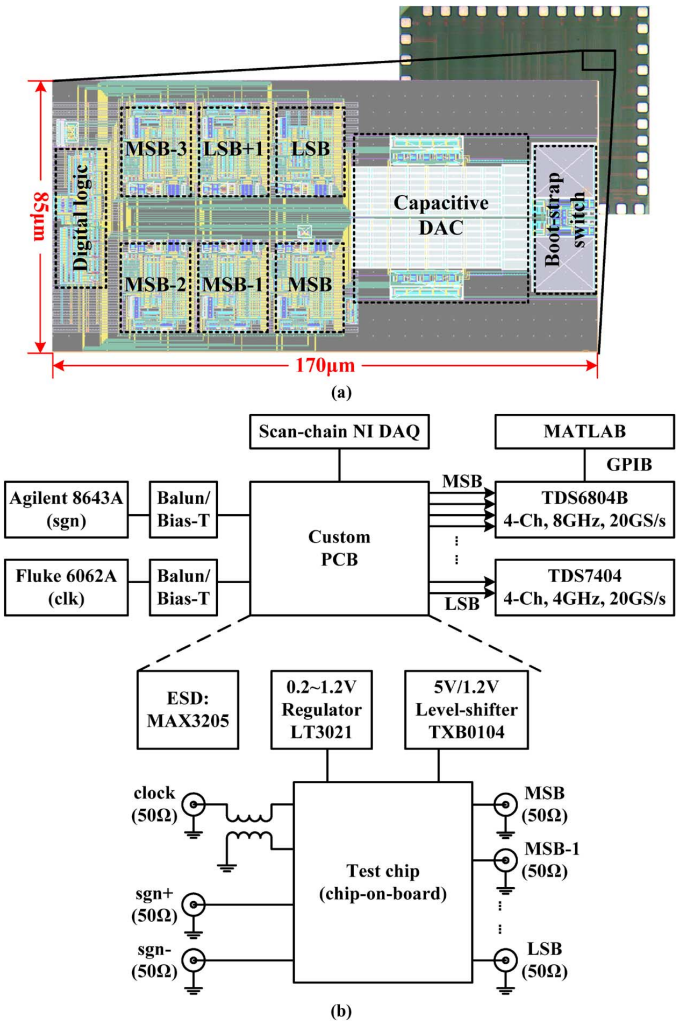


Fig. 8. (a) Chip die photograph and core circuit layout. (b) Measurement setup.

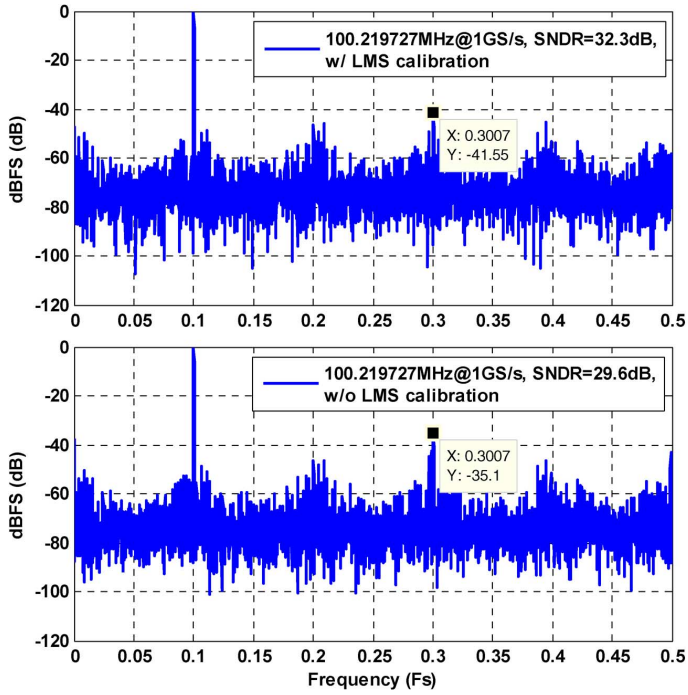


Fig. 9. ADC output spectra with and without LMS calibration.

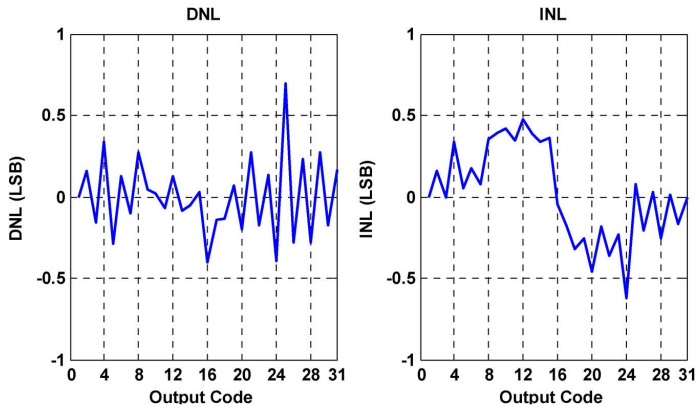


Fig. 10. DNL and INL performance after LMS calibration (5 bit).

The active area is only 170 μm $\times$ 85 μm, with a total die size of 1.8 mm $\times$ 1.5 mm. Since the chip is operating at a multigigahertz frequency, its outputs are collected using two synchronized real-time oscilloscopes through open-drain buffers, with all six outputs read into a computer and processed by MATLAB.

The measurements are performed with different supply voltages and across varying sampling rates in order to explore the chip's maximum performance. LMS offline calibration [12] is first performed by injecting a slow ramp signal into the converter, using the output code to determine the bit weights that best correspond to the known input. Because all six comparators connect to the output of the capacitive DAC, the large input gate capacitances all contribute as undesired parasitics and capacitive kickback, increasing the distortion and nonlinearity of this ADC versus a conventional structure. LMS calibration helps improve the performance considerably, as can be observed in Fig. 9, where the SNDR is improved by 2.7 dB at a sampling rate of 1 GS/s. The improvement is not as large as observed in simulation, due to the previously mentioned common-mode voltage drift that affects the comparator offset. For the same reason, the ADC cannot achieve the six b consistently through the entire input range. The DNL and INL for the first 5 b of the ADC are shown in Fig. 10, with the 6th bit acting as redundancy. ADC output spectra with near-dc and near-Nyquist input frequencies at a rate of 1 GS/s are shown in Fig. 11.

The SAR-ADC operates at 1 GS/s with a 1-V supply, consuming 1.25, 2.76, and 1.15 mW, distributed between the analog comparators, digital logic and internal clock driver, and the capacitive DAC, respectively. The ADC output spectra for different input frequencies are shown in Fig. 12, indicating a peak SNDR of 32.9 dB around dc and 27.3 dB around the Nyquist frequency, resulting in an overall FoM of 148 and 278 fJ/conversion-step. When the sampling rate is increased to 1.25 GS/s, the peak SNDR is 30.5 dB around dc and 26.8 dB around the Nyquist frequency, with a total power consumption of 6.08 mW, resulting in an overall FoM of 178 and 272 fJ/conversion-step. Another reason for the SNDR loss from dc to Nyquist is due to imperfection in the clock generator used within each conversion, resulting in increased sensitivity to supply noise and poor jitter performance. While capacitive

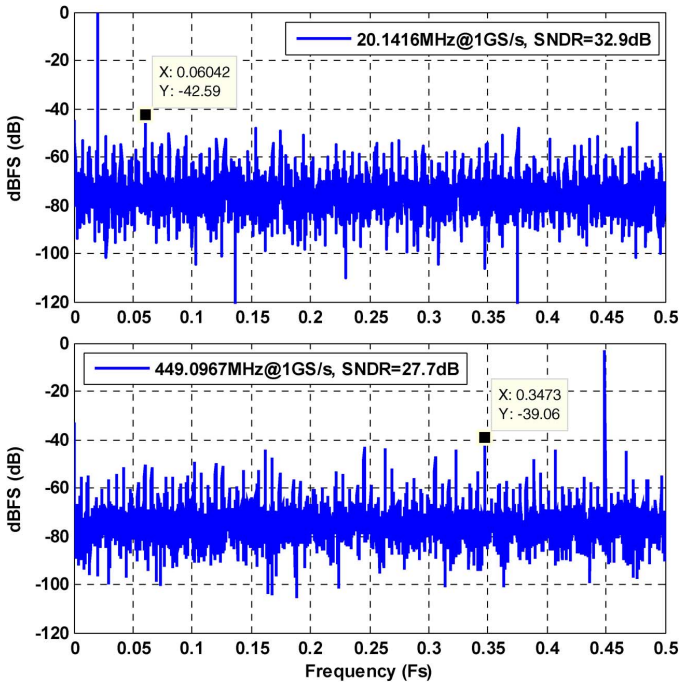


Fig. 11. ADC output spectra for different input frequencies with 1 GS/s rate.

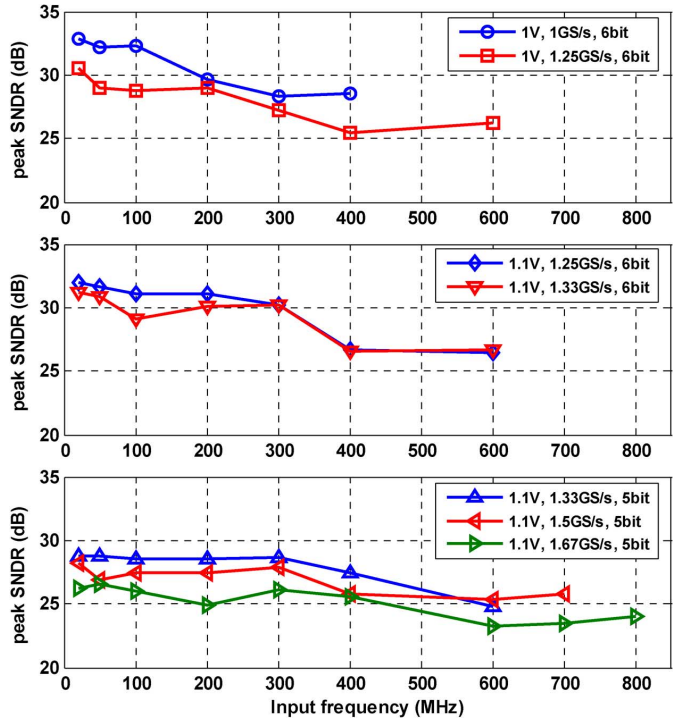


Fig. 12. Measured SNDR versus input frequency for ADC under different supplies, sampling rate, and number of bits.

parasitics contribute to the SNDR losses at low frequency, the ability to reduce to 5b conversion enables operation well above 1.5 GHz at Vdd = 1.1 V. Measurement results are summarized in Table I, along with a performance comparison versus recent >1-GS/s SAR-ADC designs.

TABLE I
COMPARISON WITH PREVIOUS WORKS

	[12]	[14]	[15]	[13]	This work			
Technology (nm)	130	130	65	65	40			
Area (mm^2)	0.12	0.09	0.018	0.11	0.014			
Resolution (bit)	6	6	5	6	5 or 6 Programmable			
Channel #	2	2	1	2	1			
Sample rate (GS/s)	0.6	1.25	0.8	1	1	1.25	1.25	1.33
Peak SNDR (dB)	34	34.9	28.2	31.5	32.9	30.5	31.8	31.3
FoM (fJ/conv)	220	-	116	210	148	178	183	188
Supply (V)	1.2	1.2	1	-	1	1	1.1	1.1
					Extra 1.2V for bootstrapped switch			
Power (mW)	5.3	32	1.97	6.7	5.28	6.08	7.26	7.52

V. CONCLUSION

A novel SAR architecture with improved feedback delay is proposed. With the comparator outputs directly fed back to the capacitive DAC, the digital FSM logic delay is eliminated, thereby greatly increasing the sample rate. Fabricated in a 40-nm CMOS process, the ADC achieves a sampling rate over 1.25 GS/s for a single channel, 56% faster than the previous fastest single-channel SAR-ADC [15].

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Tao Jiang (S'07) received the B.E. degree in electronic information and engineering and M.S.E.E. degree in electronic science and technology from Tsinghua University, Beijing, China, in 2000 and 2004, respectively. He is currently working toward the Ph.D. degree at Oregon State University, Corvallis.

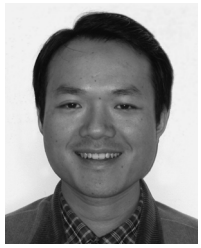
He was an Intern with LSI Corporation, Milpitas, CA, from September to December 2008, where he was involved with research on the high-speed ADC design. His current technical and research interests include low-power, high-speed ADCs and serial link design.

Wing Liu received the B.Eng. and M.S. degrees in electrical and electronic engineering from Hong Kong University of Science and Technology, Hong Kong, in 1997 and 2000, respectively.

He is currently a Design Engineer with SerDes IP Group, Altera Corporation, San Jose, CA. From 2005 to 2011, he was in HyperPhy group, LSI, where he designed high-speed circuits for black-plane channels. He was an Analog Design Engineer with Pericom Semiconductor Corporation from 2001 to 2005.

Freeman Y. Zhong received the B.S. degree from Guangzhou University, Guangzhou, China, the M.S. degree in physics from Jinan University, Nanjing, China, and the M.S. degree in electrical engineering from San Jose State University, San Jose, CA, in 1995.

From 1995 to 1998, he was with National Semiconductor Corporation, Santa Clara, CA, working on analog and mixed-signal IC designs. From 1998 to 2000, he was with NEC Corporation, working on mixed-signal IC design for storage SOC products. Since 2000, he has been a Senior Design Manager/Design Director with LSI Corporation, Milpitas, CA, where he leads the developments of Ethernet PHY and high-speed SerDes. His current research interests include high-speed SerDes and DSP-based transceivers.



Charlie Zhong received the B.S. degree from Tsinghua University, Beijing, China, the M.S. degree from the New Jersey Institute of Technology, Newark, and the Ph.D. degree from the University of California, Berkeley, all in electrical engineering.

He has been with the AT&T Bell Labs, Berkeley Concept Research Center, ST Microelectronics, Avnera, W5 networks, MediaPHY, and LSI before joining Nvidia, Santa Clara, CA, where he is currently a Senior Signal Integrity Engineer. He currently holds fifteen patents in wireless communications and high speed SerDes. His interests include high-speed SerDes and wireless networks.

Dr. Zhong was the recipient of two awards from Bell Labs in 1998 for extraordinary achievements on the CDMA program and the Management of Technology certificate from the Haas School of Business in 2003. In 2006, he received the CSG Value Recognition Award from LSI for the development of a practical tap position search algorithm for the floating tap DFE. Most recently, he received the Best Paper Award from designCon in 2011.

Kangmin Hu (S'08–M'12) received the B.S. degree in electrical engineering from Shanghai Jiao Tong University, Shanghai, China, in 2004, the M.S. degree in microelectronics from Fudan University, Shanghai, China, in 2007, and the Ph.D. degree in electrical engineering from Oregon State University, Corvallis, in 2011.

Since 2011, he has been with Broadcom Corporation, Irvine, CA, working on high-speed SerDes circuits.

Dr. Hu was a recipient of 2008 Best Poster Award from Center for Design of Analog-Digital Integrated Circuits (CDADIC). He received an Intel/Helic Student Scholarship Award at the 2011 IEEE Custom Integrated Circuits (CICC) conference. He serves as a reviewer for the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I AND II and the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION SYSTEMS.

Patrick Y. Chiang (M'05) received the B.S. degree in electrical engineering and computer sciences from the University of California, Berkeley, in 1998, and the M.S. and Ph.D. degrees in electrical engineering from Stanford University, Stanford, CA, in 2001 and 2007.

He is currently an Assistant Professor with Oregon State University, Corvallis. In 1998, he was a Design Engineer with Datapath Systems (now LSI), Milpitas, CA, where he designed a low-power, standard cell library for xDSL. In 2003, he was a Research Intern with Velio Communications (now Rambus), investigating 10-GHz clock synthesis techniques. In 2004, he was a Consultant with Telegent Systems (now Spreadtrum), where he analyzed low-phase VCOs for TV tuners. In 2006, he was a Visiting NSF Research Fellow with Tsinghua University, Beijing, China, investigating super-regenerative RF transceivers. In 2007, he was a Visiting Professor with the Institute of Computing Technology (ICT), Chinese Academy of Sciences, Beijing, China, where he designed parallel serial link transceivers. He is currently a Visiting Professor with Fudan University, Shanghai, China, developing wireless biomedical sensors. His interests are in energy-efficient circuits and systems, including near-threshold parallel computing, low-power serial link interfaces, and energy-harvested wireless sensors.

Dr. Chiang was the recipient of a 2010 Department of Energy Early CAREER award and a 2012 NSF-CAREER award. He is an associate editor of the IEEE TRANSACTIONS ON BIOMEDICAL CIRCUITS AND SYSTEMS and on the technical program committee for the IEEE Custom Integrated Circuits Conference.