High Sampling Rate 1 GS/s Current Mode pipeline ADC in 90 nm Si-CMOS Process

Shoichi Tanifuji, Kei Ando, Tuan Thanh Ta, Suguru Kameda,
Noriharu Suematsu, Tadashi Takagi and Kazuo Tsubouchi
Research Institute of Electrical Communication, Tohoku University
Katahira 2–1–1, Aoba–ku, Sendai 980–8577, Japan
E-mail : tanifuji@riec.tohoku.ac.jp

***Abstract*—We verifid possibility of high sampling rate and lower power consumption current mode ADC that focused on the most high-speed operation for millimeter-wave broadband wireless terminal such as wireless personal area network (WPAN). A 5 bit 1 giga-samples-per-second (GS/s) current mode pipeline ADC has been designed and fabricated in 90 nm Si complementary metal oxide semiconductor (CMOS) process. The fabricated ADC has no miscode and increases monotonically. In addition, differential non linearity (DNL) is less than 1.0 and integral non linearity (INL) is less than 1.25, power consumption is 52.8 mW on 1 GS/s.**

***Index Terms*—ADC, Pipeline, Current Mode, Heterogeneous, Si-CMOS**

I. Introduction

Demands for high-speed data transmission rates of wireless communication system are increasing. Novel broadband wireless services such as high speed internet access and streaming contents download require high capacity channels. For transmission of uncompressed real time high definition television (HDTV) streaming or wireless data bus, data transmission rate is needed more than 2 Gbit/s. To realize these systems, large bandwidth of spectrum is required. One method for high-speed data transmission is millimeter-wave broadband wireless systems and especially 60 GHz are promising. In these terminals, one of the most important component is analog-to-digital converter (ADC).

Fig. 1 shows sampling rate and resolution of ADC in each wireless standards. When the standards are roughly divided, there are a wide area with low-speed transmission were used mobile broadband wireless access (MBWA) on 700 MHz band, a medium range distance with medium-speed transmission were used wireless local area network (WLAN) on 5 GHz band, and a short distance with high-speed transmission were used wireless personal area network (WPAN) on 60 GHz band. Though, conversion speed and resolution demands for ADC are different according to these standards, characteristics of ADC has trade-off between conversion speed and resolution. To realize high-speed operation of ADC, the miniaturization of CMOS is needed. However, conventional voltage-mode ADCs [1]-[2] became smaller dynamic range due to low supply voltage, then signal-to-noise ratio (SNR) degraded. Moreover, it was difficult to achieve high-speed operational amplifier (OP-Amp). In these reason, the approach of without using OP-Amp are also investigated [3]-[4]. On the other hand, current-mode ADC is not affected of low supply voltage, then is is not degrade dynamic range. In addition, OP-Amp is no longer needed. Threfore, we can expect high-speed operation by current mode ADC. However, conventional current mode ADCs were low-speed operation, there were large power consumption [5]-[8]. If high-speed operation, these disadvantage of current mode ADC disappears.

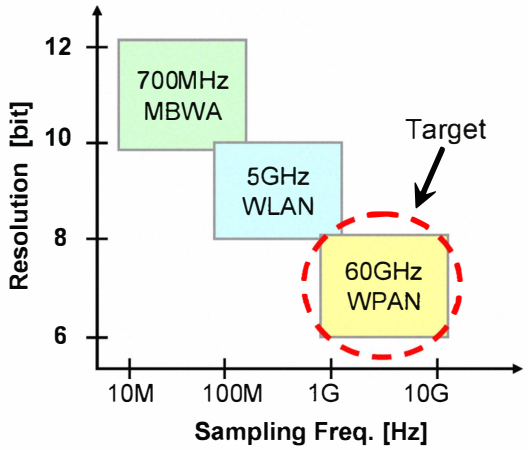

Fig. 1. Wireless communication standards and ADC spec.

In this paper, we verified possibility of high sampling rate and lower power consumption current mode ADC that focused on the most high-speed operation for WPAN terminal. In Sect. II, ADC design and fabrication are shown. In Sect. III, we evaluate designed ADC. Finally, in Sect. IV, some conclusions are drawn.

II. Design and Fabrication of ADC

Fig. 2 shows designed 5 bit current mode pipeline type ADC. Input voltage is differential, then convert to differential current by voltage-to-current converter (VIC). In current mode sample and hold (S/H) circuit, VIC output is sampled to current value. Sampled current is transferred to next pipeline stage, digital output is inputted to logic part by 1.5 bit sub-ADC. This digital output and input current amplifies to twice by MDAC, then pipeline operation is carried out are transferred to next stage. The final stage of a flash ADC is generated

978-1-4577-0963-0/11/$26.00 ©2011 IEEE

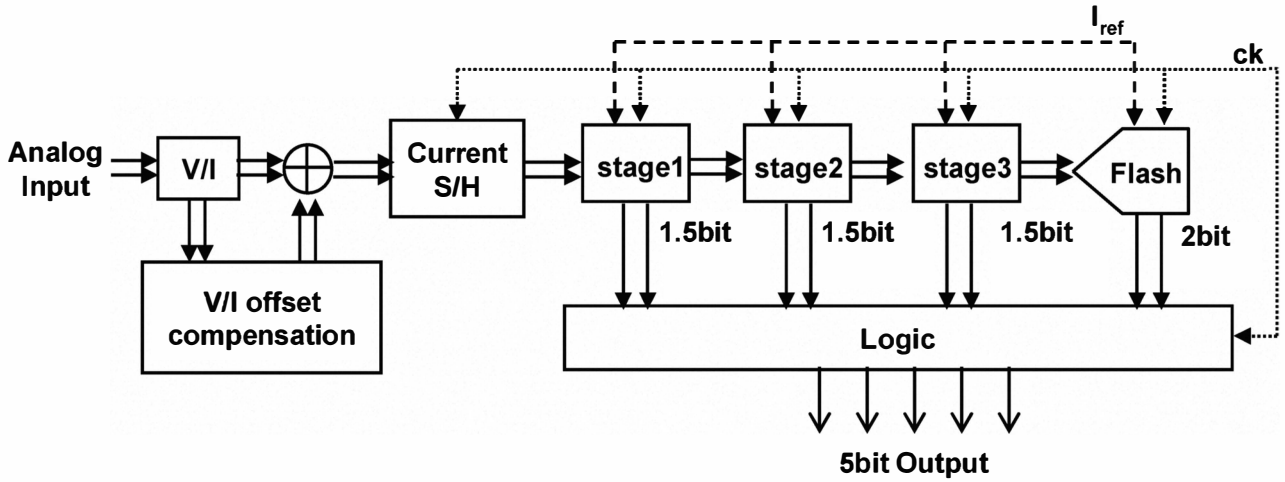

Fig. 2. Designed 5 bit 1 GS/s current mode pipeline ADC.

of 2 bit quantization, input current to logic of 2 bit digital signal. In logic part, output current of each pipeline stages and last flash ADC are delayed and added then calculate to 5 bit digital output signal. The each drain current are 500 μA, the overall power consumption is 45 mW of designed ADC.

In this section, we describes the design of element circuit to obtain high resolution of current mode ADC.

A. V/I converter

To convert input voltage to a current, voltage-to-current converter (VIC) is described. Becoming a big problem when minute silicon CMOS is used is a difference of threshold (V_{th}) of the transistor with the process variations.

VIC is particularly susceptible to the effects of process variation significantly affects the accuracy of the ADC, this is offset by reducing the impact of the VIC process variation compensation provided to the outside. Compensation for this is to generate an offset in the circuit caused by process variation, which includes an offset that is added to the VIC reverse output current.

Fig. 3 shows simulation results of input/output characteristics of VIC no offset compensation and Fig. 4 shows results with offset compensation. This simulation calculated 30 times Monte-Carlo simulation using CMOS process parameter variation supplied from the foundry. We obtained VIC characteristics improved by added compensation circuit. Moreover, -3 dB frequency characteristics of this VIC was 1.5GHz, therefore it can be converted low distortion on wide bandwidth input signal.

B. Current mode sample and hold circuit

The current mode sample and hold (S/H) circuit using the switched-current technology. Fig. 5 shows current S/H circuit using the switched-current. The cascode stages are omitted in Fig. 5. The principle of switched-current is to hold charges on gate capacity in the mirror transistor for current sampling. The effect of clock feed-through and charge injection was greatly reduced by adding dummy transistor at CMOS switch. This designed S/H circuit can be sampling very fast of 1.5 GS/s.

C. pipeline stages

Fig. 6 shows the composition of the pipeline stage. This pipeline stage of the current mode pipeline type ADC is composed by the current S/H circuit, sub-ADC, and multiplying digital to analog converter (MDAC). sub-ADC outputs 1.5 bit digital signal to logic part and MDAC according to input current (I_{in}). 1.5 bit operation of sub-ADC is intended to current compensate for comparator offset of sub-ADC. The current comparator of sub-ADC compare between the reference current (I_{ref}) and I_{in} using diode-connected transistors. MDAC amplifies I_{in} to twice, then add or subtract to I_{ref} according to the digital values received from sub-ADC , such as $2\,I_{in} \pm I_{ref}$. I_{ref} are generated by external current mirror circuit describe in next subsection.

D. Current mirror circuit

The current mirror circuit used for various parts in this current mode ADC. This current mirror circuit is used cascode current mirror to improve copy accuracy. Fig. 7 shows 3-stages cascode current mirror circuit as an example. Cascode current mirror circuit can be accurately copy the current increase of cascode stages. However, distortion of the signal would be increased by increasing cascode stages. Especially, when using low-voltage process, this distortion influence appears clearly. In this subsection, we optimize the current mirror stages of the simulation.

Fig. 8 shows precision and current copy error characteristics of frequency harmonic distortion power when cascode stages were assumed to be 2, 3 and 4. The 3^{rd} harmonic distortion power at 500 MHz input frequency were -49 dB (equivalent resolution of 7.8 bit), -47 dB (equivalent 7.5 bit), -43 dB (equivalent of 6.8 bit), respectively. The current copy errors were 1.82% (equivalent resolution of 5.8 bit), 0.31% (equivalent of 8.3 bit), 0.06% (equivalent of 10.7 bit), respectively.

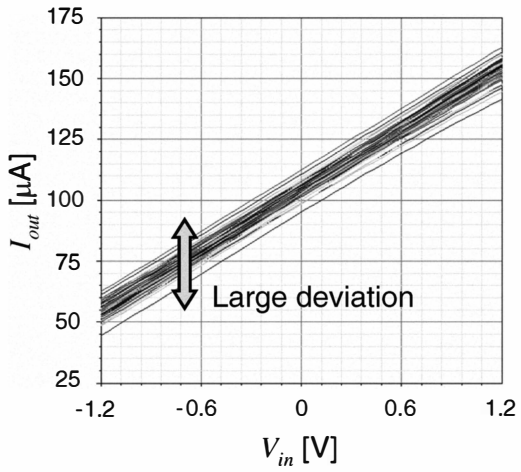

Fig. 3. Input/output characteristics of VIC no offset compensation.

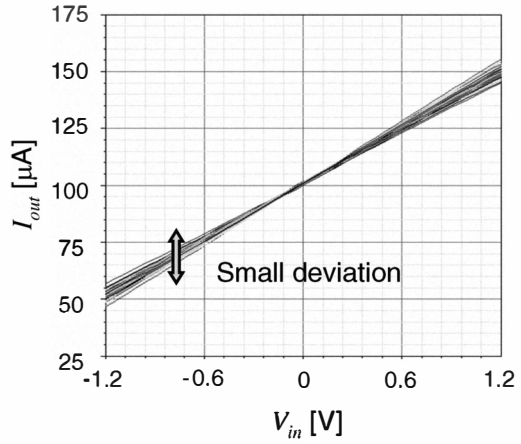

Fig. 4. Input/output characteristics of VIC with offset compensation.

Therefore, to obtain high resolution of the ADC, we adopted 3-stages cascode current mirror circuit in designing.

E. Fabrication

Fig. 9 shows circuit layout of designed ADC based on the previous subsection. Differential voltage input to the chip from left side, 5 bit digital code is output from lower side. Bias input to operate cascode transistor is applied from top of chip. Clock is generated by internal clock generator from input sine wave. Power supply voltage are applied to analog part, logic part and buffer from right side of chip. Bypass capacitors are added to power supply for power regulation. In addition, power lines of analog and logic part are isolated to suppress clock noise, also added guard ring around logic part to reduce noise from substrate.

The size of analog part of ADC is 1200 μm × 140 μm, the entire chip including pads is 1380 μm × 630 μm.

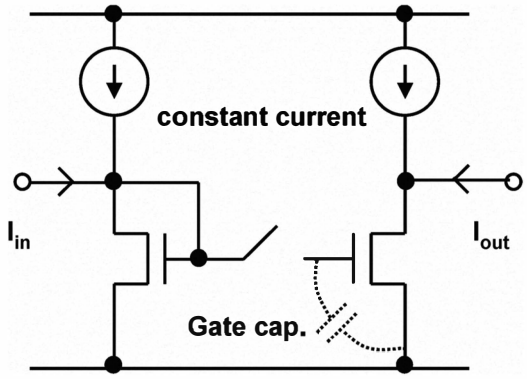

Fig. 5. Current mode sample and hold circuit.

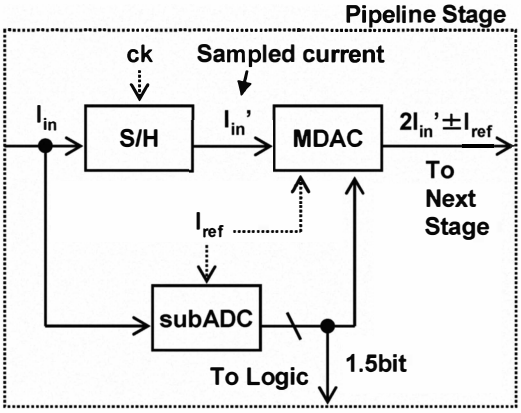

Fig. 6. pipeline stage.

III. Experimental Results and Discussion

Fig. 10 shows ADC characteristics for ramp signal input. Sampling frequencies are 500 MHz, 1 GHz and 1.3 GHz, respectively. Horizontal axis is the input voltage, vertical axis is ADC output code, Bold solid line is 500 MS/s, thin solid line is 1 GS/s, dashed line is 1.3 GS/s. We obtained almost same result on 500 MS/s 1 GS/s, normal operation of 5 bit ADC was confirmed up to 1 GS/s. When sampling frequencies over 1 GHz, miscode gradually increase, resolution less than 4 bit on 1.3 GS/s.

Fig. 11 shows measured differential non linearity (DNL) and integral non linearity (INL) characteristics on sampling frequency of 1 GHz. Rectangular points are DNL, triangular points are INL. DNL is less than 1.0, INL is less than 1.25 in all codes, very good results are obtained. In this case, supply voltage, current consumption and power consumption were 1.2 V, 44 mA and 52.8 mW, respectively.

IV. Conclusion

To realize high sampling rate and lower power consumption, current mode pipeline ADC focused on millimeter-wave band WPAN terminal is designed and fabricated.

Ramp signal input characteristic obtained normal operation as 5 bits ADC on 1 GS/s, when input was assumed to be

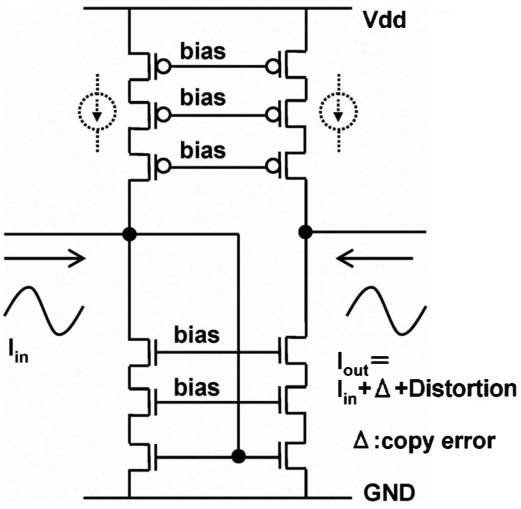

Fig. 7. 3-stages cascode current mirror.

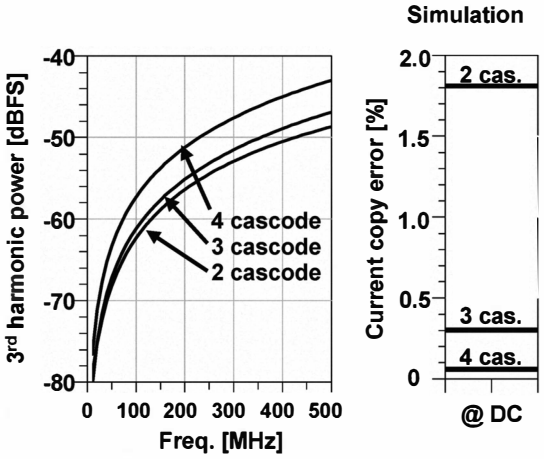

Fig. 8. Characteristics of cascode current mirror.

ramp signal input and monotonous increase. Moreover, DNL and INL obtained excellent result in all codes on 1 GS/s less than 1.0 and less than 1.25, respectively. From these results, high-speed sampling approached Flash type ADC by designed current mode pipeline type ADC.

ACKNOWLEDGMENT

The authors would like to thank Core Research for Evolutional Science and Technology (CREST) program of the Japanese Science and Technology Agency (JST) for fund support.

REFERENCES

[1] Y.-J. Kim et al., "A 10b 120MS/s 45nm CMOS ADC using a reconfigurable three-stage switched op-amp," CICC, 2010.
[2] K.-W. Hsueh et al., "A 1V lib 200MS/s pipelined ADC with digital background calibration in 65nm CMOS," IEEE ISSCC, 2008.
[3] A. Matsuzawa, "Trends in high speed ADC design," IEEE ASICON, 2007.
[4] A. Matsuzawa, "High speed and low power ADC design with dynamic analog circuits," IEEE ASICON, 2009.

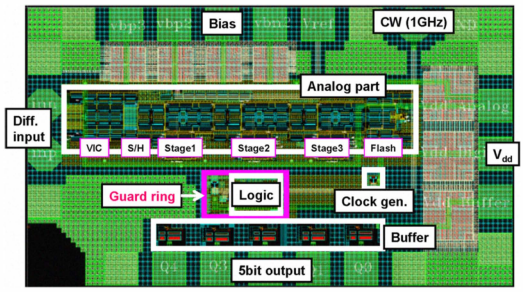

Fig. 9. Circuit layout of designed ADC.

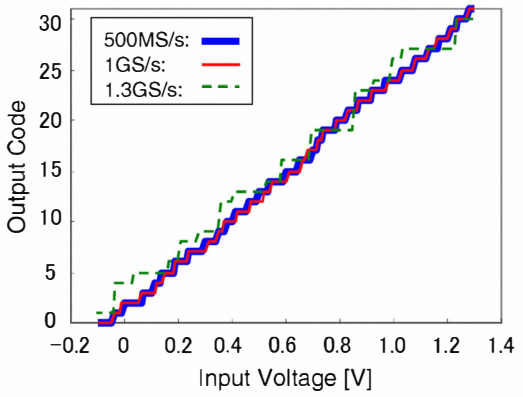

Fig. 10. ADC characteristics for ramp signal input.

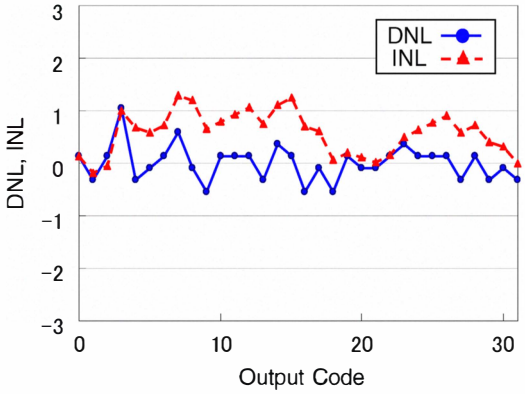

Fig. 11. DNL and INL characteristics.

[5] O. Bernal et al., "Current-Mode Pipelined ADC for High Resolution Monolithic CCD Processors," IEEE IMTC, 2005.
[6] P. Mahatthumthanant et al., "A Current-mode CMOS Sample-and-Hold Circuit for ADC," IEEE SICE-ICASE, 2006.
[7] Y. Sun et al., "Low Power High Speed Switched Current Comparators for Current Mode ADC," IEEE ISCIT, 2007.
[8] S. R. Krishna et al., "Current-mode CMOS pipelined ADC," IEEE EUROCON, 2009.