A 1.2 V 1.0-GS/s 8-bit Voltage-Buffer-Free Folding and Interpolating ADC

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***Abstract*—A single-channel 1.0-GS/s 8-bit Voltage-Buffer-Free Pipelined-Folding-Interpolating analog-to-digital converter (PL-FAI-ADC) is presented. Grouped T/H blocks are adopted to cancel the voltage buffer between the T/H block and the pre-amplifiers array. A new full-digital T/H switch is proposed to cancel the bootstrapped capacitor, which can save the chip area grandly. An improved single-diode switch with an extra reset path is proposed as inter-stage sampling switches. The ADC implemented in 65nm CMOS technology achieves SNDR of 47.5 dB and SFDR of 57.8 dB for 487.3 MHz input frequency at the rate of 1.0-GS/s. The power consumption is 75 mW with supply voltage of 1.2 V.**

I. Introduction

Low-power ADCs with gigahertz sampling frequency play an important role in broadband communication systems such as mm-wave receivers, OFDM-Based 60GHz receivers and future optical communication, which require high sampling rate and low power.

Currently, Most design of such kind of ADCs focuses on Time-Interleaved (TI) architecture using pipelined or Successive-Approximation-Register-Based (SAR) ADCs as sub-ADCs [4,7]. This kind of ADCs process high conversion rate with embedding more channel Sub-ADCs. But it also suffers from mismatch among sub-channels. Usually, digital calibration needs to be added and guarantees its performance. As a result, digital calibration will leads an extra chip area and power consumption. Furthermore, it may interrupt analog-to-digital conversion period.

In this design, a pipelined structure is applied in FAI-ADC to reach gigahertz sampling rate [3]. A cascaded folding amplifiers stage is adopted to reach high bandwidth [5]. A Voltage-Buffer-Free stage is proposed to cancel voltage buffers and save power consumption, where a full-digital T/H switch is presented to meet with an array application. Furthermore, an improved inter-stage sampling switch based on a single-diode bootstrapped switch [6] is inserted into analog pre-processing pathes to reach high sampling rate.

II. Voltage-Buffer-Free Folding and Interpolating Architecture

A. Voltage-Buffer-Free T/H Block

Traditionally, a high linearity voltage buffer is always implemented between the T/H block and the pre-amplifiers array [1,3]. The voltage buffer usually adopts a source-follower structure [3] to drive the next stage. Considering the settling precession depending high inputs linearity and wide outputs bandwidth of the source follower, the voltage buffer is required much higher driving currents. According to simulation results, this part of power consumption is about twenty percent of the whole ADC system. So canceling voltage buffers is critical for low power design.

However, if voltage buffers are not used, a kick-back noise will feed back to C_S. Where C_S stands for the sampling capacitor of the T/H block. The value of the kick-back noise depends on the rate of C_S and C_P. C_P is a sum of parasitic capacitors on inputs of pre-amplifiers, which is variable with different working modes of inputs transistors. And the working region of inputs MOSFETS is defined by the amplitude of signals. So the kick-back noise will be changed in different inputs amplitudes, which equals to adding a variable capacitor on C_S and will worsen the dynamic performance of the T/H block. In this paper, pre-amplifiers and sub-T/H switches are both divided into five groups as shown in Fig. 1. It means that C_P is divided into five parts, but sampling capacitors of each sub-T/H is not changed. The rate between $C_{P(1/5)}$ and C_S is reduced greatly. Though the kick-back noise still exist, the bad effect led by $\Delta C_{P(1/5)}$ can be ignored. Post-layout simulation results show that SFDR (Spurious Free Dynamic Range) increases about 5 dB, and ENOB is improved 1 bits in the same simulation environment.

What is more, considering a same load for each pair of outputs in one sub-T/H block with different inputs, Fig. 1 shown that the first part and the fifth part make a cross-linking connection. Meanwhile, the second part and the fourth part are also connected like that. That will weaken even harmonics led by the mismatch between the plus end and the minus end.

B. Pipelined Folding and Interpolating Architecture

As shown in Fig. 1, five stages form a pipelined folding and interpolating ADC system. The implementation of a T/H array saves the voltage buffer and a resistor ladder between two reference voltages generates 35 level voltages in the first stage. The 35 level voltages generated by the former stage divide the whole quantified range into 34 sections for five groups of pre-amplifiers, which is composed by 36 overall differential

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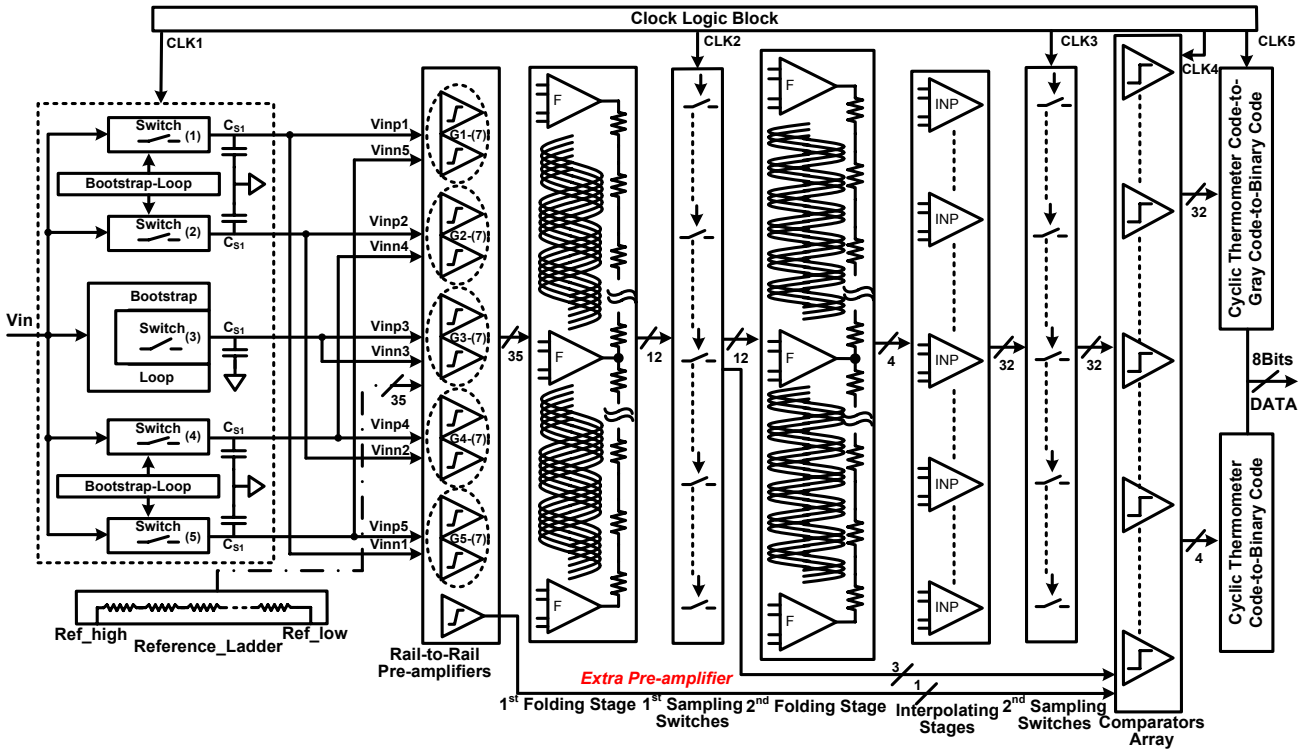

Fig. 1. Block diagram of the ADC

rail-to-rail amplifiers with resistive load including dummies. 12 folder signals with 35 zero-crossings are generated by the first stage of two cascaded-stage folding amplifiers [5], and sampled by the first inter-stage sampling switches in the second pipelined stage. In the next pipelined stage, 12 folded signals through the second folding stage become 4 folded signals with 35 zero-crossings, which are interpolated by a 3-stages active interpolating block with the interpolating factor $2X$ of each stage [5]. In the final two pipelined stages, comparators array receives 32 pairs of differential signals from the former inter-stage sampling switches, 3 pairs of differential signals generated by the first folding stage and one pair of differential signals generated by an extra pre-amplifier. 36 digital logic signals generated by comparators are divided into two groups. One group is used to encode low 5-bit, which are encoded from cycle thermometer codes through gray codes to binary codes. The other one is used to encode high 3-bit, which are encoded from cycle thermometer codes to binary codes directly. This encoding method guarantees the precision of lower bits and the low power of higher bits.

Besides, one of the non-ideal factors of such kind of ADCs is the mismatch among folding or interpolating signal pathes, which can be reduced by adopting an averaging resistor network. Considering the gain of folding amplifiers reduction and the complex connections led by adding the averaging resistor network, a cascaded averaging resistor network is used in this design [5].

III. CIRCUIT DESIGN

A. Full Digital T/H Switch

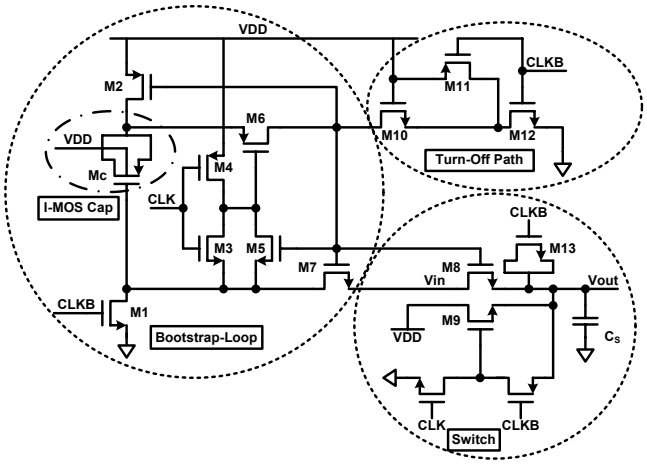

Fig. 2. A full digital track and hold bootstrapped switch

Most of bootstrapped switches include two parts. Fig. 2 shows them. One is the bootstrapped loop and the other is a bootstrapped switch. A capacitor is always needed to bootstrap the gate voltage of the switch, whose value is about 1-1.5 pF in generally. When a MOM capacitor is adopted to reach it, it will take up much larger chip area and not be suited for an array application.

In this design, a full digital T/H switch is proposed to meet with a array application in this paper. As shown in Fig. 2, a MOSFET capacitor in inversion mode (I-MOS capacitor) is used to replace the MOM capacitor as a bootstrapped capacitor. The curve of a MOSFET capacitor depended different modes is shown in Fig. 3 (a). The horizontal axis shows a voltage difference between the gate and the source/drain of an I-MOS capacitor, and the longitudinal axis shows values of an I-MOS capacitor. As known to all, the voltage difference between two sides of a bootstrapped capacitor is about VDD either in the reset mode or the bootstrapping mode. So the region marked by dotted lines is real working region as a bootstrapped capacitor in this design. The voltage difference between two sides of the bootstrapped capacitor is about from 0.95 V to 1.1 V, which leads the nonlinearity of an I-MOS capacitor change from 0.949 pF to 1.101 pF. The bad effect led by ΔC can be ignored. Furthermore, the chip area saved by this improvement is much considerable. Fig. 3 (b) shows the rate between one I-MOS capacitor area and one MOM capacitor area with a same capacitor value. The former is about twenty five percent of the later.

Besides, several MOSFETs are introduced to overcome the effect of clock through and charge injection such as M9, M13 in this full digital T/H switch. Where the size of M9 is the same as M8 and the size of M13 is half of M8. Meanwhile, M10, M11 and M12 are added to assist M8 in turning off.

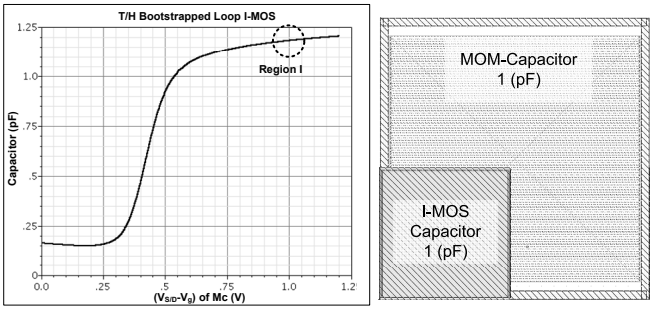

Fig. 3. (a) An I-MOS curve of T/H switch (b) A comparison of the area between IMOS-Cap and MOM-Cap

B. Inter-stage Sampling Switch with Reset Path

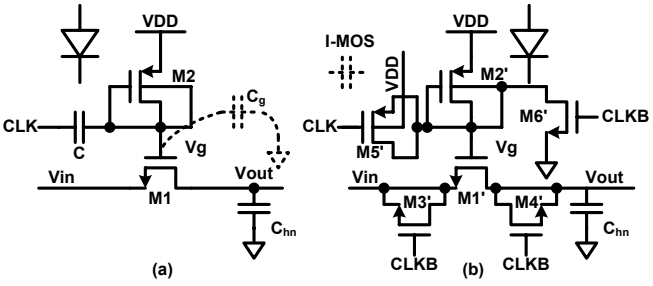

Fig. 4. (a) A single-diode inter-stage sampling switch (b) An improved inter-stage sampling switch

In a pipelined folding and interpolating structure, inter-stage sampling switch is used to shorten the analog signal pre-processing path. Inter-stage sampling switches are required to have a small on-resistance and a simple structure. In the published works [3], CMOS switches are used, but the overdrive voltage of a CMOS switch is smaller with the lower supply voltage. On-resistance of it will be increased, which will introduces a longer signal delay and more thermal noise. As an alternative, a bootstrapped switch is useful to lower the on-resistance and reduce the signal delay in low supply voltage. But the complicated bootstrapped circuits [9] are not suitable for a array mode in terms of chip area and power efficiency.

Fig. 4 (b) shows an improved single-diode bootstrapped switch with a reset path proposed in this paper, which is based on a kind of single-diode bootstrapped NMOSFET sampling switch shown in Fig. 4 (a) [6]. Where M1 is the NMOSFET switch and C_{Hn} is the next stage inputs capacitor. M2 and C compose the bootstrapped circuit. The substrate and the drain of M2 are connected together (N-well technology is adopted), so that M2 works as a diode. The source of M2 as the positive terminal is led to V_{DD} and the gate, drain and substrate are all led to the gate of M1 as the negative terminal (V_g), which prevents the PN junction formed between the N-well and the P+ source diffusion from becoming forward biased, and allows positive voltage swings larger than the threshold voltage of a PN junction over V_{DD}. During a positive edge of ΔV_{CLK}, V_g would have a positive step of ΔV_g along with CLK and M1 would turn on. Similarly, a negative edge of CLK awakes a negative step of V_g and M1 turns off. ΔV_g is given as

$$\Delta V_g = \frac{C}{C + C_g} \cdot \Delta V_{CLK} \tag{1}$$

Where C_g is the total parasitic capacitor of V_g and C is a coupling capacitor. C_g mainly composes of two variable capacitors. One is the gate capacitor of M1, and the other is the PN junction's capacitor. They would change with the bias voltage of the node V_g. So C_g has floating values in positive edge or negative edge of the CLK, which leads to a difference between $\Delta V_{g,r}$ and $\Delta V_{g,d}$. If $\Delta V_{g,r}$ is larger than $\Delta V_{g,d}$, the extra charge would be accumulated at the node V_g and rise its voltage. M1 would be broken down.

In this design, an extra reset path is added to discharge the extra charge at the node V_g and avoid breaking down. Furthermore, an I-MOS capacitor is adopted to take place of MOM capacitors and saves much chip area. Compared with CMOS switches, bootstrapped switches and traditional single-diode switches, it features a lower and invariable on-resistance, simplicity and stableness. It is more suitable for the inter-stage sampling switches array.

IV. EXPERIMENTAL RESULTS

A single-channel 1.0-GS/s 8-bit $PL\text{-}FAI\text{-}ADC$ is designed in 65-nm CMOS. The core area is about 0.24 mm^2. The layout photograph is shown in Fig. 5. Fig. 6 shows the post-layout simulated SNDR/SFDR versus input signal frequency

at 1.0 GS/s in the worst process corner. SNDR/SFDR achieves 48.1 dB/56.0 dB at a 12.7 MHz input and 47.5 dB/57.8 dB at a 487.3 MHz input, respectively. Fig. 7 shows the post-layout simulated ENOB versus input signal frequency at 1.0GS/s in the worst process corner. ENOB is maintained above 7.6 in the whole nyquist frequency range. The total power consumption is 75 mW at a 1.2 V supply voltage. The performance summary is given in Table I, and its FOM is 0.39 pJ/Conv-step ($Fom = P_{diss}/(2^{ENOB} \times 2 \times ERBW)$).

TABLE I
PERFORMANCE SUMMARY AND COMPARISON

PARAMETER	[1]	[2]	[This work]
Technology	55-nm	90-nm	65-nm
Sampling Rate	1GS/s	1.25GS/s	1.0GS/s
Resolution	8-bit	8-bit	8-bit
ENOB	6.9bit	7.0bit	7.7bit
ERBW	400 MHz	625 MHz	500 MHz
Supply	1.2 V	1.0 V	1.2 V
Power	16 mW	207 mW	75 mW
Active Aera	0.2 mm^2	0.66 mm^2	0.24 mm^2
Fom(/Conv-step)	0.164 pJ	1.2 pJ	0.39 pJ

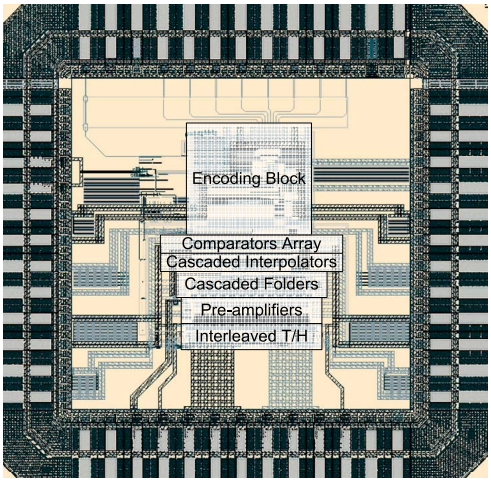

Fig. 5. Layout of the Chip

V. CONCLUSION

A 1.0-GS/s 8-bit single-channel Voltage-Buffer-Free PL-FAI-ADC is presented. The post-layout simulation results show that the ENOB is larger than 7.6 bits across the full Nyquist range at a sampling rate of 1.0-GS/s. Its power consumption is 75 mW in a performance efficient way at 1.2 V supply voltage.

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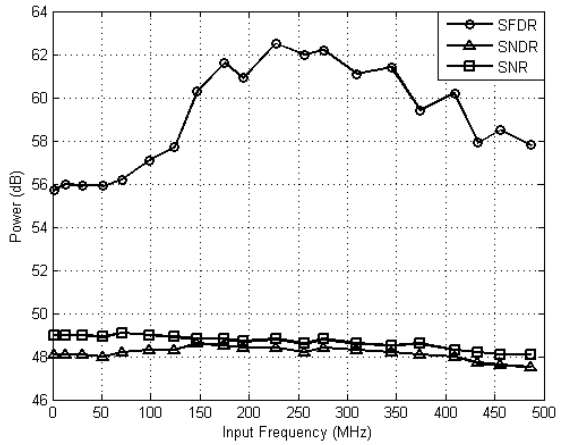

Fig. 6. Post-layout simulated SNR/SNDR/SFDR versus Fin

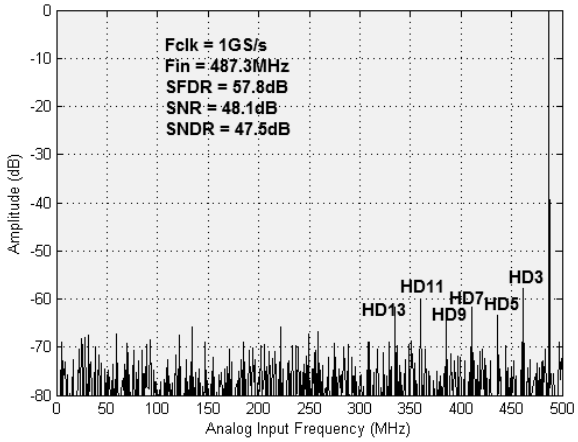

Fig. 7. The spectra of the ADC output when Fin= 487.3 MHz

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