3 GS/s S-Band 10 Bit ADC on SiGeC Technology

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Abstract—

In advanced applications such as digital radar, Ultra Wide Bandwidth communications and software defined radio, the need for instantaneous bandwidth often drives system design decisions. Access to high speed data converters enabling up and down conversion directly in the L Band and S Band removes the limit imposed by bandwidth scarcity and allows the design of flexible and simplified system architectures. Broadband ADC's (Analogue to Digital Converters) are key enabling components which open up new design opportunities for digital Receiver systems.
In this regard, this paper describes a new 10bit 3GS/s ADC with 5 GHz Bandwidth, based on a 200 GHz SiGeC bipolar Technology, which enables the direct digitizing of 1GHz arbitrary broadband waveforms directly in the high IF region closer to the Antenna (L-Band or S-Band) .

Keywords: Development of next-generation broadband flexible radar systems; Increased sampling rates, bandwidth and resolution; Broadband instantaneous frequency capture; Direct sampling of arbitrary UWB signals in the L-Band or S-Band;

I. INTRODUCTION

High speed ADCs featuring a good linearity over a wide range of frequency inputs are key components for new generations of broadband RF Radar Receivers.
In this regard, a new generation of low latency Ultra Wide Band ADC circuitry based on a 200 GHz SiGeC (SiGe Carbon) fully bipolar Technology has been designed to serve the next-generation broadband flexible radar and countermeasure systems.

II. 10 BIT 3 GS/S ADC AND TECHNOLOGY

A. 10 Bit 3 GS/s ADC based on 200 GHz SiGeC (SiGe Carbon) Technology

The 10-Bit ADC operates at 3 GS/s (Giga Samples per second) and features 5 GHz full power input bandwidth which allows operation in either L-Band or S-Band.
The ADC is packaged in a Multi-Chip-Module (MCM) EBGA317 (Enhanced Ball Grid Array) with a 1:4 DMUX companion chip, with selectable output DMUX ratio.

The ADC is based on a single core architecture, and does not rely on internal interleaved core ADCs to achieve 3GS/s. Hence, the ADC does not require any calibration before or during operation over temperature as sometimes required with multi-cores architectures to align the gain, offset, and aperture delays to avoid intermodulation performance degradation.
The ADC embeds multiple 8 Bit Control DACs, which are monitored through a 3 Wire Serial Interface (3WSI), for remote fine tuning of the ADC sampling delay, gain and offset. This feature is useful for instrumentation applications which can tolerate calibration, enabling easy interleaving of multiple ADCs to increase the actual sampling rate.

B. Performance enabling SiGeC Technology

III. The ADC is manufactured on SiGeC bipolar HBT technology[3]. The process uses a double-polysilicon self-aligned transistor configuration, with shallow and deep trench isolation, featuring selective epitaxial growth of boron doped SiGeC base; Carbon reduces boron diffusion (steep doping profile), and graded Ge profile gives accelerating drift field for electrons. This technology offers NPN transistors with a cut-off frequency (fT) of 200 GHz at a current density of 6.5mA/um2, and fmax of 300GHz, which allows high performance with low power trade-off. The metallization consist of four copper layers with a 2.5-um-thick top layer. In addition, two poly-silicon resistor types, thin film TaN resistors, and MIM capacitors are available.

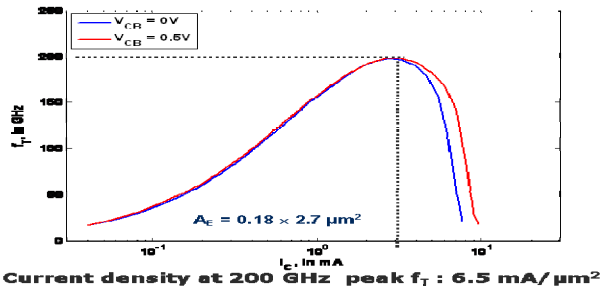

Figure 1. SiGeC transistor measured peak cutoff frequency (fT) vs. current density

IV. 10 BIT 3 GS/S ADC +1:4 DMUX

A. Receiver System Architecture improvements

Innovative architecture concepts together with the high cut-off frequency of the SiGeC Technology allows for enhanced

linearity and noise performance for the ADC enabling 5 GHz full power input bandwidth, and update rates of 3 GS/s together with multi Nyquist operation. Direct under sampling of Ultra Wide Band (UWB) signals of up to 1GHz instantaneous bandwidth in either L-Band or S-Band can be envisioned. The following figure (Fig.2) depicts the architecture improvement in terms of size, power, complexity and cost of a typical receiver system based on a performing UWB ADC.

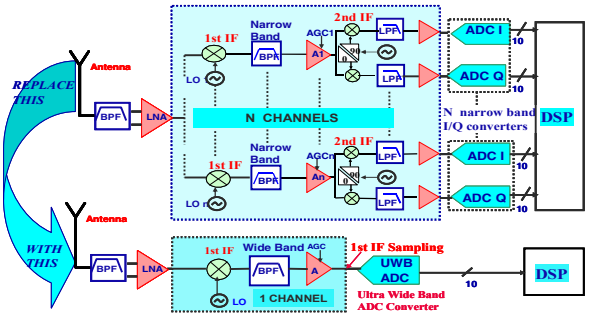

Figure 2. Example of Receiver System Improvement with UWB ADC

B. 10 Bit 3 GS/s ADC Chip Description

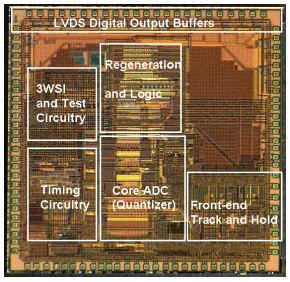

Figure 3. 10 Bit 3 GS/s ADC Microphotograph

The ADC is based on 100 % fully bipolar vertically isolated NPN transistors. Component count is 6500 SiGeC transistors and 8000 oxide isolated resistors (Fig.3). Accurate thin film TaN resistors are used for embedded 50Ω terminations.

The interconnections are based on four levels of Copper metallization to achieve low RC parasitic. The ADC architecture is fully differential from Analog input and Clock input up to the LVDS compatible Digital Outputs. The ADC Power Consumption is 4.2 Watt at Tj = 125°C junction temperature. Power supplies are +5.0V and +3.3V for the Analog section, and + 2.5V for the digital output buffers. The 1:4 DMUX companion chip is designed on a 45 GHz fully bipolar SiGe technology, and operates up to 4 GS/s for a power dissipation of 2.3 Watt. Total Power is nearly 6.5 Watt.

C. 10 Bit 3 GS/s ADC Architecture general Description

The ADC architecture is based on a fast settling Core ADC (analog quantizer), driven by a front-end Track and Hold (T/H). The T/H is a bipolar version of the differential switched follower structure described in [1]. The T/H shall feature enhanced large signal dynamic performance in track mode, together with fast hold to track acquisition times, in order to recapture the analogue input after hold mode in less than ¼ of the clock period, i.e. in less than 80ps at 3 GS/s. The analogue quantizer is designed to settle to final accuracy within the T/H hold mode time width of nearly 150ps. The analogue quantizer is based on a flash like architecture, featuring uniform quantification noise, and does not rely on noise shaping techniques, used for instance in band-pass multi bit sigma-delta converters. The quantizer is based on fast settling cascaded folding and interpolation structures [2], designed to feature low throughput propagation delay, together with low input dynamic loading effect for the front-end T/H.

D. ADC Characterization Results

1) ADC Single Tone FFT Computation at 3 GS/s in 1st, 2nd and 3rd Nyquist zones

At 3 GS/s in the 1st Nyquist (Fin=1495MHz, -1dBFS), an ENOB of 8 Bit and an SFDR of 59 dBc is achieved (Fig. 4).

In the 2nd Nyquist (Fin=2995MHz, -3dBFS), an ENOB of 8 Bit is still achieved, with an SFDR performance of 58 dBc (Fig. 5). With Fin=3995MHz (-3dBFS), corresponding to the S-Band upper limit, the ENOB is still 7.7 Bit, with an SFDR of 55dBc, and the SNR is 49dBFS (Fig.6). The SNR roll off versus input frequency is related to the voltage noise induced by the 120fs rms internal sampling clock jitter of the ADC. The large signal linearity roll off over frequency is mainly related to the dynamics of the front-end Track and Hold.

The 0dBFS ADC Full Scale reference voltage span is 500 mV. The Full Scale input power is -2dBm if single-ended driven in 50Ω, and -5dBm if differentially driven in 100Ω termination. At 3 GS/s and Fin = 3 GHz, an SNR of 50 dB is leading to an FFT noise floor of: SNR + 10log (N/2) = 50dB+10log (16384 points)=92dB per 32K FFT bin width.

The normalized noise floor in dBc/Hz at Fs=3 GS/s is 50 dB + 10log (Fs/2)=141.7dBc/Hz. Since ADC Full Scale differential input power is -5dBm, the normalized (per/Herz) Noise floor is -5dBm-142dB=-147dBm/Herz. The ADC total noise power includes the input referred thermal noise and the voltage noise induced by sampling clock jitter. Therefore the contribution of the ADC to the overall system noise figure can be estimated.

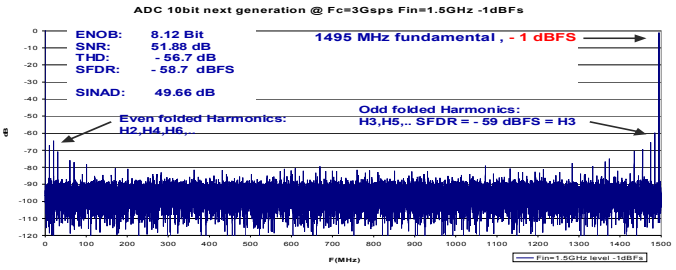

Figure 4. FFT Computation at 3 GS/s 1st Nyquist Fin= 1495 MHz , - 1dBFS

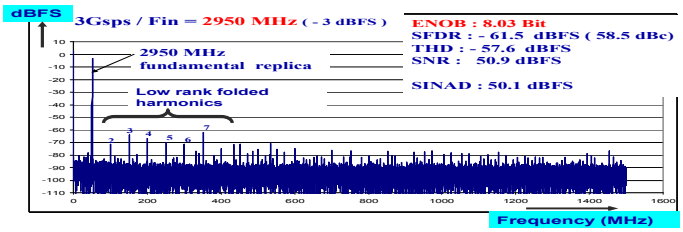

Figure 5. FFT Computation at 3 GS/s 2nd Nyquist,Fin= 2950 MHz , - 3dBFS

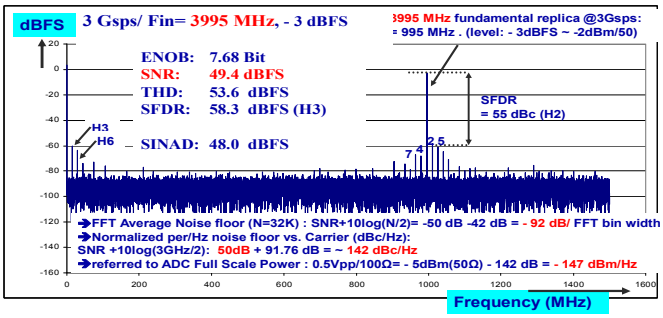

Figure 6. FFT Computation at 3 GS/s 3rd Nyquist, Fin=3995 MHz , - 3dBFS

2) Single Tone ENOB, SNR and SFDR rolloff characteristics at 3 GS/s over 3 Nyquist Zones vs. Input level

The single tone Signal to Noise and Distortion (SINAD) relationship is reminded here below, showing the different noise components and harmonic contributions to the Effective Number of Bit (ENOB) of the ADC:

$$SINAD = 20\,Log \frac{Arms}{\sqrt{n_{qi}^{\,2} + n_{qd}^{\,2} + (n_{thermal})^2 + (n_{jitter})^2 + \left(\frac{Arms}{10^{\frac{THD}{20}}}\right)^2}}$$

With : SINAD = 6,02.ENOB + 1,76 (Sinewave input)

and with : Arms: rms Input level
Nqi: Ideal ADC Quantization noise : q/√12
Nqd: deviation from ideal quantization noise = DNL (rms)
Nthermal : thermal noise (ADC front-end T/H, input referred)
Njitter : voltage noise induced by sampling clock jitter
THD: Distortion components: (10 first low rank Harmonics)

3) Single Tone ENOB, SNR and SFDR rolloff characteristics at 3 GS/s over 3 Nyquist Zones vs. Input level

The following figures depict respectively the ENOB (Fig. 7, 8), the SNR (Fig. 9,10) and SFDR (Fig. 11,12) characteristics versus analogue input frequency measured at 3GS/s over 3 successive Nyquist zones (DC up to Fin = 4 GHz), covering the L-Band and S-Band regions. The signal level is ranging from -1dBFS to -18dBFS, to illustrate large signal roll off over frequency performance versus small signal performance.
The ENOB roll-off characteristics depicted in (Fig.6) results from the contribution of SNR (Noise) and THD (Linearity) components which are RSS summed.
Another way to illustrate the large signal versus small signal roll off is shown in (Fig.7), with the ENOB plot versus input level, for different input frequencies.
The ADC features more than 8 Bit ENOB at 3 GS/s in the 1st Nyquist zone for signals close to ADC Full Scale. In the 2nd Nyquist, an ENOB of 8 Bit is still achieved for slightly lower input levels (-3dBFS). In the 3rd Nyquist with Fin=4GHz, the 8 Bit ENOB performance is achieved with -6dBFS input levels. At -1dBFS and Fin=4GHz, the ENOB rolls off to 7.2 Bit is due to large signal non linearity effects in the front-end T/H, and voltage noise induced by sampling clock jitter .

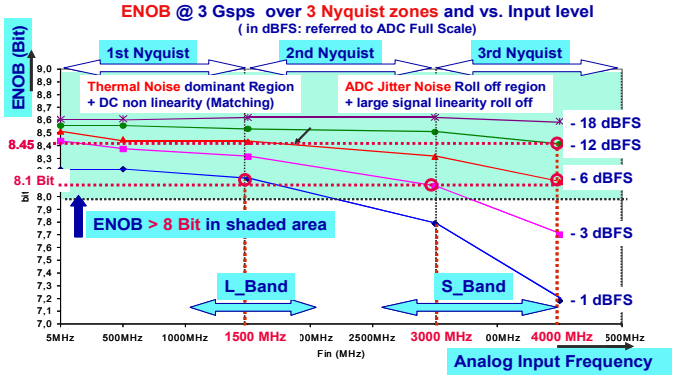

Figure 7. ENOB roll off over 3 Nyquist zones at 3 GS/s vs. Input level

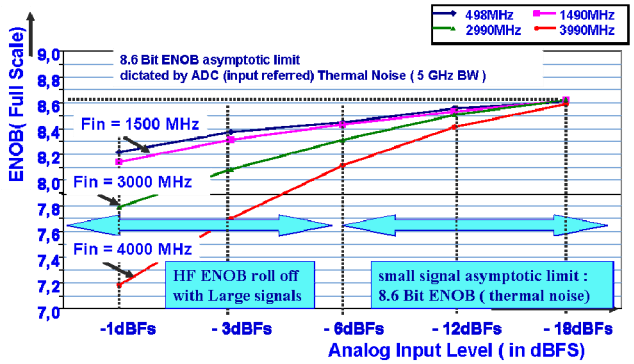

Figure 8. ENOB roll off vs. input level at 3 GS/s and vs. input frequencies

The SNR Characteristic roll off (Fig. 9, 10) is dictated mainly by two noise components:
- The ADC input referred thermal noise, related to front-end T/H thermal noise spectral density integrated over ADC input Bandwidth (i.e.: 5GHz.Π/2). Since the thermal noise power features much higher weighting than the quantization noise power, it clips the SNR to 54 dB, instead of 62 dB if only ideal 10bit quantification noise is considered.
- The voltage noise induced by sampling clock time jitter: The ADC internal jitter is 120 fs rms, causing the SNR to roll off for fast slewing analogue inputs (e.g.: SNR=54dB for low input frequencies and SNR=50 dB at Fin=3GHz, -1dBFS).
Phase Noise floor requirements for clock source shall be better than 155dBc/Hz: for a 5.5 GHz integration bandwidth, the L(f) integrated Single Side Band (SSB) phase noise floor 10log (Rad^2/Hz) expressed in dBc/Hz is given by: -155+10log ($5{,}5.10^{09}$) = -57.6 dB. The total integrated phase noise power is SQRT ($2.10^{-57{,}6\,/\,10}$) = $1{,}86.10^{-03}$ radians (rms). With a 3 GHz sinewave clock source, the corresponding rms time domain jitter is $1{,}86.10^{-03}$ radians (rms) / 2.Π.3GHz = 98 fs rms. An SSB phase noise floor of 160dBc/Hz will only contribute for 55 fs rms time jitter. Total sampling clock jitter will be: SQRT (120^2 +50^2) =130fs rms. Therefore any clock source phase noise floor in the range of 160dBc/Hz will have negligible contribution to total sampling jitter.

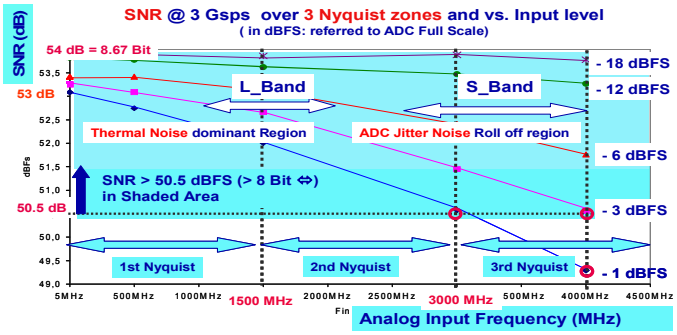

Figure 9. SNR roll off over 3 Nyquist Zones at 3 GS/s & vs. Input level

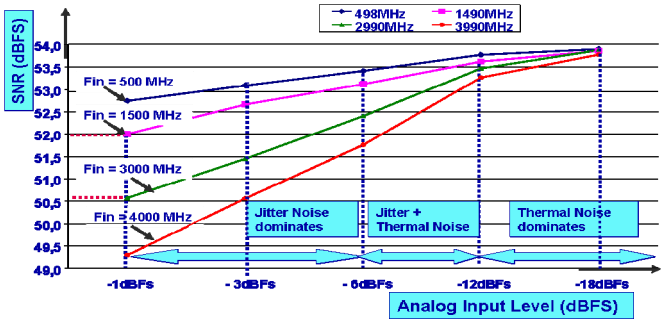

Figure 10. SNR roll off 3 GS/s vs. input level and vs. input frequencies

The Spurious Free Dynamic Range (SFDR) roll off characteristic is shown in (Fig.10, 11) over three Nyquist zones. The large signal distortion rolloff over frequency and versus signal level is depicted. The - 60dBFS spurious level is achieved in the 1st Nyquist with - 1dBFS level, - 3dBFS in the 2nd Nyquist, and - 6dBFS in the 3rd Nyquist region.

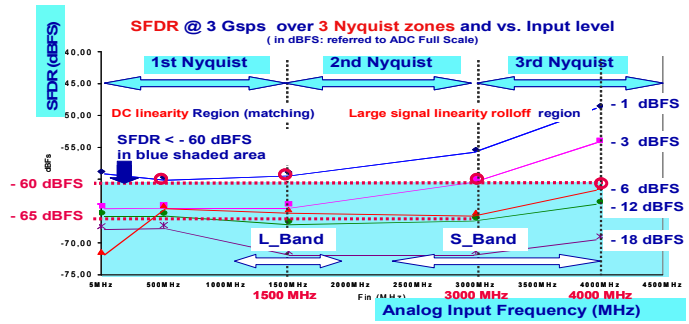

Figure 11. SFDR roll off over 3 Nyquist Zones at 3 GS/s vs. input level

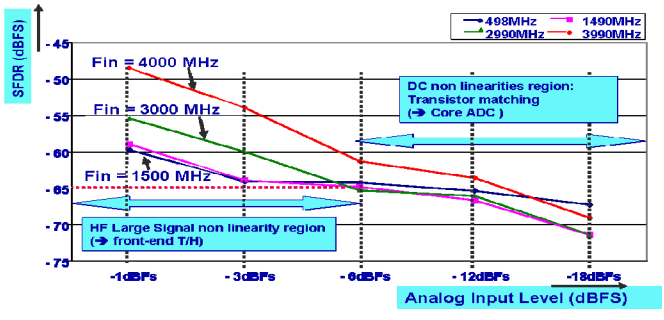

Figure 12. SFDR roll off 3 GS/s vs. input level and vs. input frequencies

4) Dual tone FFT computations at 3 GS/s and IMD3 performance in 1st Nyquist and 2nd Nyquist.

Dual tone FFT computations were carried out at 3 GS/s with -7dBFS tones places at (2950MHz,2960MHz), showing the different inter modulation products. The IMD3 performance is given by the (2F1-F2, 2F1-F2) non filterable product terms close to the carriers. The IMD3 performance is 58 dBc in the 2nd Nyquist region (Fig.13) Complement of investigation still needs to be carried out at higher input frequencies (3rd Nyquist) and for lower input levels to check small signal IMD3.

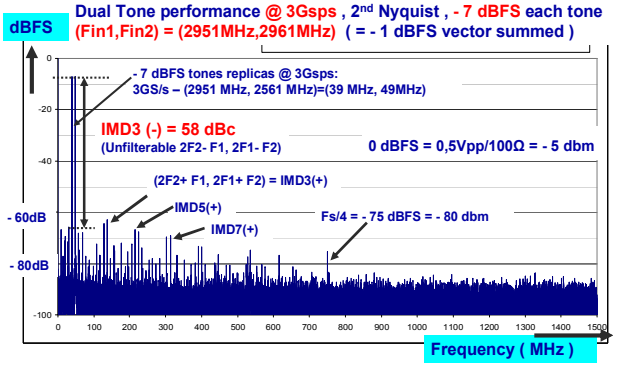

Figure 13. Dual Tone FFT computation at 3 GS/s (295MHz, 2961 MHz)

V. 10 Bit 3 GS/s ADC Broadband Noise Power Ratio Performance

A. Noise Power Ratio (NPR) General

The dynamic performance of an ADC with broad bandwidth input is sometimes characterized by measuring a quantity known as the Noise Power Ratio (NPR). In ADC applications where the input signal contains a large number of incoherent tones or narrow bandwidth signals, it is generally desired that distortion, due to combinations of strong signal components, should not interfere with detection of weaker signal components. An example of such an input signal is one which contains a large number of frequency division multiplexed (FDM) channels, which are stacked in frequency for transmission over Radar equipments:

For instance, 5MHz Channels may be stacked over a 500 MHz or 1000 MHz instantaneous Band of Interest.

The NPR is the measure of the spectral power of all contributed RMS errors, such as inter modulation distortion (cross channels interference), quantization noise, thermal noise and jitter noise, in a narrow frequency slot (channel width) within the band of the composite signal being processed.

Optimum loading Factor (Peak to RMS):

In Broadband FDM Systems having several hundreds of Channels stacked over frequency, the FDM incoming Signal Amplitude distribution can be approximated by Gaussian Noise Probability Density Function (PDF).

Therefore, the RMS level of the composite input signal shall be tuned at an optimum factor k from the ADC full Scale, in order to achieve the optimum between saturation noise (ADC Full scale clipping effect) and ADC quantification Noise:

Quantification and saturation represent added noise terms at the device output. They depend both on:
The number of bit of the ADC (number of quantization levels), and the rms input level relative to the saturation level of the converter.
For a given number of Bit, the rms (σ) input level of the composite signal is adjusted to minimize the sum of the two noise powers, at an optimum factor *k*.
e.g: for a 10 Bit ADC the optimum peak to rms loading factor is k = 4.50, with 20log (k) = - 13.1dBFS. (Fig. 15)
From a mathematical background, the total noise power PN due to ADC error signal *e(x)* can be broken into 2 components: Quantization Noise QN (error signal from 0 to *kσ),* and Saturation Noise SN (error signal integrated from *kσ to infinite)* , with :

$$Q_N = 2\int_0^{k\sigma} e^2(x)P(x)dx \qquad S_N = 2\int_{k\sigma}^{\infty} e^2(x)P(x)dx$$

$$P(x) = \frac{1}{\sigma\sqrt{2\pi}}e^{-x^2/2\sigma^2} \qquad Q = \frac{k\sigma}{2^{N-1}-1}$$

For a more complete mathematical background on NPR see the reference paper from G. A. Gray and G. W. Zeoli [3].
For an ideal ADC, taking into account the quantification noise only, the relationship between broadband NPR and single tone SNR is given by:

$$SNR(ideal) = 20\log\frac{A/\sqrt{2}}{Q/\sqrt{12}} \qquad NPR(ideal) = 20\log\frac{rms(\text{broadband pattern level})}{Q/\sqrt{12}} = 20\log\frac{A/k}{Q/\sqrt{12}}$$

yielding (for an ideal ADC): NPR = SNR - 20log(k)+3dB
With A/k the rms level of the broadband composite signal.
For a real ADC, the relationship includes all noise components (quantification, thermal, jitter) and intermodulation products:

$$SINAD(real\_ADC) = 20\log\frac{A/\sqrt{2}}{\sqrt{(Q/\sqrt{12})^2 + (Thermal)^2 + (Jitter)^2 + (THD)^2}}$$

$$NPR(real\_ADC) = 20\log\frac{A/k}{\sqrt{(Q/\sqrt{12})^2 + (Thermal)^2 + (Jitter)^2 + (IMD)^2}}$$

1) Noise Pattern Generation for ADC Noise Power Ratio Measurement

To measure the ADC NPR, the noise pattern is synthesized by a 12 Bit 3GS/s DAC (also designed by e2v), featuring 53 dB NPR at 3 Gsps with 1 GHz pattern (> 10 Bit ENOB) in the baseband, which is enough to measure the NPR of the ADC estimated to 43 dB at 3GS/s with a 1GHz pattern. The spectrum of a 1 GHz UWB patterns with 50 MHz notch synthesized at 3 GS/s and replicated over 1st, 2nd and 3rd Nyquist zones is shown in (Fig.14). The NRZ mode null function sinc(x) of the DAC does not allow operation in the 2nd and 3rd Nyquist. For operation in the 2nd and 3rrd Nyquist, a mixed mode (RF) needs to be implemented in a future version of the 3 GS/s DAC, which will enable L-Band and S-Band pattern generation with appropriate band-pass filtering.
The 3GS/s replicated patterns have been low pass filtered at 1.5 GHz.

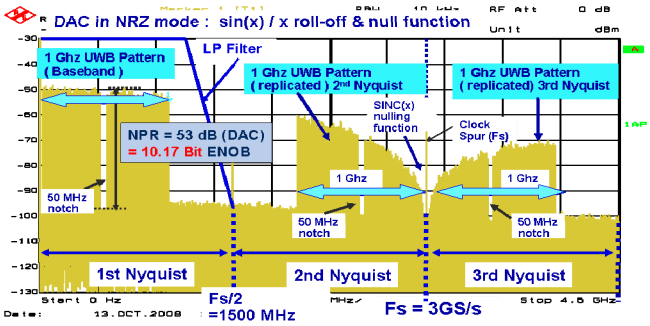

Figure 14. 12 Bit 3GS/s DAC NPR pattern in NRZ mode replicated over 3 Nyquist zones (DC to 4500MHz) for ADC pattern generation

2) ADC Noise Power Ratio Measurement

To illustrate the NPR issue, the following is an example of a 700 MHz noise pattern with 5 MHz notch, synthesized at 3GS/s by a 12 Bit DAC, low pass filtered in the 1st Nyquist, and re-sampled by the ADC at 1.5GS/s. The noise pattern in time domain sampled by the ADC (131.072 samples), is shown in (Fig.15), with Gaussian Probability Density function for signal amplitude distribution. The rms (σ) level of the composite signal is at optimum loading factor k =4.50 from ADC Full Scale (10 Bit) ; with 20log(k) = -13dBFS.

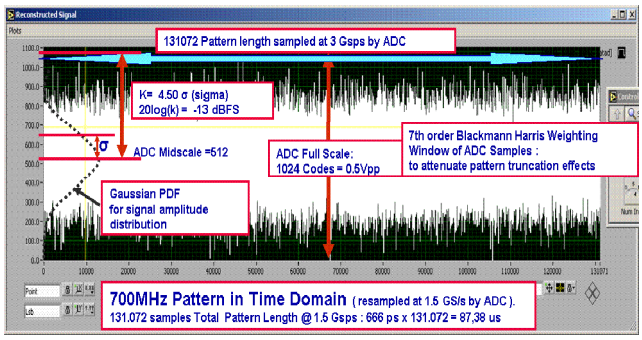

Figure 15. Gaussian Distribution (PDF) for Time Domain Pattern amplitudes

The corresponding pattern in frequency domain is shown in (Fig.16). A 7th order Blackman-Harris weighting window has been used to attenuate the truncation effect of the 131.072 samples of the noise pattern. The NPR is computed as the ratio of the average power spectral density inside the notched frequency to that outside the notched band.

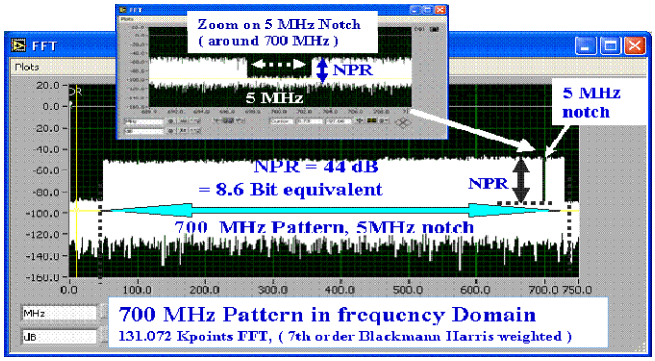

Figure 16. 700 MHz frequency doimain Pattern sampled at 1.5 GS/s with 5 MHz notch : NPR = 44 dB (ENOB = 8.6 Bit equivalent)

With an ideal ADC, the notch is filled with quantization noise only. For a real ADC, the notch is filled with additional thermal noise, voltage noise induced by time jitter, and intermodulation products resulting from all the surrounding carriers placed within the pattern. Hence, the NPR is representative of the ADC performance digitizing UWB patterns. The measured NPR at 1.5 GS/s with 700 MHz pattern is 44 dB, which is 8.6 Bit equivalent, showing strong correlation with single tone ENOB in the small signal region. At 3GS/s with 1 GHz pattern, the expected NPR is 43 dB which is 8.5 Bit ENOB equivalent: measurements will be available for the conference. The following are ideal NPR curves versus loading factor, computed for ideal ADCs (10Bit to 16 Bit), compared to the 10 Bit ADC measured NPR.

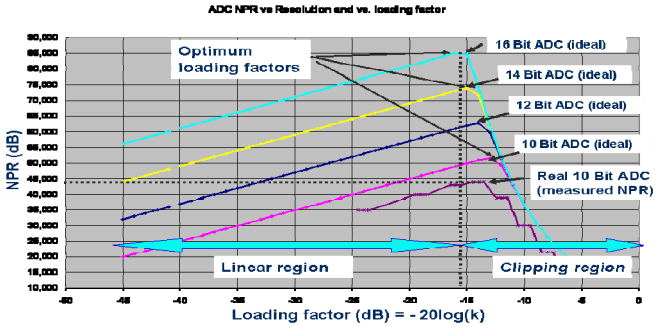

Figure 17. NPR versus loading factor for ideal 16 to 10 Bit ADCs, vs. measured NPR for 10 Bit ADC.

VI. Packaging and Testing Issues

The increased sampling rates also created new challenges in package HF modelling and industrial testing:
The ADC Multi Chip Module (MCM) EBGA317 Package has been developed with the help of 3D-HF Software for the design of the 50 ohms controlled impedance lines, to minimize the effect of package transition impedance discontinuity (Fig.18). The measured input VSWR is lower than 1.5:1 from DC up 5 GHz. The maximum junction temperature is 110°C for 6.5Watt total power. The junction to board thermal resistance is ~ 10°C/Watt, and junction to case is 4°C/W. Using a 4°C/Watt heat-sink the thermal resistance becomes 10°C/Watt in parallel with 8°C/Watt = 4,4°C/Watt, which allows nearly for: 110°C-30°C = 80°C ambient temperature.

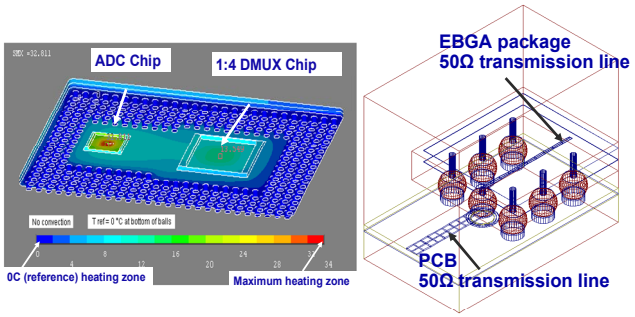

Figure 18. EBGA317 MCM Package Thermal resistance computation ; 3D HF modelling of 50Ω transmission line (board to package transition).

The packaged ADC parts are tested industrially and screened at full operating speed (3GS/s). The testing board features 50 ohms controlled impedance transmission lines together with adequate shielding and very low test fixture parasitic.

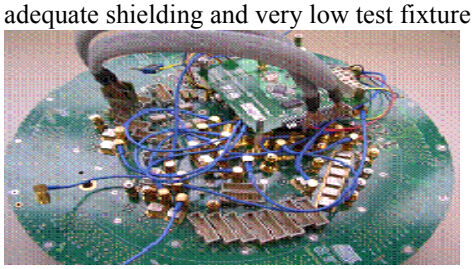

Figure 19. Test Board for screening the packaged 10 Bit 3 Gs/s ADCs

VII. Summary

A 10 Bit 3 GS/s ADC featuring 5 GHz full power input bandwidth showing multi Nyquist sampling capability of 1GHz instantaneous bandwidth signals has been designed and fabricated on a 200 GHz SiGeC bipolar technology. The ADC has been characterized at 3 GS/s over three Nyquist zones, showing cutting-edge performances with the direct sampling of 1 GHz UWB signals directly in the L-Band or in the S-Band, simplifying the RF transceivers complexity, cost and size, with increased flexibility for Radar systems.
Based on the same SiGe:C platform and similar architecture, further axis of improvements for the ADC can be envisioned, depending on Radar needs: Either increasing the ADC Bandwidth (e.g. up to 7-8 GHz) and sampling speed (e.g. 4 GS/s), to cover the entire S-Band in the 2nd Nyquist region, or increasing the resolution for > 9 Bit ENOB and nearly 70dBc SFDR by operating at lower rates (1GS/s to 1.5GS/s) to improve settling accuracy.

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References

[1] Huseyin Dinç, Phillip E. Allen "A 1.2 GSample/s Double-Switching CMOS THA With - 62 dB THD" IEEE Journal of Solid-State Circuits, vol. 44, N0. 3, March 2009.

[2] Alireza Razzaghi, Sai-Wang Tam, Pejman Kalkhoran, Yu Wang, Chih-Yi Kuan, Brian Nissim, Lan Duy Vu, M.C. Franck Chang,"A Single-Channel 10b 1GS/s ADC with 1-cycle latency using pipelined cascaded folding,", IEEE BCTM 16.4,2008,pp.265–268

[3] J.Böck, H.Schäfer, K.Aufinger, R.Stengl, S.Boguth, R.Schreiter, M.Rest, H.Knapp, M.Wurzer, W. Perndl, T.Böttner, and T.F. Meister, "SiGe bipolar technology for automotive radar applications" in *Proc. Bipolar/BiCmos Circuits and Technology Meeting (BCTM)*.,Montreal, Canada, Sep. 2004, pp.84-87.

[4] Glenn A. Gray, Gene W. Zeoli, "Quantization and Saturation Noise Due to Analog-to-Digital Conversion" IEEE Transactions on Aerospace and Electronic Systems of Solid-State Circuits, January 1971.