DESIGN OF 4-BIT PARALLEL SUB-SAMPLING A/D CONVERTER FOR IR-UWB RECEIVER

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ABSTRACT

This paper presents the design of a dual-channel 4-bit analog-to-digital converter (ADC) for the sub-sampling impulse radio ultra-wideband (IR-UWB) receiver with the sampling rate of 2.112 GS/s. The ADC's specifications are optimized at the system level. Two parallel channels help to achieve high conversion speed and low power consumption. To tackle the problem of clock mismatch between the channels, a twice sampling front end is used. An improved averaging termination technique using intended asymmetric spatial filter response is proposed. This design is simulated in a 0.13 μm CMOS technology with 1.2 V power supply. Simulation results show a 26 dB SNDR in 4.8 GHz bandwidth with 36 mW power consumption and the Figure of Merit (FOM) is 0.24 pJ/step.

Index Terms— ADC, sampling, averaging, comparator

1. INTRODUCTION

Impulse radio ultra-wideband (IR-UWB) is one of the attractive technologies for near-field wireless communication. In 2002, the Federal Communication Commission (FCC) authorized the use of UWB signal for communication purpose in the band from 3.1 to 10.6 GHz with a minimum bandwidth of 500 MHz [1]. An analog-to-digital (A/D) converter is the key component to construct an IR-UWB receiver because demanding requirements on speed, accuracy and power consumption exist in the front-end and make the design challenging [1], [2]. The input signal frequency of most ADCs is generally lower than half of the sampling frequency, as determined by the Nyquist sampling theory. An obvious solution, which requires capturing an input Gaussian pulse whose band spans from 4.3 to 4.8 GHz, is to use an ADC, which is capable of sampling at a frequency two times higher than 4.8 GHz. However, such a converter consumes about hundreds of milliwatts. Therefore, a low-power sub-sampling ADC is desired.

In this paper we describe the conception, design, and optimization of a 4-bit parallel sub-sampling flash ADC for 4 GHz band UWB application. A twice sampling front end avoids the clock mismatch between channels. The self-biasing buffer supports the sub-sampled signal passing to the following comparator array. A comparator without preamplifier with offset self-calibration is used here to save power consumption. An improved averaging termination technique using intended asymmetric spatial filter response corrects the edge threshold shift. The ADC consumes 36 mW power and achieves 4.8 GHz Effective Resolution Bandwidth (ERBW). The FOM value of 0.24 pJ/step referred to the Nyquist rate ADC proves the efficiency of the proposed design.

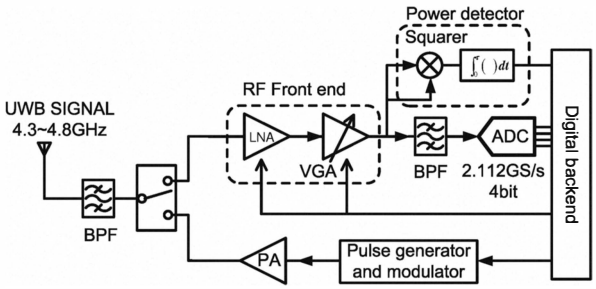

Fig. 1. Architecture of the proposed IR-UWB transceiver

2. ADC SPECIFICATION

ADC's specifications such as sampling rate and resolution should be analyzed at the overall receiver level. Fig. 1 shows the non-coherent sub-sampling transceiver blocks. Down-converter is replaced by ADC directly without PLL simplifying the front end design. The signal transmitted from the TXs with 4 dBm strength would be attenuated dependent on the wireless distance. Considering the worst situation, ten meters between TXs and RXs, the attenuation will be around 60 dB. If the RF front end has 50 dB power gain, the minimum average peak value approaches 80 mV as the ADC's input. Therefore, the full scale is designed of 400 mV_{pp} or -4 dBm with enough margin.

Since the power consumption of a Flash ADC scales exponentially with number of bits, minimizing ADC resolution is crucial to reduce the power consumed in the receiver. The bit-error rate (BER) generated from a infinite resolution ADC

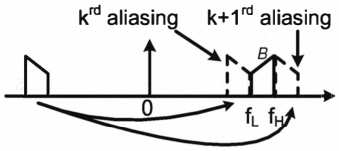

Fig. 2. Sampling rate based on bandpass Nyquist theory: spectrum alias of sampled bandpass signal

keeps close to a 4-bit converter. This is true in both a noise-limited environment where the signal is degraded by additive white Gaussian noise (AWGN) and in an interference-limited environment, where the signal is corrupted by a powerful narrowband sinusoidal interference [1]. Another important parameter is the sampling rate. As mentioned before, the ADC sub-samples the input bandpass signal which spans from 4.3 to 4.8 GHz. The spectrum aliasing is shown in Fig. 2. To ensure the k^{rd} and $k+1^{rd}$ aliasing from negative frequency not overlap the initial bandpass signal, there should be

$$\begin{aligned} -f_L + kf_s &\le f_L, \\ -f_H + (k+1)\, f_s &\ge f_H, \end{aligned} \tag{1}$$

where f_s is the sampling rate, f_L, f_H are the minimum and maximum frequencies of bandpass signal respectively. Then we have

$$f_s \in \bigcup_{k=0}^{\left\lfloor \frac{f_L}{B} \right\rfloor} \left[\frac{2f_H}{k+1}\ \frac{2f_L}{k} \right],\ 0 \le k \le \left\lfloor \frac{f_L}{B} \right\rfloor. \tag{2}$$

Here eq. 2 describes the discrete regions available for bandpass sampling behavior [3]. On the other hand, UWB impulse is so narrow in the time domain that it doesn't need to be sampled too densely. For a Gaussian impulse with 500 MHz bandwidth in the 4G band, it keeps effective in a 2.6 ns time window. If it is sampled by a 2 GHz clock, five points would be captured successfully resulting in no information loss. Finally a sampling rate of 2.112 GHz is decided accordingly with the factor k of 4 in the eq. 2.

3. CONVERTER DESIGN

3.1. Proposed ADC Architecture

In order to achieve the required data throughputs, two parallel channels work under anti-phase clocks. It is used to relax the bandwidth limitations of the individual channel except for the front-end track and hold blocks. This leads to a more efficient sub-sampling converter with reduced overall power consumption. The flash ADC's architecture is shown in Fig. 3. An open-loop THA front end is implemented to ensure the desired dynamic range. The first THA avoids the clock mismatch between parallel channels. A source follower (SF), following the second THA, buffers the sampled signal

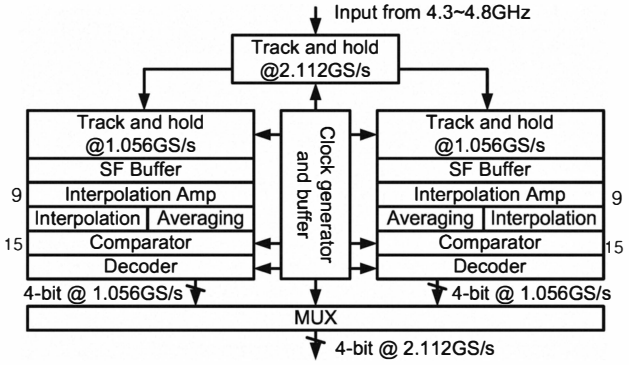

Fig. 3. 2-GS/s 4-bit ADC architecture

and isolates it from back-award blocks. Interpolation generates required reference voltage saving the number of front amplifiers. An offset-calibrated comparator is used to quantize analog values. To correct the bubble error from high-speed glitches, the decoder transfers the Thermometer code to the Gray code at first then maps it to the Binary code. All the analog signal paths are fully differential.

3.2. Improved Averaging Termination

Averaging technique used extensively in flash ADCs. [4] shows that averaging acts like a spatial filter which smoothes the zero-crossing transconductors' current contributions. It has the advantage of reducing the offset voltage from the front amplifier. Generally the differential nonlinearity (DNL) gets more improvement than the integral nonlinearity (INL). However, the practical averaging includes the boundary offset shifting to inside which deteriorates the linearity at the network edge. Either dummy amplifiers with sufficient number to preserve a infinitely long character of array or special termination circuits to compensate edge offset [4], [5] are used in previous works. But large number of dummies would waste the full scale range and too much power consumption, on the other hand, special termination always require delicate control of amplifier's input transconductance which is not efficient adequately.

To solve the averaging termination efficiently, an network with intended asymmetric spatial filter response is proposed as shown in Fig. 4. Conventional spatial filter response is symmetric as shown in Fig. 5(a) with R_T/R_1 equaling one. Here W_{IR} is width of a rectangular impulse response [5], $h(n)$ is relative response to the main distributed current as described in eq. 3. This profile is practical when the input signal lies at the center of full scale because hardware keeps balance too. Obviously this is not true at the boundary even though cross connection is adopted. Fig. 5(b) shows the block diagram of the correction scheme, where W_{ZX} is defined as a rectangular signal window [5]. Front amplifiers outside the W_{ZX} would goes into saturation region. Not like other exist-

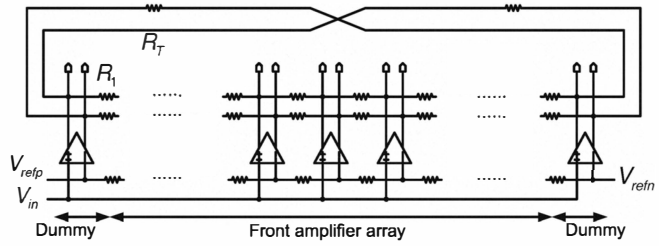

Fig. 4. Proposed averaging network with dummy amplifier and cross connection with optimized R_T/R_1

ing termination techniques which adjust dummy amplifiers, an intended asymmetric spatial filter just keeps single dummy on both sides and adjusts the boundary averaging resistor R_T to match the filter character to the W_{ZX} window as shown in Fig. 5(a). W_{IR} on the right-hand side is reduced as the increasing R_T/R_1, suppressing the current contribution from two dummies. $H(n)$ is absolute response derived from

$$h(n) = b^{-|n|},\ b = e^{-\left|a\cosh\left(1+\frac{R_1}{2R_0}\right)\right|} < 1,$$
$$H(n) = \frac{h(n)}{\sum_i h(i)}, \tag{3}$$

Actually spatial response depends not only on the position but also on the ratio between averaging resistor R_1 and the front amplifier's loading resistor R_0. Although offset reduction would be improved by small R_1/R_0 [5], the factor is always decided close to one for enough gain of the front amplifier. From Fig. 5(a), asymmetric response would touch a limitation as R_T/R_1 increasing. During this process, a best ratio could be found by sweeping termination reference voltage offset ratio with R_T/R_1 as shown in Fig. 5(c). In this design, R_1/R_0 equals 0.9 and R_T/R_1 is adjusted to 7 with error ratio less than 1%.

3.3. Analog Circuit Implementation

3.3.1. THA

As the front end block of a sub-sampling ADC, the THA not only tracks and holds the analog signal but also overcomes the clock mismatch between different channels. Fig. 6 shows the employed twice sampled THA. NMOS transistors M_1 and M_2 are used as sampled switches. Dummy transistors reduce the charge injection influence. Self-biased source followers [2] M_3 and M_4 are adopted to grantee enough gain and output swing at 1.2V power supply. Replica source followers M_5 and M_6 with smaller size compared to main follower which help to bias the back-gate of M_4 so that there is no body effect and bulk capacitor loading. Replica source followers employs self-biasing too. MOS capacitors are inserted across between followers' input and output to absorb the kickback noise from

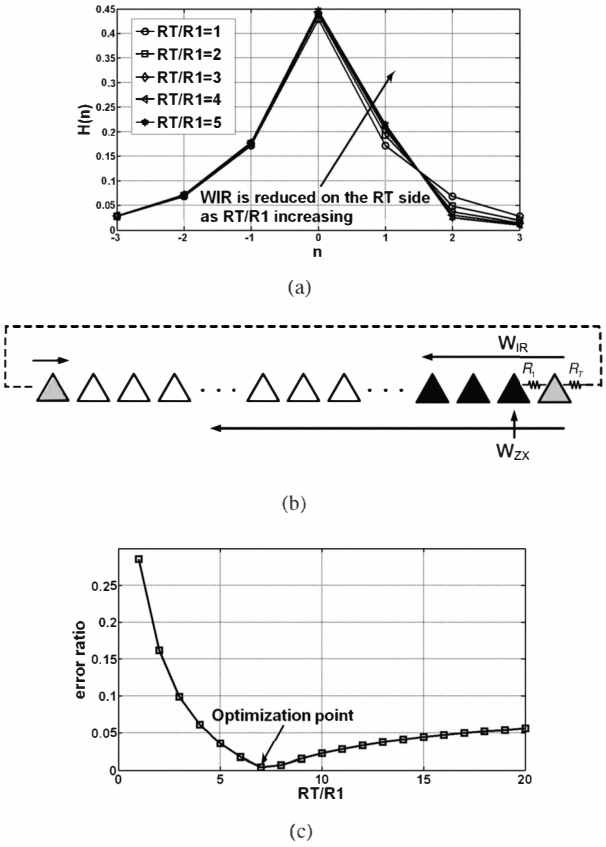

Fig. 5. intended asymmetric spatial filter response: a) averaging network with a input at boundary b) spatial filter response with different R_T/R_1 c) optimization ratio decision for minimum static error

back-award circuits. Here $clks$ is sampling clock with 2.112 GHz which is two times of $clk1$ and $clk2$.

3.3.2. Comparator

An offset self-calibrated comparator [6] is used in this design as shown in Fig. 7. M_1 M_4 form a sensing amplifier which is sensitive for the input difference followed by a digital latch. The whole dynamic comparator only consumes current when operation happens. The threshold voltage offset of the input transistors is stored on C_{os} during clk_a when M1 and M2 are cut off as follows

$$V_{Cos1} = V_{cmi} - V_{t1} - V_b,\ \ V_{Cos2} = V_{cmi} - V_{t2} - V_b, \tag{4}$$

and applied to the overdrive voltage of M1 and M2 during clk_L as follows

$$\begin{aligned} V_{ov1} &= V_{cmi} + 0.5v_{in} - V_{Cos1} - V_{t1} = V_b + 0.5v_{in}, \\ V_{ov2} &= V_{cmi} - 0.5v_{in} - V_{Cos2} - V_{t2} = V_b - 0.5v_{in}. \end{aligned} \tag{5}$$

Here V_{Cos} is voltage of capacitors, V_{cmi} is input common-

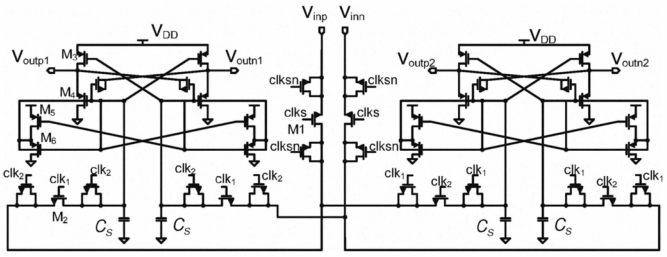

Fig. 6. Twice sampled THA with self-bias source follower buffer for parallel ADC

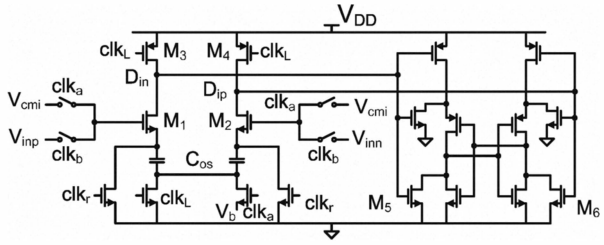

Fig. 7. Circuit of the comparator

mode voltage, V_t and V_{ov} are threshold voltage and overdrive voltage of input transistors. Offset has no effect on the final comparison result. Using self-calibrated comparator, a high frequency preamplifier before comparator can be omitted to save power consumption. clk_r resets the plate voltage of C_{os}. ADC's clock waveform is shown in Fig. 8.

4. SIMULATION RESULTS

The entire parallel flash ADC is simulated at transistor level with a 4.8 GHz input tone. The master clock is generated from a buffered sinusoidal waveform by inverters. The SNDR and SFDR of ADC is 25.8dB and 35.9dB respectively using 4096-points FFT. Fig. 9 shows the spectrum of the ADC. To value the performance of the simulated converter, the FOM defined by $Power/\left(2^{ENOB} \times 2ERBW\right)$ is used, where $ERBW$ and $ENOB$ are the effective resolution bandwidth and effective number of bits, respectively. A FOM value of 0.24pJ/step indicates the design efficiency.

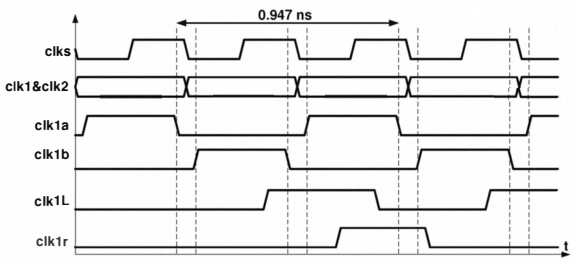

Fig. 8. Multi-phase clocks of ADC

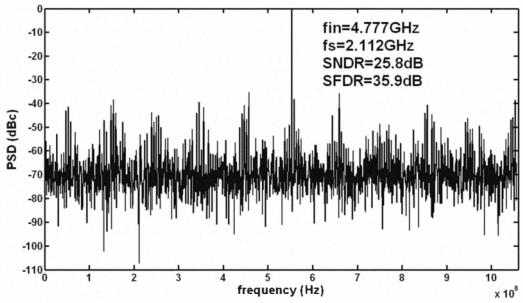

Fig. 9. The FFT plot of the designed ADC at f_{in}=4.8GHz

5. CONCLUSION

A 2.112 GS/s 4-bit parallel flash ADC is designed in 0.13 μm CMOS technology for sub-sampling IR-UWB receiver. An improved asymmetric averaging termination technique is used to tackle the boundary offset. To save the power consumption, a self-calibrated comparator is proposed without preamplifier. Simulation shows that 36 mW is paid for 25.8 dB SNDR and 35.9 dB SFDR with 4.8 GHz input signal.

6. REFERENCES

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