4-bit, 15 GS/s ADC in SiGe

Yevgen Borokhovych
Chair of System Design
IHP/BTU Joint Lab
Frankfurt (Oder), Germany
borokhovych@ihp-microelectronics.com

Hans Gustat
Department of Circuit Design
IHP
Frankfurt (Oder), Germany

***Abstract*— This paper presents a high-speed 4 bits full-flash Analog-to-Digital Converter for an UWB radar applications, implemented in 190 GHz SiGe BiCMOS technology. The ADC occupies 1.5 x 1.5 mm^2, including bondpads. Converter has 6 GHz input bandwidth and operates up to 15 GSample/s. Power dissipation is 1 W including test buffers and 600 mW for a core part itself.**

I. INTRODUCTION

Ultra wideband (UWB) radar is of great interest for a number of applications such as surface penetrating radar, surveillance and emergency radar, medical instrumentation, non-destructive testing in civil engineering and the food industry, industrial sensors and many others.

UWB radars have excellent spatial resolution and it is supposed that they can be advantageously applied in the field of localization. There are a number of applications that would take advantage from precise indoor positioning such as automatic storage, tracking of various targets (e.g. at airports), or people in dangerous environments and so on.

II. ARCHITECTURE

The simplified architecture of M-sequence UWB radar is shown in Figure 1. The UWB-system operates in a frequency range from DC to 10 GHz. The ADC, which is located closely to the antenna, has to operate at least up to half of system frequency. Full-flash architecture well suited for gigahertz range and therefore it was chosen for the implementation.

A block-diagram of the ADC is shown in Figure 2. In general the full-flash architecture does not need a track-and-hold amplifier (THA) [1]. But one of the limiting factors of ADC performance is a clock jitter. If the frequency of the input signal is high, the clock uncertainty can cause errors. For 5 GHz input frequency to have the error lower than ± 1/2 LSB the jitter has to be lower than $\Delta t < 1/2\pi f_{in} 2^N < 1.9 ps$, for 4 bits ADC. A general relation between signal to noise ratio and clock jitter is: $\mathrm{SNR} = -20\log(2\pi f_{in}\Delta t)$ [2].

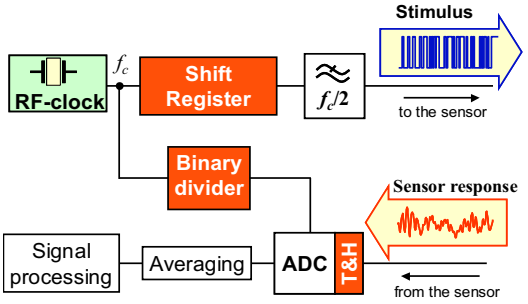

Figure 1. M-Sequence UWB Radar Architecture.

To prevent degradation of the ADC performance due to clock jitter and relax requirement to the clock distribution the differential track-and-hold amplifier is used at the front of the ADC. After THA the quasi-constant input signal is divided in 16 equal parts by a reference network and converted into thermometer code by comparators. An encoding circuitry converts thermometer code into binary code. Output buffers are used to drive output digital signals over 50 Ohm loads during the measurement.

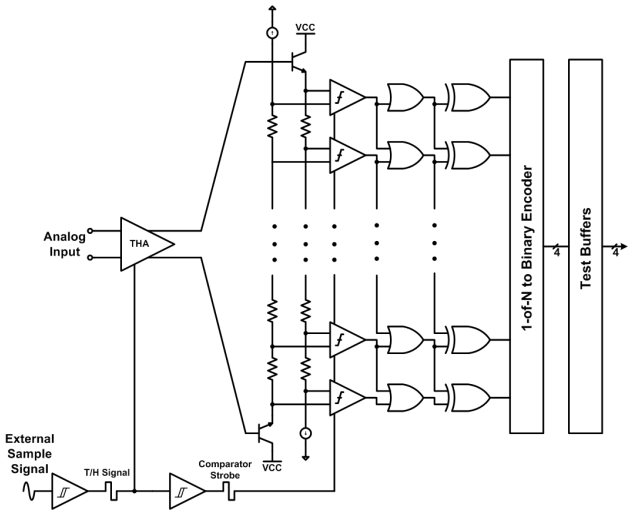

Figure 2. Block-diagram of the ADC.

III. CIRCUIT DESIGN

A. THA

For very high speed and moderate accuracy, differential open-loop architecture is an obvious choice. As shown in Figure 3, the THA includes a fully differential THA core based on the well-known switched-emitter-follower (SEF) proposed by Vorenkamp [3]. Beyond the hold capacitors C_H, pseudo differential output buffers are used. The simplicity of the SEF circuit described in [3] allows design for low power dissipation. In this THA type, the load resistors of the input differential stage along with their parasitic capacitances dominate the settling time. To reduce this effect and the power consumption, minimum-size transistors are used throughout the THA core. The design goal was to achieve 15 Gs/s operation at minimum power while maintaining an accuracy of ≥ 5 bits.

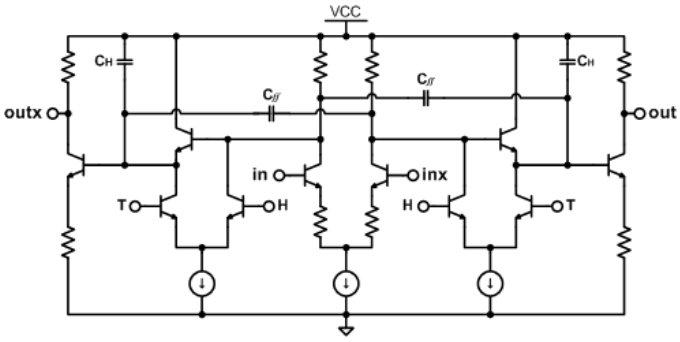

Figure 3. Fully differential THA architecture.

B. Comparator

The comparator usually consists of preamplifier, master and slave latches. There are several factors that limit performance of the comparator: 1) Ability of the preamplifier to amplify the input signal which is changed from maximal value to LSB, overdrive conditions; 2) Kickback noise, due to injection of charge into the base. The kickback noise can significantly distort input signal and further follows to erroneous comparison; 2) Recovery time of the comparator, t_{rec}, the time to change logic output of the comparator to midpoint of logic stage. Worst case is when input signal is 1/2 LSB; 3) Charge time t_{charge} – time required to charge base-emitter capacitance of the latch; 4) Regeneration time t_{reg} – time that comparator needs to achieve output voltage.

A simple differential pair with emitter followers usually used as amplification stage in the preamplifier. But the differential pair can not properly amplify the input signal under overdrive conditions. At high frequencies sensitivity of the preamplifier drastically decreases. Consequently the sensitivity of the whole comparator also decreases. The good solution of this problem is the limiting amplifier based on Cherry-Hooper architecture. Advantages of this amplifier in our case are: 1) Better sensitivity; 2) Good isolation of latch stage from the reference network. It allows to omit emitter followers after amplification stage and decrease power; 3) Lower power dissipation compare to differential pair with emitter followers. The Cherry-Hooper amplifier utilizes two current sources, but to achieve required bandwidth the total current will be lower than the current of the differential amplifier with emitter followers.

The performance of the latch is limited by the recovery time and the regeneration time. They can be estimated by formulas (1) and (2), [4].

$$t_{rec} = R_L C_{total} \ln\left(1 + \frac{1}{\tanh\left(\frac{qV_{in}}{2kT}\right)}\right) \quad (1)$$

$$t_{reg} = \tau_{reg} \ln\left(\frac{4V_T}{LSB}\right), where\ \tau_{reg} = \frac{C_{total}}{g_m}\left(\frac{g_m R_L}{g_m R_L - 1}\right) \quad (2)$$

From (1) and (2) obvious that performance of the latch mainly depends on load resistance R_L and total parasitic capacitance C_{total}. Minimum-size transistors minimize parasitic capacitance and also minimize power dissipation of the comparator. The full schematic of the comparator is shown in Figure 4.

To further improve performance of the latch an additional current source I1 is added. This current source gives us several benefits: 1) It decreases time to charge base-emitter capacitance; 2) Being negative resistance, increases gain of track stage and decreases recovery time. The payment for those benefits is hysteresis, which decrease sensitivity of the latch. The current I_1 has to be sufficiently small, about 10% from tail current.

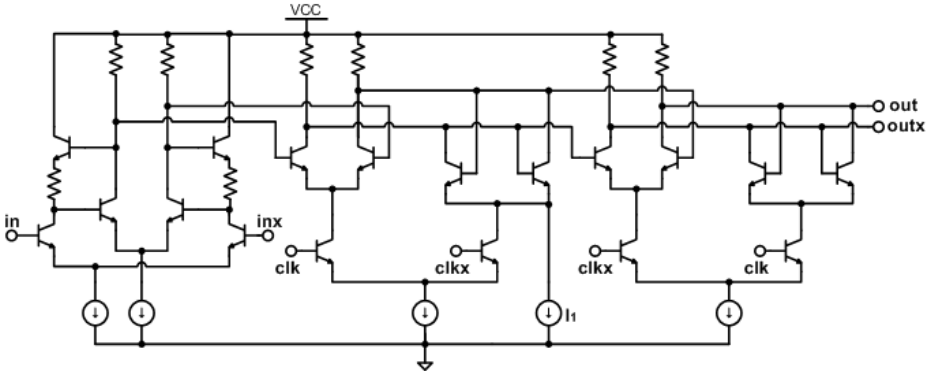

Figure 4. Schematic of the comparator.

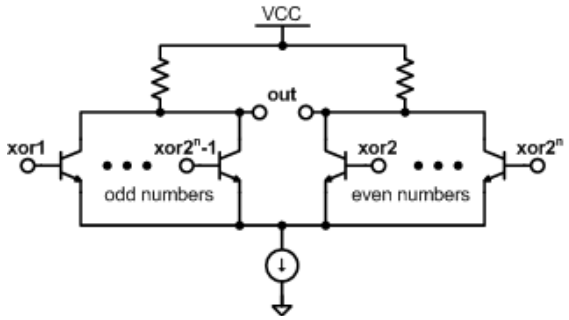

Figure 5. Configuration of wired-OR gate for conversion 1-of-N code to LSB.

C. *Encoder*

Produced by comparators thermometer code goes to encoding circuitry (encoder). The encoder can be logically divided in two parts: correction logic and thermometer-to-binary encoder. The correction logic can detect and correct errors in thermometer code. The states of two adjacent comparators are analyzed therefore only one erroneous output of comparator ("bubble") can be corrected. Two adjacent 'bubble' will cause an error in the output binary code. Corrected thermometer code is converted to 1-of-N code by XOR gates. It should be mentioned that obtained 1-of-N code is single-ended. It was made for minimization the number of logic elements and simplifying further encoding. 1-of-N code is converted to binary code by wired-OR gates. Figure 5 shows configuration of wired-OR for obtaining LSB. The wired-OR gate has differential structure and despite single-ended input it makes fully differential binary output.

IV. Experimental Results

The ADC is fabricated in a commercially available low-cost 0.25 µm 190 GHz SiGe BiCMOS technology [5]. The technology provides five metal layers with two thick top metals, a full suite of RF passive elements including metal-insulator-metal (MIM) capacitors and spiral inductors.

The chip micrograph is shown in Figure 6. The ADC occupies 1.5×1.5 mm^2 including bondpads. The pad configuration was optimized for on-wafer measurement with certain probe configuration.

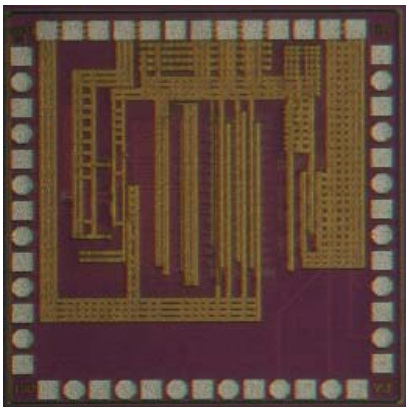

Figure 6. Chip micrograph.

To characterize a static performance of the ADC, the slow 50 MHz quasi-triangle (sine with big amplitude) input signal was digitized with 5 GSample/s sample rate. The output binary code was registered with 4 channels 20 GS/s real-time oscilloscope and reconstructed using internal mathematic functions. Despite the ADC is fully differential, only single-ended outputs were used for measurement due to measurement set-up limitation. The reconstructed 50 MHz input signal is depicted in Figure 7. Both rise and fall edges of reconstructed signal are symmetrical and stairs are regularly distributed. The width of stairs in the central part is lower than width of stairs in the top and bottom because input sine signal is only approximately linear, and this nonlinearity is represented by the variation of stairs width. An integral and differential nonlinearity of ADC itself are less than 1/2 LSB.

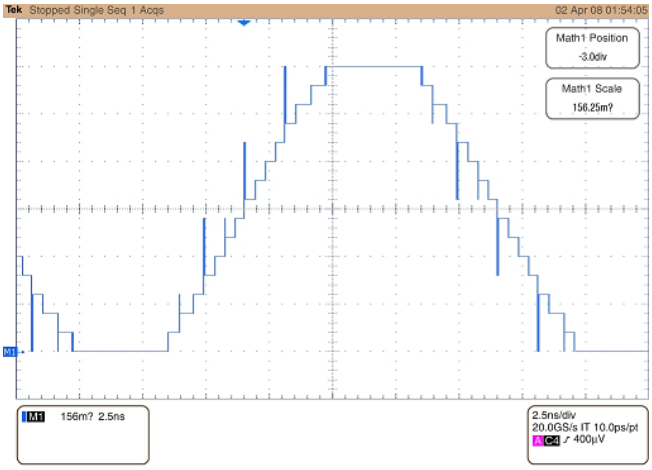

Figure 7. Transfer function of the ADC at 50 MHz sine input and 5 GS/s sample rate.

The bandwidth of the ADC was measured using a beat frequency method. This method allows qualitative estimate maximum frequency of input signal, which can be resolved by the ADC. The performance of the ADC is degraded at 6 GHz input, the levels '0000' and '1111' are narrower from ideal, but all quantization levels still present and there are no missing codes. Further increasing of the input frequency leads to disappearing of quantization level which corresponds to binary code '0000', therefore the non-missed code bandwidth of the ADC is 6 GHz.

To characterize a dynamic performance, the ADC was tested over whole input frequency range with constant sample rate equal to 15.01 GS/s. Input signal was applied with the amplitude 1 V_{p-p}, which corresponds to dynamic range of the converter. Output of the ADC was reconstructed as described above and transformed into frequency domain. Signal-to-Noise-and-Distortion-Ratio (SINAD) was measured at each input frequencies. The Figure 8 shows performance of the ADC over frequency range up to 5 GHz at constant 15.01 GS/s sample rate.

TABLE I. COMPARISON OF HIGH-SPEED ADCS

Sample Rate, GS/s	Resolution, bits	ENOB, bits	Bandwidth, GHz	Power Dissipation, W	FOM, pJ	Technology	Type	Ref.
10	5	> 4.1		3.6	47	0.18 µm SiGe, BiCMOS	flash	[2]
40	3	2.8	20	3.8	13.6	0.12 µm SiGe	flash	[6]
20	8	4.6	6.6	9	28	0.18 µm, CMOS		[7]
22	5	3.5	7	3	19	0.13 µm SiGe, BiCMOS	flash	[8]
20	3		4.2	2.36	8.5	0.12 µm SiGe	flash	[9]
24	6	3.5	12	1.2	4.4	90 nm, CMOS		[10]
15	4	3	5	0.6*	7.5	0.25 µm SiGe, BiCMOS	flash	This work

* without test buffers

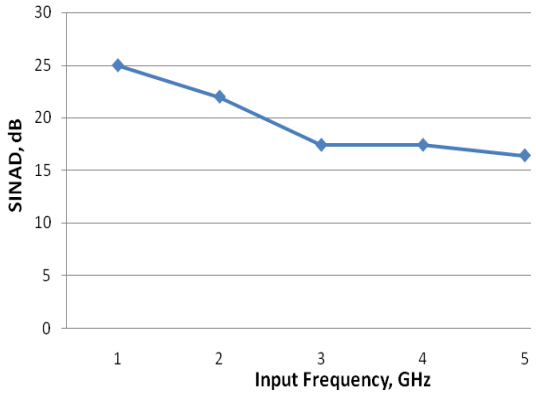

Figure 8. Dynamic performance of the ADC over frequency range up to 5 GHz at 15.01 GS/s sample rate.

A compariosn of this work with similar high-speed ADC designs implemented in different technologies is shown in TABLE I. The present ADC has lowest power dissipation among compatitors and second lowest energy pro conversion step.

The main parameters of the ADC are summarized in the TABLE II.

CONCLUSION

The high speed Analog-to-Digital converter has been designed and fabricated in a low-cost 190 GHz SiGe BiCMOS technology. The ADC is functional up to 15 GSample/s and can be used in UWB system with bandwidth up to 6 GHz.

ACKNOWLEDGMENT

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TABLE II. SUMMARY OF MAIN PARAMETERS OF THE ADC.

Resolution	4 bits
Input range	1 V_{p-p}
Sampling rate	15 GS/s
INL	< 1/2 LSB
DNL	< 1/2 LSB
Non missed code bandwidth	6 GHz
SINAD @ 2 GHz	22 dB
SINAD @ 5 GHz	17 dB
Supply voltage	3 V
Power dissipation:	
Clock buffers	150 mW
Core part	450 mW
Output buffers	400 mW
Chip size	1.5×1.5 mm^2

REFERENCES

[1] B. Razavi, “Principles of Data Conversion System Design”, IEEE Press, New York, 1995.

[2] J. Lee, “A 5-b 10 GSample/s A/D Converter for 10-Gb/s Optical Receivers”, IEEE JSSC, Vol. 39, pp. 1671-1679, 2004.

[3] P. Vorenkamp et al., “Fully Bipolar 120-MSample/s 10-b Circuit”, IEEE JSSC, Vol. 27, pp. 988-992, 1992.

[4] Y. Borokhovych et al. “A 20 GSample/s, 40 mW SiGe HBT Comparator for Ultra-High-Speed ADC”, ECS Meeting, Vol. 3, 2006.

[5] B. Heinemann et al., “Novel Collector Design for High-Speed SiGe:C HBTs“, Proc. IEDM, pp. 775-778, 2002.

[6] W. Cheng, “A 3b 40GS/s ADC-DAC in 0.12 µm SiGe”, ISSCC, 2004.

[7] K. Poulton et al., “A 20GS/s 8b ADC with a 1MB Memory in 0.18 µm CMOS, IEEE ISSCC, 2003.

[8] P. Schvan et al., “A 22GS/s 5b ADC in 0.13µm SiGe BiCMOS”, IEEE ISSCC, 2006.

[9] Y. Yao et al., “A 3-Bit 20GS/s Interleaved Flash Analog-to-Digital Converter in SiGe Technology”, IEEE ASSCC, pp. 420-423, 2007.

[10] P. Schvan et al., “A 24GS/s 6b ADC in 90nm CMOS, IEEE ISSCC, 2008.