Single-Channel, 1.25-GS/s, 6-bit, Loop-Unrolled Asynchronous SAR-ADC in 40nm-CMOS

Tao Jiang[1], Wing Liu[2], Freeman Y. Zhong[2], Charlie Zhong[2], Patrick Y. Chiang[1]

[1] Oregon State University, Corvallis, OR 97331

[2] LSI Corporation, Milpitas, CA 95035

***Abstract*-A single channel, loop-unrolled, asynchronous successive approximation (SAR) ADC fabricated in 40nm CMOS is presented. Compared with a conventional SAR structure that exhibits significant delay in the digital feedback logic, the proposed 6b SAR-ADC employs a different comparator for each bit of conversion, with an asynchronous ripple clock generated after each quantization. With the sample rate limited only by the six delays of the C-DAC settling and comparator quantizations, the 40nm-CMOS SAR-ADC achieves a peak SNDR of 32.9dB and 30.5dB at 1GS/s and 1.25GS/s, respectively, consuming 5.28mW and 6.08mW in a core area less than 170um x 85um.**

I. Introduction

High-speed, medium-resolution, low-power ADCs have a wide range of applications in communication systems such as UWB, mm-wave, serial link transceivers, Ethernet, and digital oscilloscope [1-5].

With continued technology scaling, the Successive Approximation ADC (SAR-ADC) has quickly improved its sample rate to 100-1000 MHz, surpassing its flash counterpart due to its excellent energy efficiency. However, for applications requiring sampling rate exceeding tens of gigahertz, a tradeoff must be made between a large number of cascaded channels of time-interleaved, lower-speed sub-ADCs, or a smaller number of channels with higher-speed sub-ADCs. While lower-speed SAR-ADCs [6] typically achieve better FoM values than their higher-speed counterpart, time-interleaving a large number of sub-ADC requires significant design effort and complexity, such as the multi-phase clock generation/distribution, as well as schemes for compensating the offset, gain and phase skew mismatches between the sub-channels.

On the other hand, achieving a high sampling rate over 1GS/s with 6b conversion is extremely challenging, even with continued CMOS scaling. Most previously reported 6b SAR-ADCs over 1GS/s time-interleave more than two channels [2][4], with the state-of-art fastest single-channel SAR-ADC resolving 5b at 800MS/s [3]. Therefore, a fundamental architectural innovation needs to be developed in order to improve the sample rate of these feedback-limited SAR-ADCs.

A. Conventional SAR-ADC Approach

Fig. 1 shows the conventional SAR ADC architecture. In this structure, the most critical bottleneck to increased sampling rate is the digital logic delay during operation of the successive approximation algorithm. After the comparator quantizes and generates an output, the digital result must be sent into a digital SAR logic first before being sent to the capacitive DAC for settling the charge sharing before the next bit comparison. As pointed out in [2], this logic gate delay can occupy up to 75% of the cycle time, thereby greatly limiting any possibility for future speed improvements.

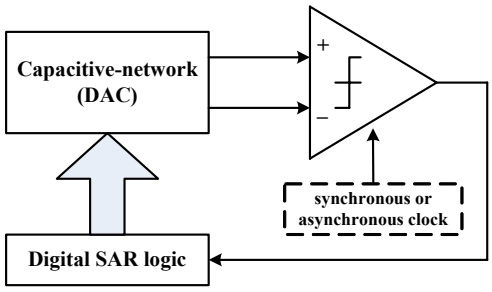


Fig. 1. Conventional SAR ADC structure.

B. Proposed Work: Loop-Unrolled, Asynchronous SAR-ADC

As shown in Fig. 2, the proposed SAR-ADC architecture here features two methods to reduce the conversion time. First, an asynchronous structure [1, 4] takes advantage of the faster comparison cycles, as there will only be one conversion where the input level will occur below 1/2 LSB due to the SAR algorithm. With the global clock *cks* sampling the signal and starting the quantization in the MSB cell, internal comparisons from MSB to LSB will be triggered like dominoes from the outputs of the ready logic.

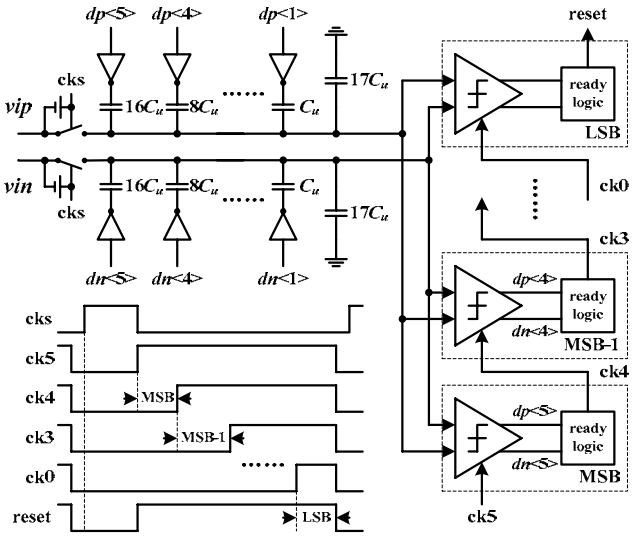


Fig. 2. Proposed loop-unrolled SAR architecture.

978-1-4244-5760-1/10/$26.00 ©2010 IEEE

Second, different from the conventional SAR architecture that uses only one comparator followed by a SAR digital logic for determining the conversion bit, the new architecture uses N comparators for a N-bit conversion, storing the comparison result of each bit within the digital output of each comparator. In this way, no additional digital logic is needed to perform the SAR process, and the comparison result is directly fed back to the capacitor network without any logic gate delay.

One additional benefit of the proposed architecture is that the resolution of the SAR ADC can be easily programmed by disabling the last LSB cell, using *ck0* as the *reset* signal. This programmability may be useful for applications where higher sampling rate is preferred over precision.

In the next several sections, detailed circuits will be introduced along with the measurement results, followed by the conclusion.

II. Circuit Implementation

A. Capacitive DAC and bootstrapped switch

A normal capacitive DAC is employed, except for a minor change that the capacitor directly connected to ground is made $17C_u$ rather than C_u. In this way, the reference voltage is made 1.5 times of full scale, and will accelerate the settling speed of DAC. Considering the parasitics contributed by comparators' ΔC, the real reference voltage should be trimmed to be

$$V_{ref} = 1.5 \cdot V_F \cdot \left(1 + \Delta C / 48C_u\right) \quad (1)$$

Bootstrapped switches [7] are employed (Fig. 3) in the sampling circuit in order to achieve both smaller on-resistance and minimal signal-dependent sampling distortion. The circuit is carefully designed so that the voltages between all transistor terminals are below 1V.

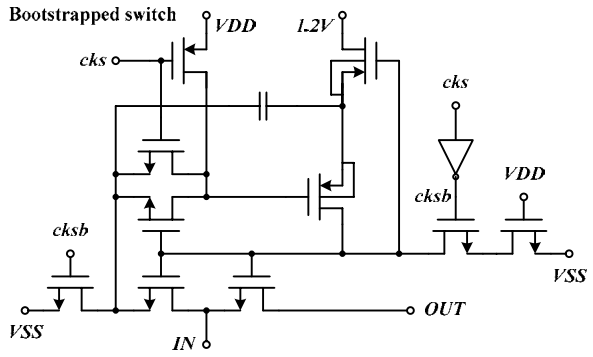


Fig. 3. Bootstrapped switch used in capacitive DAC.

B. Comparator design and offset cancellation scheme

Six simple StrongARM comparators (Fig. 4) are used for the entire 6-bit quantization. Clocked by the ready signal from the preceding conversion, each comparator evaluates the input signal and sends its output directly to the capacitive DAC, maintaining its digital output until it is reset at the end of the 6b conversion. Because each comparator quantizes only once per clock period, the total power consumption of the six comparators does not exceed that of a conventional architecture where one comparator evaluates six times every conversion period.

Unlike the conventional structure where only one comparator is used, each of the six comparators will exhibit a different mismatch such that the offset is no longer a systematic error that can be subtracted during the post signal processing. Therefore, offset cancellation of each comparator is performed where an off-die offset cancellation circuit composed of two sets of 7-bit binary current sources is used. Monte Carlo simulations show a reduction in 3s offset below 0.5LSB (15mV).

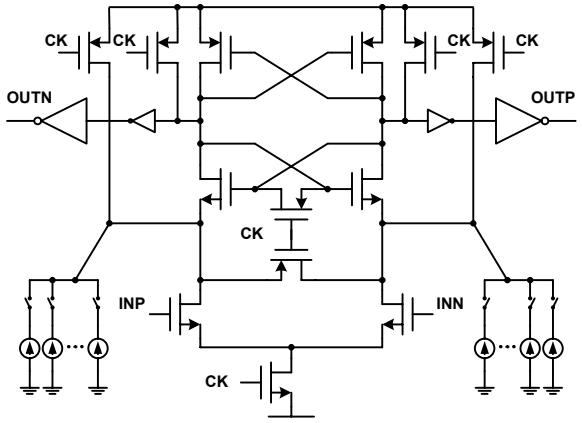
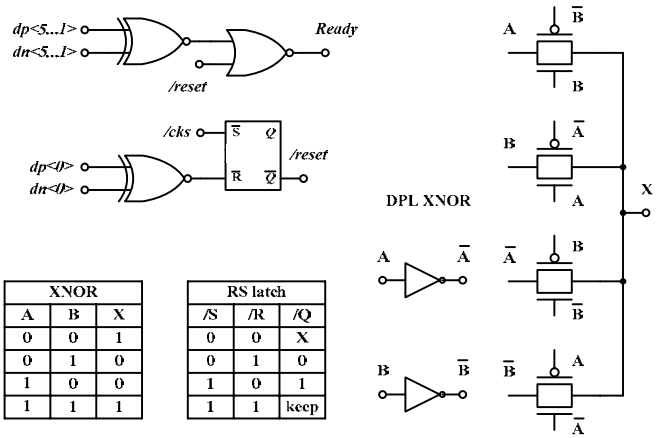


Fig. 4. Comparator design with current steering offset cancellation circuit.

C. Ready signal logic

As can be seen from Fig. 2, each of the six comparators is followed by a logic circuit that determines if the current quantization is complete, followed by generation of an asynchronous clock to trigger the next quantization. The comparator in the first MSB cell is triggered by the falling edge of the sampling clock, while the other five comparators are triggered by the ready signals from each preceding cell. The comparator in the LSB cell generates a ready signal that is used to reset all of the six comparators, shorting the bottom plates of the capacitors in the capacitor network to ground during the next sampling phase.



XNOR		
A	B	X
0	0	1
0	1	0
1	0	0
1	1	1

RS latch		
/S	/R	/Q
0	0	X
0	1	0
1	0	1
1	1	keep

Fig. 5. Ready signal generated logic and DPL XNOR circuit.

Since the comparator is precharged to supply every reset interval, its output can only be changed from "HH" to "HL" or

"LH". In a time-constrained system such as a high-speed ADC, a NAND gate for the ready logic might be preferred due to its single stage delay. However, the NAND must be carefully designed in order to prevent it from making a wrong decision – for example, if the comparator meets metastability and its differential outputs result in "LL". On the other hand, while a XOR gate is more robust as it will not evaluate with the "LL" situation, it suffers from relatively long delay. DPL (double pass-transistor logic) circuit is employed here to reduce the gate delay while always making the correct decision. The final ready logic is designed according to De Morgan's law and shown in Fig. 5. After the first five MSB cells, each ready signals will be reset by the ready signal of the final LSB cell, signifying that 6b conversion is complete and the comparators need to be precharged.

D. Metastability detector

Metastability will occur when the input signal level is so small that the comparator takes an excessive amount of time to complete a quantization. The probability for encountering metastability is even greater for high sample rates, since less time is available for the quantizer's positive feedback to regenerate to full digital level. Hence, a metastability detector is designed to detect its occurrence, stop the current conversion, and force the remaining quantizers' outputs to a digital "1" followed by all digital "0"s.

In the circuit shown in Fig. 6, a delay signal starting from the input clock *ck_in* is deliberately generated, with its delay time comparable with that of the delay path through the comparator and the ready logic. Signals *ck_out* and *ck_delay* are sensed by the D flip-flop as the data and clock, and the output /Q of the D flip-flop is used as a local reset signal that is responsible for stopping the current conversion and setting forced values for the remaining bits. If the comparator is not metastable and generates an asynchronous clock, the length of the delay in the comparator-ready-logic path will be shorter. Then the signal *ck_out* will toggle to "1" when the sampling phase of the D flip-flop *ck_delay* comes and the conversion will not be interrupted. In contrast, if the comparator becomes metastable, the signal *lclrst* will toggle to "1" and the conversion will be stopped.

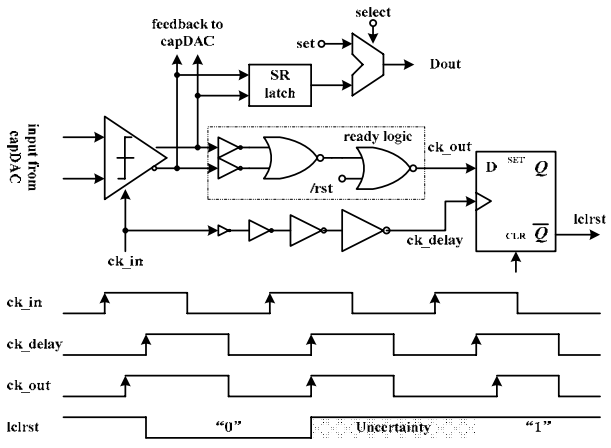


Fig. 6. Metastability detection circuit and its working process.

III. Measurement Results

The SAR ADC is fabricated in a 1V, 40nm CMOS process, with the die shown in Fig. 7. The total active area is only 170μm by 85μm, with a total die size of 1.8mm by 1.5mm.

The measurements are performed with different supplies across varying sampling rates in order to explore the chip's maximum performance. Least mean square (LMS) calibration [1] is performed by injecting a slow ramp signal into the converter, using the output code to determine the bit weights that best correspond to the known input. Because all six comparators connect to the output of the capacitive DAC, the large gate capacitances all contribute as parasitic, making the distortion and non-linearity of this ADC larger than a conventional structure. LMS calibration helps improve the performance considerably, as observed in Fig. 8, where the SNDR is improved by 2.7dB at 1GS/s sampling rate.

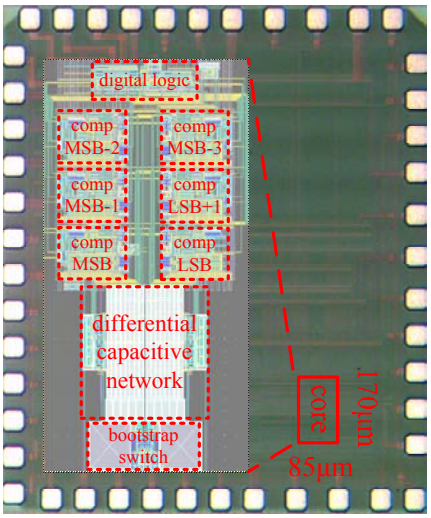


Fig. 7. Chip die photo and core circuit layout.

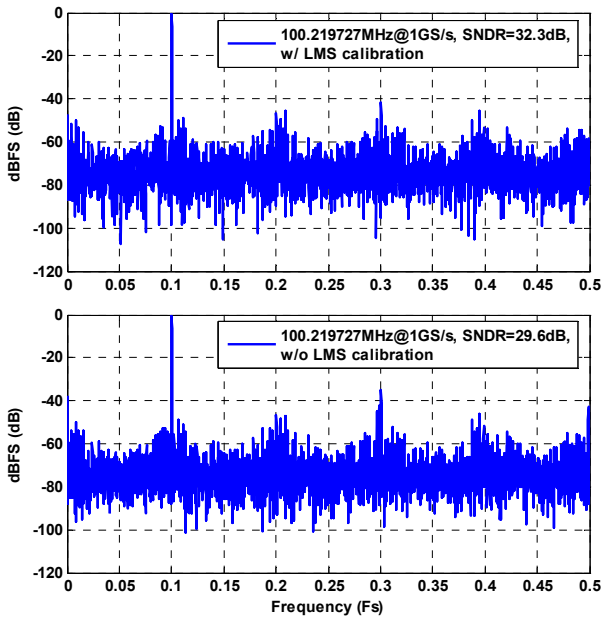


Fig. 8. ADC output spectra with and without LMS calibration.

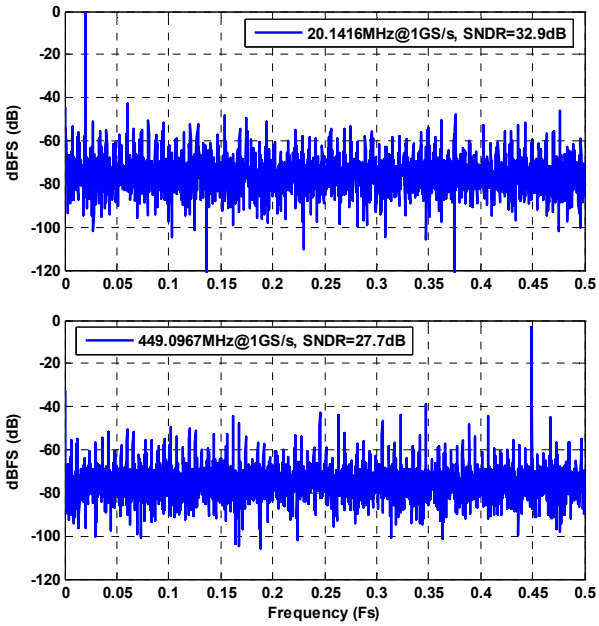


Fig. 9. ADC output spectra with different input frequencies with 1GS/s rate.

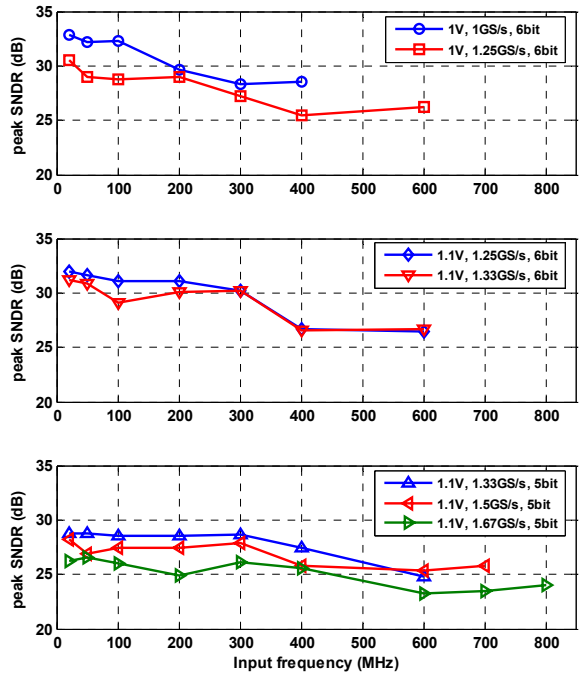


Fig.10. Measured SNDR versus input frequency for ADC under different supplies, sampling rate, and number of bits.

The SAR-ADC operates at 1GS/s with a 1V supply, consuming 1.25mW, 2.76mW and 1.15mW in the analog comparators, digital logic and internal clock driver, and the capacitive DAC, respectively. The ADC output spectra with different input frequencies is shown in Fig. 9, indicating a peak SNDR of 32.9dB, resulting in a general FoM of 148fJ/conversion-step. When the sampling rate is increased to 1.25GS/s, the peak SNDR is 30.5dB, with a total power consumption is 6.08mW. While capacitive parasitics contribute to the SNDR losses at low frequency, the ability to reduce to 5b conversion enables operation well above 1.5GHz at Vdd=1.1V.

Measurement results are summarized in Table I, along with a performance comparison versus recent SAR-ADC designs.

TABLE I
COMPARISON WITH PREVIOUS WORKS

	[1]	[2]	[3]	[4]	This work			
Technology (nm)	130	130	65	65	40			
Area (mm^2)	0.12	0.09	0.018	0.11	0.014			
Resolution (bit)	6	6	5	6	5 or 6 Programmable			
Channel #	2	2	1	2	1			
Sample rate (GS/s)	0.6	1.25	0.8	1	1	1.25	1.25	1.33
Peak SNDR (dB)	34	34.9	28.2	31.5	32.9	30.5	31.8	31.3
FoM (fJ/conv)	220	-	116	210	148	178	183	188
Supply (V)	1.2	1.2	1	-	1	1	1.1	1.1
Power (mW)	5.3	32	1.97	6.7	5.28	6.08	7.26	7.52

IV. CONCLUSION

A novel loop-unrolled SAR architecture is proposed. With the comparator outputs directly fed back to the capacitive DAC, the digital FSM logic delay is eliminated, thereby greatly increasing the sample rate. Fabricated in a 40nm CMOS process, the ADC achieves a sampling rate over 1.25GS/s for a single channel, 56% faster than the previous fastest single-channel SAR-ADC [3].

REFERENCES

[1] S.-W. M. Chen and R. W. Brodersen, "A 6-bit 600-MS/s 5.3mW asynchronous ADC in 0.13-µm CMOS," *IEEE JSSC*, vol. 41, no. 12, pp. 2669-2680, Dec 2006.

[2] Z. Cao, S. Yan and Y. Li, "A 32mW 1.25GS/s 6b 2b/step SAR ADC in 0.13µm CMOS," *IEEE JSSC*, vol. 44, no. 3, pp. 862-873, Mar 2009.

[3] Y.-Z. Liu, S.-J. Chang, Y.-T. Liu, C.-C. Liu and G.-Y. Huang, "A 5b 800MS/s 2mW asynchronous binary-search ADC in 65nm CMOS," *ISSCC Dig. of Tech. Papers*, pp. 80-81, Feb 2009.

[4] J. Yang, T. L. Naing and B. Brodersen, "A 1-GS/s 6-bit 6.7-mW ADC in 65nm CMOS," *CICC* 2009, pp. 287-290.

[5] Y. M. Greshishchev, et. al., "A 40GS/s 6b ADC in 65nm CMOS", *ISSCC Dig. of Tech. Papers*, pp. 390-391, Feb 2010.

[6] C.-C. Liu, et. al., "A 10b 100MS/s 1.13mW SAR ADC with binary-scaled error compensation," *ISSCC Dig. of Tech. Papers*, pp. 386-387, Feb 2010.

[7] M. Dessouky and A. Kaiser, "Very low-voltage digital-audio ΔΣ modulator with 88-dB dynamic range using local switch bootstrapping," *IEEE JSSC*, vol. 36, no. 3, pp. 349-355, Mar. 2001.