Track-and-Hold and Comparator for a 12.5GS/s, 8bit ADC

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***Abstract*— This paper discusses the design and characterization of a track-and-hold amplifier (THA) and a comparator which are the essential building blocks of an 8bit, 12.5GS/s folding-interpolating analog to digital converter (ADC) with a 3GHz bandwidth. The circuits are implemented in a 0.25µm, 190GHz SiGe BiCMOS process. The THA occupies an area of 0.5mm^2. It features a SNDR of 47dB or 7.5bits ENOB for a 3GHz bandwidth, a hold time of 21ps with a droop rate of 11mV/80ps and a power dissipation of 230mW from a 3.3V supply. The comparator occupies an area of 0.38mm^2 and exhibits an input sensitivity of ±2mV, an input offset voltage of 1.5mV, latch and recovery times of 19 and 21ps respectively and a power dissipation of 150mW from a 3.3V supply.**

I. INTRODUCTION

High speed-medium resolution ADC converters are key building blocks in the next-generation of satellite communication receivers. Several mixing stages are typically used to down-convert the satellite RF signal to the IF band which is then digitized through a medium bandwidth ADC. The multiple down conversion is predicted by the limited bandwidth of the ADC. If a wide-bandwidth ADC is available, a single down conversion can be used and a 64QAM RF signal in the 10-30GHz band can be down-converted to 1-3GHz and digitized through an 8bit, 3GHz ADC. This improves the linearity of the receiver significantly. The sampling frequency F_s in the ADC must be higher than the Nyquist rate in order to compensate the performance degradation of the ADC near the Nyquist bandwidth ($F_s/2$) [1]. In the present case, a sampling frequency F_s=12.5GS/s was selected.

Current state of the art CMOS technologies cannot meet the required performance specifications of the ADC due to their inherent limited supply voltage and small dynamic range. The selected technology for the ADC implementation is a 0.25µm 190GHz, 5 metallization layers 3.3V SiGe BiCMOS process from IHP Microelectronics [2].

The architecture selected for the implementation of the ADC is a folding-interpolating topology [1]. This architecture was selected because for 8-bit resolution, it provides an optimum trade-off between high-speed and power dissipation as compared to other high-speed ADC architectures. The overall ADC system architecture is shown in Fig.1. It uses a fully differential architecture to maximize the swing and minimize common-mode noise. In this architecture, the output of the THA circuit is applied to the input of the several folding amplifiers where it is compared to the reference voltages generated by the resistor ladder. Analog processing is used by each folding amplifier to transform the input signal into a repetitive triangular-shaped output signal. The differential outputs of the folding amplifiers are then applied to a set of interpolating resistors located between the folding amplifiers and the comparators. The outputs of the interpolating resistors are finally applied to a set of comparators to translate the analog information into digital data. Finally a digital encoder with bubble error correction is used to obtain the LSB bits. A coarse quantizer along with bit synchronization is used in parallel with the folding interpolation to generate the two additional MSB bits. The relationship between the resolution of the converter (N), the folding factor (F), the number of folding amplifiers (NF) and the interpolation rate (IR) is given by the following equation [1]

$$2^N = F \times NF \times IR \qquad (1)$$

For the 8-bit converter considered in this work, realistic choices for the NF, F and IR are 4, 8 and 8, respectively.

The two most critical blocks in the folding-interpolating ADC are the THA and the comparator. The THA circumvents the degradation of the SNDR due to clock jitter or skew caused by signal-dependent delays [3]. It also helps to relax the bandwidth limitations caused by the frequency multiplication effect of folding and maintains the accuracy of the ADC at high-speed [1]. The output signal swing of THA must be maximized since it determines the LSB of the ADC. To achieve an LSB of at least ±2mV, the THA must provide an output voltage range of ±0.5V over its full bandwidth. Furthermore, the hold time of the THA must also be maximized and the THA must operate at 12.5GS/s, with a bandwidth of 3GHz.

The comparators are also critical in the implementation of the folding-interpolating ADC. Not only do they represent the link between the analog and digital domain but they also play a significant role in the overall sampling rate and resolution of the ADC. Individual comparators must be able to detect and compare a 3GHz input signal with a sensitivity of ±2mV (defined by THA) at a sampling speed of 12.5GS/s. This requires the input-offset voltage to be below ±2mV to ensure 8-bit resolution for the ±0.5V output swing provided by the THA. The power

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dissipation must also be minimized as the proposed ADC system includes of 38 comparators.

To verify the feasibility of the overall ADC at the target specifications, these two critical blocks were implemented and fully characterized. Details of the circuit design and experimental results are presented in the following section.

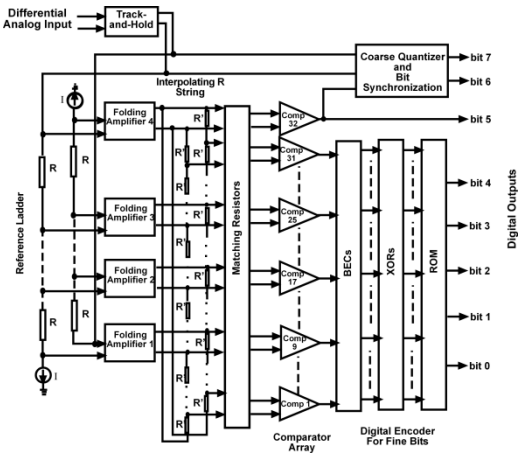


Fig. 1: Folding Interpolating ADC Architecture

II. CIRCUIT DESIGN AND IMPLEMENTATION

A. Track-and-Hold Amplifier

The circuit diagram of the THA is given in Fig. 2. An open loop architecture was used in the implementation of the THA to enhance its sampling rate. The circuit consists of an input buffer, sampling switches, output buffers and tapered output buffer. The differential input signal is applied to the bases of transistors Q_1 and Q_2.The outputs of the input buffer go to the track-and-hold switches. Each track-and-hold switch consists of three transistors Q_3,Q_4,Q_5 (or Q_6,Q_7,Q_8), a current source (I_2) and a hold capacitor C_H. During the track mode, the tail current I_2 is switched through Q_4 (or Q_7), and Q_5 (or Q_8). During that time, transistor Q_5 (or Q_8) acts as an emitter follower. As a result, the switch is conducting and the output voltage of the switch depends linearly on the input voltage. During the hold mode, the tail current of the switching transistor Q_5 (or Q_8) is switched off. Transistor Q_5 (or Q_8) does not conduct and C_H holds its previous voltage. Transistors Q_9-Q_{13} act as output buffers.

To achieve an LSB of at least ±2mV, the THA must provide a wide dynamic swing of ±0.5V over its full bandwidth. This is accomplished by biasing the transistors in the midpoint of the active region of the SiGe HBT to ensure linearity is maximized. High signal swing is also achieved by using a fully differential design while tapered output buffers ensure an adequate driving capability while achieving a high output swing.

In this differential architecture, only the difference between the outputs of the THA is important, resulting in a higher dynamic swing as well as a significant improvement in the pedestal error and droop rate over the single ended case. The feedforward capacitor C_{FF} is added between the input stage and the hold mode capacitor C_H [5] to reduce the hold mode feedthrough. At high-frequency, the hold mode feedthrough is approximately determined by the ratio of the base emitter capacitance C_{be} of Q_5 (or Q_8) and the hold capacitor C_H and is given by [5]

$$\text{Feedthrough Ratio} \approx \frac{C_{be5}}{C_H} \qquad (2)$$

The hold mode feedthrough can be reduced by adding cross-coupled compensation capacitors C_{FF} between the hold capacitors at the emitter of Q_5 (or Q_8) and the collector of Q_1 (or Q_2) [1, 5, 6], as illustrated in Fig. 2. As a result the hold mode feedthrough ratio is now given by [5]

$$\text{Feedthrough Ratio} \approx \frac{C_{be5}}{C_H} \times \left(1 - \frac{C_{FF}}{C_{be5}}\right) \qquad (3)$$

Complete feedthrough cancellation is obtained when C_{FF} is equal to the base emitter capacitance of Q_5 (or Q_8).

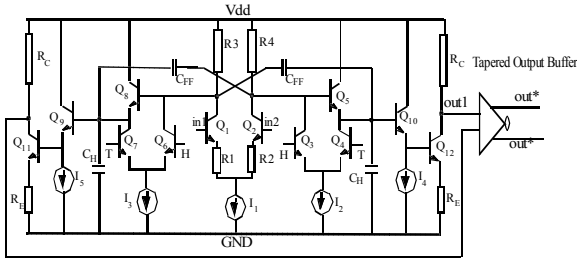


Fig. 2: Track-and-Hold Amplifier Circuit

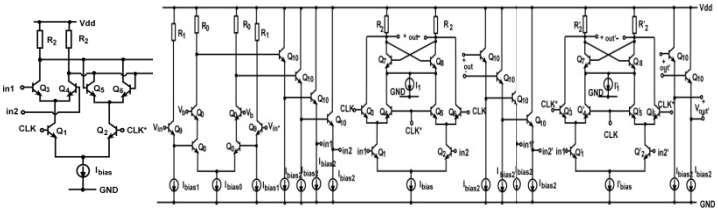
In order to maximize the hold-time of the THA, the acquisition time must be minimized. This is accomplished by biasing the transistors of the switching stage at peak f_T current density. The speed is further maximized by sizing the hold capacitor C_H, as a compromise between bandwidth and droop rate to obtain 8-bit resolution at the highest possible speed. The hold capacitor is made small enough such that the THA operates at 12.5GS/s, but large enough such that it has a droop rate that is adequate for 8-bit resolution.

B. Comparator

The circuit diagram of the basic comparator is shown in Fig. 3a. In this design, the input and clocking transistors are switched to improve the isolation between the digital output and the analog input, thus minimizing the kickback effect. The overall speed of the comparator is increased by introducing the current source I_1 at the emitters of Q_7-Q_8, This will increase the delay in decision-making of the latch comparator when the latch command is initiated. At maximum clock rate, the base emitter junction charging times of Q_7-Q_8 limit the maximum speed of the comparator. The addition of this current source allows transistors Q_7-Q_8 to remain partially "on" during the track phase of the comparatorA pre-amplifier preceding the comparator can be used to ensure that the output of the comparator is large enough to avoid metastability. The pre-amplifier also improves the accuracy of the comparator as it helps prevent kickback that would otherwise corrupt the input signal. Lastly, power dissipation is minimized by biasing the transistors for the comparator at half peak f_T current density.

The complete comparator circuit used is shown in Figure 3b. It consists of a pre-amplifier and two cascaded differential comparators in a master-slave configuration [7]. The pre-amplifier is designed in a cascode configuration to achieve the required gain and bandwidth and includes an input buffer (Q_9)

to achieve the proper DC bias through level shifting. The master-slave comparators are identical and driven by complementary clocks. When the master comparator goes into track mode, the slave comparator is in latch mode and holds its digital value. Alternatively, when the master comparator goes into latch mode, the slave comparator is in track mode and tracks the latched signal of the master comparator [7]. This ensures that a fully digital output is obtained at the output of the comparator. Buffers (emitter followers Q_{10}) are used to level shift the signals between the master and slave comparators and the pre-amplifier.



(a) (b)

Fig. 3: (a) Basic Comparator Circuit, (b) 12.5GHz Master-Slave Comparator Circuit

III. IMPLEMENTATION AND EXPERIMENTAL RESULTS

The micrograph of the THA is shown in Fig. 4. The circuit occupies an area of 0.54mm^2 including bond pads.

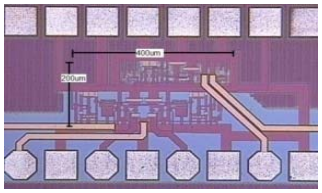


Fig. 4: Micrograph of THA

The differential output voltage of the THA is shown in Fig. 5 for an input frequency F_{in} of 3GHz and a sampling frequency F_s of 12.5GS/s. The circuit exhibits a droop rate of 11mV/80ps, a pedestal error of less than 4mV and a hold time of 21ps.The resulting single ended frequency spectrum is illustrated in Fig. 6. The circuit exhibits a SNDR and a resolution of 47dB and 7.5bits, respectively. The SNDR was calculated based on a frequency window of $F_s/2$. The even harmonic at 6 GHz was ignored since it cancels out when the circuit is connected differentially. The complete simulated and experimental characteristics of the THA for an input frequency of 3GHz and a 12.5GS/s sinusoidal clock are listed in Table 1. The experimental results are in good agreement with simulations and indicate that the THA meets the required ADC specifications. The results obtained for the present THA were also compared to previously reported 8-bit, GS/s sampling rate THAs implemented in SiGe HBT technology. This comparison is provided in Table 2. Included in the comparison is the figure of merit (FOM) for the THA defined as

$$\mathrm{FOM} = \frac{P_{diss}}{2 \times \mathrm{ERBW} \times 2^{\mathrm{ENOB}}} \qquad (4)$$

where P_{diss} is the total power dissipation of the ADC, ENOB is the effective number of bits at the effective resolution bandwidth ERBW. The present THA design achieves a FOM of 0.21pJ/conversion, which is the best reported to date for 8-bit SiGe THAs.

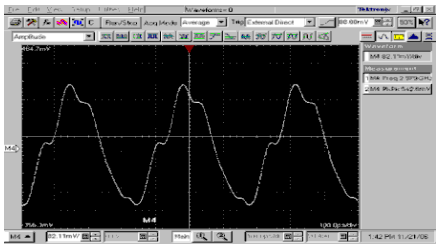


Fig. 5: Differential Output of THA at F_{in}=3GHz and F_s=12.5GS/s

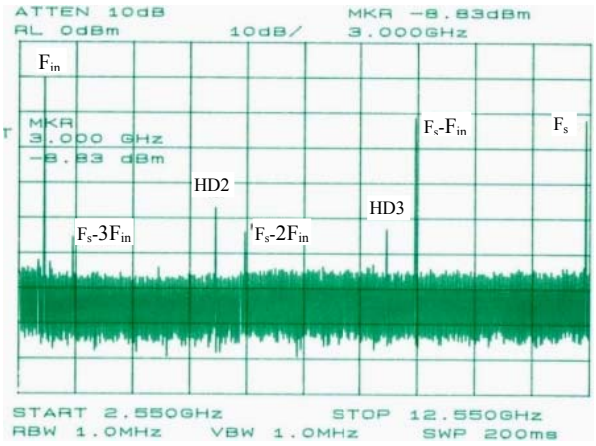


Fig. 6: Frequency Spectrum of the Single Ended Output of THA at F_{in}=3GHz, F_s=12.5GS/s

Table 1: Experimental Characteristics of THA

Parameter	Post Layout (Sine Wave Clock)	Experimental (Sine Wave Clock)
Supply Voltage	3.3V	3.3V
Sampling Rate	12.5GS/s	12.5GS/s
SNDR@ Fin=3.0GHz	48.0dB	47dB
ERBW	3.5GHz	3.0GHz
ENOB@ Fin=3.0GHz	7.7bits	7.5bits
Output Swing	1.01V peak-peak	1V peak-peak
Hold Time	23ps	21ps
Droop Rate	9.01mV/80ps	11mV/80ps
Pedestal Error	2.7mV	<4mV
Hold mode Feedthrough	-51.1dB	Negligible
P_{diss}*	0.21W	0.23W
Die Size	0.54 mm^2	0.54 mm^2

*Excluding the tapered output buffers

Table 2: Comparison of SiGe 8-bit, GS/s THAs

	SiGe Process	Supply Voltage [V]	F_s [GHz]	ERBW [GHz]	ENOB [bit] @ F_{in}=ERBW	P_{diss} [W]	Chip Area [mm^2]	FOM [pJ/conversion]
Vessal [1]	0.5µm f_t=47GHz	3.3	2.0	0.9	8.0	0.55	1.4	1.19
Li [8]	0.25µm f_t=200GHz	3.5	12.1	5.5	7.4	0.70	1.2	0.38
This Work	0.25µm f_t=190GHz	3.3	12.5	3.0	7.5	0.23	0.5	0.21

The micrograph of the comparator is shown in Fig. 7. The circuit occupies an area of 0.38mm^2 including bond pads. The differential output waveforms of the comparator are shown in Fig. 8. The results indicate that the comparator can detect a ±2mV sinusoidal input signal of 3.125GHz and a sinusoidal clock signal of 12.5GS/s. The measured charge, latch and recovery times of the comparator are 7.2ps, 19ps and 21ps, respectively. The comparator circuit dissipates only 150mW power from a 3.3V supply. The complete simulated and experimental characteristics of the comparator for a sinusoidal clock are listed in Table 3. The experimental results are in agreement with simulations and confirm that the comparator meets the required ADC specifications. A comparison to other high-speed stand-alone comparators, operating at similar sampling frequencies, is provided in Table 4 and indicates that the implemented comparator provides low power dissipation, a high resolution and low chip area.

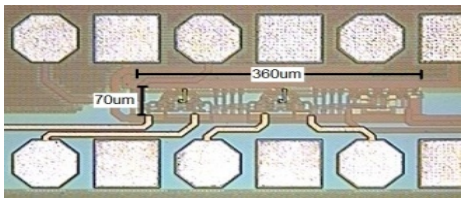


Fig. 7: Micrograph of Comparator

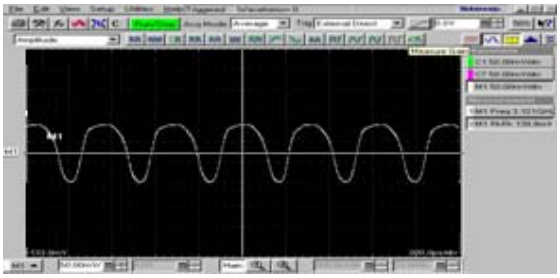


Fig. 8: Comparator Waveform for F_{in}=3.125GHz and F_s=12.5S/s (Input of ±2mV)

Table 3: Experimental Characteristics of the Comparator

Parameter	Post Layout (Sine Wave Clock)	Experimental (Sine Wave Clock)
Supply Voltage	3.3V	3.3V
Input Offset	<1.5mV	2-3mV
Sampling Rate	12.5GS/s	12.5GS/s
Input Frequency	3.125GHz	3.125GHz
Input Sensitivity	±2mV	±2mV
Charge Time	6ps	7.2ps
Latch Time (10%-90%)	16ps	19ps
Recovery Time (10%-90%)	16ps	21ps
P_{diss}	0.14W	0.15W
Chip Area	0.38 mm^2	0.38 mm^2

IV. Conclusion

The THA and the comparator, as the most critical building blocks that affect the overall performance of the ADC, were implemented experimentally and fully characterized to verify the feasibility of the overall ADC. The THA exhibits the required 8-bit resolution, an ENOB of 7.5bits and an ERBW of 3GHz at a sampling speed of 12.5GS/s with an excellent FOM as compared to previously reported designs. The comparator detects and compares a 3.125GHz input signal with a sensitivity of ±2mV (±0.5LSB) at a sampling speed of 12.5GS/s. The experimental results confirm that the characterization of both circuits are in good agreement with simulation and meet the expected specifications and can be used as key building blocks in the final implementation of the ADC.

Table 4: Comparison of SiGe, GS/s Comparators

References	SiGe Process	Supply Voltage [V]	Maximum F_s [GHz]	Input Sensitivity@ Input/Clock [GHz/GS/s]	P_{diss} [W]	Chip Area [mm^2]
Vessal [1] (simulation)	0.5µm f_t=47GHz	3.3	2	±2mV [0.2/2.0]	0.6	N/A
Borokhovych [9]	0.25µm f_t=200GHz	3.5	32	±18.5mV [5.0/32.0]	0.4	1.9
Li [10]	0.18µm f_t=120GHz	3.5	20	±4.45mV [3.0/18.0]	0.08	1.8
Jensen [4]	0.5µm f_t=55GHz	3.3	16	N/A	0.22	N/A
This Work	0.25µm f_t=190GHz	3.3	12.5	±2mV [3.125/12.5]	0.15	0.38

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