# A 6-Bit, 1.2-GS/s Dual Channel ADC in 0.13-µm CMOS for MB-OFDM UWB Receivers

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***Abstract*—This paper presents a 6-bit, 1.2-GSample/s flash ADC for MB-OFDM UWB receivers fabricated in TSMC 0.13-µm CMOS 1P8M process. Using a dedicated track-and-hold amplifier (THA) at front, it can eliminate different paths skew between comparators and clock jitter degradation to the comparators. Moreover, the proposed converter is designed with averaging and interpolation technique so that the offset of the preamplifiers and comparators, and power consumption can be reduced. A reference generator generating reference voltage for preamplifiers array also has been included in this design. It can track the common mode voltage between THA and resistor ladder center tap.**

**Operating at 1.2-GS/s both the I/Q channel ADC achieves an effective resolution bandwidth (ERBW) of 450-MHz, and greater than 5-bits effective number of bits (ENOB) at 350-MHz of input frequency. The peak DNL and INL are measured as 0.39-LSB and 1-LSB, respectively. A single channel ADC consumes about 84-mW including internal reference at 1.2-V supply. The test chip single channel occupies 1.45x0.78-mm$^2$ of active area.**

***Index Terms*—Analog-to-digital converter (ADC), multiband orthogonal frequency division multiplexing (MB-OFDM), Ultra-wideband (UWB), flash converter, CMOS analog integrated circuits, averaging and interpolation.**

## I. Introduction

High speed and medium to moderate (i.e. 4-7 bits) resolution analog-to-digital converters (ADCs) are commonly been used in read-write channel of a hard disk drive system, Gigabit Ethernet, and wireless receivers. ADC usually is the dominant power hungry block for the whole analog front-end, thus reducing its power consumption is very important for many handheld wireless applications including UWB system. Recently, a lot of effort has been put to reduce the ADC power consumption, e.g. a time-interleaving SAR array [1], a pipelined ADC [2], low power flash with capacitor averaging and interpolation [3] and two-step subranging with time interleaving [4].

This paper presents an I/Q channel 6-bit, 1.2-GS/s flash ADC using 0.13-um CMOS process with resistor averaging and interpolation techniques to reduce the ADC total power consumption. Both channels can achieve an ENOB greater than 5-bits with an input bandwidth of 350-MHz and each channel consumes 84-mW, which fulfills the requirement it needed for a MB-OFDM UWB system [5].

## II. ADC Architecture

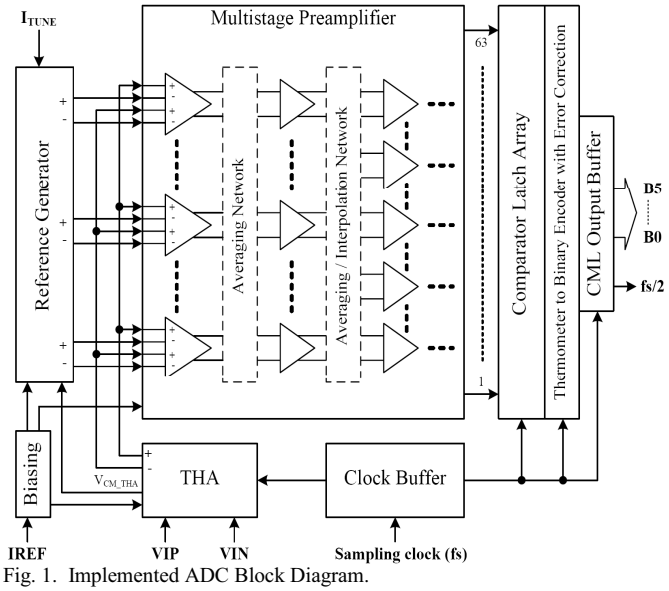


Fig. 1. Implemented ADC Block Diagram.

The flash architecture shown in figure 1 consists both analog and digital circuits blocks. Analog blocks include a dedicated THA, an on-chip reference generator, multistage preamplifiers and biasing circuits. THA tracks and holds the input differential signal to become a DC level for the first stage preamplifiers. The advantage of a dedicated THA is to eliminate different paths skew between comparators and clock jitter degradation to the comparators. Multistage preamplifiers are necessary to provide enough gain for the small least significant bit (LSB) level to overcome comparator static and dynamic offset. Using averaging [6], [7] and interpolation [8], [9] techniques reduces the offset contributed by the preamplifiers and reduce their power consumption. On-chip reference generator provides all the reference signal levels. Biasing circuits provide the mirrored tail current for preamplifier, THA, and reference generator.

Digital blocks consist of clock buffer, comparator latch array and encoder. Clock buffer provides the timing for the digital and analog blocks. The comparator latch regenerates the amplified signal by the preamplifiers and provides it to the SR latch. Logic circuits based encoder instead of ROM is used to convert thermometer code to Gray code, which has intrinsic bubble error correction properties [10]. Current mode logic (CML) based output buffer provides low swing differential

output signals to drive the output pads and parasitic transmission lines on the PCB to reduce noise coupling to the ADC core.

## III. Implemented Design

### A. Pseudo differential track-and-hold amplifier

Figure 2 shows the pseudo differential THA schematic. Voltage buffer has been added before THA to remove the wire bonding effect. It is solely for measurement purpose, thus its power has been excluded from the total power. Simple NMOS switch M1 with low-Vt in deep n-well to remove body effect with a holding cap of 0.8-pF is designed to have track and hold function. After this switch cap, a simple PMOS buffer to drive the first stage preamplifiers has been purposed. Since the ADC resolution is only 6-bits, no bootstrap switch technique is needed. Due to the low supply voltage (1.2-V), the input signal swing cannot be too high to insure decent linearity in the THA. In our design, we used peak-to-peak differential input range of 0.4-V, while the input common mode is 0.32-V. THA consumes 4-mA, with $f_{-3db}$ greater than 1.8-GHz according to post-simulation results.

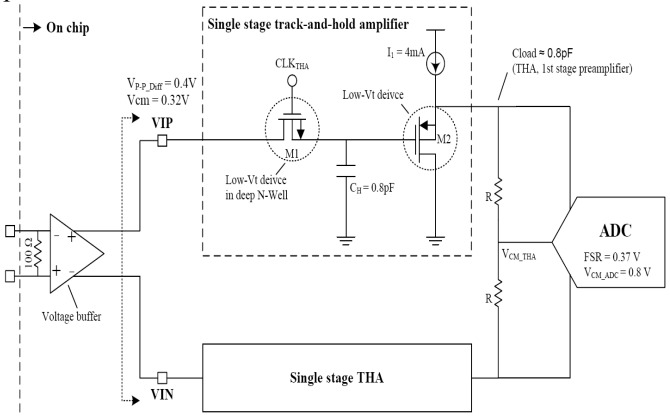


Fig. 2. Pseudo differential THA schematic.

### B. Reference generator with common mode tracking

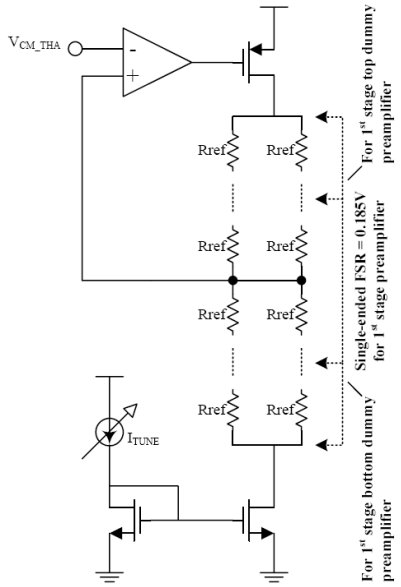


Fig. 3. Reference generator schematic.

Figure 3 shows the on-chip reference generation schematic. It is needed to remove THA and resistor ladder DC common mode offset caused by temperature, process and voltage supply variations. The circuits consist of a two-stage operational transconductance amplifier (OTA), resistor ladder and a variable current mirror source to insure constant reference voltage for all corners. Two inputs of the OTA are from the center taps of the resistor ladders and the output common mode of the THA. Two rows of resistor ladders are design for better layout routing, which is important for high speed dynamic performance.

### C. Multistage Preamplifier stages

Since the overall preamplifiers bandwidth should be greater than the maximum sampling frequency, the gain of each preamplifier has been designed to be around 2. Comparator offset consisting of static and dynamic offset is estimated to be at 50-mV. Thus four stages preamplifiers shown in figure 4 were designed to have a total gain around 18, which makes the input referred offset to be less than 0.5-LSB. One LSB in this design is 5.8-mV. Comparator kickback noise to the reference ladder is negligible because multistage of preamplifiers are used. Since averaging is used to reduce the offset contributed by preamplifiers, dummy preamplifiers have to be deployed to remove the boundary effect. The numbers of dummy preamplifiers are optimized using the spatial filter theory developed in [7]. Because resistor-averaging technique is used in this design, interpolation is a by-product of this technique. Using interpolation can reduce the number of preamplifiers and the loading of the THA output buffer, thus reduce the analog power consumption. Total interpolation by 8 with each stage by 2 except for the first stage is chosen to have the best speed to power ratio.

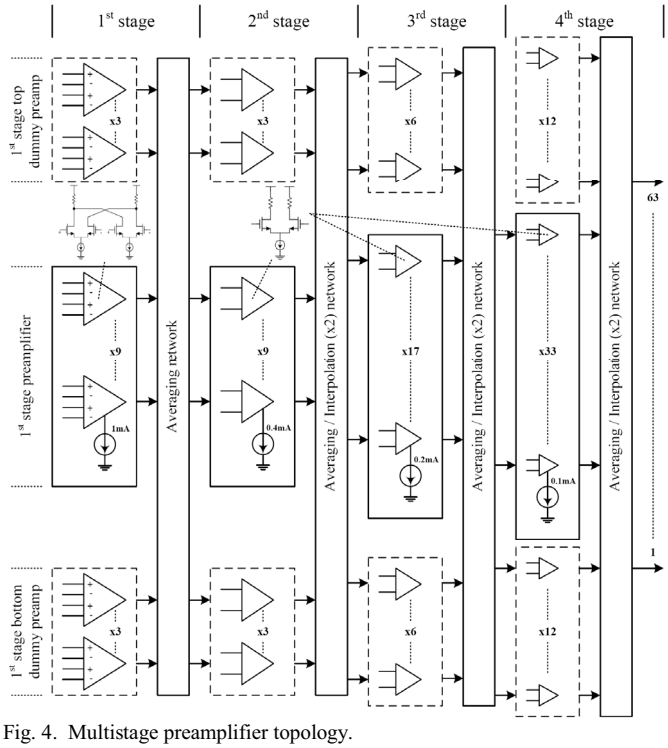


Fig. 4. Multistage preamplifier topology.

### D. Digital circuits

The comparator circuit based on [11] is shown in figure 5. Dynamic latch is chosen to reduce power, while introducing dynamic offset, which can be removed by preamplifier. When $CLK_{CMP}$ is low, the output is precharge to supply voltage to remove memory effect. The comparator latch is fast enough using 0.13-µm CMOS, thus it is no need to reset to mid level. Q and Qbar of the SR latch will keep its previous value during precharge. When $CLK_{CMP}$ is high, the two outputs will go down initially. If $V_{INP}$ is greater than $V_{INN}$, then $V_{ON}$ will drop faster than $V_{OP}$. Once $V_{ON}$ hits one threshold voltage below, M8 will turn on and the latch will start to regenerate. Given enough time, Vop will go to supply voltage and Von will go to almost ground. True single phase clock (TSPC) based D flip-flop (DFF) was designed. The overall ADC timing diagram is shown in figure 6. The THA clock is a delay of the comparator and the DFF clock. The comparator latch enables at almost the end of THA hold period to ensure the input signal has fully propagated through the preamplifiers.

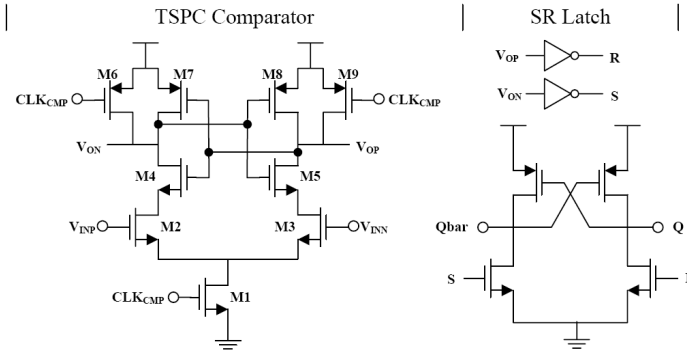


Fig. 5. High-speed comparator latch schematic.

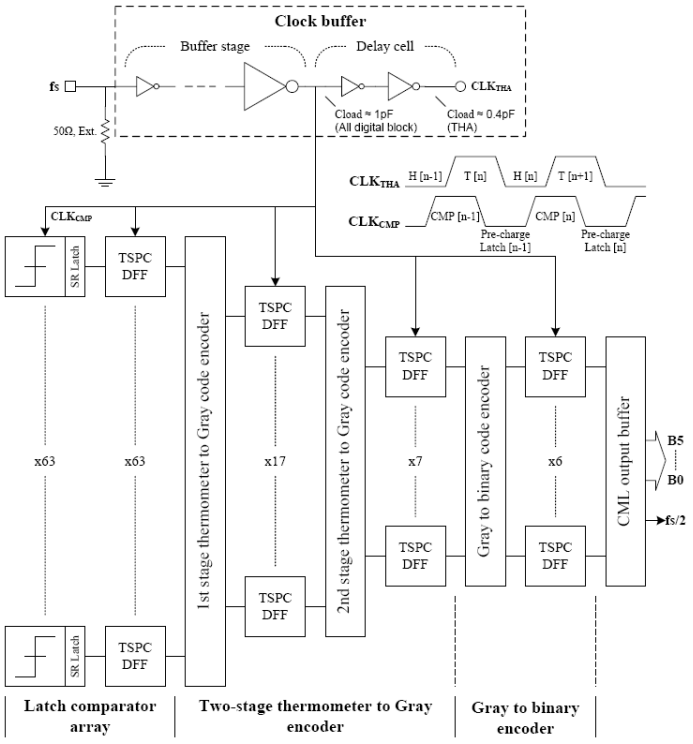


Fig. 6. Digital circuits and timing diagram of the ADC.

## IV. Experimental Results

Figure 7 is the prototype dual channel ADC measurement evaluation board. DeMUX arrays are for digital baseband circuits interface, not for measurement. The measurement setup is shown in figure 8. The ADC has six output differential signals plus one differential clock output. The Agilent 16900A logic analyzer with 16760A receiver module uses this clock output to double edge trigger the six ADC output signals for real-time measurement up to 1.6-GHz. Figure 9 and 10 shows the prototype ADC I/Q channel DNL and INL static performance. Both the DNL and INL are within 1-LSB. The dynamic performance is shown in figure 11. The ENOB for I/Q channel at DC is 5.25 and 5.35-bits respectively. At fin equals 350-MHz, the ENOB are 5.08 and 5.05-bits respectively. ERBW is around 450-MHz. Figure 12 is the output spectrum of an input signal of 350-MHz with 1024-points FFT diagram, indicating SFDR of 37.78-dB, which is dominating by 2nd order harmonic. Figure 13 is the chip die photo. All the performance values are summarized in table I.

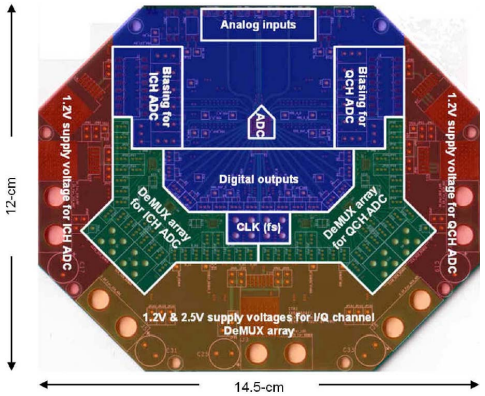


Fig. 7. Evaluation board of the ADC.

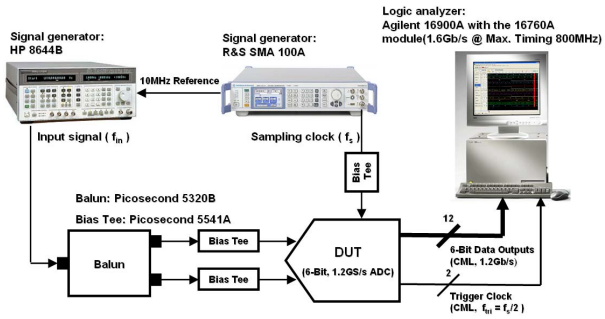


Fig. 8. ADC measurement environment.

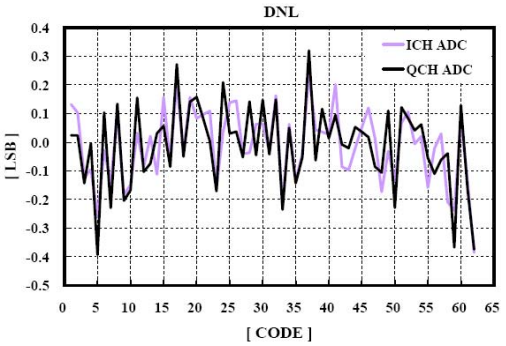


Fig. 9. Measured DNL at 1.2-GS/s and 1-MHz input frequency.

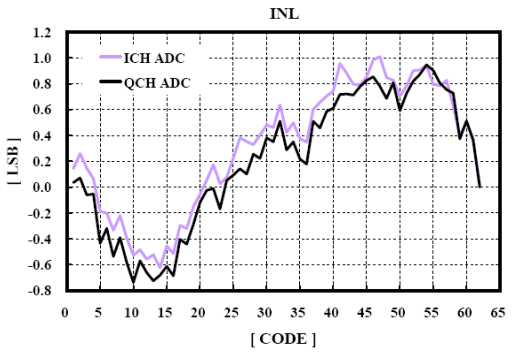


Fig. 10. Measured INL at 1.2-GS/s and 1-MHz input frequency.

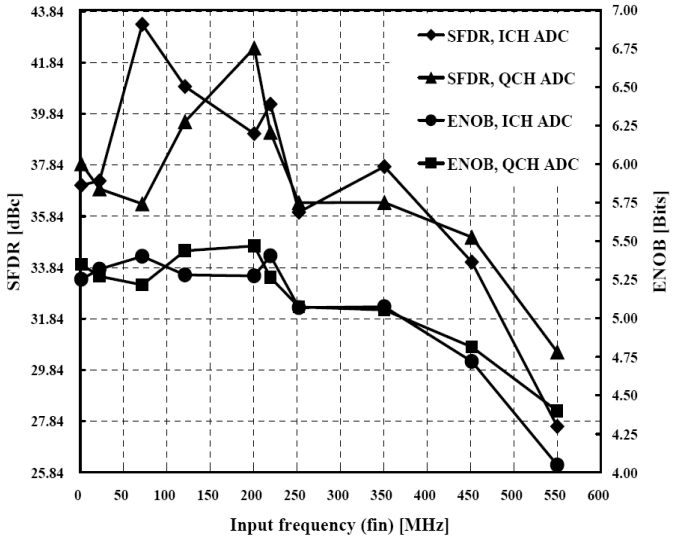


Fig. 11. Measured dynamic performance versus input frequency at 1.2-GS/s.

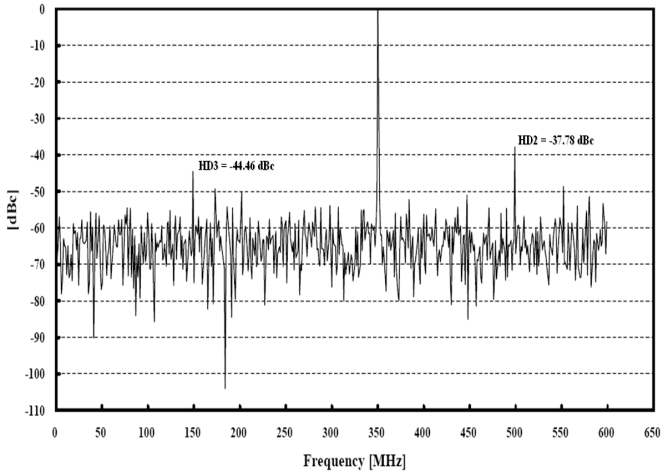


Fig. 12. Measured I channel ADC spectrum at 1.200128-GS/s, 350.428-MHz input frequency, and 1024-points.

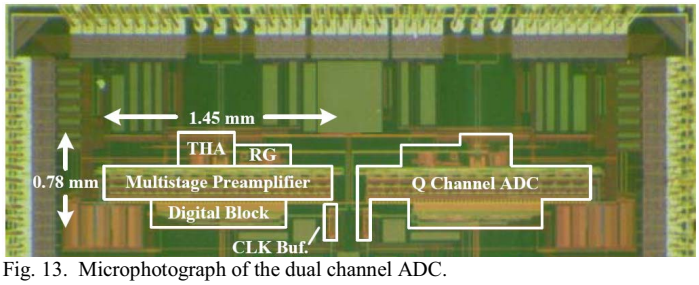


Fig. 13. Microphotograph of the dual channel ADC.

TABLE I
ADC PERFORMANCE SUMMARY

| | | |
|---|---|---|
| **Technology** | **0.13 um CMOS** | |
| **Sampling Rate** | **1.2 GS/s** | |
| **Resolution** | **6 Bits** | |
| **I/Q Channel ADC** | **I Channel** | **Q Channel** |
| **Input Range (Differential)** | **0.4 Vp-p** | |
| **DNL / INL**<br>**@ 1MHz input frequency, 1.2GS/s** | **0.39 LSB / 1 LSB** | **0.39 LSB / 0.95 LSB** |
| **ENOB @ fin=1MHz**<br>**@ fin=350MHz** | **5.25 bits**<br>**5.08 bits** | **5.35 bits**<br>**5.05 bits** |
| **ERBW** | **≈ 450 MHz** | |
| **Supply Voltage** | **1.2 V** | |
| **Power consumption (including ref. gen. w/o output buffer)**<br>**- Active mode (70% due to analog )**<br>**- Sleep mode** | <br>**88 mW**<br>**0.16 mW** | <br>**84 mW**<br>**0.19 mW** |
| **FoM★ ( pJ / convstep )** | **3.72** | **3.62** |
| **Single ADC area** | **1.45 x 0.78 mm$^2$** | |

★ **FoM=Power/($2^{ENOB}$ · 2 · fin)**
**Where input frequency (fin) is defined when ENOB ≧ 5 bit.**

## V. CONCLUSION

A prototype I/Q channel 6-bit, 1.2-GS/s ADC using 0.13-um CMOS process with averaging and interpolation has been purposed, which meets the MB-OFBM UWB system requirement. The figure-of-merit (FoM) of the dual channel ADC are 3.72 and 3.62-pJ/convstep, respectively. The single channel ADC occupies 1.45x0.78-mm$^2$ active area.

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