12 Bit 1.5 GS/s L-Band ADC on 200 GHz SiGeC Technology

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Abstract—

In advanced applications such as digital radar, Ultra Wide Bandwidth communications and software defined radio, the need for wide instantaneous bandwidth often drives system design decisions. Broadband 12 Bit ADC's (Analogue to Digital Converters) are key enabling components which open up new design opportunities for digital Receiver systems. In this regard, this paper describes a new 12bit true single Core 1,5 GS/s ADC with 2,3 GHz Bandwidth, based on a 200 GHz SiGeC bipolar Technology, which enables the direct digitizing of 500MHz broadband arbitrary waveforms directly in the 2nd Nyquist region closer to the Antenna (L-Band), enabling the design of flexible and simplified Radar receiver system architectures.

Keywords: Development of next-generation broadband flexible radar systems; Direct sampling at 1,5GS/s of 500MHz arbitrary UWB signals in the L-Band with > 9 Bit ENOB in the 2nd Nyquist;

I. INTRODUCTION

High speed ADCs featuring 12 Bit (70dB) linearity and better than 9 Bit ENOB over a wide range of frequency inputs with 1,5GS/s update rates are key components for new generations of broadband RF Radar Receivers. In this regard, a new generation of low latency Ultra Wide Band 12 1,5GS/s Bit ADC circuitry based on a 200 GHz SiGeC fully bipolar Technology has been designed to serve the next-generation of broadband flexible receivers including radar systems.

II. 12 BIT 1,5 GS/S ADC AND TECHNOLOGY

A. 12 Bit 1,5 GS/s ADC based on 200 GHz SiGeC (SiGe Carbon) Technology

The 12 Bit ADC operates at 1,5GS/s (Giga Samples per second) and features 2,3GHz full power input bandwidth , with nearly 57 dB SNR in the 2nd Nyquist zone with Fin = 1500MHz at – 1dBFS, which allows direct undersampling of signals in the 2nd Nyquist zone (L-Band).

The 12 Bit ADC is based on a true single core architecture, and does not rely on internal interleaved core ADCs to achieve 1,5GS/s update rate. Hence, the 12 Bit ADC does not require any form of calibration before or during operation over extended temperature range (-55C TCase up to +125C Junction temperature). Indeed, calibration is sometimes requested with internal interleaved ADCs Cores to avoid SFDR performance degradation due to misalignment of gain, offset, and sampling aperture delays. The 0dBFS Full Scale reference voltage span of the 12 Bit 1,5GS/s ADC is only 500 mV peak to peak into 100Ω differential impedance (embedded). The corresponding Full Scale input power is -2dBm if single-ended driven in 50Ω, and -5dBm if differentially driven in 100Ω termination . The low Full Scale input power of - 5dBm makes this ADC very easy to drive at 1,5GS/s especially in the 2nd Nyquist region, which relaxes the linearity constraints of the fixed or variable gain Amplifier driving the ADC. The 12 ADC embeds multiple 10 Bit and 12Bit Control DACs, which are monitored through a 3 Wire Serial Interface (3WSI), for remote fine tuning of the sampling delay, gain and offset. This feature is useful for instrumentation applications enabling easy interleaving of multiple standalone ADCs to increase the actual sampling rate.The ADC is packaged in a FPBGA196 Plastic Package, and features selectable 1:1 or 1:2 output DMUX ratio.

B. Performance enabling SiGeC Technology

III. The 12 Bit ADC is manufactured on SiGeC bipolar HBT technology [1]. The process uses a double-polysilicon self-aligned transistor configuration, with shallow and deep trench isolation, featuring selective epitaxial growth of boron doped SiGeC base. Carbon reduces boron diffusion (allowing steep doping profile). This technology offers NPN transistors with a cut-off frequency (fT) of 200 GHz at a current density of 6.5mA/um2, and fmax of 300 GHz, which allows high performance with low power trade-off. The metallization consist of four copper layers with a 2.5-um-thick top layer. In addition, two poly-silicon resistor types, very accurate thin film TaN resistors, and MIM capacitors are available.

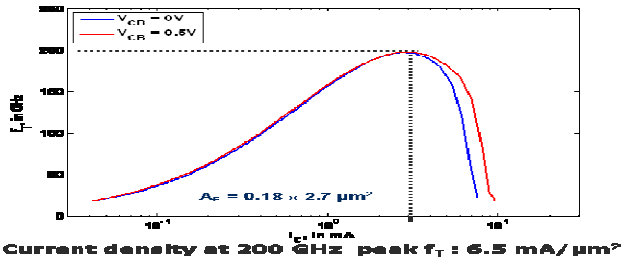

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Figure 1. 200 GHz SiGeC transistor measured peak cutoff frequency (fT) vs. current density

IV. 12 Bit 1,5 GS/s ADC +1:2DMUX

A. *Receiver System Architecture improvements*

Innovative architecture concepts together with the 200GHz cut-off frequency of the SiGeC Technology allows for enhanced noise and linearity performance in the 2nd Nyquist zone (Fin = 1500MHz) with 1,5GS/s update rates. SNR Noise performance of 57 dB is achieved thanks to the 100 fs rms sampling jitter of the ADC. Direct under sampling in the 2nd Nyquist of Ultra Wide Band (UWB) patterns of up to 500MHz with nearly 9,3 equivalent Bit ENOB (47 dB measured Noise Power Ratio (NPR) with -14 dBFS optimum loading factor) is demonstrated. The following figure (Fig.2) depicts the potential architecture improvement in terms of size, power, complexity, and cost of a receiver system based on such a performing UWB 12 Bit ADC.

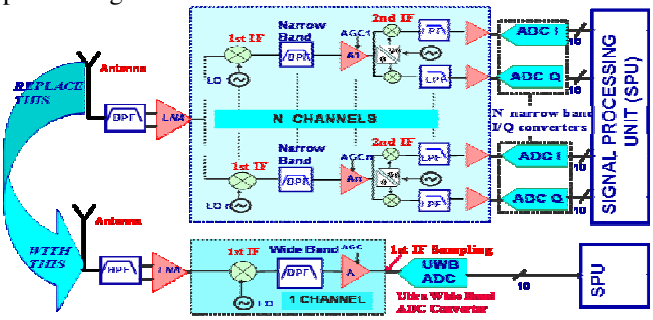

Figure 2. Example of Receiver System Improvement with 2nd Nyquist 12 Bit 1,5 GS/s ADC

B. *12 Bit 1,5 GS/s ADC Chip Description*

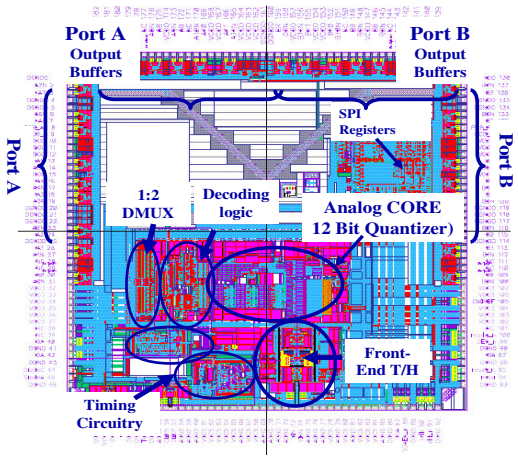

Figure 3. 12 Bit 1,5 GS/s ADC Chip Layout (to be replaced with chip microphotograph)

The 12 Bit ADC is based on 100 % fully bipolar vertically isolated NPN transistors. Component count is nearly 7000 SiGeC transistors and more than 10000 oxide isolated resistors (Fig.3). Accurate thin film TaN resistors are used for embedded 50Ω terminations (100 ohms differential).

The interconnections are based on four levels of Copper metallization to achieve low RC parasitic. The ADC maximum Power Consumption is 3,2Watt at Tj = 125°C junction temperature, including the 1:2 DMUX which is embedded on chip. Power supplies are +5.0V and +3.3V for the Analog section, and + 2.5V for the digital output buffers.

C. *12 Bit 1,5 GS/s ADC Architecture general Description*

The ADC architecture is fully differential from Analog input and Clock input up to the LVDS compatible Digital Outputs.
The ADC architecture is based on a fast settling 12 Bit Core ADC (analog quantization stage), driven by a fast and accurate front-end Track and Hold (T/H), featuring 70 dB linearity up to the 2nd Nyquist region. The 12 Bit quantizer is based on fast settling (flash like) folding and interpolation structures, designed to feature low throughput propagation delay, together with low input dynamic loading effect for the front-end T/H. The analogue quantizer is designed to settle to 12Bit accuracy within the T/H hold mode time width (half a clock period at 1,5GS/s = 333ps). It is pointed out that the 12 Bit quantization is performed within only one clock cycle, the 3 next clock cycles being dedicated to multiple cascaded regeneration latches to achieve better than 10E-13 Bit Error rates at 1,5GS/s. The total pipeline delay (latency) is therefore only 4 clock cycles, (i.e. 666ps each clock cycle.)

D. *12 Bit 1,5Gsps ADC Characterization Results*

The ADC performance has been characterized respectively in single tone, Dual tone, and also in broadband, by measuring the Noise Power ratio (NPR) with a 500 MHz pattern at - 14 dBFS optimum loading factor, to measure the ADC performance not only with single tones, but also in the situation of digitizing up to 500MHz UWB Patterns at 1,5GS/s, in either 1st or 2nd Nyquist regions.

1) 12 Bit ADC Single Tone FFT Computation at 1,5 GS/s in 1st, 2nd Nyquist zones (Fin = 740MHz & Fin = 1490MHz)

In the following figure (Fig.4), the time domain reconstructed sinewaves are shown at 1,5GS/s sampling rate, with Fin of respectively 10MHz, 740MHz, and 1490MHz at –1 dBFS, showing clean waveforms. On the eye diagrams, it is not possible to distinguish between the 10MHz curve from the 740MHz and 1490 MHz sinewaves.
Therefore, FFT computations have been carried out for fine spectral analysis of the noise floor (SNR) and the spurious levels (SFDR), with Fin = 740MHz and Fin = 1490MHz , and input levels of -3 dBFS and - 8 dBFS, to analyze large signal and small signal effects on SNR and SFDR.
At 1,5GS/s in the 1st Nyquist zone (with Fin=740MHz, -3dBFS), an ENOB of 8,88 Bit is achieved with an SNR of 57,5dBFS with an SFDR of 60dBFS clipped by the 3rd Harmonic (H3) , and - 72dBFS excluding H3. With an input level of – 8dBFS, the ENOB becomes 9,3 Bit including H3, with an SNR of 58,3 dBFS and an SFDR of - 75 dBFS .
At 1,5GS/s in the 2nd Nyquist, with Fin=1490MHz,-3dBFS, an ENOB of 8,72 Bit is achieved with an SNR of 57,2dBFS and

an SFDR of 59dBFS clipped by the 3rd Harmonic (H3), and 68dBFS excluding H3 (Fig.4). With an input level of - 8dBFS the ENOB becomes nearly 9,3 Bit including H3, with an SNR of 58,3 dBFS and an SFDR of - 72 dBFS (Fig.5).

For Broadband Radar applications with UWB patterns of up to 500MHz, the large signal H3 is not an issue, since we are concerned only by small signal linearity characteristics (see SectionV: Noise Power Ratio). For Narrow Band Applications using large signals, the H3 can always be filtered out. For instrumentation applications, it is possible to use a look up table to correct for the INL (Integral Non Linearity) characteristic of the ADC and take out the 3rd order Harmonic.

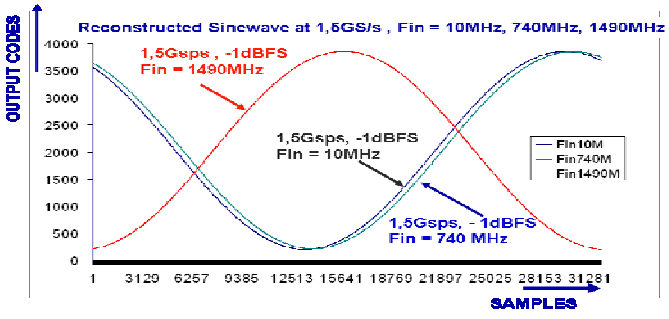

Figure 4. Time domain reconstructed sinewaves at 1,5GS/s , Fin= 10MHz, 740MHz, 1490 MHz , - 1dBFS

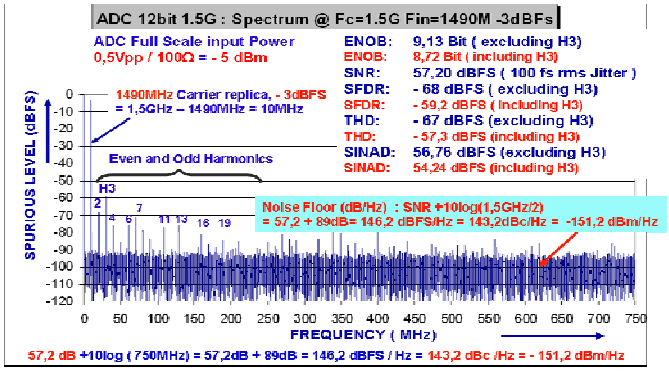

Figure 5. FFT Computation @ 1,5 GS/s 1stNyquist,Fin=1490 MHz , - 3dBFS

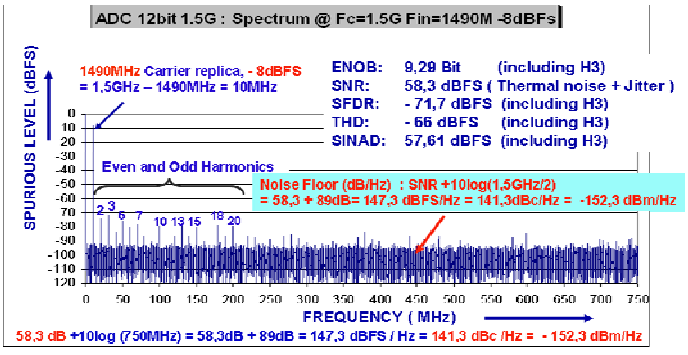

Figure 6. FFT Computation @1,5GS/s 2ndNyquist,Fin=1490 MHz , - 8dBFS

2) Single Tone SNR characteristics at 1,5 GS/s over 2 Nyquist Zones (DC to 1500 MHz) and vs. Input level

The following (Fig.7) depicts the large signal SNR rolloff versus analogue input frequency measured at 1,5GS/s over 2 Nyquist zones (DC up to Fin = 1500 MHz). The signal levels are ranging from -1dBFS to -12dBFS, to illustrate large signal SNR roll off due to sampling clock jitter, from small signal SNR performance related to input referred thermal noise of the front-end Track and Hold(T/H): The SNR roll off versus input frequency at -1dBFS is related to the voltage noise induced by the 100fs rms internal sampling clock jitter of the ADC.

With Fin = 1500MHz, the jitter effect on SNR is dominant and dictates the 56,5dBFS SNR at -1dBFS. With Fin = 10MHz, the jitter effect is negligible, and the 59 dBFS SNR is dictated by the input referred thermal noise of the front-end T/H.

An SNR of 56,5 dBFS at - 1dBFS leads to a noise floor given by : SNR + 10log(Fs/2) = 56,5dBFS+89dB = 145,5 dBFS/Hz = 144,5dBc/Hz. Since the ADC Full Scale differential input power is only -5dBm into 100Ω, the noise power spectral density is -5dBm-145,5dBFS = -150,5dBm per Herz.

The corresponding 32K points FFT noise floor in the FFT figures is given by SNR + 10log (N/2) = 57dB+10log (16384 points) = 92dB per 32K FFT bin width.

The ADC total self noise power includes the input referred thermal noise of the front-end Track and Hold (T/H), and the voltage noise induced by sampling clock jitter.

Therefore the contribution of the ADC to the overall system noise figure can be estimated.

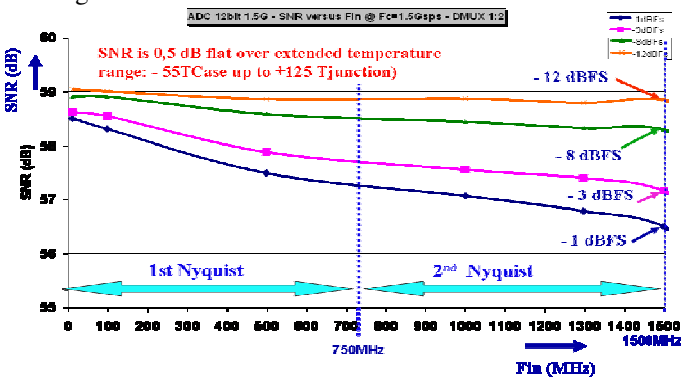

Figure 7. SNR roll off from DC to 1500MHz at 1,5 GS/s and vs. input level

3) Dual tone FFT computations at 1,5 GS/s and IMD3 performance in 2nd Nyquist vs Input level

Dual tone FFT measurements have been carried out at 1,5 GS/s with 2 tones places at (1450MHz,1460MHz), (Fig.8), showing the different intermodulation products with -7dBFS input tones levels (= -1dBFS vectorially summed). The IMD3 performance is given by the 3rd order (non filterable) intermodulation products terms (2F1-F2, 2F2-F1) close to the carriers, and is 67,6 dBc (which is nearly 11 Bit linearity).

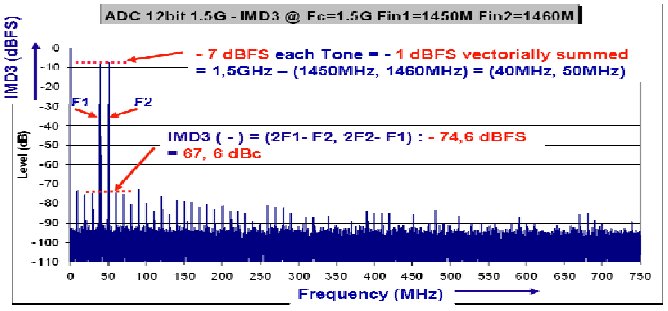

Figure 8. Dual Tone FFT computation at 1,5 GS/s (1450MHz, 1460 MHz)

V. 12 BIT 1,5 GS/S ADC BROADBAND NOISE POWER RATIO PERFORMANCE

A. *Noise Power Ratio (NPR) General Issues*

The dynamic performance of an ADC with broad bandwidth input is sometimes characterized by measuring a quantity known as the Noise Power Ratio (NPR). In ADC applications where the input signal contains a large number of incoherent tones or narrow bandwidth signals, it is generally desired that distortion, due to combinations of strong signal components, should not interfere with detection of weaker signal components. An example of such an input signal is one which contains a large number of frequency division multiplexed (FDM) channels, which are stacked in frequency for transmission over Radar equipments: For instance, hundreds of Channels may be stacked over a 500 MHz UWB wide frequency slot. For an ideal ADC NPR, only the quantization noise is taken into account: the relationship between broadband NPR and single tone SNR is given by:

$$SNR(ideal) = 20\log\frac{A/\sqrt{2}}{Q/\sqrt{12}} \qquad NPR(ideal) = 20\log\frac{rms(\text{broadband pattern level})}{Q/\sqrt{12}} = 20\log\frac{A/k}{Q/\sqrt{12}}$$

yielding : NPR = SNR - 20log(k)+3dB with A/k the rms level of the broadband composite signal (also called loading factor). For a real ADC, the NPR is the measure of the spectral power of all contributed RMS errors, such as inter modulation distortion (cross channels interference), quantization noise, thermal noise and jitter noise, in a narrow frequency slot (channel width) within the band of the 500 MHz UWB composite signal being processed, yielding :

$$NPR(real\_ADC) = 20\log\frac{A/k}{\sqrt{(Q/\sqrt{12})^2 + (Thermal)^2 + (Jitter)^2 + (IMD)^2}}$$

Therefore it is shown that there is a strong correlation between small single tone ENOB (SINAD) and NPR :

The rms (σ) level of the 500 MHz composite signal has to be placed at optimum peak to rms loading factor k =5 of the 12 Bit ADC Full Scale, with 20log(k) =-14dBFS, to avoid NPR rolloff due to ADC Full Scale clipping effect, (saturation noise), assuming Gaussian Probability Density function for signal amplitude distribution.[2]. Hence, the NPR is representative of the ADC performance in the situation of digitizing 500 MHz UWB patterns with 1,5GS/s update rate.

1) *ADC Noise Power Ratio Measurement*

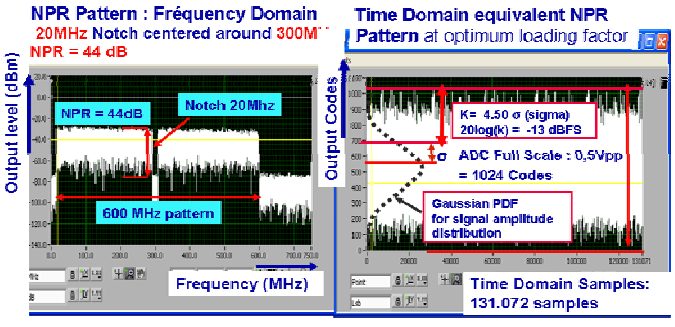

Figure 9. 10 Bit 1,5GS/s ADC NPR measurement results with 600 MHz input pattern with – 13 dBFS optimum loading factor =20log(k=4,5)

The NPR measurement Results of the 12Bit 1,5Gsps ADC will be presented at the Conference. The expected NPR is 47dB to 48dB, strongly correlated with the 9,3Bit ENOB (57,6 dB SINAD) measured at -8dBFS with 1,5Gsps and Fin= 1490MHz. For illustration, the measured NPR of a 10 Bit 1,5Gsps ADC (also designed by e2v) is shown in Fig.9, at 1.5 GS/s with 600 MHz pattern and 20 MHz notch. The measured NPR is 44dB with –13dBFS optimum loading factor, which is 8,65Bit equivalent, strongly correlated with the single tone ENOB measured for this 10 Bit ADC at – 8 dBFS.

B. *Packaging and Testing Issues*

The increased sampling rates also created new challenges in package HF modelling and industrial testing: The 12 Bit ADC is packaged in an fPBGA196, designed by e2v with the help of 3D-HF Software. The maximum power consumption of the ADC is 3,2Watt. The ADC measured SNR and SFDR is 1dB flat over a wide temperature range, (from – 55C Tcase up to Tj = +125C junction temperature), thus relaxing the thermal cooling constraints of the chip. The packaged ADCs are tested industrially and screened at full operating speed (1,5GS/s) in the 1st and 2nd Nyquist.

VI. SUMMARY

A 12 Bit 1,5GS/s ADC featuring 2,3 GHz full power input bandwidth has been characterized at 1,5 GS/s in 1st and 2nd Nyquist. The low full scale input power makes the ADC drivable by standard variable gain amplifiers. The ADC features stable high dynamic performance over extended temperature range (Tc=-55C to Tj=+125C) without the need of any form of calibration. This enables the direct sampling of 500MHz wide signals with > 9Bit resolution with center frequencies located up to the L-Band region, simplifying the Radar Receivers complexity, cost and size, with increased flexibility , including both airborne and space applications.

ACKNOWLEDGMENT

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