A 24GS/s 5-b ADC with Closed-Loop THA in 0.18µm SiGe BiCMOS

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***Abstract*-A 5-b flash ADC with a closed-loop THA is implemented in 0.18-µm SiGe BiCMOS. A global shunt feedback THA and a current-weighted comparator allow the ADC to achieve wide resolution bandwidth of 6.5GHz and high sampling rate up to 24GS/s. The ADC shows an SNDR of 28dB and an SFDR of 36dB with a 1GHz input sampled at 16GS/s. It consumes 3.3W from 3.6/3-V supplies and occupies 8.68mm^2 silicon area.**

I. INTRODUCTION

The demand of high-speed ADCs is rapidly increasing with the advent of higher data capability communication systems like a 40Gb/s optical coherent system. The recent interest of coherent detection is mainly motivated by the ability to receive complex modulation formats as well as the ability to access the full information of optical field in the electrical domain [1]. In a 40-Gb/s coherent system (Fig. 1), four bits of information can be encoded per symbol when DQPSK is used in conjunction with double polarization multiplexing. Thus, DSP-enhanced receiver requires four 5-b 20GS/s ADCs so that the ADC should be ultra-fast and low-power. Moreover, the resolution bandwidth of the ADC must exceed 0.6*symbol rate (of 10GBaud) > 6 GHz to take place smaller OSNR penalty.

CMOS time-interleaved ADC [2], SiGe flash ADCs [3, 4, 5], or InP flash ADC [6] are recently developed ultra-high-speed ADCs. However, most state-of-the-art ADCs have failed to achieve enough resolution bandwidth for coherent application because of the lack of a high-speed, high-dynamic range (DR) sampling circuit. In this paper, a 24GS/s 5b flash ADC embedded a closed-loop track and hold amplifier (THA) in 0.18-µm SiGe is presented. The design achieves a linearity of 4.4 effective bits for a 1GHz input signal and the effective resolution bandwidth up to 6.5GHz at 16GS/s.

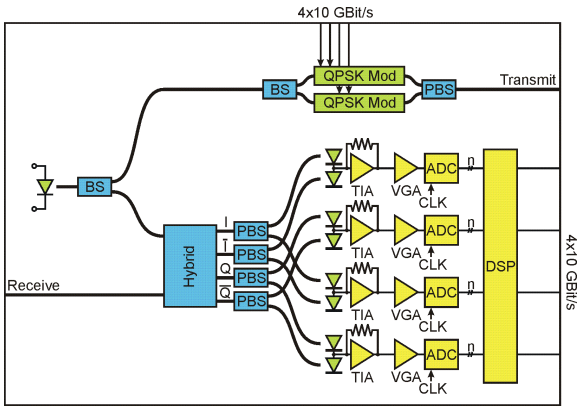

Fig. 1. Block diagram of a 10GBaud 40Gb/s coherent receiver [1].

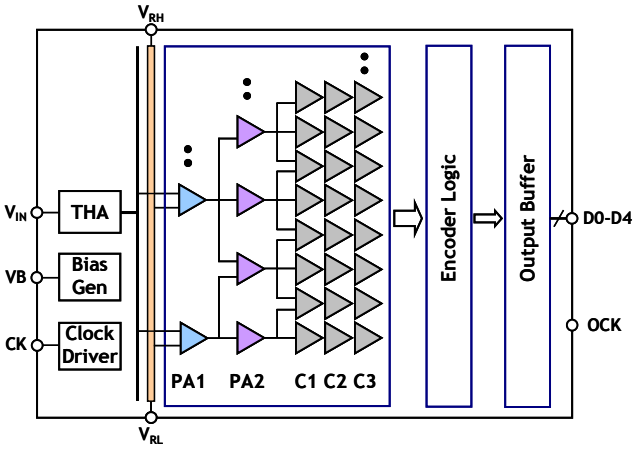

Fig. 2. Architecture of the ADC.

II. ARCHITECTURE

The architecture of the ADC is shown in Fig. 2. The input circuit of the ADC is constructed with a dedicated THA. The differential THA provides high-speed sampling operation and drives the flash quantizer with a full-scale range of 1-$V_{p\text{-}p}$ differential. The quantizer consists of a resistive ladder followed by 9 first-stage preamplifiers (PA1), 17 second-stage preamplifiers (PA2), and 33 master (C1) - slave (C2) - master (C3) comparators. This design applies amplification and interpolation per each PA stage in order to reduce large parasitic capacitance at the output of the THA and to relieve comparator offset requirements. The 31 thermometer code outputs are delivered to the encoder logic through differential microstrip transmission lines to suppress signal reflections. The encoder converts thermometer code into Gray code, and finally 5-b binary code.

III. Circuits Design

A. *Global Shunt Feedback THA*

A schematic of the THA is depicted in Fig. 3. At sampling frequencies of multiple tens of gigahertz, the wideband THA is hard to design, and critical for achieving good dynamic performance over broadband input signal. A compact wide-band THA is proposed using an active feedback

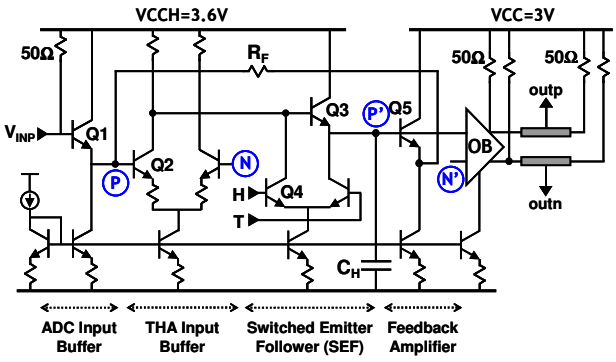

Fig. 3. Front-end THA with a closed-loop feedback.

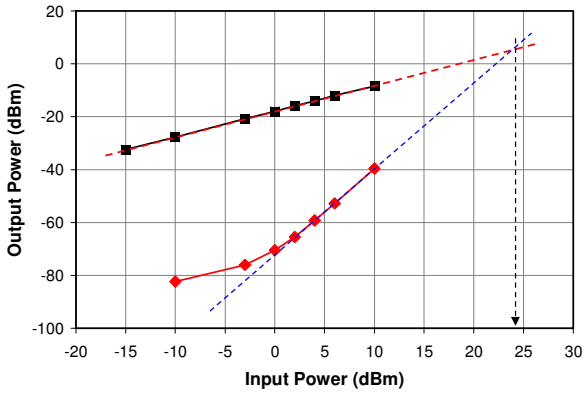

Fig.4. Measured input IP3 of the front-end THA.

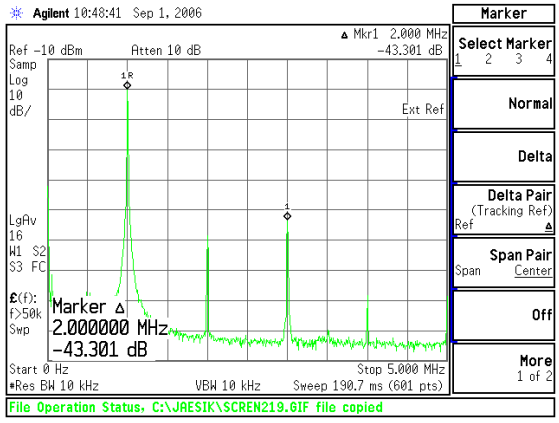

Fig.5. THA beat frequency test for track-to-hold mode with a 20GHz input signal and a beat frequency of 1MHz (Single-ended measurement).

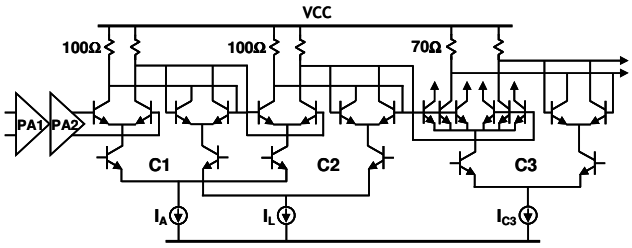

Fig.6. Schematic of M-S-M comparator array with bubble error correction.

topology. This global shunt feedback is employed at the output of the switched emitter follower (SEF) to the base of the THA input buffer to suppress the error from nonlinear parasitic and track-to-hold transition. The feedback is realized with a series combination of a unilateral feedback amplifier (Q5) and a shunt feedback resistor R_F. The feedback amplifier guarantees the isolation of a hold node from the input signal through R_F and compensates for the first-order hold-mode feedthrough caused by the C_{BE} of the SEF (Q3). Amount of feedback has been determined to make sure that the overall THA stability has been confirmed by S-parameter (S11 and S22) and K-factor. The ADC input emitter follower (Q1) that precedes the THA is necessary to decouple the input signal from the sampling circuit and ease the off-chip driving requirement for the THA. The input transistor (Q1) utilizes a large emitter length of 4x10-μm which is sufficient to drive the subsequent closed-loop THA with broadband input impedance of approximately 200Ω. In order to reduce the signal reflections the differential output of the THA is distributed to the PA1 through a balanced microstrip transmission line which achieves a characteristic impedance of 50Ω using a 2.8-μm-thick top metal layer (metal width of 10-μm) over M1 ground plane.

Measurements of the stand-alone THA show the advantages of the global shunt feedback THA which obtains 5.6dB gain of track mode dynamic range and 7.2dB gain of track-to-hold transition mode dynamic range, in comparison with the conventional open-loop THA. The track-mode bandwidth (S21) exceeds 26GHz in S-parameter measurements. This THA exhibits an input IP3 of 24dBm from two-tone intermodulation test with 10GHz and 10.1GHz input signals (Fig. 4), so that the SFDR is better than 48dBc with an input-referred noise power of -48dBm. The spectral characteristic of the beat frequency test at track-to-hold mode with $f_{IN} = f_S + \Delta f$, f_S = 20 GHz, and Δf = 1 MHz, at an input power of 0 dBm is obtained with the third-order harmonic distortion better than -43 dB (Fig. 5). The power dissipation of the THA including a clock buffer is 310 mW from 3.0/3.6 V supplies.

B. Current-Weighted Comparator

Two-stage PA array in conjunction with two-time interpolation allows reducing the number of preamplifiers from 33 to 9, thus reducing the nonlinear output capacitance of the THA. This topology also provides enough PA gain of 17 dB (= PA1 of 8dB + PA2 of 9dB) for the comparator's offset voltage as well as very small kickback noise. The overall bandwidth of the two-stage PA exceeds 20GHz. The comparator schematic shown in Fig. 6 consists of current-weighted master-slave (C1-C2) comparators followed by a

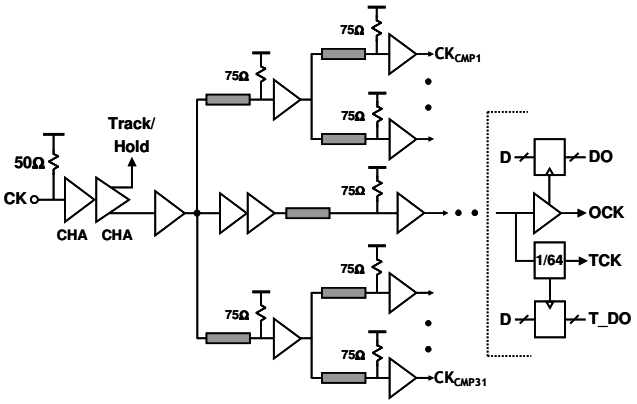

Fig.7. Clock distribution. The CHA denotes a Cherry-Hopper amplifier.

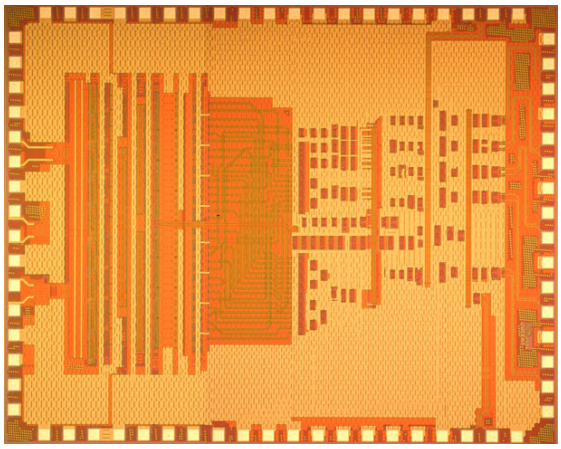

Fig.8. Die photograph.

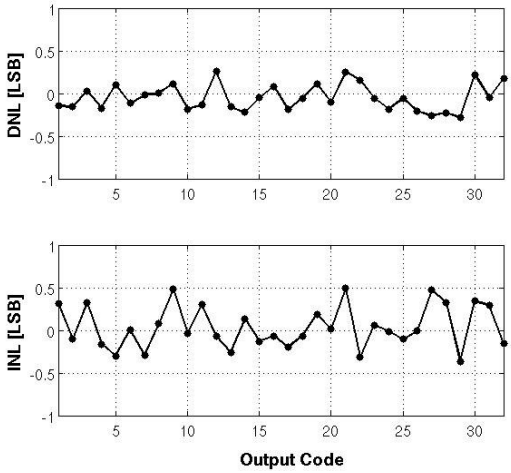

Fig.9. Static performance of the ADC.

third comparator stage (C3) with a bubble error correction to force a clean decision. The input BJTs in the comparator are chosen to guarantee 3σ offset voltage less than 0.2LSB (emitter length of 2.5-µm), while the transistors in the rest are chosen small (emitter length of 0.8-µm) for high-speed operation. The regeneration time constant is estimated about 12ps, mainly dependent on the device cut-off frequency and bias current. In the current-weighted M-S comparator, the bias current of the amplification (I_A=2.2mA) is emphasized over that of the latch (I_L=1.6mA) to suppress random offset and probability metastability, as well as reducing the overall comparator power dissipation. This 3-stage comparator guarantees a metastable error rate of less than 10^{-10} at 20GS/s.

C. *Circuits Implementations*

The routing of 31 differential thermometer traces is the most complicated and needs careful layout design. The balanced differential microstrip lines are used for interconnect with M6 (width of 3-µm for 75Ω) over M1 ground plan and M5 for routing bridge. This microstrip line is also used for clock distribution to reduce aperture jitter (Fig. 7). The encoded binary output can be switched to a test mode for decimated by-64 to enable easy acquisition by a logic analyzer.

IV. Measurement Results

The ADC has been implemented in a 0.18-µm SiGe BiCMOS. The chip occupies 2.63 x 3.3 mm^2 silicon area. Multiple power supplies are used: 3.6V for THA, 3V for analog part, and 3V for digital part. At the maximum clock frequency of 24 GHz, power dissipation is about 3.3W. Digital part including encoder logic and output buffers consumes around 1.6W, whereas the analog part including PA stages, comparator arrays, and line drivers for 31 thermometer codes consumes about 1.2W. The circuit board easily manages several watts power dissipation with simple stacked structure assembly. The ADC was mounted on the ceramic substrate via epoxy glue, which was then recessed into a circuit board. The substrate was carefully mounted on heat sink to minimize thermal resistance between the substrate and heat sink.

At 1 GS/s, measured DNL and INL are below 0.32 LSB and 0.53 LSB, respectively, as shown in Fig. 9. Figure 10 shows a spectrum measured for 1008.8 MHz input signal frequency at f_S = 16GS/s with 1/64 decimation (f_O=250 MHz). Thus, the fundamental spectrum is located at $f_{IN} - 4*f_O$ = 8.8 MHz. The SFDR is 35.8 dBc and effective number of bit (ENOB) is 4.4-bit. Fig. 11 shows the measured SFDR, SNDR, and SNR at the sampling rate of 16GS/s. While the SNR is better than 24dB up to Nyquist frequency, the SNDR is degraded to 21dB at Nyquist. The SNDR degradation at high input frequencies is mainly determined by signal-frequency-dependent spurious tones, rather than aperture jitter of 500fs. The effective resolution bandwidth (ERBW) is 6.5 GHz, and the figure of merit (FoM) of energy per conversion step is 11pJ. The die micrograph of the ADC is shown in Figure 8.

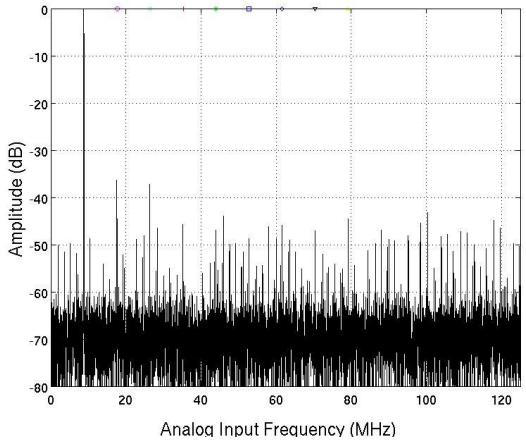

Fig.10. Output spectrum measured at 1008.8MHz input signal frequency. The sample rate is 16GS/s with 1/64 decimation (16384 FFT).

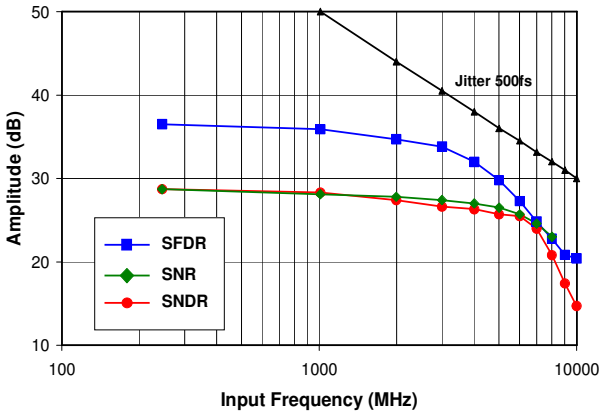

Fig.11. Measured SNDR and SFDR versus analog input frequency at f_S=16GS/s.

V. Conclusion

We report a 5-b 24GS/s ADC with enough resolution bandwidth for 10GBaud 40-Gb/s optical receivers. In order to achieve the best resolution bandwidth of 6.5GHz, a global shunt feedback THA has been embedded in the ADC. ENOB is > 3.5-bit up to Nyquist at 16GS/s. The FoM of 11pJ/conversion step, which is the best in comparison with prior arts, has been obtained with 3.3W power consumption.

	5-bit 20GS/s ADC
Input Frequency (f_{in})	< 10 GHz
Sampling Frequency (f_s)	> 20 GHz
DNL/INL	+/- 0.32 / 0.53 LSB
SNDR @ fin = 1GHz	> 28 dB
SNDR @ fin = 3GHz	> 26.5 dB
ERBW *	> 6.5 GHz
Timing Jitter (RMS)	< 500 fs
Power Dissipation @3/3.6V	~ 3.3 W
FoM **	*11 pJ*
Technology	SiGe 0.18-μm BiCMOS

Table 1. Summary of the ADC characteristics.

Acknowledgements

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