A 20-GS/s 5-b SiGe ADC for 40-Gb/s Coherent Optical Links

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***Abstract*—A 10-GBd 40-Gb/s coherent optical transport is a promising technology for higher data rate communications by virtue of improved sensitivity and high spectrum efficiency. One of the major challenges in designing a 40-Gb/s coherent quadrature-phase-shift-keying receiver is to achieve high-speed data conversion at around 20-GHz sampling rate with at least 5-bit resolution. With the detailed design framework for the target requirements, this paper presents a 5-bit 20-GS/s flash analog-to-digital converter (ADC) realized in 0.18-μm SiGe BiCMOS technology. The ADC includes a track-and-hold amplifier (THA) incorporated with linear distortion compensation, double-interpolation preamplifier, current bias-weighted comparator, and high-speed encoder logic. At 4 V, the THA had a bandwidth that exceeded 23 GHz and an IIP3 of 24 dBm. The ADC achieves a signal-to-noise-plus-distortion ratio of 28.6 dB and a spurious-free dynamic range of 36 dB with a 1-GHz input sinusoid sampled at 20 GS/s. The ADC has a wide resolution bandwidth of 7 GHz, and the figure of merit is 9.54 pJ/conversion-step. The ADC consumes 3.24 W from 4- and 3-V supplies when sampled at 20 GHz. The prototype ADC occupies 8.68 mm^2 of silicon area.**

***Index Terms*—Analog-to-digital converter (ADC), coherent optical receiver, linearity compensation scheme, resolution bandwidth, SiGe BiCMOS, track-and-hold amplifier (THA).**

I. Introduction

HUGE capacity-growth forecasts have led to the development of technology for the next-generation transmission rate, such as 100-Gb/s coherent optical transmission. Recent attention on coherent detection is mainly motivated by its ability to receive complex modulation formats, as well as the ability to access full information of the optical field in the electrical domain [1]. In a 10-GBd 40-Gb/s coherent system, a digital-signal-processing (DSP)-based receiver requires four ADCs for polarization multiplexing, so the ADC should be ultrafast and of low power. State-of-the-art ADCs such as CMOS time-interleaved [3], [4], SiGe flash [5]–[9], [15], and InP flash [10] have recently been developed for use in DSP-based signal equalization. However, most high-speed medium-resolution ADCs have failed to achieve the target performance for 40-Gb/s coherent applications due to lack of enough resolution bandwidth.

This paper presents a 20-GS/s 5-b SiGe ADC that is capable of managing sufficient resolution bandwidth and higher dynamic performance over prior arts while simultaneously achieving power efficiency. The design has carefully been optimized by taking account of the system requirements. The ADC with linear distortion compensation track-and-hold amplifier (THA) is presented in 0.18-μm SiGe BiCMOS technology. The prototype ADC digitizes a 1-GHz input with a linearity of 4.5 effective bits and a 7-GHz input with 4 effective bits at 20 GS/s.

Section II reviews the architecture of a coherent quadrature phase-shift keying (QPSK) receiver and the ADC, and the details of circuit design follow in Sections III and IV. The experimental results are reported in Section V.

II. Architecture

Advanced coherent optical transport technologies that support the need for high spectral efficiency and high-performance communications are attractive to future free-space and terrestrial optical communications to meet the ever-increasing demand of transmission capacity. Recent coherent receivers are based on DSP techniques for transmit-local oscillator (LO) laser synchronization, instead of traditional phase-locked-loop techniques. In this scheme, the phase or frequency fluctuation of the free-running LO laser is compensated in the digital domain [1], [2]. Fig. 1 illustrates a simplified schematic of a DSP-based receiver setup for the coherent polarization-division-multiplexed QPSK 10-GBd 40-Gb/s signal. The receiver consists of a free-running optical LO laser, an optical hybrid that mixes the received optical signal with the LO laser signal, balanced photodiodes, and an electronic receiver. The front-end electronic receiver includes a transimpedance amplifier (TIA), variable gain amplifiers (VGAs), ADCs, and a DSP unit. Digital coherent detection with polarization diversity is used to sample the fields of the two orthogonal components of the received optical signal, so that four electric channels, in-phase/quadrature components, and horizontal/vertical components (I/Q and X/Y) are arranged. Then, a DSP unit is advantageously used to relax the constraints on the LO. Even more importantly, the DSP unit has a tremendous potential to mitigate the impact of propagation impairments, such as chromatic dispersion, polarization mode dispersion, and nonlinear effects.

In a coherent optical link, a high-speed ADC is a fundamental component. The system bit error rate (BER) required determines the resolution needed for digital conversion. The resolution of the ADC is chosen, so that the quantization noise is below the maximum noise level that allows the system to operate. The

Manuscript received November 09, 2009; revised February 04, 2010; accepted March 10, 2010. Date of publication May 27, 2010; date of current version October 08, 2010. This work was supported in part by DARPA under Contract HR0011-05-C-0153 supervised by Dr. Jay Lowell. This paper was recommended by Associate Editor S. Pavan.

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Digital Object Identifier 10.1109/TCSI.2010.2048678

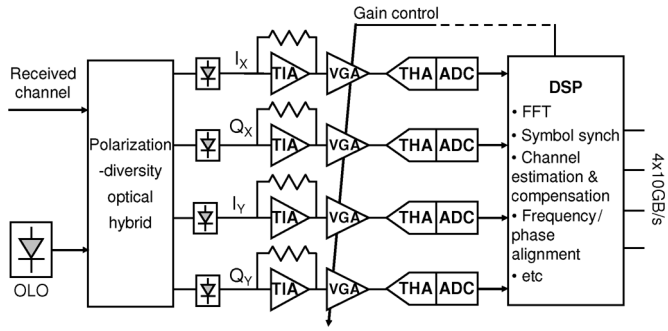


Fig. 1. Block diagram of a 40-Gb/s 10-GBd coherent QPSK optical receiver.

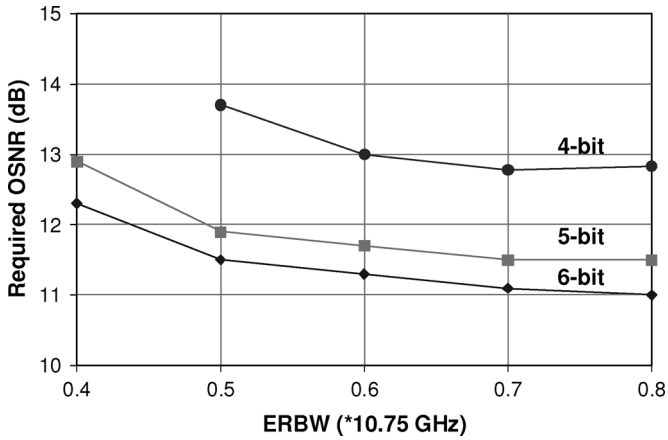


Fig. 2. Required OSNR versus ERBW of the ADC.

analysis is based on Monte Carlo simulation with additive white Gaussian (AWG) noise source for optical noise. The quantization noise and distortion are added by time-domain discretization of the signal-plus-AWG noise. The ADC resolution bandwidth is modeled by reducing the gain of the ADC in the frequency domain using a Bessel-shaped low-pass filter in front of it. All other noise sources of the ADC are not included. The required optical signal-to-noise ratio (OSNR) is for a BER of 10^{-3}. Fig. 2 shows the simulated OSNR requirement versus the effective resolution bandwidth (ERBW) of ADC with respect to the ADC resolutions. In the simulations, the symbol rate is 10.75 GBd. Simulations show that using a lower ADC resolution requires higher ERBW to maintain a similar OSNR. From the application frameworks, target specifications of the ADC are summarized in Table I.

When designing a high-speed ADC, a large number of options must be considered. One fundamental choice is whether to use silicon or III-V technology. The capability of Si-based technologies for ADCs with a sampling rate of tens of gigasamples per second has been demonstrated [3]–[9], [15]. Emergence of Si-based CMOS or SiGe is attributed to their fast device scaling, which continues to drive them toward achieving higher speed, higher integration level, and lower cost. Different Si-based technologies, however, usually employ different architectures to achieve ultrafast digitization operation. CMOS ADCs [3], [4] have mainly relied on the sophisticated interleaved architecture with heavy digital calibration, whereas SiGe ADCs [5]–[9], [15] utilize straightforward architecture and design due to the benefits of their inherent high-speed low-noise bipolar properties. This ADC has been implemented in a 0.18-μm

TABLE I
PERFORMANCE REQUIREMENTS

Specifications	Value
Input voltage range	1 $V_{p\text{-}p}$ differential
Resolution	4-bit
Resolution bandwidth	7 GHz
Signal bandwidth	20 GHz
Sampling rate	20 GHz
Static performance	1 LSB
Supply voltage	4 V and 3 V
Power budget	3 W
Figure of Merit (FoM)	10 pJ/conv-step

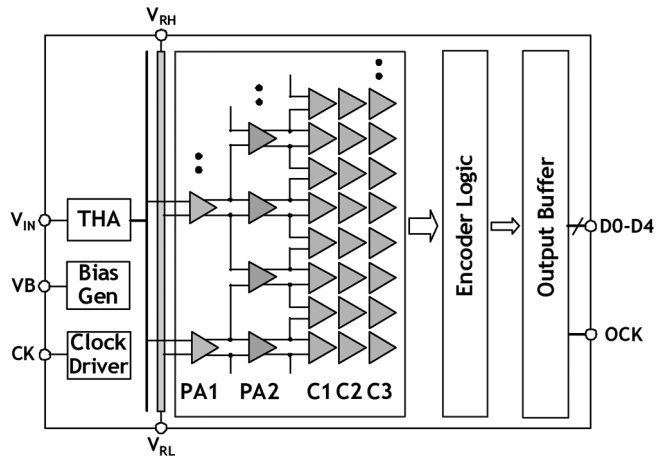


Fig. 3. Architecture of the ADC.

SiGe BiCMOS process, which offers high-speed n-p-n bipolar transistors ($f_T/f_{\max}$ of 200/200 GHz), six layers of metal, a metal–insulator–metal (MIM) capacitor, and low-resistance metal resistor.

This ADC deploys a one-step fully differential flash architecture, as presented in Fig. 3. The ADC consists of a front-end sampling circuit, a 5-b flash quantizer including a two-stage preamplifier and a three-stage comparator, and high-speed encoding logic. The sampling circuit is constructed with a dedicated THA. The THA is required to overcome the limitation on analog signal bandwidth and to compensate for the linearity degradation from the long settling time and nonlinear parasitic of the subsequent flash quantizer. The front-end THA potentially provides a bandwidth of 20 GHz, which enables ultrafast sampling and drives the quantizer with a full-scale range of 1 $V_{\mathrm{p-p}}$ differential. The THA is, however, difficult to implement since fully integrated sampling circuits with wideband and high dynamic linearity are not available. A distortion-compensated linear sampling circuit is proposed for this ADC, which is incorporated with a global shunt feedback [9] and feedforward compensation scheme. The details of this operation will be described in the next section.

The flash quantizer consists of a resistive reference ladder, followed by nine first-stage preamplifiers (PA1), 17 second-stage preamplifiers (PA2), and 33 master–slave–slave

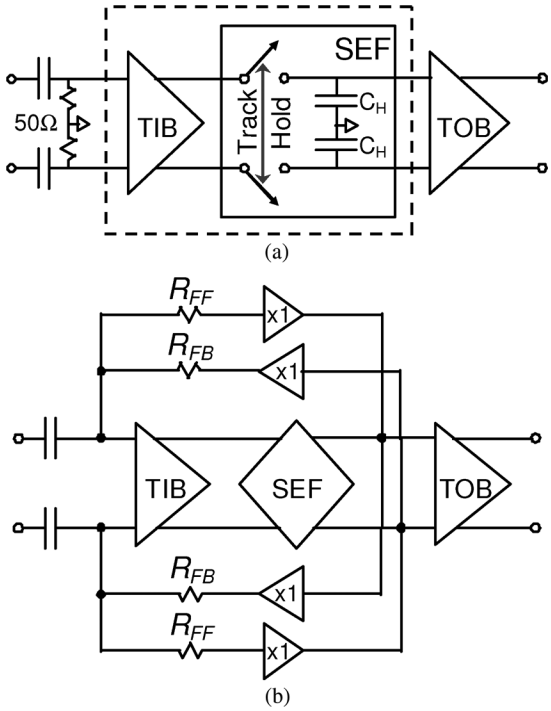


Fig. 4. Comparison of (a) open-loop and (b) closed-loop THA.

comparator arrays, thus forcing a clear decision. Tantalum nitride (TiN) metal resistors are used for a low-resistive reference ladder (each tap resistance $\sim$ 10 Ω) to ensure a small resistor mismatch. Along with using 10-μm wide resistors, a great deal of attention has been focused on the layout design in order to improve the symmetry. The quantizer design applies amplification and interpolation for each preamplifier stage to reduce the large parasitic capacitance at the output of the THA and to relieve the comparator offset requirement. The comparator is a high-gain three-stage configuration, which includes a master–slave current bias-weighted comparator (C1 and C2) and a bubble error correction comparator (C3). The 31 thermometer code outputs are delivered to the encoder logic through balanced microstrip transmission lines to enhance high-speed signal integrity. The encoder converts the thermometer code into Gray code and, finally, 5-b binary code.

III. THA

The receiver front-end, including TIA and VGA in Fig. 1, is usually a high-performance digitally controlled variable-gain differential ADC driver. As the signal frequency increases up to 10 GHz in a 40-Gb/s coherent receiver, the VGA that drives the significant capacitive loading of the ADC must keep pace by delivering low distortion and noise. A high-speed driver amplifier [3] or THA [5] in front of the quantizer is effectively used for easing the off-chip driving requirement. For tens of gigahertz sampling frequencies, however, the requirements of bandwidth and linearity of the driver or THA are critical to achieving good dynamic performance over broadband signal frequency. The conventional open-loop bipolar THA in Fig. 4(a) consists of a switched emitter follower (SEF), a hold capacitor, and an input and output buffer (TIB/TOB). It is intrinsically simpler and faster than the closed-loop architecture because of lack of a feedback loop. State-of-the-art THAs based on open-loop architectures can sample the signal up to 40 GS/s [11], [12]. However, the accuracy of the open-loop architecture is substantially lower than that of the closed-loop alternative because of the offset and gain errors among components, signal-dependent distortions, and input-dependent track-to-hold mode errors. To attenuate the errors in the THA, a fully differential closed-loop THA is proposed, as illustrated in Fig. 4(b). The use of global negative feedback has several effects on the THA performance: It can significantly reduce the dependence on device parameters and any input-referred offset and gain errors of input amplifier and the SEF. In addition, it can suppress signal-dependent charge injection in track-to-hold mode or on-resistance variation in track mode, thereby reducing harmonic distortion.

A. Circuit Configuration

The circuit diagram of the closed-loop THA is shown in Fig. 5 (single-ended description for simplicity). It consists of the THA input buffer TIB (Q_1 and R_{C1}), followed by the SEF (Q_2 and $Q_3 - Q_4$) as an active switch, and the THA output buffer TOB. One of the important features of the design is that it uses feedback circuits by means of a shunt feedback resistor $R_{\rm FB}$ and a unilateral feedback amplifier, formed by a common-collector configuration (Q_5). The global shunt feedback is developed around two stages, leading from the output of the SEF to the input of the input buffer. The TIB is a moderately degenerated differential amplifier. It has a small-signal bandwidth of at least 25 GHz over process and temperature corners. The input transistor Q_1 is biased to minimum noise figure current density at around 10 GHz. The second stage is the unity-gain SEF and a hold capacitor C_H of 285 fF. It includes a 202-fF MIM capacitor and a parasitic capacitance of approximately 83 fF including the input capacitance of both the output buffer and the feedback amplifier. The bandwidth of the SEF is below 20 GHz in simulation because of a large hold capacitor, yet it is able to suppress hold mode distortion. Q_5 forms a unilateral feedback amplifier inserted in the feedback path. It is capable of driving the shunt feedback resistor $R_{\rm FB}$ in track mode and isolating the hold capacitor from the input signal in hold mode. In addition, it partially compensates the first-order hold-mode feedthrough caused by the $C_{\rm BE}$ of $\rm Q_2$ with the $C_{\rm BE5}$.

In this feedback loop design, only one moderate gain stage TIB is used to preserve a high bandwidth with adequate phase margin. The open-loop voltage gain and bandwidth of TIB + SEF are about 3.2 ($\sim$ 10 dB) and 16 GHz, respectively. In the closed-loop configuration, meanwhile, the voltage gain is reduced to 3 dB, and its bandwidth is expanded to 27 GHz.

The value of the shunt feedback resistance influences the linearity of the THA, and simulations were performed from 100 to 500 Ω. Fig. 6 shows the results of the dynamic range test [DR = fundamental—third-order intermodulated distortions (IMD3)] for a 10-GHz sinusoidal input signal for different feedback resistances $R_{\rm FB}$. The DR of the open-loop THA with $R_{\rm FB} = 15$ kΩ for a 150-mV single-ended input voltage is 29.6 dB. It is degraded to 24.5 dB when the input voltage increases to 250 mV. The DR of the closed-loop THA ($R_{\rm FB} = 100\ \Omega$) is 40.5 dB for a 150-mV single-ended input voltage, so the gain of DR is 10 dB. The linearity gain with closed loop is reduced

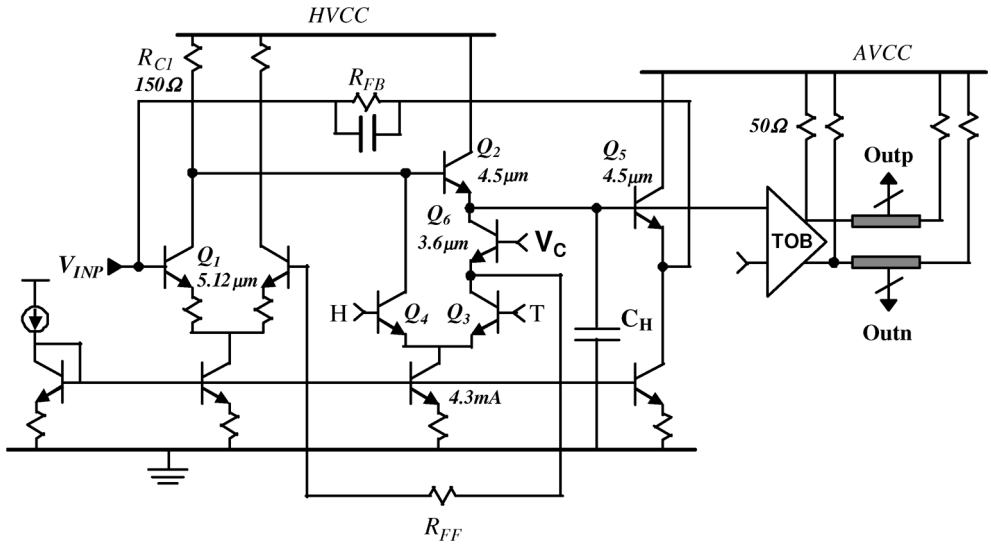


Fig. 5. Simplified schematic diagram of front-end THA. The minimum emitter width of 0.18 μm is used for all heterojunction bipolar transistors (HBTs).

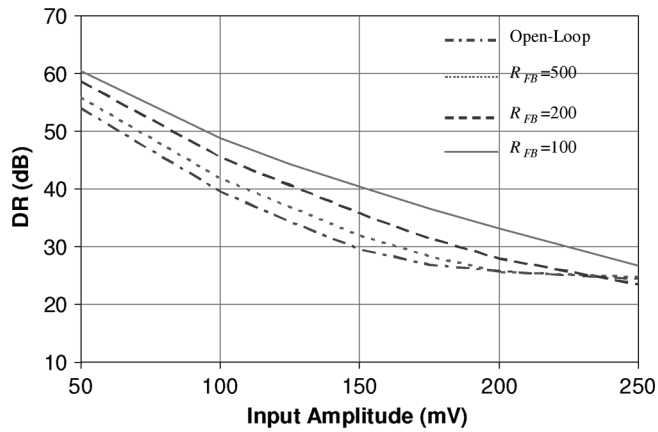


Fig. 6. Simulated dynamic performance with respect to various feedback resistance $R_{\rm FB}$.

to 2.5 dB when the input voltage is increased to 250 mV. In this design, $R_{\rm FB}$ is set to 150 Ω.

In order to reduce the signal reflection, the differential output of the THA is distributed to the first preamplifier stage (PA1) through a balanced microstrip transmission line. This differential transmission line provides a characteristic impedance of 50 Ω. It is implemented with 2.8-μm-thick 10-μm-wide top metal lines spaced 30 μm apart over M1 ground plane.

B. Stability

Since the global shunt feedback path encircles four internal poles, special attention should be given to the stability of the loop. When three gain stages in the loop accumulate extra phase shift, the transit-time delay increases, resulting in reduced stability. To properly account for the stability, the Bode plot and stability factor (k-factor) have been examined. The appropriate Bode plot of the loop gain includes four poles and one zero: two poles for the THA's open-loop gain; two poles for the $1/\beta$ curve, where β is the feedback factor; and one zero along the feedback path resulting from the finite output impedance of feedback amplifier. The dominant pole occurs at the output of the SEF, $\tau_{P1} \sim (1/g_{m2} + R_{E2}) * C_H$, due to the large hold capacitance. The second pole is located at the output of the input buffer, i.e., $\tau_{P2} \sim R_{C1} * (C_{\rm BE2} + C_{jo1} + C_{jo4})$. The $1/\beta$ curve includes two poles, where one pole occurs at the input of the input buffer, i.e., $\tau_{P3} \sim (R_S \| R_{\rm FB} \| R_{\rm FF}) * C_{\rm IN}$, and the other occurs at the output of the feedback amplifier, i.e., $\tau_{P4} \sim (R_{\rm FB} \| R_{O5}) * (C_{\rm FB} + C_{\rm BE5})$. The zero occurs at the shunt feedback resistor, i.e., $\tau_z \sim R_{\rm FB} * (C_{\rm FB} + C_{\rm RF})$. The condition for the THA stability is that the closed-loop's phase margin is approximately 90°. This stability condition should meet the following condition:

$$f_Z < f_{P4} < f_{P2}.$$

This condition sets the load resistance R_{C1} of the input buffer to be 150 Ω, which leads to low loop gain and limits the effective distortion suppression of the feedback loop.

The stability is also confirmed with k-factor in S-parameter simulations. As well known, a k-factor > 1 is sufficient to guarantee unconditional stability in the THA. For the regions where $k < 1$, the THA is only conditionally stable under specific load conditions. This simulation indicates that a smaller feedback resistance results in large k-factor stability margin over process and temperature variations.

C. Feedforward Compensation Technique

A source of distortion in this architecture is the signal-dependent modulation of the base–emitter voltage $V_{\rm BE2}$ that might occur at the SEF. This distortion is caused by charging and discharging the current to the hold capacitor C_H, and it might result in the deterioration of a third-order harmonic [13], i.e.,

$$HD_3({\rm dB}) = 20 \log \left[1/12 * A_{\rm IN}^2 v_T (f_{\rm IN} * C_H / I_{\rm SEF})^3\right]$$

with $f_{\rm IN}$ and $A_{\rm IN}$ denoting the input signal frequency and amplitude, respectively. In order to enhance the linearity at the SEF, the hold capacitance must be designed with a relatively low value. However, it can lead to the degradation of pedestal error or hold-mode feedthrough. This tradeoff can be overcome by adding an additional current in the feedforward signal path.

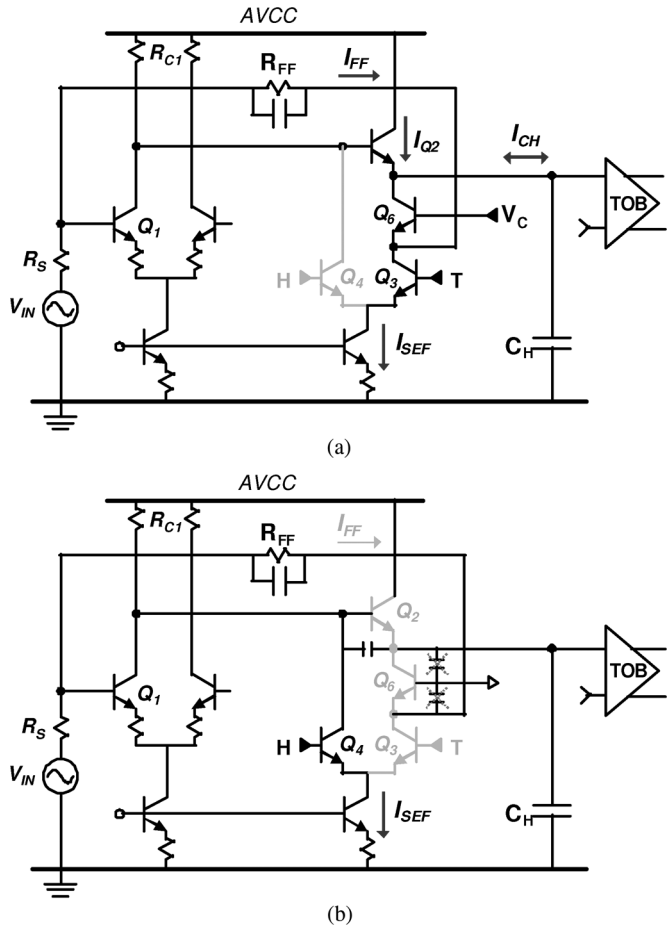


Fig. 7. Operations of the THA in (a) track mode and (b) hold mode.

From the schematic of the feedforward amplifier in Fig. 7, a feedforward current $I_{\rm FF}$ through a relatively large feedforward resistor $R_{\rm FF}$ and a feedforward amplifier is given by

$$I_{\rm FF} = V_{\rm IN} * (R_{\rm FF} + R_S) * A_{\rm FF}$$

when $R_{\rm FF} + R_S \gg R_{\rm IN}$ of the feedforward amplifier. The feedforward amplifier is a broadband common-base configuration, and its voltage gain is almost unity, i.e.,

$$A_{\rm FF} = g_{m6} * R_O = g_{m6} * 1/g_{m2} \sim 1.$$

In track mode in Fig. 7(a), the feedforward amplifier delivers the input signal to the output of the SEF and compensates the charging/discharging current $I_{\rm CH}$ from the collector current I_{Q2} of the SEF. In hold mode in Fig. 7(b), the feedforward amplifier is turned off, hence isolating the hold node from the input signal. The collector–base capacitance $C_{\rm CB6}$ does not cause high-frequency feedback from output to input, so the hold-mode feedthrough is not degraded at all. Fig. 8 illustrates the simulated spurious-free dynamic range (SFDR) versus the feedforward resistance at 10-GHz input signal. Here, the SFDR is defined by $2/3 * (IIP3 - P_{\rm Nin})$ [4], where $P_{\rm Nin}$ is the input-referred noise power. This plot shows that the feedforward compensation with $R_{\rm FF}$ of 400 Ω has ∼5 dB better linearity than the alternatives. The degradation of the SFDR as $R_{\rm FF} > 500\ \Omega$ results from the increase in input-referred noise power $P_{\rm Nin}$.

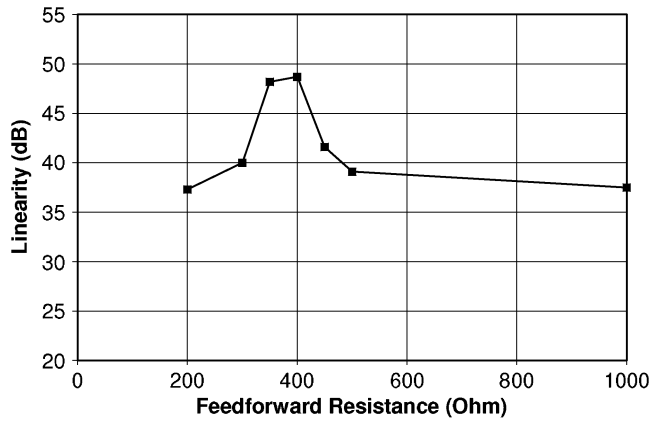


Fig. 8. SFDR over feedforward resistance $R_{\rm FF}$.

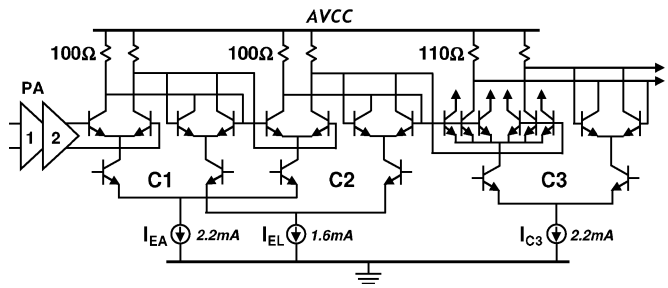


Fig. 9. Schematic of the master–slave–slave comparator with a bubble error correction.

IV. Design and Implementations

A. Current Bias-Weighted Comparator

The basic circuit of the newly designed comparator array is shown in Fig. 9. The key factors in forcing a clean decision while reducing the power consumption are the use of double interpolation and optimally designed current bias-weighted comparator [5], [14]. Double interpolation incorporated with a two-stage preamplifier allows reducing the number of preamplifiers from 31 to 22 (not counting the dummies), thus minimizing the nonlinear parasitic capacitance at the THA output. In addition, it not only reduces the power dissipation but also improves the differential nonlinearity (DNL). The two-stage preamplifier, as shown in Fig. 10, provides a sufficient gain of 17 dB to relieve the comparator's offset requirement and to minimize kickback noise. The overall bandwidth of the preamplifiers exceeds 20 GHz, which is critical to obtaining a very small recovery time. The recovery time of the PA is inversely proportional to the PA bandwidth and must be less than 25 ps to achieve a conversion rate of more than 20 GHz. The recovery time constant can be expressed as follows [5]:

$$\tau_{\rm rec} = V_{\rm Logic} * C_{\rm total}/I_{\rm EA} * \ln\left(1 + 1/\tanh(G_{\rm PA} * \Delta v/2v_t)\right)$$

where $V_{\rm Logic}$ is a logic level, $C_{\rm total}$ is the total parasitic capacitance, $I_{\rm EA}$ is the operating current of the amplifier, $G_{\rm PA}$ is the total gain of the amplifier, and Δv is the initial voltage difference between the input and the reference signal. The recovery time constant is related to the regeneration time constant at the latching comparator with the expression

$$\tau_{\rm reg} = 2 * v_t * C_{\rm total}/I_{\rm EL}$$

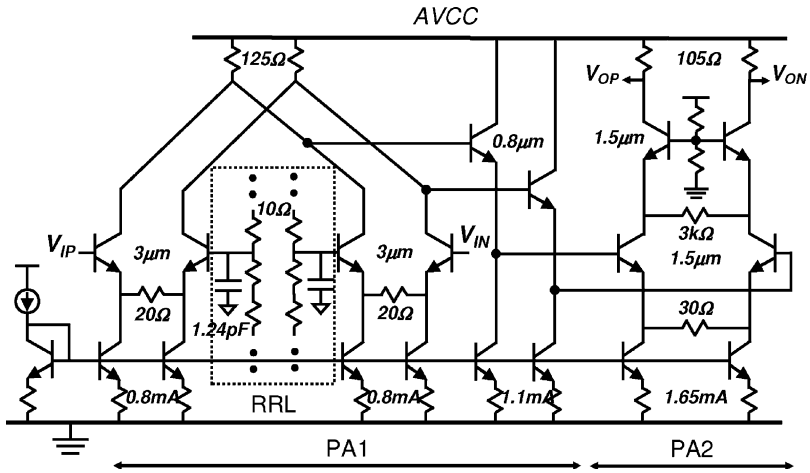


Fig. 10. Schematic of two-stage preamplifiers. The RRL denotes the reference resistive ladder.

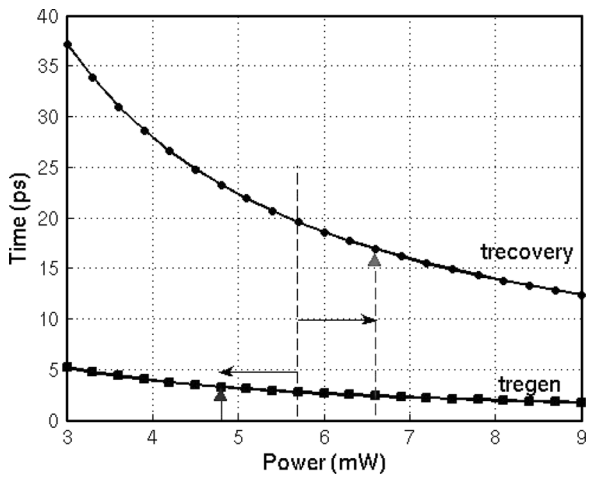


Fig. 11. Comparison of recovery time and regeneration time constant with respect to power dissipation.

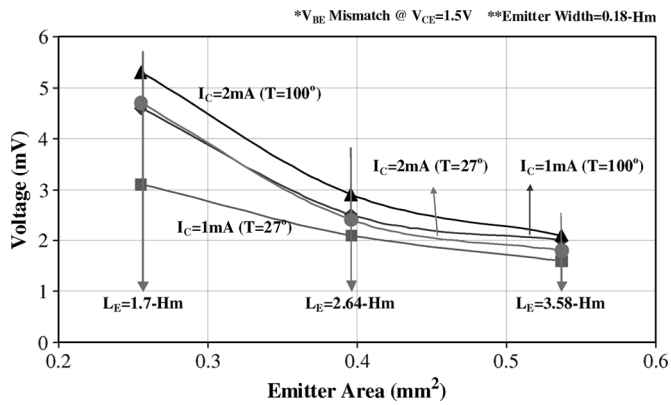


Fig. 12. Estimation of HBT offset voltage.

where I_{EL} denotes the operating current of the latch. The regeneration time constant is usually much shorter than the recovery time and is not the key factor governing the speed–power tradeoff. At room temperature for $V_{\mathrm{Logic}} = 300$ mV, $\Delta v = 1/4$ LSB, and $G_{\mathrm{PA}} = 17$ dB, Fig. 11 demonstrates the dependence of the two speed parameters on their power dissipation. The recovery time is seven to eight times longer than the estimated regeneration time constant, and the current required for overdrive recovery is much larger than that needed for sufficiently fast regeneration amplification. The bias-weighted comparator permits the operating current I_{EA} of the amplifier and the current I_{EL} of the latching circuit to be individually designed. In the proposed topology, the bias current of the amplification ($I_{\mathrm{EA}} = 2.2$ mA) is emphasized over that of the latch ($I_{\mathrm{EL}} = 1.6$ mA) to suppress random offset and probability metastability, as well as to reduce the overall comparator power dissipation. The regeneration time constant is estimated to be 4.2 ps, and it is mainly determined by the device cutoff frequency. The third comparator (C3) entails a bubble error correction function and incorporated with the bias-weighted comparator, guarantees a metastable error rate of less than 10^{-10} at 20 GS/s.

Without any offset compensation techniques in this ADC, care is taken to choose the physical dimensions of the input transistors to guarantee a 3σ offset of less than 0.2 LSB. Fig. 12 shows the estimated offset voltage versus emitter area based on the intrinsic base–emitter voltage matching with respect to collector current and temperature. The offset voltage is approximately 2 mV with an emitter area of 0.45 μm^2, corresponding to an emitter length of 3.0 μm with a minimum emitter width of 0.18 μm. The dimensions of the rest of the transistors are chosen to be small (with an emitter length of 1.0 μm) for high-speed operation.

B. Digital Encoder and Clock Distribution

Because the routing of 31 differential thermometer output traces from the comparator to the Gray encoder is the most complicated step, significant attention is paid to layout design. Balanced differential microstrip lines with a balanced source termination are used for interconnect with M6 (Zo $= 75\,\Omega$ with 3-μm width) over the M1 ground plan. M5 is used for routing bridges. The 31 transmission line drivers are arranged just after the last comparator (C3) to drive the transmission lines with lengths of approximately 1000 μm.

The clock distribution is the most important factor to account for sampling jitter. In order to achieve low-noise clock distribution, a tree-based clock distribution network is constructed, as shown in Fig. 13, with the 75-Ω balanced microstrip line

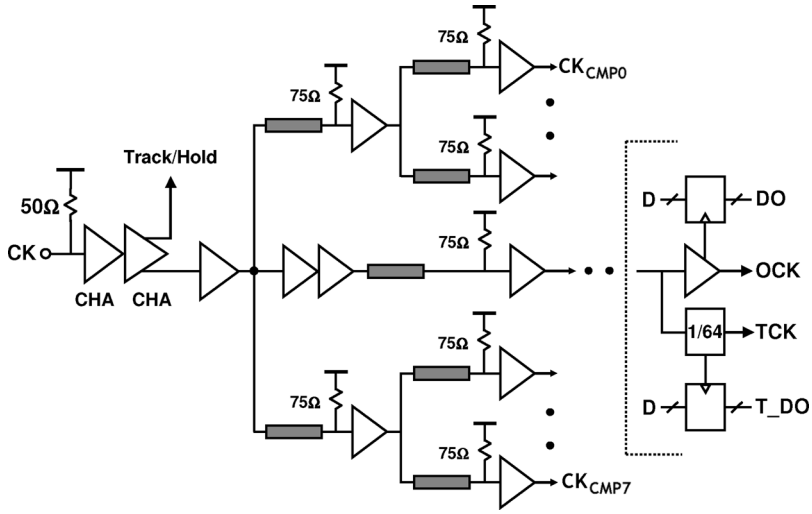


Fig. 13. Clock distribution. CHA denotes a Cherry-Hooper Amplifier.

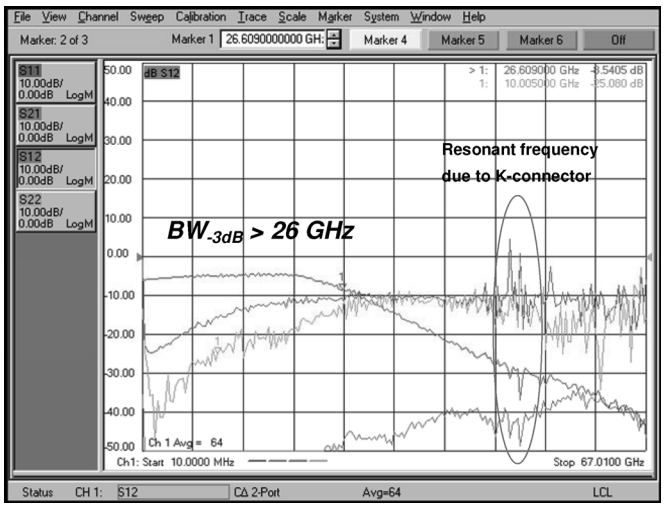


Fig. 14. **S**-parameter measurements of the THA.

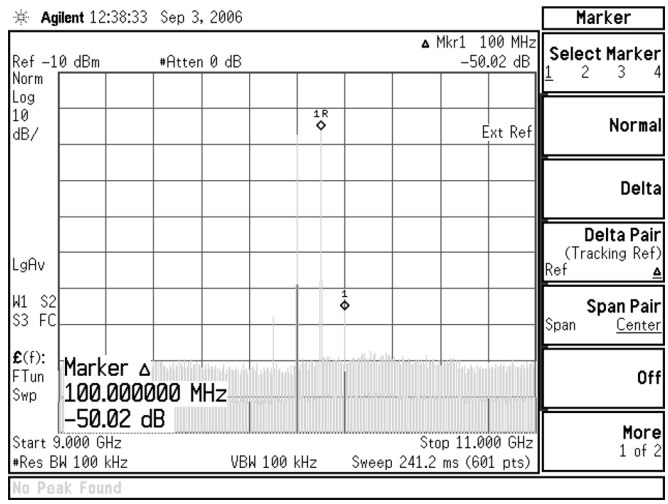


Fig. 15. Two-tone intermodulation test with two input signals at 10 GHz and 10.1 GHz with an input power of −6 dBm.

to reduce clock jitter. A two-stage Cherry-Hooper-based clock buffer with 50-Ω input termination can simultaneously provide adequate bandwidth and gain: 20-dB gain and 28-GHz bandwidth with a bit of peaking. The eight local clock drivers are designed based on the cascode differential amplifier + emitter follower configuration to drive 31 comparator arrays, i.e., four comparator arrays per a clock driver. In order to relax the speed constraints on the timing alignment of the pipelined encoder circuitry, a string of clock buffers is added to create delays for correct timing of the D-FFs. A test mode is included, so that the binary-encoded digital data rate is decimated by $64(= f_S/64)$ to enable easy acquisition by a logic analyzer.

V. Measurement Results

Along with the ADC prototype, a separate test chip was fabricated for testing a distortion-compensated THA. On-wafer probe testing was carried out using 150-μm pitch probes. Two supply voltages are used: 4 V $(HVCC)$ for the front-end THA and 3 V $(AVCC)$ for the output buffer. At the clock frequency of 24 GHz, the THA power dissipation is 280 mW. The S-parameter data are measured with an Agilent 67 GHz network analyzer, as shown in Fig. 14. The small-signal bandwidth (S21) in track mode exceeds 25 GHz with a flat passband gain of −4.8 dB (single-ended measurements). The measured input return loss S11 is well below −10 dB up to 45 GHz. Two-tone intermodulation tests are performed with 10 GHz and 10.1 GHz at the input power of −6 dBm. Fig. 15 shows the measured third-order intermodulation distortion of about −50 dB below the fundamental. The THA exhibits an input IP3 of 24 dBm, so, from the input referred noise power of −48 dBm, the SFDR is calculated to be 48 dBc. The spectral characteristic of the beat frequency test during track-to-hold mode is performed with a 20-GHz input signal and a beat frequency of 1 MHz. Fig. 16 shows the measured results of the third-order harmonic distortion to be better than −43.3 dB at the input power of 0 dBm.

The measurement results show the advantages of the global shunt feedback incorporated with feedforward compensation THA. It achieves a 3.4-dB gain of track-mode dynamic range and a 7.2-dB gain of track-to-hold mode dynamic range over the open-loop counterpart.

The ADC was fabricated in 0.18-μm SiGe BiCMOS. The chip occupies a 2.63×3.3 mm^2 silicon area with an active

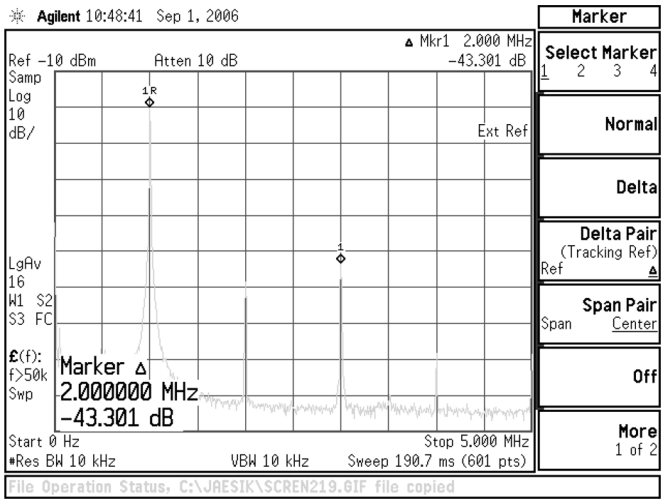
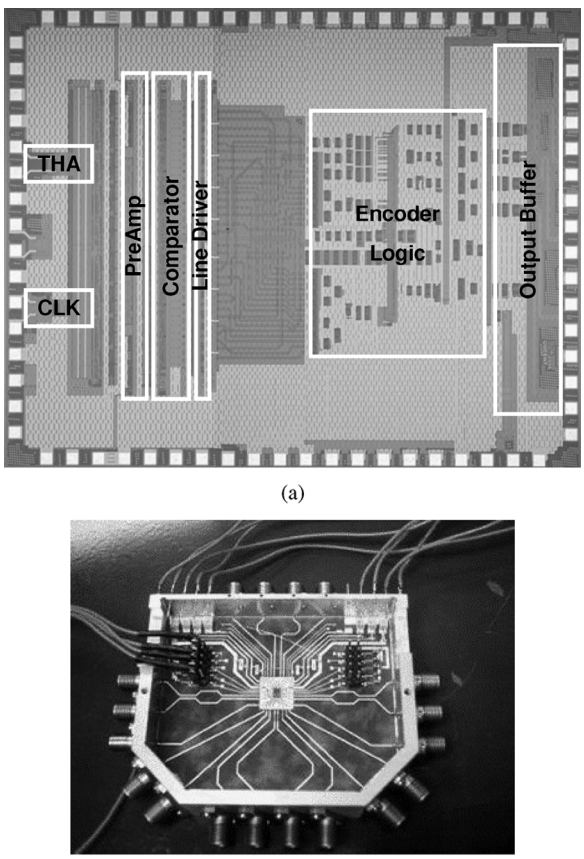


Fig. 16. Beat frequency test at track-to-hold mode with an input signal at 20 GHz and the beat frequency of 1 MHz with an input power of 0 dBm.



(a)

(b)

Fig. 17. (a) ADC and (b) its package.

area of 1.8×2.8 mm^2. The ADC microphotograph and its package are shown in Fig. 17. It is packaged in a customized gold housing package with SMA and K-connectors. Then, the chip is mounted on the metal plate through a window in the alumina ceramic substrate using conductive epoxy glue for high thermal dissipation. There are two power supplies used for the analog building blocks ($AVCC = 3$ V) and the digital parts ($DVCC = 3$ V). Forty-four of the 72 bonding pads are dedicated to the power and ground networks to supply sufficient current with low bondwire inductance. At the clock frequency

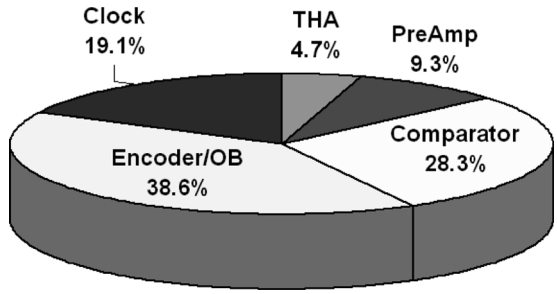


Fig. 18. Power breakdown of the ADC.

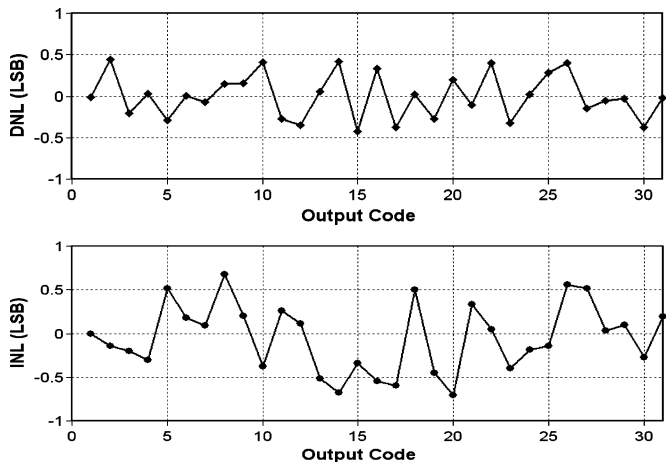


Fig. 19. Measured (a) DNL and (b) INL at 20 GS/s.

of 20 GHz, power dissipation is 3.24 W. Fig. 18 illustrates the power dissipation breakdown of the ADC. While the backend block including encoder logic, output buffers, and transmission line drivers consumes 1.25 W, the comparator consumes less than 0.92 W. The large power consumption of the encoder logic is mainly attributed to the large number of synchronization circuits along the data and clock distribution network for seeking precise sampling time. The power dissipation of the clock is 620 mW (∼19% of the total ADC power consumption), which is increased to support 20-GS/s conversion operation with 270-mVpp signal swing average.

Fig. 19 shows the measured static linearity of DNL and integral nonlinearity (INL) at 20 GS/s, where the peak DNL is 0.43 LSB and the peak INL is 0.7 LSB, respectively. The low DNL results from double interpolation topology, whereas the high INL is due to the nonlinearities in the sampling circuit and in the resistive reference ladder. Fig. 20 shows the output spectra measured with a 1.0-Vp-p input sinusoid at 1008.8 MHz using a sampling frequency of 16 GS/s. With the 64 × decimated ADC output ($f_O = 250$ MHz), the fundamental spectrum is observed at $f_{\rm IN} - 4 * f_O = 8.8$ MHz. The SFDR of 36 dBc and signal-to-noise-plus-distortion ratio (SNDR) of 28.6 dB are measured, so the effective number of bit (ENOB) is 4.5 bits. Fig. 21 shows the measured SFDR and SNDR over analog input frequencies at the sampling rate of 20 GS/s. The ERBW where the SNDR drops 3 dB from its low frequency value is 7 GHz, which is suitable for target applications, such as the 40-Gb/s coherent QPSK receiver. The figure of merit (FoM) $=$ Power$/(2^{\rm ENOB} * 2 *$ ERBW) is 9.54 pJ/conversion-step. The SNDR at Nyquist frequency ($\sim f_S/2$) versus

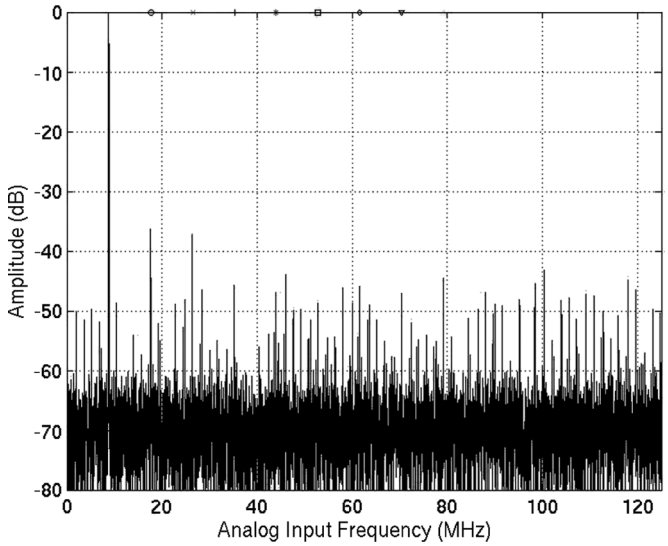


Fig. 20. Output spectrum measured at 1008.8-MHz input signal frequency. The sample rate is 16 GS/s with 1/64 decimation (16384 FFT).

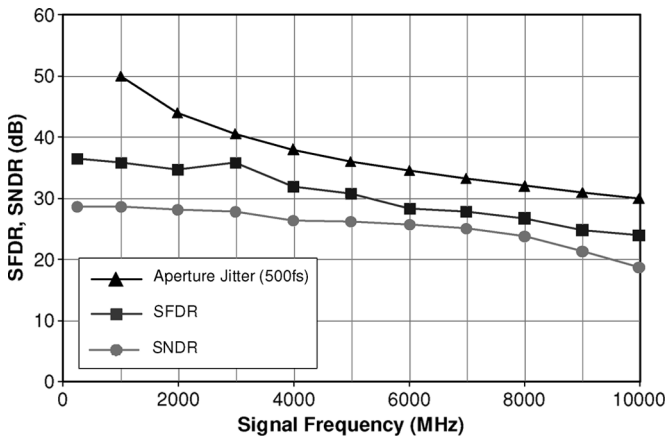


Fig. 21. Measured SNDR and SFDR versus analog input frequency at f_S = 20 GS/s.

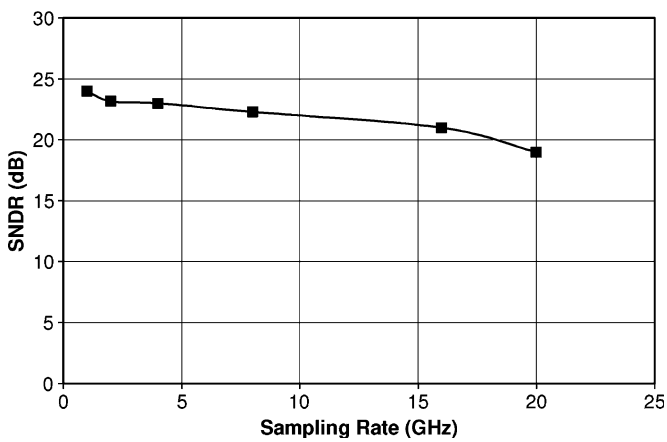


Fig. 22. Measured SNDR versus sampling frequency f_S at Nyquist frequency $\sim f_S/2$.

sampling frequency is illustrated in Fig. 22. The SNDR is better than 24 dB at 1 GS/s, but it is degraded to 19 dB at 20 GS/s. The SNDR degradation at high input frequencies is dominated by the following:

1) signal-frequency-dependent spurious tones at THA output;
2) aperture jitter limitation including external clock jitter (approximately 500 fs) and internal clock distribution and thermal jitter;
3) timing misalignment at the encoder logic;
4) increasing second harmonic distortion, which may come from the single-ended output measurement and the phase error from a 180° hybrid coupler used for differential input at the test setup.

TABLE II
PERFORMANCE SUMMARY

	5-bit 20-GS/s ADC
Input Frequency (f_{in})	> 10 GHz
Sampling Frequency (f_S)	> 20 GS/s
DNL/INL	+/- 0.43 / 0.7 LSB
SNDR at f_{in} = 1 GHz	28.6 dB
SNDR at f_{in} = 7 GHz	25.3 dB
SFDR at f_{in} = 1 GHz	36 dB
Effective Resolution Bandwidth	7.0 GHz
Timing Jitter (RMS)	< 500 fs (RMS)
Power Dissipation (at f_S=20GS/s)	3.24 W
Figure of Merit (FoM)	9.54 pJ
Technology	SiGe 0.18-µm BiCMOS

TABLE III
COMPARISON TO STATE-OF-THE-ART ADCS

Papers	Technology	Bits (bits)	$f_{(sample)}$ (Sample/s)	ENOB (bits)	Power (W)	ERBW (GHz)	FoM (pJ/c.s.)
[3]	CMOS	8	20G	6.5	10	2	27.6
[5]	SiGe	5	10G	4.1	3.6	2.2	47.7
[7]	SiGe	5	22G	4.7	3	4.6	10.2
[4]	CMOS	6	24G	5.5	1.2	6.4	2.1
[8]	SiGe	5	35G	4.6	4.8	4.5	22
This work	SiGe	5	20G	4.5	3.24	7	9.54

Table II summarizes the performance. Table III shows the performance comparison between this ADC and prior arts. This ADC achieves the best ERBW and high power efficiency.

VI. CONCLUSION

For 10-GBd 40-Gb/s coherent QPSK receivers, a framework of the required ADC performance has been given. This work has highlighted the superior capability of the ADC with respect to sampling frequency, resolution bandwidth, and power efficiency. The linearity-assisted THA and the bias-weighted comparator has simultaneously achieved the best resolution bandwidth of 7 GHz and the maximum sampling frequency over 20 GS/s. The power dissipation of 3.24 W is a bit higher than the design target, due to the power consumption from the multiple transmission line drivers and clock buffers used for timing synchronization. The FoM of 9.54 pJ/conversion-step, however, is

the best energy efficiency over the prior arts. This ADC potentially expands the range of applications in which a high sampling rate is desired, including, in a wideband data acquisition system, a fast digital oscilloscope, a millimeter-wave radio, and electronic warfare systems.

ACKNOWLEDGMENT

The authors would like to thank P. Roux of Bell Labs for his support in the packaging and Dr. A. Leven and Dr. N. Kaneda of Bell Labs for the valuable discussions on the coherent optical system.

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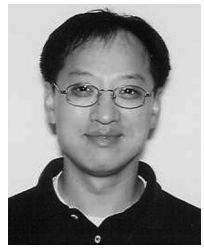

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