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A 5-bit 3.2-GS/s Flash ADC With a Digital Offset Calibration Scheme

Ying-Zu Lin, Cheng-Wu Lin, and Soon-Jyh Chang

***Abstract*—In high-speed Flash analog-to-digital converters (ADCs), preamplifiers are often placed in front of a comparator to reduce metastability errors and enhance comparison speed. The accuracy of a Flash ADC is mainly limited by the random offsets of preamplifiers and comparators. This paper presents a 5-b Flash ADC with a digital random offset calibration scheme. For calibration, programmable resistive devices are used as the loading devices of the second-stage preamplifiers. By adjusting the calibration resistors, the input-referred offset voltage of each comparator is reduced to be less than 1/2 LSB. Fabricated in a 0.13-μm CMOS process, experimental results show that the ADC consumes 120 mW from a 1.2-V supply and occupies a 0.18-mm^2 active area. After calibration, the peak differential non-linearity (DNL) and integral non-linearity (INL) are 0.24 and 0.39 LSB, respectively. At 3.2-GS/s operation, the effective number of bits is 4.54 b, and the effective resolution bandwidth is 600 MHz. This ADC achieves figures of merit of 3.07 and 4.30 pJ/conversion-step at 2 and 3.2 GS/s, respectively.**

***Index Terms*—Digital calibration, digitally assisted analog-to-digital converter (ADC), Flash ADC, high-speed data converter, offset calibration.**

I. Introduction

Low-resolution gigasample/second analog-to-digital converters (ADCs) are extensively used in recent communication applications. In a receiver, an ADC converts RF or intermediate-frequency signals into digital codes for baseband processing. A Flash ADC is often utilized in such applications, owing to its high-speed potential and low latency. The accuracy of Flash ADCs is mainly limited by the offsets of the preamplifiers and comparators [1]. Offsets can be categorized as systematic, random, and dynamic offsets. A systematic offset occurs due to improper architecture or circuit design. Its quantity is predictable during the design stage. Process variations during fabrication phases lead to the generation of random offsets. A dynamic offset is associated with the regenerative latch in a comparator. Preamplifiers are often placed in front of a latch-based comparator to suppress dynamic offsets and mitigate kick-back noises. The preamplifiers and comparators, however, contribute random offsets. Enlarging device sizes reduces the random offset since the quantity of the offset voltage is inversely proportional to the square root of the transistor size. However, large-size devices limit the bandwidth of an amplifier and consume larger power. The resistive averaging network is a popular technique for offset reduction. The averaging technique neutralizes random offsets by connecting adjacent preamplifiers together. The output of an averaged preamplifier is not only defined by itself but also by all the preamplifiers nearby. The resistive averaging network has been proven a useful technique for linearity enhancement but requires extra dummy preamplifiers to maintain boundary conditions [2]. As a result, there is a tradeoff between power consumption and averaging efficiency. Calibration techniques are alternative solutions for offset reduction [3]–[7]. In addition to an ADC core, extra circuits are introduced to perform calibration for preamplifiers or comparators.

Digital-to-analog converters (DACs) are utilized in a 4-b 4-GS/s Flash ADC to trim the output voltages of the comparators [4]. However, these DACs induce extra capacitive loading to the comparators. A 4-b 1.25-GS/s Flash ADC uses programmable capacitor arrays to perform offset calibration [5]. The capacitor arrays also contribute extra loading to the comparators. A 5-b 3.5-GS/s Flash ADC directly trims its reference voltages to cancel the offset [6]. A background offset calibration scheme is proposed in a 6-b 1-GS/s two-step ADC [7]. An auxiliary differential pair helps reduce the offset of the main differential pair. This calibration technique requires a reset phase and is therefore not suitable for conventional continuous-time Flash ADCs. This paper proposes a foreground digital calibration scheme. By adjusting the programmable resistive loading devices of the preamplifiers, the random offsets are reduced.

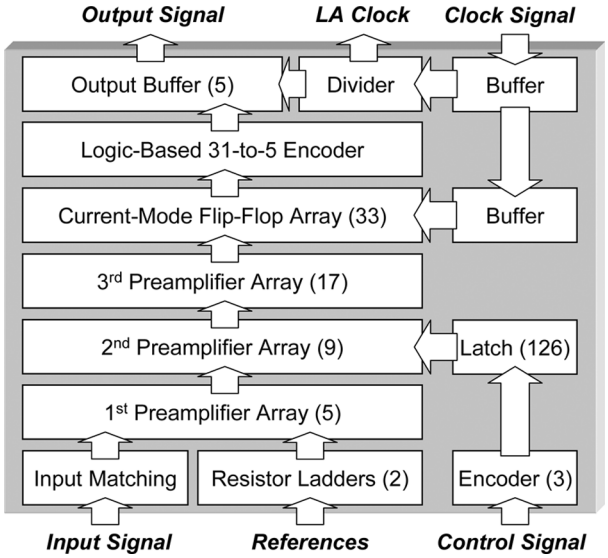

Fig. 1. Simplified block diagram of the proposed ADC.

II. ADC Architecture and Building Blocks

Fig. 1 shows the simplified block diagram of the proposed ADC where *LA Clock* means the trigger signal for the logic analyzer. The ADC architecture mainly follows the design in [8]. This ADC core consists of two reference ladders, three preamplifier arrays, a current-mode flip-flop array, a logic-based 31-to-5 encoder, and digital circuits for offset calibration. For impedance matching, a 100-Ω resistor is connected to the differential input ports to make the amplitude of the input signal stable in the desired frequency range. For measurement, output data of the encoder are sampled by flip-flops clocked at 1/32 sampling frequency.

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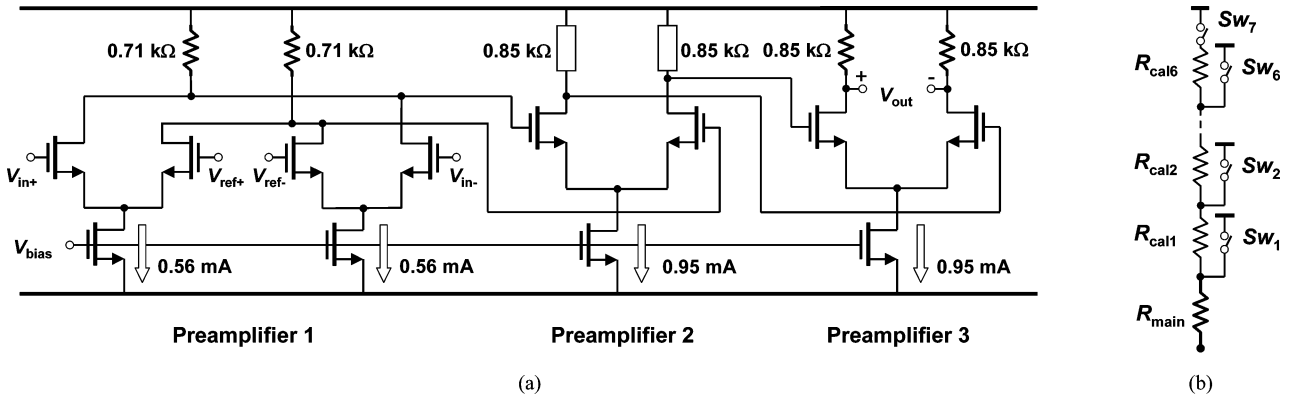

Fig. 2. (a) Employed preamplifiers. (b) Loading device of the second-stage preamplifier.

Preamplifiers are often placed in front of a comparator to reduce metastability errors and suppress dynamic offsets. For high-speed operation, cascaded high-bandwidth preamplifiers provide sufficient gain for input signals. The differential devices in a preamplifier are the sources of random offsets. If the outputs of a preamplifier are connected to the inputs of another preamplifier, the input-referred offset caused by the succeeding stage is reduced by a factor of the gain of the preceding amplifier. If each preamplifier stage is designed to contribute the same offset voltage, the device sizes of the succeeding preamplifiers can be scaled down stage by stage to save power consumption. Fig. 2(a) shows the schematic of the employed preamplifiers. The first four-input preamplifier subtracts the differential input signals from reference voltages and amplifies the difference. The two succeeding cascaded two-input preamplifiers amplify the output signals of the first preamplifier.

According to the aforementioned rule, the preamplifiers in [8] are scaled down stage by stage. In this paper, the transistor sizes of the three preamplifiers are identically small since an offset calibration scheme is used. The calibration in this paper is performed by adjusting the resistive loading devices of the second-stage preamplifiers. Each loading device of a second-stage preamplifier consists of a main resistor ($R_{\rm main}$), six calibration resistors ($R_{\rm cal1}-R_{\rm cal6}$), and seven p-type transistor switches (Sw_1-Sw_7), as shown in Fig. 2(b). The nominal loading resistance (0.85 kΩ) of the second-stage preamplifier, i.e., the resistance in reset state, is the summation of the resistance of the main resistor ($R_{\rm main}$), the resistance of three calibration resistors ($R_{\rm cal1}+R_{\rm cal2}+R_{\rm cal3}$), and the on-resistance of the reset switch (Sw_4). The detailed operation of the calibration circuits is described in Section III.

A current-mode flip-flop is used as the comparator for analog-to-digital conversion up to 3.2 GS/s. The flip-flop is composed of two identical current-mode latches. The flip-flop periodically samples and amplifies their input signals into robust digital voltage levels for the following encoder [8]. Because a conventional ROM-based encoder is not sufficient for 3.2-GS/s operation in this process, a current-mode logic-based encoder is utilized instead. The encoder is very compact since it consists of only 26 logic gates. Moreover, there is only one kind of logic gate in the encoder. To save hardware, the thermometer codes are directly converted to gray codes. Current-mode flip-flops are inserted into the critical paths to pipeline the encoder to make it sufficient for 3.2-GS/s operation.

III. Proposed Calibration Scheme

A. Calibration Procedures and Control Scheme

There is a current-mode flip-flop placed behind each third-stage preamplifier. After the preamplified signal is sampled by a current-mode flip-flop, the analog information is converted into digital form. The calibration is performed in a preamplifier one at a time. Whenever a second-stage preamplifier is selected, the output of its corresponding current-mode flip-flop is detected via a 9-to-1 multiplexer. In this way, the polarity of the offset voltage is observed. In the beginning of the calibration, all the input nodes of the first-stage preamplifiers are connected to $V_{\rm CM}$, and all the second-stage preamplifiers are reset. Ideally, the voltage levels of the two output nodes of a second-stage preamplifier are the same. In practical cases, the two nodes do not possess the same voltage, owing to random offsets. Although the value of the offset is unknown, the polarity can be observed by detecting the output of the corresponding flip-flop. When the initial polarity is detected, the calibration switches are adjusted successively according to the read data until the polarity changes.

In each loading device of the second-stage preamplifier, only one switch transistor is on at a time. In the reset state, reset switch Sw_4 is on, and the other switches are off. Static latches are connected to all the switches to hold the calibration information, on or off. Three binary to one-of- n code encoders are employed to realize the control scheme. The selection of the calibrated preamplifier is controlled by a 4-to-9 encoder, and the selection of the switch is controlled by two 3-to-7 encoders. The control signals of the three encoders are given externally. All the calibration procedures are controlled by an off-chip microcontroller.

B. Design Considerations of the Calibration Circuits

The maximum value of the input-referred offset voltage after calibration is determined by the quantity of the calibration resistance. The change of the input-referred offset by each calibration step is

$$\Delta V_{\rm cal} = (0.5 I_{\rm bias} \times R_{\rm cal})/A_1 A_2 \tag{1}$$

where $I_{\rm bias}$ is the bias current of the second-stage preamplifier, $R_{\rm cal}$ is the resistance of each calibration resistor, and $A_{1,2}$ are the gains of the first- and second-stage preamplifiers. Among all kinds of mismatches, the threshold voltage mismatch dominates. The standard deviation of the offset voltage induced by the threshold voltage mismatch is

$$\sigma(\Delta V_{\rm th}) = \frac{A_{V\rm th}}{\sqrt{WL}} \tag{2}$$

where $A_{V\rm th}$ is a process-dependent parameter which is generally a value around 5 mV $\cdot$ μm in a 0.13-μm CMOS process. In this design, the length and width of the input transistors of all the preamplifiers and flip-flops are 0.13 and 7.5 μm, respectively. Replacing the device sizes into (2), the standard deviation of the offset voltage in this design is 5.06 mV. In the proposed ADC, the reference ladders, preamplifiers, and current-mode flip-flops contribute random offsets.

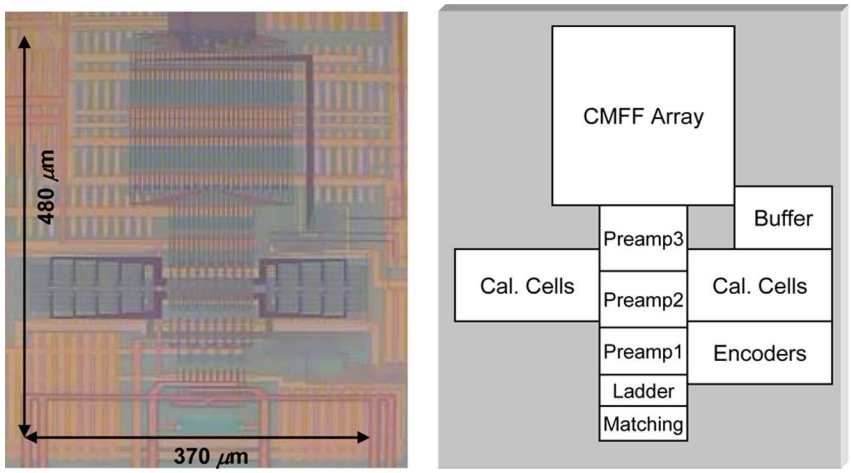

Fig. 3. (Left) Chip micrograph and (right) floorplan of the major part.

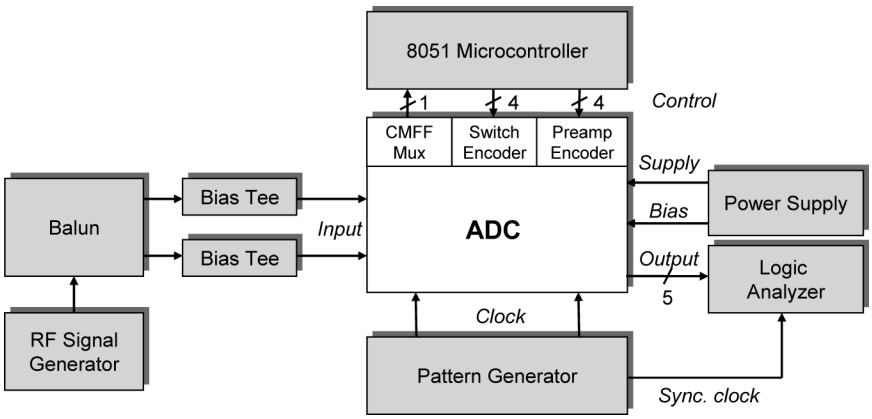

Fig. 4. Measurement setup.

The offsets induced by the ladders are reduced by layout techniques and therefore negligible. The value of $\sigma(\Delta V_{\rm th})$ of the second- and third-stage preamplifiers is 5.06 mV. Assuming that the mismatches of the two input pairs in a first-stage preamplifier are mutually independent, the resultant $\sigma(\Delta V_{\rm th})$ is 7.16 mV. The gain of the first-stage preamplifier is 1.6 V/V, and that of the second- and third-stage ones is 2.8 V/V. The input-referred offsets contributed by the second-stage preamplifier, third-stage preamplifier, and flip-flop are 3.16, 1.13, and 0.4 mV, respectively. Assume that all the preamplifiers are independent, and then, the overall input-referred $\sigma(\Delta V_{\rm th})$ is 7.92 mV where the first- and second-stage preamplifiers contribute 98.82% of the offset. Because the input-referred random offsets induced by the third-stage preamplifiers and flip-flops are relatively small, calibration is performed in the second-stage preamplifiers. In this case, only nine second-stage preamplifiers are calibrated, instead of 17 third-stage preamplifiers or 33 comparators. Performing calibration in third-stage amplifiers or comparators causes larger overheads including die area, routing effort, and control complexity. Although some of the third-stage preamplifiers and flip-flops are not calibrated, the proposed calibration scheme is still capable of enhancing the accuracy of the ADC to the required level.

To guarantee 99.7% (3-σ) of fabrication yield, this ADC has to cancel a maximum offset voltage up to 23.75 mV, three times the overall input-referred $\sigma(\Delta V_{\rm th})$. One LSB of the ADC is 13.3 mV. To limit the maximum error after calibration to less than 1/2 LSB, each calibration step must be less than 6.7 mV. The condition where the maximum voltage difference occurs is that Sw_1 turns on in one loading device and Sw_7 turns on in the other one. The maximum difference is the summation of the voltage drop of six calibration resistors. In this paper, a calibration resistor is designed to provide an input-referred voltage step around 4 mV. Since the resultant maximum calibration

TABLE I
SPECIFICATION SUMMARY

Specification (Unit)	Experimental Result	
Supply Voltage (V)	1.2	
Input CM Voltage (V)	0.8	
Input Range (V_{pp})	0.4	
DNL (LSB)	+0.18 / -0.24	
INL (LSB)	+0.39 / -0.29	
Power (mW)	120	
Sampling Rate (GS/s)	2.0	3.2
ENOB (bit)	4.44	4.54
ERBW (MHz)	900	600
FOM (pJ/conv.-step)	3.07	4.30
Input Capacitance (fF)	95	
Active Area (mm^2)	0.18	
Resolution (bit)	5	
Technology	TSMC 0.13μm CMOS	

TABLE II
COMPARISON OF STATE-OF-THE-ART 5-b FLASH ADCS

	ESSCIRC'06 [9]	*CICC*'06 [6]	*CICC*'07 [8]		Proposed	
Supply (V)	1.2	1.4	1.2		1.2	
Power (mW)	46	227	180		120	
Sampling Rate (GS/s)	1	3.5	3.2	4.2	2	3.2
ENOB (bit)	4.73	4.28	4.44	4.20	4.44	4.54
ERBW (MHz)	470	< 1000	1650	1750	900	600
FOM (pJ/conv.-step)	1.8	5.84	2.51	2.80	3.07	4.30
Active Area (mm^2)	0.20	0.66	0.16		0.18	
Calibration	No	Yes	No		Yes	
Technology (nm)	130	90	130		130	

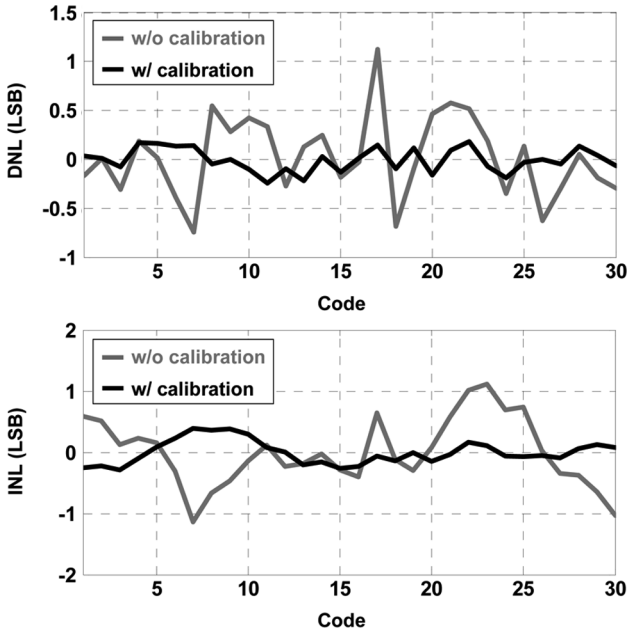

Fig. 5. Measured DNL and INL (black) with and (gray) without calibration.

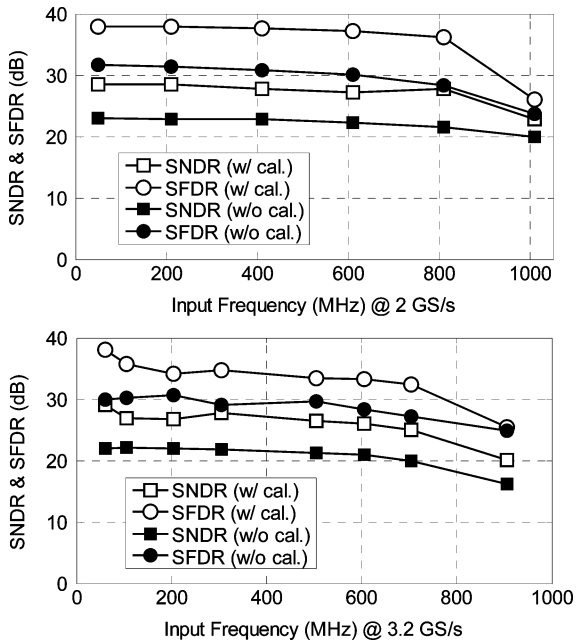

Fig. 6. SNDR and SFDR versus input frequency at 2 and 3.2 GS/s.

range is 24 mV, the six calibration resistors have to provide an output voltage difference of 108 mV. The bias current of the second-stage preamplifier is 0.95 mA. Therefore, the resistance of each calibration resistor is 38 Ω. Considering other minor sources of mismatches, including transistor current factor β and resistor mismatch, a larger value of 40 Ω is used.

IV. EXPERIMENTAL RESULTS

The proposed ADC is fabricated in a TSMC 0.13-μm 1P8M CMOS process. The chip micrograph and floorplan of the major part are shown in Fig. 3. The occupied active area is 0.18 mm^2. If the calibration control circuits are integrated on chip, a 7755-μm^2 extra die area is required. Excluding output buffers, this ADC consumes an average power of 120 mW from a 1.2-V supply voltage. The bare die is directly mounted on a printed circuit board (PCB), and the pads of the die are connected to the traces of the PCB through bonding wires. The measurement setup is shown in Fig. 4. A pattern generator Agilent 81250 is used to provide differential clock signals up to 3.2 GHz. An RF signal generator Agilent E4438C provides single-ended sinusoidal signals which are then converted into differential ones by an RF transformer. Two bias tees bias the differential signals to the designated input common-mode voltage, 0.8 V. The calibration processes are controlled by an off-chip 8051 microcontroller. Fig. 5 shows the measured DNL and INL with and without calibration. Before calibration, the peak DNL and INL are 1.12 and 1.13 LSB, respectively. After calibration, the peak DNL and INL are 0.24 and 0.39 LSB, respectively. Fig. 6 shows the measured signal-to-noise-plus-distortion ratio (SNDR) and spurious-free dynamic range (SFDR) at 2 and 3.2 GS/s with and without calibration. This ADC achieves figures of merit of 3.07 and 4.30 pJ/conversion-step at 2 and 3.2 GS/s, respectively.

The specifications and experimental results are summarized in Table I. Table II shows the comparison of the proposed ADC to other state-of-the-art 5-b Flash ADCs. The table shows that the proposed ADC has the smallest power consumption compared with the other two over 3-GS/s Flash ADCs. The calibration circuits only occupy little area, around 0.03 mm^2. The architecture of the proposed ADC is

similar to that in [8]. The main differences are that the track-and-hold amplifier (THA) is removed and some calibration circuits are added in the proposed work. The preamplifiers in [8] are scaled down stage by stage while only one small-size preamplifier is used in this work. Compared with that in [8], 1/3 of the power consumption, 60 mW, is saved due to the removal of the THA (12 mW) and the utilization of small preamplifiers (22 mW) and flip-flops (26 mW). The experimental result shows that the input 3-dB bandwidth is only 650 MHz at 3.2 GS/s. The reduction of the input bandwidth is mainly caused by the removal of the THA.

V. Conclusion

A 5-b Flash ADC with a sampling rate of up to 3.2 GS/s is proposed. The accuracy of this Flash ADC is enhanced by a digital calibration scheme. This paper has demonstrated the effectiveness of the calibration scheme. Compared with the published calibration schemes, the proposed one does not limit the bandwidth of the calibrated preamplifier and comparator.

Acknowledgment

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