3 GS/s 7 GHz BW 12 Bit MuxDAC for Direct Microwave Signal Generation over L, S or C Bands

François Boré, Marc Wingender, Nicolas Chantier, Andrew Glascott-Jones, Emmanuel Dumaine, Carine Lambert, Sergio Calais
HiRel Semiconductor Solutions
e2v
Saint-Egrève, France
francois.bore@e2v.com, marc.wingender@e2v.com, nicolas.chantier@e2v.com, andrew.glascott-jones@e2v.com

Abstract— **In advanced applications such as digital radar, frequency hopping encryption data links, Micro-Wave Waveform Design Systems, Ultra Wide Bandwidth communications and software defined radio, the need for instantaneous bandwidth often drives system design decisions. The availability of powerful signal processors able to handle broadband signal vectors is not an issue anymore; the bottleneck is now the availability of high sampling rate and high linearity data converters, ADC (Analogue to Digital Converter) for reception and DAC (Digital to Analogue Converter) for transmission. Access to high speed data converters enabling up and down conversion directly in the L Band, S Band and C Band will allow system architects to operate in the digital world ever closer to the antenna, thus simplifying drastically receiver or transmitter architecture by removing costly Intermediate Frequency stages. Broadband DAC's are key enabling components which open up new design opportunities for direct digital Synthesizer systems.**

In this regard, this paper describes an innovative multimode 12 Bit 3GS/s MuxDAC, offering 46ps full swing rise time (that is 7.5 GHz analogue output bandwidth), based on a 200 GHz SiGeC bipolar Technology, which enables direct micro wave signal generation of up to 1.2 GHz width arbitrary waveforms directly in the high IF (L S or C Band) region closer to the Antenna.

Beyond system and DAC design considerations this paper includes extended capability measurement performed on silicon. This DAC is turning Software Defined Micro-Wave or Direct Micro-Wave Synthesis (DMWS) from pure concept into proven reality up to C-Band.

Keywords-components: Development of next-generation broadband flexible radar systems; Increased sampling rates, bandwidth and resolution; Expanded output frequency spectra and update rates; Broadband instantaneous frequency generation; Waveform Design; Software Defined Microwave; Direct digital synthesizing of arbitrary UWB signals in L Band , S Band or C Band.

I. INTRODUCTION

High speed DACs featuring a good linearity over a wide frequency range are key components for new generations of broadband RF Radar transceivers. In this regard, a new generation of Ultra Wide Band DAC circuitries based on Infineon's B7HF200 200 GHz SiGeC (Silicon Germanium Carbon) fully bipolar Technology [1] has been designed to address both industrial applications and next-generation of broadband flexible radar and countermeasure systems as well as space-borne electronics.

This paper introduces a new multimode Ultra Wide band DAC, which can be considered as the second generation of the 12bit 3Gsps DAC demonstrator [2], this new DAC is meant to be a product over extended temperature range.

The demonstrator has been designed and fabricated on a 200 GHz cut off frequency HBT SiGeC process, and fully characterized. Considering these first results the CNES (Centre National d'Etude Spatiale, the French Space Agency) has significantly supported the development of a new circuit with extended features and functionalities and targeting also extended performances.

This new product has been designed and fabricated on the same process, and has undergone thorough characterization in two different packages (ceramic CI-CGA255 for applications requiring hermetic package, and organic FpBGA196 for other applications where cost is more an issue).

This circuit is setting new standards of high dymanic range performances over L, S and C bands through the combination of the following innovations:

- The introduction of innovative output modes bypassing the limits of sinc(Fout/Fclock) found in most DACs, and extending significantly DAC linearity (patents pending).
- Architectural breakthrough (patents pending) minimizing C and L parasitics on critical nodes, thus allowing an extension of DAC usable output bandwidth up to 7GHz.

In its ceramic package, this new device is currently going through an ESCC evaluation (space qualification level according to European Space Agency standards).

II. TRANSMITTER ARCHITECTURE CONSIDERATION

A. Transmitter Systems Architecture simplifications

Zero IF or single IF architecture for transmitter was for a long time a pure concept, but for practical reasons (insufficient cost effective computation power, unavailability of UWB DAC) system architects and system designers were obliged to stick to the current concept, that is channeling and synthesis in base-band (narrow band approach), two or three stages of up-conversion with all the associated analogue difficulties. This means significant complexity for the system and especially for the analogue and RF part with many local oscillators and a lot of analogue filtering and almost no flexibility at system level.

The availability of cost effective powerful DSP is not an issue anymore, and the last road block to true broadband software defined radio or waveform engineering is now lying in the

availability and Ultra Wide Band (UWB) and high dynamic range DAC.

Direct IF synthesis allows I-Q modulated signal to be directly synthesized in a single modulated IF output (Fig. 1). This avoids the distortion issues that external analogue vector modulator may introduce. Digitally Summing I and Q channels gives excellent amplitude and phase matching with ideal symbol timing. Direct RF synthesis eliminates the need for external components for up converting the IF signal to an RF frequency. As a consequence direct UWB synthesis in the high IF region (L-Band, S-Band or even C-Band) offers more versatility together with size, power, weight and cost reductions of the transmitter system [3], provided a high performance ultra wide band DAC is available

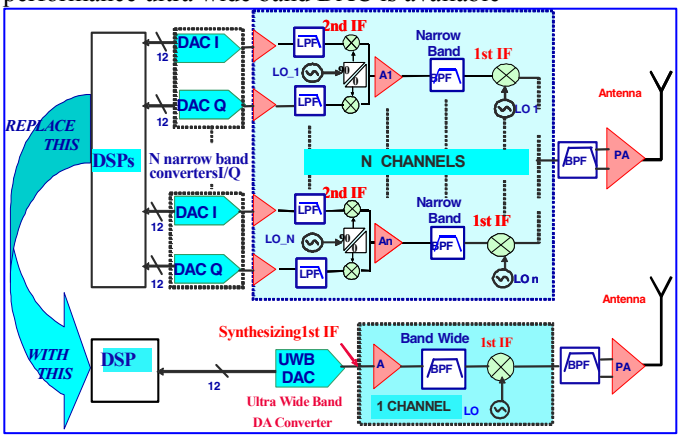

Figure 1. Typical Transmitter Architecture Improvement

Direct Digital Synthesis (DDS) is a requirement for arbitrary waveform generator, with bandwidths generation capability of up to 1GHz in the high IF region. DDS allows easier discrimination of targets and increased number of waveform. Compared to Phase Locked Loop based synthesizers, benefits of DDS include immediate frequency hopping, continuous phase and flexibility provided by Digital signal processing.

The receiving path issues (availability of ADCs and DSPs) have been addressed with more or less success by different vendors in the last past years, and until now the limiting factor to true full duplex Ultra Wide Band Software Defined Radio was the availability of ad hoc DACs.

Architectural breakthroughs combined with the 200GHz cut-off frequency of the SiGeC (Silicon Germanium Carbon) technology allow for enhanced linearity and noise performance of the DAC with conversion rate of 3GS/s, together with multi Nyquist operation.

B. DAC requirement for such a system

Beyond the pure performance considerations, in order to be able to build a cost effective system, an Ultra Wide Band DAC should embed some specific features to address the following issues:

- How to generate a broadband pattern with the DAC?
- How to extend functionality up to or beyond the end of the 3rd Nyquist Zone?
- How to maintain spectral purity at high sampling rate?
- How to synchronize easily the DAC with the DSP or the FPGA steering data?

To address the first point, a high sampling rate is mandatory, since under sampling and spectrum periodicity allows only for narrow band operations. High sampling rate requires data throughput not compatible on a single channel approach with cost effective DSP or FPGA (yet in a near future the use of a few synchronized High Speed Serial Links [HSSL] can be envisioned, with appropriate process for the DAC), this is why we have chosen the a 4:1 LVDS compatible MUX DAC approach.

To address the second point, the DAC must embed features allowing overcoming the sinc(x) roll-off by the introduction of new output modes beyond the "classical" Non Return to Zero mode. To take benefits from these new modes the DAC output bandwidth must be extended as much as possible.

To address the third point, mechanisms at stake in the degradation of spectral purity of a DAC must be carefully reviewed and understood before the design (and even the specification) of the DAC.

III. DAC Architecture Overview

A. Overview common to the new product and the demonstrator

The DAC presented in this paper is the next generation of the DAC presented at MIKON (Vilnius June 14th-16th 2010) referred to as the demonstrator. Yet both circuits are based on the same architecture, the implementation of said architecture into the new circuit has led to strongly different choices.

Both circuits are based on a 4 to 1 Multiplexer and a 12 bit current steering DAC, segmented for the most significant bits (MSB) and binary weighted for the least significant bits (LSB), the binary weighted structure being implemented by means of a R2R structure.

The DAC is based on a single core architecture, and do not rely on internal interleaved core DACs to achieve 3GS/s. Hence, the DAC does not require any calibration before or during operation over temperature as sometimes required with interleaved multi-cores architectures.

The DAC features a Return To Zero (RTZ) mode for operation in the 2nd and 3rd Nyquist zones, enabling direct digital synthesis of UWB arbitrary waveforms directly in the high IF region (S_Band).

B. Performance enabling SiGeC Technology

The DAC is based on innovative architecture concepts applied of Infineon's B7HF200 SiGeC HBT bipolar technology. The DAC performance is allowed by the combination of the architecture and the technology.

The technology features deep trench vertical isolated bipolar NPN transistors enabling peak cut-off frequency (f_T) of 200 GHz for low current densities, with 4 levels of Copper metal for very low interconnect parasitics, furthermore this technology displays sufficient matching of device to build a 12 bit DAC without calibration or post process trimming. The 12 Bit 3GS/s 7GHz BW DAC reported in this paper is based on this technology.

Furthermore inherent radiation tolerance property of SiGe HBT [4, 5] makes this process choice particularly relevant for military or space applications.

C. *Evolution regarding the demonstrator*

The design of the new product (fig 2) incorporates new features and functionalities:

- Improved communication with the FPGA, featuring Setup Time Violation Flag and Hold Time Violation Flag.
- Introduction of new output modes: RF and Narrow Return to Zero (NRTZ), in addition to Non Return to Zero (NRZ) and Return To Zero (RTZ)
- Improvement of MUX part to mitigate potential meta-stability issue on port A, as observed in specific conditions on the demonstrator (symptom: signal related spurs at Fc/4 +/-Fout).

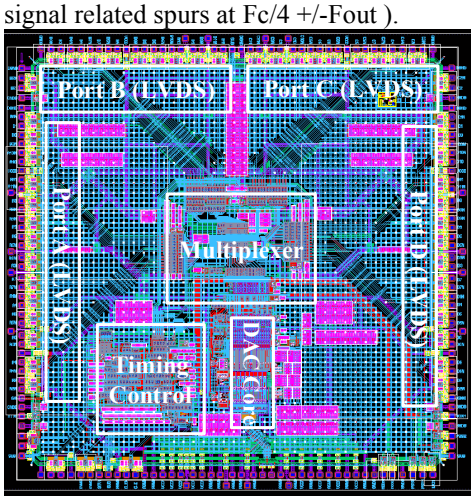

Figure 2. 12 Bit 3 GS/s 4:1 MuxDAC Chip Layout

The design of the new product has also taken in account specific spatial constraints, that is:

- TMV (Triple Majority Voting) in clock dividers controlling the MUX part of the circuit.
- ESD protections allowing for cold sparing (live inputs must not trigger protections when supplies are not powered or tied to ground).

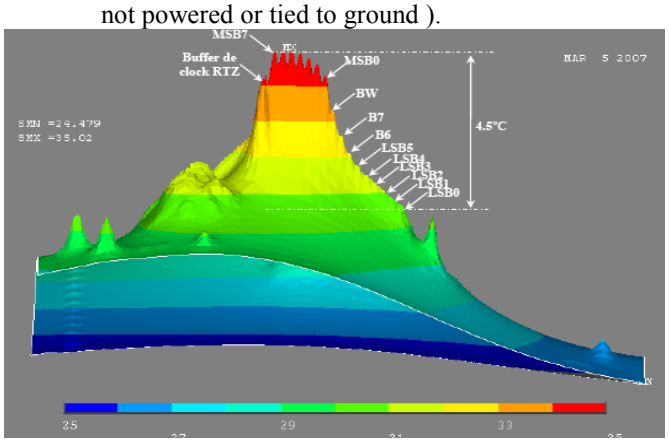

Figure 3. Thermal simulation of the Demonstrator

The design of the analogue core has been revisited, yet keeping the same architectural choices, to improve or secure performance of the demonstrator. This includes:

- Dedicated GND node for substrate plugs, targeting better isolation of Analogue and Digital parts.
- Tighter core layout to reduce clock distribution path to the switches, targeting steeper internal clock edges.
- Tighter layout of the core for better management of thermal gradient effect targeting improved linearity (thermal simulation results are given Fig. 3 and 4).
- Reduction of routing between internal output termination and actual output pads location.

The topology of the final clock tree driving NRZ mode and RF mode switches in the DAC core and the topology of the analogue merging tree have been optimized using Agilent EESOF's electromagnetic simulator MOMENTUM.

DAC core width has been shrunk from 1080µm to 350µm, its length has increased from 330µm to 615µm, thus allowing for a reduced thermal gradient across the DAC core.

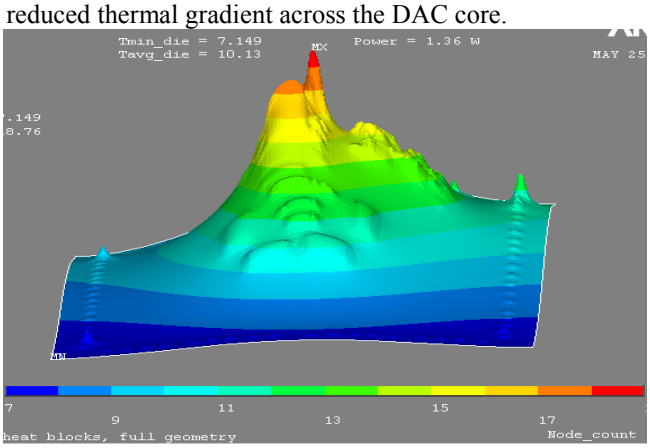

Figure 4. Thermal simulation of new Product.

The thermal mismatch across the DAC core is reduced to 1.2°C (fig. 4) for the new product against 4.5°C (fig. 3) for the demonstrator. Thermal issue (deterministic) was dominant over matching issues (statistical) in Integral Non Linearity observed on the demonstrator. The topological improvements of DAC core targets significant INL decrease altogether with spectral purity improvement for the new product.

D. *Pushing the sinc(x) limits with the different output modes*

The response of a classic (NRZ) DAC submitted to the sinc(x) attenuation where sinc(x)=sin(π.x)/π.x, and x is the normalised output frequency (F_{out}/F_{sample} where F_{sample} is the sampling rate).

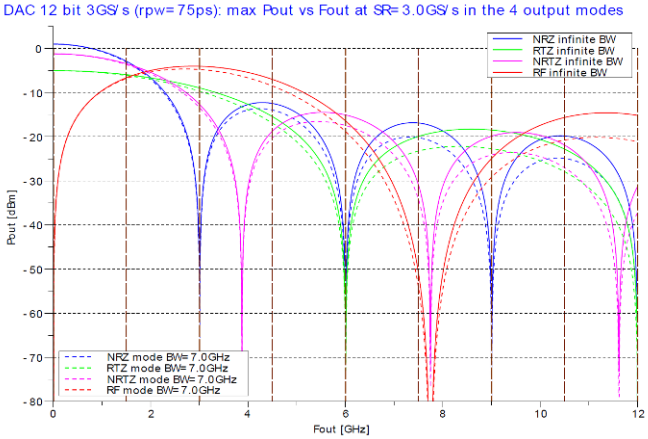

Figure 5. Max available power at DAC output at nominal gain at 3GS/s over 8 Nyquist zones (DC to 12GHz)

With a 50% resampling clock pulse width in RTZ mode, the zero order hold time window is half the clock period and allows the expansion of the DAC sinc function by a factor 2, the ideal formula of attenuation becomes ½.sinc(x/2). This enables operation in the 2nd and 3rd Nyquist regions. However, the RTZ mode induces a 6 dB loss in carrier power, which directly impacts the SFDR level in dBc.

Beyond the expansion of the sinc function, the main interest of RTZ mode is that it transmits only settled values to the output of the DACs, thus allowing for best spectral purity even at high Fout.

We have also implemented the Narrow RTZ mode which combines the advantages of RTZ mode (increased spectral purity) with the advantages of NRZ mode (high power available in 1st Nyquist zone) thanks to an asymmetrical re-sampling clock. One positive side effect of this new mode is also to allow for operation over the 4th Nyquist zone (fig. 5).

For operation in the 3rd Nyquist zone with maximized available power, an alternate mode called "RF" or "mixed" has been introduced in the new product.

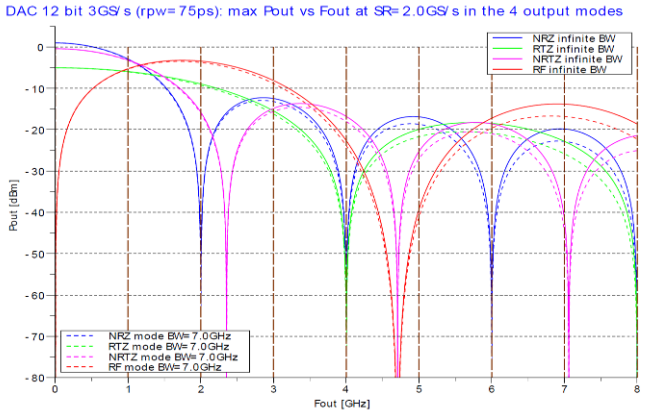

Figure 6. Max available power at DAC output at nominal gain at 2GS/s over 8 Nyquist zones (DC to 8 GHz)

Figure 5 illustrates over 8 Nyquist zones the theoretical (infinite Bandwidth) [solid line] and the actual (fitted taking in account finite bandwidth effect due to circuit and package) [dashed line] available output power in the four modes when the DAC is operated at 3GS/s, vertical long dashed brown lines highlight the limits of Nyquist zones. Figure 6 is plotted for operations at 2GS/s.

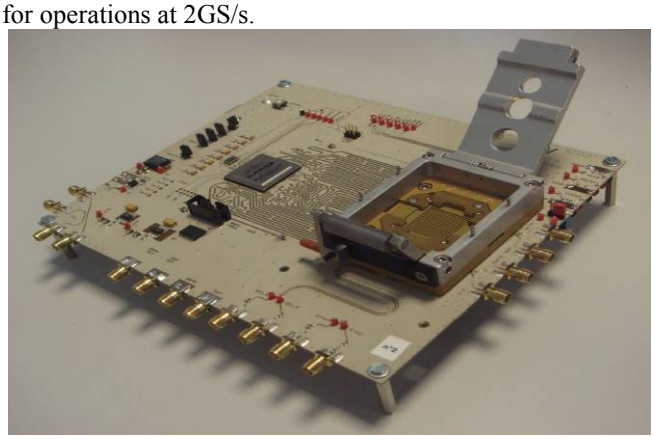

Figure 7. 12 bit 3S/s 4:1 MuxDAC characterization board

IV. CHARACTERIZATION RESULTS

The circuit has undergone a thorough characterization either at lab on characterization board (figure 7), which is by the way the evaluation board mounted with socket, or on Teradyne's Tiger industrial tester. For obvious reasons it is not possible to give here the complete results, instead we will give the most demonstrative and significant characterization results.

A. Static performance

Integral Non Linearity (INL) and Differential Non Linearity measurements performed at full sampling rate but for a slow Fout, allows for checking if the architectural options taken address successfully the issues detected on demonstrator regarding static linearity.

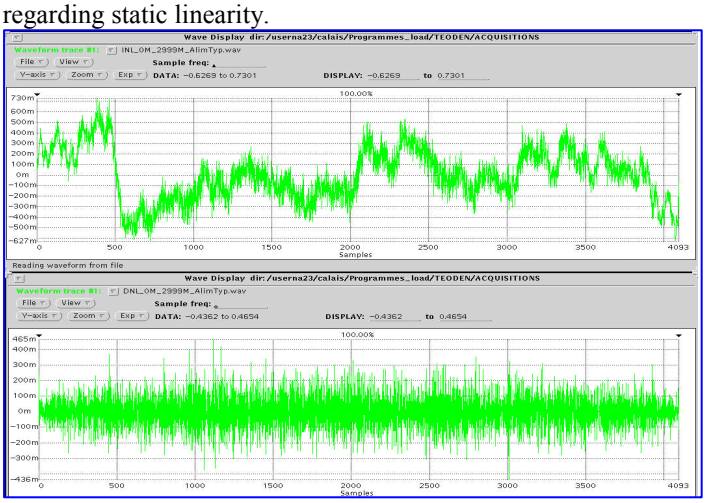

Figure 8. INL and DNL measured for at 3GS/s

The INL is divided by five regarding the demonstrator; issues affecting static linearity have been successfully addressed.

B. Analogue Output Bandwidth.

High analogue output bandwidth is a key feature of this DAC. There are two ways to estimate the output bandwidth of a DAC:

- Measure Pout Vs Fout, and compute the deviation from the theoretical response Pout vs Fout (solid lines in figure 5 and 6).
- Measure the 10% 90% rise time or fall time of a full swing step, and compute the Bandwidth applying the formula BW=0.35/Tr (assuming a first order cut-off).

The second method is somehow more accurate and easier to apply, granted the probe contribution is not overlooked (see $Tr_{measured} = sqrt(Tr_{DAC}^2+Tr_{probe}^2)$.). Using both methods we obtained consistent results.

The probe used is 12.5GHz BW limited, therefore we must use Tr_{probe}=28ps (that is 0.35/BW) for probe de-embedding.

Best measurements are obtained on the evaluation board with the probe as close as possible of the DAC output, with a soldered device on the board (due to the finite bandwidth of the socket, measurement with socketed devices are a little bit pessimistic, and gives Tr 2 or 3ps longer than for soldered devices).

Measurements of fpBGA196 plastic package always display higher bandwidth (ranking from 7GHz for socketed device to

7.5GHz for soldered device) than measurements of CI-CGA 255 ceramic package (ranking from 5.9 to 6.2GHz).

C. Single tone measurement and spectral purity

One recurrent issue of high speed DAC is collapsing of high frequency linearity resulting in spectral purity degradation for operation beyond baseband (that is for operation beyond the first quarter of the first Nyquist zone). This collapsing has two root causes:

- At high sampling rate the spectral contribution of the transition between settled output levels is no more negligible regarding the spectral contribution of the settled output levels. If output bandwidth is not sufficient regarding sampling rate this term may become the leading factor in performance
- Furthermore transition between two successive output levels is history dependant with the classical NRZ approach, and things turn nasty when leaving baseband operations

Yet introduction of NRTZ or RTZ modes may allow to decrease or to suppress this history dependence, this is not always the case either because the return to zero is perform by mean of action on the digital code fed to the converter, or because the analogue output bandwidth of the DAC is not sufficient to allow for history dependence cancelling.

The architectural choices made for this product seems to be particularly relevant for this issue, and this is clearly illustrated by figures 9 to 11.

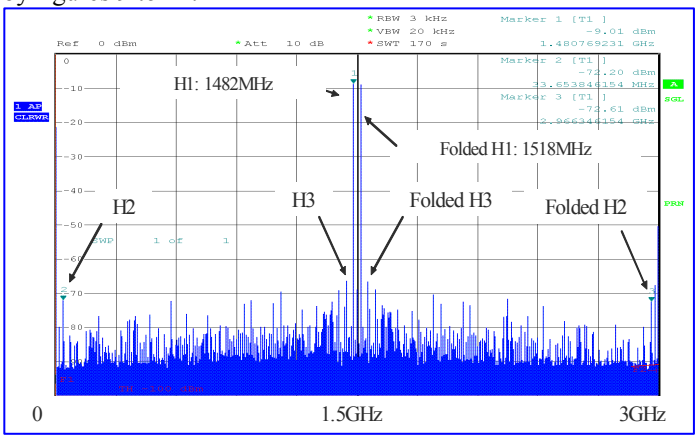

Figure 9. Spectrum from DC to 3GHz for a tone at 1482MHz, -3dBFS generated at 3GS/s in NRZ mode

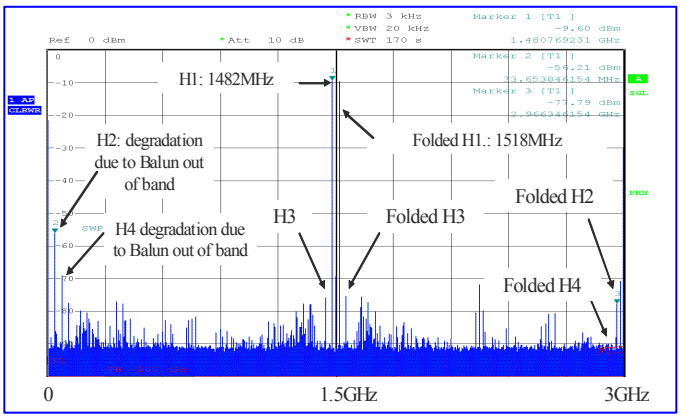

Figure 10. Spectrum from DC to 3GHz for a tone at 1482MHz, -3dBFS generated at 3GS/s in NRTZ mode.

Figure 9 shows that the spectral degradation occurring at high Fout high sampling rate in NRZ mode is pretty well contained thanks to the high output bandwidth of this DAC. Nevertheless NRTZ and RTZ output mode of the DAC still allow for further improvement in spectral purity.

Figure 10 shows significant spectral purity improvements brought by the NRTZ mode which decreases the history dependence of the transition between successive output levels, yet there still should be some possible improvements.

Figure 11 illustrates further improvements brought in spectral purity by RTZ, thanks to a longer reshaping which allows to suppress completely history dependence of the transition between output levels, but the price to pay for that is a 6dB power loss regarding NRZ mode at low output frequency (or a 3dB loss at end of the first Nyquist zone, see figure 5).

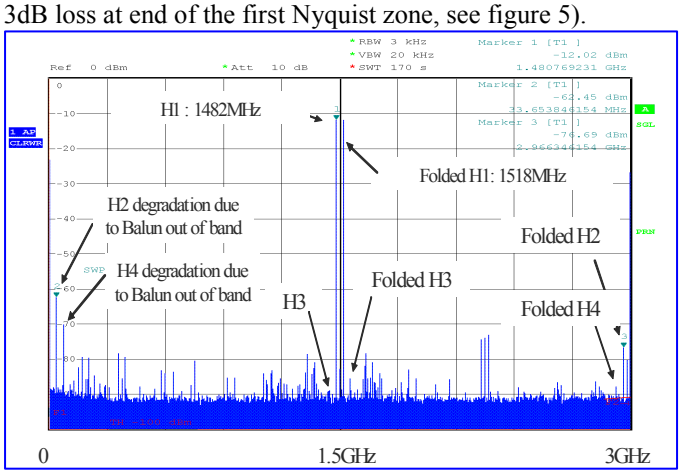

Figure 11. Spectrum from DC to 3GHz for a tone at 1482MHz, -3dBFS generated at 3GS/s in RTZ mode.

Metrology issue: the balun used for measurements including the 2nd or the 3rd Nyquist zones, is specified for a frequency range from 500MHz to 7GHz, the presence of significant energy level in spectral cases below 400MHz (either low order harmonics or folded low order harmonics) lead to apparent significant degradation of performances which are in fact due to the balun limitations.

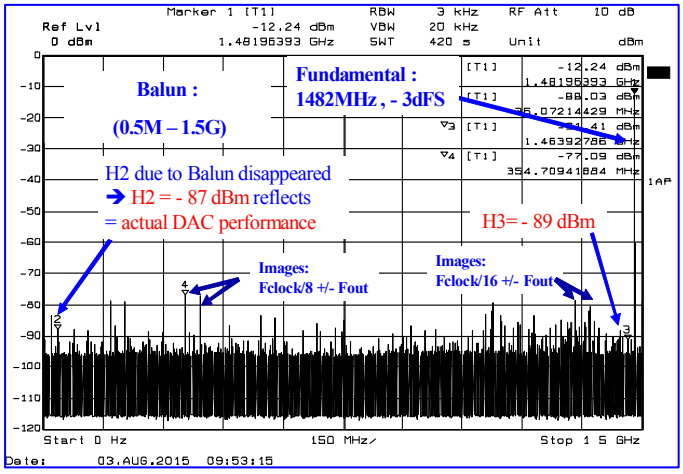

Figure 12. Output mode RTZ :Spectrum of 1st Nyquist zones, with optimum Balun (0.5M-1.5G, instead of 0.5G-7G): H2 issue is solved

Figure 12 shows measurement restricted to the 1st Nyquist zone with a more relevant balun (0.5MHz to1.5GHz specified

frequency range), with the same pattern as the one used for figure 11, and indeed there is a strong improvement.

D. Multi-tone measurements up to 5th Nyquist Zone

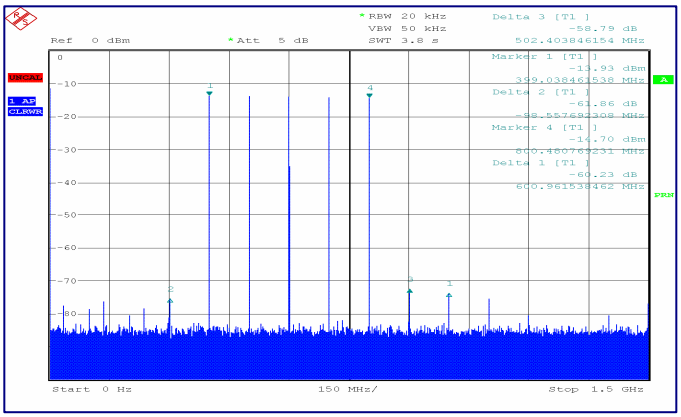

Figure 13. NRTZ mode: 5tones in 1st Nyquist Zone, SFDR=58.8dB

The pattern used is five tones ranking from 400MHz to 800MHz generated at 3GS/s (figure 13), by folding the five tones in second the Nyquist zone (figure 14) are ranking from 2.6GHz (3GHz-0.4GHz) down to 2.2GHz (3GHz-0.8GHz), in the 3rd Nyquist zone (figure 15) the tones are ranking from 3.4GHz to 3.8GHz, in the 4th Nyquist zone (figure 16) the tones are ranking from 5.6GHz down to 5.2GHz and the 5th Nyquist zone (figure 17) the five tones are ranking from 6.4GHz to 6.8GHz. Reminder in odd Nyquist zones, spectrum is translated, in even Nyquist zones spectrum is mirrored.

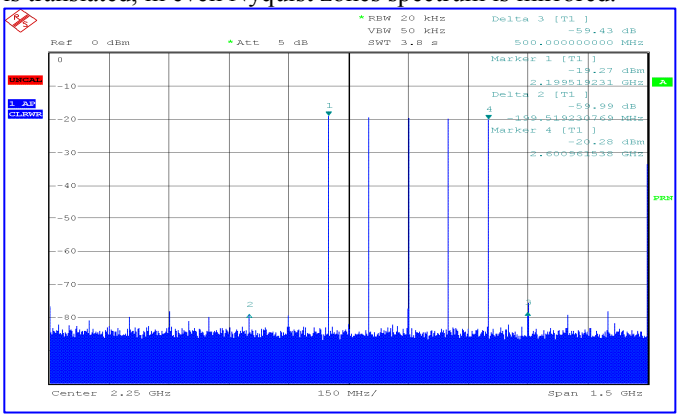

Figure 14. RF mode: 5 tones in 2nd Nyquist Zone (S-Band), SFDR=59.4dB

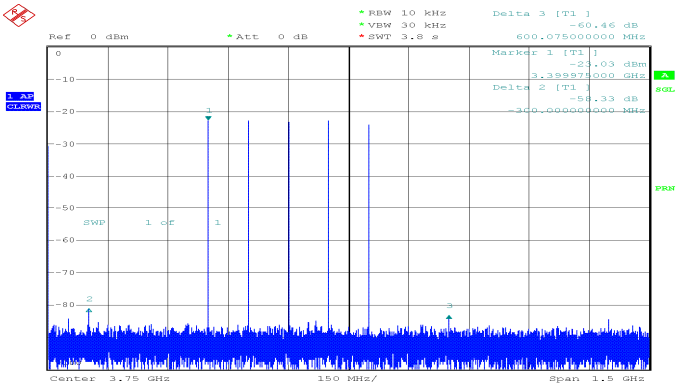

Figure 15. RF mode: 3rd Nyquist Zone (S-Band), SFDR=58.3dB

Figures 14 to 17 demonstrate the usability of the DAC for Direct Micro Wave Synthesis far beyond the 1st Nyquist zone, and up to the 5th Nyquist Zone, that is the lower C-Band.

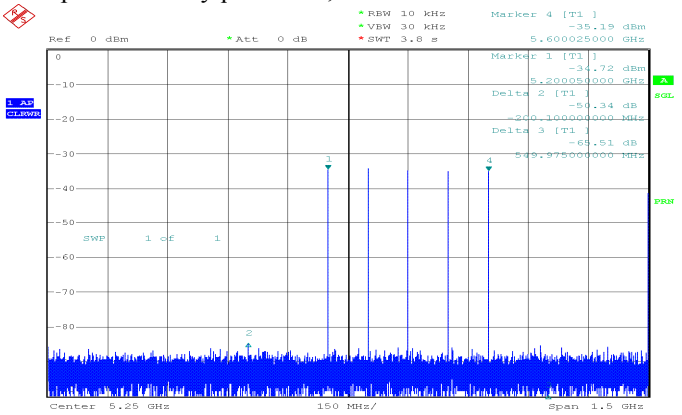

Figure 16. NRTZ mode: 5 tones in 4th Nyquist Zone(C-Band), SDFR=50.3dB

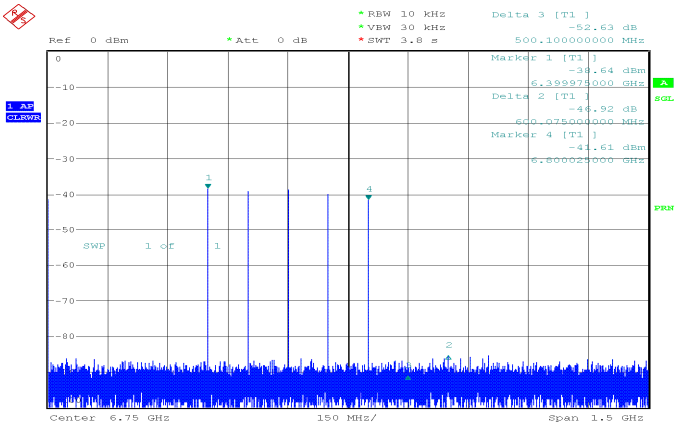

Figure 17. NRTZ mode: 5 tones in 5th Nyquist Zone (C-Band), SFDR=46.9dB

E. DOCSIS v3.0 measurements (1st Nyquist)

Measurements as per DOCSIS v3.0 of ACPR in NRTZ mode for a 6MHz wide QAM128 channel centred on 300MHz (fig. 18) or 900MHz (fig 19) illustrate clearly the interest of NRTZ mode, with almost no degradation in term of ACPR when increasing the centre frequency of the channel generated.

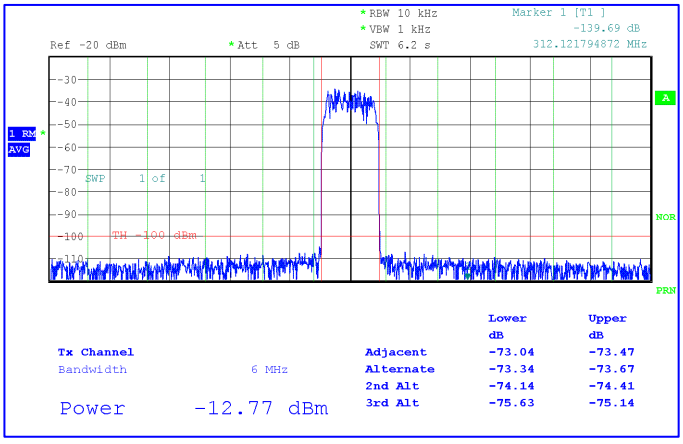

Figure 18. Measurement of 1 channel 6MHz wide QAM 128 as per DOCSIS v3.0 centred on 300MHz: ACPR in excess of 68.5dB

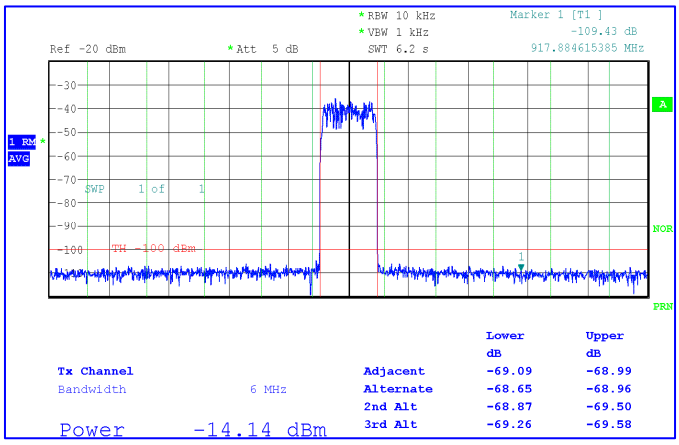

Figure 19. Measurement of 1 channel 6MHz wide QAM 128 as per DOCSIS v3.0 centred on 900MHz: ACPR in excess of 68.5dB

F. QPSK modulation measurement up to 5th Nyquist Zone

The following figures illustrate the capability of the DAC for Direct Microwave synthesis far beyond the 1st Nyquist zone and up to the 5th Nyquist zone, which means direct synthesis in S or C Bands.

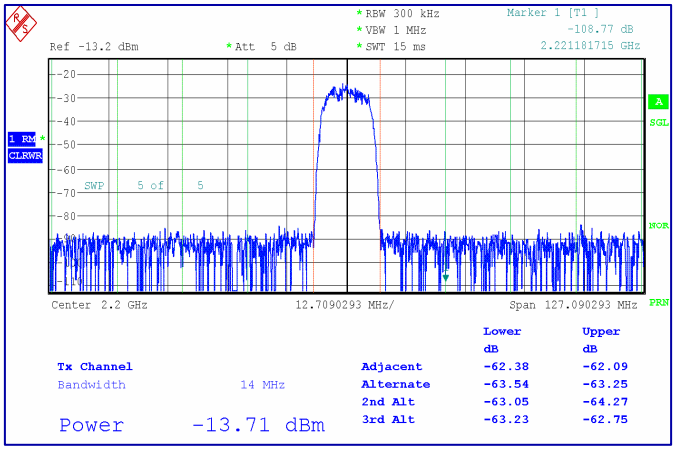

Figure 20. NRTZ mode: a 10 MHz wide QPSK modulation centred on 2.2GHz (S-Band): ACPR in excess of 62dB

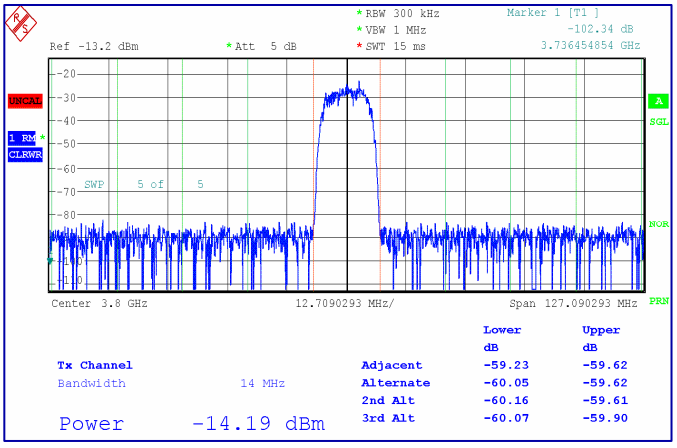

Figure 21. RF mode, A 10MHz wide QPSK modulation centred on 3.8GHz (S-Band): ACPR in excess of 59 dB

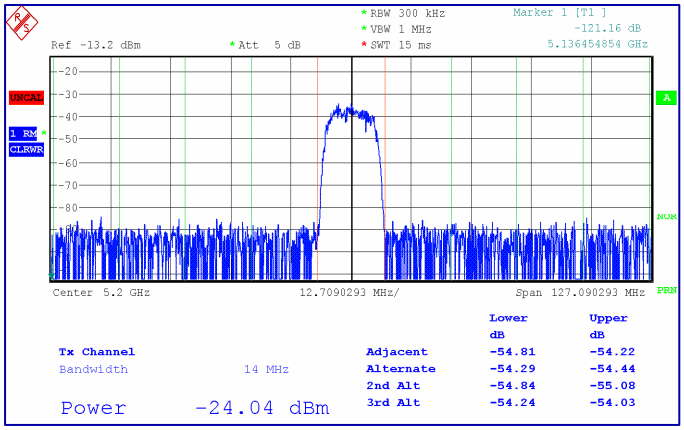

Figure 22. NRTZ mode: a 10 MHz wide QPSK modulation centred on 5.2GHz (C-Band): ACPR in excess of 54 dB

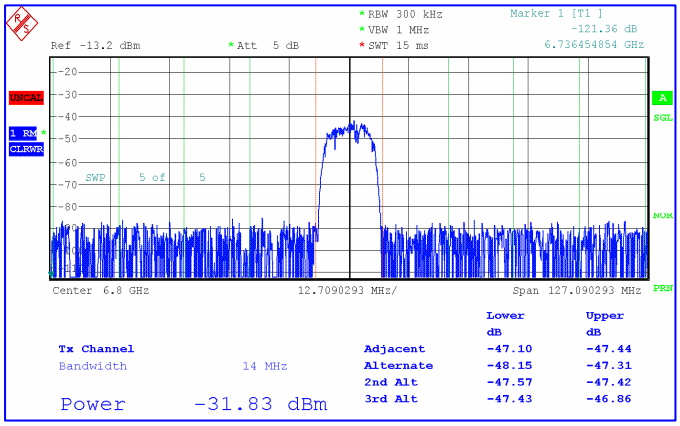

Figure 23. NRTZ mode: a 10MHz wide QPSK modulation centred on 6.8GHz (C-Band): ACPR in excess of 47dB

G. NPR measurements

NPR is probably the most relevant figure to reflect the usability of a device in real life condition, theory is clearly explained for ADC by Walt Kester [6], by duality this is also applicable to DAC. The principle is to use a broadband (Gaussian) noise pattern with a notch in the pattern, and to compare power density inside and outside of the notch.

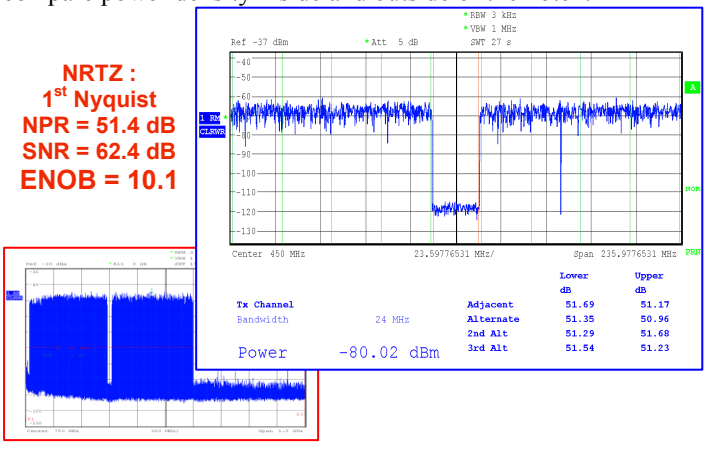

Figure 24. NPR @ 3GS/s, NRTZ output mode, 20MHz-900MHz wide pattern, loading factor -14dB, 25MHz notch centered on 450MHz.

The ratio between the standard deviation of the noise and the full scale of the system, is called loading factor, when the

noise level is too small the noise NPR is not optimal because of thermal noise floor in the notch, and when the noise level is too large, due to clipping effect the system becomes non linear and the notch is filled by inter-modulation products. For a 12 bit quantification (either DAC of ADC by duality of the theory), the optimal loading factor (LF) is -14dB (that is sigma of the noise used is Full Scale divided by 5).
A pattern compliant with the above specification is fed to the DAC and the output is observed with the spectrum analyzer in detection mode RMS, value is computed using the ACP function of the analyzer.

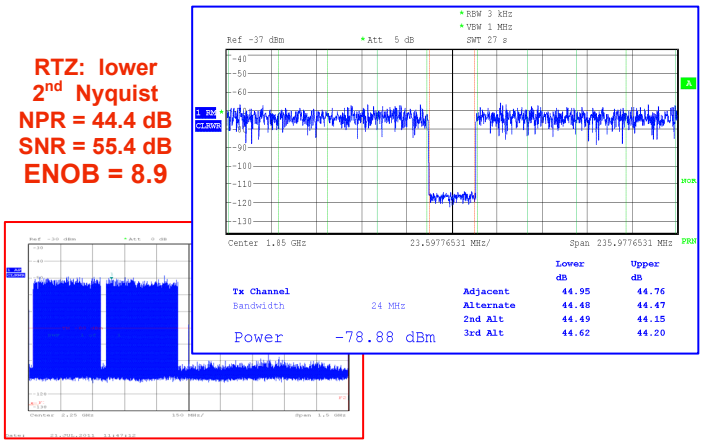

Figure 25. NPR @ 3GS/s, RTZ output mode, 1.52GHz-2.2GHz wide pattern, 25MHz notch centered on 1.85GHz, -14dB loading Factor.

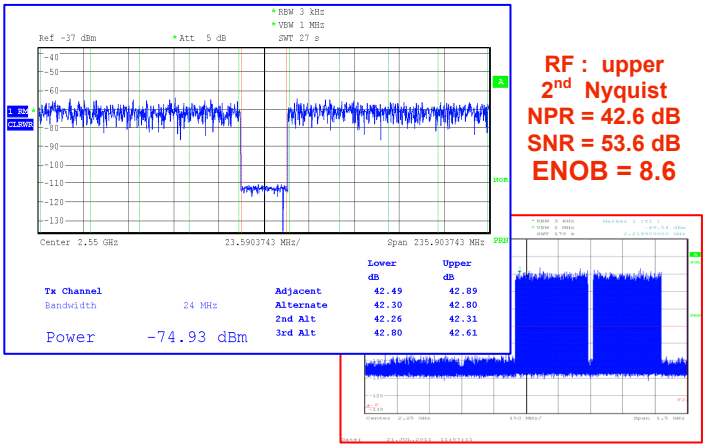

Figure 26. NPR @ 3GS/s, RF output mode, 2.2GHz-2.88GHz wide pattern, 25MHz notch centered on 2.55GHz, -14dB loading Factor.

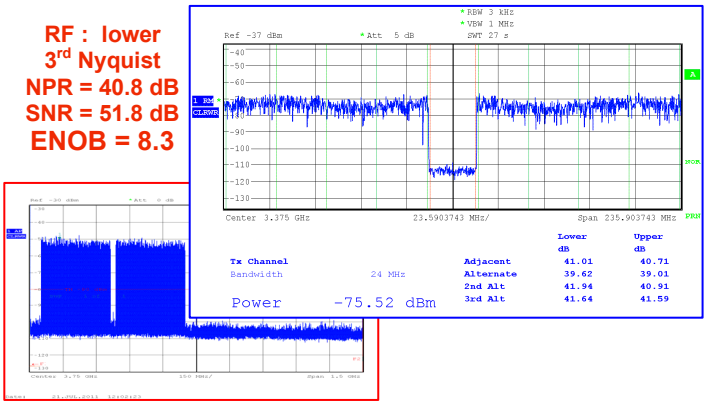

Figure 27. NPR @ 3GS/s, RF output mode, 3.05GHz-3.7GHz wide pattern, 25MHz notch centered on 3.755GHz, -14dB loading Factor.

All measurements given figures 24 to 27 are performed at optimal loading factor.
It is quite easy to derive the SNR from NPR measurement using the formula: SNR[dB]=NPR[dB]+|LF|[dB]-3.
The Equivalent Number Of Bit is then given by the formula: ENOB[effective bit]=(SNR[dB]-1.76)/6.02.

V. SUMMARY

We have introduced a multi-mode 12 bit 3GS/s Mux DAC based on Infineon's B7HF200 technology. Thanks to an innovative architecture combined with the high performance level of the process in terms of speed and matching, we have been able to demonstrate direct digital synthesis in L, S and C bands with cutting edge performances (in excess of 10 effective bit for base band operation, more than 8.6 effective bit in L-Band, and more than 8.3 effective bit in S Band).
The availability of such a component dissipating only 1.4W will probably bring to life new architectural concepts in transmission systems.
Possible applications are in Arbitrary Waveform Generators, Gigabit Passive Optical Network, Data on Cable (DOCSIS), systems using complex microwave waveform design and engineering (new radar paradigm), ciphered wideband communication by frequency hopping; other possible uses are in Automated Test Equipment, Reflectometry, LIDAR…

ACKNOWLEDGMENT

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