Design of a 3 Bit 20 GS/s ADC in 65 nm CMOS

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***Abstract*— A 20 GS/s 3 bit flash ADC with an analog input bandwidth of 10 GHz is realized in a 65 nm LP CMOS technology. By employing a fourfold parallelization a high sample rate is achieved, while a large input bandwidth is maintained. Simulations at 20 GS/s exhibit an effective resolution of 2.5 Bits at the Nyquist frequency. The chip area is 5.2 mm² while the ADC core area is 0.16 mm².**

I. Introduction

As fiber dispersion limits the maximum transmission distance in 10 to 40 Gbit/s fiber-optic systems, electronic equalization is necessary. A cost-effective electronic equalization can be realized by integrating an ADC with a digital equalization circuit on a single CMOS chip. For this equalization method only a relatively low resolution of about 3 bits is required [1], [2].

The fastest published CMOS ADC achieves an effective resolution of 4.2 bit at 8 GHz input frequency and 3.5 bits at 12 GHz with a sampling rate of 24 GS/s. With a 160-fold parallelization the core area of the chip is 16 mm² [3].

In this work a fourfold 3 Bit 20 GS/s Flash ADC in 65 nm CMOS technology is presented which consumes a total area of 0.16 mm² for the core ADC, allowing a cost-effective integration in a system on a chip equalizer. The second section of this paper introduces the basic ADC blocks and components. The third section shows simulation results on layout level. Section four summarizes the final realization.

II. ADC Design

A. ADC Concept

Fig. 1 shows the block diagram of the ADC. The analog input is multiplexed by four sample and hold amplifiers to four parallel ADC channels. Following the sample and hold amplifier, seven comparators and flip-flops perform the quantization of the sampled input signal. Thereafter a thermometer-to-binary encoder performs the binary encoding. All four channels are synchronized by a three step synchronizer to allow a synchronous data output of all four channels [4], [5].

B. Sample and Hold Circuit

Fig. 2 shows the sample and hold circuit. It consists of two cascaded track and hold circuits in a master-slave configuration. The first track and hold sampling switch is a differential n-channel transfer gate that is compensated on the output by dummy transistors, to prevent clock and charge feedthrough. The following unity gain amplifier passes the signal to the second track and hold circuit. The hold capacitance of the first track and hold circuit is composed of the gate capacitance of the unity gain amplifier and the hold side transfer gate capacitance.

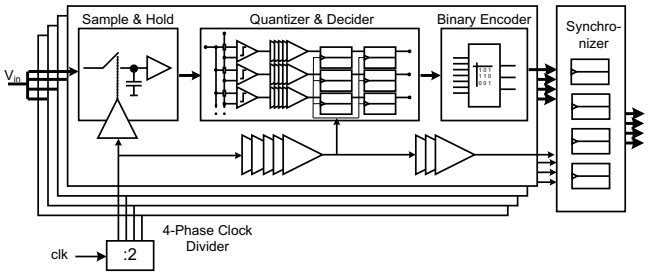

Fig. 1. Block diagram of the ADC.

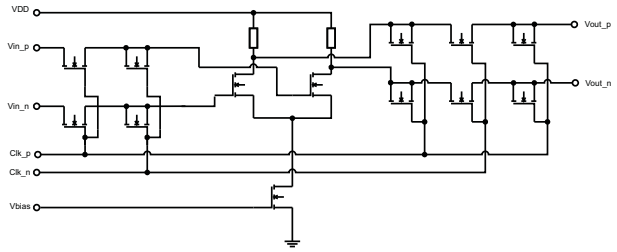

Fig. 2. Sample and Hold Circuit.

The second track and hold circuit contains compensated differential n-channel transfer gates with dummy FETs at the input and the output side. The output is directly connected to the input of the comparators. Thus the hold capacitance is composed of the gate capacitance of the comparators and the hold side of the second track and hold circuit. By removing the output amplifier in the second track and hold circuit an additional offset, gain error and nonlinear distortion source is eliminated.

The circuit is designed for a single-ended input signal amplitude of +/-200 mV around the input common mode level, resulting in the capability to handle differential input signals in the range of +/-400 mV. The required single-ended clock signals are generated from an external differential clock which is internally divided by two and buffered by a chain of CML and CMOS inverters and finally shifted up by a bootstrap circuit. Altogether the clocking and the input circuit are the most critical part of the circuit as they directly affect the resulting effective resolution bandwidth (ERBW).

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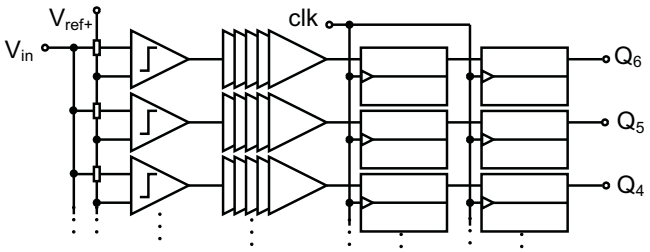

Fig. 3. Quantizer and Decider Circuit.

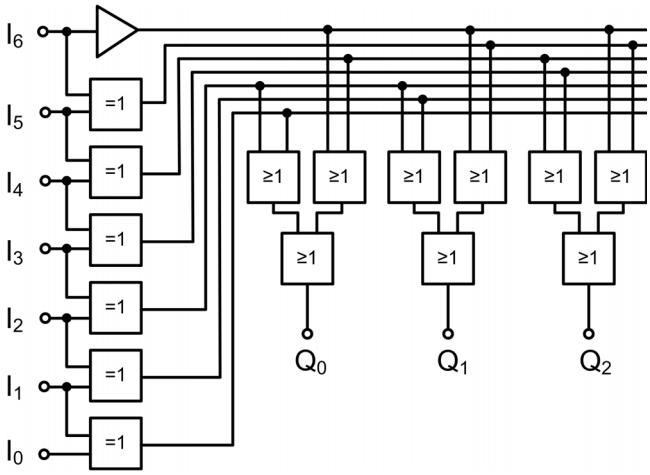

Fig. 4. Block diagram of the Thermometer-to-Binary Encoder.

C. Quantizer and Decider Circuit

The comparator block depicted in Fig. 3 is build up of a fully differential comparator [4] followed by five amplifiers and two flip-flops. The comparator compares the input signal with the constant reference voltage generated from a resistive reference ladder. The limiting function is implemented by a chain of high-speed low-gain differential amplifiers and two flip-flop stages, which also act as decision flip-flops. When the analog input voltage of a comparator is near the reference voltage of the comparator a metastable state may occur on the input of a connected decision flip-flop. Using two flip-flops as deciders significantly reduces the metastable states at the output of the quantizer and decider circuit.

D. Thermometer-to-Binary Encoder

The thermometer-to-binary encoder in Fig. 4 is based on a ROM structure. A priority encoder, implemented by XOR-gates, generates seven signals which are directly encoded by OR-Gates into the 3 bit binary code. An advantage of the circuit is the regular structure and a symmetric delay for all paths. A disadvantage is that single bubble errors lead to a completely wrong output. But as the decision levels are 100 mV apart, bubble errors are very unlikely to occur.

E. Synchronization Circuit

The four time-interleaved 3 bit ADCs are synchronized to the phase of a common clock in three flip-flop stages as shown in Fig. 5. In the first stage channel two is synchronized to

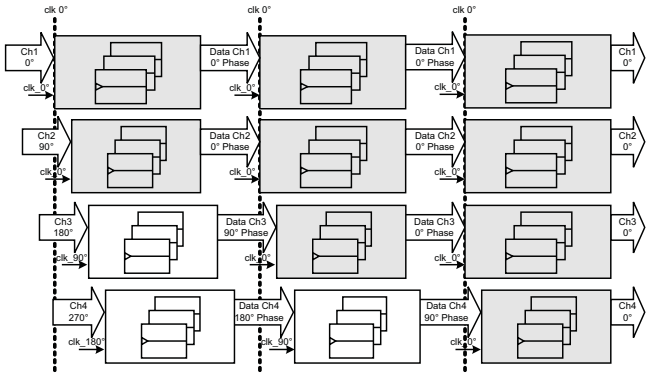

Fig. 5. Block diagram of the Synchronizer.

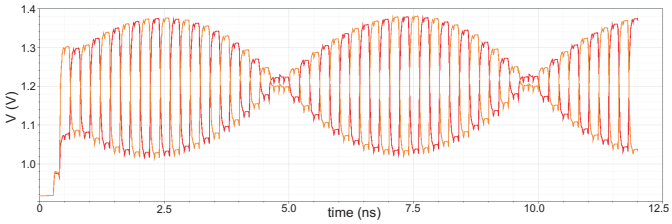

Fig. 6. Single ended comparator input voltages at an input frequency of 7.4 GHz for a single channel sampling rate of 5 GS/s.

channel one while channel three is synchronized to channel two and channel four is synchronized to channel three. After this stage channel one and two are synchronous to each other. Following this principle, after the next stage channel one to three are synchronous to each other. Finally after the third stage all channels are synchronous to each other.

III. Simulation Results

In Fig. 6 the simulation results of the beat-frequency test at the output of the sample and hold circuit, respectively at the input of the comparator circuit is depicted. The figure shows the results for an input frequency of 7.4 GHz. The input signal is undersampled, thus the output signal of the sample and hold circuit has a frequency of 2.4 GHz. This is slightly less than half the sampling rate, thus the amplitude of the output signal will vary from a maximum to a mimimum, depending on the sampling point. The maximum of the output amplitude is used to determine the attenuation of the circuit, as it corresponds to the sampling of the input signal sine wave at its extremum. The simulation is done on layout level under the constraint that parasitic layout effects are only extracted for the sample and hold circuit and the quantizer and decider circuit including the corresponding clock drivers.

The input bandwidth of the sample and hold circuit is derived by repeating the above simulation at various input frequencies. The results of the simulations are depicted in Fig. 7. As the 3 dB cutoff frequency is at 10 GHz a high input bandwidth is achieved. This results in an effective number of bits (ENOB) of 2.5 bit at the Nyquist frequency.

Table I summarizes the simulated characteristic values under the assumption of an effective resolution of 2.5 bit at the

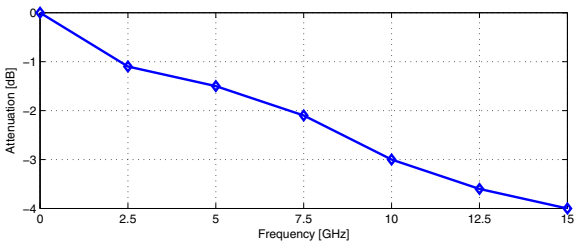

Fig. 7. Input bandwidth of the Sample and Hold Circuit.

TABLE I
ADC PERFORMANCE

Nominal resolution	3 bit
Conversion rate	2-20 GS/s
Input voltage range	0.8 $V_{pp\text{-}diff}$
ENOB @ 10 GHz	2.5 bit
Power consumption	3.3 W
Figure of Merit	20.6 pJ/conv
Supply Voltage	1.5 V
ADC core size	0.16 mm^2
ADC chip size	5.2 mm^2

Nyquist frequency which corresponds to 3 dB attenuation of the sampled signal at this frequency. In practice this effective resolution is not achievable at this sampling rate, as all mismatch effects were neglected and the sensitivity of the comparators and the decider flip-flops is not included in this simulation. Also the channel mismatch of the four times interleaved structure will degrade the overall effective resolution [6].

IV. REALIZATION

The layout of the core ADC is shown in Fig. 8. The four ADC channels are placed next to each other, the sample and hold circuits are located directly in front of the corresponding ADC channel. This is to minimize the parasitic capacitance between the output of the second track and hold circuit and the input of the comparators at the cost of a slightly higher input capacitance at the input of the first track and hold circuit. The large clock drivers are placed together with the bootstrap circuit directly in front of the sample and hold circuits, to minimize parasitic effects on the clock lines.

In Fig. 9 the chip layout is depicted. The digital outputs are on the left and the right hand side. The analog input, the clock input and the clock output are on the bottom side. An additional half rate clock output and control signals are on the top side. The ADC core is placed close to the analog input. Due to the high output count the chip size was determined by the pad configuration. The pads are placed in a single row with a pitch of 100 µm. All differential signals have a GSSG configuration, besides the ADC analog input with a GSGSG configuration. The connection from the pads to the input and output circuits are designed as transmission lines with a characteristic impedance of 50 Ohm.

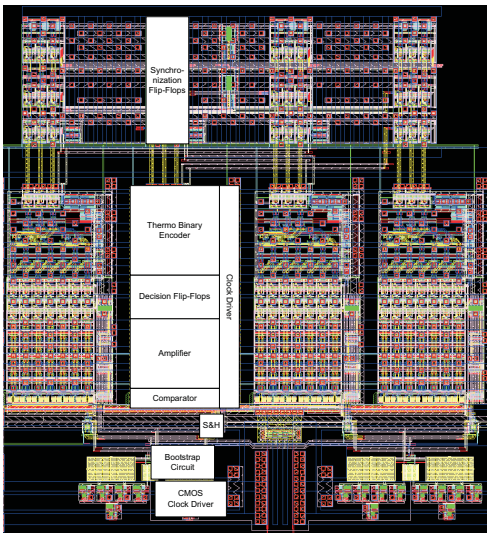

Fig. 8. Layout of the ADC core.

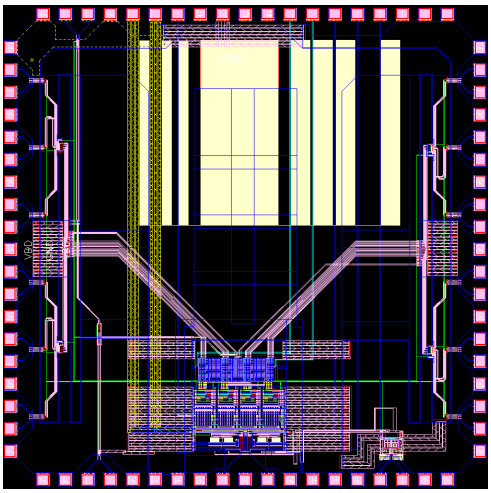

Fig. 9. Layout of the ADC chip.

V. CONCLUSION

The presented 3 bit 20 GS/s CMOS ADC has an effective resolution of 2.5 bit at the Nyquist frequency and a small core size of 0.16 mm^2. The ADC is suitable for integration with digital systems on a single chip. The measurements will be published elsewhere.

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