A 1-GS/s CMOS 6-bit Flash ADC with an Offset Calibrating Method

Chih-Hsiang Chang, Chih-Yi Hsiao, and Ching-Yuan Yang
Department of Electrical Engineering
National Chung Hsing University
Taichung, Taiwan
d9564501@mail.nchu.edu.tw; ycy@nchu.edu.tw

Abstract **— In this paper a 1-GS/s 6-bit flash type analog-to-digital converter (ADC) is designed in 0.18-μm one-poly six-metal CMOS. An offset calibrating method is used to improve the performance of ADC. To reduce the input capacitance of the ADC and the amount of calibration circuit, the active interpolation technique is applied. Measured results show the ADC achieves a SNDR of 32.5 dB for a 7 MHz input at 1 GS/s, and 25.4 dB for a 108-MHz input. The power consumption is 550 mW at 1 GS/s from a 1.8-V supply.**

I. INTRODUCTION

Analog-to-digital converters (ADC) play a crucial role in the data-transform interfaces. High-speed ADCs are widely used for the application in disk drive read channels and communication systems such as UWB receivers [1]. A time interleaved multi-channel ADC [2][3] is often used to achieve multi-GHz sampling rate, but this architecture needs very precise multi-phase clocks. Flash-type architectures are typically the simplest and fastest structures that can be used to implement very high-speed converters.

This paper presents the design of a 6-bit 1-GS/s ADC implemented in a 0.18-μm CMOS technology. Because of such a high-speed sampling rate, signals in data-converting process are fully-differential type. By employing an offset calibration technique in the pre-amplifier array, the mismatch of advanced logic CMOS transistors can be decreased, and high speed signal path will not be affected.

II. A/D CONVERTER ARCHITECTURE

A. Overall Structure

The architecture of the proposed flash ADC is shown in Fig. 1. The main blocks include two six-bits ADCs, one multiplexer and a set of common resistor ladder. We use clkmode and its reverse phase, clkmodeb, to control the ADC converting data or calibrating offset. Eventually the six-bit multiplexer selects the ADC to convert data to the output. The detail architecture of the flash ADC in this paper is shown in Fig. 2.

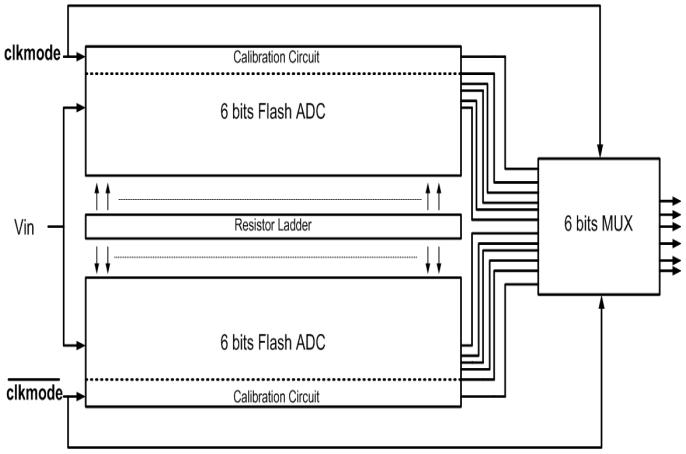

Fig.1. Overall architecture

B. The Active-interpolation Structure

Although flash ADCs can provide high-speed operation, they have the disadvantage of higher power consumption and higher input capacitance as the number of pre-amplifiers increases exponentially with the resolution. Besides, every pre-amplifier in this design has an offset calibrating circuit, more pre-amplifier circuits have more offset calibration circuits. To overcome these drawbacks, several ways like interpolation and two-step method are usually applied. Interpolation reduces the number of pre-amplifier and input capacitance in the front end.

Several interpolating techniques are widely used in flash ADC as a method to reduce power consumption and input capacitance [4][5]. Resistive interpolation is a very popular way,

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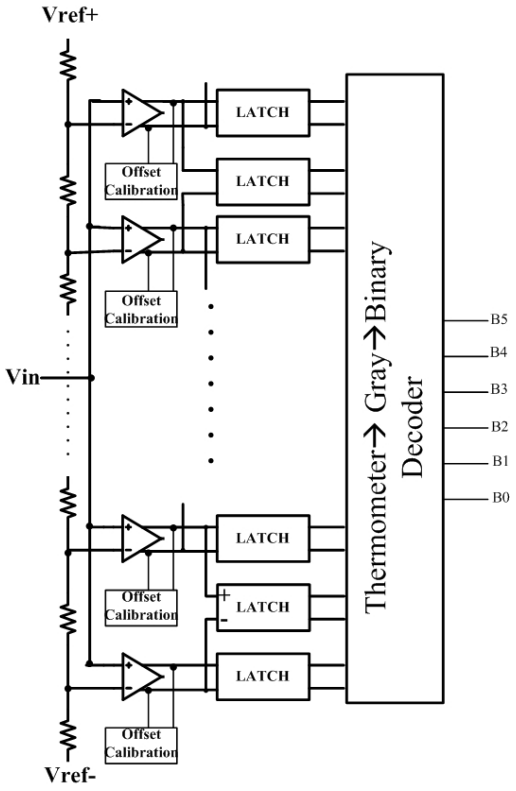

Fig.2. Flash-ADC architecture

but it relies on good linearity of pre-amplifiers. Besides, interpolating outputs with resistors create an additional RC circuit that limits the bandwidth in the interpolated signal path. Active interpolation does not suffer from this disadvantage because there is no resistor in the interpolated signal path.

C. Pre-amplifier and Latch

The preamplifier usually provides the requirements in terms of signal bandwidth, input common-mode range, input capacitance, voltage gain, and capacitive feedthrough to the reference ladder. The pre-amplifier schematic is shown in Fig. 3. A fully-differential design is applied for good rejection of kickback from latch and improved dynamic performance. Such a circuit has a total of four inputs, and the signal to be amplified is thus ((Vin+ – Vin-) – (Vref+ – Vref-)). The size of two differential pair influences the pre-amplifier characteristic. Larger devices have smaller variation and larger g_m. Additional dummies are set on both sides of the latch chain to provide equal loads.

D. Offset Calibrating Circuit

The offset voltage is the important issue in such high-speed flash ADCs. One popular approach to reducing the offset

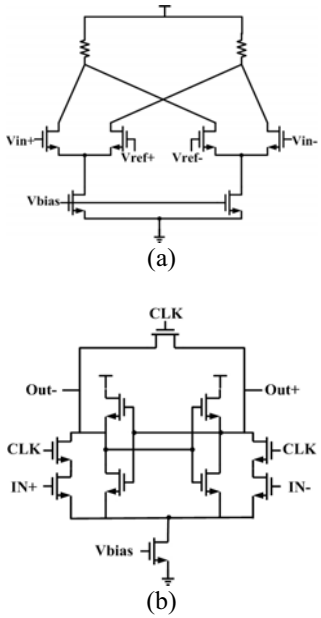

Fig.3. (a) pre-amplifier and (b) latch

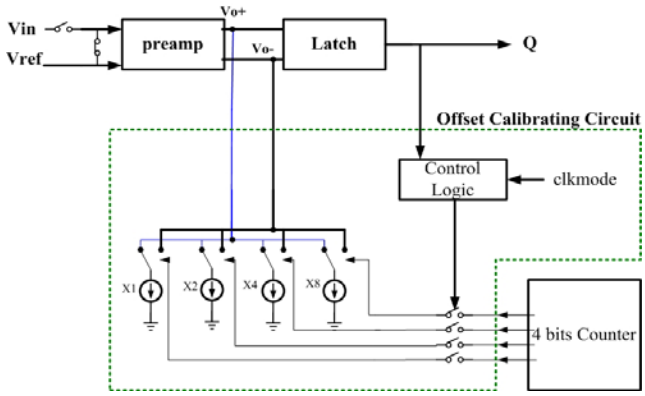

Fig.4. Offset calibrating circuit

voltage is the averaging technique [2][5][6][7]. However, the averaging technique is not enough to cancel the larger offset voltage. Therefore, other methods are devised to cancel the offset [8].

The architecture of the offset calibrating circuit is shown simply in Fig. 4, including one set of binary weighted current source, and one set of control logic. Every flash-ADC has only one four-bit counter, and every offset calibrating circuit connect to the same four bits counter. When the offset calibrating mode is turned on, Vin of pre-amplifier is connected to Vref, and output of the counter is 0000. In other words, the current of binary weighted source all flow to “Vo-” side. The current will

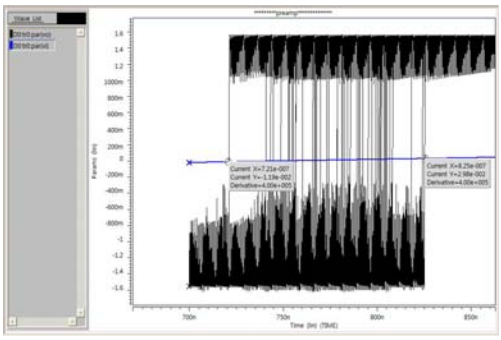

Fig.5. Monte-Carlo simulation

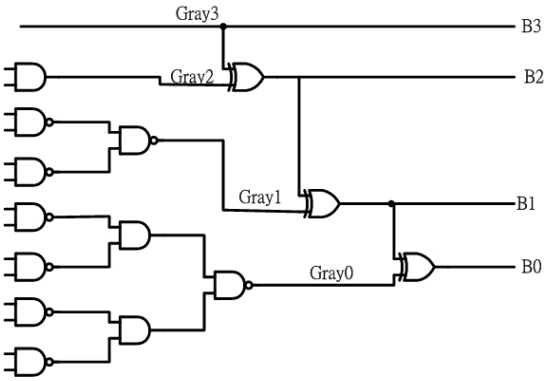

Fig.6. 4-bit thermometer-to-binary decoder

result in the offset on pre-amplifier's output. As counter's output enables, current switch from "Vo-" to "Vo+" side, and then the offset of pre-amplifier decease. Once the offset changes from positive to negative, we know it becoming very small. At this time, the control logic will turn off the switch between counter and offset calibrating circuit. The frequency of counter is 16 times of clkmode, so the output of counter will not return to 0000. Because the clock of the four-bit counter is independent of sampling rate, we can use very low speed to calibrating offset.

How much offset we can calibrate is a issue in our design .We utilize Monte-Carlo simulation to suppose the maximum offset that maybe occurred, and then we decide the unit current of binary weighted current source . The simulation is shown in Fig. 5.

E. Thermometer to Binary Decoder

Because of the metastability and sparkle error, gray coding process in many converters is used before the final binary code is generated. These errors can cause serious degradation in the linearity and the signal-to-noise and distortion ratio (SNDR) of the ADC [9][10]. For example, Fig. 6 shows a schematic of a 4-bit encoder.

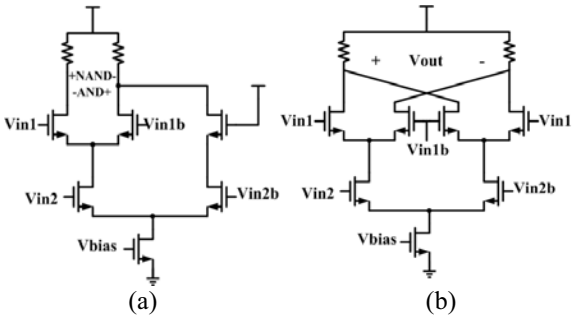

Fig.7. Current mode logics: (a) NAND &AND, (b)XOR

The speed of the encoder is one of the bottlenecks of many flash ADCs. Thus in this paper we utilize the CML (current mode logic) to implement it. Using the CML implementation has the benefits that all the signals in the circuit are differential type. Differential signals can suppress noise, and they can transfer by low-swing signals to lower dynamic power consumption. This low-swing operation is important especially for high frequency operation. Low swing differential clock signals also can be used for high speed .Current mode logics are shown in Fig. 7.

III. Measured Results

The ADC are designed and measured in a 0.18-μm CMOS technology with a 1.8-V supply. Fig. 8 shows the FFT at 1 GS/s with a 7 MHz input frequency. The ADC remains 40-dB SFDR and 32.5-dB SNDR when the input frequency 7MHz. Fig. 9 shows the SNDR at 1 GS/s, without and with calibration. We can see that the proposed offset calibration technique improve the ADC. DNL and INL characteristics are compared in Fig. 10 before and after calibration. It can found that linearity becomes better. Table I summarizes the ADC performance. Fig. 11 shows the microphotograph of the test chip with an area of 1.4×1.4 μm^2 including the output buffers and I/O pads.

IV. Conclusion

In this paper, a 1-GS/s 6-bit ADC with various aspects of high-speed design is presented. Active interpolation is used to reducing power consumption and input capacitance. We also use a offset calibration technique to improve the performance of the ADC. The ADC is designed and simulated in a 0.18-μm 1P6M CMOS technology.

Acknowledgment

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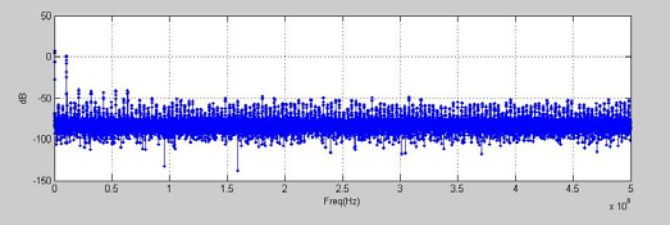


Fig. 8 . FFT analyses of the ADC at fin = 7MHz and fs = 1GS/s

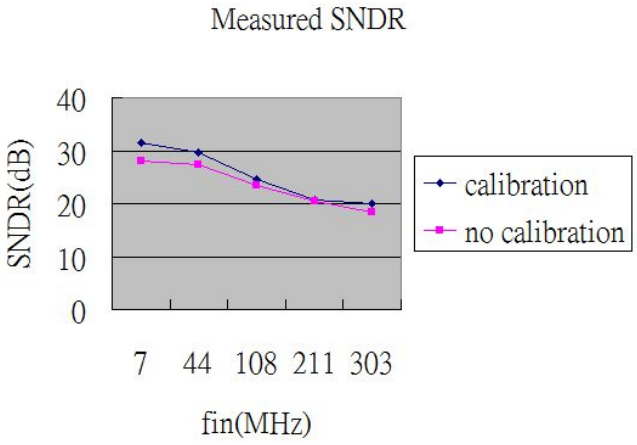
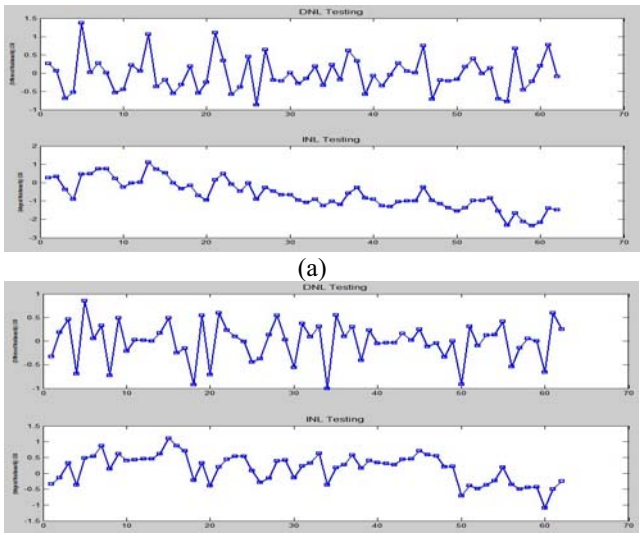


Fig.9. SNDR with 1GS/s sampling rate



(a)

(b)

Fig.10. DNL and INL at fs=1GS/s, fin=15MHz
(a)Before Calibration, DNL=1.4, INL=2.2
(b)After Calibration, DNL=1, INL=1.1

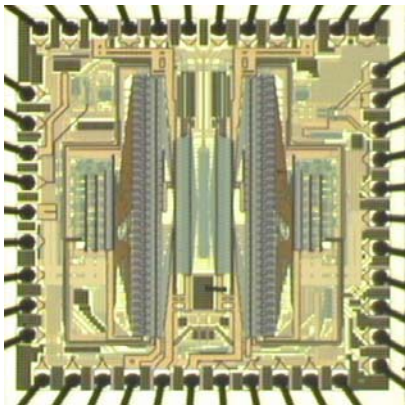


Fig.11. Die photo of the fabricated chip

Table I. Performance Summary

technology	0.18-µm CMOS
Resolution	6 bits
Power supply	1.8V
Area	1.4um X 1.4um
Power consumption	550mW
Sampling rate	1 GS/s
DNL	< 1 LSB
INL	< 1.1 LSB
ENOB	5.1 bits (fs=1GS/s, fin=7MHz)