A 5-GS/s 4-Bit Flash ADC with Triode-Load Bias Voltage Trimming Offset Calibration in 65-nm CMOS

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***Abstract*-A 5-GS/s 4-bit flash ADC is implemented in 65-nm CMOS. Offset calibration is achieved by digitally adjusting the bias voltages of the triode loads in the preamplifier without introducing additional capacitive loading in the analog path and degrading the high-speed performance. The ADC consumes 34.3 mW from a 1.2-V supply at 5 GS/s, and occupies 0.0828mm^2 active area. The ADC achieves 3.93 ENOB with a 2.5-GHz ERBW and a 0.45-pJ/convstep FOM at 5 GS/s.**

I. Introduction

The increasing demand on the data rates in serial links and optical communication systems and the emerging ultra-wideband (UWB) wireless receivers put increasing requirements on the speed and power specifications of the flash analog-to-digital converters (ADCs). Though high-speed ADCs can be fabricated in heterojunction bipolar transistor (HBT) technology, such as SiGe HBT [1], and SiGe BiCMOS HBT [2], etc., they are not suitable for integration with DSP core on the same silicon substrate to form SoC in an advanced CMOS technology. Efforts were put on the high-speed flash ADCs in deep sub-micro CMOS in recent years [3]-[8]. With the CMOS technology scaling, the increasing of cut-off frequency enables higher sampling speed of flash ADCs. However, the accuracy of the flash ADCs is still mainly limited by random offsets of preamplifiers and comparators due to device mismatches [9].

In this paper, a new digitally controlled trimming offset calibration technique by modifying the triode load bias voltages in the input differential preamplifiers is proposed to calibrate preamplifier and comparator offsets. In this technique, the trim voltages are directly connected to the bias voltages of the triode loads in the preamplifier. Therefore this technique does not affect the high-speed analog signal path. Also the technique does not require an additional power supply as in bulk voltage trimming [8], and can achieve larger offset calibration range than bulk voltage trimming [8] for the same 4-bit trimming DAC. A 2.5-GHz ERBW, 5-GS/s 4-bit flash ADC with this technique was fabricated in 65 nm CMOS.

II. ADC Architecture

Fig. 1 shows the 4-bit flash ADC architecture. The ADC includes 15 two-stage preamplifiers (A1 and A2) with each having an offset calibration circuit (OSCAL) connected to the first-stage preamplifier. The ADC also includes 15 three-stage comparators (C1, C2, and C3), 15 DFFs, and a thermometer-1

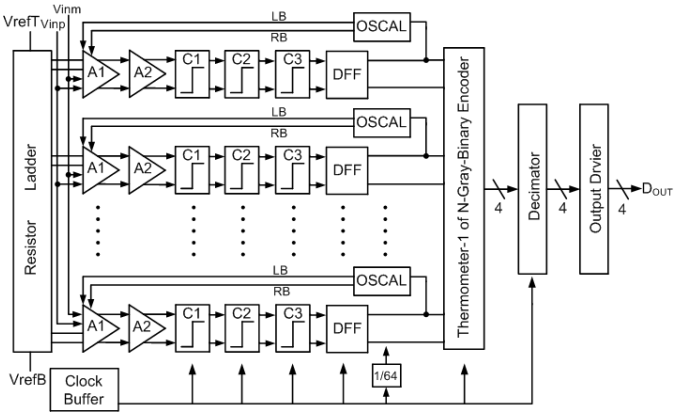


Fig. 1. ADC Architecture.

of N - gray - binary encoder. The binary output of the encoder is decimated by 64 to facilitate testing of the prototype.

III. Triode-Load Bias Voltage Trimming Offset Calibration

Fig. 2 shows the schematic of the first-stage preamplifier and the proposed offset calibration scheme. The first-stage preamplifier is a common source stage of two differential pairs with triode loads. A MOS transistor operating in deep triode region behaves as a resistor and can be used as a load in an amplifier. For $V_{SD} << 2(V_{SG} - |V_{t,p}|)$, M5 and M6 can be treated as linear resistors with value:

$$R_{on} \approx \frac{1}{\mu_p C_{ox} W/L (V_{SG} - |V_{t,p}|)}, \quad (1)$$

The resistor values can be changed by changing the bias voltages LB and RB. By setting the bias voltages LB and RB to different values, the resistances of the loads M5 and M6 are different, and then the offset can be calibrated.

The OSCAL consists of a control circuit, a 4-bit resistor string trimming DAC with a tree decoder and multiplexers (MUXs). The resistor string is shared by all 15 OSCALs, and each OSCAL has its own tree decoder. The control circuit consists of a detection circuit, a 4-bit counter, and a 4-bit register. During calibration, both the differential analog input and the differential reference input are set to zero. The digital output of the DFF after the comparator is determined only by the preamplifier and comparator offsets. A trigger signal TRG is applied to the control circuit to initiate the calibration. The ADC sampling rate is 5 GS/s and the OSCALs work at 1/64 of the sampling rate during calibration. The detection circuit in

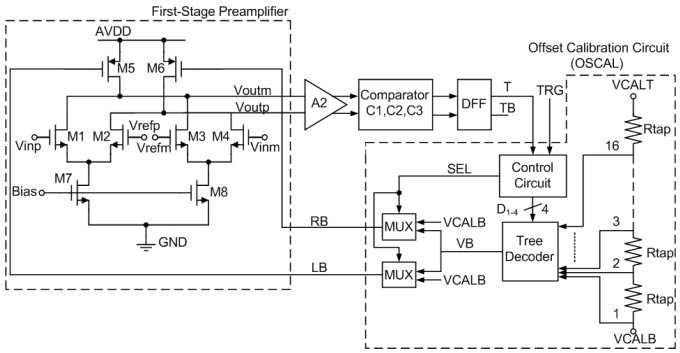
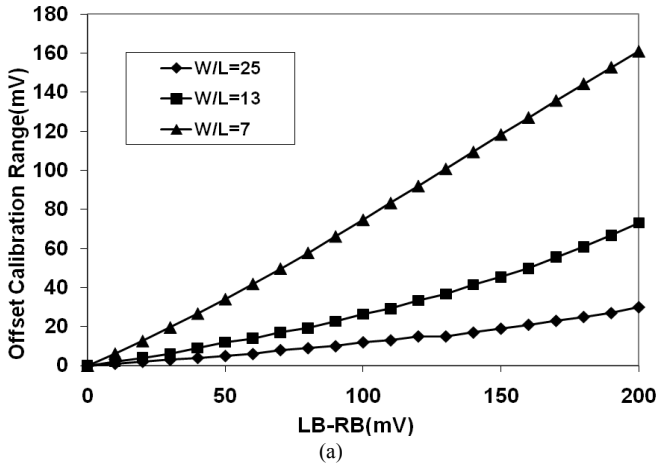


Fig. 2. Schematic of the first-stage preamplifier and the proposed triode-load bias voltage trimming offset calibration scheme.

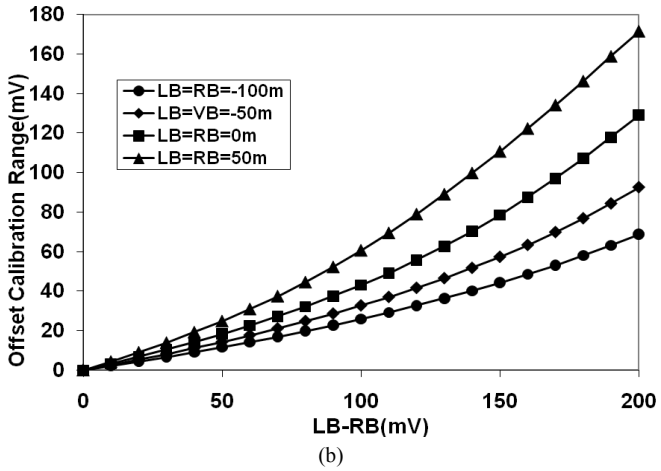
the control circuit can detect the first occurring of 0→1 or 1→0 of the digital output T after the calibration initiates. VB is set to VCALB after the calibration initiates. The value of T is stored after the calibration initiates, and SEL is set to the stored value. For zero offset, the digital output T dithers between 0 and 1, and 0 or 1 is stored, so SEL can be 0 or 1. The detection circuit detects the first occurring of 0→1 or 1→0 when T dithering between 0 and 1. The counter in the control circuit is stopped before countering up and VB is not increased and stays at VCALB. So it does not matter whether SEL = 0 or 1, the trim voltages LB and RB are both set to VCALB for zero offset. For nonzero offset, T is 0 or 1 depending on the offset polarity. If T = 0, SEL = 0, LB = VB and RB = VCALB. If T = 1, SEL = 1, LB = VCALB and RB = VB. VB is increased in a step of 1 LSB of the DAC until the output of the DFF changes or the counter has counted to 1111.

As shown in Eq. (1), there are two design parameters for the resistor value of the load. One is the aspect ratio W/L of the PMOS triode load, the other is the bias voltage of the PMOS. With a fixed bias voltage, a smaller aspect ratio W/L results in a larger resistor value R_{on} and a larger voltage gain of the preamp. A larger voltage gain results in a larger offset calibration range. With a fixed aspect ratio W/L, a higher bias voltage results in a smaller overdrive voltage, a larger resistor value R_{on}, and a larger voltage gain of the preamp, and then a larger offset calibration range.

Fig. 3 shows how the simulated output offset calibration range of the first-stage preamplifier changes with the aspect ratio W/L and the bias voltage of the PMOS triode load. In Fig. 3(a), bias voltages LB and RB are set to 0 initially, and the output offset calibration range is obtained by setting LB to higher values. It shows that larger offset calibration range is obtained with smaller W/L. In Fig. 3(b), W/L is set to 10, and larger offset calibration range is obtained with higher bias voltage. The output offset calibration range is increased from 68mV to 171mV when the bias voltage is increased from LB = RB = -100mV to 50mV. Triode-load bias voltage trimming can achieve larger output offset calibration range in the preamplifier than bulk voltage trimming [8] by choosing appropriate aspect ratio and bias voltage of the triode-load. But with larger offset calibration range, the condition



(a)



(b)

Fig. 3. Simulated output offset calibration range of the first-stage preamp varies with (a) W/L and (b) the bias voltage of the PMOS triode load.

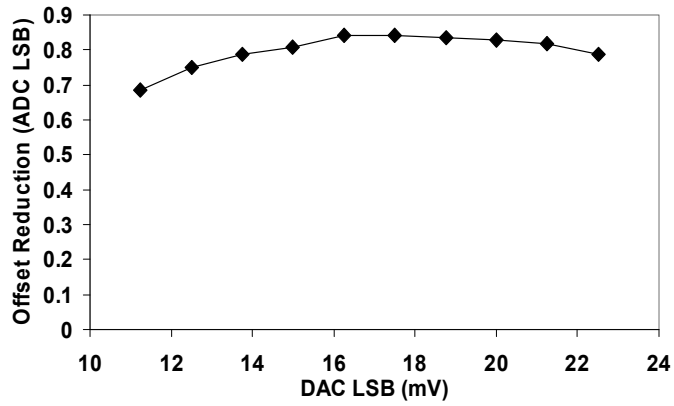


Fig. 4. Reduction value of offset standard deviation after calibration vs. DAC LSB size.

$V_{SD} << 2(V_{SG} - |V_{t,p}|)$ will not be satisfied, thus, the linearity will be degraded as shown in Fig. 3(b). This is the system nonlinearity of the triode-load bias voltage trimming offset calibration. Another contribution to the nonlinearity of the offset compensation is the nonlinearity due to the random resistor mismatch of the trimming DAC. The actual offset

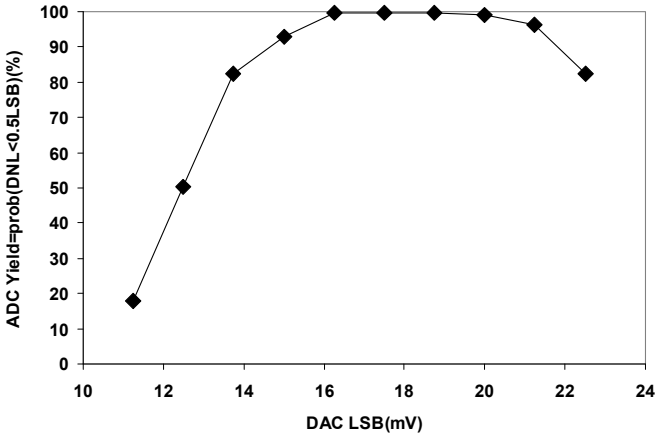


Fig. 5. ADC yield after calibration vs. DAC LSB.

calibration accuracy of the calibration scheme may be different for each step of DAC LSB during calibration due to the nonlinearity of the offset compensation, but the nonlinearity of the offset compensation does not affect the proper operation of the proposed offset calibration scheme.

In this design, the voltage value of LB and RB is set to 0 initially, and W/L of the triode load PMOS is set to 10.

After the design parameters of the preamplifier are determined, the offset calibration range and accuracy of the calibration scheme are determined by the resolution and the LSB size of the trimming DAC. The tradeoff is the digital circuit complexity and the offset calibration result achieved. A 4-bit DAC is used in this design to balance the tradeoff. In order to find the optimum value for the DAC LSB Monte Carlo simulations have been run to obtain the offset standard deviation before and after calibration. Fig. 4 shows the reduction value of offset standard deviation after calibration vs. DAC LSB size. It is shown that the largest offset reduction (or a smallest offset) after calibration is obtained when DAC LSB is 16.25 mV. Fig. 5 shows that the ADC yield for DNL<0.5LSB is 99.8% when the DAC LSB is 16.25mV. The total input referred offset calibration range is ±2.284 LSB of the ADC. The corresponding offset calibration accuracy is 0.152 LSB of the ADC. The offset calibration range of the triode-load bias voltage trimming in this design is larger than that of the bulk voltage trimming for the same 4-bit DAC [8]. In bulk voltage trimming [8], the offset calibration range is only ±0.67 LSB of the ADC. Larger offset calibration range for the calibration scheme is achieved by designing the calibrating preamplifier that has larger output offset calibration range. Thus, the offset reduction after calibration of the triode-load bias voltage trimming is larger than that of the bulk voltage trimming.

IV. Measurements

The ADC is fabricated in 65 nm CMOS and packaged in a QFN56 plastic package. Fig. 6 shows the die micrograph. The active area of the ADC is 0.0828 mm^2 including the resistor string and excluding output drivers. Fig. 7 shows the measured DNL and INL of the ADC for a 4 MHz input at 5 GS/s sampling rate. The measured DNL range was reduced from -1.00 ~ 2.34 LSB before calibration to -0.44 ~ 0.41 LSB after calibration. The measured INL range was reduced from -1.63 ~ 0.80 LSB before calibration to -0.39 ~ 0.44 LSB after calibration.

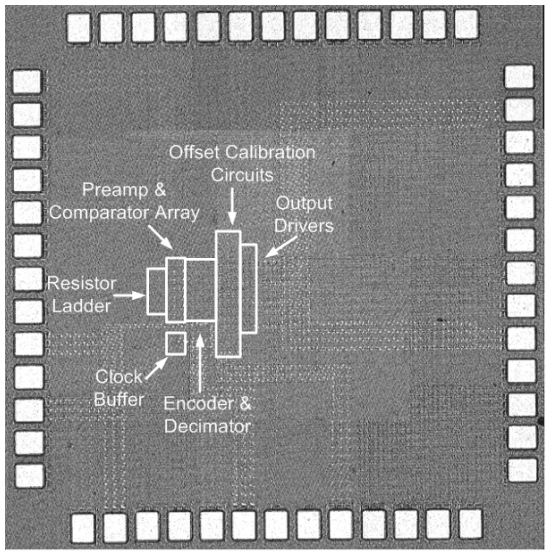
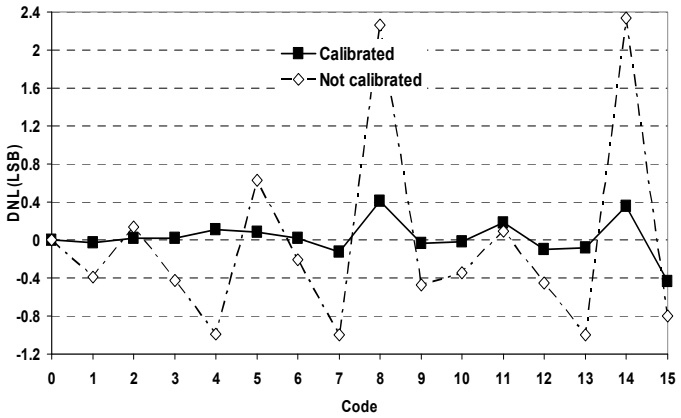
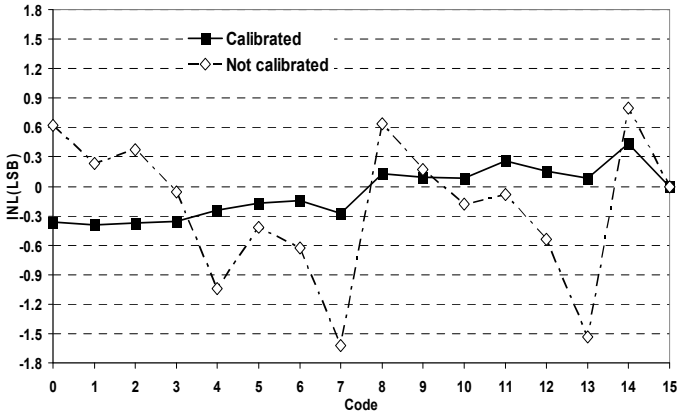


Fig. 6. Chip micrograph.



(a)



(b)

Fig. 7. Measured (a) DNL and (b) INL at 5 GS/s.

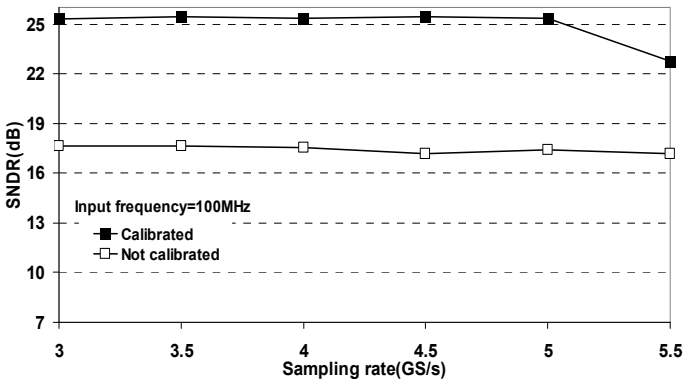


Fig. 8. Measured SNDR versus sampling rate for a 100 MHz input signal.

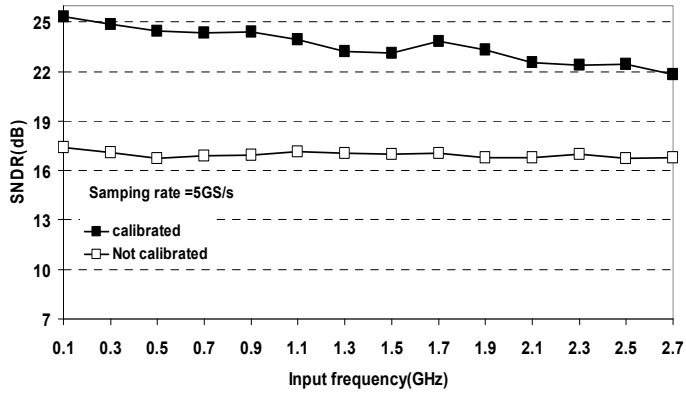


Fig. 9. Measured SNDR versus input signal frequency at 5 GS/s.

TABLE I
ADC PERFORMANCE

Technology	65 nm CMOS
Resolution	4 bits
Sampling Rate	5 GS/s
Supply	1.2 V
Power	34.3 mW@f_s=5 GS/s, f_{in}=2.5 GHz
Input Range	0.4 $V_{pp\text{-}diff}$
DNL	-0.44~0.41 LSB (after calibration) -1.00~2.34 LSB (before calibration) @ f_s =5 GS/s, f_{in}= 4MHz
INL	-0.39~0.44 LSB (after calibration) -1.63~0.80 LSB (before calibration) @ f_s=5 GS/s, f_{in}=4MHz
ENOB	3.93@f_s=5 GS/s, f_{in}=4 MHz 3.44@f_s=5 GS/s, f_{in}=2.5 GHz
FOM	0.45 pJ/convstep@5 GS/s
Active Area	0.0828 mm^2 (230 μm×360 μm) (incl. res. ladder)
Input Capacitance	90 fF

Fig. 8 shows the measured SNDR versus sampling rate for an input signal of 100 MHz before and after calibration. The SNDR was about 17.5 dB before calibration and was above 25 dB after calibration up to 5 GS/s. Therefore, there was approximately 7~8 dB improvement in SNDR after calibration up to 5 GS/s. Fig. 9 shows the measured SNDR versus the input signal frequency at 5 GS/s sampling rate before and after calibration. At 5 GS/s, the ENOB is 3.93 at low frequency inputs and is 3.44 ENOB at 2.5 GHz after calibration, i.e. the ERBW is above the Nyquist frequency. There is approximately 8 dB improvement at low frequency and 5 dB

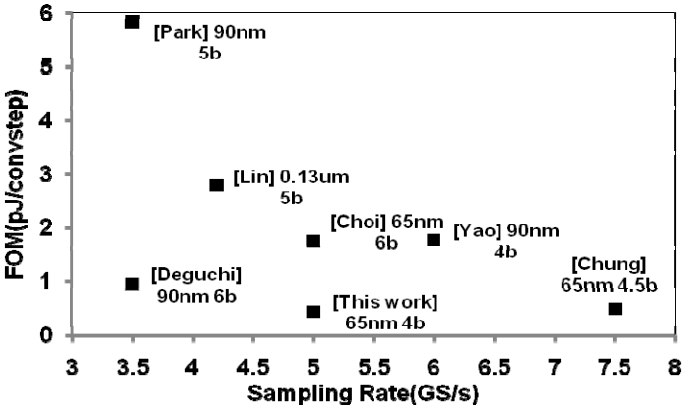


Fig. 10. Comparison to state-of-the-art high-speed low-resolution flash ADCs.

improvement at the Nyquist frequency after calibration. The power consumption is 34.3 mW at 5 GS/s and the calculated FOM is 0.45 pJ/convstep.

Table I summarizes the performance of the ADC with triode-load bias voltage trimming offset calibration. Fig. 10 compares this work with state-of-the-art high-speed low-resolution flash ADCs. They are ADCs with sampling speed higher than 3.5 GS/s, and the proposed ADC achieves the lowest FOM value.

V. CONCLUSION

A 5-GS/s 4-bit flash ADC in 65 nm CMOS is presented. The accuracy of the flash ADC is enhanced by digitally adjusting the bias voltages of the triode loads in the preamplifier. This technique dose not introduce additional capacitive loading in the analog path and avoids degrading the high-speed performance. The proposed ADC achieves 3.93 ENOB with a 2.5-GHz ERBW and a 0.45-pJ/convstep FOM at 5 GS/s.

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