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A 7-Bit 1.5-GS/s Time-Interleaved SAR ADC with Dynamic Track-and-Hold Amplifier

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***Abstract*— This paper presents a 7-bit 1.5-GS/s time-interleaved (TI) SAR ADC. The scheme achieves better isolation between channels thanks to embedding a track-and-hold (T/H) amplifier and reference voltage buffer in each channel. The proposed dynamic T/H amplifier enables high-speed, low-power operation. The prototype is fabricated in a 65-nm CMOS technology. The total active area is 0.14mm^2 and the ADC consumes 36mW from a 1.2-V supply. The measured results show the peak spurious-free dynamic range (SFDR) and signal-to-noise-and-distortion ratio (SNDR) are 52.4 dB and 39.6 dB, respectively, and an Figure of Merit (FoM) of 300 fJ/conv. is achieved.**

I. Introduction

The demand for high-speed, >1 GS/s, high-resolution, >6 bit, ADC has increased in recent wireless communication systems [1] - [5]. The TI architecture with SAR ADC is an efficient design methodology for implementing such an ADC [1]. A major design challenge of TI-ADC is to provide sufficient isolation between channels because the performance is limited by the kick-back noise induced by the input signal sampling. A TI-ADC with T/H amplifiers has been reported and achieves a better performance [2]. Such a T/H amplifier, however, results in larger power dissipation.

This paper presents a 7-bit, 1.5GS/s, 8-channel TI-SAR ADC based on a low-power design of the source follower based T/H amplifier. A key technique is expansion of the allowable settling time of the T/H amplifier. Each SAR ADC performs the signal sampling and A/D conversion in its sampling period. Thus the T/H amplifier should charge a hold capacitor with the input signal in a short time, especially in high-speed, high-resolution design. To extend the sampling time, the interleaving technique is further employed in the sub-ADC. Another key technique is dynamic operation of the T/H amplifier. The reduction of the constant current for the amplifier enhances the efficiency of the power. The proposed dynamic source follower achieves further reduction of the constant current. The additional circuitry of the proposed techniques is only one transistor. Thus the amplifier keeps the small area property. The prototype is fabricated in 65nm CMOS technology. The effectiveness of the proposed T/H amplifier is demonstrated through experimental results.

II. Architecture and Circuit Implementation

Fig. 1 shows a block diagram of the proposed TI-SAR ADC. The ADC consists of a front-end switch, 8 T/H amplifiers, and 8 SAR ADCs. The global sampling realized by the front-end switch solves the timing skew issue, which is one of the major drawbacks of TI-ADCs [3]. The bootstrapping assists on-resistance reduction of the global and the local sampling switches, resulting in better SFDR performance at high input frequency. The channel-to-channel interference of the voltage reference variation is a critical noise source in TI-ADC as well as the signal sampling kick-back effect. The proposed ADC has a voltage reference buffer for each SAR ADC individually.

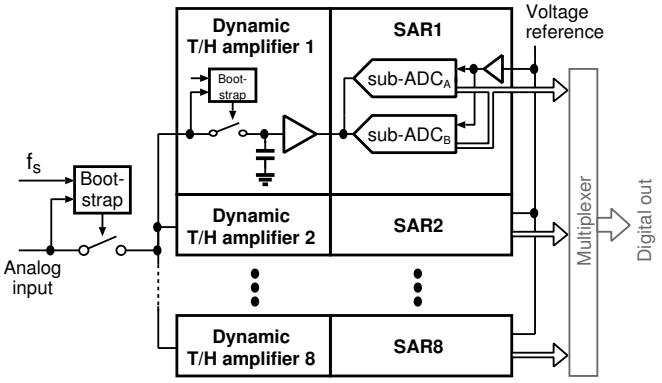

Fig. 1. Time-interleaved SAR ADC block diagram.

A. T/H amplifier

Fig. 2 shows a circuit schematic of the T/H amplifier where the first channel is considered. The circuit basically corresponds to the source-follower-based T/H circuit. The sampling network of the T/H amplifier consists of a local sampling switch, $\mathrm{SW_{ch1}}$, and a sampling capacitor, $\mathrm{C_{ch1}}$. The switches, $\mathrm{SW_{SAR,A}}$ and $\mathrm{SW_{SAR,B}}$, and the capacitors, $\mathrm{C_{SAR,A}}$ and $\mathrm{C_{SAR,B}}$, represent the sampling networks of the sub-ADCs. The switches, $\mathrm{SW_{r1}}$ and $\mathrm{SW_{r2}}$, are used for the proposed dynamic operation. The timing diagram of the T/H amplifier for the first channel is shown in Fig. 3. The phase, Φ_i $(i = 1, 2, \cdots, 8)$, means the local sampling where the phase of each clock is shifted from Φ_{i-1} by $2\pi/8$ synchronizing f_s. The circuit operation is divided into three phases: reset, track and hold. First, the circuit performs the reset operation when Φ_8 is high. The input and output nodes of the source follower are connected to the ground by turning $\mathrm{SW_{r1}}$ and $\mathrm{SW_{r2}}$ on. Next, track and hold are performed by Φ_1. The timing of the global sampling is determined by the fall edge of f_s. The sub-

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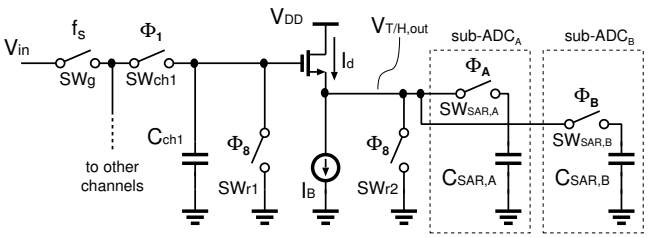

Fig. 2. Proposed dynamic T/H amplifier and two sampling capacitors of the SAR ADC for the first channel.

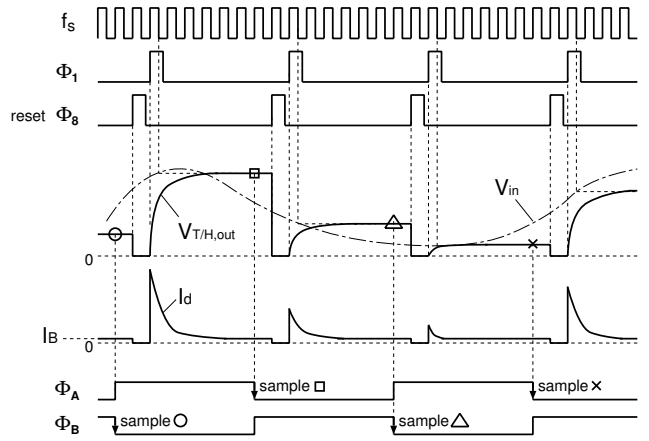

Fig. 3. Timing diagram of the Proposed dynamic T/H amplifier and 2 TI-SAR ADC.

ADCs sample the output of the T/H amplifier, $\mathrm{V_{T/H,out}}$, at the falling edge of Φ_A and Φ_B.

In a traditional source follower, since the discharge speed for the load capacitor, $\mathrm{C_{SAR,A}}$ or $\mathrm{C_{SAR,B}}$, is limited by its slew rate, the power consumption strongly depends on the required speed performance. In the proposed T/H amplifier, the discharge operation is not needed during the track and hold phases because the output voltage always starts from zero in the track phase owing to the reset. Therefore, the settling speed is independent of the amount of the bias current. This property is essential for realizing a high-speed T/H amplifier with low power consumption. The additional reset operation consumes only one-clock period in the hold phase. Note that the bias current should be set to a certain small value, not zero. If $I_B = 0$, there is a slight leak current after settling, which causes a ramped-up waveform of the output voltage, $\mathrm{V_{T/H,out}}$. Although there is still a little bias current, the proposed T/H amplifier can perform high-speed operation under low power consumption compared with the conventional one. In [6] a dynamic T/H amplifier has been reported, which introduces only $\mathrm{SW_{r1}}$ not $\mathrm{SW_{r2}}$. The completion of the reset, however, still depends on the bias current of the source follower and thus large power is required for fast reset operation.

B. SAR ADC

Fig. 4 shows the circuit schematic of the SAR ADC in a channel. Two sub-ADCs are employed in each channel.

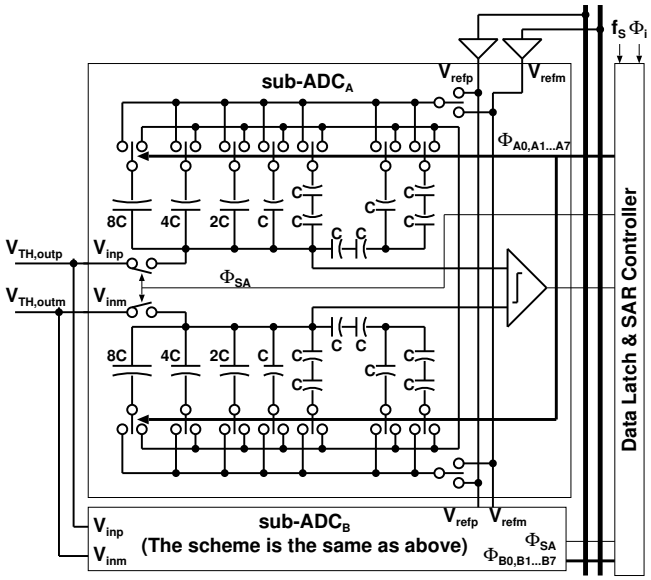

Fig. 4. Circuit schematic of the SAR ADC for the first channel.

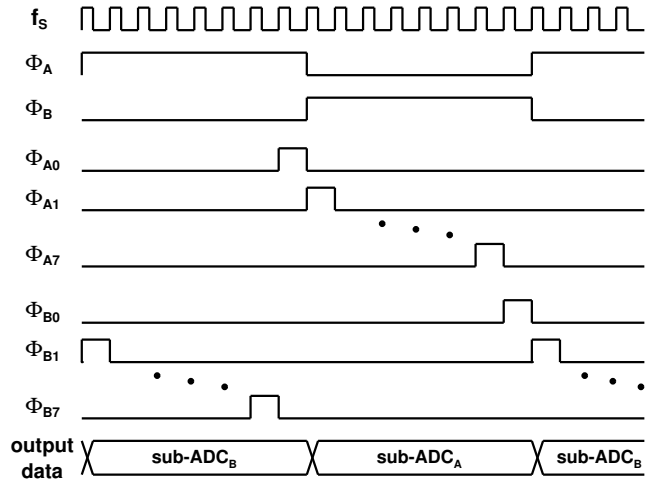

Fig. 5. Timing diagram of the SAR ADC for the first channel.

The sub-ADC consists of a binary weight capacitor DAC, a comparator and a control logic. The comparator consists of a pre-amplifier and a dynamic latch. The SAR architecture uses a capacitive split array consisting of a 5-bit main-array and a 2-bit sub-array. The unit capacitance is 11fF and the total sampling capacitance is 176 fF differential, where a stacked capacitor cell is used for the unit capacitor. To minimize the circuit area, the SAR quantizes the sign of the T/H output to give the MSB decision. Although the seven decisions and sign decision result in 8-bits resolution, one bit is used for the gain and offset calibration.

The mismatch of the gain and offset among channels is calibrated in the digital domain. A zero differential signal and a single tone sine wave are used for the measurement of the offset and gain, respectively. The ADC full scale is 1 $\mathrm{V_{pp\text{-}diff.}}$

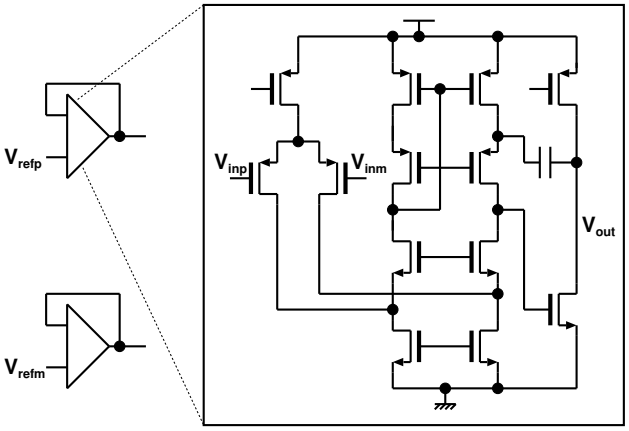

Fig. 6. Amplifier of the voltage reference buffer embedded in the channel.

including about 20% over range for the digital calibration.

The problem of the low-power T/H amplifier design is short sampling period because the SAR ADC requires a number of bit decisions in addition to the sampling operation. To solve this, we also utilize the interleaving technique to the channel. The key advantage of the proposed SAR ADC is expanding the sampling period and relaxing the power consumption of the T/H amplifier. Fig. 5 shows the timing diagram of the SAR ADC. The sampling frequency of the sub-ADC is set to $f_s/16$ and each sub-ADC operates in two time-interleaving manner, where f_s is the sampling frequency of the TI-ADC. The eight clock periods can be assigned for the sampling, and the hold time of the T/H amplifier increases eight times compared with a conventional approach.

The operation of each sub-ADC is divided into two phases, sampling and SAR A/D conversion. The circuit of the sub-$\mathrm{ADC_A}$ is described first. During Φ_A is active, the top plates of the MSB bank in the DAC are connected to the T/H amplifier output and the signal is sampled onto the DAC. The input of the comparator is also connected to the T/H amplifier output and the comparator decides the MSB at the end of the sampling phase. After sampling, the SAR A/D conversion is operated. At Φ_{B0} is active, the floating nodes of the DAC are connected to the common-mode voltage for initializing. The sub-$\mathrm{ADC_B}$ begins the sampling operation at the Φ_{A1} is active. The circuit operation is the same as the sub-$\mathrm{ADC_A}$.

The op-amp used for voltage reference buffer is shown in Fig. 6. The load capacitance affects the phase margin of the buffer. In the SAR, the load capacitance is changed by the conversion phases. The single-stage op-amp is usually used for the high-speed operation. However, the small load capacitance decreases the phase margin and the phase compensation capacitor requires additional power consumption. To realize a sufficient phase margin for a small capacitance at the LSB conversion phase, two-stage configuration is adopted for the buffer. To increase the phase margin at the MSB conversion phase, the conventional improved compensation technique is adopted [7]. The open-loop gain, 30 dB, and unity gain frequency at the large load capacitance, 1.3 GHz, are confirmed by SPICE simulation. While the buffer consumes relatively large power, i.e. about 30 %, the buffering of the voltage reference guarantees better isolation for the channel compared with the buffer less architecture.

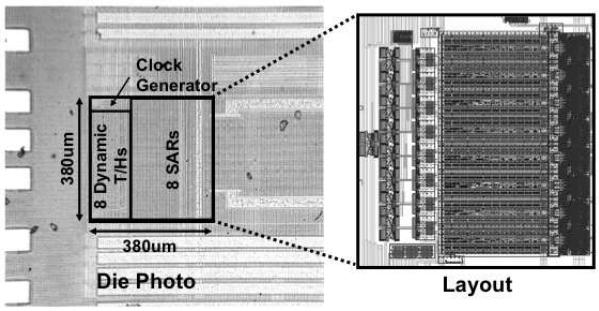

Fig. 7. Chip microphotograph and its expanded layout.

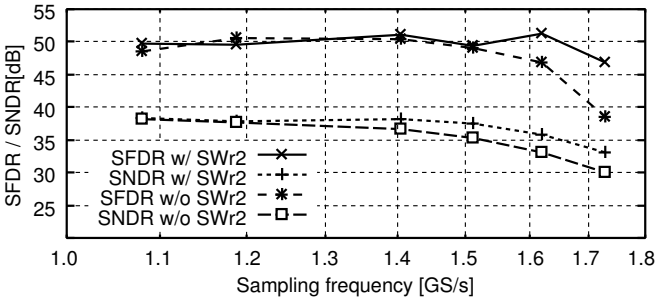

Fig. 8. Measured SNDR and SFDR versus sampling frequency.

III. Measured Results

A 7-bit 1.5-GS/s TI-SAR ADC using the above techniques is fabricated in a 65nm CMOS process with MOM capacitors and the chip microphotograph is shown in Fig. 7. The core of the ADC including the T/H amplifier, reference buffer, clock buffer and the current generator occupies $380\mu\mathrm{m} \times 380\mu\mathrm{m}$. The calibration logic is not implemented in the prototype. The measured results of the SFDR and SNDR in Fig. 8 show the effectiveness of the proposed dynamic operation, where the active line and dash line are with and without dynamic operation. The performance of without dynamic operation is measured by gating the control signal of $\mathrm{SW_{r2}}$. In the same power consumption, the SFDR and SNDR in a high-frequency region are more 5dB and 2dB larger than that without one. For achieving the same performance, the required total power for T/H amplifier is two times larger than that of the proposed T/H amplifier.

Fig. 9 shows the ADC output spectrum with the input frequencies at 19MHz and 742MHz. The third-harmonic distortion determines the SFDR: 51.8 dB at low frequency. At near the Nyquist frequency, the SFDR is degraded to 49.9dB due to the distortion introduced by the timing mismatch between the channels. Fig. 10 shows the measured SFDR and SNDR of the ADC with $\mathrm{SW_{r2}}$ over the Nyquist frequency,

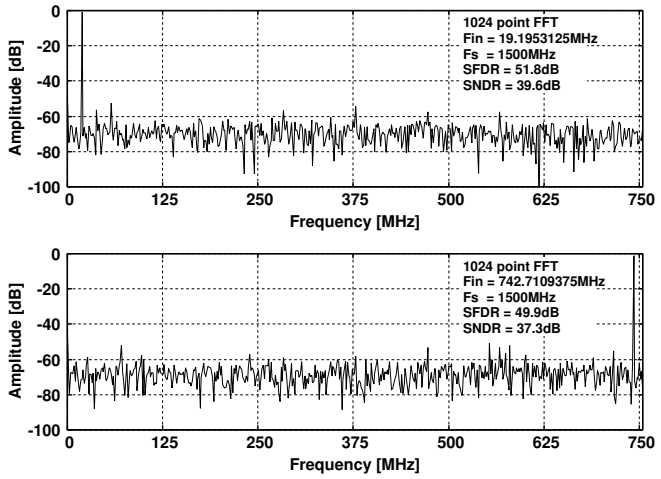

Fig. 9. ADC output spectrum. The input is either a 19 MHz and 742 MHz sine wave (full-scale) sampled at 1.5-GS/s.

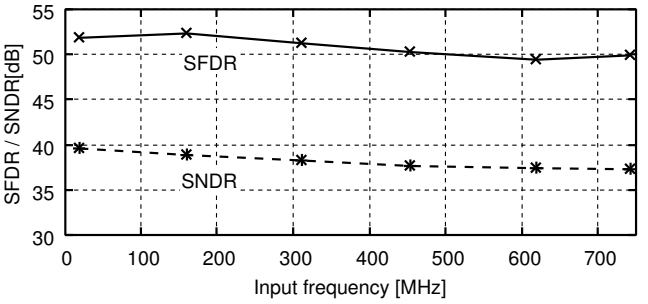

Fig. 10. Measured SNDR and SFDR versus input frequency.

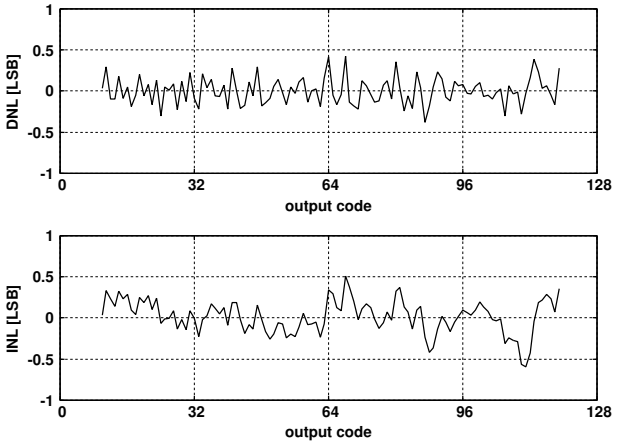

Fig. 11. Measured DNL and INL sampled at 1.5-GS/s.

TABLE I

PERFORMANCE SUMMARY AND COMPARISON.

Ref.	[1]	[2]	[3]	[4]	[5]	This work
Process [nm]	45	130	130	90	65	65
V_{DD} [V]	1.1	1.2	1.2	1.3	1.0	1.2
Power [mW]	50	175	250	46	35	36
f_s [GS/s]	2.5	1.35	1.0	1.1	1.5	1.5
Area [mm^2]	1.0	1.6	3.5	0.19	0.5	0.14
SFDR [dB]	43	–	58.5	–	43	52.4
ENOB [bit]	–	7.7	8.88	6.52	5.8	6.29
(@ $f_s/2$)	(5.4)	(–)	(8.35)	(5.7)	(–)	(5.9)
FoM [fJ/conv.]	480	600	530	460	420	300

where the sampling frequency is 1.5-GS/s. The peak SNDR of 39.6 dB, corresponding to an ENOB of 6.29 bit, and 5.9 ENOB near the Nyquist frequency are marked. The differential nonlinearity (DNL) and integral nonlinearity (INL) are illustrated in Fig. 11. At 1.5-GS/s, the DNL and INL are +0.42/-0.38 LSB and +0.51/-0.59 LSB, respectively. The performance summary of the designed ADC and comparison with other high-speed, high-resolution ADCs are shown in Table I. The designed ADC consumes 36 mW from a power supply of 1.2 V. The lowest FoM of 300 fJ/conv. and the smallest active area, 0.14 mm^2, in Table I are achieved. In [4], although relatively low FoM with small active area has been accomplished, its ERBW is actually less than the Nyquist frequency, 300 MHz. The comparison in Table I shows the designed ADC is superior in terms of FoM and active area among high-speed, high-resolution ADCs.

IV. CONCLUSIONS

A 1.2 V 7-bit 1.5-GS/s 8-channel TI-SAR ADC has been presented. The interleaving architecture of the capacitor DAC in the channel and the power efficient dynamic T/H amplifier enable high speed and low power ADC operation. The simple structure of the presented T/H amplifier keeps small area property. Embedding a T/H amplifier and a voltage reference buffer in each channel provides the channel-to-channel isolation and better performance over 6-bit ENOB is achieved. The prototype is fabricated in a 65-nm CMOS technology. The designed ADC consumes 36 mW from a power supply of 1.2 V. The presented ADC achieves a power efficiency, 300fJ/conversion-step that is the best design with similar speed and resolution published to date.

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