A 2.5-GS/s 30-mW 4-bit Flash ADC in 90nm CMOS

Timmy Sundström and Atila Alvandpour

Division of Electronic Devices, Department of Electrical Engineering
Linköping University, SE-584 39 Linköping, Sweden
E-mail: {timmy, atila}@isy.liu.se

***Abstract*—A 2.5 GS/s flash ADC, fabricated in 90nm CMOS, avoids traditional power, speed and accuracy trade-offs by using comparator redundancy with power-gating capabilities. Redundancy removes the need to control comparator offsets, allowing the large process-variation induced mismatch of small devices in nanometer technologies. This enables the use of small-sized, ultra-low-power comparators. Measurement results show that the ADC dissipates 30 mW at 1.2 V. With 63 gate-able comparators, the ADC achieves 4.0 effective number of bits.**

***Index Terms*—Analog-digital conversion, CMOS analog integrated circuits, high-speed electronics, power demand.**

I. INTRODUCTION

As CMOS technologies continue to scale down deeper into the nanometer regime the process variations has become an ever increasing problem for the design of any VLSI circuit [1]. The within-die variations of random dopant fluctuations and process imperfections, related to the sub-wavelength lithography, cause large variations of circuit parameters such as transistor threshold voltage [2], [3]. Device mismatch will increase with the technology scaling and pose greater challenges for accuracy control of analog and mixed-signal circuits.

High-speed low resolution ADCs are required in both wire transmission such as gigabit ethernet as well as wideband wireless receivers. Monolithical integration requires the ADC to be implemented in nanometer CMOS processes where the increasingly large process variations can cause significant overhead in terms of power and complexity.

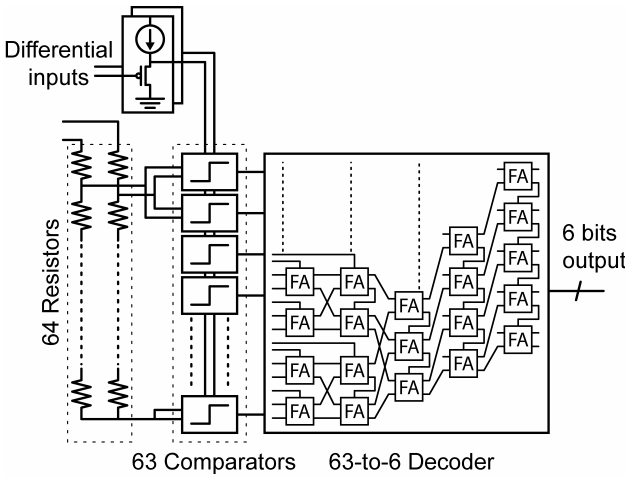

Fig. 1. Flash ADC Architecture

Traditionally accuracy in ADCs has been achieved by sizing in the analog domain together with calibration methods. In [4] redundancy was used to relax the accuracy constraints of the comparators in the ADC and in [5] a combination of redundancy and calibration was used to lower the power dissipation through minimizing the power used by the redundant circuits.

The aim of this paper is to show how redundancy can be used to achieve an overall low power design with the sole focus on designing for speed and low power at the building block level. As the mismatch induced comparator offsets will get worse with scaling, using comparator redundancy is a means for taking full advantage of decreased feature sizes in future CMOS processes, with higher speeds and lower power dissipation.

This paper is organized as follows, in section II the effect of comparator redundancy is explained and a description of the ADC architecture is given. This is followed by a detailed design explanation of the ADC components. Section III presents the measurement results of the ADC and a comparison with other designs. The paper is concluded in section IV.

II. ADC ARCHITECTURE

In traditional ADCs, careful design choices must be made in the trade-offs between power, speed and accuracy [7]. However, comparator redundancy can be used to break this link [5]. Redundancy is commonly used in the design of pipelined ADCs to reduce the accuracy requirements of the comparators in the MDAC stages. However, in Flash ADCs, it has not been used to the same extent. In [6] and [4] redundancy is used to increase the yield and provide the desired resolution. The presented ADC utilizes that, with redundant comparators, the accuracy requirement is vastly reduced. This means that the comparator sizing can be done with the concern for speed and power alone to achieve a low-power ADC by allowing large mismatch induced comparator offsets.

Figure 1 show the block diagram of the ADC architecture.

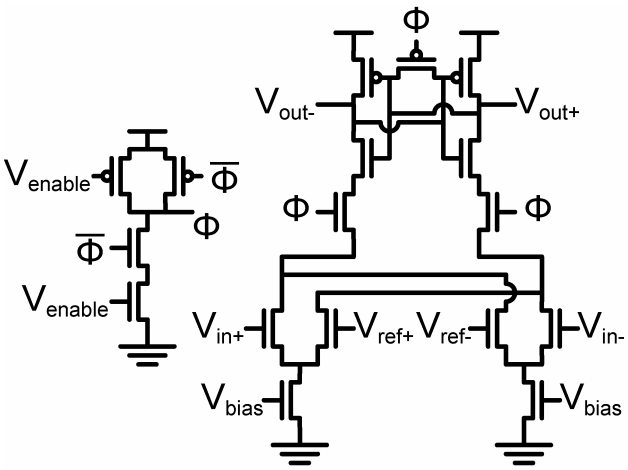

Fig. 2. Differential pair sense-amplifier based comparator and clock-gating circuit

The input signal is buffered through a source follower stage to reduce kick-back effects and drive the comparator array consisting of 63 comparators. A register, which is programmed through an external port, controls which of the comparators should be enabled. This way, individual comparators that do not contribute towards an increased resolution can be disabled to save power.

The accuracy of the individual comparators in the ADC will be deteriorated due to process variations, resulting in a non-perfect thermometer coded output. In order to avoid complicated bubble-suppression logic a summing decoder is used to efficiently convert the output vector into binary.

A. Comparator

The ADC uses a differential-pair sense-amplifier based comparator as shown in figure 2. With 63 comparators in the array, the number of comparators affecting the input buffer and reference ladder has increased by a factor of four compared to what is ideally needed to achieve 4-bit resolution. This has caused the kick-back charge from the comparators to the input buffer and reference network to increase. Compared to a typical sense-amplifier comparator that has a clocked tail NMOS transistor, the proposed ADC use a comparator with the clocked transistors placed between the cross coupled

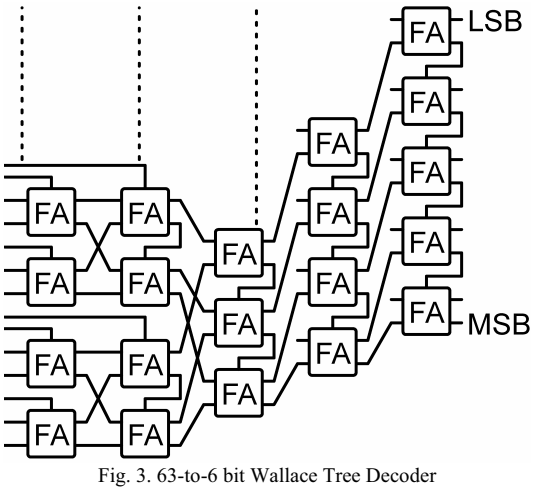

Fig. 3. 63-to-6 bit Wallace Tree Decoder

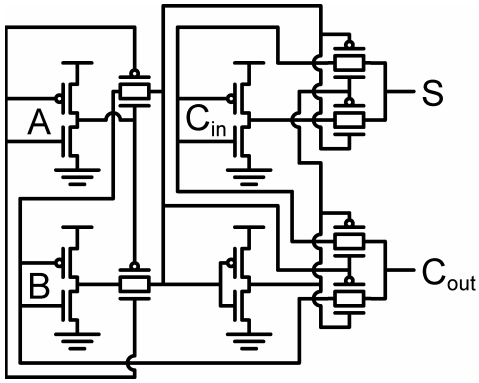

Fig. 4. A transmission gate full adder cell

invert pair and input transistors. This is to prevent the source and drain of the input transistors to be pre-charged, since the simultaneous discharge of these nodes cause common-mode kickback to the input. With the increased number of comparators needed for redundancy this common-mode kick-back cause too large transients on the reference and input voltages. By placing the clocked transistors above the input pair, the pre-charge of these nodes is prevented and the common-mode kick-back charge is reduced by 6x, reducing the power dissipation in the reference ladder and input buffer by the same amount [8].

As the accuracy of the comparators is handled by redundancy, the transistor sizing can be done without regard for mismatch with the focus only on speed and power. For this design, the transistor widths were smaller than 1 µm with the exception of the equalization PMOS which was 1.45 µm in order to remove the memory effects. The small transistor sizes allow ADCs of this architecture to take full advantage of the decreased feature sizes in future CMOS technologies.

In order to save power, the comparators that do not contribute to the effective resolution are disabled. This is implemented using clock-gating as shown in figure 2. The local clock-gating circuit is implemented as a NAND-gate to emphasize the rising edge of the clock at minimal clock load. When disabled, the comparators will be kept in the latching state and changes in the input signal will not affect the output or dissipate power due to switching. Since the latched output could be either high or low the enabled signal is also used to reset the output signal in the subsequent latch to prevent the disabled comparator from biasing the final output.

The references to the comparators are generated by a differential resistor ladder. The resistor ladder is implemented with capacitively decoupled internal nodes in order to further reduce the transient effect that both common-mode and differential kick-back cause.

B. Decoder

In a traditional ADC, the output of the comparator array is thermometer coded since the accuracy of the individual comparators is well controlled. When the accuracy requirements of the comparators can be ignored, due to the use of redundancy, the output will no longer be thermometer coded because of the large expected mismatch induced comparator offsets. The output array is then effectively converted to binary by using a summing decoder that

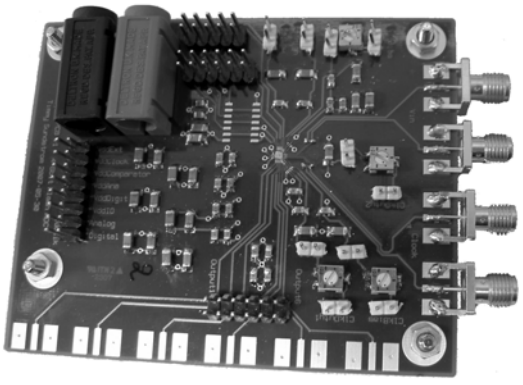

Fig. 5. The PCB with the directly bonded die.

disregards internal comparator order. This is implemented as a 6-bit Wallace Tree decoder as shown in figure 3.

As the critical path of a 6-bit Wallace Tree decoder is 9 Full Adders [9] the decoder is pipelined to handle the throughput of a multi-GS/s ADC's [6].

The full-adders used in the Wallace Tree decoder are the transmission gate based full adders shown in figure 4, which are chosen for the best resulting power-performance trade-off for the entire pipelined decoder based upon a target sampling frequency of 3 GS/s.

C. Calibration

To calibrate the ADC for 4-bit, low-power operation, each comparator is characterized with a trip-point. This is externally controlled by a computer, which characterize the comparators one by one through a calibration port. Once the trip points are known, the optimal number of comparators required for 4-bit performance is selected based on the ideal transfer function. The rest of the comparators are disabled to save power. The architecture allows any number of comparators to be enabled to provide the desired 4 bit functionality.

III. Measurement Results

The ADC was designed and manufactured in a 7 metal, 90nm CMOS process and the active die area is 0.04 mm^2. For measurements, the die was directly bonded unto a PCB, as shown in figure 5, to reduce the parasitics. The micrograph of the chip is seen in figure 6.

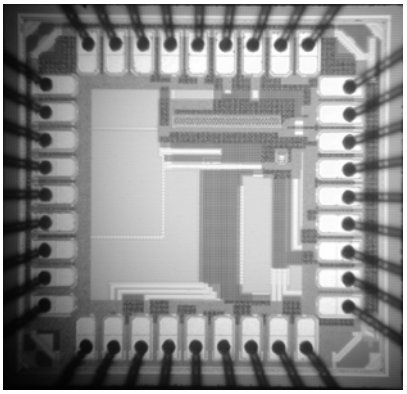

Fig. 6. Chip micrograph

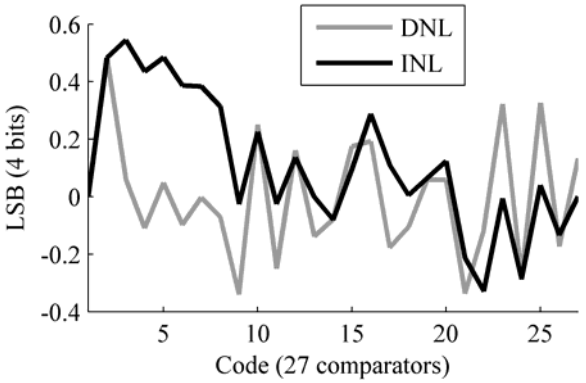

Fig. 7. Differential non-linearity (DNL) and integral non-linearity (INL) of the ADC

With the ADC operating at a sampling frequency of 2.5 GS/s the maximum effective number of bits achieved after calibration was 4.0 bits when 27 comparators were enabled. This was measured for an input signal of 1 MHz. The differential and integral non-linearities (DNL and INL) related to an LSB of the 4 bit output are given in figure 7. The maximum absolute DNL and INL were 0.48 and 0.54 LSBs respectively.

Operating with low input frequencies the effective number of bits were above 3.87 for sampling frequencies up to 2.8 GS/s as seen is figure 8. Above this, the decoder starts to experience timing problems, and spikes appear at the output.

For input frequencies between DC and Nyquist and a sampling frequency of 2.5 GS/s, the signal to noise and distortion ratio (SNDR) is depicted in figure 9. The effective range bandwidth, where the SNDR has decreased by 3 dB, was 250 MHz.

Note that at 2.8 GS/s the ADC achieves 3.98 effective bits and dissipates 34.4 mW but the effective resolution bandwidth had degraded compared to that up to 2.5 GS/s.

The total power dissipation in the ADC, measured at 2.5 GS/s while running at a power supply voltage of 1.2 V, was 30.2 mW. Out of these, 16.8 mW (55%) were used for clocking and clock generation, 9.4 mW (31%) for the input buffer, 0.25 mW (1%) for the reference generation, 1.7 mW (5.5%) were dissipated in the comparator array, and 2.4 mW (7.5%) in the digital logic.

The performance of the ADC is summarized in Table I together with other state-of-the-art ADCs with sampling rates

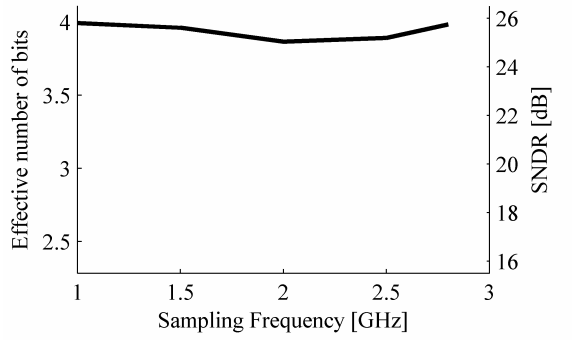

Fig. 8. Effective number of bits and SNDR vs Sampling Frequency

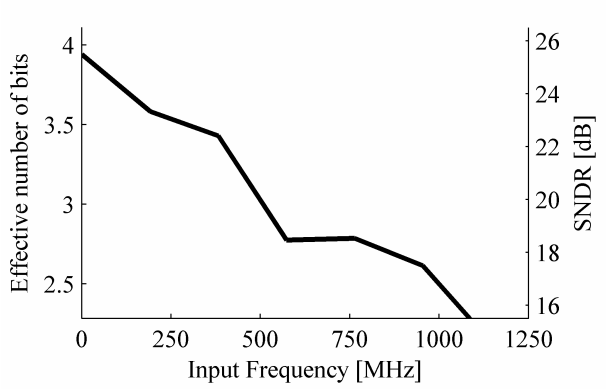

Fig. 9. Effective number of bits and SNDR vs input frequency

above 2 GS/s. Here, two common figures of merit are used to compare ADC performance, FoM1 and FoM2 which are given as follows:

$$FoM1 = \frac{P}{2^{ENOB} \cdot f_s} \quad (1)$$

$$FoM2 = \frac{P}{2^{ENOB} \cdot 2 \cdot ERBW} \quad (2)$$

where P is the power dissipation, ENOB the effective number of bits, f_s the sampling frequency, and ERBW the effective resolution bandwidth.

The authors of [4], [6], [11], [12] and [14] also report effective resolution bandwidths lower than the Nyquist frequency. However, the most common cause is the increased effect of sampling jitter at higher input frequencies. In our design the problem is related to an error in the layout of the input buffer, causing the two differential source follower circuits to behave differently. For the next generation of the chip the bandwidth performance will be improved, and closer to that indicated by the simulations with extracted parasitics as larger than the nyquist frequency. Although the bandwidth was reduced, the proposed ADC achieves a FoM1 of 0.76 pJ/Conversion-step and a FoM2 of 3.1 pJ/Conversion-step, proving comparator redundancy as an efficient method in designing low-power flash ADCs.

IV. Conclusion

Through the use of redundancy a low-power high-speed flash ADC has been designed. The redundancy allowed the comparators to be designed with trade-offs only between speed and power. The use of ultra-low-power comparators resulted in a 2.5 GS/s, 4-bit ADC that dissipates 30.2 mW of power. The resulting FoM1 of 0.76 pJ/Conversion-step is, to the author's best knowledge, the best reported of flash ADCs with sampling rates over 2 GS/s. Although the bandwidth was reduced, the FoM2 is still amongst the state-of-the-art for high-speed flash ADCs.

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TABLE I – PERFORMANCE COMPARISON

Author Year	Effective Number of Bits (ENOB)	Sampling Frequency (f_s)	Effective Resolution Bandwidth (ERBW)	Process	Power Dissipation (P)	FoM1	FoM2
[4] 2004	6.0	4 GS/s	1 GHz	0.13µm CMOS	990 mW @ 1.5 V	3.87 pJ/Conv-Step	7.73 pJ/Conv-Step
[6] 2007	3.9	4 GS/s	100 MHz	0.18µm CMOS	608 mW @ 1.8 V	10.2 pJ/Conv-Step	20.4 pJ/Conv-Step
[10] 2008	5.3	5 GS/s	2.5 GHz	65nm CMOS	320 mW @ 1.3 V	1.62 pJ/Conv-Step	1.62 pJ/Conv-Step
[11] 2005	5.5	2 GS/s	250 MHz	0.18µm CMOS	145 mW @ 1.8 V	1.60 pJ/Conv-Step	6.41 pJ/Conv-Step
[12] 2007	4.0	5 GS/s	528 MHz	0.13µm CMOS	113 mW @ 1 V	1.41 pJ/Conv-Step	6.69 pJ/Conv-Step
[13] 2007	4.9	3.5 GS/s	1.75 GHz	90nm CMOS	98 mW @ 900 mV	0.95 pJ/Conv-Step	0.95 pJ/Conv-Step
[14] 2007	4.2	4.2 GS/s	1.75 GHz	0.13 µm CMOS	180 mW @ 1.2 V	2.33 pJ/Conv-Step	2.80 pJ/Conv-Step
This Work	**4.0**	**2.5 GS/s**	**300 MHz**	**90nm CMOS**	**30.2 mW @ 1.2 V**	**0.76 pJ/Conv-Step**	**3.1 pJ/Conv-Step**