A 4.5 GHz to 5.8 GHz Tunable ΔΣ Digital Receiver with Q enhancement

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***Abstract* — A digital receiver tunable from 4.5 GHz to 5.8 GHz is reported for the first time. The circuit is based on a 40 GS/s continuous-time bandpass ΔΣ ADC with Q-enhancement. In addition to the center frequency, the receiver bandwidth is independently tunable between 120 MHz and 500 MHz. An SNR of 37.9 dB is measured at 5 GHz over 500 MHz bandwidth. Center frequency scaling of bandpass digital receivers from 2 GHz to 5.8 GHz is shown without changing the digital section and clock frequency of the ADC. The circuit, which consumes 2.09W from 2.5V supply, can be used as a broadband RF sampler for 5.8 GHz WLAN, or as the digital IF of a 60 GHz radio.**

***Index Terms* — Analog-to-digital converter, bandpass, continuous-time, delta-sigma, direct sampling.**

I. Introduction

Continuous-time bandpass ΔΣ ADCs with GHz clocks have been reported with center frequencies up to 2GHz [1-4]. This work is the first to demonstrate theoretically and experimentally that they can be scaled in frequency from 2GHz to 5.8GHz without changing the digital section and the sampling rate of the ADC. An analytical and experimental performance comparison of a 2GHz bandpass ΔΣ ADC in [5] and of the 4.5GHz to 5.8GHz bandpass ΔΣ ADC developed in this work shows that the SNR is a strong function of the center frequency and of the filter quality factor Q. The 5GHz ADC employs the same quantizer, DACs and clock distribution as the 2GHz version [5], while having a modified loop filter with 25% tuning range. The resulting tunability of the entire receiver allows for operation in the 5.2GHz to 5.8GHz WLAN bands, or in the IF stage of a 60GHz radio system, where a bandwidth larger than 1.5GHz must be covered, either directly or through tuning.

II. System Level Analysis

Figure 1 illustrates the system-level architecture of the ADC with PLL. The ADC is a fourth-order bandpass continuous-time ΔΣM with RZ DACs for immunity against loop delay [1, 4]. The single-bit quantizer is a D-type flip-flop, realized with two latches in a master-slave configuration, and clocked by a 40GHz PLL [6]. The loop was designed in the frequency domain by describing the switching effect of the quantizer with a rational function approximation [4]. Once the noise transfer function (NTF) is known, the linearized ΔΣ loop model leads to a simple and accurate calculation of SNR. For

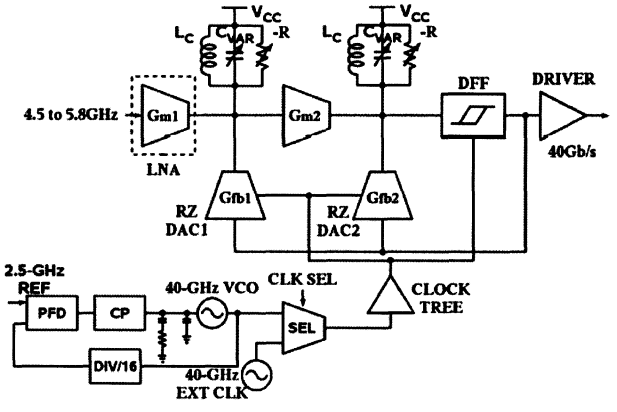

Figure 1: Block diagram of the direct sampling receiver.

a bandpass loop with transconductances G_m and G_{fb} in the forward and feedback paths, respectively, the filter transfer function is

$$H(s)=\frac{G_m}{C}\frac{s}{s^2+\frac{\omega_o}{Q}s+\omega_o^2} \quad (1)$$

The noise transfer function NTF(s) can be shown to be

$$NTF(s)=\frac{\left(s^2+\frac{\omega_o}{Q}s+\omega_o^2\right)^2}{\frac{G_{fb2}}{C}s^4+\left(\frac{G_{fb1}G_{m2}}{C^2}+\frac{G_{fb2}\omega_o}{CQ}\right)s^3+\frac{G_{fb2}\omega_o^2}{C}s^2} \quad (2)$$

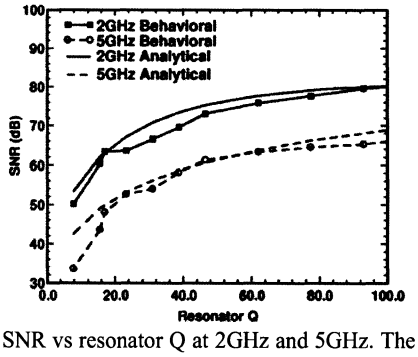

Figure 2: SNR vs resonator Q at 2GHz and 5GHz. The SNR was estimated with an analytical model using (2) and (3), and with a behavioral model simulated in Matlab Simulink.

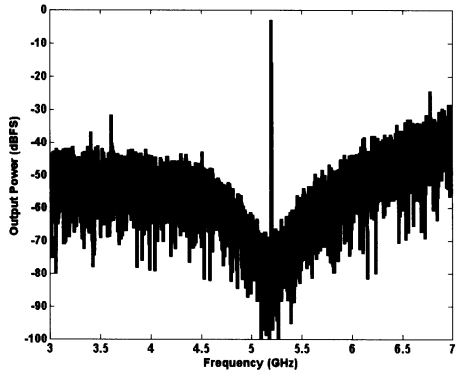

Figure 3: System level simulation of ΔΣ ADC at 5.2 GHz (NFFT=65536).

To find the total quantization noise one has to integrate (2) over the band of interest BW. The SNR can then be calculated as the difference between the full-scale power level, P_{FS}, and the integrated quantization noise, P_{QN}, for a quantizer step size Δ

$$SNR = P_{FS} - P_{QN}$$
$$= P_{FS} - \frac{\Delta^2}{12F_S}\int_{2\pi\left(f_o-\frac{BW}{2}\right)}^{2\pi\left(f_o+\frac{BW}{2}\right)} \left|NTF(j\omega)\right|^2 d\omega \quad (3)$$

Integration with a symbolic mathematical tool using (3) shows that the SNR degrades by a factor approximately equal to the frequency ratio when the center frequency is changed from 2GHz to 5GHz (Fig. 2). This relationship was also verified in system-level simulations. The simulated SNR is 61dB over 60MHz at 2GHz with a filter Q of 17 [5]. At 5GHz, the simulated SNR reduces to 48.1dB over the same bandwidth and with the same filter Q. To reach an SNR of 61dB at 5GHz, the filter Q has to be at least 45. A master-slave flip-flop quantizer topology was preferred over a three-latch solution because of its higher stability. Behavioral simulation of the loop shows that, unlike the situation in the 2GHz design, the extra delay contributed by the third latch cannot be compensated by adjusting the feedback coefficients of the DACs. The output spectrum resulting from the system level simulation of the ADC at 5.2GHz is reproduced in Fig. 3.

III. Circuit Design

The transconductance stages of the loop filter are implemented with MOS-HBT cascode amplifiers, as shown in Fig. 4. This topology ensures high input linearity and low noise [4]. Since the first transconductance block G_{m1} serves as the input stage of the entire receiver, it is designed as an LNA. In contrast to the input stage of a 2GHz digital receiver [5], where a large external inductor is needed to achieve 50Ω noise and impedance matching, the transconductance cell of the 5GHz ADC can be matched to the 50Ω source impedance with on-chip inductors. This is possible because the reactance due to C_{gs} is reasonably small at 5GHz. The input impedance

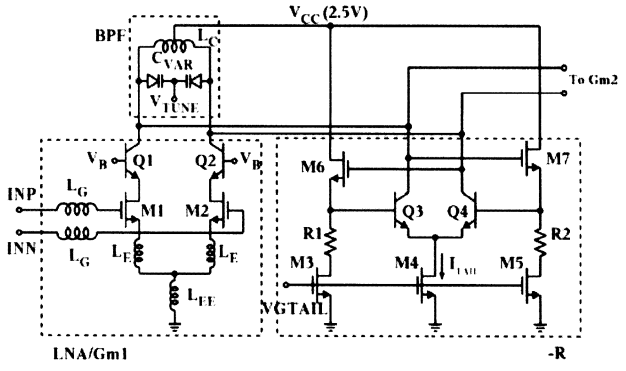

Figure 4: Circuit diagram of the tunable loop filter with Q enhancement.

matching inductor L_G is 4.6nH for an input MOSFET size of 3x32x1μmx0.13μm. The first stage is biased at the minimum noise drain current density of 0.15mA/μm. To maximize the linearity of the loop filter, the second stage is biased at the peak-g_m current density of 0.4mA/μm.

The ADC loop filter tank consists of a differential 2.3nH inductor combined with a 0.8pF accumulation mode MOS varactor. To compensate for the resistive losses of the LC tank, a Q-enhancement circuit is connected in parallel to the resonator as shown in Fig. 4. Its negative resistance is generated by a cross-coupled differential pair consisting of HBTs Q3 and Q4. The negative resistance $R = -2/g_{m3,4} = -4V_T/I_{TAIL}$ is adjusted through an external control voltage V_{CTRL}. The amount of negative resistance is determined by the stability of the closed loop system, as will be explained in Section IV. Source followers M6 and M7 are used to lower the base voltage of Q3 and Q4, and prevent them from going into saturation for large voltage swings from the filter tank.

IV. Measurement Results

The impact of the Q-enhancement circuit on the resonator Q, and the tuning range of the modulator were first verified through small-signal measurements. Figure 5 reproduces the

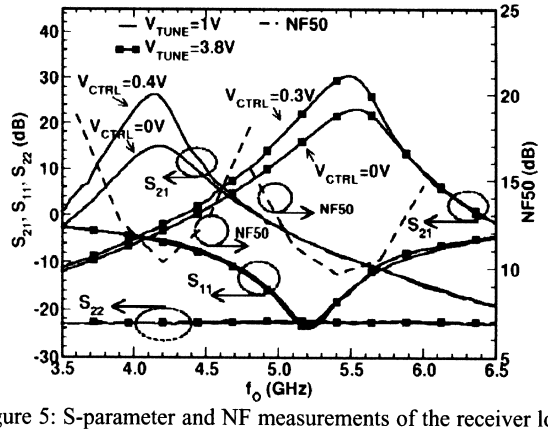

Figure 5: S-parameter and NF measurements of the receiver loop filter.

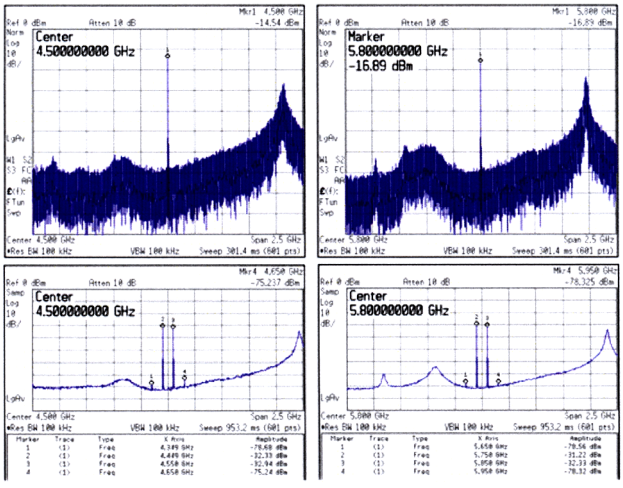

Figure 6: Output spectrum at 4.5GHz and 5.8GHz for single-tone and two-tone tests with -20dBm and -38dBm input power, respectively.

S-parameter and NF measurements for the main path of the entire ADC when the feedback is switched off, and the latches in the quantizer are placed in transparent mode. This mode of operation allows characterization of the loop filter, which is buffered from the 50Ω load by a broadband amplifier formed by the quantizer and the output driver of Fig. 1. The bandpass filter response is plotted in Fig. 5 for two values of the varactor tuning voltage V_{TUNE}. The maximum gain is 23.25dB at 5.5GHz, while NF50 has its minimum of 9.7dB at 5.3GHz. Broadband input matching is achieved with S_{11} being less than -10dB from 4.65GHz to 5.85GHz. The 3-dB bandwidth is 320MHz when the filter is centered at 4.2GHz, corresponding to a Q value of 13. When the filter is tuned to 5.5GHz, the 3dB bandwidth and Q become 400MHz and 14, respectively. Figure 5 also illustrates the bandwidth adjustment with the Q-enhancement circuit. Bandwidths as low as 120MHz and 160MHz can be achieved at 4.2GHz and 5.5GHz, respectively, corresponding to an enhanced Q of 33.

Large-signal measurements of the circuit were performed to estimate the SNR and linearity of the receiver, and to confirm the tunability of the NTF. Quantization noise is the dominant noise source in the passband of the circuit due to the finite resonator Q. Quantization and thermal noise was integrated with an Agilent E4448A spectrum analyzer for conversion bandwidths between 10MHz and 500MHz. Figure 6 shows the spectra at the output of the receiver when tuned at 4.5GHz and 5.8GHz. The single-tone and two-tone spectra correspond to input power levels of -20dBm, and -38dBm, respectively. Losses in the measurement setup are not de-embedded, and the measurement is single-ended. The noise floor of the receiver can be reduced by almost 3dB at 4.5GHz and by 0.5dB at 5.8GHz for V_{CTRL} values between 0.25 and 0.4V. Although the Q of the filter itself can be set to values between 13 and 50, the closed-loop system becomes unstable when Q

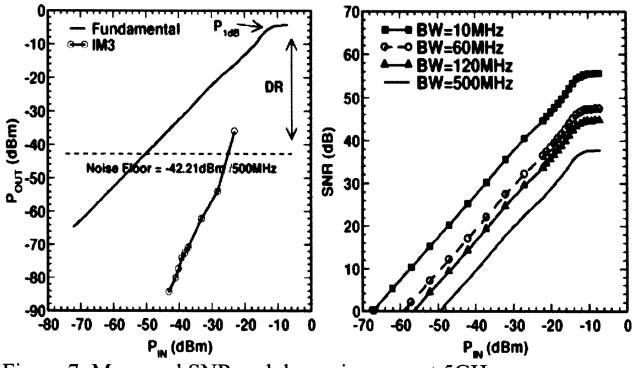

Figure 7: Measured SNR and dynamic range at 5GHz.

exceeds 35. This is attributed to the high gain in the forward path (G_{m1} and G_{m2}), which makes the ΔΣ loop unstable. Figure 7 shows the SNR and the output referred dynamic range vs input power when the receiver is tuned to 5GHz. The IM3 product power equals the integrated noise floor when the input is at -26dBm, corresponding to an SNDR of 22.1dB. The receiver achieves an SNR of 37.9dB over 500MHz and an IIP3 of -5.5dBm with a total power dissipation of 2.09W from a 2.5V supply. The output referred dynamic range is 37.2dB. An SNR comparison of the 2GHz design with the tunable 4.5GHz to 5.8GHz one shows how performance degrades as the center frequency increases (Figs. 8 and 9).

Table I compares this work to various continuous-time bandpass ΔΣ ADCs with GHz clocks. The 4.5GHz to 5.8GHz receiver has higher conversion bandwidth, while operating at the highest center frequency reported to date. The circuit was fabricated in STM's production 0.13μm SiGe BiCMOS process, and occupies 1.59x2.39mm^2 (Fig. 10).

V. Conclusion

A 4.5GHz to 5.8GHz digital receiver consisting of a ΔΣ ADC and 40GHz PLL with on-chip VCO was demonstrated. The circuit achieves an SNR of 37.9 dB and an SNDR of 22.1 dB over 500MHz. This work proves that, by keeping the same

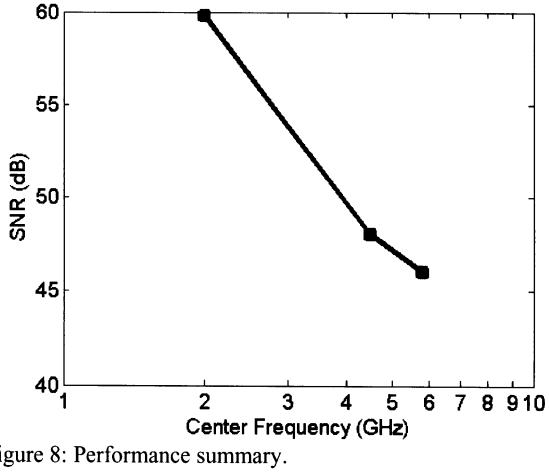

Figure 8: Performance summary.

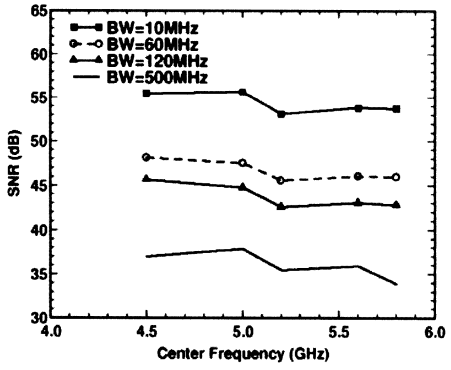

Figure 9: Measured SNR vs center frequency of the direct sampling receiver.

digital circuitry (quantizer, DACs and clock distribution) and changing the center frequency of the loop filter, a direct sampling ΔΣ ADC can be tuned to a higher band. Analysis and experiment show that the ADC performance depends on the filter quality factor and on the ADC center frequency.

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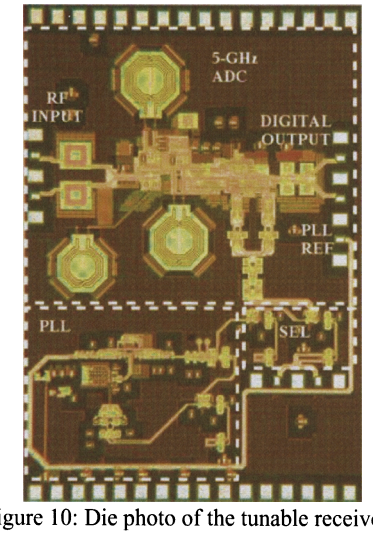

Figure 10: Die photo of the tunable receiver.

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Reference/Technology	Fo/Fs (GHz)	BW (MHz)	P (W)	SNR (dB)	SNDR (dB)	SFDR (dB)
[Cosand, JSSC2004] 130GHz InP	0.14-0.21/4	60	3.2	47.7	-88dBFS*	N/A
[Gao, VLSI1998] 50GHz SiGe HBT	1/4	4	0.35	53	N/A	69
[Jayaraman, GaAsIC1997] 40GHz GaAs	0.8/3.2	25	1.8	41	N/A	50
[Kaplan, CICC2003] 160GHz InP	1.3/4.3	200	6.2	39	N/A	N/A
[Thandri, JSSC2007] 47GHz SiGe BiCMOS	0.95/3.8	1	0.075	59	-59dBFS*	N/A
[Chalvatzis, VLSI2007] 150GHz SiGe BiCMOS	2/40	60	2.19	59.8	35.2	59
This work 150GHz SiGe BiCMOS	4.5-5.8/40	500	2.09	37.9	22.1	48

*IM3@-6dBFS input

Table I: Comparison of continuous-time bandpass ΔΣ ADCs.