4-bit, 16 GS/s ADC with new Parallel Reference Network

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***Abstract* — This paper presents a high-speed 4 bit full-flash Analog-to-Digital Converter with a new parallel reference network for an UWB radar. The ADC is implemented in 190 GHz SiGe BiCMOS technology, has more than 6 GHz effective resolution input bandwidth and operates up to 16 GSample/s. Power dissipation is 1.15 W including test buffers and 750 mW of the converter itself.**

I. INTRODUCTION

Ultra wideband (UWB) radar is of great interest for a number of applications such as surface penetrating radar, surveillance and emergency radar, medical instrumentation, non-destructive testing in civil engineering and the food industry, industrial sensors and many others.

UWB radars have excellent spatial resolution and it is supposed that they can be advantageously applied in the field of localization. There are a number of applications that would take advantage from precise indoor positioning such as automatic storage, tracking of various targets or people in dangerous environments and so on. A special variant of UWB radar using M-sequences provides both simple architecture and wide frequency range [1], [2]. This work has been focused on developing an ADC particularly suited for such a systems, but also useful for other applications where low input capacitance and high input bandwidth are important.

II. ARCHITECTURE

A simplified architecture of M-sequence UWB radar is shown in Figure 1. The UWB-system operates in a frequency range from DC to 10 GHz. The ADC, which is located closely to the antenna, has to operate at full system frequency range. Full-flash architecture is well suited for gigahertz range and therefore it has been chosen for the implementation.

A block-diagram of a typical flash ADC is shown in Figure 2. The big capacitive load on the reference network caused by a bank of comparators is one of the known problems of such architecture. The proposed reference network, described below, distributes the load over several nodes and allows to achieve higher input bandwidth. The rest part of the ADC is well-known from the literature [3].

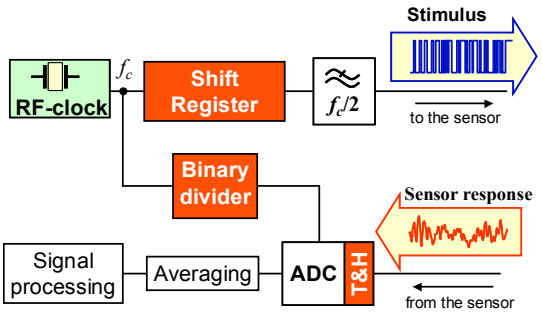

Figure 1. M-Sequence UWB Radar Architecture.

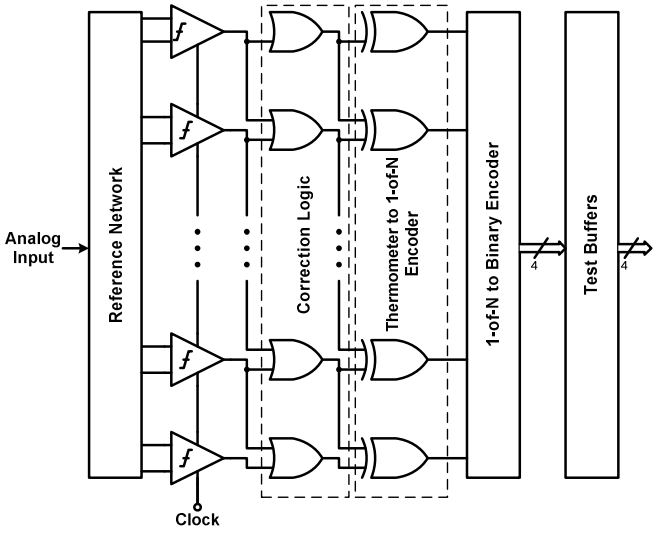

Figure 2. Block-diagram of the flash ADC.

III. CIRCUIT DESIGN

A. New Parallel Reference Network

One of the bottlenecks of flash ADCs is the reference network. A positive part of a conventional differential reference network is depicted in Figure 3a. The bandwidth of the network depends on: tail current I_{EF}, total resistance of the resistor ladder and load capacitances C_{load} which consist of input capacitance of the next stage (comparator) and parasitic capacitances. The bandwidth of the complete reference network of the ADC is proportional to $1/(n \times C_{load})$ and $1/(n \times R)$, where n is the number of comparators, R is the tap resistance.

A common way to increase BW is to decrease the value of resistor R. This leads to increase of the tail current I_{EF}, assuming that the input range is kept constant. Furthermore increasing of I_{EF} leads to increase of geometrical size of resistor R that leads to increased parasitic capacitances. Beyond a certain resistor size the parasitic capacitances would be dominant and limit the bandwidth for a given technology.

To overcome described drawbacks, a new parallel reference network is proposed [4]. The main idea is to convert the serial resistor ladder to a parallel one. In [4] several possible configurations are described, but most practical one from author's point of view is shown in Figure 3b. The value R of the resistor and the current I_{EF} in general case can be arbitrary. For simplicity in Figure 3b all tail currents are equal. The main condition is that the voltage drop at adjacent branches should be different by 1 LSB. Obviously that the last branch has the lowest bandwidth and the first one the highest. By tuning the tail currents near the same bandwidth for all branches has been achieved.

The proposed reference network has several advantages: 1) higher bandwidth; 2) bandwidth is independent from the number of subsequent load stages; 3) possibility to equalize the bandwidth of the each branch; 4) possibility to calibrate the tail currents and compensate device mismatches (not implemented in this work).

Worse linearity because of nonregular distribution of resistors is only one disadvantage known to the authors.

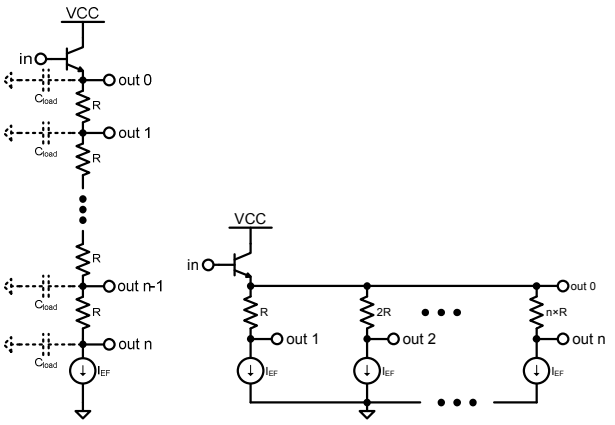

Figure 3. a) Conventional differential reference network (positive part), b) Proposed differential reference network (positive part)

B. Comparator

The comparator usually consists of preamplifiers, master and slave latches. There are several factors that limit the performance of the comparator: 1) ability of the preamplifier to amplify the input signal while it changes from the maximal value to one LSB, i.e. overdrive conditions; 2) kickback noise, due to injection of charge into the base. It can significantly distort the input signal and further leads to the erroneous comparison; 3) recovery time of the comparator t_{rec} is the time to change the logic output of the comparator to the midpoint of the logic stage. The worst case is when the input signal is 1/2 LSB; 4) charge time t_{charge} is the time required to charge the base-emitter capacitance of the latch; 5) regeneration time t_{reg} is the time that the comparator needs to achieve the full output voltage.

A simple differential pair is usually used as amplification stage in the preamplifier. But the differential pair can not properly amplify the input signal under overdrive conditions. At high frequencies, the sensitivity of the preamplifier drastically decreases. Consequently the sensitivity of the whole comparator also decreases. A good solution of this problem is the limiting amplifier based on the Cherry-Hooper architecture. Advantages of this amplifier are better sensitivity and good isolation of the latch from the reference network. It allows to omit emitter followers after amplification stage and decrease the power.

The performance of the latch is limited by the recovery time and the regeneration time. They can be estimated by formulas (1) and (2) [5].

$$t_{rec} = R_L C_{total} \ln\left(1 + \frac{1}{\tanh\left(\frac{qV_{in}}{2kT}\right)}\right) \quad (1)$$

$$t_{reg} = \tau_{reg} \ln\left(\frac{4V_T}{LSB}\right), where\ \tau_{reg} = \frac{C_{total}}{g_m}\left(\frac{g_m R_L}{g_m R_L - 1}\right) \quad (2)$$

From (1) and (2) it is obvious that performance of the latch mainly depends on the load resistance R_L and the total parasitic capacitance C_{total}. Minimum-size transistors minimize parasitic capacitance and also minimize power dissipation of the comparator. The full schematic of the comparator is shown in Figure 4.

To further improve the performance of the latch an additional current source I1 is added. This current source provides several benefits: 1) it decreases the time to charge the base-emitter capacitance; 2) cross-coupled differential pair, being a negative resistance, increases the gain of the track stage and decreases the recovery time. The penalty for those benefits is hysteresis, which decreases the sensitivity of the comparator. Therefore the current I_1 has to be sufficiently small. In this work the current value has been chosen about 10% of the tail current.

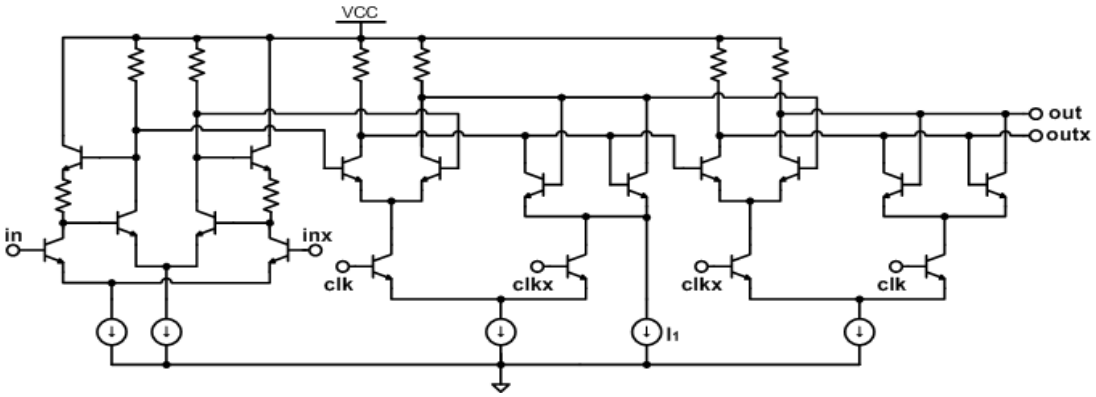

Figure 4. Schematic of the comparator.

C. *Encoder*

The thermometer code produced by the comparators is fed to the encoding circuitry (encoder). The encoder can be logically divided in two parts: correction logic and thermometer-to-binary encoder. The correction logic detects and corrects errors in the thermometer code. The states of two adjacent comparators are analyzed therefore only one erroneous output of the comparator ("bubble") can be corrected. Two adjacent 'bubbles' will cause an error in the output binary code.

IV. Experimental Results

The ADC is fabricated in a commercially available low-cost 0.25 µm 190 GHz SiGe BiCMOS technology [6]. The technology provides five metal layers with two thick top metals, a full suite of RF passive elements including metal-insulator-metal (MIM) capacitors and spiral inductors.

The chip micrograph is shown in Figure 5. The ADC occupies 1.5×1.5 mm^2 including bondpads.

To characterize the static performance of the ADC, a slow 50 MHz sine input signal was digitized with 5 GSample/s sample rate. The output binary code was registered with a 4 channels 20 GS/s real-time oscilloscope and reconstructed using MATLAB. Despite the ADC is fully differential, only single-ended outputs were used for characterization due to measurement set-up limitations. INL and DNL were measured by histogram test. Results are shown in Figure 6.

To characterize the dynamic performance, the ADC was tested over the whole input frequency range with a constant sample rate of 16.01 GS/s. The input signal was applied with the amplitude of 1 $V_{p\text{-}p}$, which corresponds to the full scale input range of the converter. The output of the ADC was reconstructed as described above and transformed into frequency domain. Signal-to-Noise-and-Distortion-Ratio (SINAD) was measured at each of the input frequencies. Figure 7 shows the performance of the ADC over a frequency range up to 6 GHz at constant 16.01 GS/s sample rate. The decay of SINAD value does not exceed 3 dB at 6 GHz input, that corresponds to a minimum effective resolution bandwidth (ERBW) of 6 GHz. Measurements at higher input frequency were not possible with our current measurement set-up.

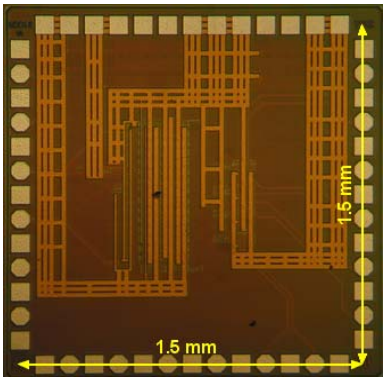

Figure 5. Chip micrograph.

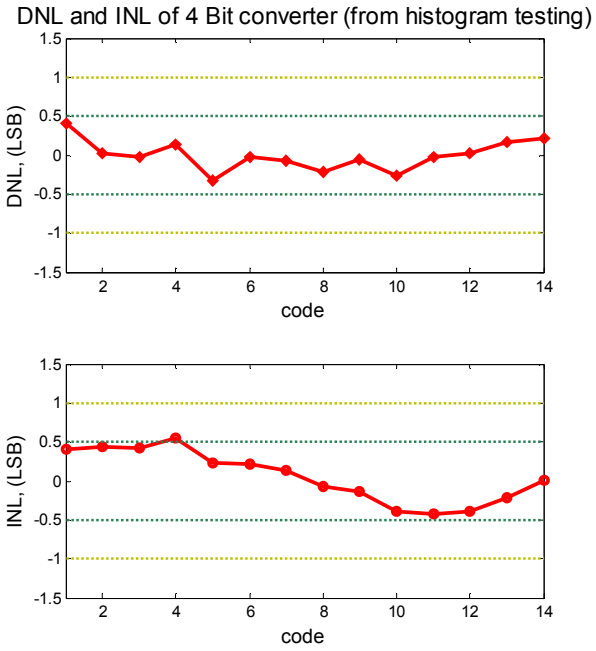

Figure 6. DLN and INL mesusrement results from hystogram test.

TABLE I. COMPARISON OF HIGH-SPEED ADCS

Sample Rate, GS/s	Resolution, bits	ENOB, bits	ERBW, GHz	Power Dissipation, W	FOM, pJ	Technology	Type	Ref.
10	5	> 4.1		3.6	47	0.18 µm SiGe, BiCMOS	flash	[7]
40	3	2.8	20	3.8	13.6	0.12 µm SiGe	flash	[8]
20	8	4.6	6.6	9	28	0.18 µm, CMOS		[9]
22	5	3.5	7	3	19	0.13 µm SiGe, BiCMOS	flash	[10]
24	6	3.5	12	1.2	4.4	90 nm, CMOS		[11]
20	3		4.2	2.36	8.5	0.12 µm SiGe	flash	[12]
16	4	3	6	0.75*	7.8	0.25 µm SiGe, BiCMOS	flash	This work

* without test buffers

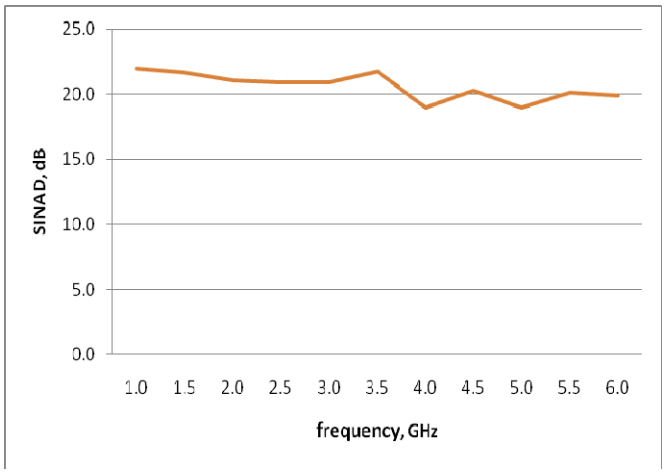

Figure 7. Dynamic performance of the ADC over frequency range up to 6 GHz at 16.01 GS/s sample rate.

A comparison of this work with similar high-speed ADC designs implemented in different technologies is shown in TABLE I. The presented ADC has the lowest power dissipation among competitors and the second lowest energy pro conversion step.

The main parameters of the ADC are summarized in the TABLE II.

CONCLUSION

A high speed analog-to-digital converter for UWB applications with a new parallel reference network has been designed and fabricated in a low-cost 190 GHz SiGe BiCMOS technology. The new reference network overcomes some limitation of a conventional one and allows to achieve higher effective resolution bandwidth of the ADC. Despite worse linearity of the reference network, the INL of the ADC is less or equal to 0.5 LSB and do not need additional calibration. Therefore proposed network is very well suited for low resolution high-speed A/D converters.

ACKNOWLEDGMENT

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TABLE II. SUMMARY OF MAIN PARAMETERS OF THE ADC.

Resolution	4 bits
Input range	1 V_{p-p}
Sampling rate	16 GS/s
INL	≤ 1/2 LSB
DNL	< 1/2 LSB
ERBW	6 GHz
Supply voltage	3 V
Power dissipation:	
Clock buffers	150 mW
Core part	600 mW
Test buffers	400 mW
Chip size	1.5×1.5 mm^2

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