A 6.1 GS/s 52.8 mW 43 dB DR 80 MHz Bandwidth 2.4 GHz RF Bandpass ΔΣ ADC in 40 nm CMOS

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***Abstract* — A 2.4 GHz 4th order BP ΔΣ ADC is presented. The feedforward topology uses Gm-LC resonators that can be calibrated in frequency. The quantizer is split in 6 interleaved comparators to relax speed. Clocked at 6.1 GHz, it achieves a DR of 43 dB in 80 MHz consuming 52.8 mW. Implemented in 40 nm CMOS, it achieves a FoM of 3.6 pJ/conv. step, which is to date the lowest published value for RF BP ADCs.**

***Index Terms* — ΔΣ ADC, RF bandpass filters, high-speed comparators**

I. Introduction

The recent growth of circuit techniques that leverage the high speed capabilities of deep submicron CMOS devices is gradually renovating the architectures of RF communication systems. In this evolution, RF bandpass (BP) ΔΣ ADCs have the potential to provide a substantial paradigm shift in RF communication systems towards directly quantized RF signals. These converters could pave the way towards entirely software radios where all signal conditioning would be done in the digital domain. However, the replacement of the entire receiver chain by an ADC poses enormous requirements on the converter mainly in terms of dynamic range, leaving its reality for a long term future. Nevertheless, this work attempts to set a step forward for these systems by demonstrating the capability of integrating such a BP ADC in a digital 40 nm CMOS process at power levels compatible with mobile applications.

The ADC is designed to operate in the 80 MHz wide 2.4 GHz ISM band. The architecture uses a ΔΣ loop where a BP loop filter is used to filter out the oversampled quantization noise created by the internal quantizer.

The paper is structured as follows. Section II describes the architecture of the converter; Section III and IV provide implementation details of the loop filter circuits and the quantizer; Section V introduces the calibration method proposed to adjust the filter center frequency and quantizer thresholds respectively; finally, Section VI provides measurement results of the implementation and Section VII concludes the paper.

II. ADC Architecture

Fig. 1 shows a block diagram of the modulator. The 4th order BP loop filter is a feedforward structure with two Gm-LC resonators. The system clock chosen is 6.1 GHz such that the bandwidth of the filter is centered at 0.4xFs = 2.44 GHz. The bandwidth of the modulator is 80MHz leading to an oversampling ratio around 38. The quantizer is split into 6 interleaved quantizers to relax speed requirements mainly limited by comparator metastability.

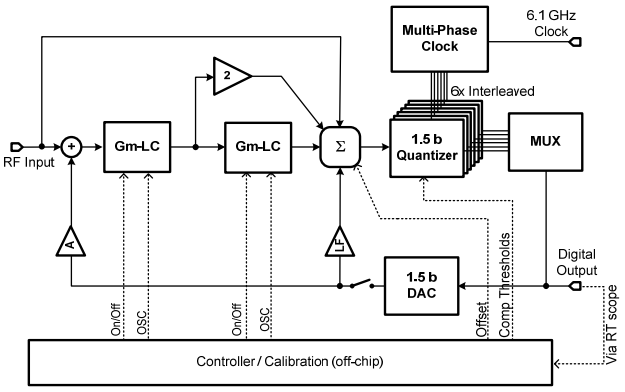

Figure 1: RF Bandpass ΔΣ modulator architecture

The six output streams are then multiplexed to feed a single DAC in order to avoid component mismatches in the feedback path. The signal is quantized into 3 levels (1.5 bit) to extend the dynamic range of the modulator. The center frequencies of the resonators as well as the threshold levels of the comparators are adjusted via a calibration procedure that monitors in open-loop the statistics of the quantized signal. A local feedback path is added to the architecture to accommodate for loop delay in the feedback path.

III. Loop Filter Circuits

A resonator circuit is shown in Fig. 2 (left). The input transconductance is a cascoded pseudo-differential pair for

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improved isolation and linearity. Each resonator tank is made of a center-tap differential 4-turn inductor of 4 nH in parallel with a capacitor. The capacitor is a fixed MoM capacitor in parallel with binary weighted switched NMOS capacitors allowing for center frequency adjustment. To improve the in-band noise shaping by the filter, the quality factor of the tank is enhanced with cross-coupled pairs that compensate for tank losses. This negative resistance is implemented as an array of switchable binary weighted devices. The four-input adder, shown in Fig. 2 (right), is made of 4 cascoded differential pairs loaded by a common resistor. The resistor size of 110 Ω results from a compromise between loop gain and minimum phase shift around 2.4 GHz when loaded by the quantizer. The gain of 2 in the internal feedforward path is emulated by duplicating the corresponding adder stage. All bias voltages and currents are provided by an on-chip bandgap reference circuit, guaranteeing a fixed voltage drop across R_L over PVT variations.

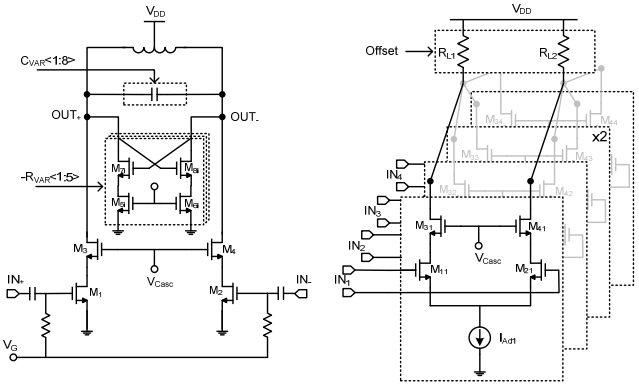

Figure 2: Resonator circuit (left) and adder circuit (right)

IV. Quantizer Implementation

The 1.5 bit quantizer is made of two banks of 6 interleaved comparators as used in [1], with opposite threshold levels as shown in Fig. 3. The interleaved clock of the comparators is produced by a synchronous divider made of 12 high speed TSPC flip-flops [2] in a closed loop. The flip-flops are reset to the value '111000111000', which, runs through the flip-flop chain at the rhythm of the 6.1 GHz clock. Each flip-flop output is used as interleaved clock for one single comparator. Although a chain of 6 flip-flops could be sufficient, the use of 12 flip-flops reduces the load on each flip-flop and facilitates the layout. Once a comparator decision is taken, its value is held constant during the reset phase of the comparator by an SR latch. To realize the multiplexing operation, the comparator decision value is NANDed with a pulse of one clock period, obtained by NANDing two appropriate interleaved clocks. Depending on the decision value, a pull-up pulse or a pull-down pulse is created activating either the PMOS or the NMOS transistor of the tri-state buffer. The short pulse ensures that after the operation, all transistors return to cut-off leaving the line at high impedance. The multiplexed output data are latched before activating the DAC to guarantee a stable loop delay and to reduce jitter in the feedback path. The DAC uses a switched NMOS current source topology with positive/negative/dump-to-supply output for proper 1.5 bit operation.

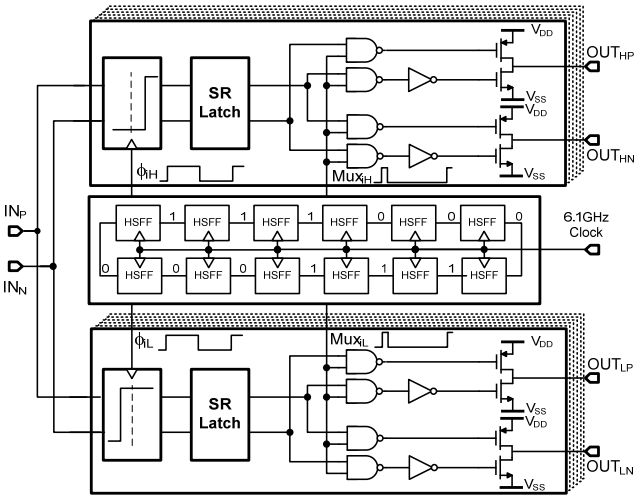

Figure 3: Interleaved quantizer and multiplexing stage

V. ADC Calibration

Before closing the loop, the loop filter and the quantizer thresholds need to be calibrated. The resonators are calibrated by turning them into their oscillating mode using sufficient negative resistance. As shown in Fig 4, the oscillation frequency can be detected digitally with a counter at the output of the quantizer. A frequency locked loop can then adjust the center frequency via a controller, which is positioned off-chip. The two resonance frequencies can be detuned to extend the bandwidth of the modulator. The center frequency is controlled with an accuracy of a few MHz to guarantee the final ΔΣ performance. Once calibrated, the resonator Q is reduced until no more oscillation is observed at the output. The measured calibrated loop filter transfer function is plotted at the bottom of Fig. 3. To calibrate the comparator thresholds, the required offset voltage is applied at their input by simply setting an imbalance in the load resistors of the preceding adder. Each comparator is then calibrated

individually using a capacitor array as in [3], of which the setting is selected that flips the output.

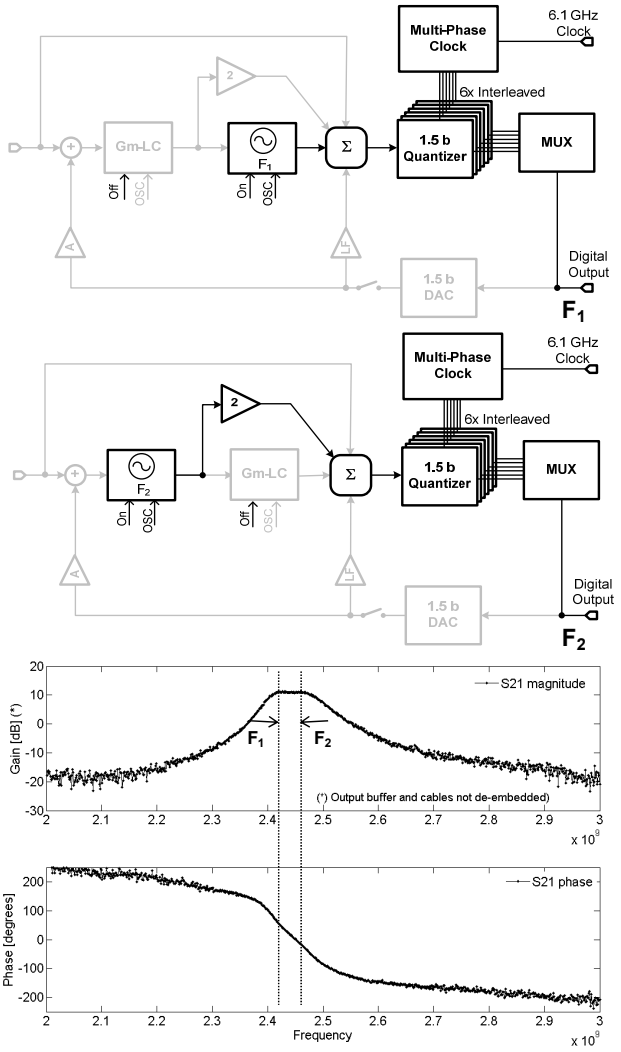

Figure 4: Center frequency calibration and resulting measured loop transfer function

VI. Measurements

The ADC was fabricated in a 40 nm CMOS technology and a chip micrograph is shown in Fig. 5. The active area is 0.4 mm^2 and is substantially reduced with respect to [4] thanks to the use of 2 inductors instead of 4.

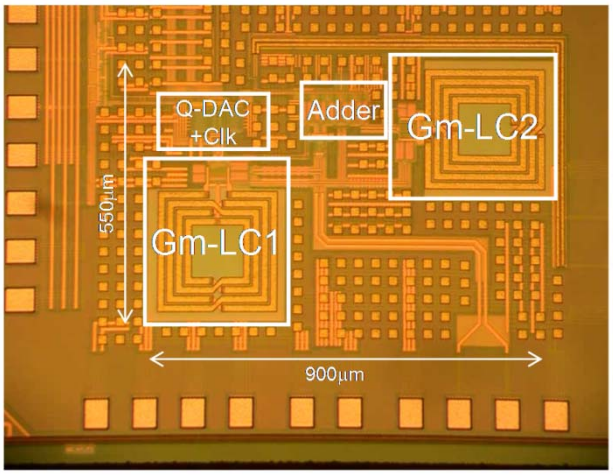

Figure 5: Chip micrograph. Quantizer, DAC and clock generation/distribution are highlighted together

The digital output data were measured on a 12GHz real-time oscilloscope. An FFT of the digital bit stream for a 2.42 GHz input tone at -15 dBm input power (-8 dBFS) is given in Fig. 6.

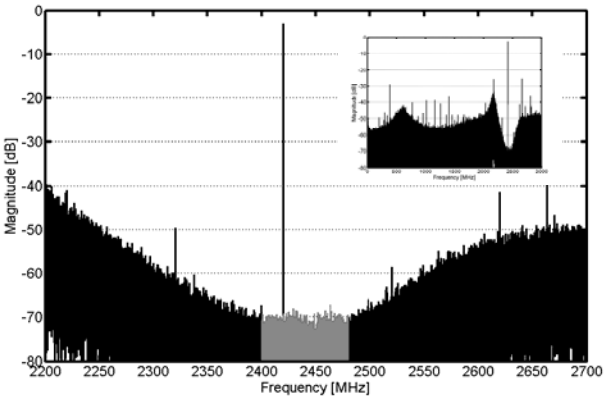

Figure 6: Output spectrum obtained from an FFT on the digital bit stream around the center frequency for an input signal at 2.42GHz

The SNDR and SFDR (single-tone) vs. input signal power are plotted in Fig. 7. Measured on a bandwidth of 80 MHz, a maximum SNDR of 41 dB and SFDR of 65 dB were obtained and a dynamic range higher than 43 dB was measured. The IIP3 of the ADC was measured to be -5 dBm. The current consumption breakdown is 30 mA for the RF filter, 12 mA for the quantizer and clock network, and 6 mA for the DAC including bandgap reference circuit, clock drivers and low-jitter re-timing latches.

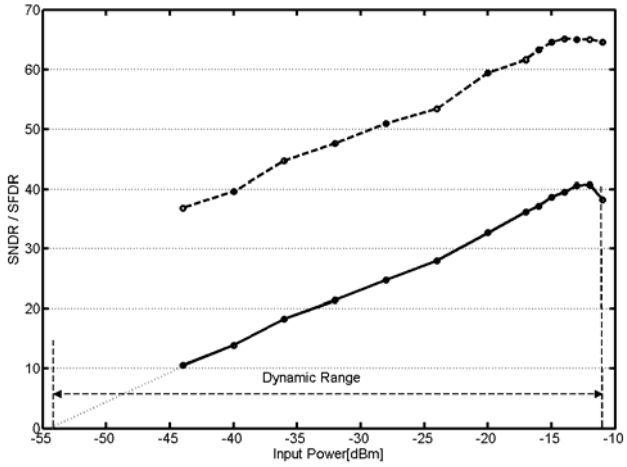

Figure 7: Measured SNDR and SFDR plotted against absolute input power

With a total power consumption of 52.8 mW from a 1.1 V supply, the FoM, is 3.6 pJ/conversion step which is to date the lowest value published for designs in SiGe [5-7] as well as CMOS [4], [8], while implemented in an advanced 40 nm CMOS technology. Also, when compared to [4], the proposed ADC uses 2 inductors instead of 4, which not only reduces the area by more than a factor 2, but also reduces the complexity of the system, simplifying the calibration of the resonators and reducing the effect of coupling between inductors. A comparison of this design with state of art implementations is given in Table 1.

Table 1: Performance summary and comparison to state of art

	[4]	[5]	[6]	[7]	[8]	This work
Center frequency	2.4 GHz	2 GHz	950 MHz	1 GHz	2.442 GHz	2.44 GHz
Clock frequency	3 GHz	40 GHz	3.8 GHz	4 GHz	3.256 GHz	6.1 GHz
SNDR	40 dB	52 dB	59 dB	40 dB	34 dB	41 dB
Bandwidth	60 MHz	120 MHz	1 MHz	20 MHz	25 MHz	80 MHz
Power Consumption	40 mW	1600 mW	75 mW	450 mW	26 mW	52.8 mW
Technology	90 nm CMOS	0.13 µm SiGe	0.25 µm SiGe	0.5 µm SiGe	130 nm CMOS	40 nm CMOS
Active Area	0.8 mm^2	~1 mm^2	1.08 mm^2	1.36 mm^2	0.27 mm^2	0.4 mm^2
FOM [pJ/conv. step.]	4.1	20.4	51.5	142.9	12.7	3.6

VII. Conclusion

This paper described the implementation of an RF bandpass ΔΣ ADC in a standard 40 nm CMOS process. Its low power and low complexity demonstrates the feasibility of bringing an ADC next to the antenna of a wireless receiver. A calibration procedure is also proposed to compensate for the inherent process variations in the loop filter and in the quantizer thresholds. Although the performances obtained are not yet sufficient to substitute a complete receiver chain, this design sets a new path towards entirely software receivers.

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