A 35 GS/s 5-Bit SiGe BiCMOS Flash ADC with Offset Corrected Exclusive-Or Comparator

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***Abstract*-The design and wafer probe test results of a 5-bit SiGe ADC are presented. The integrated circuit, fabricated in a 200/250 GHz f_T/F_{max}, SiGe BiCMOS technology, provides a 5-bit analog to digital conversion with input tone frequencies up to 20 GHz and sampling clock rates up to 35 GS/s. The ADC makes use of a comparator with an integrated exclusive-or function to reduce power consumption. The device also generates two half-rate interleaved outputs to ease in data capturing with laboratory equipment. An effective number of bits (ENOB) of nearly 5.0 is achieved for low frequency input tones, dropping to 4.0 at 10 GHz.**

I. INTRODUCTION

In high speed optical communications receivers, high speed ADCs are required to provide sample information for use with DSP-based signal equalization [1,2]. Equalization is needed to compensate for signal dispersion in the optical fiber. High speed ADCs are also needed for spectral identification of high speed signals and can provide the interface to an on-chip integrated FFT engine [3]. In order to improve the performance of such systems, high sampling rate and high input bandwidth ADCs are being pursued. This paper describes an ADC with higher speed sampling capability (greater than 30 GS/s) and higher input bandwidth (20 GHz) compared to previous designs [1,2,4,5] while minimizing power consumption through the use of a new comparator architecture integrated with Gray code back-end logic.

II. ARCHITECTURE

The goal of the design was to develop a 5-bit ADC with a sampling rate of at least 20 GS/s (preferably higher) and input bandwidth of at least 20 GHz, while simultaneously minimizing power consumption. No track and hold circuit was used in order to simplify the input driver design, contrary to other approaches described elsewhere [1,7]. The elimination of the track and hold requires optimization of several critical performance parameters in other circuit areas. The comparators require a 20 GHz bandwidth and a symmetric input signal distribution network with equal delay to all comparators. In addition, all of the comparators must be sampled simultaneously requiring precision clock distribution and input distribution networks. The ladder reference voltage range of the ADC is limited to roughly 1V due to breakdown voltage limitations for the 130 nm generation SiGe npn bipolar transistors. For a 5-bit design, the size of the least significant bit (LSB) is approximately 30mV for a ladder reference range of 1V. With 130 nm emitter dimensions, the npn transistor Vbe matching can be quite poor. Mismatches of 15 to 20mV are common in this generation of technology, which translates to comparator offsets on the order of 0.6 LSBs. For this reason, offset correction capability was added to allow for the correction of Vbe mismatches. The analog input into the ADC is single-ended. Care was taken in the design and layout to minimize coupling of the input signal into sensitive circuitry and ensure that there would be minimal coupling from other circuit areas into the input signal path. Differential circuits were used for the signal paths from the comparator outputs, through the back-end logic and the output drivers. At the output, two 5-bit words are provided. Both words are in time synchronization with each other and each is updated at half the sampling rate. The output words are provided in Gray Code format to allow for easier testing and diagnosis of any logic or timing errors in the back-end logic.

A block diagram of the chip is shown in Figure 1. The reference ladder contains 31 buffers with programmable output voltages which are used to compensate for comparator input offset voltages. The buffer output voltages are controlled by an integrated 6-bit DAC with an adjustment range of +/- 63 LSBs, where the LSB value is approximately 1mV. The adjustments for each reference are stored in an on-chip shift register. A permanent adjustment can be programmed on-chip through the use of electrical fuses.

The analog input signal is buffered and sent to all comparators with equal time delay. The input is then compared to these references through the use of 15 comparators with a built-in exclusive-or (XOR) function (described in the next section) and one buffering comparator. The outputs of the comparators are sent to the back-end logic to decode the sample value.

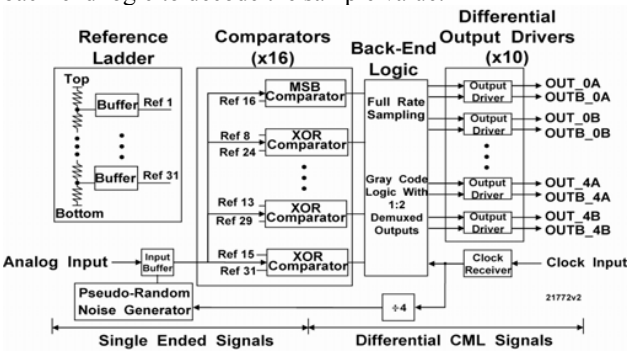

Fig. 1. Block Diagram of 5-Bit Flash SiGe ADC.

III. CIRCUIT CONCEPTS

In order to reduce total power consumption, XOR functions (required for Gray-Code output coding) were incorporated into the comparators. A comparison of a comparator with a built-in XOR function to a traditional comparator is shown in Figure 2. In a traditional design, the XOR operation occurs after the individual comparisons are latched. This is shown in the upper schematic after the gain stages. In the lower schematic, the exclusive OR function occurs prior to the gain stage through a combination of differential pairs and current sources. The operation is as follows: if the input is below or above both references, the output is a zero. If the input is between the two references, the output is a one. A critical part of this front-end circuitry is to maintain constant gain during both transitions as well as retaining a constant output common mode level into the gain stage. By integrating the exclusive OR function into the front-end of the comparator; the number of comparators as well as the circuitry following the comparators can be reduced by a factor of two. This generates a large power saving of at least 1W in the back-end logic and 0.5W in the comparators. In addition, clock loading is reduced which allows an additional power savings in the clock drivers.

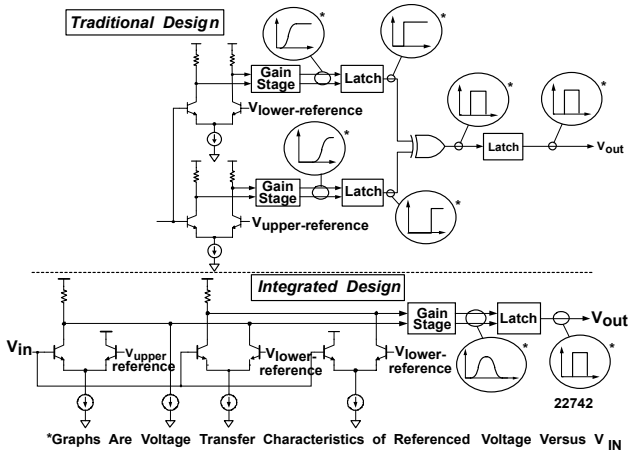

Fig. 2. Comparison of Dual Reference Comparator with Traditional Comparator

A detailed representation of a portion of the back-end Gray Code logic can be seen in Figure 3. The back-end logic includes the D-Flip-Flops which perform the sampling operation at full clock rate. The remaining latches and XOR circuits are clocked in an interleaved fashion at half rate with final outputs time-aligned with the half-rate clock.

The on-chip sampling clock receiver generates full-rate differential buffered clocks which perform the sampling operation. Local divide-by-2 circuits generate half-rate clocks to clock the remainder of the back-end logic.

The analog input path of the ADC consists of a single-ended 50-ohm transmission line that routes the input signal to the input driver where it is terminated with a 50 ohm resistor.

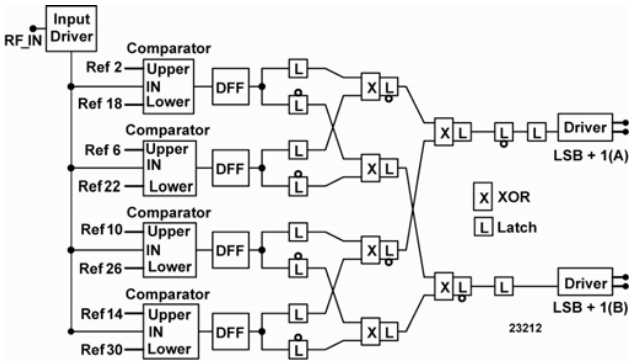

Fig. 3. Detailed Block Diagram of the LSB+1 Signal Path within the Interleaved Gray-Coded Back-End Logic

This input driver then drives the inputs of all of the comparators (Figure 4). The input driver is needed to maximize the input bandwidth of the signal into the comparators by presenting a 15 ohm drive impedance to the comparators instead of a 50 ohm impedance from off-chip. Another feature added to the input driver circuit of the ADC for decreasing the amplitude of in-band spurs is a selectable 2^{20}-1 pseudo-random noise generator. It can be used to inject band-limited pseudo-random jitter to dither the input signal [6].

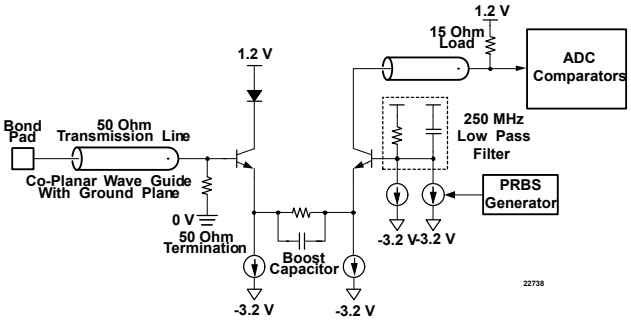

Fig. 4. Diagram of Input Driver Which Interfaces to ADC Comparators

A photograph of the ADC die is shown in Figure 5. The die dimensions are 3.5mm x 3.5mm. The chip includes two rings of bond pads. The outer ring contains all of the high frequency signals entering or leaving the chip and includes a pair of ground pads on each side of every signal, whether differential or single-ended. The inner ring of bond pads are primarily used to provide multiple supply voltage connections to the chip, namely V_{CC} (+1.2 V), GND (0 V) and V_{EE} (-3.2 V). The bond pads are arranged to allow either probing or wire bond connections.

The single-ended input tone enters the chip from the left side and interfaces with the analog input driver through a 50 Ohm-terminated coplanar waveguide with ground (CPWG) transmission line. The single-ended sampling clock input is routed from the right side. These two signals were separated in this manner to minimize coupling. The two interleaves of 5-bit output words come off the chip differentially and are located on the top, right and bottom sides. On the left side of the chip, are various low frequency control lines on the

outer pad ring. The analog input driver feeds a relatively wide trace that connects all 16 comparators. This trace is located over a ground plane whose main purpose is to terminate field lines, thus minimizing coupling of the comparator input signal to the reference power supplies and other sensitive circuits. The reference ladder is located on the left side of the chip. It provides the inputs to the offset correction circuitry located in the upper left and lower left sides of the chip. The comparators are located in the middle of the chip. The back-end logic is located to the right of the comparators. The chip contains approximately 1.67nF of decoupling capacitance between V_{CC} and GND as well as approximately 1.67nF of decoupling capacitance between V_{EE} and GND. The chip layout was executed using 7 layers of metal, with the top layer of metal used for bond pads and power supply distribution.

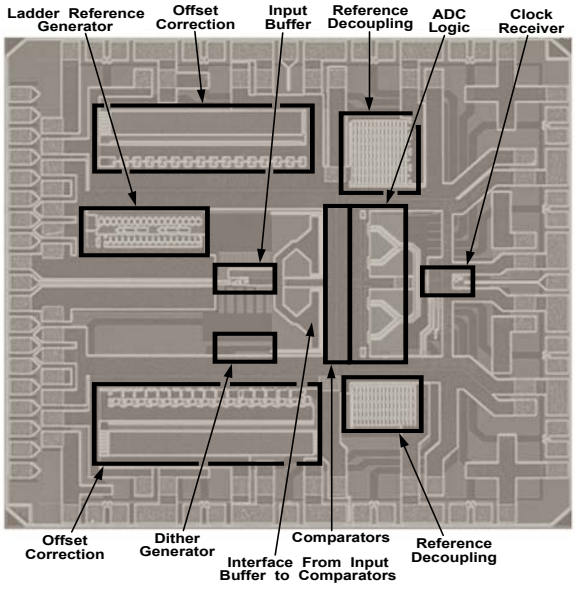

Fig. 5. Photograph of 5-Bit Flash SiGe ADC

IV. TESTING AND MEASURED PERFORMANCE

Probed testing of the 5-bit SiGe ADC was performed using an Alessi automated probe station. Two Agilent 8257D signal generators were used: one for the sampling clock source, and a second for the input tone. These generators were chosen due to their very low phase noise close-in to the carrier frequency. Clock frequencies from 0.1 to 40 GHz were used in testing the ADC. An HP 80000 data generator was used to load the on-chip shift register with sign and magnitude of the offset corrections applied to each of the ADC comparators. An Agilent 81250 ParBERT was used to receive the 5-bit digital words coming from the ADC. Only one of the two interleaved outputs from the ADC was observed at any one time due to the limited number of receive channels available.

Under nominal voltage conditions, V_{CC} and Vee currents were observed to be about about 525mA and 1280 mA respectively. Total typical power dissipation (from approximately 10 devices) under these conditions was 4.85 W. DC transfer curves were measured on six die with most of the code transitions being sharp with good gain (approximately 4 mV of transition width). Three comparator transitions have poorer gain which is believed to be due to an npn bipolar device saturation issue in the first stage of the comparator. After comparator input offset correction, the Integral Non-Linearity (INL) and Differential Non-Linearity (DNL) (Figure 6) were both measured to be less than 0.1 LSB.

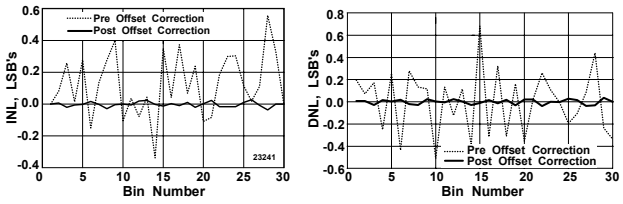

Fig. 6. Measured INL and DNL Before and After Applied Offset Corrections

The driver input bandwidth characteristics, as shown in Figure 7, was measured by performing a sine wave fit to the ADC samples for each of the input tone frequencies, keeping the input amplitude at the input pads fixed. The input gain curve drops by 3dB from DC to 9 GHz but thereafter is roughly flat out to approximately 17 GHz, allowing sampling with reasonable gain degradation out to roughly 20 GHz. This degraded bandwidth performance, relative to the goal of 20 GHz bandwidth, was not expected. A simulation was performed with the actual parasitic capacitances extracted from the chip layout. Once the correct parasitic capacitance was included in the simulation, the simulated input gain exhibited a similar droop near 9 GHz, roughly consistent with the measured results. A reduction in signal line width from the input buffer to the comparators is expected to fix the bandwidth problem.

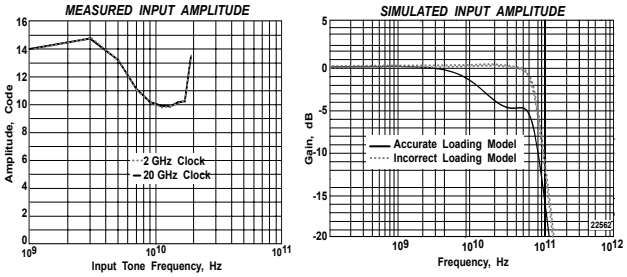

Fig. 7. Measured and Simulated Amplitude of Signal at Input of Comparators

Determining the maximum sample rate of the ADC for low frequency input tones is useful in finding out how well the back-end logic performs from a timing point of view. It also provides one measure of the robustness of the input clock receiver. Figure 8 shows the effective number of bits (ENOB) measured with an input tone of 10 MHz and a sampling clock in the range of 2 to 37 GS/s. The ENOB value of 4.3 to 4.4 remains fairly constant independent of

sampling frequency. The back-end logic starts to have timing issues past the sampling rate of 36 GS/s so the ENOB degrades significantly past that point. Testing of three additional devices showed sampling rate capability above 30 GS/s.

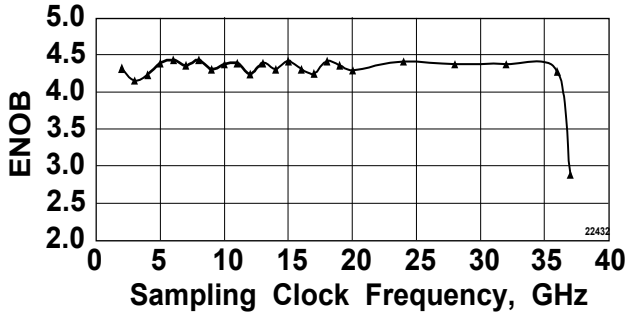

Fig. 8. Measured ENOB Versus Sampling Clock Frequency

Figure 9 shows the calculated ENOB under nominal and optimum supply voltage bias conditions. An increase in supply voltage to an optimal value, in an attempt to improve the suspected comparator saturation problem mentioned above, shows an improvement in ENOB. It can be seen that the ENOB values are fairly insensitive to clock frequency. This suggests that clock noise injection is not a problem.

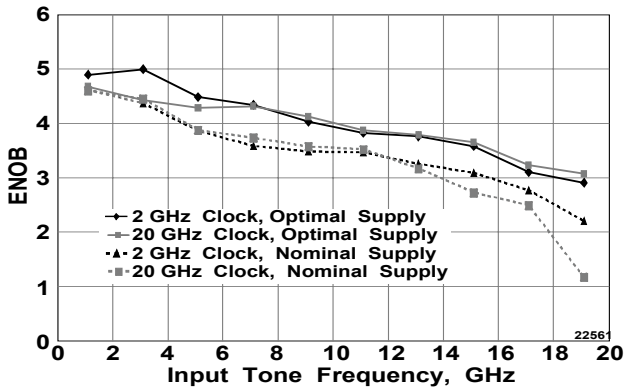

Fig. 9. Measured ENOB Versus Input Tone Frequency; Sampled at 2 GS/s and 20 GS/s

Table 1 shows a comparison of this work to other high sample rate SiGe BiCMOS-based FLASH ADCs. This device is capable of high sampling rates and high input bandwidth at a reasonable power dissipation.

V. Conclusion

In conclusion, a 5-bit flash ADC was developed and tested. A comparator with an exclusive-or function has been described, supporting Gray-Code outputs with significant power reduction. An input bandwidth of 20 GHz is achievable through the use of a low impedance input driver with a minor layout correction. Comparator offset correction through the use of electrical fuses has made it possible to achieve INL and DNL values of less than 0.1 LSB. The back-end Gray code logic achieved a sampling rate of 35 GS/s under nominal operating conditions. An ENOB value of greater than 4.0 was achieved with input tones up to 10 GHz. The nominal power dissipation was 4.85 W.

	TelAsic [7]	Lucent [1]	Nortel [2]	This Work
Publication	ISSCC 2004	JSSC 2004	ISSCC 2006	BCTM 2008
# of Bits	3	5	5	5
Max. Sampling Rate	40 GS/s	10 GS/s	22 GS/s	37 GS/s
Input Bandwidth	13 GHz	6.8 GHz	~10 GHz	20 GHz
Power Dissipation	3.8 W	3.6 W	3.0 W	4.8W
Technology	0.12um SiGe BiCMOS	0.18um SiGe BiCMOS	0.12um SiGe BiCMOS	0.12um SiGe BiCMOS

Table 1. Comparison of Different High Speed SiGe-Based Flash ADCs

Acknowledgments

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References

[1] J. Lee, P. Roux, U.V. Koc, T. Link, Y. Baeyens and Y.K. Chen, "A 5-b 10-GSample/s A/D Converter for 10-Gb/s optical Receivers," *IEEE Journal of Solid-State Circuits,* Vol. 39, pp. 1671-1679, October 2004.

[2] P.Schvan, D. Pollex, Shing-Chi Wang, C. Falt and N. Ben-Hamida, "A 22GS/s 5b ADC in 0.13um SiGe BiCMOS," *ISSCC Digest of Technical Papers,* pp. 572-573, Feb. 2006.

[3] C.-I. H. Chen, K. George, W. McCormick, J.B.Y.Tsui, S.L. Hary and K.M.Graves, "Design and Performance Evaluation of a 2.5 GSPS Digital Receiver," *IEEE Transactions on Instrument and Measurement*, Vol. 54, No. 3, pp.1089-1099, June 2005.

[4] K. Poulton, R. Neff, B. Setterberg, et.al., "A 20 GS/s ADC with a 1 MB memory in 0.18um CMOS," *ISSCC Digest of Technical Papers*, pp. 318-319, Feb. 2003.

[5] P.Schvan, J. Bach, C. Falt, et.al.,"A 24 GS/s 6b ADC in 90nm CMOS", *ISSCC Digest of Technical Papers,* pp. 544-545, Feb. 2008.

[6] B. Brannon, "Overcoming Converter Nonlinearities with Dither", Analog Devices Application Note: AN-410.

[7] W. Cheng, W. Ali, M.J. Choi, et.al., "A 3b 40GS/s ADC-DAC in 0.12um SiGe," *ISSCC Digest of Technical Papers,* pp. 262-263, Feb. 2004.