A 12-Bit 3 GS/s Pipeline ADC With 0.4 mm^2 and 500 mW in 40 nm Digital CMOS

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***Abstract*—A 12-bit 3 GS/s 40 nm two-way time-interleaved pipeline analog-to-digital converter (ADC) is presented. The proposed adaptive power/ground architecture eliminates the headroom limitations due to the deeply scaled power supply in nanometer CMOS technologies, while preserving the intrinsic speed of thin-oxide MOSFETs with minimum channel length for key analog blocks. Moreover, in terms of the signal swing, the proposed reference extrapolation scheme offers a smooth transition between the multiplying digital-to-analog converter stages and the last flash stage. With these two techniques, the ADC achieves a SNR of 61 dB and a DNL of $-0.5/+0.5$ LSB, while consuming 500 mW at a 3 GS/s sampling rate and occupying an area of 0.4 mm^2 in 40 nm CMOS process.**

***Index Terms*—Adaptive power and ground, CMOS technology, extrapolation, high resolution, high speed, multiplying-digital-to-analog converter (MDAC), pipelined analog-to-digital converter (ADC).**

I. Introduction

DRIVEN by the unprecedented advancement in technology, modern communication systems and measurement instruments replace the conventional analog processing blocks with their digital alternatives to save power and reduce silicon area. This change creates a great demand for high-speed and high-resolution analog-to-digital converters (ADCs). Compared with other conversion architectures such as flash [1], folding [2], [3], and successive approximation register (SAR) [4], [5], the pipeline conversion architecture offers the optimal tradeoff between conversion speed and resolution [6]. This architecture achieves an n-bit quantization by cascading several coarse digitization stages, as shown in Fig. 1. Except for the last flash stage, each stage consists of a sampler, a coarse ADC, a digital-to-analog converter (DAC), and an amplifier. A pipeline stage takes the difference between the sampled voltage and its quantized version offered by the coarse ADC and the DAC to obtain the residual voltage. The residual voltage is further amplified by a precision amplifier to the full scale and is quantized by the subsequent stages. The DAC and the amplifier are typically called the multiplying-DAC (MDAC). Typically the stage resolution is 4 bits/stage or less, so the resultant stage scaling offers optimal power efficiency [7], and the reasonable complexity of MDAC stages is also good for fast stage operation. Enabled by concurrent operations of all pipelined stages, the conversion rate of the whole ADC is the same as that of a single stage.

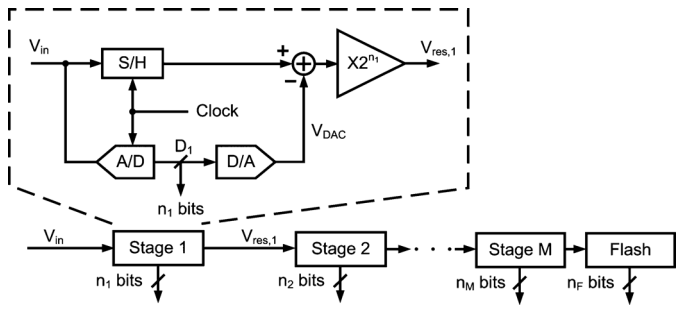

Fig. 1. Block diagram of a typical pipeline ADC.

Although advanced fabrication technologies deliver high f_t MOSFETs, the accompanying side effects, such as low breakdown voltage, low power supply, low intrinsic device gain, and deteriorated device noise, make the analog design environment increasingly hostile. For precision amplifiers in pipeline ADCs, low power supply voltages pose the most significant design challenge. As the usable signal swing shrinks proportionally, the desired signal-to-noise ratio (SNR) becomes difficult to achieve. [8] shows that pipeline ADCs with a split correlated level shifting technique can handle rail-to-rail signal swing to mitigate the SNR challenge. But unless multiple power supplies are used, it is extremely difficult for the preceding blocks of the ADC to provide the full-swing signals in an SoC environment. Meanwhile, low supply voltages also force designers to minimize the number of MOSFET stacks in precision analog circuits. Therefore, single-stage telescopic cascode amplifiers [9], not to mention double cascode amplifiers, are abandoned nowadays. Instead, folded cascode amplifiers become the main stream for pipeline ADCs in deep submicrometer technologies [10], [11]. The signal swing, however, comes at the expense of other analog merits, including dc gain, current efficiency, operation speed, phase margin, and noise performance. In addition, low intrinsic device gain, due to various short channel effects, further deteriorates the design space of precision amplifiers which, according to the feedback theory, require high open-loop dc gain. To deliver sufficient dc gain for a 14-bit 20 MS/s ADC in 0.18 μm CMOS, the nested gain boosting technique presented in [7] recursively applies a two-level gain booster to a pseudo-differential cascode amplifier. A three-stage amplifier with reversed nest miller compensation is built in [12] for a 12-bit 160 MS/s ADC in a 65 nm process. Unfortunately, these techniques involve complex differential-mode and common-mode signal paths and a sophisticated compensation

Manuscript received August 27, 2011; revised November 18, 2011; accepted December 26, 2011. Date of publication February 29, 2012; date of current version March 28, 2012. This paper was approved by Guest Editor Makoto Nagata.

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Digital Object Identifier 10.1109/JSSC.2012.2185192

scheme that exempts them from being considered for multi-gigahertz applications. Other works suggest digital-friendly alternative structures, such as the dynamic amplifier and the comparator-based MDAC stage, but they also face many speed and/or accuracy bottlenecks and thus cannot be immediately applied in most modern wideband applications [13], [14]. To address these design difficulties of high speed and high resolution pipeline ADCs in deep submicrometer technologies, this paper proposes an adaptive power/ground technique that allows the coexistence of the high power supply and the fast nanometer MOSFETs. The proposed technique enables the most power-efficient and fastest single stage telescopic cascode amplifier, with gain boosting for all sample-and-hold amplifiers (SHAs) and MDACs in a 12-bit 1.5 GS/s single-channel ADC in 40 nm CMOS [15].

The last stage of the pipeline ADC shown in Fig. 1 is a flash ADC with the signal swing matching that of MDAC stages. Designing a power-efficient multigigahertz 6-bit flash ADC with good differential/integral nonlinearity (DNL/INL) performance is nontrivial. Power efficiency is typically achieved by scaling the size of comparator and reducing the number of components in the comparator bank. Averaging is an effective and popular technique to relax the matching requirement of comparators based on a low-pass spatial filtering mechanism, thus allowing the input pairs of preamplifiers to be aggressively scaled [16], [17]. On the other hand, the interpolation technique effectively reduces the required number of preamplifiers by creating more decision levels from adjacent preamplifiers [18]. Combining these two techniques not only saves the power of preamplifiers but also reduces the total input capacitance, which relaxes the design of the preceding block. It is known that, due to the asymmetric nature of the signal, averaging suffers from the boundary effects close to the upper and bottom signal swing. The conventional solution to maintain good linearity at the boundaries is to extend the reference voltages and preamplifiers so that the uniform range covers the whole signal swing [19], [20]. These dummy amplifiers not only incur power penalties but also require overranged reference voltages. In pipeline ADCs, the extended reference voltages of the flash stage cannot be shared with those of the MDACs. Moreover, separate reference voltages for MDACs and the flash ADC create a stage mismatch, which hurts the overall linearity. A triple-cross termination scheme is proposed as an effective way to avoid extended reference voltages, but the undermined gain of amplifiers at the boundaries due to the negative transconductance of interface amplifiers can worsen the INL at both ends [21]. This paper introduces a reference voltage extrapolation scheme that overcomes the boundary effects without the necessity of extending reference voltages beyond the signal swing or the gain reduction of boundary amplifiers.

To further push the conversion speed, the time-interleaving technique is also adopted [22], [23]. With an interleaving factor of two, as shown in Fig. 2, this ADC eventually achieves a 3 GS/s sampling rate with a 12-bit resolution. The timing mismatch between each slice is compensated by digital filters [25].

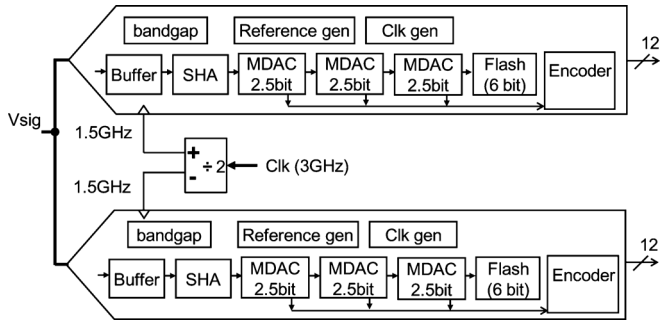

Fig. 2. Two-way time-interleaved pipeline ADC.

Section II discusses the tradeoff of high-performance pipeline ADC design, which justifies the adaptive power/ground technique and the reference voltage extrapolation for the flash stage in pipeline ADCs. Sections III and IV present detailed descriptions of the adaptive power/ground structure and the reference voltage extrapolation, respectively. Section V presents the measurement results. Section VI presents the conclusions reached in this paper.

II. Background

In typical pipeline ADC structures, the amplifiers used in the SHA and MDAC stages consume the most power. The required minimum unity gain bandwidth f_u for the amplifier is proportional to the sampling frequency f_s

$$f_u = \frac{g_m}{2\pi C} = \alpha f_s \tag{1}$$

where α is a constant related to ADC resolution and the stage feedback factor, C is the output loading capacitance, and g_m is the transconductance of the amplifier, which can be further expressed as

$$g_m = \frac{2\eta I_D}{V_{\mathrm{DSAT}}} = \frac{2\eta \cdot \mathrm{Power}}{V_{\mathrm{DSAT}} \cdot V_{\mathrm{DD}}} \tag{2}$$

where V_{DSAT} is the overdrive voltage, η is the factor of current efficiency, which depends on the amplifier architecture. For example, η of a telescopic cascode amplifier and that of a folded cascode amplifier with a branch ratio of 1:1 are 100% and 50%, respectively.

For high resolution pipeline ADCs, C is determined by the kT/C noise to meet the SNR requirement

$$\mathrm{SNR} = \frac{V_s^2}{V_n^2} = \frac{V_s^2}{\lambda \frac{kT}{C}} = \frac{\beta^2 V_{\mathrm{DD}}^2}{\lambda kT} C \tag{3}$$

where V_S is the root-mean-square voltage of the usable signal swing. Therefore, V_S^2 defines the maximum affordable signal power. $V_n^2$is the total noise power. β denotes the voltage efficiency defined by the ratio of the supply voltage V_{DD} to the V_S. $\lambda(\lambda > 1)$ is the noise-excess factor—the total amount of noise over the sampling noise. Combining (1)–(3), the figure of merit (FOM) can be written as

$$\frac{\mathrm{Power}}{\mathrm{SNR} \cdot f_s} = \frac{\pi \alpha \lambda kT}{\eta \beta^2} \cdot \left(\frac{V_{\mathrm{DSAT}}}{V_{\mathrm{DD}}} \right). \tag{4}$$

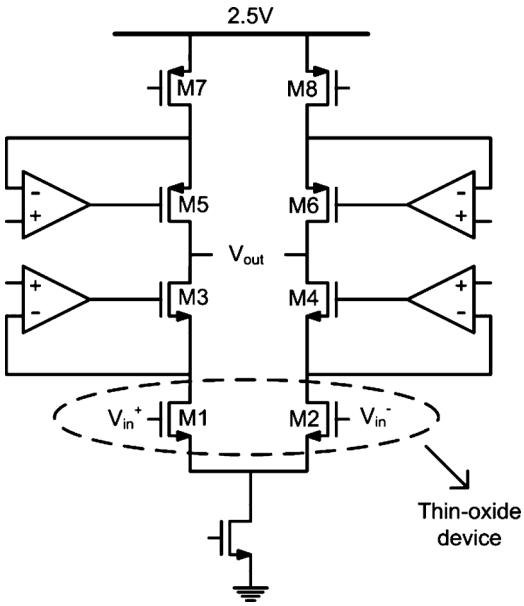

Fig. 3. Fully differential amplifier.

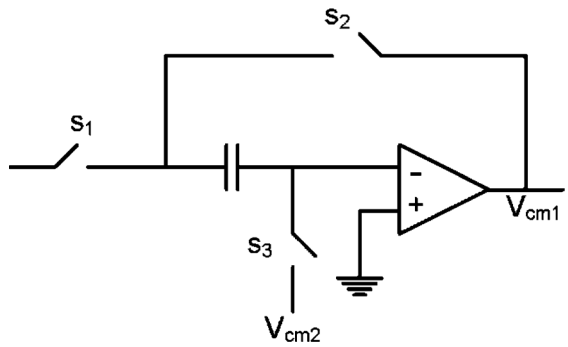

Fig. 4. Block diagram of sample-and-hold circuit.

To optimize the FOM, the amplifier design should use the maximum supply voltage to increase the signal swing. Therefore, in our pipeline ADC, the amplifiers use a 2.5 V supply to maximize the signal swing. Meanwhile, with appropriate protection, the g_m devices are implemented by thin-oxide MOSFETs with minimum feature size in the 40 nm technology and a large W/L ratio. Thus, they offer sufficient g_m with minimum $V_{\rm DSAT}$ as well as a small parasitic capacitance, which are optimal for the wide bandwidth and the good phase margin. In addition, the adoption of 2.5 V supply enables a single-stage telescopic cascode amplifier, which has a small λ and a large η, compared with the folded cascode counterpart. Meanwhile, it further enhances the amplifier speed, stability, and SNR performance.

III. Adaptive Power/Ground for CMOS Switch and Logic

The key to achieving high speed and high resolution in this work is the combination of a 2.5 V supply for amplifiers and 40 nm thin-oxide MOS transistors for both g_m devices and switches. The use of a 2.5 V supply maximizes the peak-to-peak differential signal swing to 1.4 V and improves the SNR compared to using a 1 V supply based on (4).

Fig. 3 shows the amplifier structure used in the SHA and MDACs. To achieve wide bandwidth, good phase margin, and low noise, a single-stage amplifier structure is chosen. In addition, high amplifier gain that is required for 12-bit linearity is achieved by using a telescopic cascode structure with the assistance of gain boosting [9]. The input devices of gain-boosting circuit are also implemented with thin gate device to improve the bandwidth.

The use of a 2.5 V supply allows a large signal swing which, according to (4), improves power efficiency for a given SNR. Thin-oxide nMOS transistors M1 to M6 are used to achieve high g_m and low $V_{\rm DSAT}$ while having low parasitic capacitance for wide bandwidth and fast settling [24]. These input devices of M1 and M2 are protected by cascode devices M3 and M4 to prevent breakdown and reliability issues induced by over-voltage. The transistors M7 and M8 are thick-oxide devices to protect the thin-oxide devices from 2.5 V supply. Fig. 4 shows the block diagram of the SHA circuit. The amplifier output common-mode voltage $V_{\rm cm1}$ and the input common-mode voltage $V_{\rm cm2}$ track over process, supply voltage, and temperature (PVT) variations for optimum operating points.

Another critical component for high-speed pipeline ADC design is the CMOS switch that turns on and off the capacitors for signal sampling and charge transfer. In Fig. 5(a), a 2.5 V supply is used in the amplifier design, and the output common mode of the signal is about half the supply, which is about 1.25 V. Conventionally, to avoid breakdown issues, it is straightforward to implement switches S1, S2, and S3 using thick-oxide CMOS transistors with a minimum channel length of 0.25 μm in standard 40 nm CMOS technology. The thick-oxide devices, however, are slow and become the bottleneck of the ADC speed.

Table I compares the performance of a thin-oxide device under 1.0 V and a thick-oxide device under 2.5 V. From a transient analysis, the rise time is 6 ps with a fan-out of 4 for the thin-oxide inverter, whereas it is 170 ps for the thick-oxide inverter. The thin-oxide device is 28 times faster, and it consumes 1/10 the power. The fast rise and fall time characteristics are important for the switched capacitor circuit to quickly switch between the sample and hold modes. From a dc analysis, the on-resistance of the thin-oxide device is 90 times lower than that of the thick-oxide device. The smaller *RC* time constant makes the switched capacitor circuit charge and discharge faster. In addition, the thin-oxide device has a smaller parasitic capacitance, which helps to reduce the loading and improve the feedback factor for the amplifier. Therefore, to maximize the bandwidth in our design, it is crucial to use a thin-oxide device with minimum channel length as the switching device.

Because of reliability concerns, however, the thin-oxide device operating with a 1 V supply voltage does not comply with the 2.5 V amplifier design due to the difference of the common-mode voltage shown in Fig. 5(a). It would be desirable to level-shift up the power and ground of the thin-oxide switches, so that the common-mode voltage matches that of the amplifier shown

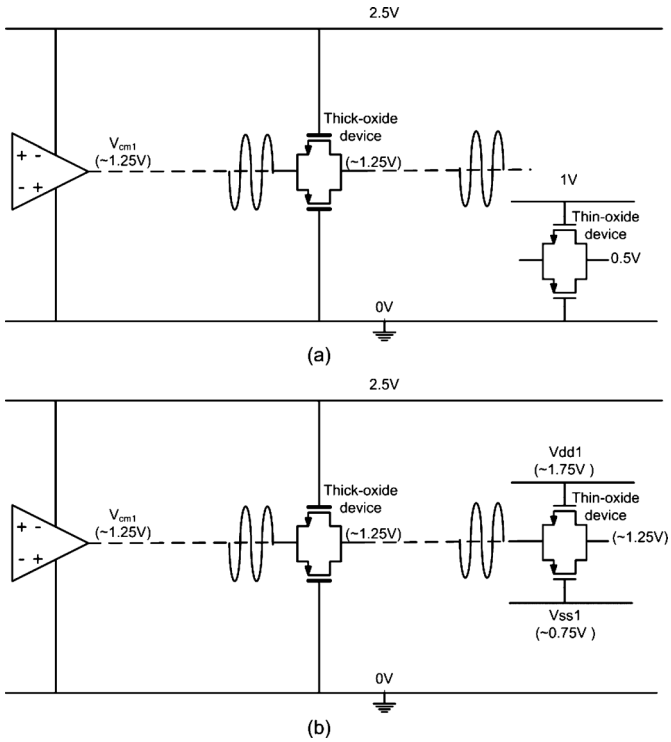

Fig. 5. Common-mode voltage of amplifier and switches.

TABLE I
COMPARISON OF THIN-OXIDE AND THICK-OXIDE DEVICES

	Transient analysis			DC analysis	
	Tr (ps)	P(μW)	Load	W/L	Ron (Ω)
1V thin-oxide inverter	6	16	FO4	10	3.8
2.5V thick-oxide inverter	170	160	FO4	10	344

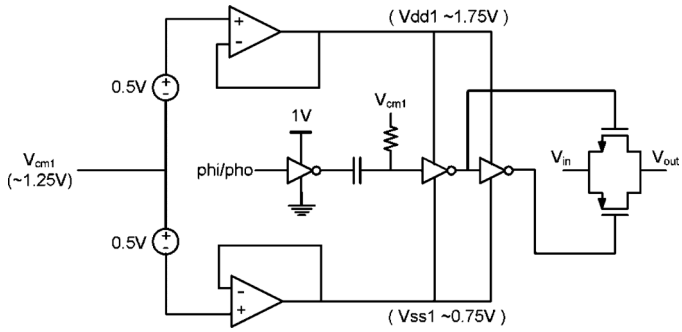

Fig. 6. Block diagram of adaptive supply/ground for CMOS switch and logic.

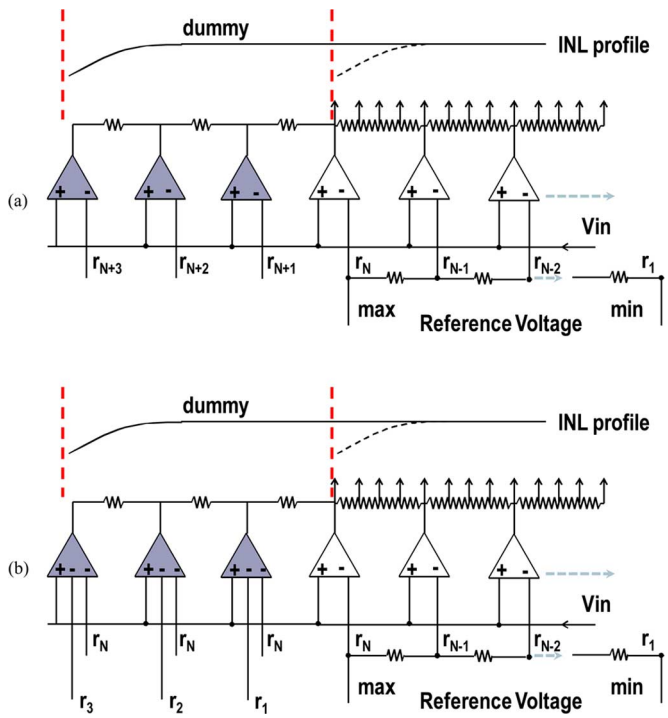

Fig. 7. (a) Averaging/interpolation with over-ranging. (b) Averaging/interpolation using reference voltage extrapolation.

in Fig. 5(b). This solution uses the adaptive power/ground technique proposed in this paper. In Fig. 6, the switches and the corresponding driver stages are all implemented using thin-oxide devices. To accommodate the large signal swing, the midpoint voltage of the local power and ground ($V_{\rm dd1}$ and $V_{\rm ss1}$) is designed to be the same as the amplifier output common-mode voltage ($V_{\rm cm1}$). On the other hand, to keep the voltage stress of the switching device within the safe level, the difference between V_{dd1} and $V_{\rm ss1}$ is regulated to be equal or less than 1 V, which is limited by the 40 nm technology. The $V_{\rm dd1}$ and $V_{\rm ss1}$ are generated internally using two low dropout regulators (LDOs). For the best performance, the common-mode voltage of the LDOs tracks with the output common-mode voltage of the amplifier over PVT variations. The reference voltages for the LDOs are level-shifted up and down with a constant 0.5 V from this common mode voltage. They are generated from a replica circuit that duplicates the common mode voltage circuit in amplifiers but with 0.5 V IR drop above and below. The IR drop is referenced to bandgap circuit and is almost constant over process, temperature, and supply variation. In addition, the LDOs provide better power supply rejection for the switches, and they improve the isolation of the ADC. The ADC clock is level-shifted up through an AC coupling capacitor with a DC biased voltage of $V_{\rm cm1}$ to $V_{\rm dd1}/V_{\rm ss1}$ domain to drive the thin-oxide drivers and switches.

The same amplifier and switch topology is used in all the MDACs to achieve high-speed performance. Because the speed of the Flash ADC is critical for the MDAC operation, the thin-oxide devices are used to utilize fully their speed advantage. To digitize the high swing and high common-mode analog signal, the 2.5-bit Flash ADC in the MDAC is also implemented in the adaptive power domain. The 6-bit thermometer code from the Flash ADC is in the adaptive power domain to control the switched capacitor circuit in MDACs, whereas for the encoder, the 2.5-bit binary output is level-shifted down to the 1 V domain.

With the adaptive power/ground topology, the digital power and ground track with the analog circuit over the PVT. This key enabling technique allows us to combine the amplifier using a 2.5 V supply and high speed thin-oxide switches to achieve a wide-bandwidth ADC.

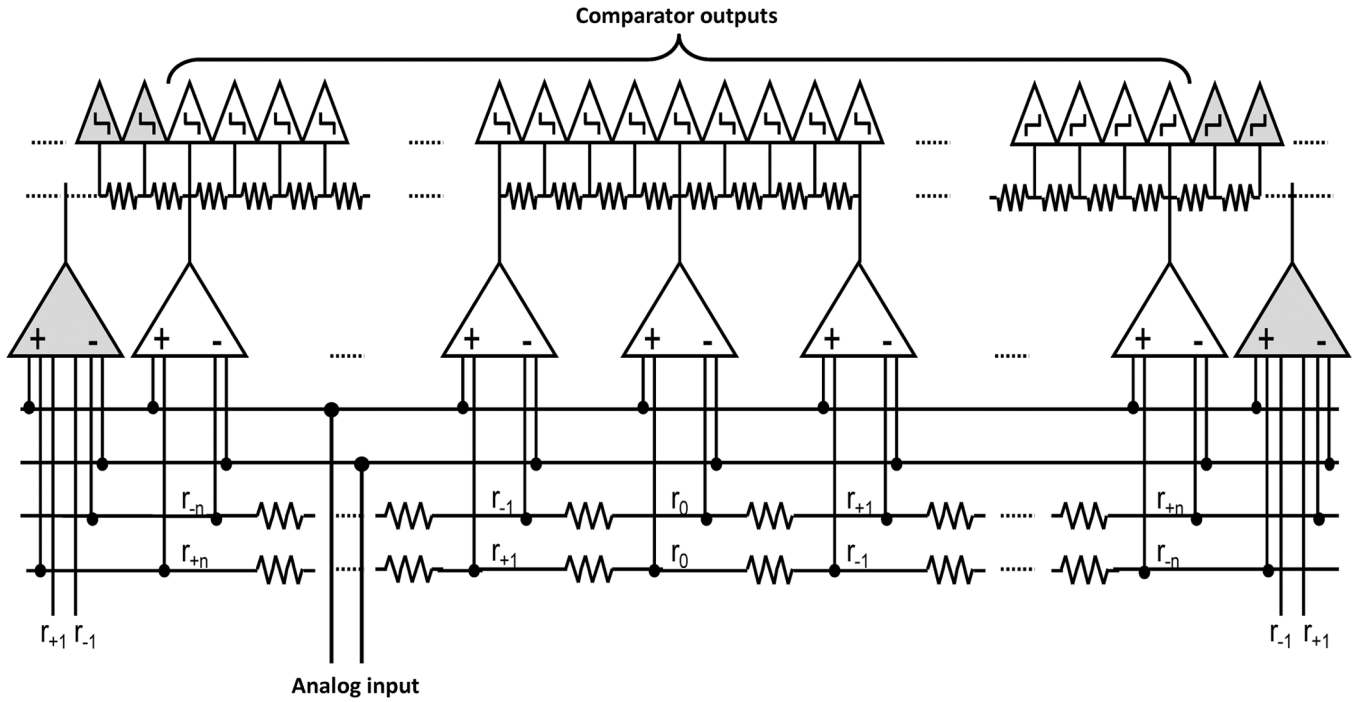

Fig. 8. Schematic of 6-bit Flash ADC.

IV. Flash ADC Design Using Reference Voltage Extrapolation

In this work, a 6-level Flash ADC generates a 2.5-bit digital output in each MDAC; a 6-bit Flash ADC digitizes the final residue. Both Flash ADCs must convert large voltage swings and produce a digital output within a fraction of the 1.5 GHz clock period, while still keeping a low-input capacitive load to maximize the signal bandwidth. The 40 nm thin-oxide devices offer great advantage for Flash ADCs over thick-oxide devices because the regeneration time can be an order of magnitude shorter. These Flash ADCs use 40 nm thin-oxide transistors exclusively, relying on carefully designed bias under multiple power/ground rails to prevent breakdown and reliability issues.

To minimize the input capacitance, the 6-bit Flash ADC uses averaging to relax the input matching requirement and interpolation to reduce the number of preamplifiers [16]–[21]. The averaging requires overranging with extra reference voltage taps outside the normal reference voltage range and dummy preamplifier cells at the edges to compensate for the INL degradation due to the boundary effect [19], [20]. Because of the limited headroom in the preamplifiers, this overranging usually leads to a reduction of the effective reference voltage and the input full-scale range, which also lowers the SNR. For example, as shown in Fig. 7(a), given a fixed headroom requirement, the input full-scale range will be reduced by a factor of r_N/r_{N+3} by overranging.

In this design, a reference voltage extrapolation method is employed to generate the extra reference voltage taps using the existing taps in the reference ladder. As shown in Fig. 7(b), three-input dummy preamplifiers at the edges generate the overranging voltages from the inner taps of the reference ladder by analog addition. For example, the extra reference voltages r_{N+K} can be extrapolated from existing voltage taps r_N and r_K as

$$r_{N+K} = r_N + r_K. \tag{5}$$

This reference voltage extrapolation technique allows voltages beyond the input full-scale voltage range to be generated without changing the reference ladder. It overcomes a common problem of the averaging and interpolation techniques and maximizes the input full-scale range, leading to higher SNR. The schematic of the 6-bit Flash ADC is shown in Fig. 8. It uses resistive averaging and 4:1 interpolation along with differential reference voltage extrapolation. Dummy latches are placed at the edges to match the capacitance and kickback at a high clock frequency.

The resistive averaging requires the preamplifiers to have a large input linear range, which is limited by low supply voltage. The reference voltage extrapolation demands the two-input preamplifiers and the three-input edge dummy preamplifiers to have the same gain and output common-mode level. To meet these requirements, a folded preamplifier topology is used. Fig. 9 shows a three-input folded preamplifier. The folded topology allows the preamplifier input stage and the output stage to be biased and optimized independently. The input stage functions as a g_m summer to realize the reference voltage extrapolation. The input stage is optimized for maximum input range without affecting the gain. The output stage is optimized for maximum output linear range while avoiding reliability problems. Both two-input and three-input preamplifier cells have the identical output loading resistors with the same output current to maintain the same gain and output common-mode level. To minimize the effect of the pMOS transistors M5 and

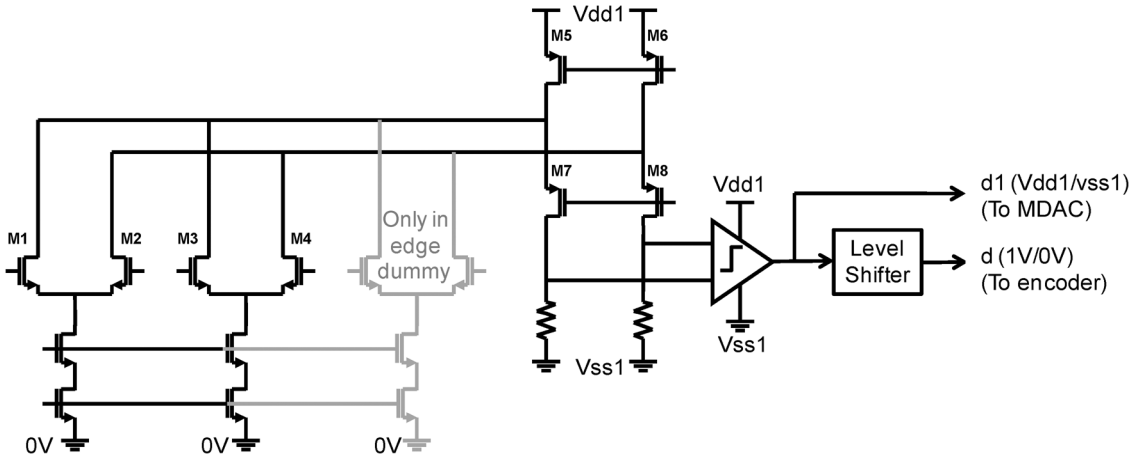

Fig. 9. Schematic of folded preamplifier under multiple power and ground rails.

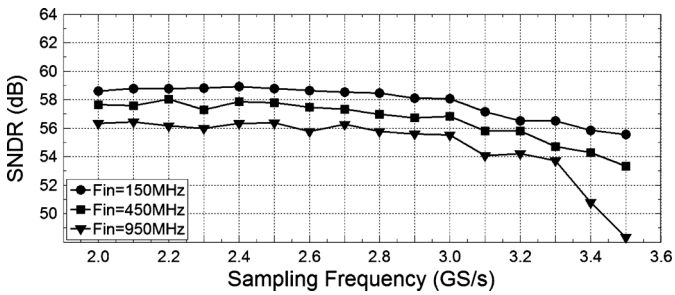

Fig. 10. SNDR versus sampling frequency.

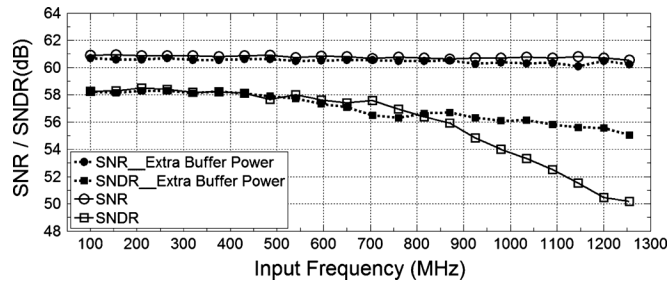

Fig. 11. SNR/SNDR versus input frequency with 2.5 GS/s sampling rate.

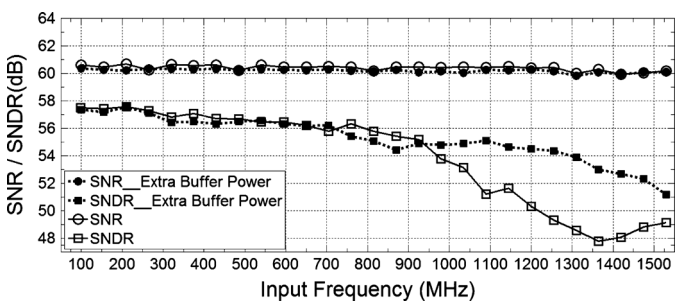

Fig. 12. SNR/SNDR versus input frequency with 3.0 GS/s sampling rate.

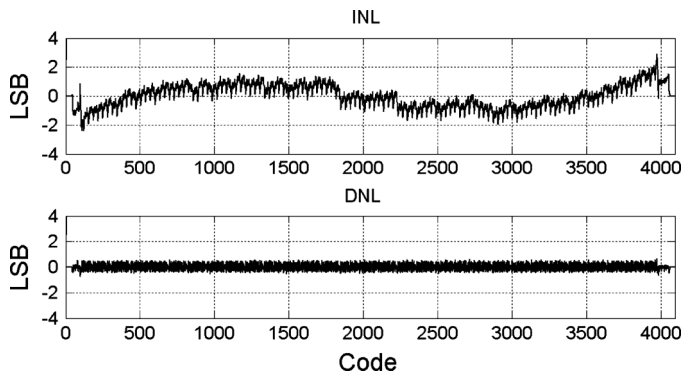

Fig. 13. INL and DNL characteristic.

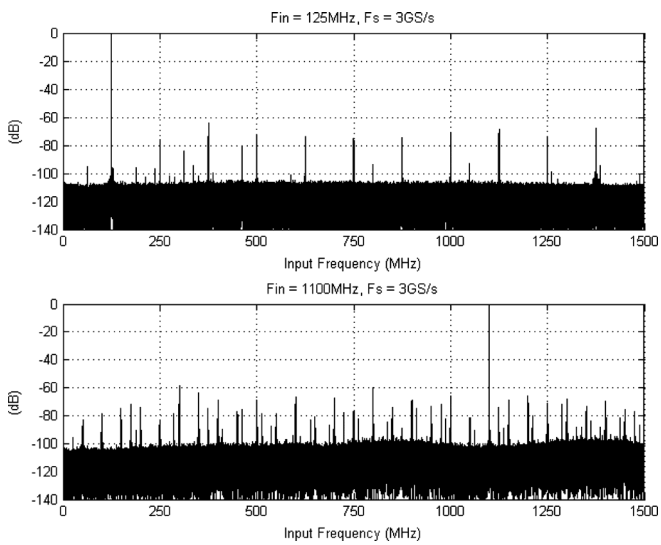

Fig. 14. ADC output spectrums of 125 and 1100 MHz signal frequencies.

M6 on the preamplifier offset, they are designed to have large area and large V_{DSAT}.

The folded preamplifiers are used in both the 2.5-bit Flash ADCs inside the MDACs and the 6-bit Flash ADC. They are designed to operate under multiple power/ground rails. Their V_{dd1} supply is generated from the same LDOs for the switches (see Fig. 6) to provide enough headroom for a large input range. The latches are operated between V_{dd1} and V_{ss1} as the switches. In the 2.5-bit Flash ADCs, the latch output between V_{dd1} and V_{ss1} directly controls the MDAC switches in the same power domain. For the 6-bit Flash ADC, high-speed level shifters convert the latch output down for the encoder in the 1 V digital power

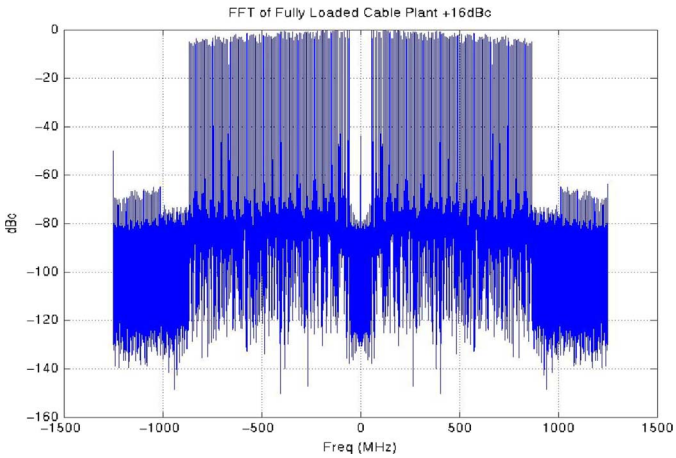

Fig. 15. ADC output spectrum of 1 GHz QAM signal.

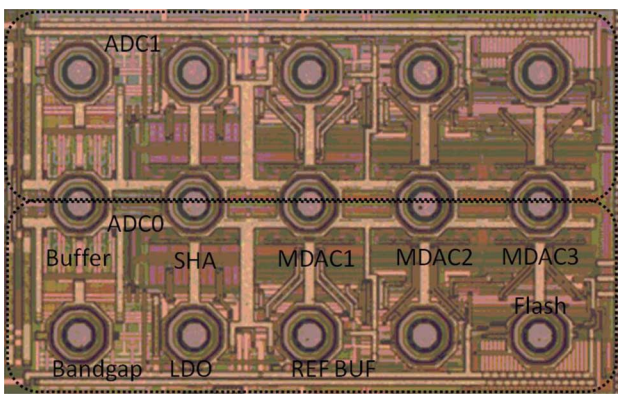

Fig. 16. Die photograph. The size is 756 um by 506 um.

domain. The use of multiple adaptive power/ground rails allows both the 6-bit Flash ADC and the 2.5-bit Flash ADC to be implemented with 40 nm thin-oxide devices exclusively without any breakdown and reliability issues.

V. Measurement Results

Fig. 10 shows the measured SNDR as a function of sampling frequency. With input frequency under 1 GHz, the ADC can remain above 50 dB up to 3.4 GS/s sampling rate, or over 55 dB with 3 GS/s sampling frequency. Figs. 11 and 12 show the measured SNR and SNDR as functions of input frequency with 2.5 and 3 GS/s sampling frequency, respectively. The SNR is almost constant with 60 dB from 100 MHz to 1.5 GHz input frequency at sampling rate of 3 GS/s. The peak SNDR is 58 dB. The SNDR remains above 50 dB up to 1.2 GHz input frequency and up to a 3 GS/s sampling rate. With an additional 35 mW consumed by the internal input buffer, the SNDR can stay above 51 dB up to 1.5 GHz input frequency, shown with a solid curve in Fig. 12. This figure shows that the SNDR is limited by the internal input buffer but can be improved by using higher power. The DNL is within ± 0.5 LSB, and the INL is within ± 3 LSB, as shown in Fig. 13. Fig. 14 shows the output spectrum for signal frequencies at 125 MHz and 1.1 GHz with sampling rate of 3 GS/s.

TABLE II
Comparison of $>$500 MS/s and $>$10 bit ADCs

References	[22]	[23]	[3]	[26]	This work
Process (nm)	130	90	180	90	40
Resolution (bit)	11	11	10	11	12
Fs (GS/s)	1	0.8	1	0.5	3
SNR (dB)	59	60	57	-	61
SNDR (dB)	55	58	56	53	58
Power (mW)	250	350	1260	55	500
Area (mm^2)	3.5	1.4	49	0.5	0.4

Fig. 15 shows the ADC output spectrum with a 1 GHz wideband QAM input signal. Fig. 16 shows the die photograph. The ADC consumes 500 mW from a 2.5 V supply and occupies an area of 0.4 mm^2 in a 40 nm digital CMOS process.

VI. Conclusion

We have shown that the proposed adaptive power/ground technique overcomes the stringent headroom requirements of precision analog circuit design in advanced CMOS technologies. Therefore, the nanometer devices with superb f_T can be incorporated into classic and mature analog structures, which enables high-speed, high-resolution, and low-power analog-to-digital conversion. Moreover, we have shown that the proposed reference extrapolation scheme seamlessly stitches the flash stage with the MDAC stages, the result of which is that the design has low complexity and avoids potential error sources. Finally, we have shown that these two schemes lead to the optimal tradeoff among speed, resolution, and power dissipation of pipeline ADCs, thus enabling a 12-bit 3 GS/s two-way interleaved 40 nm CMOS pipeline ADC. Table II shows the comparison of our results with previous published papers for ADCs with higher than 10-bit resolution and faster than 500 MSPS.

Acknowledgment

The authors would like to thank the following colleagues at Broadcom Corporation for their contributions to this project: A. Venes, J. Dou, T. Williams, T. Wang, K. Lai, P. Cangiane, S.-W. Chen, R. Gomez, S. Jaffe, L. Tan, M. Oo, S. Liu, K. Y. Kim, and K. Bult.

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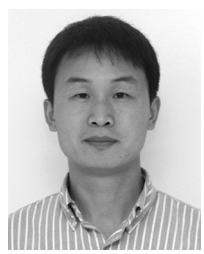

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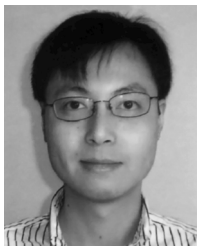

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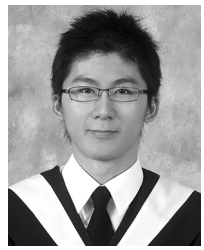

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