High Speed Comparator for Flash ADC and UWB Application in 130 nm CMOS Technology

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***Abstract*— High speed comparator for high-speed flash analog-to-digital converter (ADC) and ultra wideband applications that can work at a sampling rate of 7 GS/s is presented in this paper. This fully differential comparator consists of three stages using a new structure to improve its performance. The offset voltage of the designed comparator has been reduced by means of an active positive feedback. The analyses and simulation results were obtained by using 130 nm CMOS parameters. The comparator can operate with a 1 V peak-to-peak input range consuming 371 µW. The predicted performance is verified by analyses and simulations using HSPICE tool.**

***Keywords:* Analog-to-digital converter, comparator, flash, high speed, preamplifier.**

I. INTRODUCTION

Flash analog-to-digital converters (ADC) with ultra wide-band frequency sampling rates are critical components for applications such as radar, signal capture, satellite, digital oscilloscopes and waveform recorders [1]. Today researchers and the industry have extended the requirement for higher frequency and higher sample rate. Flash ADCs can generally achieve the higher sampling rates, with the comparator limiting the maximum achievable sampling speed. In addition, this comparator can be used for ultra wideband (UWB) and X-band technology that offer a lot of capability for the design of communications devices requiring very high performance and low power consumption. The comparators published in recent years [2],[3],[4] still have relatively high power consumption and operate with sampling rate lower than the expected future requirement in CMOS technology. Some papers proposed the use of new BICMOS structure to improve speed of comparators but its high power consumption and makes it not practical for use in flash ADC [2].

In this paper a new CMOS positive feedback and output logic is proposed to increase the speed of track and hold (T/H) of the comparator. A new structure is also proposed to achieve the overall high speed for the comparator. The comparator design incorporates various techniques to lower its power consumption and improve its overall performance.

The comparator architecture is described in Section II. The preamplifier design, T/H and output domino logic are presented in Section III. Section IV shows the simulation results, and finally Section V is the conclusion.

II. ARCHITECTURE

The architecture of the comparator is shown in Fig. 1 , The comparator structure is fully differential and consists of preamplifier, T/H and output circuits. The first stage is a low gain classical differential amplifier with resistive loads (RD), which isolates the latches from reference voltages. The comparator with resistive loads shows better linearity, offset and gain response in comparison with amplifiers with active or diode loads. Low noise amplifier (LNA) is utilized to reduce the input referred offset of the comparator.

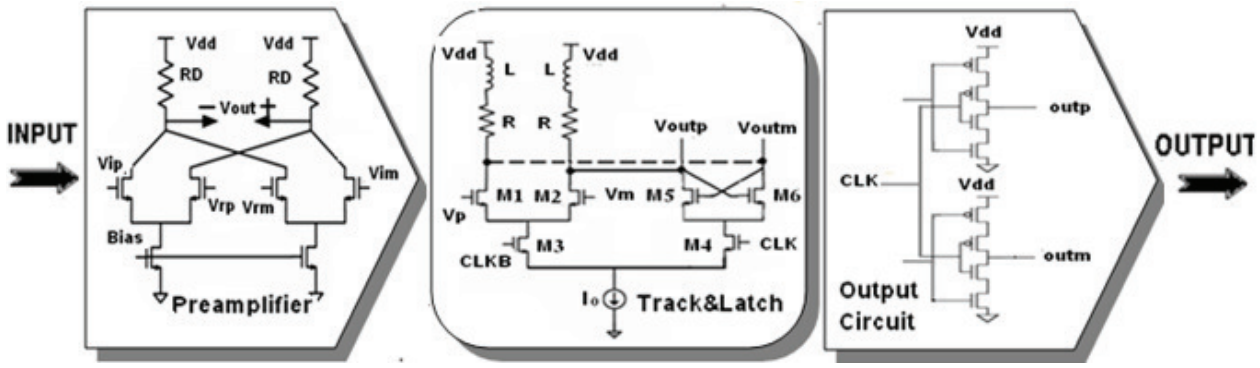

Fig.1 Schematic of comparator

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The second stage is a CMOS T/H with positive feedback and use of inductor and current source to reduce regenerative time.
What aspects of the performance of comparator are important? In addition to power dissipation and speed, such parameters as supply voltage, gain, voltage swings, band width, distortion, input offset, linearity and overdrive recovery may be important. In practice, most of these parameter trade with each other, making the design a multi-dimensional optimization problem. Illustrated in Fig.2 such trade-off present many challenges in the design of high quality comparator for flash ADC, requiring intuition and experience to arrive at an acceptable compromise .

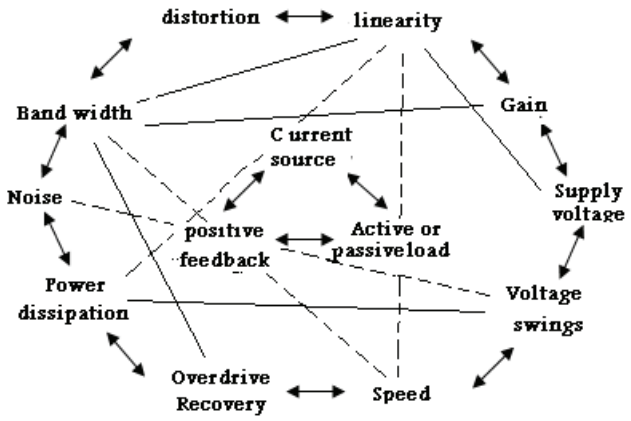

Fig.2 Relationship between comparator design parameters

III. COMPARATOR DESIGN

A. Preamplifier

The LNA preamplifier is shown in Fig. 3 .The main role of LNA is to reduce the input referred offset of the comparator. The preamplifier acts as an isolator between voltage reference and T/H to improve bandwidth and decrease input offset. The preamplifier has two inputs for differential analog signal and two inputs for voltage reference. There is a relation between offset and W/L of the preamplifier [6,7] that can be characterized by

$$Voffset = \Delta Vt + \frac{1}{gm}\left[\frac{\Delta W1}{W1} + \frac{\Delta L1}{L1} + \frac{\Delta W2}{W2} + \frac{\Delta L2}{L2} + \cdots + \frac{\Delta Wn}{Wn} + \frac{\Delta Ln}{Ln}\right] \quad (1)$$

where *Vt* is the threshold voltage, *gm* is the transconductance, and W and L are width and length respectively .
Equation (1) indicates that with increase of transistor size (W), offset will be reduced, but this increase depends on the design. In addition, swing, bandwidth, output capacitance and linearity are important factors to choose the load of pre-amplifier. The linearity and frequency response of the preamplifier with passive load is better than preamplifier with active load. It is important to note that, with increasing LNA gain, the bandwidth is also decreased.

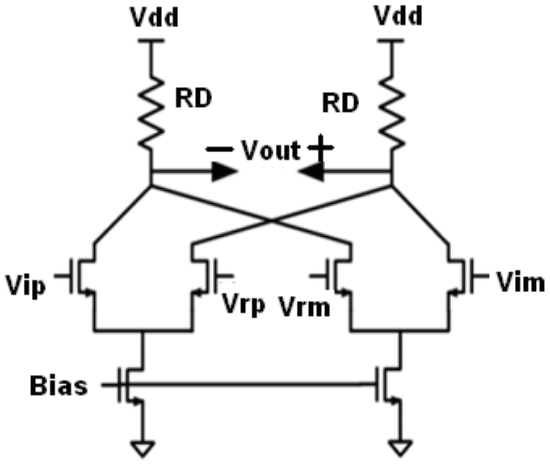

Fig.3 Preamplifier

B. Comparator core (T/H) and Output circuit

The comparator core is shown in Fig. 4. The load is formed by the series combination of a resistor and an inductor. *Vp* and *Vm* are the differential analog inputs signal from the preamplifier. It has input differential pairs (MI and M2) that turn on when the clock is low and track the input from the previous stage. When the clock is high, the comparator goes into hold mode. In this paper CMOS positive feedback is used to improve speed of comparator and reduce the regenerative time in latching mode. To achieve optimum performance, the behavior during the reset, tracking and regenerative phases should be considered.
The passive inductor peaking technique is also employed in the T/H circuit to enhance the bandwidth [8], [9], [10]. We note that a nonzero inductance improves the regeneration speed, and a more detailed analysis [8] shows that the regenerative time constant decreases monotonically with L. Therefore, the largest possible inductance is preferred. In addition, for high speed operation, there is a trade of between speed and power dissipation. With increase current source and supply voltage, speed and linearity will go up but power consumption is a big penalty. The domino output circuit as shown in Fig.5 is used instead of SR Latch to support the comparator in high sampling rate operation. The combination of T/H and output circuit creates a fast structure for the comparator. Mismatch was an important consideration while using the 180 nm process to design the comparator, therefore with careful sizing of transistors, it helped to mitigate these errors.

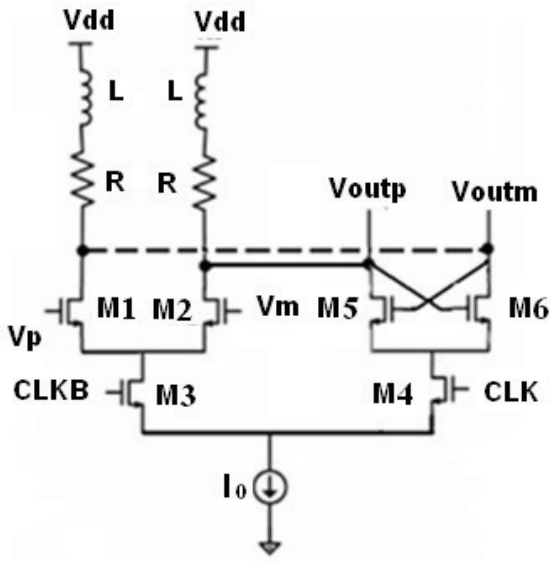

Fig.4 Comparator core (Track/Hold)

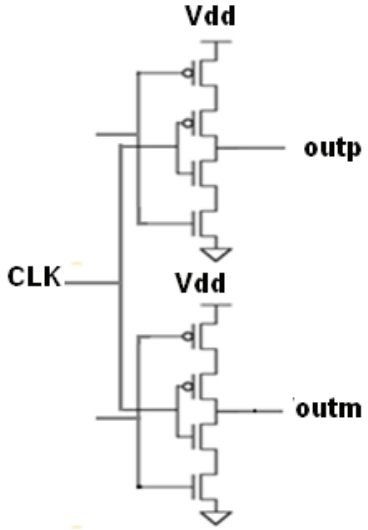

Fig.5 Output circuit of comparator

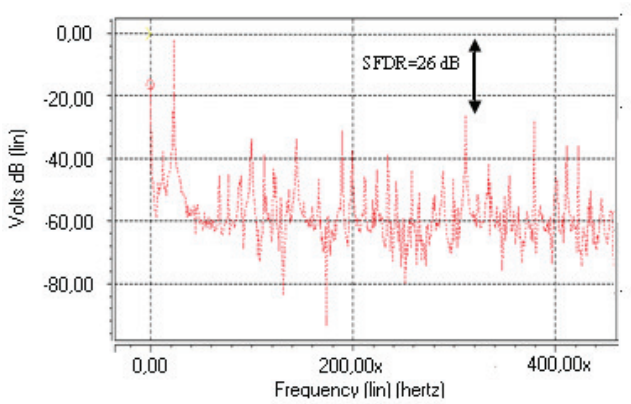

Fig.6 FFT at input frequency of 500MHz and sampling rate of 7Gs/s

IV. SIMULATION RESULTS

The proposed comparator structure was designed using 130 nm CMOS technology. All transistors used were CMOS high speed standard VT process. Simulation result was obtained by using HSPICE tool. Table I shows the summary of comparator performance, in comparison with the designs in [3] and [5]. The new comparator dissipates only 371 µW at 7 GS/s. Fig.7, shows the output wave of comparator with 0.5 GHz analog input signal and clock frequency of 7 Gs/s. Fast Fourier transform (FFT) is performed to observe the dynamic characteristics of the comparator such as the effective number of bits (ENOB). Fig.6 illustrates FFT at input frequency of 500 MHZ and sampling rate of 7 Gs/s.

TABLE I
PERFORMANCE COMPARISON

Item	[3]	[5]	This work	This work	This work
Supply voltage	1 V	1.2 V	1 V	1.2 V	1.8 V
Sampling frequency	4 Gs/s	0.5 Gs/s	4.34 Gs/s	5.4 Gs/s	7 Gs/s
ENOB	4@fin=0.528G	3.5@fin=0.5G	5.1@fin=0.5G	5.3@fin=0.5G	4.83@fin=0.5G
Power consumption	3.6 mW	148 µW	216 µW	265 µW	371 µW
process	90 nm CMOS	130 nm CMOS	130 nm CMOS	130 nm CMOS	130 nm CMOS
year	2007	2007	2009	2009	2009

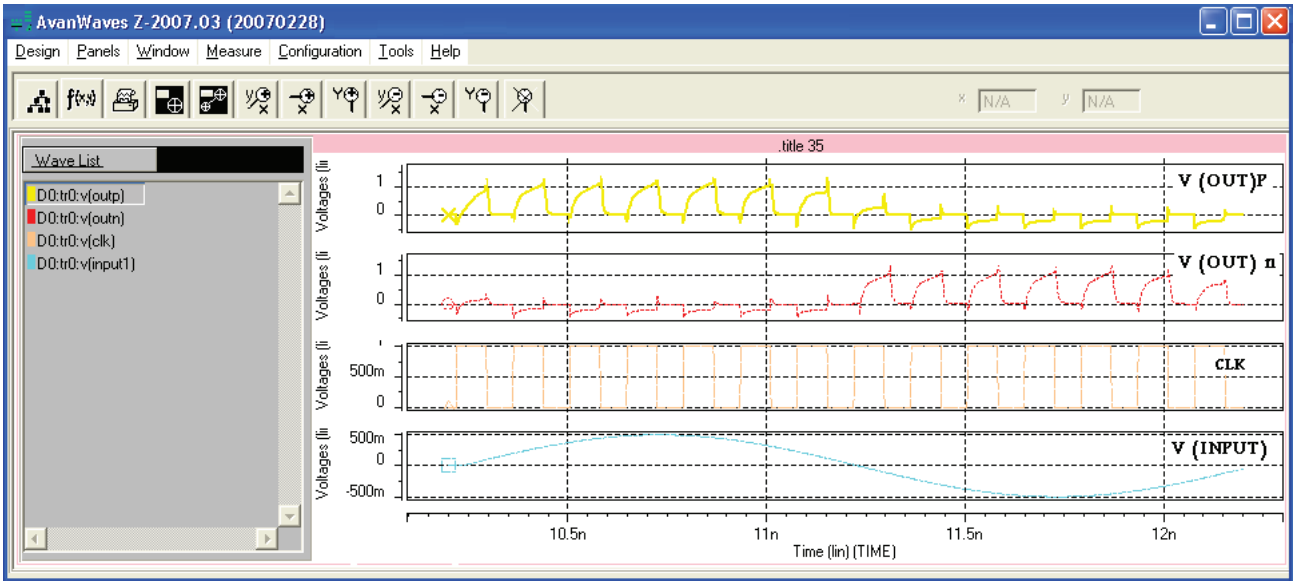

Fig.7 Output wave of comparator at Fin = 500 MGHz , Fclk = 7 Gs/s

V. CONCLUSION

In this paper, a 0.13 µm CMOS UWB comparator for high speed low power flash ADC is proposed. CMOS positive feedback and a new structure as output circuit are used to improve sampling rate and performance of comparator**.** The measured ENOB is 4.83 bits at 7 GS/s with a 500 MHz sine wave input signal.

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