A 2.2 GS/s 900 MHz Bandpass Delta-Sigma Modulator for Class-S power amplifier

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***Abstract* — A fourth-order bandpass delta-sigma modulator (BDSM) is designed for operating at decreased sampling frequency to relax the requirements of the power amplification stage in Class-S power amplifier. The modulator is fabricated in 0.25 um SiGe BiCMOS technology and achieves 43.8 dB signal-to-noise ratio (SNR) in 10 MHz bandwidth with sine wave input, while dissipating 380 mW from -2.8 V supply. For a WCDMA modulated signal the modulator demonstrates 3 % of EVM.**

***Index Terms* — bandpass ADC, sigma-delta modulation, continuous time, Class-S, power amplifiers, WCDMA**

I. Introduction

In modern telecommunication system, the peak-to-average ratio (PAR) of the transmitted signals is often more than tens dB. This aspect makes power amplifiers (PA) to work in substantial backoff from the compression point to avoid the signal peaks to experience significant distortion due to the PA non-linearity. Thus, power amplifiers with high linearity and high efficiency at several dB backoff are highly demanded at radio frequencies. At audio frequencies a switched-mode Class-S PA (Fig. 1) has been successfully used, incorporating very high efficiency (more than 80%) and excellent linearity, allowing to process audio signals that have usual PAR values up to 20 dB. Implementing the Class-S system at GHz input frequencies is a very attractive task.

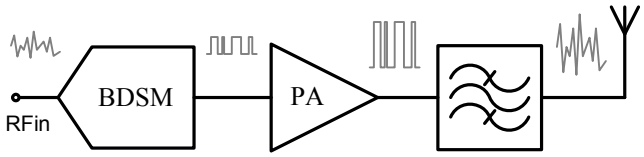

Fig. 1. Class-S BDSM-PA architecture

A Class-S system allows to process signals coded with non-constant envelope modulation schemes. Using a BDSM in a Class-S PA relaxes the requirements of the switching stage in contrast to the same PA that uses pulse-width modulation (PWM-PA). For a PWM-PA the pulses at the input of an amplification stage could be very short which requires very high f_T to process a modulated signal. For a BDSM-PA the minimum pulse length at the input of an amplifier is just one clock period, which is a substantially less demanding constraint on the f_T of the PA. Thus BDSM appears to be the architecture of choice for Class-S PAs at high clock rate.

Our previous BDSM [1] for 450 MHz carrier frequency and 2 GHz clock was based on very common fs/4 architecture [2]. The output data rate of the modulator is 2 Gb/s. This BDSM was successfully implemented in a Class-S PA system presented in [3]. The switch-mode amplifier was based on a GaN technology. The maximum possible data rate that can be processed by the GaN transistors is 2.2 Gb/s while maintaining needed power and efficiency. For a case of 450 MHz carrier the $f_S/4$ architecture was an acceptable solution. In order to design Class-S PA system at 900 MHz it is not possible anymore to use $f_S/4$ architecture for the BDSM, because output data rate is 3.6 Gb/s that is much higher than 2.2 Gb/s. This problem could be solved either by using of the power transistors with higher f_T or by reducing output data rate of the BDSM. The latter choice seems to be much easier than developing of new transistors. Similar modulator has already been done for the input frequency of 1.4 GHz and sampling frequency at 4 GHz [4]. In our work the carrier frequency is closer to the Nyquist frequency compared to [4].

This paper presents a design and measurement results of the delta-sigma modulator that operates at a reduced sampling frequency.

The paper is organized as follows in Section II the system design is described. Section III introduces circuit design and accounting for non-idealities. Section IV presents the experimental results while Section V provides the conclusions.

II. System Design

For the BDSM we have chosen 4th order LC architecture that incorporates two resonators. The design was started at system level by designing of a noise transfer function (NTF). The NTF was derived in a general form from the architecture proposed by [2] taking into account one clock delay due to the real quantizer circuit. The resonators were set to the carrier frequency while sampling frequency was 2.36 times higher. The NTF has been numerically optimized to have minimum in-band noise at the carrier frequency. Then applying impulse-invariant transformation described in [5], we obtained a continuous-time equivalent. The final CT architecture is

depicted in Fig. 2. This architecture uses three different pulse types, having three feedback coefficients to control NTF.

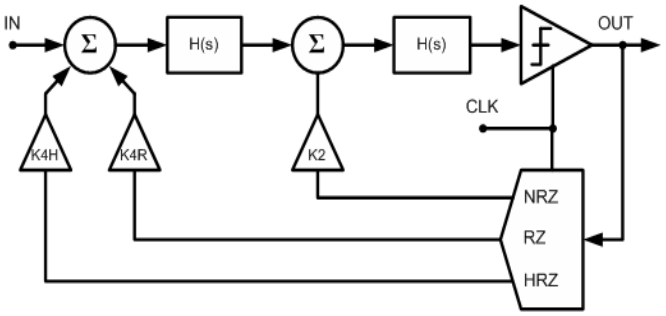

Fig. 2. Fourth order LC continuous-time BDSM architecture

On the system level the transfer function of a resonator is described by (1).

$$H(s) = \frac{As}{s^2 + \frac{\omega_0}{Q}s + \omega_0^2} \qquad (1)$$

where ω_0 is the center frequency, A – constant gain factor, Q – quality factor of the resonator. Having a very high quality factor will bring the transfer function (1) to a form of an ideal resonator.

For an estimation of parasitic effects, the resonator, comparator, and DACs were designed and modeled on the circuit level. The jitter, excess loop delay and finite quality factor of the resonator are the main non-idealities that affect the performance of a BDSM. For taking real effects into account the transfer function has been changed and a coefficient optimization was done to improve the performance of the modulator.

All simulations were done in Cadence environment, allowing simultaneous use of behavioral and transistor-based models. For the system-level design component blocks were described in Verilog-A. Transient analysis was performed by the Cadence Spectre simulator.

III. Circuit design

A fully differential circuit configuration was used to provide high common-mode noise rejection. All current sources were designed as CMOS circuits. This allows a low supply voltage without saturation of the transistors.

A. Resonator design

The complete resonator structure consists of two gm-cells and an LC tank, including varactors (Fig. 3*a*). To improve the dynamic range of the resonator a gm-cell was designed as a multi-tanh structure (Fig. 3*b*). The linearity of the gm-cell can be controlled to some extent by unbalancing the differential pairs and the emitter degeneration. Since the supply voltage was fixed to 2.8 V it is possible to use effectively only one

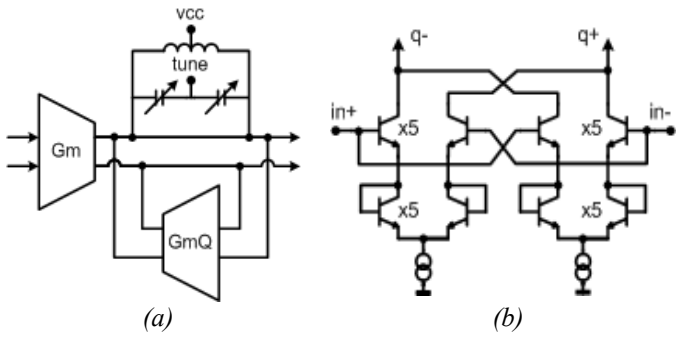

Fig. 3. (a) resonator sturcuture; (b) gm-cell schematic

diode in the emitter. So only the tail current and emitter area ratio between left side and right side transistors were optimized.

The LC tank includes a symmetrical octagonal inductor and varactors to cover frequency range around 900 MHz. The octagonal inductor has an inductance of 7.6 nH and consists of two thick layers connected in parallel in order to minimize resistive losses. Occupying an area of 320 x 320 um^2 the optimized coil has a quality factor of only 8.3 at 900 MHz. Since a low quality factor of the tank highly degrades an SNR it is necessary to compensate losses in the inductor. For this reason an additional gm-cell GmQ was connected as positive feedback (Fig. 3*a*). It is also based on the multi-tanh structure but uses four times bigger transistors and a 4-to-1 capacitive divider at the input. Both gm-cells have controlled currents to externally change gain and quality factor. The designed resonator has a maximum quality factor of 55.

B. Pulse generation circuits

A comparator was designed as a standard ECL master-slave latched circuit with preamplifier. After comparator the one-clock period delayed non-return-to-zero signal comes to the blocks that form return-to-zero (RZ) and hold-return-to-zero (HRZ) pulses (Fig. 4). This circuit is based on the comparator structure. The difference is that in the slave part the cross-coupled latch transistors are replaced with diode-connected transistors [6].

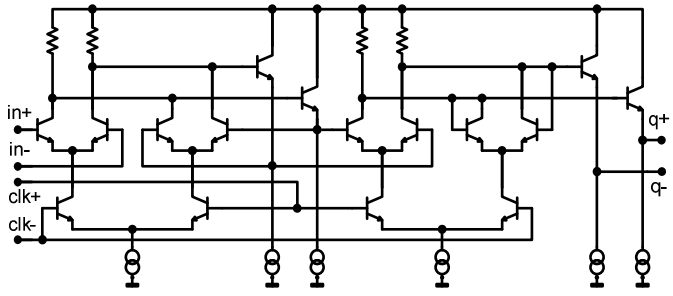

Fig. 4. Circuit for the forming of the RZ and HRZ pulses.

The circuit in Fig. 4 can form RZ pulses and, if clocked in anti-phase, HRZ pulses.

IV. Experimental results

The modulator was fabricated in a 0.25 um SiGe BiCMOS process (f_T=180GHz) with three thin and two thick metal layers [7]. Fig. 5 shows the microphotograph of the BDSM. The occupied area is 1.5 mm^2.

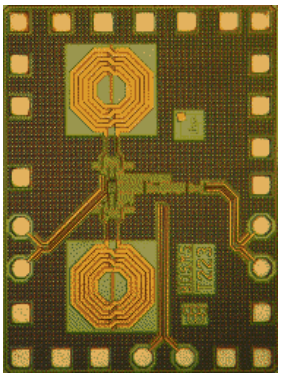

Fig. 5. Chip photo of the BDSM.

The BDSM consumes 136 mA current from -2.8 V supply voltage. The chip was mounted on the Rogers RO4003 printed circuit board with a thickness of 0.51 mm. There are more requirements that are important for the characterization of the BDSM that has to drive switch-mode amplifier. Next subsections describe the measurements of those parameters.

A. Signal to Noise Ratio

For a sine wave input we estimated the modulator performance by measuring the SNR in a 10 MHz bandwidth (Fig. 6). The output data have been captured from the oscilloscope controlled by Matlab and SNR values have been calculated.

A spectrum of the output signal calculated from the saved pulse train is shown in Fig. 7.

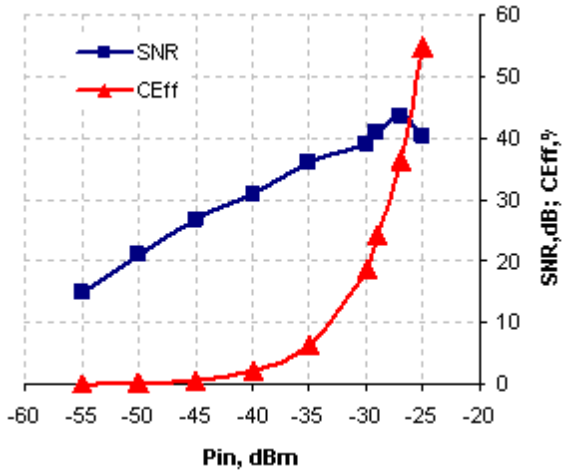

Fig. 6. Measured signal-to-noise ratio and coding efficiency for sine wave input signal at 890 MHz input frequency and 2.2 GHz clock. (SNR is measured in 10 MHz bandwidth)

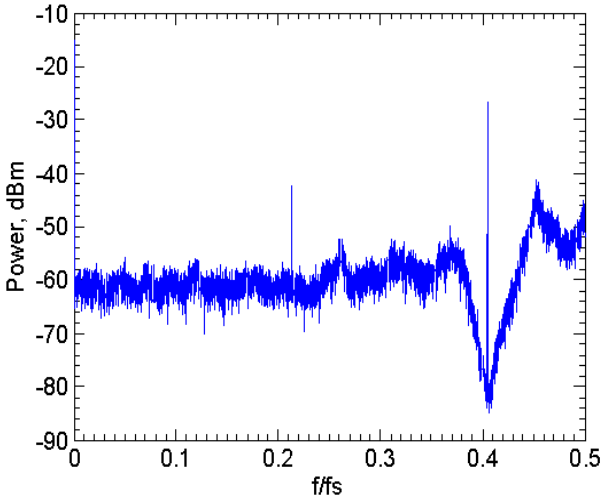

Fig. 7. Measured output spectrum of the BDSM at Pin = -30 dBm

B. Coding Efficiency

A parameter that shows how a modulator affects on the available power of the complete class-S amplifier is called coding efficiency. It is defined as the ratio of the reconstructed power by the bandpass filter to the total pulse train power and described by (2)

$$\eta_P = \frac{\text{mean signal power in pulse train}}{\text{total power in pulse train}} \qquad (2)$$

where the pulse train is assumed to be zero mean. The coding efficiency depends on the modulator architecture only [8].

For the developed modulator the coding efficiency curve vs. input power is shown in Fig. 6. The coding efficiency of 36.5% was measured at maximum SNR value.

C. Pulse width statistic

For the modulator, included in a class-S PA system the pulse widths in a pulse train have to be analysed. This caused by a low frequency dispersion effect in GaN amplification stage. For the switching mode operation, long pulses which are quite close to low frequency dispersion are amplified stronger what contributes to the kind of amplitude modulation effects and losses effect on the lower frequencies. Thus, the average pulse width in the pulse train has to be short enough to avoid this unwanted effect.

For the analysis of the pulse widths 16384 output data bits were saved and analysed. Fig. 8 shows the average pulse width for the designed modulator and for the modulator based on the fs/4 structure from [1]. The maximum average pulse width for the current design is lower than 1.5 x Ts = 0.68 ns, which is a good value taking into account that the low frequency dispersion effect for GaN transistors occurs if pulses are about 20 ns.

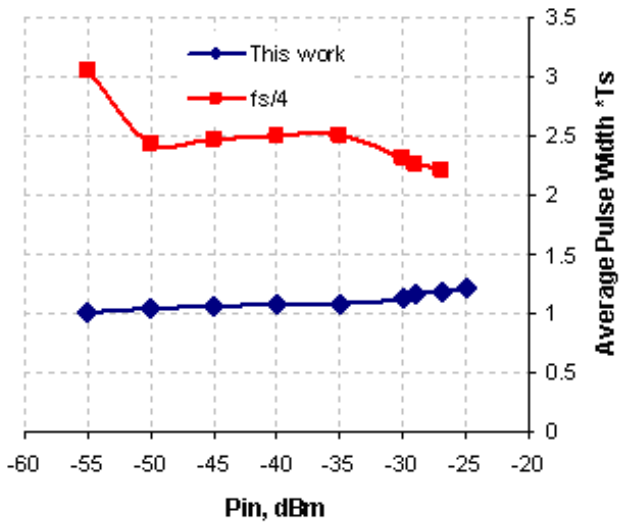

Fig. 8 Measured coding efficiency of the different modulators.

D. WCDMA input signal

To estimate how the BDSM can process realistic signals we have applied a CDMA signal corresponding to 1xEVDO communication standard. The signal occupies 1.23 MHz bandwidth at 920 MHz carrier. The peak-to-average ratio of a test signal was 9.5 dB. By using of Agilent ADS the WCDMA signal was generated and uploaded to an ESG4433C signal generator. The output signal was captured and analysed by the Agilent Vector Signal Analyzer and VSA Software. The measured EVM value was 3% at Pin =-27 dBm. The corresponding modulator output spectrum is shown in Fig. 9.

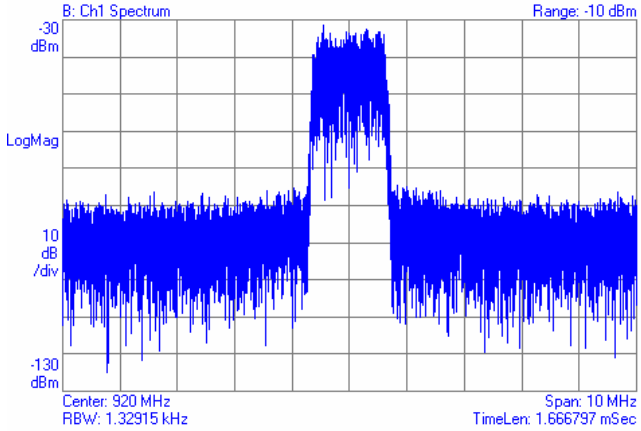

Fig. 9. Measured output spectrum of the BDSM applying WCDMA signal.

Table I summarizes the measured parameters for the designed delta-sigma modulator.

TABLE I
BDSM PERFORMANCE SUMMARY

Process	0.25 um SiGe BiCMOS
Notch frequency range	880..920 MHz
Sampling frequency	2.2 GHz
Supply Voltage	-2.8 V
Power Consumption	380 mW
Output swing, diff	0.8 V
Chip area	1.5 mm^2
SNR_{MAX} BW = 10 MHz	43.8 dB
CEff at SNR_{MAX}	36.5%
EVM at PAR = 9.5 dB	3%

V. CONCLUSION

We have presented the design and measurement results of a LC continuous-time BDSM with decreased sampling frequency for a Class-S power amplifier. The modulator clocked at 2.2 GHz has a tuned notch at 900 MHz frequency. The successfully integrated and measured BDSM has demonstrated the ability to act as an input driver in a Class-S power amplifier system for WCDMA signals, relaxing the requirements of the amplification stage. To the authors' knowledge this is the first BDSM operating with decreased sampling frequency while having a high frequency input very close to the Nyquist frequency.

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