Real-time Polarization Division Multiplexed Coherent Optical OFDM Receiver at 9.83-GS/s for 28.6-Gb/s Single-band Intradyne Detection

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Abstract: Real-time polarization division multiplexed coherent optical OFDM receiver is demonstrated to receive 28.6-Gb/s data per optical wavelength in single intradyne detection. QPSK modulated sub-carriers are detected using 9.83-GS/s ADCs and DSP implemented on three FPGAs.

OCIS codes: (060.1660) Coherent communications; (060.4510) Optical communications

1. Introduction

Coherent optical OFDM (CO-OFDM) is a promising next generation data format for high speed and high capacity optical data transmission due to its inherent advantage of simplicity in digital signal processing (DSP) algorithms and network scalability in superchannel configuration. It is thus desirable to study the precise requirement and potential issues of real-time DSP needs and algorithms of CO-OFDM. Over the past few years a number of results on real-time CO-OFDM transmitters and receivers were reported [1-3] , but the highest sampling rate for a CO-OFDM receiver demonstration so far was 3.4-GS/s [3] and a total data rate per single OFDM band of 12.1-Gb/s using 16-QAM was reported [3] but with shared light sources between transmit and receive lasers.

In this paper, we demonstrate the implementation of a real-time field programmable gate array (FPGA)-based receiver for polarization-multiplexed CO-OFDM transmission and intradyne detection. 9.83-GS/s ADCs are used to sample the data in dual polarization and DSPs are implemented on multiple FPGAs to detect QPSK modulated Polarization division multiplexed (PDM)-CO-OFDM signals totaling 28.6-Gb/s of data per CO-OFDM band.

2. Experimental setup

The setup of the 28.6-Gbit/s CO-OFDM transmission system is shown in Fig. 1. At the transmitter, an OFDM frame is constructed as shown in Fig.2 where OFDM symbol synchronization patterns and pilot symbols are followed by OFDM payload data that consists of pilot subcarriers. A payload data stream is pseudo-random bit sequences (PRBS) of length 2^{15}-1 and is mapped to 107-OFDM subcarriers with QPSK constellations. The frequency domain data is pre-emphasized to compensate for the excess low pass filtering of the transceiver front-ends including digital to analog converters (DAC) and analog to digital converter (ADC). The data is then extended by 8-pilot subcarriers, before it is converted to time domain data by 128-point Inverse Fast Fourier Transform (IFFT) with 16-point cyclic extension (1/8 of the FFT-point), all by offline processing. The computer generated time-domain data stored in an arbitrary waveform generator (AWG) is continuously applied to an I/Q modulator at a sampling rate of 9.83-GS/s. A

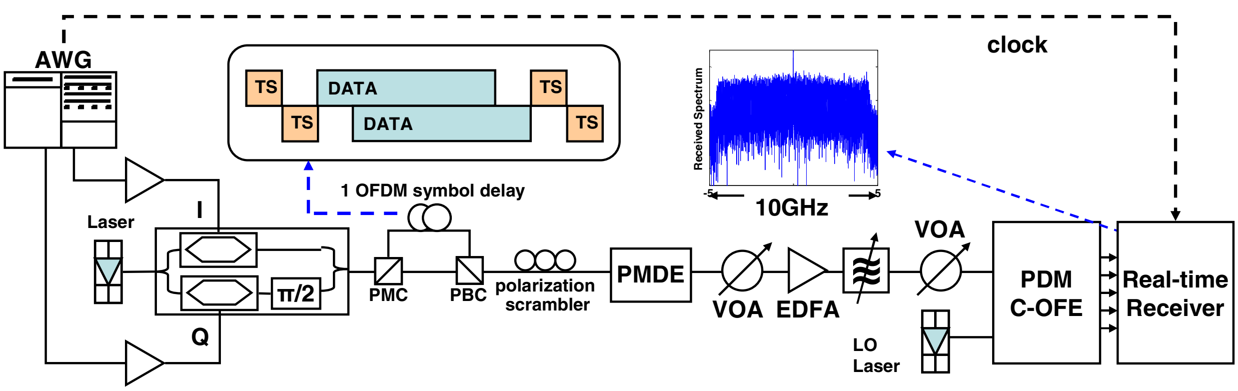

Fig. 1: Polarization-multiplexed CO-OFDM transmission system. Inlet shows illustration of PDM-OFDM data structure.

tunable external cavity laser (ECL) with specified linewidth of 100-kHz is used as a transmitter light source. PDM is achieved by splitting the modulator output using a polarization maintained coupler, delaying one branch by exactly one OFDM symbol length (144 samples), and recombining the two branches in a polarization beam combiner.

The transmitter output signal is passed through a 3-stage polarization scrambler (Agilent 11896A), followed by a polarization mode dispersion emulator to control the differential group delay (DGD) of the transmission test. A variable optical attenuator and an erbium doped fiber amplifier are used to control the received signal-to-noise ratio. At the opto-electronic receiver frontend, the signal is combined with a local oscillator (LO) laser in a polarization diversity coherent optical-front-end (PDM C-OFE) where two 90-degree optical hybrids and 4 balanced photodiodes with transimpedance amplifiers are integrated in the same package. The LO is the same model of ECL used at the transmitter, and is tuned within approximately ±50 MHz of the received signal's wavelength. The outputs of the PDM C-OFE are fed to the 4 individual ADCs. The ADCs sample the input signals with 9.83-Gs/s at a nominal resolution of 8 bits. The receiver clock is driven from a common clock source with the transmitter clock in this measurement. The receiver frontend has a measured 3-dB bandwidth of approximately 3-GHz. The 8-bit outputs of two ADCs of each polarization are interfaced with a Xilinx Virtex 5 FPGA but only 6-bit are used for the first stage of DSP, namely symbol synchronization, carrier frequency compensation and FFT. The two FPGAs then pass their data to a third identical FPGA, in which the second stage of DSP, namely channel equalization, carrier phase compensation as well as symbol decision and bit error counting are performed. The 3 FPGAs are connected to a personal computer (PC), which calculates the BER and provides a user interface to the receiver.

3. Real-time digital signal processing for CO-OFDM receiver

The FPGAs operate with a core clock frequency of 153.6 MHz which is 1/64 of ADC sampling rate, as parallelization of 64 channels are required in the FGPAs to process the received samples near 10-GS/s. As the DSP resource requirement for 64-parallel channels processing of 28.6-Gb/s PDM-CO-OFDM far exceeds the capacity of a single Virtex 5 FPGA, the functionality needs to be split into multiple FPGAs as shown in Fig. 3. FPGA1 and 2 receive the polarization multiplexed signals and process frame/symbol synchronization, frequency estimation and FFT. Those functionalities are all done in parallel processes as opposed to previously reported serial processing [2] for more hardware efficient implementation. Frame synchronization and frequency estimation are in principle based on auto-correlation [4] but are modified to achieve a more hardware efficient implementation in parallel processing. Hardware efficient parallel FFT is internally developed without sacrificing much resolution. Our FFT nominally uses 8-bit resolution though it is internally allowed to grow up to 12-bit resolution. It is highly desirable to achieve

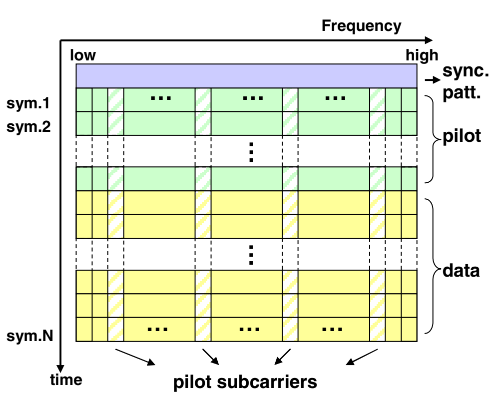

Fig. 2: CO-OFDM frame construction

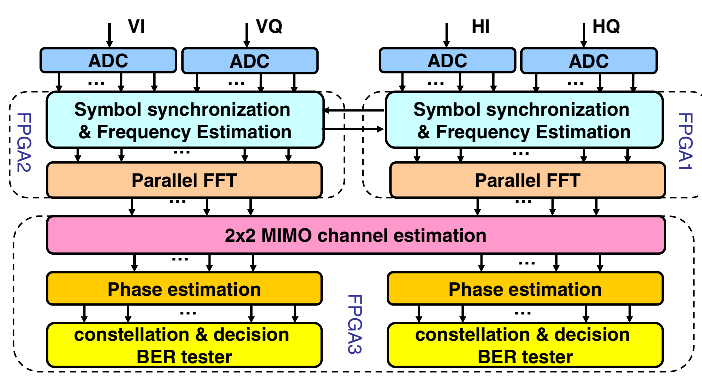

Fig. 3: PDM CO-OFDM receiver digital signal processing diagram.

all functionalities in one device, as many signal processing blocks are dependent on one another. Special attention needs to be paid to operate multiple devices in a bit-accurate manner. Maximum 6.4-Gb/s of communication channels are prepared between FPGA-1 and 2, and between 2 autocorrelations taken at FPGA-1 and -2, the stronger autocorrelation is chosen for carrier frequency estimation and compensation.

FPGA-3 does the rest of the signal processing, namely channel equalization and carrier phase recovery. Channel equalization is done in a data-aided feed forward equalization with polarization interleaved training symbols [5]. The carrier phase recovery uses data-aided feed forward compensation with pilot subcarriers [2]. Although OFDM channel estimation is much less resource intensive than the counterpart of single carrier detection [6], in order to save 50-% of the multipliers required at each polarization output of the Jones matrix inversion operation, we monitor BER of only one polarization channel at the same time. The decision making for the received QPSK constellations is done across the zeros of real and imaginary parts and the errors are counted real-time by comparing the recovered binary sequence against a stored binary sequence of the PRBS pattern in the FPGA's on-chip memory.

4. Measurement results

As OFDM signals are transmitted in frames, the measurement is not free of frame loss. There can be multiple causes for the frame loss. Such elevated errors can stem from inaccurate frequency estimation together with time-domain channel estimation's sensitivity to residual carrier frequency offset. After removing such frame losses, the bit error rate is measured against OSNR over 32 frames in which each frame consists of 2,500 OFDM symbols. The results are plotted in Fig. 4 for the measurements on the averaged 2 polarization channels with and without DGD. The polarization scrambler is turned on for all measurements and set to the fastest polarization speed available. The polarization scrambling does not affect BER indicating the adequate frequency of training symbol insertion for channel estimation. In the experiment with or without DGD, the BER floor is observed around 10^{-5}. This can be caused by multiple issues such as signal clipping due to saturation, the limited resolution of the DSP and the reduced SNR for the highest frequency subcarriers due to the reduced effective number of bit (ENOB) of both DAC and ADC at frequencies above 3-GHz. For comparison, real-time homodyne measurement with 102-subcarriers, thus reducing data rate to 25-Gb/s is conducted and the lower error floor of 10^{-6} is observed. Fig. 5 shows the measured carrier frequency offset that moves more than 5-MHz in the time span of less than 0.1-ms emphasizing the importance of DSP carrier frequency recovery in CO-OFDM intradyne detection.

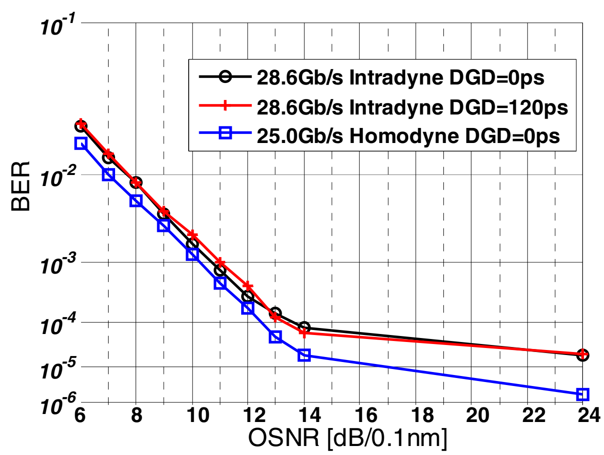

Fig. 4: BER vs. OSNR of CO-OFDM receivers for 28.6-Gb/s Intradyne detection and 25.0-Gb/s Homodyne detection.

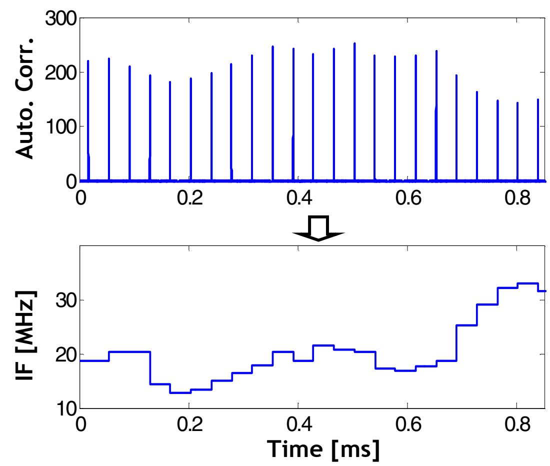

Fig. 5: Measured autocorrelation and frequency offset in a real-time DSP.

4. Summary

We have implemented a 9.83-GS/s real-time FPGA-based CO-OFDM intradyne receiver for optical PDM transmission. The data rate of 28.6-Gbit/s is achieved after subtraction of training symbols and pilot subcarriers, utilizing about 73-% of Nyquist frequency for dual polarization data transmission of QPSK modulated OFDM signals. This data rate is the highest data rate reported so far for a CO-OFDM single-band detection. The minimum BER is 2×10^{-5}, and the required OSNR of ~11dB for a BER of 1×10^{-3} is achieved.

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5. References

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