Evaluation of a Fast Pulse Sampling Module With Switched-Capacitor Arrays

Jinhong Wang, Lei Zhao, Changqing Feng, Shubin Liu, and Qi An

***Abstract*—We introduce a fast pulse sampling module with the use of switched-capacitor arrays (SCAs). The module is in the size of 3U for PCI extensions for Instrumentations (PXI), and there are a total of six channels with a sampling rate of up to 5 giga samples per second (GS/s) per channel. With this module, we evaluate the issues of fast pulse timing from reconstructed waveform, as well as the scheme of interleaved sampling between adjacent channels within the module. The timing precision of this module is proved to be below 10 ps RMS at 4.7 GS/s after a series of calibration strategies. We have also achieved 9.4 GS/s with two channels interleaved on board.**

***Index Terms*—Analog-to-digital conversion (ADC), signal sampling, switched-capacitor circuits, timing.**

I. Introduction

WAVEFORM digitization with the use of switched-capacitor arrays has been proved to be a promising technique in some fields of the physics experiments [1]–[9]. The detector signals are first sampled and stored in an array of analog capacitors at a high rate (in gigahertz range), then read out and digitized with a commercial analog-to-digital converter (ADC) at a relatively lower rate (e.g., several megahertz) before a new pulse is acquired. As a result, it is possible to achieve both high sampling rate and high analog-to-digital conversion precision at the cost of increased dead time [10].

Up to the present, several application specific integrated circuits (ASICs) of switched-capacitor arrays (SCAs) for high-energy physics experiments have been developed. Some representatives are listed as follows. In 2006, Delagnes *et al.* reported a swift analog memory (SAM) ASIC with two channels and a sampling rate of up to 2 giga samples per second (GS/s) [8]. In 2007, Varner *et al.* presented a large analog bandwidth recorder and digitizer with ordered readout (LABRADOR) ASIC featuring nine channels and a maximum sampling rate of 3.7 GS/s [11]. In 2008, Varner and his group advanced their work with the first version of the buffered large analog bandwidth (BLAB1) ASIC based upon the lessons learned from the development of LABRADOR ASIC [12]. Meanwhile, a series of Domino Ring Sampler (DRS) were developed at the Paul Scherrer Institute (PSI), Switzerland. In 2009, Ritt reported the fourth version of the Domino Ring Sampler (DRS4), which is a nine-channel ASIC with a maximum sampling rate of up to 6 GS/s [13]. It is pointed out in [14] that timing precision from the pulse sampling gives the best precision compared to the signal processing techniques of leading edge discriminators, constant fraction discriminators, and multiple threshold discriminators. Up to the present, capabilities of sub-10-ps timing precision of the digitizing modules with SAM and BLAB1 have been reported [15], [16].

In this paper, we present a compact fast pulse sampling module with DRS4. We evaluate the timing performance of the module from sampled waveforms, as well as the scheme of interleaved sampling of the analog channels. We arrange the paper as follows. In Section II, we introduce the setup of the fast pulse sampling module. In Section III, we present the methodology of the signal processing in this paper, including calibration of dc offset and uneven sampling intervals, digital processing of waveform timing, and the consideration of interleaved sampling. In Section IV, we show the performance of the module from test. We discuss some of the issues concerning the module in Section V. Finally, in Section VI, we conclude this paper and summarize what we have achieved.

II. Setup of the Fast Pulse Sampling Module

We built the fast pulse sampling module in consideration of modular instrumentation and separated it into a mother board and a daughter board. The mother board is in the size of PXI-3U, and it is mainly accountable for control of the fast pulse sampling module and data acquisition from the daughter board. The daughter board is attached to the mother board through an 80-pin dual-row slim stack connector from *Molex* [17] and is responsible for both waveform sampling and digitization.

Fig. 1 is a simplified diagram of the whole hardware setup of the module, in which Fig. 1(a) shows the block diagram of the mother board, and Fig. 1(b) illustrates that of the daughter board. In Fig. 1(a), a piece of CPLD from the Altera MAXII family (*EPM2210*) [18] is used to interface the mother board to the PXI bus with PCI *MegaCore* [19]. The CPLD also takes charge of receipt of external triggers (External Trigger) and transmission of discriminated triggers to the daughter board through control lines (Control) for waveform selection. Selected waveforms are

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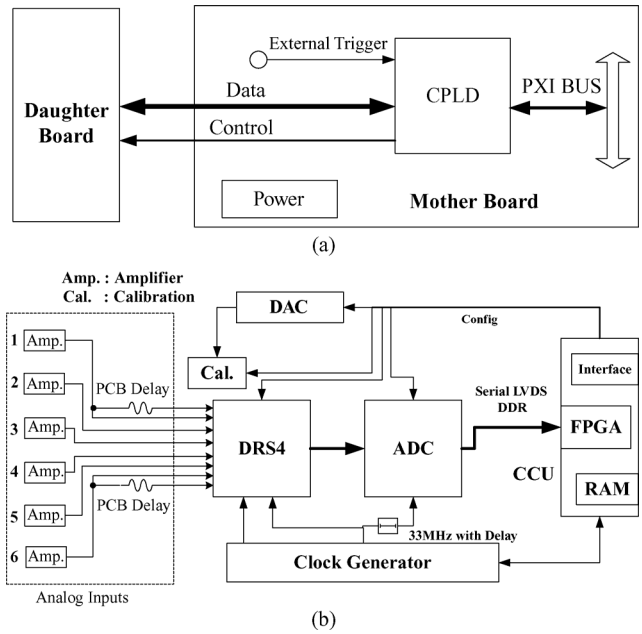

Fig. 1. Setup of the fast pulse sampling module, in which (a) and (b) show the block diagrams of the mother board and the daughter board, respectively.

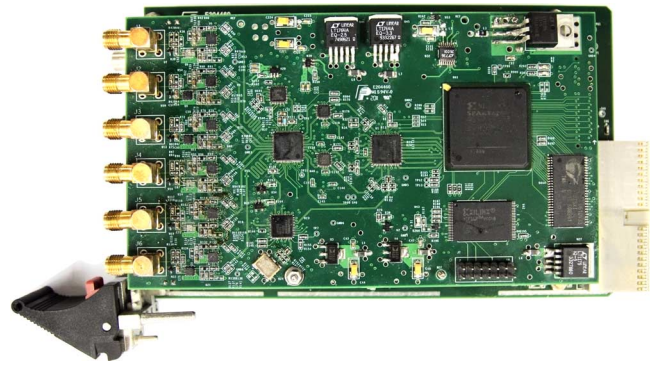

Fig. 2. Photograph of the fast pulse sampling module.

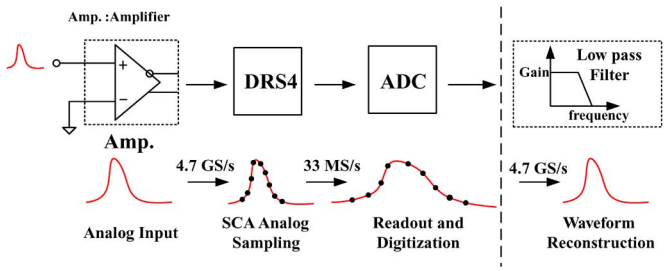

Fig. 3. Signal flow of the fast pulse sampling module.

packaged on the mother board and then transmitted to the upper-layer controller via the PXI interface.

There are a total of six channels on the daughter board, as shown in Fig. 1(b), in which two of them (1 and 6) are interleaved with delays on the printed circuit board (PCB) to two adjacent analog channels of DRS4, respectively. Anytime a hit arrives, DRS4 samples it and stores the charge in arrays of switched capacitors. The stored charges are then read out sequentially to the ADC for digitization at the speed of 33 MHz for the optimal linearity [20]. The input dynamic range of DRS4 is reported as high as 69 dB [20]. In our evaluation, we chose a 14-bit ADC from Analog Devices (*AD9252*) [21] to cover the dynamic range. A low-end field programmable gate array (FPGA) from Xilinx Spartan-3 family (*XC3S5000*) [22] is adopted as the central control unit (CCU). It is responsible for reception of ADC outputs, control of the daughter board, and communication to the mother board. Other features such as on-board calibration (Cal.) are also considered in the module. A 16-bit digital-to-analog converter (DAC) from Linear Technology Corporation (*LT2600*) [23] provides high-precision voltage levels for calibration unit (Cal.) as well as references or bias for other ICs. Fig. 2 is a photograph of the fast pulse sampling module.

III. Signal Processing Algorithms

In this section, we first analyze the noise inherent in the readout waveform, and then introduce techniques for calibration of the uneven sampling intervals and algorithms of waveform timing. Finally, we give our considerations of the signal processing of interleaved sampling.

A. Analysis of the Inherent Noise

The signal flow of the fast pulse sampling module is shown in Fig. 3. The input is first sampled and stored in capacitors (DRS4), then read out for digitization. Moreover, the analog sampling rate is comparatively high (e.g., 4.7 GS/s) with respect to the speed of readout and digitization (33 MHz). The two processes in combination are similar to that of a time-stretched analog-to-digital conversion [24]. Any noise picked up during the digitization will be multiplied by hundreds of times in the frequency spectrum of the reconstructed waveform, e.g., for 4.7 GS/s, a 10-MHz noise picked up in the readout and digitization process will correspond to a noise above 1 GHz in the spectrum. It is essential to remove these noises in the reconstructed waveform for better signal-to-noise ratio (SNR). In our evaluation, we suppress the noise in the sampled waveform with a digital low-pass filter before our signal processing algorithms. The stopband of the filter is set to be around the -3 dB bandwidth of the analog inputs to reject the noise beyond the signal band of interest.

B. Variation of Sampling Intervals

The variation of the sampling intervals of DRS4 mainly comes from the nonuniform tap delay in the domino chain. Internal phase-lock loop (PLL) of DRS4 compares the state of a probe from the domino wave to a reference clock and feeds back a voltage to stabilize the domino wave. The probe toggles its state every 1024 domino clock cycles, thus there may be variations within the 1024 sampling taps due to the variation of the IC process. It is necessary to find out the variation and compensate the waveform samples at their corresponding time stamps for better linearity.

We use the zero-crossing method to determine the uneven sampling intervals. The principle of this method is to sample a sine wave uncorrelated to the sampling clock and find the

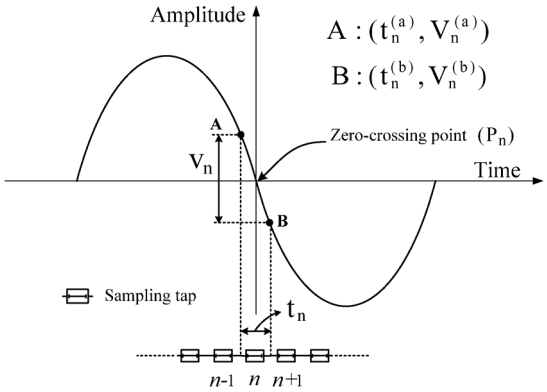

Fig. 4. Zero-crossing point of a sine wave.

zero-crossing points of the waveform. Suppose a sine input as a function of time (t) is

$$V = V_0 \times \sin(\omega t + \varphi). \tag{1}$$

In (1), V_0, ω, and φ are the amplitude, angular frequency, and phase, respectively. The fast pulse sampling module records the sinusoid, and the zero-crossing points (P_n) associated with sampling tap $n (n = 1 \ldots 1024)$ are derived from the waveform, as in Fig. 4. A $(t_n^{(\mathrm{a})}, V_n^{(\mathrm{a})})$ and B $(t_n^{(\mathrm{b})}, V_n^{(\mathrm{b})})$ are two adjacent samples across tap n, in which e.g., $(t_n^{(\mathrm{a})}, V_n^{(\mathrm{a})})$ is the time and amplitude coordinate of A. We use (a) and (b) in the superscript to distinguish the same parameter in A and B. From (1), the vertical interval (V_n) of A and B at the zero-crossing point is approximately

$$V_n \approx V_0 \omega t_n. \tag{2}$$

In (2), $t_n = |t_n^{(\mathrm{b})} - t_n^{(\mathrm{a})}|$, $V_n = |V_n^{(\mathrm{b})} - V_n^{(\mathrm{a})}|$, where the operator $|x|$ gives the absolute value of x.

The sine wave is phase-free to the domino clock, thus its zero-crossing points are considered to have identical probability to be distributed to all the sampling taps. We collect the zero-crossing points at each tap and calculate the amplitudes across tap n $(V_{n(1)}, V_{n(2)}, \ldots, V_{n(N)})$ according to (2), in which $V_{n(i)}$ $(i = 1 \ldots N)$ is the amplitude (V_n) of the ith measurement in a total of N trials for tap n. The final amplitude interval at tap $n(\widetilde{V}_n)$ is obtained by making an average of $V_{n(i)}$ $(i = 1, \ldots N)$. The proportion $\widetilde{V}_n/t_n$ is the same at all the sampling taps for a fixed sine input. We derive the sampling intervals as follows:

$$\begin{aligned} &\frac{\widetilde{V}_n}{t_n} = \frac{\widetilde{V}_m}{t_m} \qquad n, m = 1, 2 \ldots 1024; n \neq m \\ &\sum_{n=1}^{1024} t_n = 1024 \times T_{\mathrm{s}}. \end{aligned} \tag{3}$$

In (3), T_{s} is the average period of the sampling clock. From (3), the sampling interval t_n is derived as

$$t_n = \frac{\widetilde{V}_n}{\sum_{j=1}^{1024} \widetilde{V}_j} \times 1024 \times T_{\mathrm{s}}. \tag{4}$$

C. Digital Solution for Pulse Intervals

We evaluate the timing performance of the module with a cable delay test. The RMS timing precision of the module is reflected from the precision of pulse intervals derived from their waveforms. There are several digital techniques to process the arrival time of pulses, including leading edge time discrimination with one or multiple thresholds, digital constant fraction zero crossing, and pulse shape fitting. A good introduction and comparison of them is given in [14] and [25]. We will adopt digital constant fraction zero crossing and pulse shape fitting algorithms in view of their advantages in timing precision.

Digital constant fraction zero crossing is an analog of the analog constant-fraction discrimination zero-crossing technique. Suppose the input is $V_{\mathrm{in}} = A \times f(t)$, in which A is the amplitude, and $f(t)$ represents the unitary function of an arbitrary pulse. We process the arrival time of V_{in} by transforming it to a bipolar signal and find its zero-crossing time. The primary steps of signal processing are as follows.

1) Create a delayed copy (V_{delay}) of the input from the pulse samples: $V_{\mathrm{delay}} = A \times f(t - \tau_{\mathrm{d}})$, in which τ_{d} is the delay.
2) Digitally amplify the input to obtain (V_{gain}): $V_{\mathrm{gain}} = p \times A \times f(t)$, in which p is the digital gain.
3) Invert V_{gain} and add it to V_{delay} to build a new pulse V_{zc}: $V_{\mathrm{zc}} = A \times f(t - \tau_{\mathrm{d}}) - A \times p \times f(t)$.
4) Optimize the delay (τ_{d}) and the digital gain (p) to transform V_{zc} to a bipolar signal, and find the zero-crossing time of $V_{\mathrm{zc}}(t_{\mathrm{zc}})$, i.e., the solution to $V_{\mathrm{zc}} = 0$, $f(t_{\mathrm{zc}} - \tau_{\mathrm{d}}) - p \times f(t_{\mathrm{zc}}) = 0$.

The zero-crossing time of the bipolar pulse corresponds to a constant fraction of the amplitude of input. In the above steps, the baseline is removed before the signal processing.

Pulse shape fitting reconstructs the waveform from samples according to a template, e.g., the average waveform, and gives the arrival time from the characteristics of the fitting. We will fit the leading edges of the pulses with elementary functions as Gaussian function or polynomial function, and simply derive their arrival time at the crossing time of a constant threshold.

D. Consideration of Interleaved Sampling

Time-interleaved sampling is one of the most promising approaches in practice to achieve higher sampling rate beyond that of the device itself. In the field of analog-to-digital conversions, this is done by recording the input signal alternatively with M phase-shifted clocks in M parallel channels and reconstructing the waveform by merging the sampled points of M channels into a single channel. In this way, it is possible to increase the sampling rate by M times.

It is impossible to achieve interleaved sampling with phase-shifted sampling clocks in our module since the eight channels of DRS4 share the same sampling clock. However, we can interleave the analog inputs of DRS4 [13], as with channel 1 and 6 shown in Fig. 1(b). The input is split into two channels of DRS4 with additional routing delay in one channel on the printed circuit board. The routing delay is controlled to be around half the sampling period to achieve uniform interleaving, e.g., for 5 GS/s, the delay is set to be 100 ps.

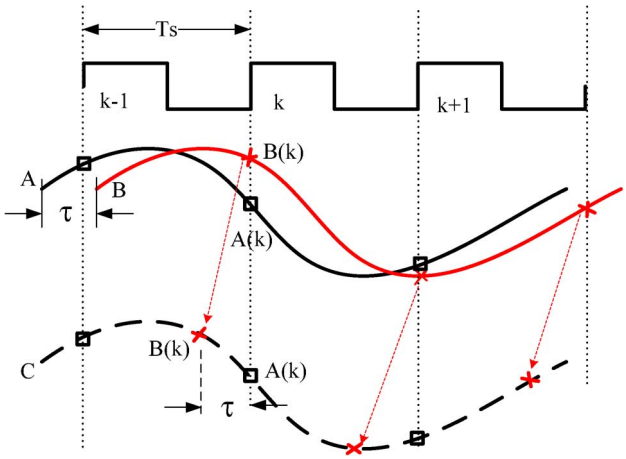

Fig. 5. Simplified illustration of the waveform reconstruction in the interleaved sampling channels.

In actual implementation, we first estimate the routing delay per inch on the PCB with the help of PCB layout tools, or multiple dielectric controlled impedance design systems such as *Polar Si8000* [26], then control the length of the routing lines carefully in the PCB layout according to the estimation. The actual delay between the two channels (τ) may vary from the preassigned value due to the variation of the PCB manufacturing process and that of input delay inside DRS4. We can calculate the delay in precision and compensate the time variation during waveform reconstruction. In Fig. 5, the module records the input of one channel (A) and its delayed copy (B) simultaneously. The samples in B $[\mathrm{B}(k), k \times T_\mathrm{s}]$ are τ earlier than their counterparts in A $[\mathrm{A}(k), k \times T_\mathrm{s}]$ when viewed from the reconstructed waveform, such as C in Fig. 5. We arrange the samples in C with respect to their time sequence, i.e., $\{\ldots, [\mathrm{B}(k), k \times T_\mathrm{s} - \tau], [\mathrm{A}(k), k \times T_\mathrm{s}], \ldots\}, k = 1, 2, \ldots$. The samples in C can be interpolated to be uniformly spaced in time.

IV. Performance of the Module

In this section, we present tests of the fast pulse sampling module, including calibration of variations of dc offset and nonuniform sampling intervals, performance of waveform timing, as well as interleaved sampling. We begin this section with the construction of the low-pass filter.

A. Construction of the Low-Pass Filter

The analog bandwidth of DRS4 is as high as 950 MHz [20], however it will drop dramatically without a proper arrangement of input driving circuits for the heavy capacitive load at its input (∼11 pF). In the module, we drive the analog input with a fully differential amplifier *THS4508* from Texas Instruments [27]. The analog bandwidth achieved is about 600 MHz for the channels without interleaved sampling scheme (normal channels: channel 2–5), as shown in Fig. 6. For the channels with interleaved sampling (channels 1, 6), the analog bandwidth is slightly higher than one half of 600 MHz (about 360 MHz)

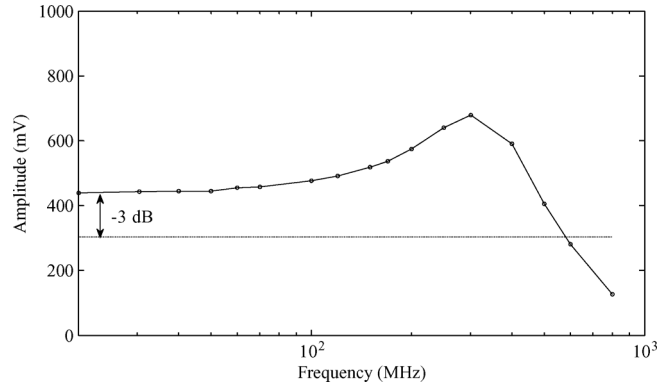

Fig. 6. Frequency response of one sampling channel in the module.

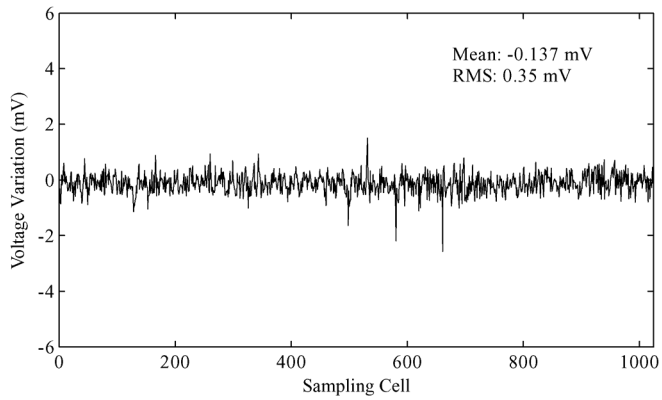

Fig. 7. 0-V dc voltage recorded by the 1024 sampling capacitors of one channel after dc offset calibration.

since the total capacitive load is about twice that of the normal channels.

In the test, we remove the noise beyond the analog bandwidth of the module with a low-pass finite-impulse response (FIR) filter. The filter is constructed with FDATool in MATLAB [28]. The stopband of the filter is about 600 MHz, and its magnitude attenuation in the stopband is 40 dB. In the following evaluation, we will process the waveform with this filter.

B. Calibration of DC Offset Variation

The dc offsets of the sampling channels are the residual voltage in the sampling capacitors of DRS4 due to the variation of the IC manufacturing process. We can characterize the offset of each sampling capacitor via dc offset test [29] and remove them from the readout voltage.

In the test, we input a high-precision reference voltage generated from the DAC to the analog channels of DRS4. The sampling capacitors record the voltage, and their offsets are evaluated from the differences of the sampled voltage to that generated from the DAC. We performed the test for all the channels of the module, and a typical result of the 0-V dc voltage recorded in one channel after calibration is shown in Fig. 7. The voltage variation of the 1024 sampling capacitors after dc offset calibration is about 0.35 mV RMS for 1-V peak-to-peak input. Meanwhile, we also characterize the noise voltage within one sampling capacitor, and typical distribution of the noise level

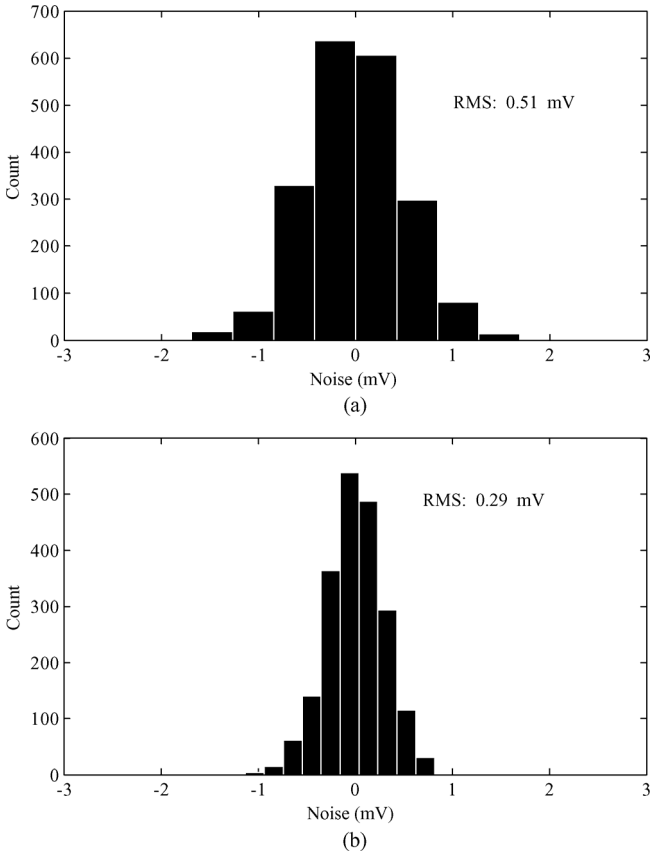

Fig. 8. DC noise level in one sampling capacitor, in which (b) is the low-pass filtered version of (a).

is shown in Fig. 8. Fig. 8(a) shows the noise level in one sampling capacitor without low-pass filtering, whereas Fig. 8(b) illustrates that after low-pass filtering. The noise level is reduced from 0.51 [Fig. 8(a)] to about 0.29 mV RMS [Fig. 8(b)] after filtering out the noise above the analog bandwidth.

C. Sampling Intervals of DRS4

In the test, a 100-MHz sine wave from the RS SMA 100-A signal generator [30] is induced to the fast pulse sampling module. The sinusoid was recorded at 4.7 GS/s, and its waveform was compensated for dc offset variation and filtered of high-frequency noise before applying the algorithms in Section III-B. Fig. 9 shows the sampling intervals derived at 4.7 GS/s, where Fig. 9(a) plots the time intervals of the 1024 taps, Fig. 9(b) illustrates their time distribution, and Fig. 9(c) depicts the nonlinearities (differential nonlinearity and integral nonlinearity). The average sampling interval is about 213 ps at 4.7 GS/s, and its standard deviation is about 4.9 ps RMS. The differential nonlinearity of the sampling intervals is in the range (−19 ps, 17.6 ps), whereas its integral nonlinearity is among (−68 ps, 344.7 ps).

The nonlinearity here is systematic and inherent in the architecture of the domino ring. We can partly compensate the deviations to reduce noise in the sampled waveform.

D. Evaluation of Waveform Timing Precision

We use the cable delay of fast pulses to evaluate the precision of waveform timing. In the evaluation, a fast pulse that is

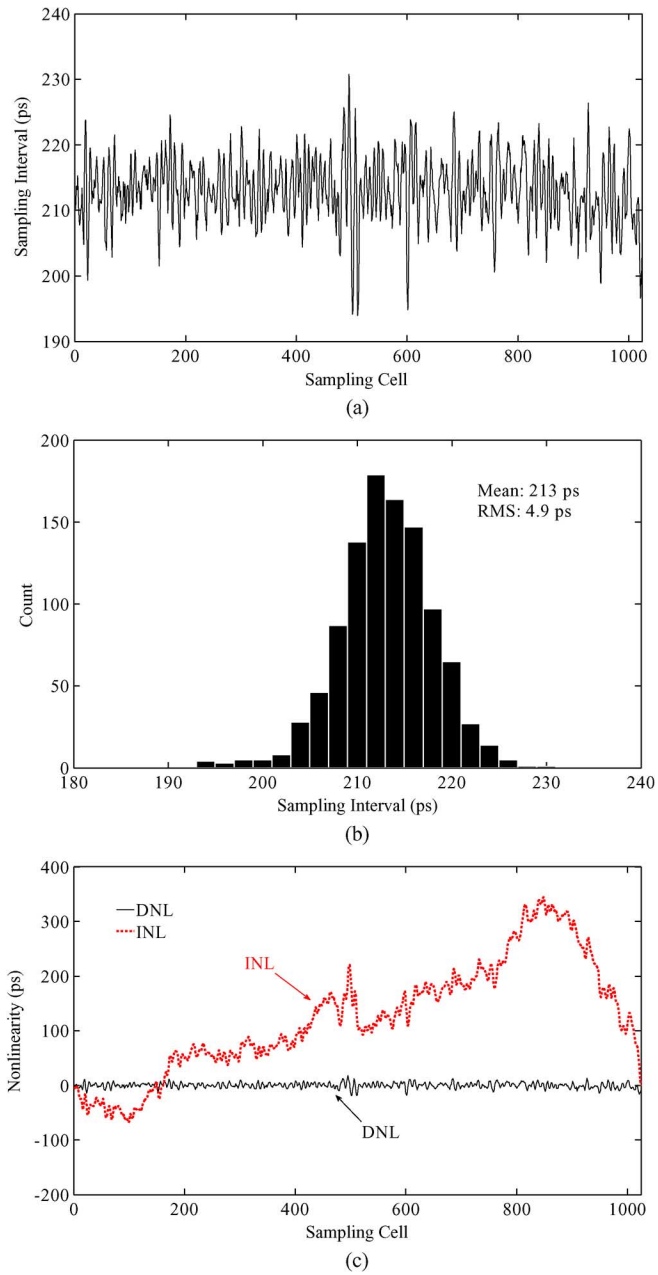

Fig. 9. Sampling intervals of DRS4 at 4.7 GS/s. (a) Sampling intervals of the 1024 taps. (b) Distribution of the sampling intervals. (c) Nonlinearities of the sampling intervals (INL and DNL).

free-running with respect to the sampling clock of the module is connected to two channels with a constant cable delay between the channels. The module records the waveform of the pulses, and typical waveforms after dc offset calibration and noise filtering are shown in Fig. 10. The time intervals of the pulses are derived with pulse shape fitting and digital constant fraction zero crossing. The two channels under test in this module are identical and independent. Therefore, the timing precision per channel is reflected as $1/\sqrt{2}$ of the standard deviation of the time intervals.

For the pulse shape fitting algorithm, we applied a polynomial fitting of the leading edges of the pulses, and the arrival time was derived at the crossing time of a constant digital discrimination level on the reconstructed leading edges. Fig. 11

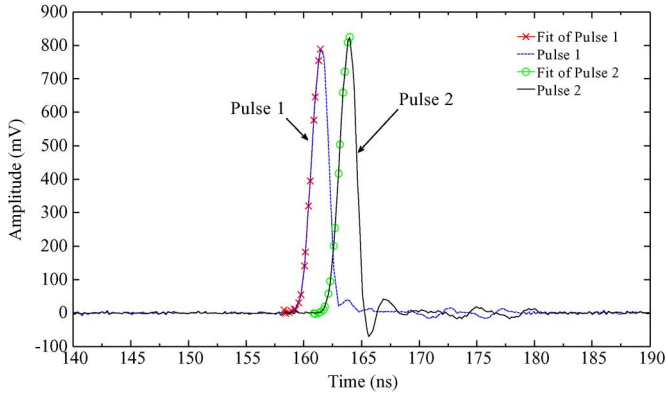

Fig. 10. Fast pulses and their polynomial fitted leading edges in the test.

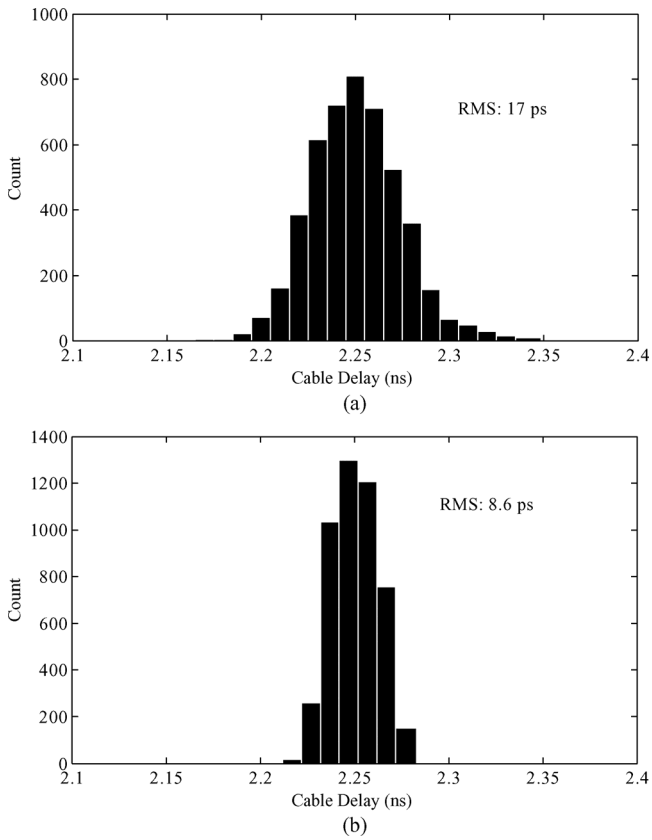

Fig. 11. Comparison of the distribution of pulse delay derived with a 6-order polynomial fitting algorithm, in which (a) and (b) are with and without calibration of nonuniform sampling intervals respectively.

shows the typical distribution of the pulse delay derived from 200 mV on 6-order polynomial fitted leading edges (as shown in Fig. 10). Fig. 11(a) and (b) shows the distribution of the pulse delay without and with calibration of the uneven sampling intervals, respectively. The timing precision per channel is improved from 17 to 8.6 ps RMS after calibration of the uneven sampling intervals. In the test, we find the RMS timing precision is improved to be below 10 ps after 4-order polynomial fitting of the leading edges. Higher order of polynomial fitting algorithms takes more time and resources particularly when implemented in hardware. Therefore, 4-order polynomial fitting is sufficient for sub-10-ps timing precision in our application.

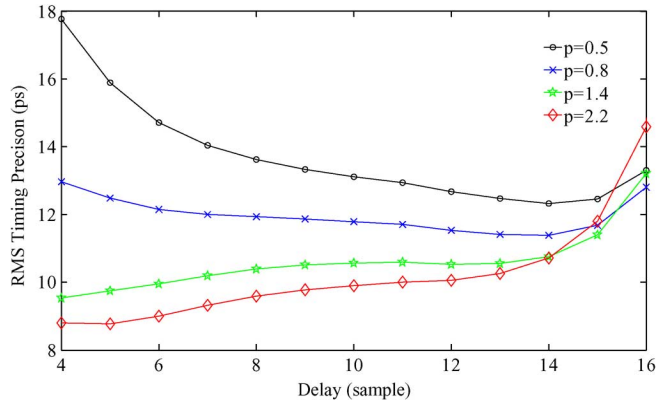

Fig. 12. RMS timing precision versus delay and the digital gain for digital constant fraction zero-crossing method.

For digital constant fraction zero crossing, we started with interpolation of the pulses with respect to their uneven sampling intervals to obtain uniformly spaced samples at 4.7 GS/s. A proper value of the delay (τ_{d}) and the digital gain (p) results in better timing precision, and the optimal values are dependent on the characteristics of the pulses. We find them with the sweep of the RMS timing precision at different delays and gain. The delay (τ_{d}) is evaluated in the range 4–16 sampling steps to cover the leading edge (about 10 samples) while p is from 0.4 to 4 for each delay. Fig. 12 shows the comparison of the RMS timing precision versus delay for p equal to 0.5, 0.8, 1.4, and 2.2. It is observed that the RMS timing precision varies at different pairs of delay and digital gain. Generally, the RMS timing precision drops as p rises from 0.5 to 2.2 for a delay within a certain range (4–13). In hardware realization of the algorithm, longer delay requires more logic resource. It is important to find out the optimal digital gain to meet the requirements of timing performance with the shortest delay, e.g., $p = 0.8$, delay $= 4$ is preferred to $p = 0.5$, delay $= 12$ for the requirement of 15 ps RMS timing precision. The optimal RMS timing precision of this algorithm is reached at $p = 2.2$, delay $= 4$, with which the timing precision is about 8.7 ps RMS.

Both the timing algorithms with polynomial fitting of the leading edges and that of the digital constant fraction zero crossing demonstrate sub-10-ps RMS timing precision of our module. We can evaluate the optimal parameters of algorithms and implement them in hardware at the minimal cost of logic resources in the future.

E. Evaluation of Interleaved Sampling

We interleave the channels of DRS4 with routing delays on the PCB. The delay between the two interleaved channels is controlled to be around 100 ps, which is approximately half the period of the domino clock (4.7 GHz in the module). In practice, the actual value is evaluated from the phase difference of sine waves recorded in the interleaved channels. Fig. 13 shows the phase difference derived from the waveforms of a 300-MHz sinusoid, in which the mean is about 78.7 ps, and its standard deviation is about 1.2 ps RMS. The phase difference reflects the interleaved interval and includes the total delay between the two channels.

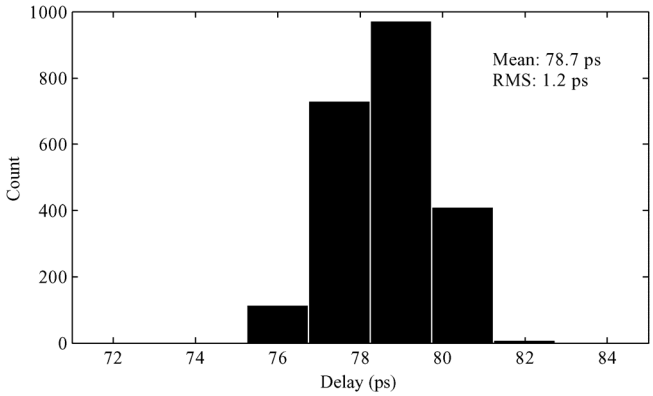

Fig. 13. Total delay of the inputs between the two interleaved channels.

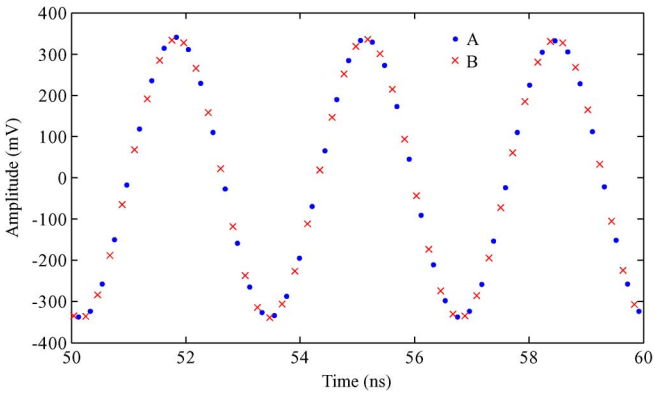

Fig. 14. Reconstruction of a 300-MHz sine wave in the interleaved channels of DRS4 at 4.7 GS/s.

We reconstruct the interleaved waveform by merging samples of two channels (A and B) together with respect to their time sequence. The offsets of the two channels were removed, and gain variations were compensated as well before the reconstruction operation. Fig. 14 shows part of the reconstructed waveform for a 300-MHz sine wave sampled at 4.7 GS/s. Twice the samples are obtained every cycle after interleaving, therefore the sampling rate (f_s) is equivalently increased by a factor of two, i.e., 9.4 GS/s.

The performance of the interleaved sampling scheme is evaluated with fast Fourier transform (FFT) analysis of the reconstructed waveform. The reconstructed waveform may not be uniformly spaced in time since it is difficult to control the interleaved interval to be exactly half the period of the domino clock, e.g., in our implementation, the actual interval is about 78.7 ps, whereas one half of the sampling period is about 106.5 ps at 4.7 GS/s. It is essential to make an interpolation of the samples to obtain their uniformly spaced counterparts for the FFT analysis, otherwise noise with peaks at $\pm f_{\rm in} + f_s/2$ in the spectrum will be induced, thereupon SNR degrades [31] ($f_{\rm in}$: input frequency). Fig. 15 represents the average of about 200 individual FFTs of a 300-MHz sine wave, in which (a) and (b) illustrate the improvement of dynamic performance with compensation of the uneven interleaved interval. In Fig. 15(a), there is a distortion located at about 4400 MHz, which is approximately $(-300 + 9400/2)$ MHz. The distortion comes from the uneven interleaved interval and disappears in the spectrum of samples after a cubic spline interpolation with uniform time-steps, as show in Fig. 15(b). Moreover, the signal-to-noise-and-distortion ratio (SINAD) is improved from

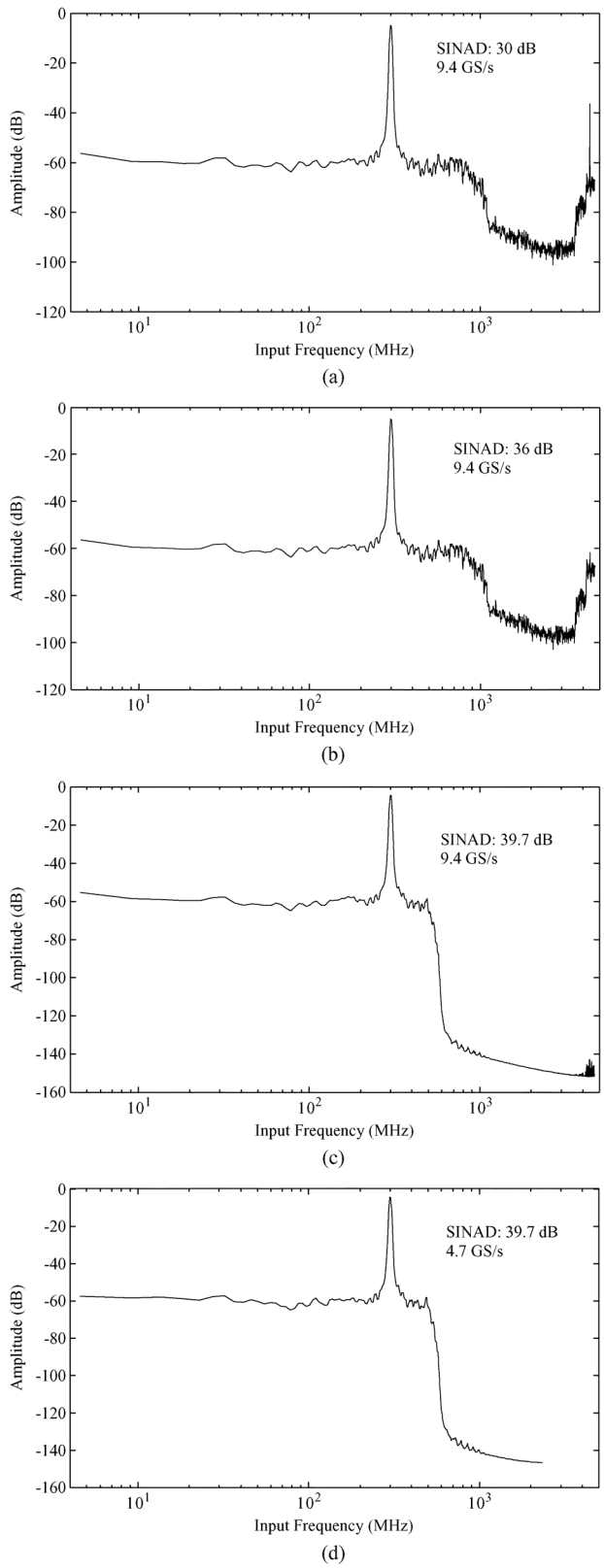

Fig. 15. FFT analysis of a 300-MHz sine wave, where (a) and (b) show the spectrum of the waveform from interleaved channels without and with calibration of the uneven interleaved sampling interval, respectively; (c) shows the spectrum of the interleaved samples in (b) after low-pass filtering, whereas (d) presents the spectrum of the low-pass filtered samples in one of the interleaved channels for comparison.

30 to 36 dB after compensation as well. SINAD can be further increased by filtering out the noise beyond −3-dB frequency band of input. In Fig. 15(c), SINAD reaches 39.7 dB after processing the samples in Fig. 15(b) with a low-pass filter described in the prior section. We also present the FFT analysis of the low-pass filtered samples in one of the interleaved channels in Fig. 15(d) and compare it to that in Fig. 15(c). We observe SINAD in Fig. 15(c) and (d), whereas both correspond to an effective number of bits (ENOB) of about 7 bits [32].

Interleaved sampling scheme doubles the sampling rate in our evaluation. However, there is no significant improvement on SINAD after applying the interleaved scheme. There are several factors limiting the dynamic performance of the module as the nonlinearity of the sampling capacitors of DRS4 and that of amplitude brought from the analog circuits on board. Moreover, the analog bandwidth is approximately halved after two-channel interleaving, which decreases the benefit of interleaved sampling dramatically. Nevertheless, the interleaved scheme itself is of great consequence. At present, the fifth version of DRS (DRS5) is planned at PSI [33]. DRS5 is schemed with a new technology, *cascaded switched capacitor arrays* (CSCAs). Fewer sampling capacitors are seen at the input of DRS5 compared to DRS4, thus the capacitive load is reduced and it is possible to interleave more analog channels without degrading the analog bandwidth significantly. The analog bandwidth of DRS5 is anticipated to reach 5 GHz with a maximum sampling rate of up to 10 GS/s per channel [33]. With the interleaved scheme, we are likely to sample ∼5 GHz input with 20 GS/s or more in the future.

V. Discussion

A. Interleaved Sampling of More Channels

In our implementation, we achieved 9.4 GS/s with two-channel interleaved sampling. The sampling rate can be further increased by interleaved sampling of more channels. However, more channels interleaving requires finer and more precise control of the routing delay on board, e.g., 25 ps routing difference is demanded per channel for eight-channels interleaving of DRS4 aiming at 40 GS/s. Moreover, the analog bandwidth will decrease dramatically without proper consideration of the analog driving circuits, which is quite challenging for the heavy capacitive load at the input. In the module, the analog bandwidth is around 600 MHz for normal channels, and about 360 MHz for the interleaved channels. The bandwidth will drop more seriously as the number of interleaved channels increases. We consider two-channel interleaving is sufficient for the current module. More channels interleaved sampling will be appreciated for DRS5 in the future.

B. Guideline for Uniform Interleaving

The interleaved samples may not be uniformly spaced if the time difference between them varies from one half of the sampling period. The nonuniformity of the interleaved interval mainly comes from the unpredicted variation of the input delay of DRS4. In the module, the delay is set to be around 100 ps for 4.7 GS/s, whereas the actual value is about 79 ps. We can interpolate the samples to achieve uniform sampling as long as the variation is within a certain percent of the sampling period [34]. On the other hand, we can also fine-tune the sampling rate of DRS4 to reduce the variation of the interleaved interval to the minimum. In actual implementation, the routing delay is suggested to be set a little larger than half the period of the maximum sampling rate to leave more room for the fine-tuning, e.g., suppose the time variation of the input of DRS4 is within 20 ps, the routing delay can be set to 120 ps for 5 GS/s. The actual interleaved delay may be 100–140 ps. We can then fine-tune the sampling rate of DRS4 to 5–3.57 GS/s accordingly to achieve a relatively more uniform interleaving.

VI. Conclusion

We presented a fast pulse sampling module with DRS4 and evaluated its performances of waveform timing and the scheme of interleaved sampling of the analog channels. In the evaluation, strategies for the calibration of the dc offset variation and nonuniform sampling intervals were developed. Algorithms for the signal processing of waveform timing and the interleaved sampling were proposed as well. It is proved that the module is capable of sub-10-ps RMS waveform timing precision after compensation for the nonuniform sampling intervals. We also have achieved about 10 GS/s with interleaved sampling between the analog inputs of DRS4.

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