Digitally-Assisted Analog Designs for Submicron CMOS Technology

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***Abstract*—Three different digitally-assisted analog designs are presented to demonstrate the powerful way to solve the analog design deficiencies in the submicron CMOS technology. A 200 MS/s 12-bit pipeline ADC is using the split-capacitor correlation method to solve the linear and nonlinear problems. A 1 GS/s 14-bit current-steering DAC is using the programmable sub-DAC to continuously trimming the current mismatches. A 25 MS/s 16-bit ΣΔ ADC is using the adaptive way to correct the leakage noise and DAC nonlinearity.**

I. INTRODUCTION

The rapidly shrunk CMOS technology has imposed very serious limitations on the conventional analog CMOS designs. The first serious limitation is the reduced voltage headroom and signal strength by the scaled power supply. The reduced voltage headroom will limit the number of the cascode voltage stack which will make the amplifier have the lower gain in the submicron CMOS technology. This also will induce the finite gain error in all the amplifier stage. The reduced signal strength, in the other way, will cause the noise-limited circuits such as ADC to reduce the possible noise sources in order to maintain the reasonable SNR ratio. This will make the chip silicon area and the power consumption rapidly increased. Besides that, the increased random process variations and the decreased intrinsic voltage gain will make the typical analog CMOS designs become even harder. However, the SOC integration requirement and the improved transistor performance will make the deep submicron analog CMOS designs have the inevitable necessity.

Several design techniques have been proposed to modify or assist the traditional analog CMOS designs in order to compensate the performance loss due to the scaled CMOS technology. Analog or digital calibrations are the mostly used method to re-vitalize the high precision CMOS designs. Among those approaches, the digitally-assisted design could be the most interesting and the most favored technique. The reason is that the scaled CMOS technology will make the digital transistors have the lower power and become much cheaper. Besides that, the digital design will make the whole digitally-assisted analog design more robust and portable. Fig. 1 shows the energy ratio required to achieve the necessary SNDR for the pure analog design, E_{ADC}, and the NAND2 digital gate, E_{NAND2} [1]. For the low SNDR design, the conventional analog design would be favored. However, for the high SNDR design, the digital approach can save the traditional analog design tremendous power and area. The typical questions for the digitally-assisted analog design are how to formulate the calibration variables, how to extract the errors and how to compensate the errors. And this approach can translate the analog precision problems into the complexity of digital signal processing circuits and take the benefits of the CMOS device scaling.

In this paper, three digitally-assisted analog designs will be briefly introduced. The first one will be a 200 MS/s 12-bit pipeline ADC with split-capacitor background calibration. The second one will be a 1 GS/s 14-bit current-steering DAC with background

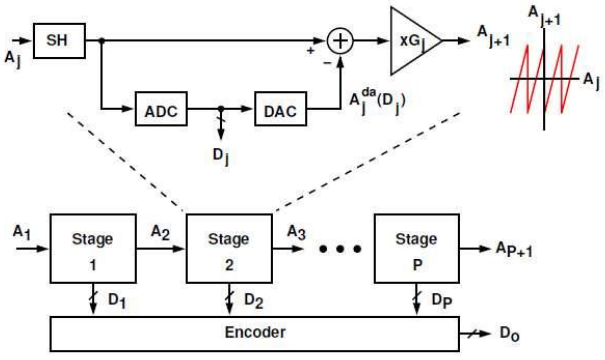
SNDR	E_{ADC}/E_{NAND2}	
30	4,679	⇨ Additional digital processing is costly!
50	37,432	⇨ Several tens of thousand gates are "free"
70	299,479	
90	2,396,045	⇨ Use as many gates as you can fit…

Fig. 1. Energy ratio between the pure analog design and the digital gate for the required SNDR precision [1].

trimming techniques. The third one will be a 25 MS/s 16-bit ΣΔ ADC with adaptive leakage noise and DAC nonlinearity calibration.

II. DIGITALLY-ASSISTED PIPELINE ADC DESIGN

In this design, we formulated to correct the opamp gain error, capacitor mismatch error, opamp and comparator offset error and opamp nonlinearity error. The offset error can be easily eliminated by the 1.5 bit redundancy architecture. The whole 12-bit pipeline ADC is then consisted of one S&H stage, 13 1.5-bit MDAC stages and one 2-bit flash sub-ADC stage. The final 12-bit output code is summarized by the digital block which includes the state-machine, adders, multipliers and accumulators. Fig. 2 shows the typical pipeline stage with the 1.5-bit transfer curve.



$$V_{j+1} = G_j \times \left(V_j - V_j^{da}(D_j)\right)$$

Fig. 2. Pipeline ADC architecture

The split-capacitor approach is adopted in this design not only to solve the linear problems, but also the nonlinear distortions [2]. We

found the split-capacitor correlation-based background calibration algorithm is quite robust that the whole algorithm is not dependent on the input signal distribution to correct the linear and the nonlinear errors [3]. The extracted errors can be easily calculated from the transition heights of the transfer curves of the 1.5-bit MDAC. Fig. 3 demonstrates the basic split-capacitor approach that the sampling capacitor is split into C_{S1} and C_{S2} from the total value of C_S. A randomly generated signal q is then injected into C_{S2}. The final transfer curve can be summarized as shown in the right hand side. The input signal can be divided into four regions. In the different region, the applied voltage for the q=1 and q=0 is shown. By collecting enough samples, the average values in the q=1 region and the q=0 region can be extracted. The difference of these two values is then the value of w_2. By exchanging the random q injected into C_{S1} instead of the C_{S2} as shown here, we can then extract the value of w_1.The sum of w_1 and w_2 is the transition height of the transfer curve. The value of the transition height is used in the digital block to correct all the linear and nonlinear errors. Of course, the nonlinear error has to go through complex distortion modeling and calculations in order to solve the opamp nonlinear problem. The nonlinear problem will become more significant when the power supply is scaled even further.

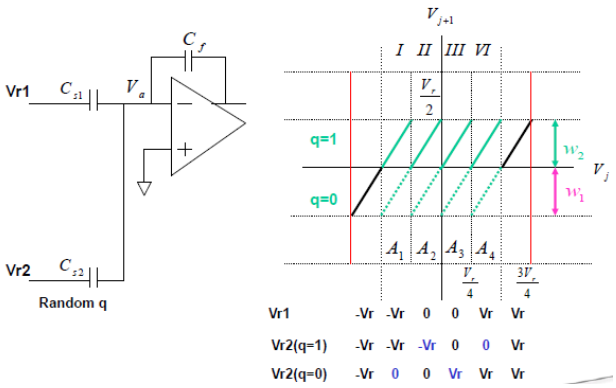


Fig. 3. Split-capacitor architecture

The MDAC opamp gain is designed with 40 dB in the 65 nm CMOS technology with only 1.2V power supply. The opamp architecture is the typical folding cascade two stage opamp. The final chip photograph is shown in Fig. 4. In the right hand side, the digital block is designed to solve both of the linear and nonlinear errors with the nonlinear error modeled with a 3-order polynomial equation.

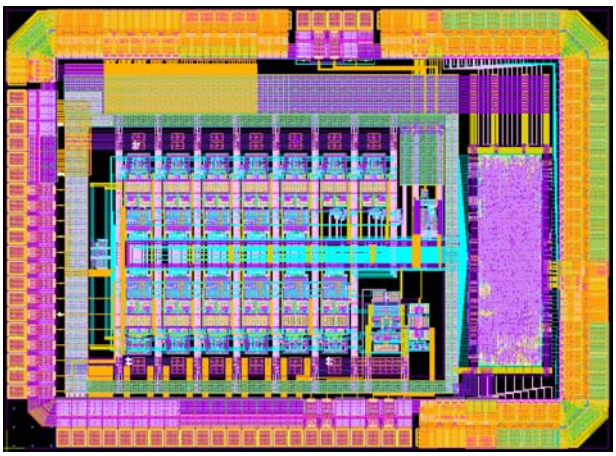


Fig. 4. Pipeline ADC photograph

The preliminary test results are shown in Figs. 5, 6, 7 and 8. Fig. 5 shows the DNL and INL errors when the digital calibration is turn off. A lot of missing codes were found. Fig. 6 shows the DNL and INL errors when the liner calibration mode is turn on. The improvement was clearly observed. Fig. 7 shows the DNL and INL errors when both of linear and nonlinear modes are turn on. A very small improvement was found which indicated that the nonlinear error is not quite serious here. Fig. 8 shows the FFT analysis in the AC testing mode.

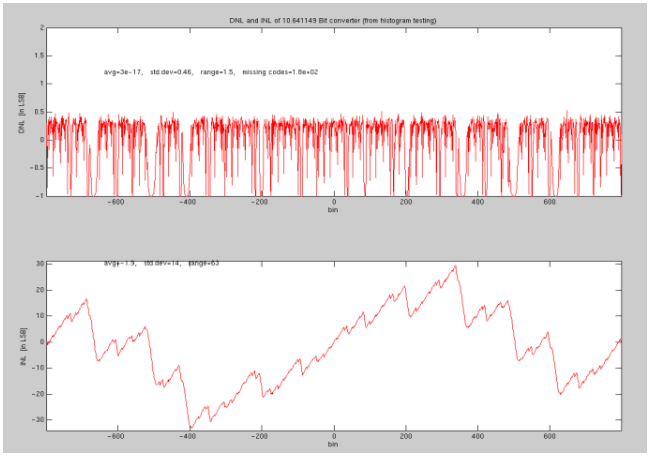


Fig. 5. DNL and INL errors with calibration turn off

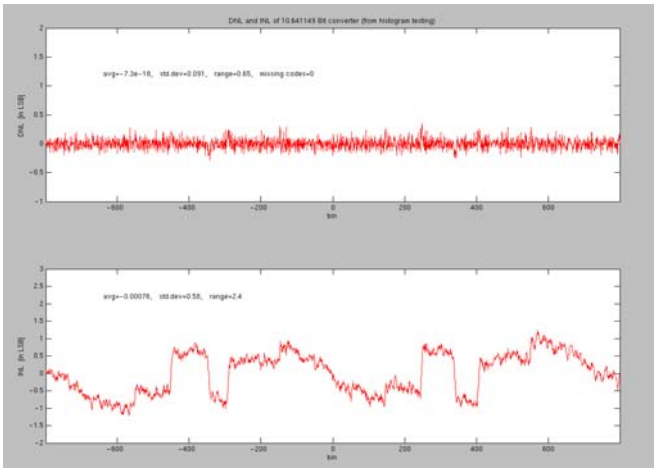


Fig. 6. DNL and INL errors with linear calibration turn on

III. DIGITALLY-ASSISTED DAC DESIGN

The 14-bit current-steering DAC is split into two 7-bit blocks. Both of the MSB and LSB blocks are coded with thermometer codes of 128 current cells in each block. The LSB current cell size is optimized and also randomly placed in order to eliminate the current mismatch [4]. The LSB block will not go through any trimming process in this chip. Its total current will then be measured into a dummy current cell as shown in Fig. 9. A two-order ΣΔ ADC is designed to measure the current difference between the two tested current cells. The measured difference is used to tune the small current DAC as shown in the calibration block of Fig. 10. In the power on stage, the current mismatch caused by the process is measured first between the LSB block and the dummy current cell. Afterward, the dummy current cell will be tracked with the voltage and the temperature variations of the LSB block. This dummy current cell will then be used to calibrate another MSB dummy cell. The 128

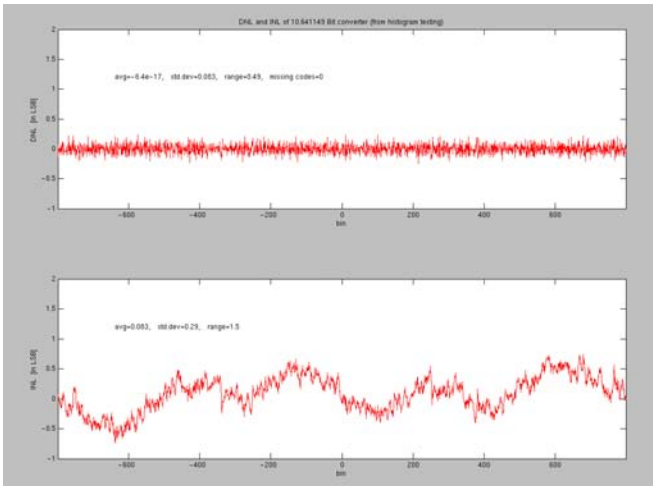


Fig. 7. DNL and INL errors with the linear and nonlinear calibration modes turn on

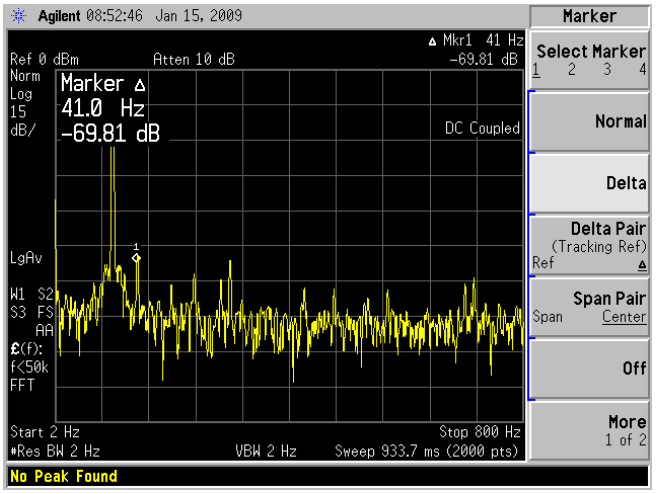


Fig. 8. FFT waveform for the pipeline ADC

MSB current cells are trimmed one by one with the LSB dummy current cell. In order to let this DAC operate continuously, the current cell in trimming is then replaced by the MSB dummy current cell. The procedure is repeated continuously while the chip is operating.

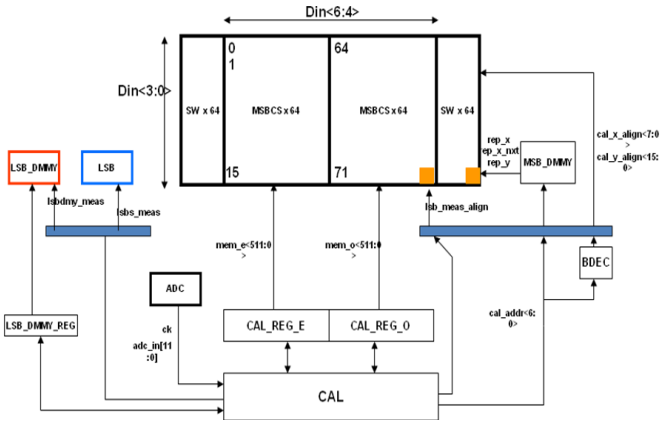


Fig. 9. 14-bit current-steering DAC architecture

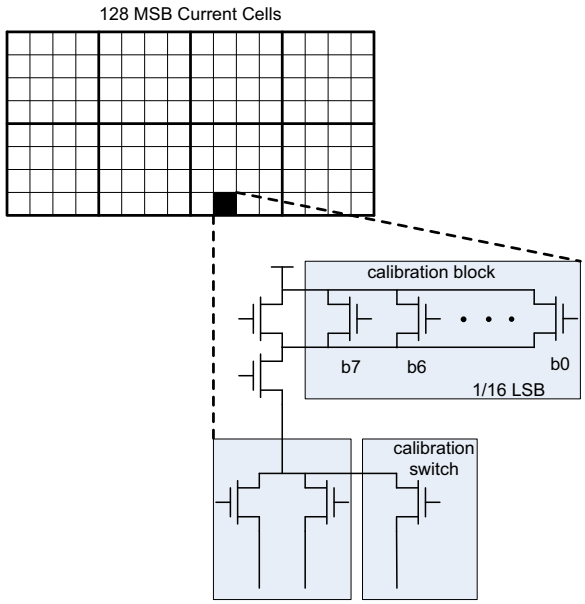


Fig. 10. MSB block current cell structure

Fig. 11 shows the photograph of the 14-bit current-steering DAC. The core area is shown on the upper left corner with the area of 1000x700 μm^2 in the 65 nm CMOS technology. The rest of area is the decoupling capacitors used to reduce the power supply bouncing problem while the chip is in testing.

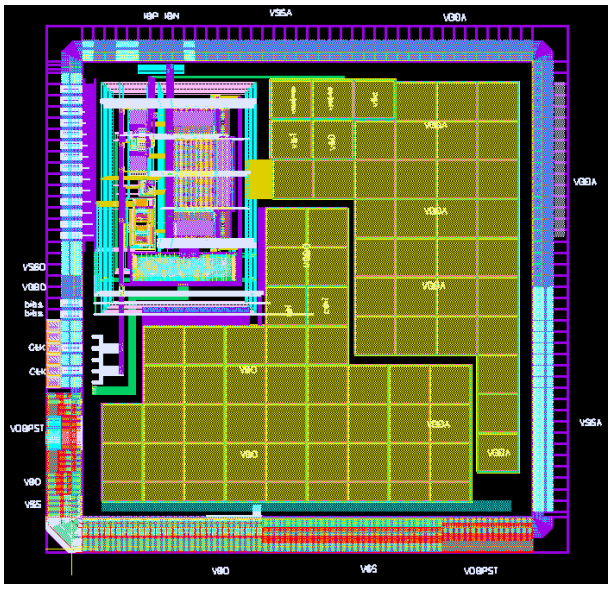


Fig. 11. Photograph of the 14-bit current-steering DAC

IV. DIGITALLY-ASSISTED ΣΔ ADC DESIGN

Oversampling ADC usually shows the very high resolution, but with a very low bandwidth. In order to achieve the 16-bit high resolution and the high bandwidth of 25 MHz, we used the MASH structure. MASH structure inherently has the stable operation, but with the noise leakage problem that it degrades the performance dramatically. Besides that, for the high resolution, we have to use the multibit DAC to reduce the quantization noise. The multibit DAC will introduce the nonlinearity problem. All of these noise leakage

and DAC nonlinearity will use the digital approach to solve. The leaked noise from the 1st stage to 2nd stage will be solved by using a adaptive FIR to combine with the original DNTF as shown in Fig. 12 [5]. The coefficients of the adaptive FIR will be updated frequently by using the LMS algorithm [6].

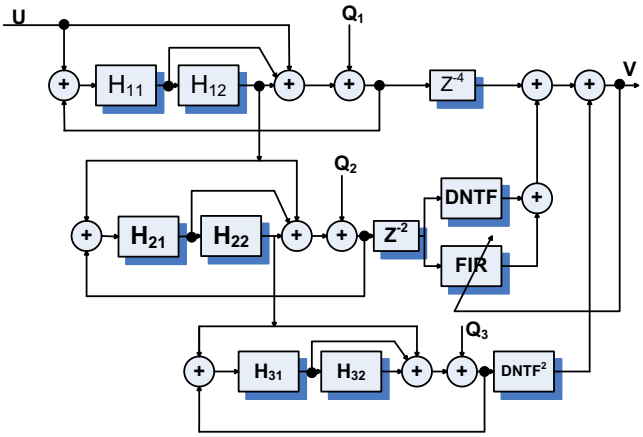


Fig. 12. MASH ΣΔ ADC architecture

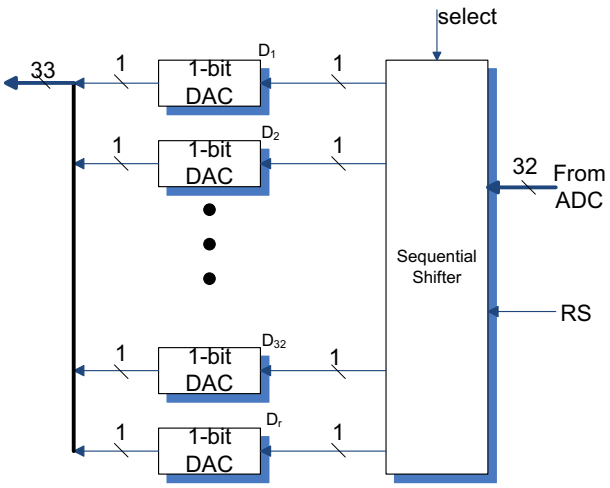


Fig. 13. Modified 5-bit DAC in the MASH ΣΔ ADC

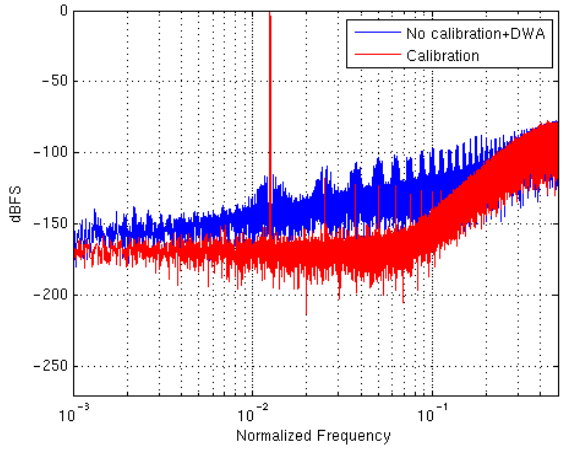


Fig. 14. Performance comparison

The DAC nonlinearity calibration is solved by inserting one more bit into the modified 5-bit DAC as shown in Fig. 13 [7]. The RS signal is a randomly generated signal. By shifting the 32-bit input signals and the RS signal, we can statistically extract the capacitor mismatch values. Fig. 14 shows the comparison between the traditional way to solve the DAC nonlinearity with DWA and the digital calibration. The digital calibration shows the superior performance. Fig. 15 shows the final simulated MASH ADC performance with the adaptive leakage noise and DAC nonlinearity background calibration.

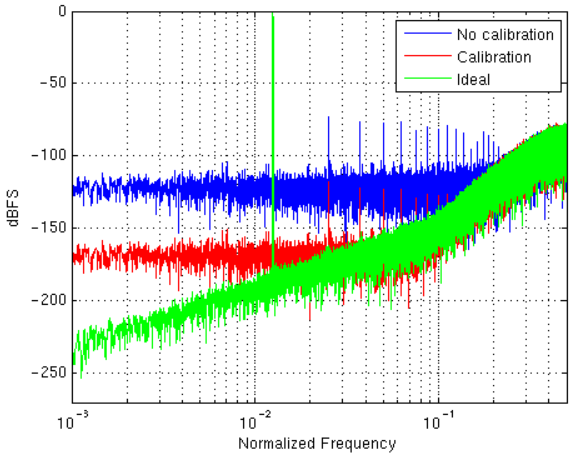


Fig. 15. The final ADC performance comparison among the one without calibration, with calibration and the ideal case.

V. CONCLUSIONS

Digital calibration shows that it is a very powerful way to solve the analog deficiencies in the deep submicron CMOS technology. By using the digital approach, the analog design can be relaxed, the larger mismatch can be tolerated and the final precision can be restored.

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