A 12b 3GS/s Pipeline ADC with 500mW and 0.4 mm^2 in 40nm Digital CMOS

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Abstract

A 12b 3GS/s 2-way interleaved pipeline ADC is presented. To achieve high speed, multiple internally generated power/ground rails are used with thin-oxide MOS devices. The ADC achieves a SNR of 61dB and a DNL of -0.4/+0.6LSB, consumes 500mW at 3GS/s and occupies 0.4 mm^2 area in 40nm CMOS process.

Introduction

A new breed of high speed and high resolution ADCs are enabling wide-band direct sampling receivers in communications systems. In this ADC, high speed is achieved by using thin-oxide transistors in key high speed blocks along with multiple internally generated power/ground rails. It achieves up to 3GS/s sampling rate and 61dB SNR while consuming 500mW power. Table I shows the performance comparison with recently published works.

Figure 1 shows the architecture of the 3GS/s 12-bit ADC. It consists of 2 interleaved ADCs running at half rate 1.5GHz clock with opposite phases. Each ADC uses a 2-2-2-6 architecture consisting of three MDAC stages and one 6b flash ADC, taking full advantage of the maximum speed in each stage to achieve the lowest power. The offset, gain and timing mismatches between the two ADC slices are corrected on chip using digital calibration.

Amplifier and Switch Design

The key to achieve high speed and high resolution in this work is the combination of 2.5V supply for amplifiers and 40nm thin-oxide MOS transistors for both g_m devices and switches. The use of 2.5V supply maximizes the signal swing to 1.4Vpp and improves SNR by more than 6dB compared to using 1V supply.

Figure 2 shows the amplifier structure used in the sample-and-hold (SHA) and MDACs. Thin-oxide NMOS transistors with large W/L ratio are used as the input differential pair to achieve high g_m and low V_{dsat} while having low parasitic capacitance for wide bandwidth and good phase margin. High gain that is required for 12b linearity is achieved by a telescopic cascode structure with the assistance of gain boosting. The cascode transistors are properly biased to protect the thin-oxide input transistors. In Figure 2, the amplifier output common mode voltage V_{cm1} and the amplifier input common mode voltage V_{cm2} levels track temperature, process variation, and supply voltage for optimum operating points.

Another bottleneck for high-speed pipeline ADC design is the CMOS switches that turn on/off the capacitors for signal sampling and charge transfer. Figure 2 shows the block diagram of sample-and-hold circuit. If the switches *s1*, *s2*, and *s3* are implemented using thick-oxide CMOS transistors with minimum channel length of 0.25 μm, it will be impossible to achieve 1.5GS/s sampling speed. To overcome this problem, we use thin-oxide CMOS transistors with minimum channel length of 40 nm for all switching devices, achieving a 10x improvement in speed and a reduction of charge inject error. As shown in Figure 2, the switch and the corresponding driver stages are all implemented using thin-oxide devices. To accommodate 1.4Vpp signal swing, the local power and ground for the switch, V_{dd1} and V_{ss1}, are designed to have the same common mode voltage as amplifier output V_{cm1}. On the other hand, to keep the voltage stress of the switch within the safe level, the difference between V_{dd1} and V_{ss1} is regulated to be less than 1V, limited by the 40nm technology. The V_{dd1} and V_{ss1} are generated inside the ADC by two low drop-out regulators (LDOs). Their common mode voltage tracks the common mode voltage of amplifier output over the process, temperature, and supply voltage variation for best performance. The ADC clock is level shifted up through an ac-coupled capacitor with a DC biased voltage of V_{cm1} to V_{dd1}/V_{ss1} domain to drive the following thin-oxide drivers and switches.

Flash Design

Each MDAC has a 2.5b flash ADC and the final residual is digitized using a 1.5GS/s 6b flash ADC. The flash ADCs must digitize 1.4Vpp voltage swing within a fraction of the 1.5GHz clock, while presenting a low input capacitance to maximize the signal bandwidth. Figure 3 shows the implementation of the flash ADC. The 40nm thin-oxide devices offer even greater advantage for flash ADCs as the regeneration time can be an order of magnitude shorter. The flash ADCs use exclusively thin-oxide transistors. Multiple power/ground rails are used to maximize input range while ensuring reliability. The folded preamplifiers are powered by the V_{dd1} supply to achieve 1.4Vpp input range. The latches are operated between V_{dd1} and V_{ss1} and their outputs can directly control the MDAC switches. The latch outputs are shifted down to 1V domain by high-speed level shifters to interface with digital circuitry. To minimize the input capacitance, the 6b flash ADC uses averaging to relax input matching requirement and interpolation to reduce the number of preamplifiers. Averaging requires over-ranging to compensate for the boundary effect and may lead to reduction of available input range. In this design, 3-input dummy preamplifiers are used at the edges to generate over-range voltages from inner taps of the resistor ladder while maintaining the maximum input range. Dummy latches are placed at the edges to equalize the capacitance and kickback at high frequency. The above techniques make it possible to build a 6b 1.5GS/s flash ADC with very low input capacitance, and enable the low power 2-2-2-6 pipeline architecture by avoiding additional MDAC stages.

Measurement Results

Figure 4 shows the measured SNR and SNDR as functions of sampling frequency and input frequency. The ADC achieves 61dB peak SNR and maintains near constant SNR from 100MHz to 1.1GHz. The peak SNDR is 59dB. The

SNDR remains above 50dB up to 3GS/s sampling rate and 1GHz input frequency. The DNL is within +0.6/-0.4LSB and the INL is within +/-2LSB. Figure 5 shows the ADC output spectrum with 1GHz wideband QAM input signal.

References	[1]	[2]	[3]	[4]	**This work**
Process (nm)	130	90	180	90	**40**
Resolution (bit)	11	11	10	11	**12**
Fs (GS/s)	1.0	0.8	1.0	0.5	**3.0**
SNR (dB)	59	60	57	-	**61**
SNDR (dB)	55	58	56	53	**59**
Power (mW)	250	350	1260	55	**500**
Area (mm^2)	3.5	1.4	49	0.5	**0.4**

Table 1: Comparison of >500MS/s and >10b ADCs.

References

[1] S. Gupta et al., "A 1GS/s 11b Time-Interleaved ADC in 0.13um CMOS," ISSCC Digest of Technical Papers, pp. 2360-2369, Feb. 2006.

[2] C-C. Hsu et al., "An 11b 800MS/s Time-Interleaved ADC with Digital Background Calibration," ISSCC Digest of Technical Papers, pp. 464-465, Feb. 2007.

[3] R. Taft et al., "A 1.8V 1.0GS/s 10b Self-Calibrating Unified-Folding-Interpolation ADC with 9.1 ENOB at Nyquist Frequency," ISSCC Digest of Technical Papers, pp. 78-79, Feb. 2009.

[4] A. Verma et al., "A 10b 500MHz 55mW CMOS ADC," ISSCC Digest of Technical Papers, pp. 84-85, Feb. 2009.

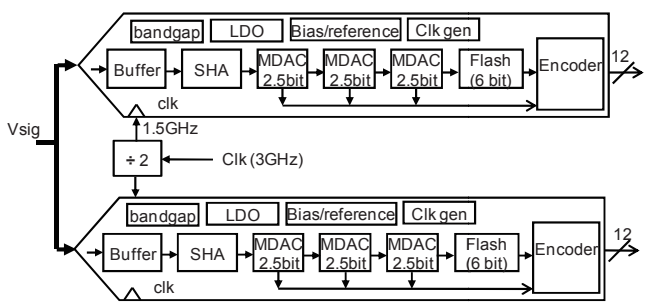

Figure 1: Architecture of 3Gs/s 2-way interleaved ADC.

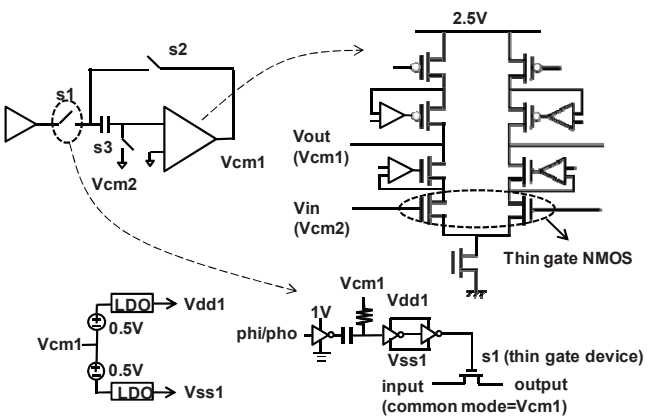

Figure 2: Sample-and-hold amplifier and switch design.

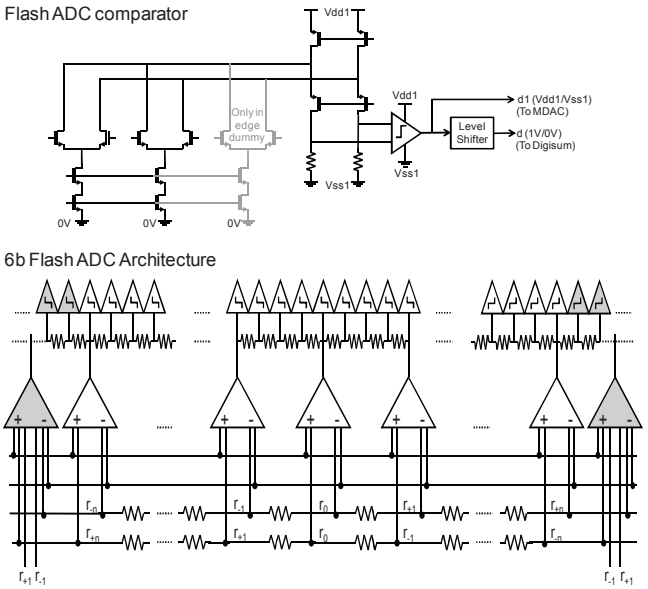

Figure 3: Flash ADC implementation.

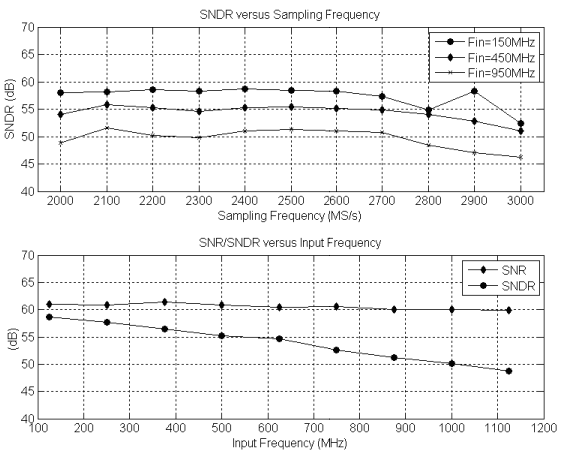

Figure 4: (a) SNDR versus sampling frequency; (b) SNR/SNDR versus input frequency.

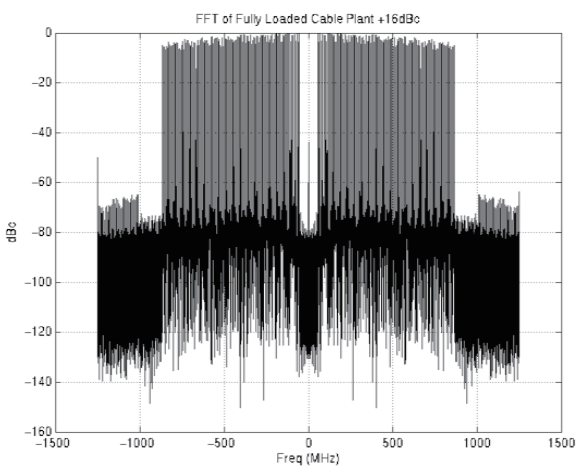

Figure 5: ADC output spectrum of 1GHz QAM signal.