A 4.8 GS/s 5-bit ADC-Based Receiver With Embedded DFE for Signal Equalization

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***Abstract*—A 5-bit 4.8 GS/s 4-way time-interleaved ADC is designed for a receiver front-end in a 0.13 μm CMOS technology. Each time-interleaved ADC uses look-ahead pipelined stages to enable higher sample rates and more linear residue characteristics than a conventional pipeline ADC. At 1.2 GHz per path, the residue amplifiers settle to 75% of their final value, however, the linear residue characteristics allows using digital reference calibration to enable 30.4 dB of SNDR with a 1.2 MHz input signal. A capacitor pre-charging technique reduces the memory effect errors of the incompletely settled residue to 2% of the stage output swing. The peak INL and DNL are measured as 0.65LSB and 0.55LSB, respectively. The measured ERBW is $\sim$ 6.1 GHz. The ADC, including the reference buffers, consumes 300 mW from a 1.2-V supply while operating at 4.8 GHz conversion rate. A stage-by-stage feedback compensates the possible bandwidth limitation of the system using a per-stage speculative DFE. The DFE tap is adjustable between 0 and 0.4 using 8 control bits.**

***Index Terms*—Analog-to-digital converter (ADC), decision feedback equalizer (DFE), digital reference calibration, equalization, incomplete settling, pipeline, time interleaved.**

I. Introduction

DATA converters have commonly been adopted in data-communication applications. ADC-based receivers have recently emerged in multi-gigasamples/second (GS/s) signaling applications across the highly attenuating channels between the integrated circuits (ICs) [1], [2]. At data rates that well exceed the 3 dB channel cut-off frequency, the channel attenuation and imperfections result in severe inter-symbol interference (ISI). ADCs and digital signal processing (DSP) enable a number of signaling and equalization techniques that can improve the signal integrity and facilitate transferring large amounts of data between ICs. In a binary signaling scheme, fully digital equalizers can be employed following the front-end ADC to cancel the ISI. Digital feedforward equalizers (FFE), decision-feedback equalizers (DFE) and sequence detectors are possible. Digital signal processing can be advantageous in that it is less sensitive than analog circuitry to process, voltage and temperature variations, is highly programmable, and scales well with CMOS process advances [1].

A front-end ADC can also be used to receive a signal with more complex symbol modulation. With a transmitter that can transmit multiple levels, modulations such as multi-level pulse-amplitude modulated (M-PAM) [2]–[4] or partial-response (PR) signaling [5]–[8] can better match the channel roll-off and make better use of the available channel capacity. It has been shown that for channel characteristics that exhibit sharp roll-off, using more complex modulation results in a lower Nyquist frequency and consequently a better signal-to-noise ratio (SNR) at the receiver than a binary data transmission at a given data rate [3].

For multi-GS/s data transmission, an ADC sampling frequency equal to the symbol rate is needed. With multi-level signals, the ADC resolution determines the maximum number of signal levels. A higher resolution is needed for ISI compensation by any subsequent digital equalizers. The required number of bits of resolution depends on the channel characteristics. A multi-GHz sampling bandwidth is also desired to avoid further distortion of the received symbols. A limited bandwidth of the ADC would appear as a low-pass filter that would result in more ISI and thus is undesirable. Furthermore, low power consumption is preferred in those applications that need multiple serial-link receivers built on a single chip.

This paper proposes a low-medium resolution pipeline ADC at 1.2 GS/s that can serve as part of a receiver front-end in a 0.13 μm CMOS technology. A sampling rate of 4.8 GS/s is achieved through 4-way interleaving. The architecture achieves a 2 $\times$ increase in sampling rate per pipeline path as compared to [9], [10], and the FOM is more than 3 $\times$ better. To achieve the improved performance, two techniques are introduced: (1) look-ahead pipeline architecture in conjunction with digital reference calibration to substantially reduce the settling time of the stages, and (2) capacitive pre-charging to reduce the memory effect errors. For equalization, the architecture introduces a DFE with a maximum tap weight of 0.4 which is a marked improvement over a coefficient of 0.25 [9]. The improvement is through employing a reduced-radix stage design and per-stage ISI speculation.

Section II describes the architecture of the proposed ADC and the stage-by-stage DFE. Circuit implementations are presented in Section III followed by a performance analysis in Section IV. Section V summarizes the performance of the ADC and DFE with the experimental results. Section VI concludes this paper.

II. Receiver Architecture

This section describes the architecture of the proposed ADC and DFE. The key techniques that achieve GS/s sampling speed and enable the signal equalization are described.

A. ADC Architecture

Fig. 1 shows the architecture of the proposed ADC which is composed of an array of 4 time-interleaved ADCs. Each time-

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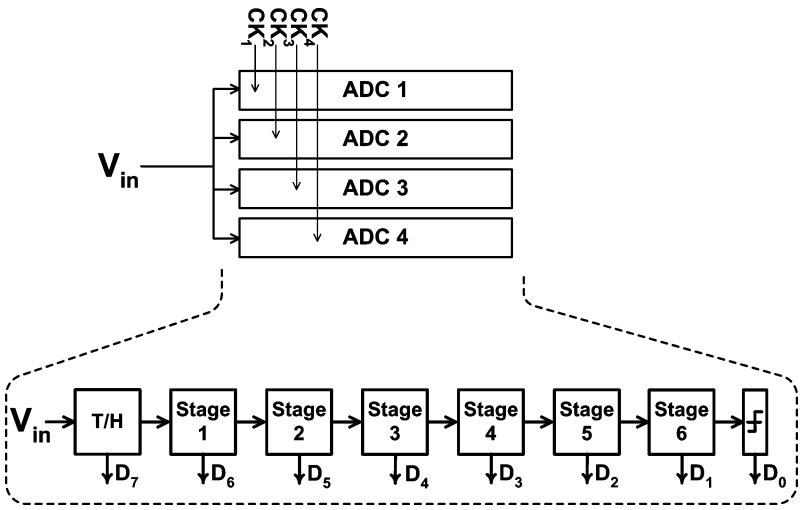

Fig. 1. ADC architecture.

slice targets 1.2 GS/s for a total sampling rate of 4.8 GS/s. Each ADC has been designed for an input sampling bandwidth of >6 GHz to allow for even higher degree of interleaving [11], [12]. Each gigasample/sec ADC employs pipeline architecture instead of the traditional flash architecture because of the potential for power efficiency, low input capacitance per path, and the ability to embed a DFE [9]. The required power consumption of a pipeline ADC is linearly related to the number of bits whereas in a flash converter such dependency is exponential. As this paper shows in Section II-C, partial signal equalization can be implemented at each stage of the pipeline ADC. In addition, pipeline converters have scaled well with CMOS technology [13]. Because digital circuits have scaled well, pipeline ADCs have benefited from a number of digital error correction techniques to improve the limited accuracy of the comparators and amplifiers. Compared with SAR ADCs, pipeline ADCs can operate at substantially higher sample rates.

To achieve 5 ENOB, each time-interleaved ADC consists of an input T/H followed by six pipelined stages and a final comparator stage.

Unlike a traditional pipeline ADC, the proposed ADC does not rely on accurate residue settling, thus enabling high sampling rates with low-power residue amplifiers [10], [14]. Section II-B proposes a modified digital reference calibration technique. A look-ahead architecture [15] is adopted in this design so that the critical path settling time is reduced and the digital reference calibration can be more effective. The ADC uses radix-1.6 pipelined stages. The operation of a radix-1.6 stage is similar to a regular 1-bit pipelined stage except that it amplifies the residue by a factor of 1.6 instead of 2. Reduced-radix stages are used in the pipeline for two purposes. First, they accommodate the over-ranging that results from applying signal equalization (discussed in Section II-C). Second, small comparators are used for power savings and any residual voltage offset from the comparators after calibration can be absorbed by the reduced-radix stage.

B. Improved Settling for Digital Reference Calibration

Increasing the sampling frequency beyond the residue-amplifiers' settling limits in a pipeline ADC results in inaccurate residues and reduced signal swing through the pipelined stages. Fig. 2(a) and (b) illustrates the impact on the signal swing. Incomplete residue settling may be viewed as residue scaling (with a scaling factor smaller than 1). At high sample rates, the output range of each pipelined stage covers a smaller portion of the input range of the subsequent stage (Fig. 2(c)) resulting in performance degradation. Digital reference calibration [10] adjusts the input range of each stage according to the maximum output swing of the previous stage (Fig. 2(d)) and recovers the degraded performance. The efficiency of the calibration depends on the linearity of the incompletely settled residue. In a regular pipeline ADC, the residue shows severe nonlinearities at high sampling rates thus limiting the efficiency of the calibration [10], [14].

In our proposed ADC, the sources of the residue nonlinear errors are identified and eliminated to achieve improved calibration efficiency. An analysis of the residue settling is necessary to identify the sources of the nonlinear residue errors. Fig. 3 shows a typical pipelined stage. The residue settling time $(t_{\rm residue})$, which is the amount of time that the pipelined stage needs to settle to the desired accuracy with the given input signal level, is composed of three partial settling times $t_{\rm latch}$, $t_{\rm sub-DAC}$ and $t_{\rm amp}$, where $t_{\rm latch}$ denotes the sub-ADC settling time (to generate $D_{\rm out}$), $t_{\rm sub-DAC}$ is the delay of the analog multiplexer and the buffer which generate $\pm V_{\rm ref}$ and finally $t_{\rm amp}$ is the amplifier's settling time. Note that these partial-settling intervals may overlap with each other, for example, the amplifier may start settling before $D_{\rm out}$ completes the selection of $\pm V_{\rm ref}$. Despite the overlap, it is instructive to consider each partial settling interval independently especially because each exhibit different characteristics. $t_{\rm latch}$ is a nonlinear function of $V_{\rm in}$ because the sub-ADC usually uses a positive feedback loop to regenerate $D_{\rm out}$. In a typical comparator that uses positive feedback to regenerate its output, the smaller the input, the longer the regeneration time. Once $D_{\rm out}$ is regenerated enough to cross the threshold voltage of the subsequent multiplexer, the correct reference voltage ($+V_{\rm ref}$ or $-V_{\rm ref}$) is selected. The delay of the analog multiplexer and buffer $(t_{\rm sub-DAC})$ is a mostly constant and input-independent number, after which the amplifier starts settling toward the correct final value, i.e., $1.6V_{\rm in}-0.6D_{\rm out}V_{\rm ref}$.

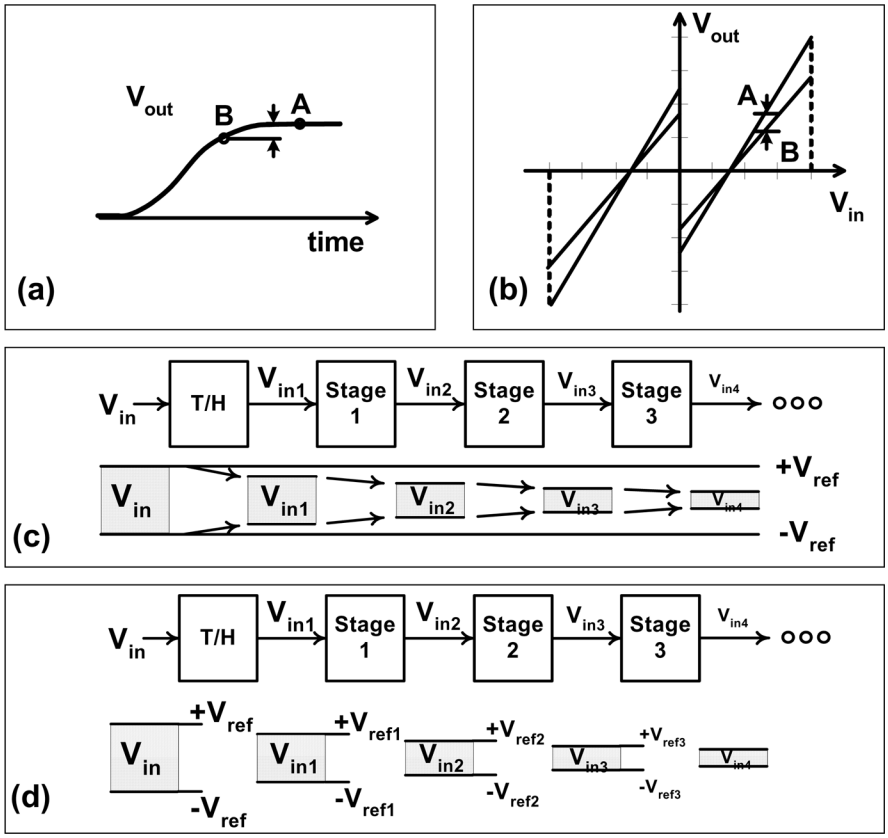

Fig. 2. (a) Incomplete residue settling at high sampling frequencies, (b) impact of incomplete residue settling on the residue plot, (c) demonstration of signal dynamic range through the pipelined stages before digital reference calibration and (d) after digital reference calibration.

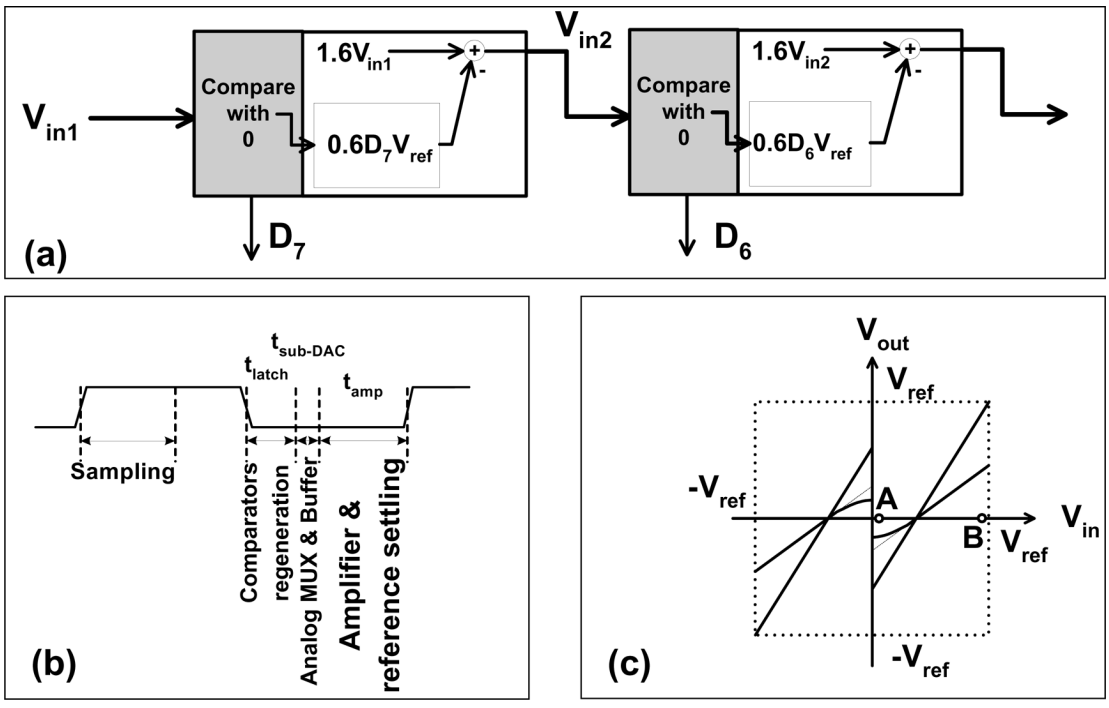

Fig. 3. (a) Two consecutive stages of a conventional radix-1.6 pipeline ADC, (b) the residue settling time and (c) the incompletely settled residue characteristics.

Finally, because an amplifier in a switched-capacitor network forms a linear system, $t_{\rm amp}$ does not depend on the input amplitude as long as slewing is avoided [16].

From this first-order analysis, $t_{\rm latch}$ is the dominant source of the nonlinearity in the residue. Being dependent on $V_{\rm in}$, $t_{\rm latch}$ occupies an input-dependent portion of the available settling

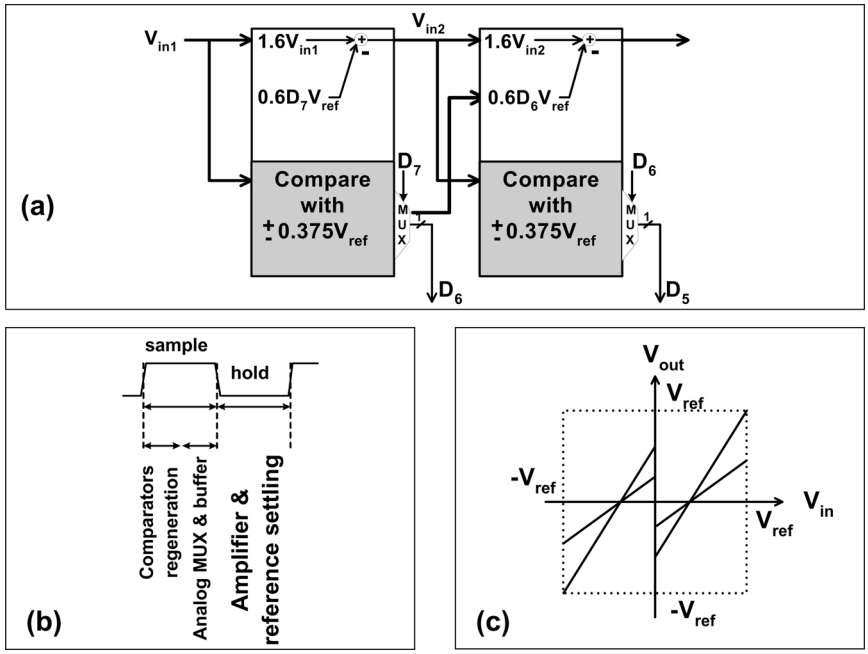

Fig. 4. (a) Two consecutive stages of the proposed look-ahead radix-1.6 pipeline ADC with (b) the residue settling time and (c) the incompletely settled yet linear residue characteristics.

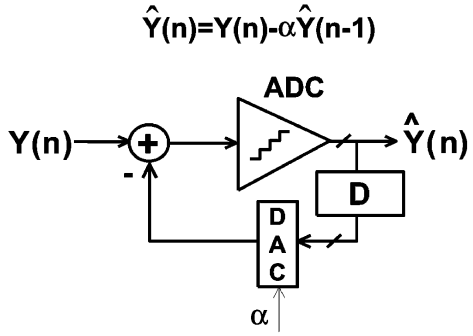

Fig. 5. The proposed single-tap DFE embedded inside the multi-level receiver.

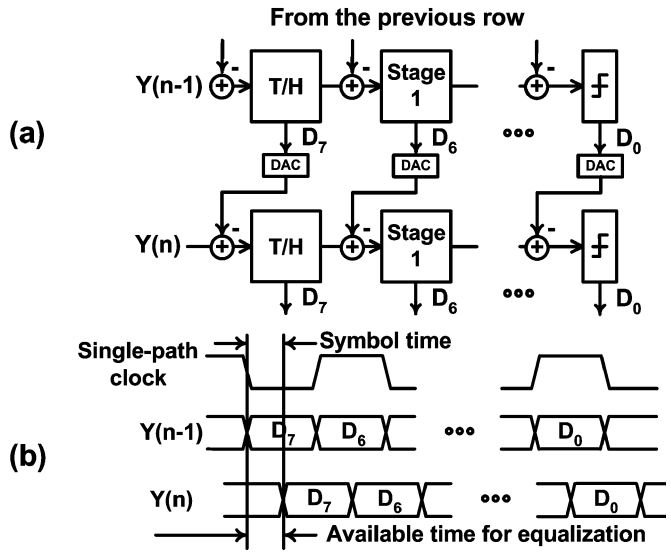

Fig. 6. (a) DFE with time-interleaved pipeline ADC with ISI subtraction at the input of the pipelined stages, (b) demonstration of DFE feedback delay requirement.

time and leaves the amplifier with an input dependent settling requirement, $t_{\rm amp} = t_{\rm hold} - t_{\rm latch}(V_{\rm in}) - t_{\rm sub-DAC}$, where $t_{\rm hold}$ is the available hold time (a constant number derived from the clock signal). For example, in Fig. 3(c), $t_{\rm latch}(A) > t_{\rm latch}(B)$ and therefore $t_{\rm amp}(A) < t_{\rm amp}(B)$. This implies a variable settling error and consequently a severely nonlinear residue characteristic at high sampling frequencies. Such nonlinearity fades away when $t_{\rm hold}$ becomes very large at low sampling frequencies when all residue values are allowed enough time to settle to the required accuracy, i.e., when $\max(t_{\rm residue}) \leq t_{\rm hold}$.

To improve the linearity of the insufficiently settled residue, the comparator's regeneration time should be removed from the hold time. Our proposed technique is to leverage a look-ahead pipeline architecture [15] in which the comparators' decision is coming from the previous pipelined stage starting half-cycle earlier. The operation of the proposed look-ahead stage is shown in Fig. 4(a). The look-ahead decisions generate the radix-1.6 residue signals. The input stage generates the MSB which is also the look-ahead decision for the first pipelined stage. The compare-with-zero operation inside each regular pipelined stage is replaced with two earlier comparisons (whose references are set by an inverse residue transfer function) and a selection (using a multiplexer) in a look-ahead stage. Fig. 4(b) shows the associated timing of the stage; the sub-ADC's regeneration time $(t_{\rm latch})$ is eliminated from the hold time and is moved to the sample time. Such a look-ahead architecture has been previously used to achieve higher sample rates without taking advantage of the linear residue settling. By employing the look-ahead structure in addition to the digital reference calibration, the architecture enables substantial improvement in the sample rate. Section IV-A discusses the simulated comparisons.

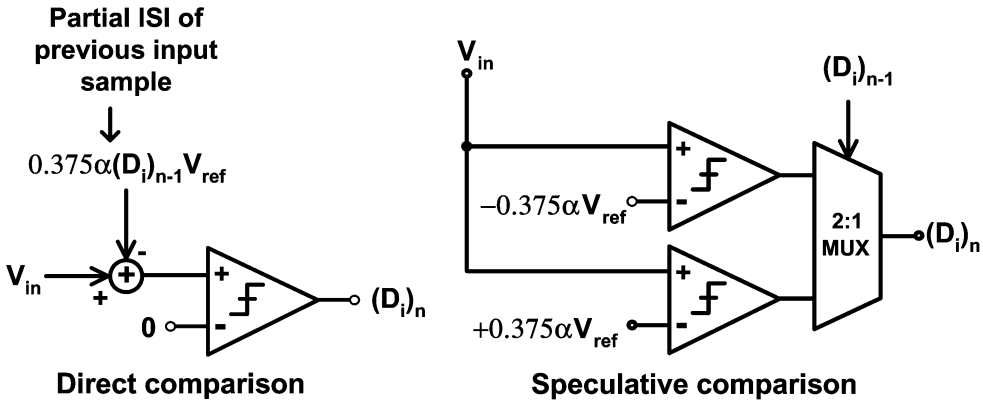

Fig. 7. Direct comparison versus speculative comparison.

C. DFE Architecture

The proposed ADC features an embedded multi-level DFE which uses the quantized decision of the previous symbol to subtract the first post-cursor ISI that results from the limited bandwidth of the communications channel. Shown in Fig. 5, the proposed equalizer is suitable for equalizing transmitted M-PAM or binary signals. In the case of the binary signaling, the proposed equalizer can be viewed as a pre-equalizer filter (similar to an IIR filter) and might be followed by digital equalizers to cancel the remainder of the ISI. Such an early ISI reduction reduces the required ADC resolution because the resolution of the ADC depends on the amount of the remaining ISI that needs to be cancelled by the subsequent digital equalizers [17], [18].

To implement the DFE with analog subtraction, the ISI of the previous input should be subtracted from the current input. The subtraction should be completed before the next input arrives, hence imposing a challenging feedback delay requirement [3], [4] especially if the signals involve multiple decision levels [9]. The timing requirement is prohibitive when implementing a mixed-signal DFE with a flash ADC due to the long settling time of both the ADC and DAC:

$$\text{ADC settling time} + \text{DAC settling time} + \text{adder delay} < \text{symbol time (208 ps)} \quad (1)$$

In a pipelined implementation, the ISI, which is proportional to the previous decision, can be subtracted across multiple clock cycles as the signal passes through each pipelined stage. Because each stage only resolves a few bits (< 1 in this design), the settling time for the sub-ADC and the sub-DAC is considerably shorter. Unlike a previous implementation [9], Fig. 6 shows that in our proposed DFE the digital outputs of each stage is feedback to the input of the stage of the next interleaved ADC to subtract the ISI. The comparator at each stage resolves its input after the partial subtraction of the ISI and therefore larger DFE taps than [9] are possible due to smaller amount of residual ISI. The feedback delay requirement is:

$$\text{sub-ADC settling time} + \text{sub-DAC settling time} + \text{adder delay} < \text{symbol time (208 ps)}. \quad (2)$$

Because of the high sampling rate, the feedback delay requirement is still challenging. To improve the feedback delay, instead of dissipating more power in the sub-ADC and sub-DAC to meet the delay requirement, this paper proposes adopting speculation in the feedback [4], [19]–[21][1]. As shown in Fig. 7, to subtract the partial ISI at the input of each pipelined stage, $0.375\alpha(D_{\rm i})_{\rm n-1}V_{\rm ref}$ needs to be subtracted from $V_{\rm in}$, where $(D_{\rm i})_{\rm n-1}$ denotes the coarse decision of the previous input sample (with i and n being the stage and input sample number, respectively). Once the partial ISI subtraction is finished, the comparators regenerate toward $(D_{\rm i})_{\rm n}$. Instead of requiring $(D_{\rm i})_{\rm n-1}$ to be determined before $(D_{\rm i})_{\rm n}$, since $(D_{\rm i})_{\rm n-1}$ must be a decision of either $-1{\rm or}+1$, two comparators can be used with the two possible comparison references. The proper decision result is selected after $(D_{\rm i})_{\rm n-1}$ arrives using a 2:1 multiplexer.

It is important to note that while the speculation can relax the feedback delay requirement, applying it directly to a flash ADC is still not feasible. The area, the input capacitance and the power consumption increase exponentially with the number of bits. For example, to implement a 1-tap DFE in a 5-bit flash ADC, 32 possible ISI values of the previous symbol need to be computed and compared with the input. A pipeline architecture enables a "per-stage" speculative DFE where the speculation is applied only to the partial ISI values with substantially fewer speculative values. The per-stage speculative DFE relaxes the DFE feedback delay requirement to

$$\text{Propagation delay} + \text{MUX delay} < \text{symbol time}. \quad (3)$$

A remaining issue with using a per-stage ISI subtraction to implement a DFE is that the output of each stage has residual ISI that needs to be subtracted at a later stage [9]. The residual ISI results in two effects. First, the residual ISI is similar to an effective data-dependent comparator offset whose absolute value does not exceed $\alpha V_{\rm ref}$. With the ISI being a data-dependent offset, the ADC characteristics changes dynamically and generates decision errors. Second, the residual ISI causes the output of each stage to exceed the assigned dynamic range of the subsequent stage. Consequently, the input signals with different values become indistinguishable by the ADC because they all result in the over-range residues generating similar output codes.

[1]Speculative DFE is also known as "partial-response DFE" or "loop-unrolled DFE". We use the term "speculative DFE" to avoid confusion with "look-ahead pipeline ADC" or "partial-response signaling".

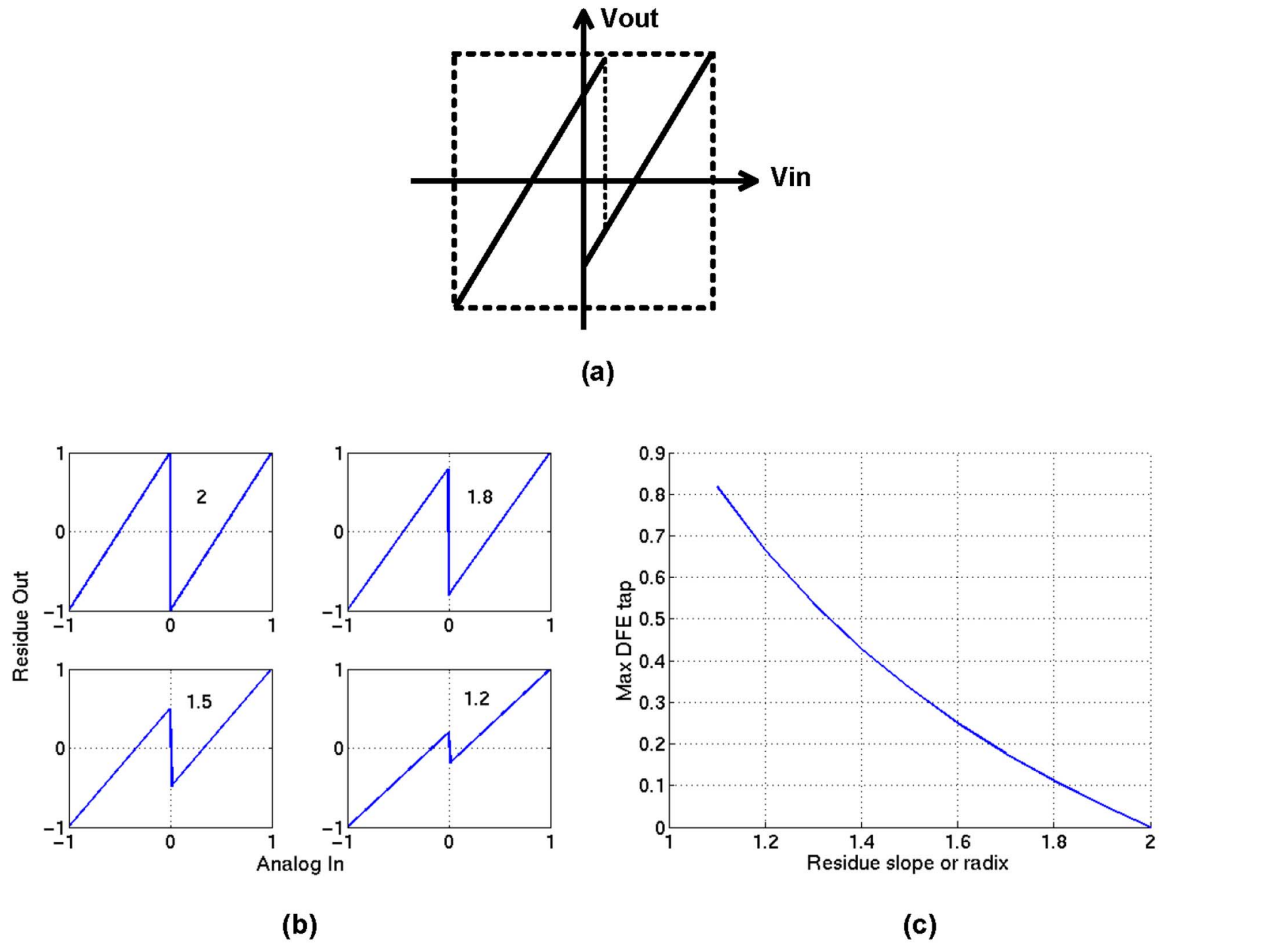

Fig. 8. (a) In a reduced-slope (radix) stage, the residue signal remains in range despite ISI, (b) various residue characteristics with different slope ($K_{\rm slope}$) values and (c) maximum DFE tap coefficient versus the slope value.

As shown in Fig. 8(a), the reduced-radix pipelined stages keep the signals in-range despite the presence of the ISI. The smaller the slope of the reduced-radix transfer function, the larger the ISI that can be absorbed (Fig. 8(b) and (c)). In this architecture, comparators are designed with digital offset correction. Residual comparator offsets will reduce the maximum tap-weight that can be programmed. Radix-converters are necessary afterwards to hide the residual ISI from the output codes. Fig. 9 shows such a radix converter where $K_{\rm slope}$ is the slope of the residue plot. By using radix-1.6 stages and per-stage ISI speculation, the tap-weight is adjustable from 0 to 0.4.

Fig. 10 illustrates the reference signals and the stage operation of the input T/H and the first stage of the time-interleaved ADC with the look-ahead decisions and the speculative DFE. Identical pipelined stages are used in this design. Adjusting α sets the DFE tap coefficient. The ADC would operate as a regular ADC by setting α equal to 0.

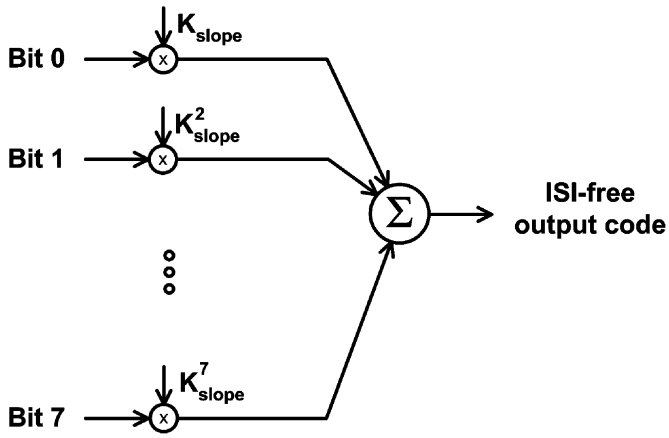

Fig. 9. Radix converter for reduced-radix pipelined stages.

III. Circuit Implementation

This section first describes the implementation of the building blocks of the proposed ADC and then shows the additional circuitry that is needed to implement the DFE. The ADC's input stage has a pseudo-differential architecture while the subsequent six identical pipelined stages and the final comparators are all fully differential. The figures, however, show the single-ended versions for clarity. Each circuit uses a 1.2-V power supply and has been implemented in a 0.13 μm CMOS technology.

A. Input Stage

Fig. 11 shows the input stage which consists of a bootstrapped sampling switch that tracks and then holds the input signal on a

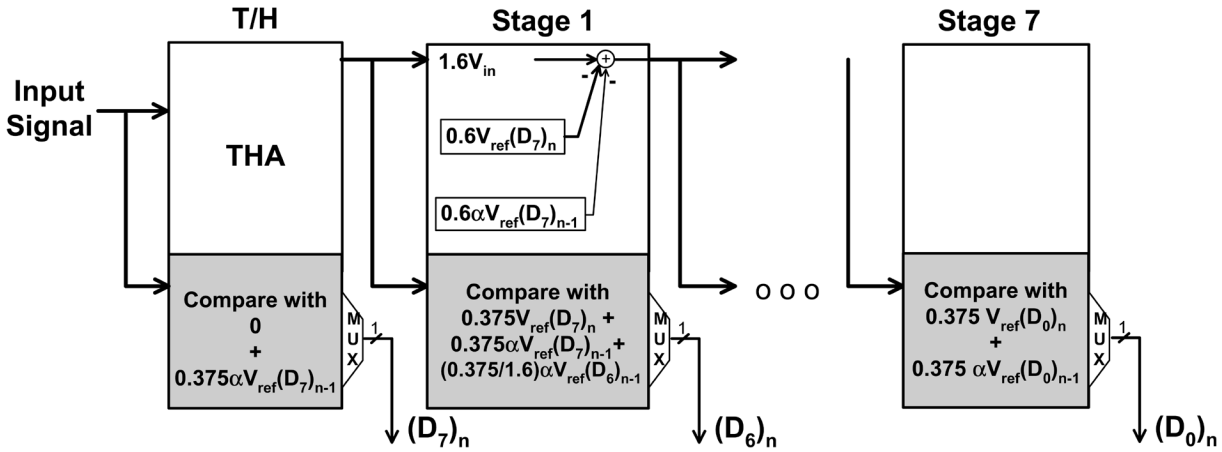

Fig. 10. Operation of each time interleaved ADC with the look-ahead decisions and the per-stage speculative DFE.

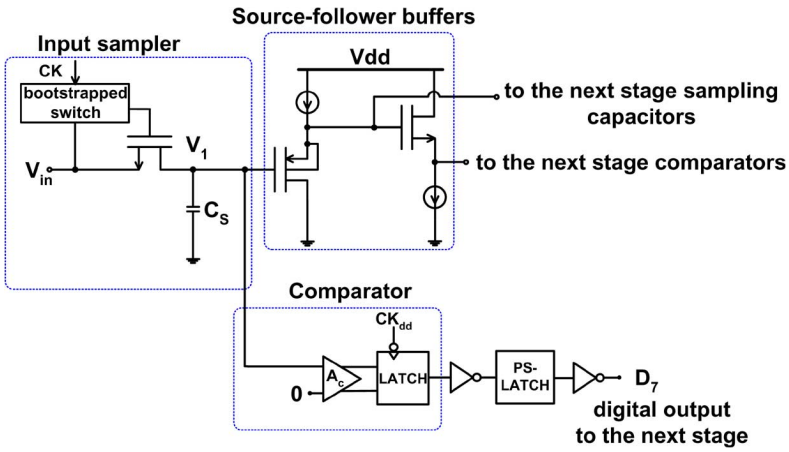

Fig. 11. Input stage.

sampling capacitor, two source-follower buffers that provide a steady input for the subsequent pipelined stage and a comparator which generates the MSB of the output code (look-ahead input bit for the first pipelined stage, as well).

The bootstrapped switches are used to achieve an input sampling bandwidth of 6 GHz such that the ADC can be used as part of a highly interleaved architecture up to 10× interleaved for 12 GS/s. A bootstrap capacitor is charged to $V_{\rm on}$ ($\sim$ 1.0 V) and is then connected between the gate and the source of the sampling switch during the tracking mode providing a relatively constant $V_{\rm GS}$ for the sampling switch. The sampling switch shows better than 9-bit linearity for input frequencies up to 6 GHz. With the differential input signal range being 0.5 $V_{\rm pp}$ and an input common-mode voltage of 0.15 V, the switch shows better than 6 GHz sampling bandwidth. The rms value of the kT/C noise associated with the 40 fF sampling capacitor is only 0.3 mV which is less than 2% of the 5-bit LSB. The bootstrapped switch also reduces the impact of the differential switch charge injection on the sampled value. Finally, it allows an input-independent sampling moment assuming the switch is turned off with the bootstrap capacitor still between the gate and the source.

In addition to sampling the large-bandwidth input, the T/H also has to provide a steady input for the succeeding pipelined stage. Source follower buffers have been widely used for this purpose [22]. Most designs use a single source-follower buffer (usually with a PMOS input pair to avoid the body effect related errors). A source follower buffer has a finite settling time-constant. Upon entering the hold mode, it needs additional time to settle to the final value as well as to recover from the large output variations arising from the switching of the capacitors of the succeeding pipelined stage. Assuming a 40 fF sampling capacitor (C_S) and a 124 fF load capacitor (C_L), a PMOS source follower alone could not settle to 5-bit accuracy when the sampling frequency is above 1 GS/s. The THA time-constant could not be improved beyond that even by increasing the bias current as it required an increase in W/L of the input and the load devices, which then resulted in an increased load capacitance.

To achieve faster settling, this design uses a cascade of two source follower buffers. The first buffer is a PMOS source follower which accommodates the 0.15 V input signal common-mode voltage. This buffer drives the sampling capacitors of the next pipelined stage (96 fF) as well as the input capacitance of the second buffer (5 fF). The buffer is fast enough to settle to 4.3-bit accuracy as is needed by the subsequent pipelined stage. The second THA which is an NMOS source follower buffer only drives the input capacitance of the comparators of the next stage (28 fF). The difference in the low-frequency gains of the two

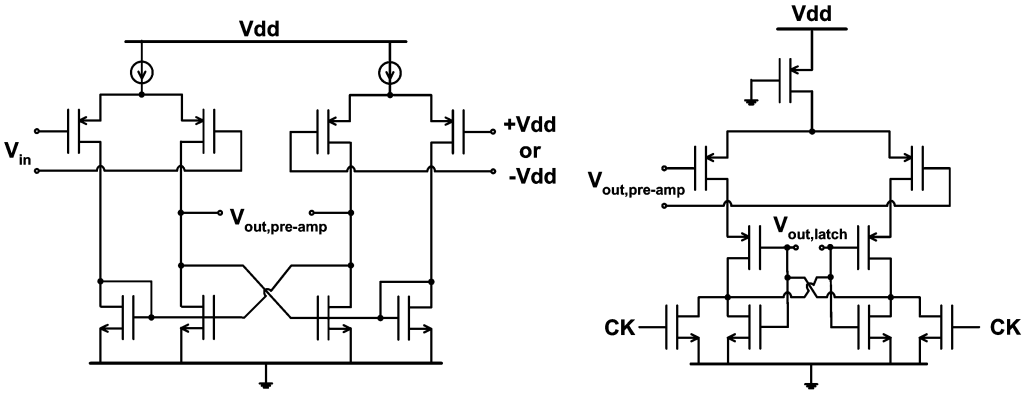

Fig. 12. Comparator architecture.

paths, i.e., from the input signal to the sampling capacitors of the first pipelined stage and from the input signal to the comparators of the first pipelined stage is corrected using digital reference calibration. The body effect of the NMOS source follower translates into a signal-dependent gain and consequently to a voltage offset at the input of the comparators of the first pipelined stage. This offset is however very small compared to the offset tolerance of the reduced-radix pipelined stages and thus is easily absorbed.

The comparator of the input stage generates the MSB of the output code. The comparator starts the regeneration after 150 ps into the hold time to ensure that its input has become stable. To suppress the kickback noise from the comparator's outputs into the sampling node, the comparator uses a pre-amplifier stage prior to the output latch stage (Fig. 12). To make sure that the MSB is available to the subsequent pipelined stage during an entire clock cycle, a pseudo-static latch (PS-latch) is used after the comparators [23].

B. Switched-Capacitor MDAC

Fig. 13 shows a single-ended detailed view of the pipelined stage which uses a closed-loop switched capacitor network to implement the radix-1.6 residue characteristics. The operation of the pipelined stage is similar to [10]. The sampling capacitor, C_S, is 60 fF. Since digital reference calibration can correct the gain errors, 5-bit matching between the sampling capacitors is not crucial. However the size of the sampling capacitors should be selected in accordance with the size of other capacitors (the input and the output capacitance of the amplifier and the parasitic capacitance of the switches) to ensure a residue gain close to 1.6 to set a good initial condition for the calibration procedure. Note that unlike [14], an additional switch in our design (S1 in Fig. 13) prevents the asymmetric clock feedthrough from arriving at the amplifier's input. The clock feedthrough due to S1 is a common-mode glitch and is absorbed by the fully differential architecture. Each MDAC uses a folded-cascode amplifier topology providing a low-frequency gain of ~ 58 while dissipating 5 mW of power consumption. The low-frequency gain was determined from the required closed-loop gain linearity to achieve 5 ENOB at 1.2 GS/s.

The amplifier uses a switched-capacitor passive common-mode feedback (CMF) architecture. To ensure fast common-mode settling, the CMF circuitry uses complementary switches. The common-mode feedback capacitor is 50 fF.

C. Digital Reference Calibration

Adjustable references are needed for digital reference calibration. Both MDAC and comparators' references need to be adjusted correspondingly. This design uses an 8-bit binary-weighted segmented DAC to adjust each reference. The comparators and the MDAC can be adjusted individually however they share the first two MSBs of the adjustment signal.

D. Memory Effect Reduction With Capacitor Pre-charging

A side effect of using pipelined stages at the very high sampling rate of 1.2 GS/s is the memory effect error [14]. Memory effect can be considered as interference from the previous inputs of a pipelined ADC on the current input akin to the idea of inter-symbol interference (ISI) in a communications link. In a switched-capacitor pipeline ADC, such errors are generated from two different mechanisms.

The first mechanism is incomplete resetting of the residue-amplifiers in the sample mode. The second mechanism shows up during the hold mode. Consider two consecutive pipelined stages. When the first stage is in the sample mode, the succeeding stage is amplifying its input which is the previous output signal of stage one $(V_{\rm out}(nT-T))$. As soon as the first stage enters the hold mode to generate $V_{\rm out}(nT)$, the sampling capacitors of stage two are switched back to stage one carrying some initial charge which consequently introduces an initial voltage which depends on previous output $V_{\rm out}(nT-T)$. In a pipeline ADC with unfinished residue settling, such initial voltage may introduce memory effect errors in the residue.

Since the reset time-constant is usually much smaller than the hold time-constant, the memory effect errors due to the incomplete resetting are usually secondary and can be made insignificant through good circuit design. This design addresses the errors injected from the subsequent stage with a capacitor pre-charging technique.

As shown in Fig. 14, the interference due to the memory effect error is proportional to the previous input $(V_{\rm in}(nT-T))$ and can cause deterministic errors as large as 4% of the maximum signal swing of the pipelined stages when sampling at 1.25 GHz (simulation results). To suppress the memory effect errors, a short reset cycle can be added after the hold time to discharge the

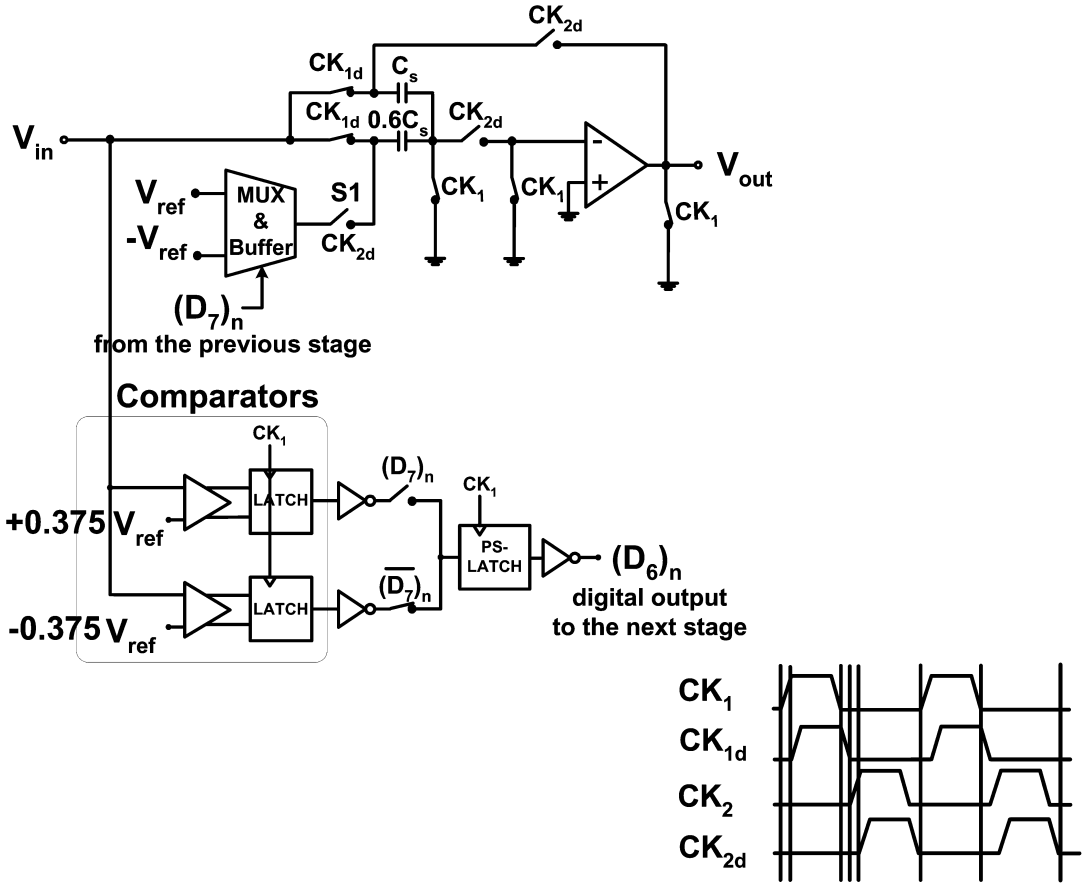

Fig. 13. Simplified single-ended illustration of the first pipelined stage of the proposed ADC (DFE disabled) and the clock signals.

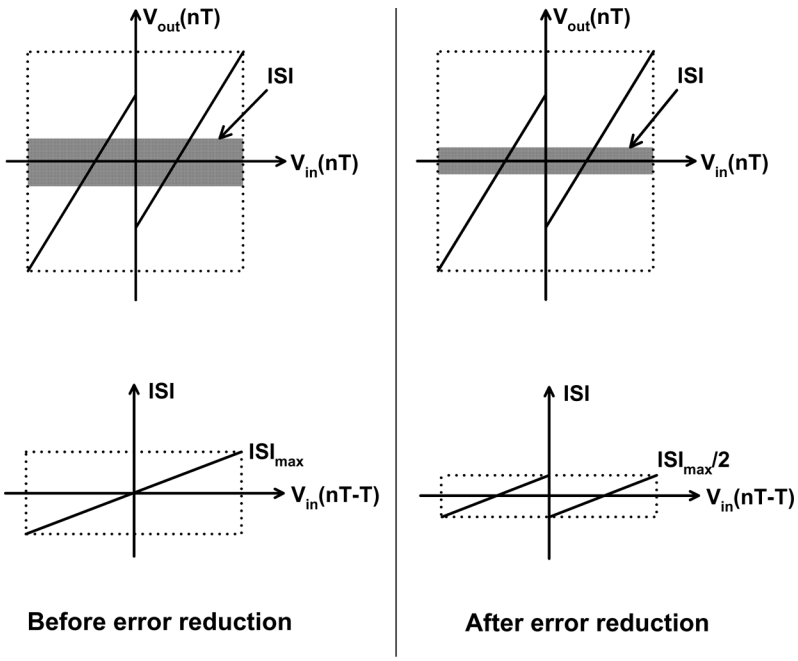

Fig. 14. Memory error reduction after subtracting the MSB portion of the ISI.

sample/hold capacitor [14]. The approach is not suitable for our application due to the speed penalty. This paper proposes a capacitor pre-charging technique to reduce the memory effect errors of the previous samples by a factor of two.

Our technique uses the sign of $V_{\rm in}(nT-T)$ which is available from the look-ahead decision and coarsely subtracts the interference. As shown in Fig. 15, the capacitor pre-charging technique uses the look-ahead decision to pre-charge and then release the

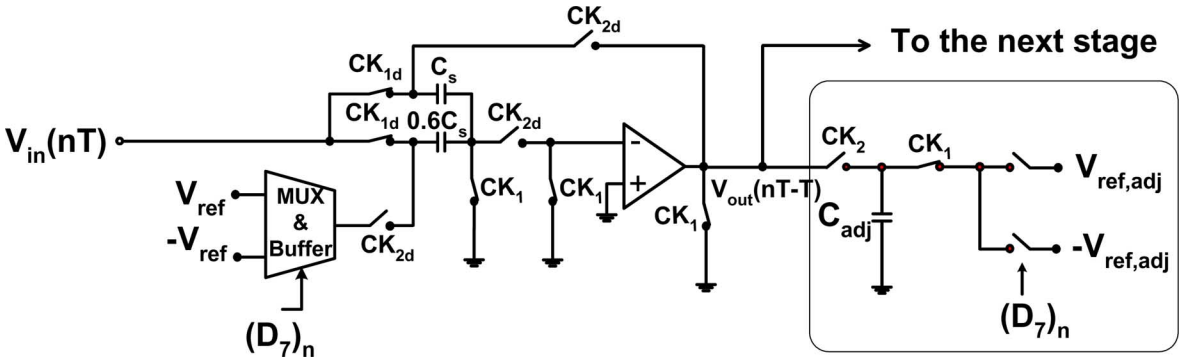

Fig. 15. The proposed capacitor pre-charging technique (shown for the first pipelined stage) to suppress the memory effect errors.

charge of auxiliary capacitors $C_{\rm adj}$ into the amplifier's output. A compensating charge proportional to $V_{\rm ref,adj} \times C_{\rm adj}$ is injected. The size of $C_{\rm adj}$ can be chosen small to minimize the capacitive loading. $V_{\rm ref,adj}$ can be adjusted digitally similar to the other adjustable references.

An alternate method to correct the memory effect errors is to use the inherent equalization of the system. The memory effect errors can be observed as the ISI of the previous symbols and thus can be cancelled by equalization. This approach is particularly useful when memory effect errors are larger than the error correction limits of the capacitor pre-charging technique. In this design, however, the memory effect errors are small and thus are corrected using capacitor pre-charging.

E. DFE Circuits

To implement the stage-by-stage DFE, an additional capacitor in each pipelined stage subtracts the partial ISI by releasing a charge of $+C_{\rm DFE}V_{\rm ref,DFE}$ or $-C_{\rm DFE}V_{\rm ref,DFE}$ depending on the received data from the previous row similar to [9]. $V_{\rm ref,DFE}$ (and consequently the DFE tap coefficient) is set by 8 bits of digital adjustments. Speculative decisions are generated using additional comparators. Fig. 16 shows the first pipelined stage along with the additional circuitry for the DFE implementation.

IV. Performance Analysis

Using digital reference calibration, the look-ahead architecture and memory effect cancellation, the simulated ADC can achieve 5 ENOB when sampling at 1.25 GS/s. This section first describes the performance improvements from using the proposed techniques. The residual nonlinearity that limits further speed-up is discussed in Section IV-B.

A. Performance Comparison

Simulation results showed that the maximum clock frequency (to achieve 5 ENOB) for a conventional pipeline ADC which uses none of the high-speed techniques introduced in this paper but uses the same core amplifiers and comparators is only 500 MS/s. The upper bound on the sampling frequency is limited by the accurate residue-settling requirement. The residue settling includes the settling of both sub-ADC and the residue-amplifiers. Digital reference calibration alone is not capable of dramatically improving the sampling frequency due to the nonlinearities of the settling response. Once the typical ADC is modified to a look-ahead pipeline converter, the maximum sampling frequency is improved to 800 MS/s (60% improvement) assuming complete residue settling. Because the look-ahead architecture provides a more linear residue characteristics, the sampling frequency of the look-ahead pipeline ADC can be increased to 1.25 GS/s with proper calibration and memory effect cancellation (an additional 56% improvement from 800 MS/s). The performance of the calibrated ADC is eventually limited by the remaining nonlinear error sources and the memory errors.

B. Linearity Analysis

To characterize the residual nonlinearity, the residue plot of one pipelined stage is simulated (at various sampling frequencies) and is compared with a linear (ideal) residue characteristics based on a first-order least-square polynomial curve fit. The residue linearity, expressed in terms of $B_{\rm max}$, is determined from the maximum difference between the two characteristics $(\max(\Delta V))$ and the maximum signal swing $(V_{\rm max})$:

$$\frac{0.5}{2^{B\,\max}} = \frac{\max(\Delta V)}{V_{\rm max}}. \tag{4}$$

Because digital reference calibration can correct the linear errors, $B_{\rm max}$ is an indicator of the maximum possible ENOB that can be achieved by the remaining pipelined stages [24]. The total achievable ADC ENOB is determined by summing the $B_{\rm max}$ of the first pipelined stage with the number of bits out of that stage and the input T/H stage. Note that the input stage (T/H) of the pipeline ADC is designed with sufficient linearity so as not to limit the overall ADC.

Residual nonlinearities of our proposed architecture are from three main sources: 1) nonlinear errors of the residue amplifier in the hold mode, i.e., the nonlinear gain error at low sampling frequencies and the nonlinear settling errors at high sampling frequencies, 2) nonlinear errors of the sampling capacitors and the switches of the pipelined stage in the sample mode, and 3) the nonlinear errors caused by variations of the look-ahead path delay when extending into the hold time at high sampling frequencies.

The nonlinear errors of the residue amplifier in the hold mode are due to the open-loop gain nonlinearity showing up in the closed-loop residue characteristics because of the finite gain of the amplifier. Simulation results showed that the open-loop low-frequency gain $(A_{\rm open})$ of the amplifier in this design varies

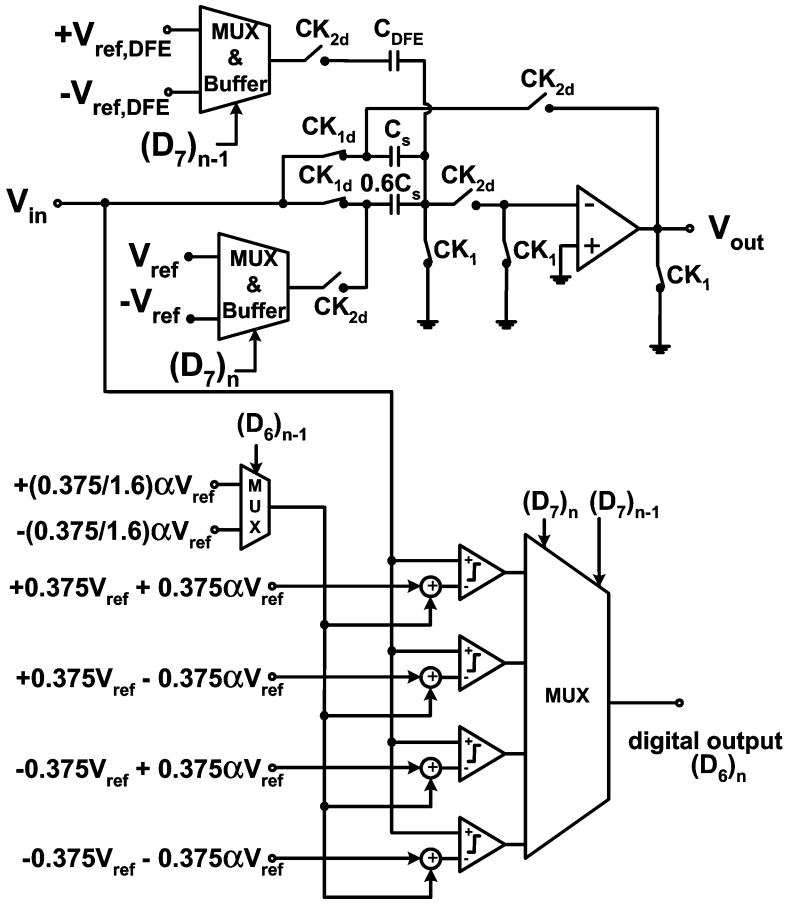

Fig. 16. The first pipelined stage along with the additional circuitry for DFE implementation.

between 58.30 and 58.56 depending on the input/output amplitude. This corresponds to $\sim$6.8-bit open-loop linearity. The gain desensitization from the feedback loop attenuates the nonlinearity [16]:

$$V_{\text{out}} = (1.6V_{\text{in}} - 0.6D_{\text{in}}V_{\text{ref}})\frac{A_{\text{open}}}{A_{\text{open}} + \left(1.6 + \frac{C_{\text{in}}}{C_S}\right)} \tag{5}$$

$$\Delta\left[\frac{V_{\text{out}}}{1.6V_{\text{in}} - 0.6D_{\text{in}}V_{\text{ref}}}\right] = \Delta\left[\frac{A_{\text{open}}}{A_{\text{open}} + \left(1.6 + \frac{C_{\text{in}}}{C_S}\right)}\right]$$

$$\cong \Delta A_{\text{open}} \times \frac{\left(1.6 + \frac{C_{\text{in}}}{C_S}\right)}{\left(A_{\text{open}} + \left(1.6 + \frac{C_{\text{in}}}{C_S}\right)\right)^2} \tag{6}$$

where $\Delta A_{\text{open}} = 58.56 - 58.3 = 0.25$ shows the maximum open-loop gain variations. Assuming $C_{\text{in}}/C_S = 1$, (6) results in $\Delta\left[V_{\text{out}}/1.6V_{\text{in}} - 0.6D_{\text{in}}V_{\text{ref}}\right] = 1.9\times10^{-4}$ which corresponds to 11.4-bit closed-loop linearity. As the sampling frequency is increased toward the GS/s regime, the effective open-loop gain becomes smaller due to incomplete settling resulting in less effective gain desensitization. This is shown in Fig. 17.

Nonlinear errors of the sampling switches are due to the input-dependent ON resistance of the switches which result in a variable sampling time-constant. These errors appear in the output residue and are boosted at high sampling frequencies when the sample time becomes comparable with the sampling time-constant.

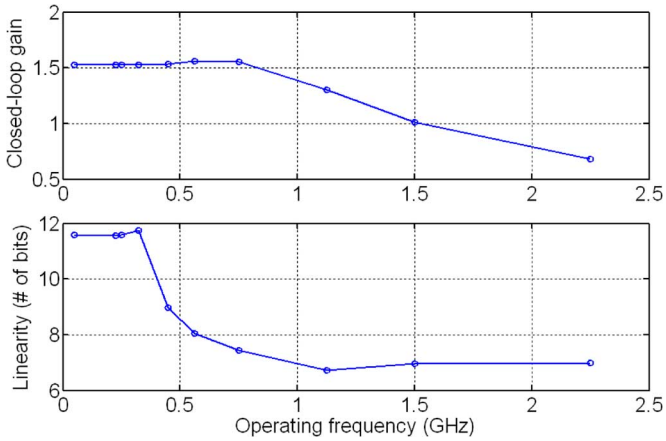

Fig. 17. Effective closed-loop gain of the switched-capacitor MDAC versus the operating frequency and the linearity of the output residue due to amplifier's finite gain.

Finally, the feedforward path delay variation also contributes to the nonlinearity of the residue characteristics. The amplifier in a look-ahead stage needs the look-ahead bit from the preceding stage, to select the correct reference ($+V_{\text{ref}}$ or $-V_{\text{ref}}$), before it can settle to the final residue value. Late arrival of the look-ahead bit delays the amplifier's settling and more importantly,

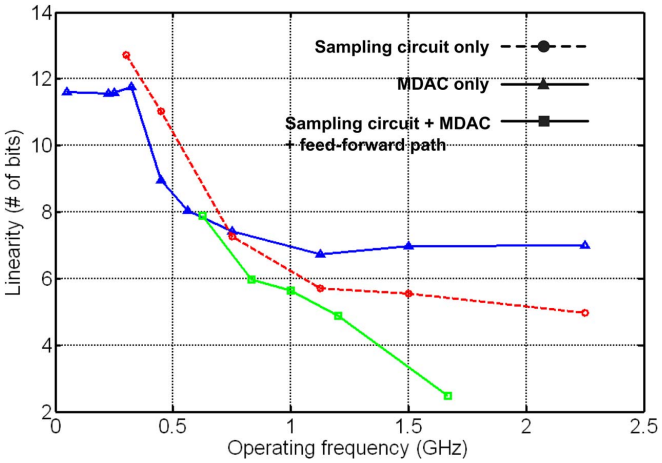

Fig. 18. The residue linearity in terms of the remaining number of bits versus the operating frequency.

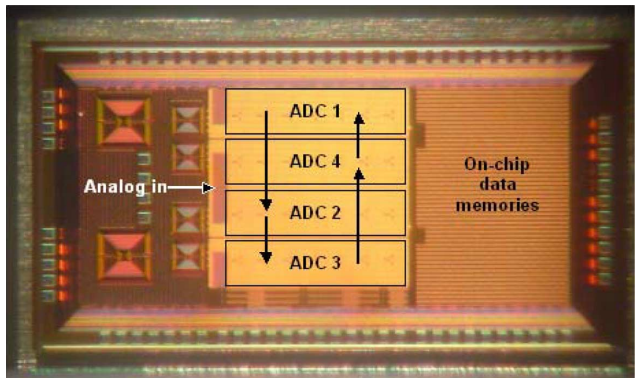

Fig. 19. Die photo. (Size of the ADC core is 1.3×1.3 mm^2).

the delay is input-dependent. This input dependence introduces nonlinearity in the output residue.

Fig. 18 shows the simulated plot of the linearity of the pipelined stage residue versus the sampling frequency. In summary, at low sampling frequencies up to $\sim$560 MS/S, the linearity is better than 8 bits and is mostly limited by the linearity of the MDAC residue amplifiers. Between 560 MS/s and 1.2 GS/s, the nonlinearity errors of the sampling circuit are dominant and drop the linearity down to $\sim$4.9 bits at 1.2 GS/s. After that point, the feedforward path delay starts to extend into the hold time and the nonlinearity grows very quickly because the feedforward delay's time-overlap with the hold time becomes larger. At 1.6 GS/s only 2.5-bit linearity is possible. Note that the simulation setup for Fig. 18 is such that the load capacitor of the pipelined stage is discharged before connecting to the output of the pipelined stage therefore memory effect errors do not appear in the plot.

At 1.25 GS/s, the linearity of the pipelined stage is 4.6 bits. Taking into account the memory effect errors (with a maximum error of 2% of the stage output swing after error reduction), a total of 5 ENOB is possible at 1.25 GS/s after including the 2×0.7 bits[2] 0.7 bits coming from the T/H and the first pipelined stage.

V. Experimental Results

The die photo of the entire ADC with DFE is shown in Fig. 19. The ADCs are placed in such an order to minimize the maximum DFE path. The raw bits out of each ADC are stored in an on-chip memory with a depth of 2000 samples and are later processed off-chip.

To characterize the ADC, first the DFE is disabled and each time-interleaved ADC is calibrated. A low-frequency input sinusoid is applied and all pipelined references are digitally adjusted until the maximum SNDR is achieved [10]. For each ADC, 13 adjustments (6 MDAC references and 7 comparators) are needed to fully calibrate at each sampling frequency. Each comparator and MDAC reference uses 8 adjustment bits sharing the first two MSBs. Given the 6 seconds dumping time from the on-chip memories, an open-loop calibration (which examines the output SNDR for all reference values and picks the maximum) is impractical. A recursive calibration algorithm is used instead; as shown in Fig. 20, the calibration starts with the coarse adjustment of the first two pipelined stages (the input T/H needs no adjustments). Then the third stage is tuned toward the maximum output SNDR. In the next step, the first three stages are finely adjusted simultaneously until the maximum SNDR is achieved. The calibration continues with the coarse adjustment of the fourth stage and so on. MATLAB simulations confirm the convergence of this algorithm to the maximum SNDR under the assumption that at each step, the SNDR metric only uses the output bits of the pipelined stages that are being adjusted at that calibration step or have been adjusted in the previous steps. For example in the first step, only D_7, D_6, and D_5 are used to calculate the output SNDR.

After calibrating each individual ADC, digital reference calibration is then used to correct the gain mismatch between the paths.

Multi-phase clocks for the time-interleaved ADC are generated from an external pulse generator. Adjustable resonant clock buffers are used to distribute the clock signal to each ADC. A digital calibration technique reduces the clock skew between channels to <1 ps [25].

The overall ADC achieves 30.4 dB of SNDR for low-frequency input signals when sampling at 4.8 GS/s and dissipating 300 mW from a 1.2 V supply. This number includes the power consumption of the reference buffers. The SNDR would improve to 34 dB when sampling at 2.4 GS/s. The differential input signal swing is 500 $\mathrm{mV_{pp}}$. At 4.8 Gs/s, the amplifiers only settle to 75% of the final value.

Integral nonlinearity (INL) and differential nonlinearity (DNL) plots are shown in Fig. 21. When digitizing a 1.2 MHz input signal the maximum DNL is less than 0.55LSB, and the maximum INL is below 0.65LSB. The input capacitance of each time-interleaved ADC is only 52 fF.

Dynamic performance of the ADC is shown in Fig. 22. The measured effective resolution bandwidth (ERBW) is $\sim$6.1 GHz (limited by clock jitter and input sampling bandwidth) indicating the potential for more interleaving for higher sampling rates.

$$\mathrm{FOM} = P/2^{\mathrm{ENOB}} \times \min(2 \times \mathrm{ERBW}, \mathrm{fs})$$

[2]Each radix-1.6 generates $\log_2^{1.6} \approx$

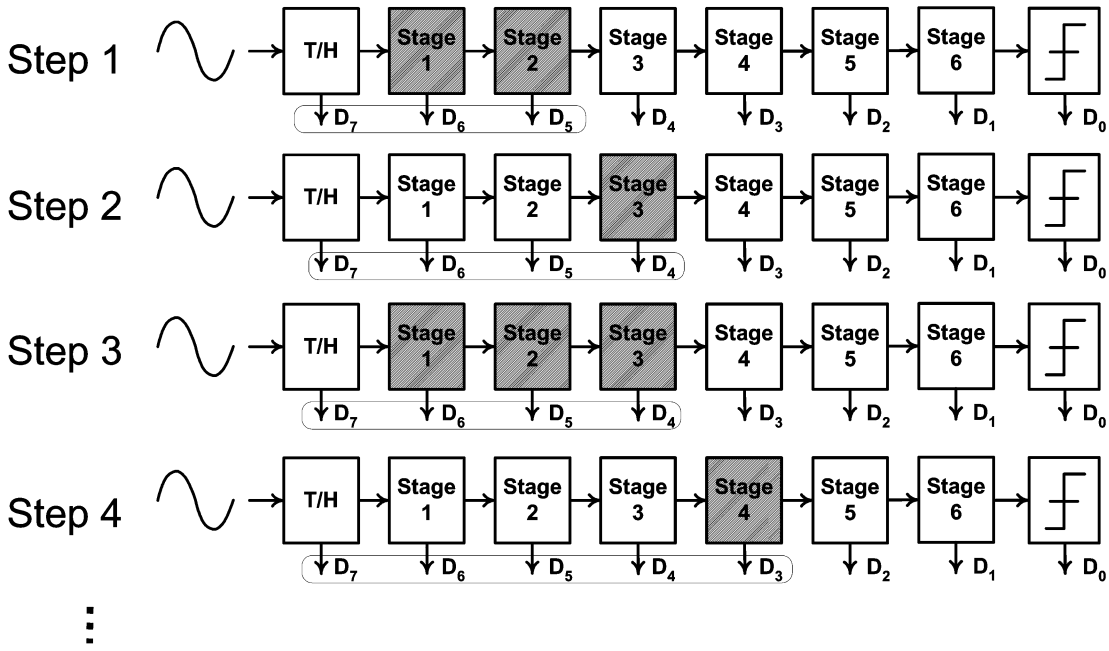

Fig. 20. Illustration of the calibration procedure.

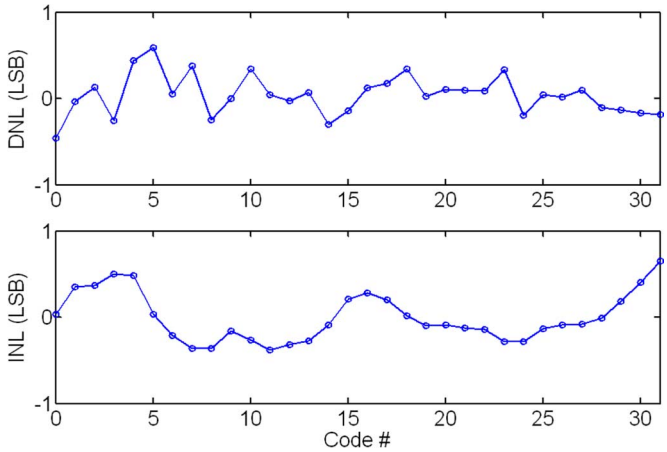

Fig. 21. DNL and INL plots with fin = 1.2 MHz at fs = 4.8 GHz. Maximum DNL and INL are 0.55 and 0.65LSB, respectively.

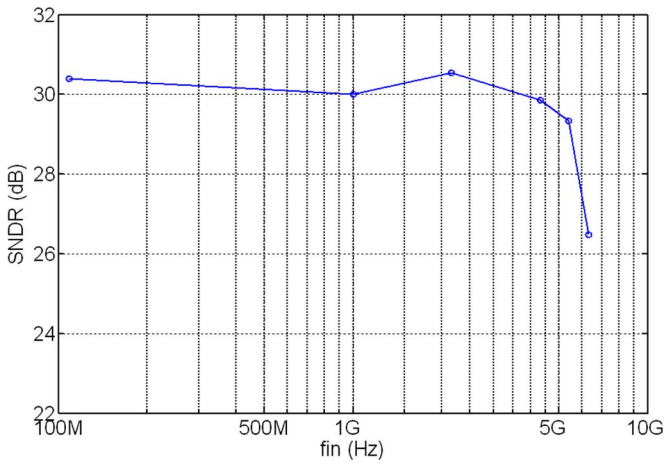

Fig. 22. SNDR versus the input frequency at fs = 4.8 GHz (DFE disabled).

is 2.3 pJ/conv-step at 4.8 GS/s. Table I compares the performance of this ADC with other high-speed ADCs. The table shows that a closed-loop pipeline ADC with our proposed techniques can surpass the power efficiency of an open-loop pipeline ADC even at very high sampling frequencies [11]. It also shows that the power efficiency of our ADC can be better than or comparable with high-speed flash ADCs in similar or slower CMOS processes [27], [30].

The performance of the DFE is verified using a partial-response (PR) sequence $(1 + 0.5D)$ sent to a low-pass channel comprising a 500 MHz power splitter which resembles a $1 + 0.25z^{-1}$ channel. The input sequence for DFE measurements is generated from summing a dual-channel pulse generator's outputs. The performance is characterized at 2.4 GS/s using the post-ADC digitized data with and without DFE. Note that as seen in Fig. 16, all DFE related reference values are proportional to ADC reference values and therefore share the same digital adjustment bits. The DFE tap coefficient is adjusted independently. Fig. 23 first shows the DFE disabled and the ADC sampling the received symbols at the optimal phase. The sampling time in this test chip is determined by adjusting the delay of the pulse generator with respect to the sampling clocks. As expected, the sampled results show a multitude of voltage levels corresponding to a closed eye. Fig. 23 then shows the DFE enabled with a tap coefficient of 0.25 to compensate the bandlimited channel. The 4 levels of the PR input sequence is recovered. Because the channel input has just 4 levels, the correct output of such a receiver would only toggle the first three stages of the pipeline ADC. Since in our measurements the ADC outputs are stored in an on-chip memory (with a depth of 8000 samples for the entire ADC) and given that each input symbol in this measurement consists of 2 data bits, the measurement results suggest that the DFE enables an error-free signaling for a stream of 16,000 consecutive input data bits.

TABLE I
PERFORMANCE OVERVIEW OF HIGH-SPEED ADCS WITH fs $\geq$ 1 GHz, ERBW $\geq$ 1 GHz, AND SNDR (LOW-FREQUENCY INPUT) $\geq$ 30 dB DATA EXTRACTED FROM JSSC, ISSCC, AND VLSI SYMPOSIUM

Author/ Year	ADC Architecture	CMOS Tech. Process (μm)	Sample Rate (GHz)	Resolution (bits)	SNDR (dB)	ENOB (bits)	Effective Resolution Bandwidth (GHz)	Power Consumption (mW)	Input Cap. (fF)	FOM (pJ/conv-step)
Poulton [12] (ISSCC 03)	Time-Interleaved Open-Loop Pipeline	0.18	20	8	41	6.5	1.9	5000	4000	14
Taft [26] (ISSCC 04)	Folding	0.18	1.6	8	47	7.5	1.1	1269	1.8	4.4
Paulus [27] (VLSI 04)	Flash	0.13	4	6	30 (SFDR)	4.7	N/A	990	N/A	9.6
Deguchi [28] (VLSI 07)	Flash	0.090	3.5	6	31.2	4.9	1.75	98	N/A	0.94
Louwsma [29] (JSSC 08)	Time-Interleaved SAR/ Pipeline	0.13	1.35	10	48.1	7.7	1	175	1000	0.6
Choi [30] (VLSI 08)	Flash	0.065	5	6	32	5.0	2.5	320	N/A	2
Nazemi [11] (VLSI 08)	Time-Interleaved Open-Loop Pipeline	0.090	10.3	6	36.6	5.8	5	1600	N/A	2.8
This work	Time-Interleaved Look-Ahead Pipeline with Calibration and Capacitor Pre-Charging	0.13	4.8	5	30.4	4.76	4	300	104	2.3

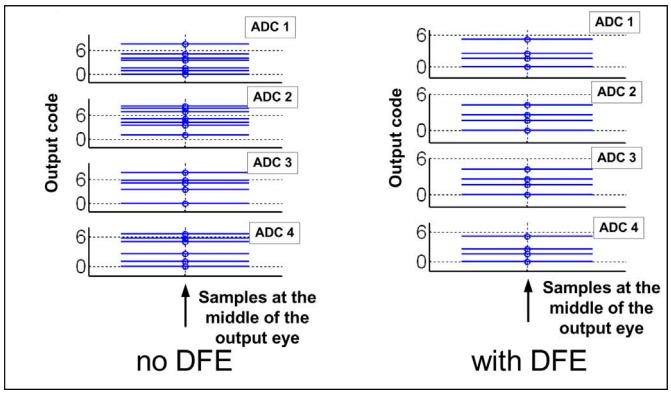

Fig. 23. Mid-point samples of the eye diagram without and with DFE, fs = 2.4 GS/s.

VI. CONCLUSION

This work demonstrates a multi-GS/s 4-way time-interleaved ADC for high-speed data transfer between ICs. The ADC can be used as the receiver in a multi-level signaling scheme or as part of an ADC-based receiver for binary signaling. Each time-interleaved ADC, running at 1.2 GS/s, uses a look-ahead pipeline architecture. At such a high sampling frequency, the residue amplifiers only settle to 75% of their final value. Using the look-ahead architecture, the incompletely settled residue remains linear allowing digital reference calibration to compensate the incomplete settling. A capacitor pre-charging technique reduces the memory effect errors. The ADC achieves 30.4 dB of SNDR.

The pipelined architecture allows implementing advanced digital signal processing techniques to counteract the system bandwidth limitations. This ADC features a stag-by-stage mixed-signal DFE which can reduce the ISI of bandlimited channels.

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