A 7.6 mW 1.75 GS/s 5 bit Flash A/D converter in 90 nm digital CMOS

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Abstract

A 5 bit 1.75 GS/s flash ADC is realized in 90 nm CMOS. It uses a comparator array with built-in imbalance and offset calibration to lower power consumption. The SNDR is 30.9 dB at low frequencies and gradually degrades to 28.2 dB at 2 GHz. The ADC occupies 280 µm by 110 µm and draws only 7.6 mA from a 1 V supply yielding an energy efficiency of 0.15 pJ/conversion step.
Keywords: ADC, flash, high speed

Introduction

For low-resolution, high-speed ADCs the flash architecture can yield an efficient implementation [1],[2]. These converters enable high speed operation, but as the required resolution goes up the number of comparators needed increases exponentially. By calibrating each comparator, the use of preamplifiers and averaging is avoided, matching requirements are relaxed and power consumption is drastically reduced.

Architecture

The proposed ADC architecture is shown in Fig. 1. The differential input is directly applied to the comparator array. Each comparator has a different intentional offset so that no reference levels have to be generated. Calibration is realized by applying a differential digitally controllable calibration voltage to a redundant input pair of each comparator. The calibration voltages are generated using a common resistive ladder and applied to the comparators using multiplexers. These are controlled by bits stored in a shift register.

The comparator outputs are buffered and then latched by a S/R latch and a digital track-and-hold (T/H) in order to increase the allowed encoding delay. The MSB is determined directly from the thermometer code by an OR gate. The 4 LSBs of the gray output codes are encoded after first order bubble error correction (by 3-input NANDs) in two split ROM encoders, of which only one is active each cycle to reduce power consumption.

Implementation

A. Comparator and Calibration

In this architecture the comparators are the critical components: power consumption, speed, offset and noise of the comparator will determine the overall ADC performance. The offset is caused by transistor mismatch, and as shown in [3] this mismatch can be reduced by using wider transistors, which increases power consumption but also decreases noise. Alternatively this offset can be cancelled using calibration. In this work the latter option has been preferred so that comparator sizing and hence power consumption is only determined by the required noise level and speed. Downsizing the comparators also yields a very low input capacitance of only 70 fF to ground for the complete ADC.

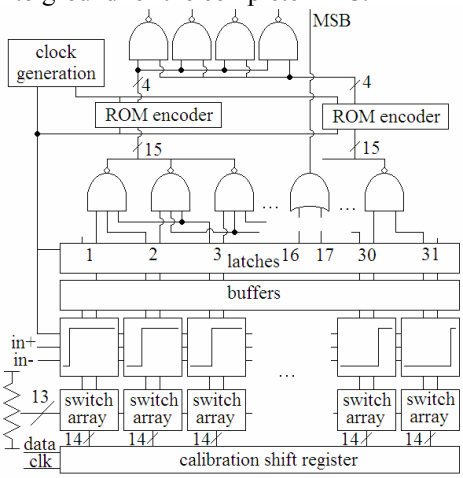

Fig. 1 Architecture of the ADC.

In this design the dynamic comparator in Fig. 2 (a) has been implemented. Transistors P3 are used for calibration (see further) and will be ignored for now. After a falling clock edge turns on the switch P1, the input transistors P2 will in a first phase charge the cross-coupled NMOS pair N1 with a slope dependant on the applied input voltage. In a second phase the N1 pair will regeneratively amplify any differential output voltage present after the first slewing phase up to a nearly rail-to-rail signal. After a rising clock edge, the output nodes are drawn back to ground using switches N2 while P1 is turned off. Imbalance is introduced in this comparator by using different widths for P2a and P2b, resulting in 16 different comparator sizings, 15 of which are mirrored and reused. This intentional imbalance replaces the reference voltages at the input of the comparators in a classical flash ADC architecture.

Calibration is achieved with transistor pair P3. Their current is added to the P2 current so that the slew rate in the first phase is no longer only dependant on the input voltage. By applying different voltages to the gates of these transistors, the effective offset of the comparator can be changed. A resistive ladder supplies 7 coarse and 7 fine calibration voltages and one of each is applied to the gates of P3 by multiplexers.

The resistive ladder has been constructed in standard N+ poly-Si (14 Ω / square) and consumes 100 µA of static current, which is the only static power consumption. Layout of both ADC inputs has been realized in matched metal trees, and the clock routing is realized in a similar tree to minimize timing errors and thus maximize the ERBW.

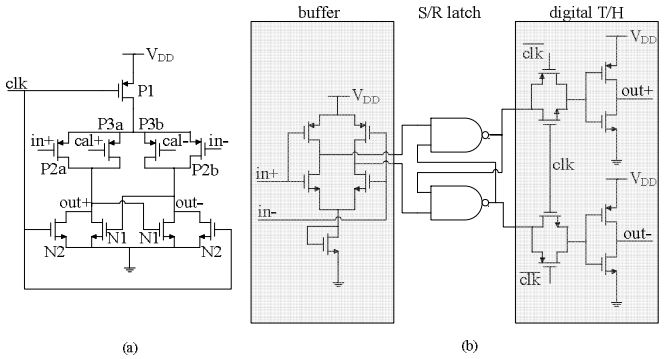

Fig. 2 Schematic of the comparator (a) and following stages (b).

B. Encoding

During the first phase of the comparison the output signals will go up to roughly halfway the supply voltage. To avoid transient currents in the next stage, a buffer is placed before the S/R latch. This buffer has a high input threshold, which is obtained by the use of a diode-connected NMOS transistor (see Fig. 2b). This prevents that a "short-circuit current" flows before the comparator has regenerated. After the S/R latch a digital T/H decouples the encoder from the comparator array for half a clock period to increase the allowed delay. These blocks are shown in Fig. 2 (b).

Each cycle the ROM encoder lines are precharged by PMOS transistors, and discharged by NMOS transistors when needed. Each NMOS transistor is controlled by one out of 30 signals (see Fig. 1) which is gated by the clock; the PMOS is controlled by a non-overlapping clock. By splitting up the ROM encoder into two parts the routing capacitance is halved and the junction capacitance is decreased (we need 8 NMOS, 1 PMOS instead of 16 NMOS, 1 PMOS for each encoder line). As each transistor now has a much smaller relative load to drive, the speed is greatly increased, even with the added delay of the NAND gate used to combine both encoders. All output bits of the ADC are brought off chip at full speed.

Measurements

Each comparator has been calibrated by applying the desired threshold voltage and stepping first the coarse and then the fine calibration voltage. When the comparator offset is close to the applied input voltage the comparator noise will dither the output and the best setting can be determined.

Maximum INL and DNL values before calibration are -1.0/+3.6 and -5.0/3.4 LSB and -0.07/+0.39 and -0.34/+0.38 LSB after calibration. SNDR and SFDR as a function of input frequency at 1.75 GS/s are shown in Fig. 3. The measured ENOB for different clock frequencies with an input frequency of 10 MHz is shown in Fig. 4.

Conclusions

A 5 bit 1.75 GS/s flash ADC in 90 nm digital CMOS has been presented. The ADC leverages comparator calibration to decrease power consumption. It achieves 4.85 ENOB at low frequencies and 4.6 at Nyquist frequency with the ERBW extending to 2 GHz. The ADC consumes only 7.6 mA from a 1 V supply voltage and thus achieves an energy efficiency of 0.15 pJ/conversion step.

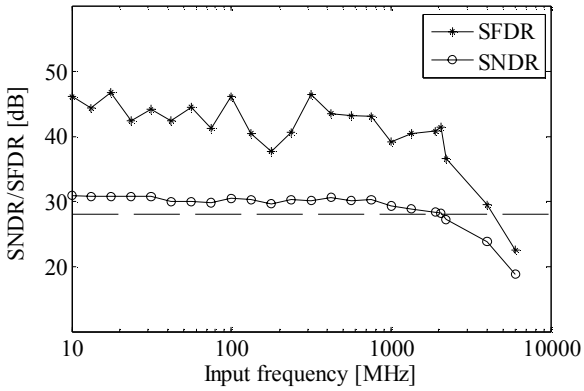

Fig. 3 Measured SNDR and SFDR.

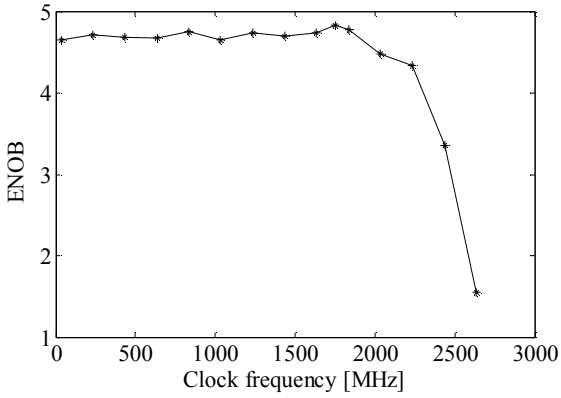

Fig. 4 ENOB with 10 MHz input signal vs. clock frequency.

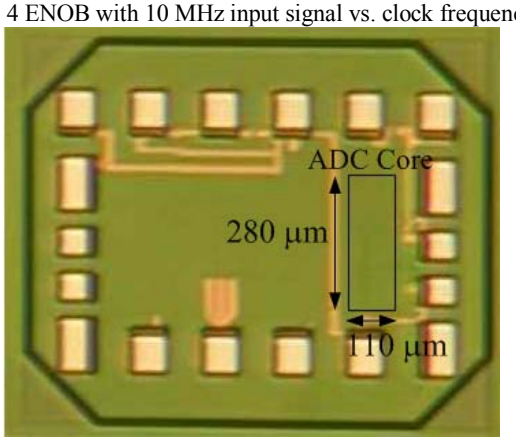

Fig. 5 Chip micrograph.

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