A Background Self-Calibrated 6b 2.7 GS/s ADC With Cascade-Calibrated Folding-Interpolating Architecture

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***Abstract*—We have developed a 6b 2.7 GS/s folding ADC with on-chip background self-calibration in 90 nm CMOS technology. The ADC achieves high-speed operation of 2.7 GS/s at low power consumption of 50 mW from a 1.0 V power supply and the figure of merit (FOM) is 0.47 pJ/conversion-step. The key technique is a digital background self-calibration architecture which compensates for the large mismatch of small devices in the ADC and also corrects the ADC characteristics degradation during operation due to the drift of environmental factors such as temperature. This background calibration technique suited for multi-GHz operation is realized by two-channel ADC architecture and digital smoothing technique, which uses averaging of two comparator offsets and reconfiguration of reference connection. To minimize the power dissipation, a cascade-calibrated folding-interpolating architecture has been developed. It reduces the overall analog power of our design by 50%, compared with a conventional architecture which applies calibration only to preamplifiers. By utilizing these low-power techniques, we have successfully developed a low-power ADC with all functions including the background self-calibration control circuit.**

***Index Terms*—ADC, analog-to-digital conversion, background, calibration, digital smoothing, folding, interpolation, low-power.**

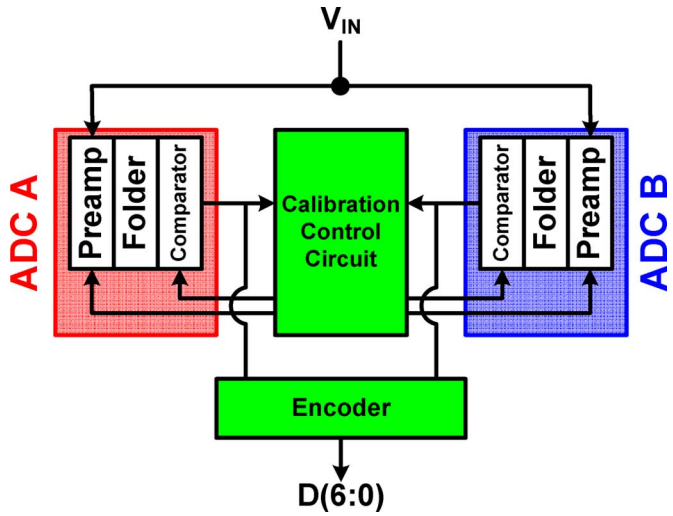

Fig. 1. Background calibration realized by two-channel ADC which converts the same input.

I. Introduction

LOW-POWER ADCs with multi-GHz sampling frequency are key elements in broadband communication systems such as mm-wave receivers, UWB, and future optical communication systems. These applications demand ultrahigh speed ADCs with low power consumption. In addition to low power consumption, small die area is also an important concern in implementing the ADC in large-scale SOCs.

Using fine-line CMOS devices is advantageous for boosting the power efficiency. However, to implement a power efficient ADC with a fine-line CMOS process is a challenging task because of the limited dynamic range at low supply voltage, poor matching characteristics between minimum size devices, and long-term degradation of devices. For example, when comparators with small size are used in flash-type ADCs, the large device variation of the comparators results in degraded linearity of the ADC. To improve the integral nonlinearity (INL) and differential nonlinearity (DNL), an averaging technique was first reported by Kattmann *et al.* [1] and later by Bult *et al.* [2]. Since then, the averaging of preamplifiers has been widely used for flash-type ADCs. However, due to the limited number of non-saturated preamplifiers, the improvement of INL and DNL is inadequate, as suggested in [3], [4].

We have resolved these issues by using compensation of device variation by calibration techniques. The calibration techniques, which take advantage of device scaling, can be categorized into foreground [5], [6] and background techniques [7]. An ADC with foreground calibration techniques requires an additional calibration when the temperature is changed, if there is environment dependence of ADC characteristics. During these foreground calibration cycles, normal ADC operation must be interrupted, which is a serious issue. Furthermore, ADC characteristics degradation due to long-term variation of device mismatch must be taken into consideration. Because the process of long-term variation of device mismatch is stochastic [8], it is difficult to predict the long-term degradation of ADC characteristics. To guarantee the ADC characteristics for a long-term period without interrupting the normal operation, the ADC must be calibrated in parallel with the normal operation. The ADC with the background calibration technique is therefore strongly required.

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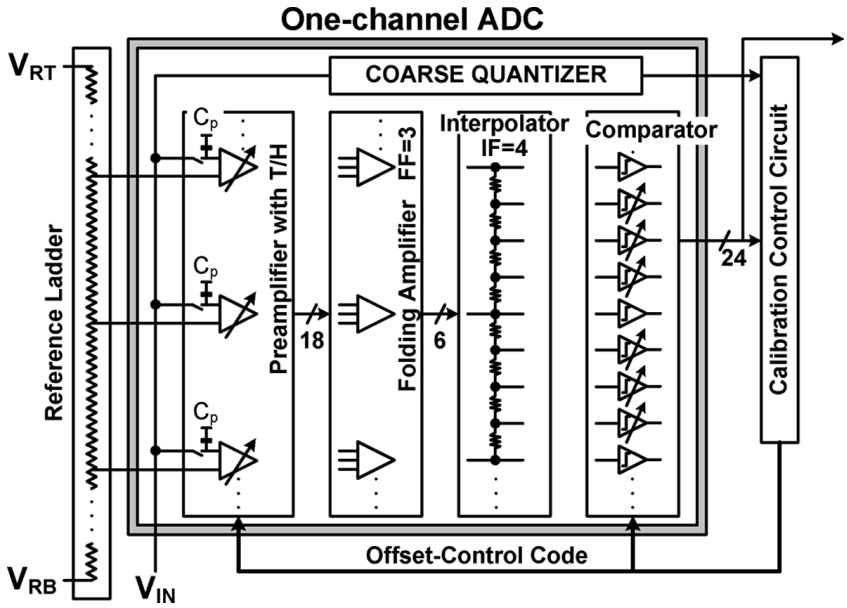

Fig. 2. Block diagram of the one-channel ADC with cascade-calibrated folding-interpolating architecture, reference ladder, and calibration control circuit.

Realizing background calibration for multi-GHz ADCs has been difficult because of lack of appropriate architecture. An example of background calibration is a previously reported background-calibrated comparator described in [7]. This uses random choppers, but the conversion frequency has to be limited to avoid performance degradation due to the slow chopping operation. Another example is that previously reported in [9], [10] which uses two-channel ADC technique to allow background calibration. Because it uses pipelined or cyclic architecture, it does not provide conversion frequency over GHz operation.

In this paper we propose a new architecture to realize a multi-GHz ADC with on-chip background calibration. We have developed a 6 bit 2.7 GHz ADC in 90 nm digital CMOS technology and the FOM of the ADC is 0.47 pJ/conv. To calibrate the ADC in the background, we have developed a new architecture using two-channel ADC which converts the same input. The developed ADC shown in Fig. 1 includes two-channel parallel type ADC (folding ADC A and B), a digital calibration control circuit, and an encoder. The outputs of two ADCs are thermometer code, which are combined and encoded into 7-bit digital output in the following encoder. The whole system therefore outputs the averaged code of two channel outputs. The difference between the two channels is used for developing the background digital calibration.

II. Folding-Interpolating ADC

There are two approaches to realizing an ultra high speed ADC. The first approach is to use time-interleaved architecture [11], [12] which employs multiple converters with a lower sampling rate and lower power consumption. In [12], 18 successive approximation register (SAR) ADCs are interleaved to realize overall higher sampling rate of 2.5 GHz. However, this interleave-based multi-GHz ADC results in large die area due to overhead for the high interleaving. It also requires calibration of gain, offset, and timing skew between channels. The second approach is to use flash-type architecture, which provides the highest sampling frequency for a single channel. Because flash-based multi-GHz ADC requires smaller die area than the time-interleaved ADC, it can be easily embedded in an SOC chip.

Among flash-type architectures, a folding-interpolating technique [5] is attractive because it can achieve high-speed operation at lower power dissipation and die area. The developed folding ADC block diagram is shown in Fig. 2. Although the schematic is shown as a single-ended circuit, the implementation is a differential circuit. The proposed ADC is composed of preamplifiers with a distributed T/H each, folding amplifiers, interpolators, comparators, and a coarse quantizer. The preamplifiers amplify an input signal and generate 18 zero crossings. These are followed by folding amplifiers with a folding factor (FF) of three. The low FF is chosen to maintain the high bandwidth of the folding amplifiers. The output signals of the folding amplifiers go through a resistive interpolation circuit with an interpolating factor (IF) of four, and finally are quantized by the comparators.

III. Cascade-Calibrated Folding-Interpolating Architecture

To reduce power dissipation while maintaining high-speed operation, we have developed a calibration architecture suitable for folding ADCs, namely cascade-calibrated folding-interpolating (CCFI) architecture. This calibration technique calibrates both preamplifiers and comparators so that it compensates for the offsets of all analog paths. This new architecture therefore allows the use of small size transistors in spite of the large mismatch.

Fig. 3(a) shows a schematic diagram of a conventional folding ADC. The ADC is composed of amplifiers (preamplifiers and folding amplifiers), resistive interpolator, and comparators. To suppress the device mismatch, large device size is used and quantized signals at the comparator outputs have ignorable error. However, large power consumption is required.

A previous report described in [5] uses smaller devices to reduce power consumption and applies the calibration tech-

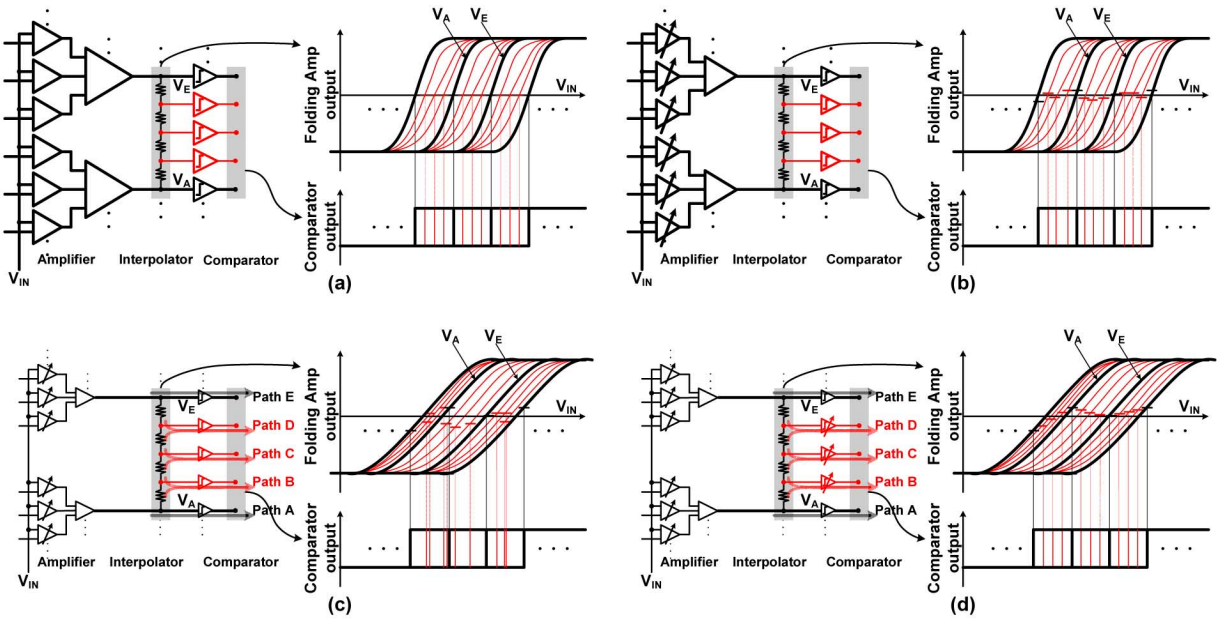

Fig. 3. Various schematic diagrams for the folding ADC (a) Ideal case using large devices. Large device size and power consumption are required. (b) Calibration of preamplifiers only. Smaller devices are used to reduce power consumption. (c) Calibration of preamplifiers only. Smallest devices are used to further reduce power consumption. (d) Cascade-calibrated interpolation technique.

nique only to preamplifiers and not to comparators, as shown in Fig. 3(b). This structure cancels the offsets of the amplifiers while the offsets of the comparators still remain. The amplifier must therefore amplify a small signal difference into a much larger signal than the input-referred offset of the comparator. Thus, a large "effective" amplifier gain is required, which we define here as the ratio of the output voltage of folding amplifier at the end of a clock period and the applied input voltage of preamplifier. The large gain results in significantly large power dissipation of the amplifier.

When the power dissipation of the amplifier and comparator is further reduced, the effective amplifier gain is reduced and becomes insufficient. This causes an issue: the comparator offset degrades the offsets along interpolated paths (paths B, C, and D) in Fig. 3(c). The accuracy along these paths is therefore degraded.

This problem is solved by the developed CCFI architecture shown in Fig. 3(d). In this architecture, both preamplifiers and comparators are calibrated to compensate for the offsets. Therefore, cancellation of the input-referred offsets of all analog paths is provided. In other words, not only the accuracy along the analog paths A and E, but also the accuracy along the interpolated analog paths B, C, and D are compensated for. In addition, the error caused by mismatch of interpolators also can be calibrated.

By successfully using fine-line CMOS devices to these paths, low power consumption is therefore achieved. To minimize the power dissipation of the amplifier, we have intentionally minimized the effective amplifier gain and reduced it to 1.4 in our design, whereas a gain of three was required in the architecture shown in Fig. 3(b). By utilizing CCFI architecture instead of the architecture shown in Fig. 3(b), the overall analog power of our design is reduced by 50%.

It may be worth mentioning, in passing, that the architecture which employs the calibration of only comparators does not provide cancellation of the input-referred offsets of all analog paths for the folding-interpolating ADCs. This is because multiple paths are combined at the folding amplifier and offsets of these paths can not be adjusted independently.

IV. Background Calibration Architecture

The block diagram for background calibration architecture is shown in Fig. 4. The key concept is *digital smoothing* operation, which is provided by two techniques. The first is the averaging of two comparator offsets; the digital comparators in the calibration control circuit average the offsets of the corresponding two comparators in ADC A and B. The second is reconfiguration of reference connection; the reconfiguration of reference connection is provided by the barrel shifters between reference ladder and preamplifiers, and the barrel shifters between comparators and digital comparators. In the signal flow view, the shift of reference ladder corresponds to injection of signal m (or n) into the reference voltage. The signal is digitally subtracted later by the barrel shifter that follows the comparators. The switching process is therefore transparent to the normal ADC operation.

Although the concept is applied to both preamplifiers and comparators, only the calibration of comparator is explained by the circuit shown in Fig. 5. The barrel shifters in Fig. 4 are implemented by the analog switches between the reference ladder and the comparators, and digital switches between the comparators and the digital comparators. These switches can change the reference connection, and therefore the circuit has two operation modes [Fig. 5(a), (b)]. In the first operation mode, the offsets of oppositely placed comparators (e.g., A_i and B_i) in the two ADCs are averaged. In the second operation mode, the offsets of diagonally placed comparators (e.g., A_i and B_{i+1}) are averaged.

Fig. 6 shows the transfer curves of two-channel ADC. Before calibration, two ADCs have the degraded characteristics as shown in Fig. 6(a) because of the random offsets of comparators. By using these two operation modes, the offsets of adja-

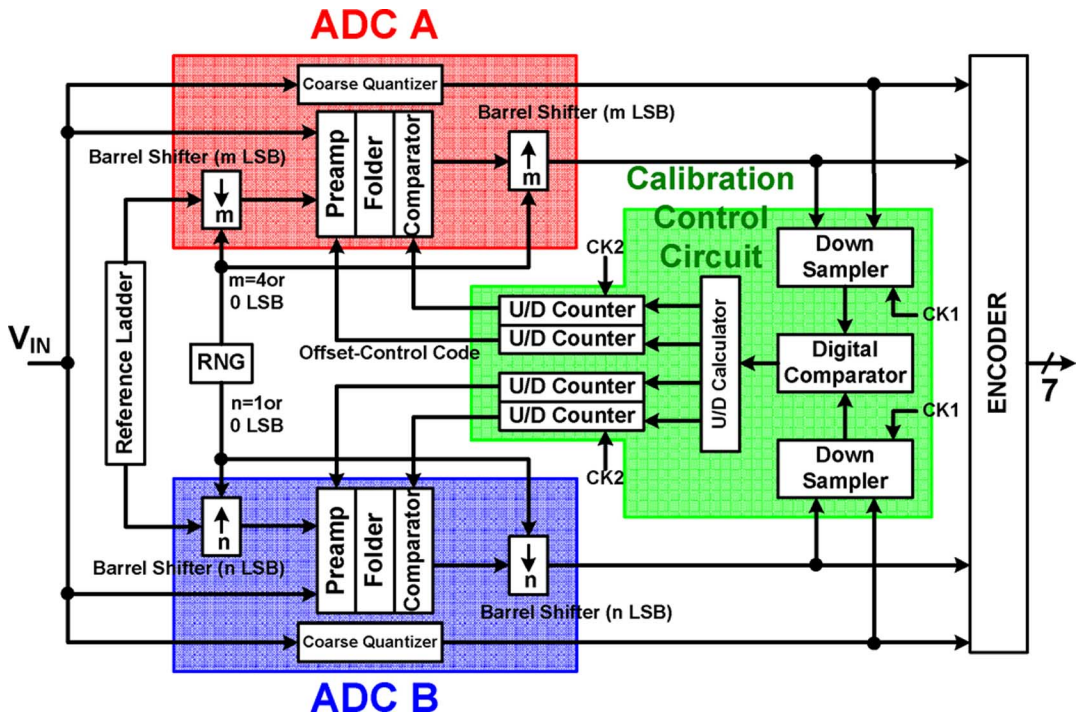

Fig. 4. Block diagram for background calibration architecture achieved by *digital smoothing* operation.

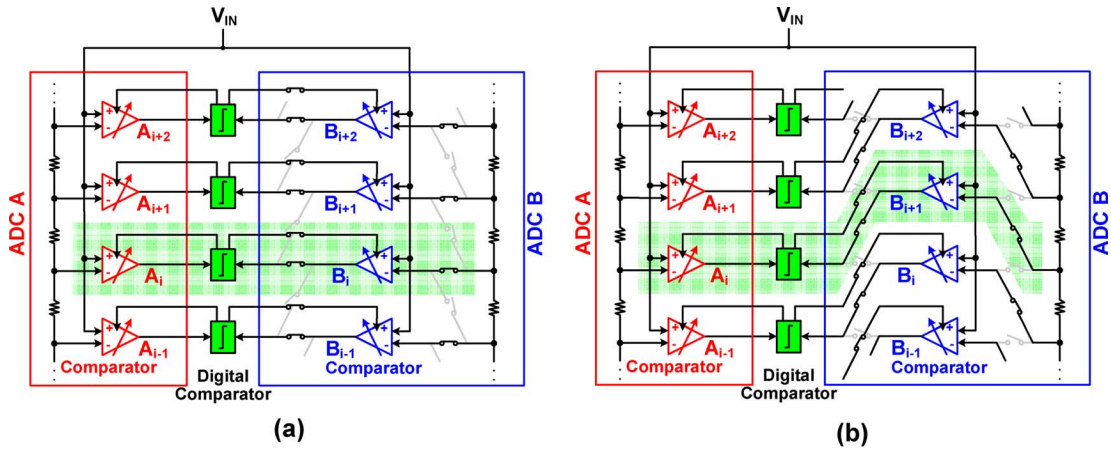

Fig. 5. Principle of *digital smoothing* operation of two-channel ADC. The operation can be changed between the two modes, by the switches. (a) First operation mode: The offsets of oppositely placed comparators are averaged. (b) Second operation mode: The offsets of diagonally placed comparators are averaged.

cent comparators *within* each ADC are averaged and reduced. The developed algorithm therefore enhances the linearity of the ADC, and the improved characteristics are obtained after calibration [Fig. 6(g)].

The circuit in Fig. 5 has periodically repeated structure. One slice of the circuit is shown in Fig. 7(a). The two comparators have offsets $V_{\mathrm{OS},A}$ and $V_{\mathrm{OS},B}$, which can be adjusted by calibration signals Calib_A and Calib_B, respectively. In the initial condition, $V_{\mathrm{OS},A}$ and $V_{\mathrm{OS},B}$ have random values due to the device local variation as shown in Fig. 7(b). The two comparators in Fig. 7(a) compare the same analog input V_{IN} with the same reference REF. The outputs of two comparators OUT_A and OUT_B are transmitted to the digital comparator, and the digital comparator compares these outputs. If OUT_A and OUT_B differ, the digital comparator feeds back the calibration signals (Calib_A and Calib_B), which is up or down signal, to the comparators. Then the offsets of comparators ($V_{\mathrm{OS},A}$ and $V_{\mathrm{OS},B}$) are changed by a step size defined as δ LSB; when OUT_A is "1" and OUT_B is "0", $V_{\mathrm{OS},A}$ is increased and $V_{\mathrm{OS},B}$ is decreased; when OUT_A is "0" and OUT_B is "1", $V_{\mathrm{OS},A}$ is decreased and $V_{\mathrm{OS},B}$ is increased. By this operation, $V_{\mathrm{OS},A}$ and $V_{\mathrm{OS},B}$ approach each other and eventually these are averaged. Here, the assumption that there is non-zero probability density of V_{IN} at comparator trip voltages is used, which assumption holds for most applications.

In the following, the calibration principle is described step by step, by using the comparator offsets $V_{\mathrm{OS},A,i}[n]$ and $V_{\mathrm{OS},B,i}[n]$, where the index i is the comparator number and n is the calibration step number. Before calibration, the comparator offsets are random values, which are $V_{\mathrm{OS},A,i}[0]$ and $V_{\mathrm{OS},B,i}[0]$. Because of these random offsets, two ADCs have the degraded characteristics as shown in the transfer curves of two-channel ADC [Fig. 6(a)].

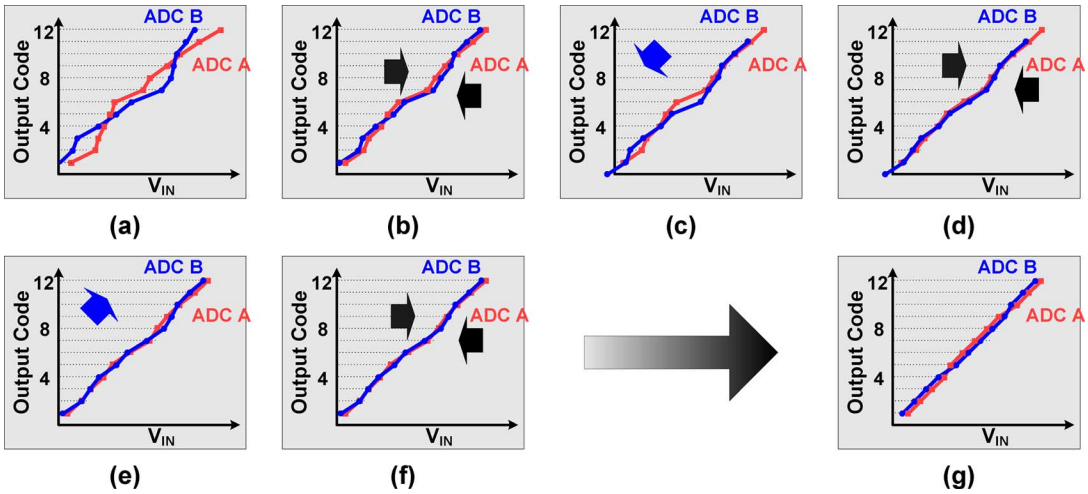

Fig. 6. *Digital smoothing* operation showing the transfer curves of two-channel ADC. (a) Before calibration. (b) First step: The transfer curves of ADC A and B are averaged. (c) Second step: The transfer curve of ADC B is shifted to lower left by 1 LSB. (d) Second step (continued): The transfer curves of ADC A and B are averaged. (e) Third step: The transfer curve of ADC B is shifted to upper right by 1 LSB. (f) Third step (continued): The transfer curves of ADC A and B are averaged. (g) After calibration.

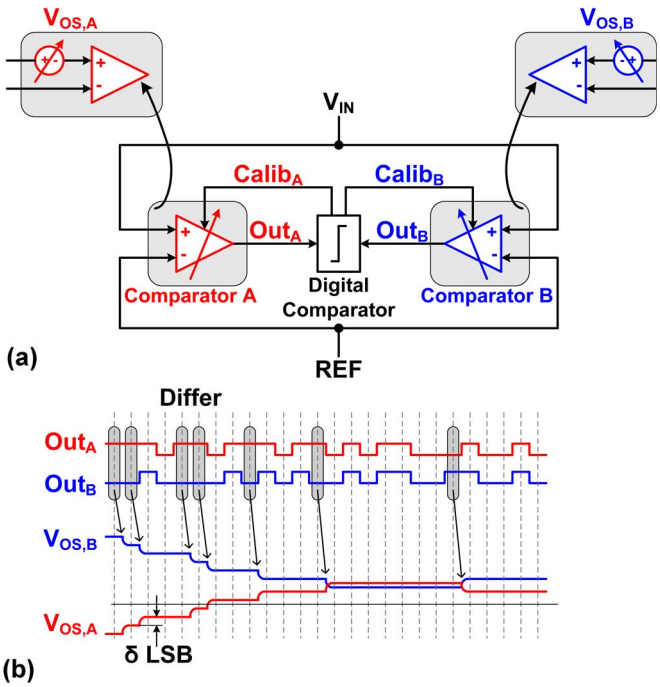

Fig. 7. (a) One slice of the schematic in Fig. 5(b). The waveforms showing operation. The thresholds of the two comparators are digitally averaged in the background.

In the first step of calibration, the first operation mode [Fig. 5(a)] is used. The offsets of opposite comparators ($V_{\mathrm{OS},A,i}$ and $V_{\mathrm{OS},B,i}$) therefore approach each other and eventually these are averaged and $V_{\mathrm{OS},A,i}[1] = V_{\mathrm{OS},B,i}[1] = (V_{\mathrm{OS},A,i}[0] + V_{\mathrm{OS},B,i}[0])/2$ is obtained. By this operation, the two transfer curves of the ADCs are averaged as shown in the transfer curve view of Fig. 6(b). However, this operation alone does not improve the linearity of the ADCs.

In the second step of calibration, the second operation mode shown in Fig. 5(b) is used, and $V_{\mathrm{OS},A,i}$ and $V_{\mathrm{OS},B,i+1}$ are averaged. Therefore, $V_{\mathrm{OS},A,i}[2] = V_{\mathrm{OS},B,i+1}[2]$

$$= \frac{1}{2}\left(\frac{V_{\mathrm{OS},A,i}[0] + V_{\mathrm{OS},A,i+1}[0]}{2} + \frac{V_{\mathrm{OS},B,i}[0] + V_{\mathrm{OS},B,i+1}[0]}{2}\right) \quad (1)$$

is obtained. Here, $(V_{\mathrm{OS},A,i}[0] + V_{\mathrm{OS},A,i+1}[0])/(2)$ (the average of offsets of adjacent comparators *within* ADC A) appear in the right-hand side of (1). Fig. 6(d) shows the obtained transfer curve after the second step according to (1). In the transfer curve view, the change of reference connection means that the transfer curve of ADC B shifts to the lower left by 1 LSB [Fig. 6(c)]. Next, the two transfer curves are averaged again [Fig. 6(d)], so that the transfer curves become smoother than before.

The two operation modes described above are switched back and forth. In the third step of calibration, the offsets of the comparators become $V_{\mathrm{OS},A,i}[3] = V_{\mathrm{OS},B,i}[3]$

$$= \frac{V_{\mathrm{OS},A,i-1}[0] + 2V_{\mathrm{OS},A,i}[0] + V_{\mathrm{OS},A,i+1}[0]}{8} + \frac{V_{\mathrm{OS},B,i-1}[0] + 2V_{\mathrm{OS},B,i}[0] + V_{\mathrm{OS},B,i+1}[0]}{8}. \quad (2)$$

In the transfer curve view, the transfer curve of ADC B shifts to the upper right by 1 LSB [Fig. 6(e)] and the two transfer curves are averaged again [Fig. 6(f)]. The curves therefore become smoother and smoother.

Continuing in this way, the offsets of the comparator evolve as follow. For odd steps,

$$V_{\mathrm{OS},A,i}[2n+1] = V_{\mathrm{OS},B,i}[2n+1] = \frac{\sum_{j=1}^{l} w_j \frac{V_{\mathrm{OS},A,j}[0] + V_{\mathrm{OS},B,j}[0]}{2}}{\sum_{k=1}^{l} w_k} \quad (3)$$

where $w_j = \binom{2n}{n-i+j}$. For even steps,

$$V_{\mathrm{OS},A,i}[2n] = V_{\mathrm{OS},B,i+1}[2n] = \frac{\sum_{j=1}^{l} w_j \frac{V_{\mathrm{OS},A,j}[0]+V_{\mathrm{OS},B,j}[0]}{2}}{\sum_{k=1}^{l} w_k} \quad (4)$$

where $w_j = \binom{2n-1}{n-1-i+j}$. Here, n is an integer, l is the total number of comparators, and $\binom{n}{k}$ is a binomial coefficient.

Now the right side of (3) is evaluated. Because

$$\binom{2n}{n+l} \le w_j \le \binom{2n}{n} \quad \text{for} \quad \{j | 1 \le j \le l\}$$

and

$$\binom{2n}{n+l} \Big/ \binom{2n}{n} \to 1 \quad (n \to \infty),$$
$$\frac{w_j}{\sum_{k=1}^{l} w_k} \to \frac{1}{l} \quad (n \to \infty) \quad (5)$$

holds. By substituting (5) into (3),

$$V_{\mathrm{OS},A,i}[2n+1] = V_{\mathrm{OS},B,i}[2n+1] \to \frac{1}{2l}\sum_{j=1}^{l}(V_{\mathrm{OS},A,j}[0] + V_{\mathrm{OS},B,j}[0]) \quad (n \to \infty) \quad (6)$$

is obtained. The offsets of comparators therefore converge toward the mean of all comparator offsets, and the linearity of the ADC is improved.

In real implementation, the calibration step size δ LSB is finite as shown in Fig. 7. After the convergence, the offset difference between two comparators is within 2δ for Fig. 5(a) and (b). Therefore,

$$|V_{\mathrm{OS},A,i+1}[n] - V_{\mathrm{OS},B,i+1}[n]| < 2\delta \quad (7)$$

and

$$|V_{\mathrm{OS},B,i+1}[n] - V_{\mathrm{OS},A,i}[n]| < 2\delta. \quad (8)$$

The absolute of differential nonlinearity (DNL) of each ADC is $|V_{\mathrm{OS},A,i+1}[n] - V_{\mathrm{OS},A,i}[n]|$

$$= |(V_{\mathrm{OS},A,i+1}[n] - V_{\mathrm{OS},B,i+1}[n]) + (V_{\mathrm{OS},B,i+1}[n] - V_{\mathrm{OS},A,i}[n])| < 4\delta \quad (9)$$

where inequalities (7) and (8) are used. Therefore, the upper limit of DNL is 4δ LSB. More precise evaluation, however, requires simulation.

As described, the linearity improvement is achieved by *digital smoothing* operation. The advantages of this architecture are as follows.

1) Because the calibration operates completely in the background, the additional calibration cycle is eliminated. Moreover, the ADC can correct the degraded characteristics due to the drift of environmental factors or long-term device variation.
2) The background calibration of ultrahigh speed ADC is realized, which is accomplished by completely separating the calibration signal paths from high-speed analog signal paths.
3) This architecture eliminates a high precision reference signal source for foreground calibration, which is additionally required by the prior technique in [5]. Consequently, there is no need for inputting a predetermined specific signal for calibration. Moreover, since it eliminates a high precision signal source, the calibration control circuit can be made up with only digital circuits. The obtained simple circuit structure makes it easy to integrate all functions for the background calibration control circuit.
4) The accuracy of preamplifiers and comparators is not dependent on device matching property. In reality, the accuracy is determined only by calibration step voltage. For example, in our design the INL is improved by up to eight times. On the other hand, it is suggested in [3] that the traditional averaging technique can only improve the INL up to three times when the number of non-saturated preamplifiers is nine.
5) Once the calibration converges, the calibration can be stopped and the two ADCs can be separated by disconnecting the common input line of the two ADCs. Thus, these can be used as individual ADCs which convert independent signals, although the background calibration function is disabled. In this method, matched two channel ADCs are obtained. We call this operation mode "separation mode."

V. Circuit Implementation

A. Calibration for CCFI Architecture

The principle described above is applied to the CCFI architecture described in Section III. Since both the calibration functions of preamplifiers and comparators are implemented, the calibration control system has two feed back loops. The designed circuit in Fig. 4 is reconfigurable by the barrel shifter. The shift amounts of two reference ladders are four or zero LSB for ADC A and one or zero LSB for ADC B. The combination of shift amounts of two reference ladders is controlled by a 2-bit mode signal PN, which is switched from zero to three in the background.

The corresponding four circuit configurations are shown in Fig. 8. When PN is zero or one, the circuit configuration in Fig. 8(a) is used and the preamplifiers are calibrated; The accuracy along the non-interpolated analog paths, which are shown as paths A and E, is compensated for. When PN is two or three, the circuit configuration in Fig. 8(b) is used and the comparators are calibrated; The accuracy along the interpolated analog paths, which are shown as paths B, C, and D, is compensated for. Notice that the only comparators connected to the interpolated paths are calibrated, and the structure is the same as that of Fig. 3(d).

During calibration, the adjusted offsets of comparators on interpolated paths (B, C, and D) are also affected by the offset control of preamplifiers. But these offsets of comparators on

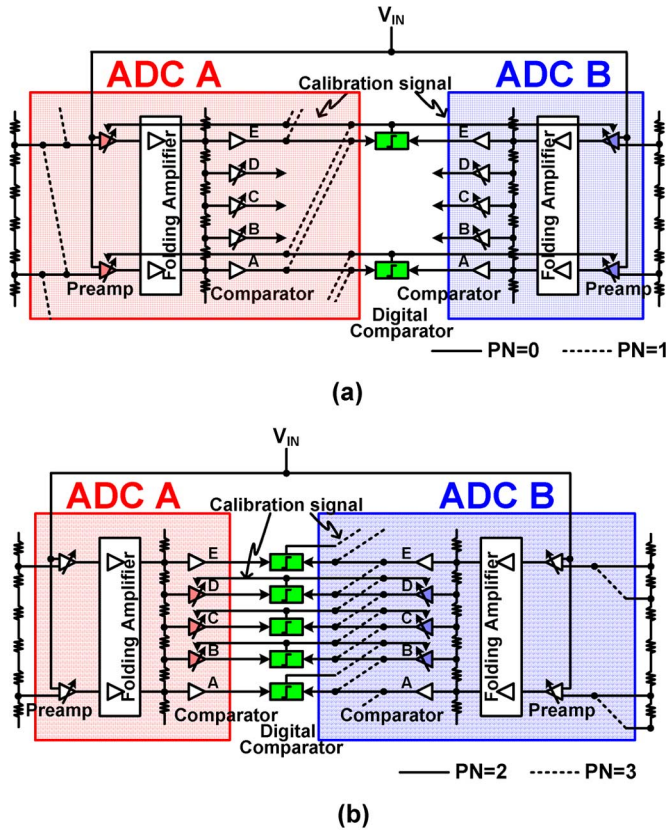

Fig. 8. (a) Circuit for background calibration of preamplifiers. When PN is zero or one, this circuit configuration is used. (b) Circuit for background calibration of comparators. When PN is two or three, this circuit configuration is used.

interpolated paths also converge after the convergence of the offsets of preamplifiers. Thus, the offsets of all preamplifiers and comparators are uniquely determined after calibration. After the convergence of feed back loops, the quantized signals at the comparator outputs have ignorable error as shown in Fig. 3(d).

B. Timing and Mode Sequence Design

The timing diagram of the circuit in Fig. 4 is shown in Fig. 9. The calibration control circuit is triggered by the two-phase clocks CK1 and CK2, resulting in reduced circuit complexity. The outputs of comparators are down-sampled by flip-flops at the rising edge of CK1, which has a lower frequency rate than the operation frequency of the comparators. The digital comparators compare the down-sampled data and output up or down signals. The values of up/down counters are set by these signals at the rising edges of CK2, and output offset-control codes to the preamplifiers and comparators. Then the offsets of the preamplifiers and comparators are adjusted by these offset-control codes. Although the sampling frequency of the ADC is 2.7 GHz, the calibration control circuit does not need to operate at GHz. To reduce the digital power consumption, the calibration control circuit is operated at a lower frequency of 125 MHz.

To eliminate the influence of the mode sequence, the 2-bit mode signal PN is generated by an on-chip random number generator (RNG). The PN signal is switched among four values and changes from cycle to cycle.

C. Low-Power Distributed T/H and Preamplifier

In folding ADC, input signal frequency is multiplied by the folding factor in the folding circuit. A track and hold (T/H) circuit is therefore necessary at the input of ADC to improve dynamic performance. Several T/H circuits have been proposed previously.

A well-known structure is to add a sampling switch and a buffer circuit in front of the ADC as shown in Fig. 10(a), but the power consumption of the additional buffer circuit between the sampling switch and first-stage preamplifier is high. Another traditional technique is to use distributed T/H which was introduced by Venes *et al.* [13]. In this technique, the sampling switch is placed at the preamplifier output as shown in Fig. 10(b). However, this structure prevents high-speed operation since the preamplifier output is a high impedance node. Moreover, because of the high impedance, local variation of time delay between T/Hs is significant when the input frequency is high.

The proposed distributed T/H and preamplifier with calibration is shown in Fig. 10(c). We placed the switch at the preamplifier input node and the input signal is sampled at the gate capacitance of each preamplifier. Because the analog signal is commonly connected to each T/H, the local variation of time delay between T/Hs is smaller than in the case of 10(b). The dynamic characteristics are therefore improved.

In addition, the charge injections of each T/H, which are different due to device mismatch and voltage-dependent charge injection, are compensated for by the calibration of the preamplifier.

The offset of the preamplifier is calibrated by a current-steering DAC and adjusted by 4-bit 2's complementary offset-control code, as shown in Fig. 10(d). This calibration circuit cancels the combined offset of the preamplifier, the preceding T/H, and the following folding amplifier. Thus, the transistor size can be reduced, which results in low-power operation. The device area is reduced by 90%, and this circuit enables sampling of broadband signal and power dissipation is reduced by 70% compared with the circuit in Fig. 10(b).

D. Folding Amplifier and Comparator

The following circuit is a folding amplifier with a folding factor of three. Traditionally, a folded-cascode circuit is required to drive large parasitic capacitance of the folding bus, as reported in [5]. However, the folded-cascode circuit requires an additional current path and high power consumption. To minimize the parasitic capacitance, we have positioned the three differential pairs close together. The obtained low parasitic capacitance allows to eliminate the folded-cascode circuit and the low-power operation is successfully achieved. The offset of the comparator is adjusted by 4-bit offset-control code. The calibration circuit for the comparator is implemented by variable capacitance at drain nodes of differential pair which is described in [14] as well as in [15]. The variable capacitance is composed of 4-bit binary weighted pMOS transistors and the capacitance is adjusted by applying a digital signal to the transistor gate. We have used pMOS transistors with minimum size of width and weighted size of length, instead of using transistors with minimum size of length and weighted size of width. The diffusion capacitance of transistor is therefore minimized so that the operation frequency of the comparator is maximized.

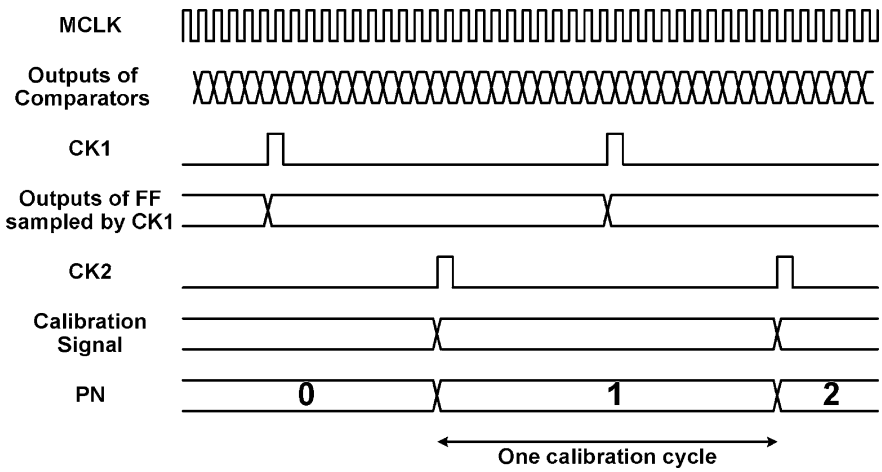

Fig. 9. Waveforms showing calibration operation.

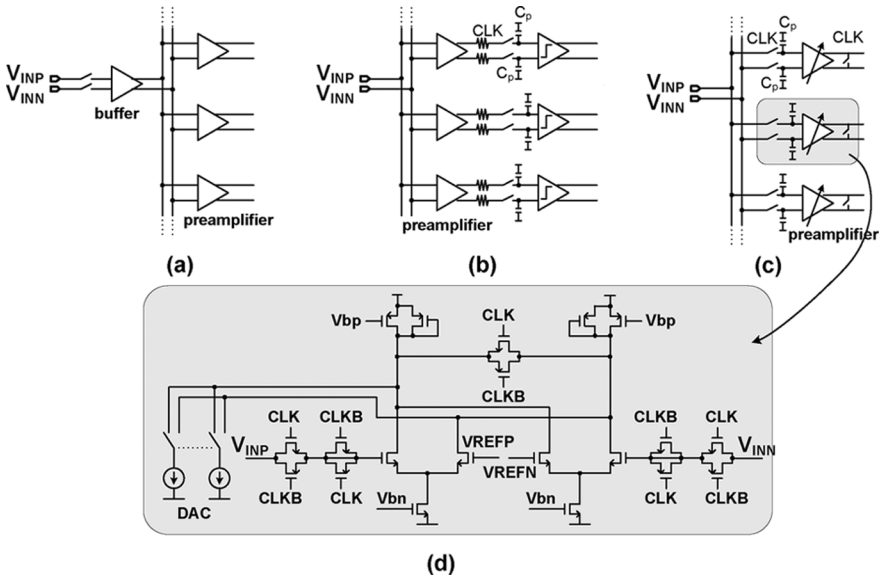

Fig. 10. (a) Traditional technique of a buffer which precedes preamplifiers. (b) Traditional distributed T/H technique. (c) Proposed distributed T/H and preamplifiers with calibration. (d) Detailed schematic of one T/H and preamplifier in (c).

VI. Experimental Results

Fig. 11 shows a histogram of offset-control codes for preamplifier and comparator after calibration. These codes have been measured from both ADC channels of 10 samples. These are 4-bit digital signals and take values from -8 to 7. By these offset-control codes, the transition levels of each ADC are adjusted. The transition level which corresponds to the path A and E in Fig. 3(d) (non-interpolated path) is adjusted by a unit of 0.4 LSB by the preamplifier. The transition level which corresponds to the path B, C, and D in Fig. 3(d) (interpolated path) is adjusted by a unit of 0.28 LSB by the comparator. The histogram shows that our design covers the 3.4 sigma value of the offset variation of both preamplifiers and comparators, and therefore good production yield is obtained.

Fig. 12 shows the measured INL and DNL before and after calibration, measured at 2.7 GS/s with a full-scale ramp input employing a histogram method. The 1 LSB of vertical axis is $800\ \text{mV}/2^6 = 12.5\ \text{mV}$. The measured DNL of 1.83 LSB before calibration is sufficiently reduced to 0.53 LSB after calibration. This figure is in agreement with the design, since the simulated DNL assuming typical sample is 0.5 LSB. The obtained INL and DNL are sufficient for our application. Although enhancing the resolution of offset-control code will further reduce the INL and DNL, we have selected the 4-bit resolution to reduce the die area of the calibration control circuit.

When the input voltage is varied across a transition level of the ADC, the transition between the lower code and the higher code is blurred. Therefore, the transition point between the two codes has a finite width. By calculating the probability of getting higher code as a function of the input voltage, we have evaluated the input-referred noise of the ADC. The obtained sigma of the input-referred noise is 1 mV, which is one fourth of the quantization noise of the ADC. This result indicates that the noise limit of the ADC is around an accuracy of 8 bits.

Fig. 13 is the results of the SNDR measurement as a function of the calibration cycle number, where one calibration cycle is defined in Fig. 9. After the initial power-on, the sine wave is

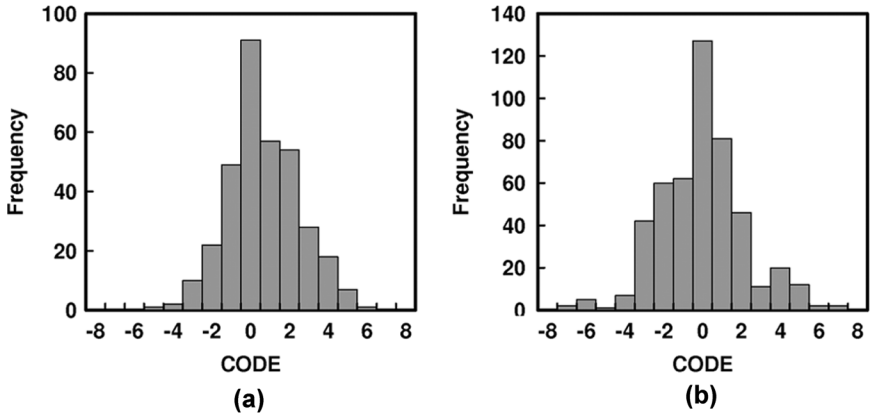

Fig. 11. Histogram of offset-control codes for (a) preamplifier and (b) comparator.

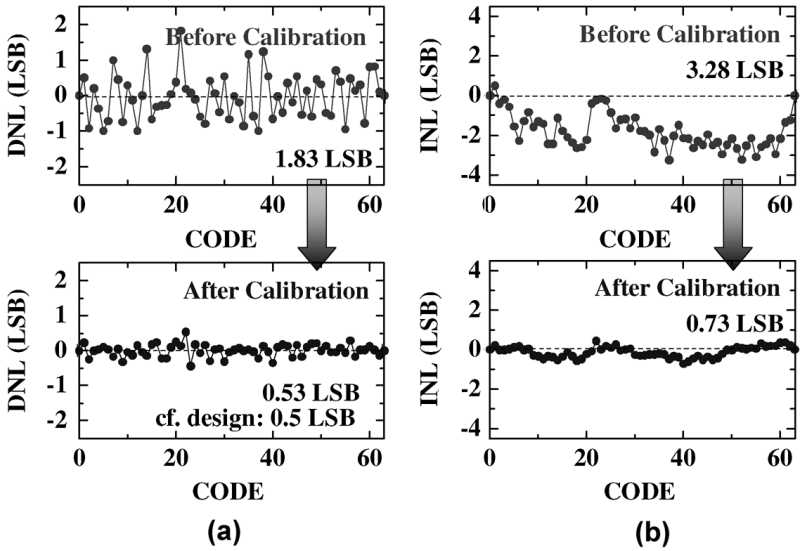

Fig. 12. Measured (a) DNL and (b) INL before and after calibration.

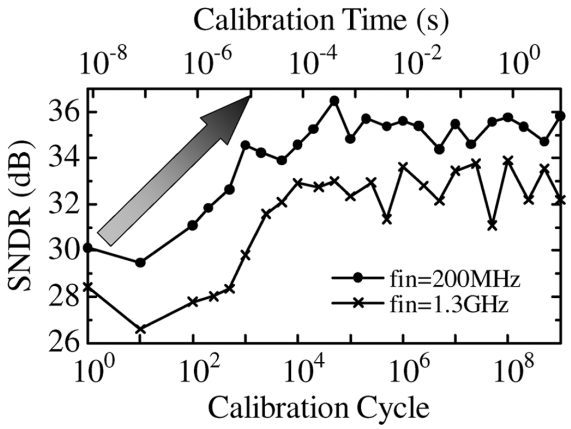

Fig. 13. Measured SNDR convergence during calibration at sampling frequency of 2.7 GHz. The SNDR is measured with input frequency of 200 MHz and 1.3 GHz.

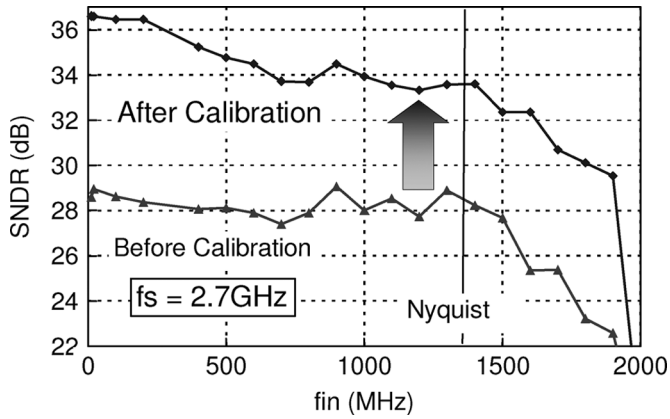

Fig. 14. Measured SNDR versus fin before and after calibration.

input. The steady state is attained after 1×10^4 clock cycles. This number corresponds to 100 μs of calibration time, which is acceptable for most applications. The obtained SNDR for input frequency of 200 MHz is above 34 dB and the performance slightly degrades for higher input frequency. One explanation for the degradation might be that the SNDR improvement by calibration is limited by the requirement of channel timing and bandwidth matching between the two ADCs.

Input signal frequency versus measured SNDR before and after the calibration is shown in Fig. 14. The sampling frequency is 2.7 GHz and input signal frequency is varied ranging from DC to 2 GHz. The ADC is calibrated in the background using input sine wave of each frequency. After the calibration, the

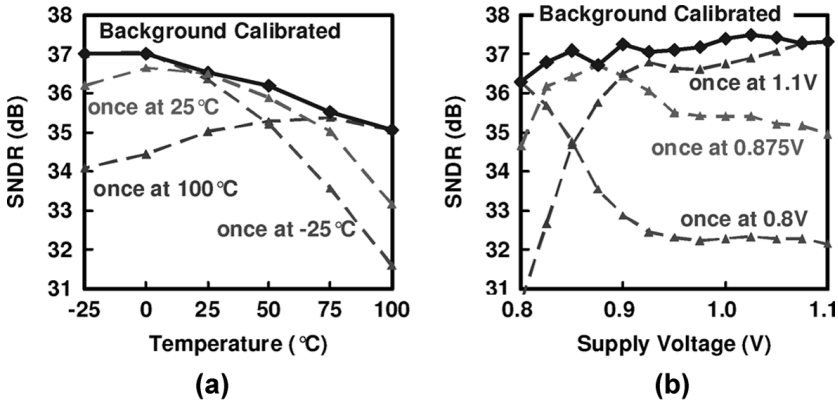

Fig. 15. Measured environment dependence. (a) Temperature dependence of SNDR with sampling frequency of 2.7 GHz, input frequency of 200 MHz, and supply voltage of 1 V. The SNDR versus temperature is measured when the ADC is calibrated once at $-25°$C, once at 25°C, once at 100°C, and in the background. (b) Supply voltage dependence of SNDR with sampling frequency of 1 GHz, input frequency of 250 MHz, and temperature of 25°C. The SNDR versus supply voltage is measured when the ADC is calibrated once at 0.8 V, once at 0.875 V, once at 1.1 V, and in the background.

SNDR at Nyquist frequency is 33.6 dB, so that the SNDR is enhanced by 6 dB by the calibration. The obtained SNDR at high frequency shows that the full-Nyquist ADC has been developed by utilizing the broadband T/H design described before.

Fig. 15 shows the measured environment dependence. These data show that the calibration technique has enabled a design robust against the drift of environmental factors.

Fig. 15(a) shows the temperature dependence. The calibration was temporarily stopped during operation at $-25°$C. Next, the temperature was changed to 100°C. Since the SNDR degrades from 37 dB to 31.6 dB, it has temperature dependence. Similarly, when the ADC is once calibrated only at 100°C, the SNDR degrades at $-25°$C. On the other hand, when the background calibration is continuously used, the SNDR is maintained above 35.1 dB.

Fig. 15(b) shows the supply voltage dependence. To show that the calibration technique is well suited to the ultra-low voltage operation, the supply voltage is varied from 0.8 V to 1.1 V. When the background calibration is used, the SNDR is maintained above 36.3 dB. Notice that the background calibration allows the low voltage operation at 0.8 V, although the design target is from 0.9 V to 1.1 V.

The measured characteristics of the ADC are summarized in Table I. We have successfully integrated all functions including background self-calibration control circuit in 0.36 mm^2 as shown in Fig. 16. The ADC does not need an additional analog circuit such as a high-precision reference source for calibration.

Fig. 17 is the comparison of the figure of merit FoM $=$ power$/2^{\mathrm{ENOB}} \times \min(2 \times \mathrm{ERBW}, f_{\mathrm{sample}})$ of multi-GHz ADC with 6-bit or more resolution previously published [12], [16]–[21]. The SNDR of our ADC is 33.6 dB and the figure of merit is 0.47 pJ/conv. The FOM of our work is improved by two times compared with a previous work of uncalibrated flash type ADC [20]. The sampling rate is comparable to and the FOM is slightly better than those of the time-interleaved ADC reported by Alpman *et al.* [12]. Notice that the area of our 90 nm CMOS ADC is smaller by more than two times compared with Alpman *et al.* [12], which was fabricated in 45 nm CMOS.

Fig. 17 also shows the FOM of separation mode. When the calibration is stopped and the two-channel ADC is used in separation mode, each ADC has an SNDR of 33.0 dB. In this mode, the FOM is further reduced to 0.25 pJ/conv so that it is approximately halved compared with background calibration mode.

TABLE I
PERFORMANCE SUMMARY OF ADC

Process		90 nm CMOS
Resolution		6 bits
Sampling Rate		2.7 GS/s
Power Supply		1V
Input Voltage Range		800mVpp, diff
Power Consumption @1V	Total	50 mW
	ADC A	22.5 mW
	ADC B	22.5 mW
	Calibration control circuit	5 mW
SNDR	@fin=10MHz	36.5 dB
	@Nyquist(1.35 GHz)	33.6 dB
Figure of Merit	Background calibration mode	0.47 pJ/conv.
	Separation mode	0.25 pJ/conv.
INL		0.73 LSB
DNL		0.53 LSB
Active Die Area		0.36 mm^2

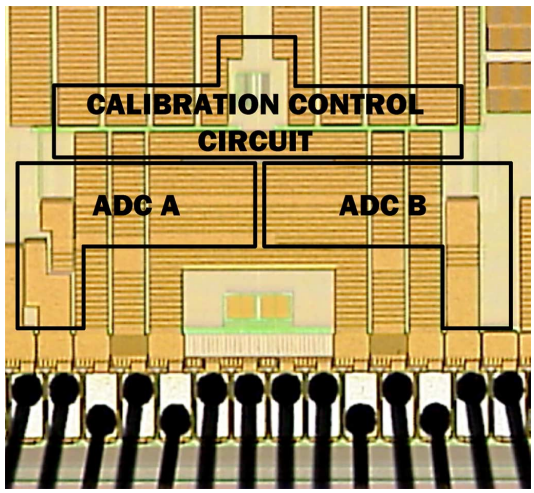

Fig. 16. Photograph of ADC.

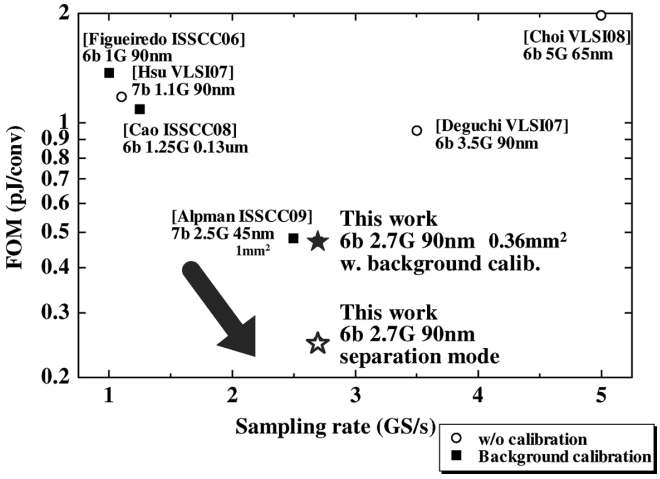

Fig. 17. Comparison of multi-GHz ADCs with 6-bit or more resolution.

This result is consistent with the noise limit of the ADC, which is around accuracy of 8-bit and exceeds the ADC resolution of 6-bit.

VII. Conclusion

In this work, we have developed a 6-bit 2.7 GS/s folding ADC with on-chip background self-calibration in 90 nm CMOS technology. The FOM is 0.47 pJ/conversion-step. The key technique is a digital background self-calibration architecture which compensates for the large mismatch of small devices in the ADC and also corrects the ADC characteristics degradation during operation due to the drift of environmental factors such as temperature. This background calibration technique suited for multi-GHz operation is realized by two-channel ADC architecture and digital smoothing technique, which uses the averaging of two comparator offsets and reconfiguration of reference connection. The architecture made is capable of successfully implementing all functions including the background self-calibration control circuit in small die area. The ADC does not need an additional analog circuit such as a high-precision reference source for calibration.

The proposed technique is anticipated to further advance the state of the art of ADC architectures.

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