Delay-Line-Based Analog-to-Digital Converters

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***Abstract*—We will introduce a design of analog-to-digital converters (ADCs) based on digital delay lines. Instead of voltage comparators, they convert the input voltage into a digital code by delay lines and are mainly built on digital blocks. This makes it compatible with process scaling. Two structures are proposed, and tradeoffs in the design are discussed. The effects of jitter and mismatch are also studied. We will present two 4-bit, 1-GS/s prototypes in 0.13-μm and 65-nm CMOS processes, which show a small area (0.015 mm^2) and small power consumption ($<$ 2.4 mW).**

***Index Terms*—Analog-to-digital converter (ADC), delay line, scaling.**

I. Introduction

In MOST analog-to-digital converters (ADCs), the input analog voltage is converted into a digital code by an explicit voltage comparison [1]. However, when integrated circuit fabrication technologies (e.g., CMOS) reach the deep-submicrometer regime, circuits that process analog voltage signals encounter scaling impediments [2], [3]. In particular, due to supply voltage reduction, the voltage domain is becoming noisier. In addition, the relatively high threshold voltage makes the available headroom very small for any sophisticated analog architectures. On the positive side of scaling, with rising and falling times on the order of 10 ps, the switching characteristics of MOS transistors offer excellent timing accuracy at high frequencies. Thus, a new design paradigm with deep-submicrometer CMOS technologies is possible, in which the time-domain resolution of a digital signal edge transition is superior to the voltage resolution of an analog signal [2]. This, along with considerations of chip area and power dissipation, gives rise to an upcoming trend to "digitize" part of or even the whole mixed-signal blocks [3]. These encourage us to study ADC structures based on digital blocks and compatible with scaling.

Functionally, ADCs are quite similar to time-to-digital converters (TDCs), which are used to quantize time intervals in applications such as phase-locked loops [4]. A digital delay-line-based TDC approach has recently become attractive, particularly for deep-submicrometer technologies [3]. The basic structure consists of buffers and flip-flops, as shown in Fig. 1(a). Initially, all buffers are reset to "0." Then, a rising edge is fed into "Start" and propagates along the delay line. After a while, "Stop" goes high and triggers the flip-flops to sample the delay line, which produces a thermometer code such as "$1\ldots1100\ldots0$." The number of "1"s in the codeword provides a measure of the delay between "Start" and "Stop," with a resolution of D, which is the delay per buffer. The vernier structure in Fig. 1(b) is often used to achieve a higher resolution: Each stage reduces the delay between "Start" and "Stop" rising edges by δ, i.e., the difference between the two delay cells, which leads to a time resolution of δ. Other advanced structures include the pulse-shrinking delay line and the local time-interpolation technique. A summary of these structures can be found in [3], and for more details, please refer to [4]–[7].

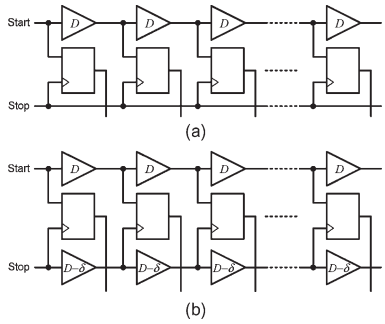

Fig. 1. Delay-line-based TDCs. (a) Basic structure. (b) Vernier structure.

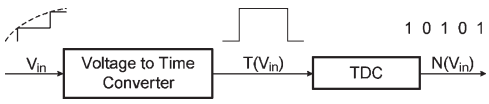

Fig. 2. Illustration of voltage-to-time-to-digital ADCs.

In light of the analogy between ADCs and TDCs, it seems promising to design new ADCs using similar structures. A straightforward way is the *voltage-to-time-to-digital* approach in Fig. 2: The sampled input voltage $V_{\rm in}$ is first converted to a time window $T(V_{\rm in})$, which is then quantized by TDCs. This design stems from integrating ADCs, which are believed to be suitable for high-resolution applications [8], [9]. However, typical integrating ADCs quantize the time window by counting a reference clock, which largely constrains them to low-frequency applications. As digital delay-line-based TDCs can now achieve time resolutions on the order of picoseconds (e.g., 4.7 ps in [3]), they can achieve a much higher speed of AD conversion if used in place of counters. In this brief, we will study the issue of using delay-line-based TDCs in ADCs. Specifically, we will compare different TDC structures for use in ADCs and study the effects of nonideal factors such as noise and mismatch on ADC performance.

Another way of using delay lines in ADCs is the *voltage-to-delay-to-digital* scheme: The input signal modulates the delay per buffer instead of the time window (Fig. 3), and thus, the

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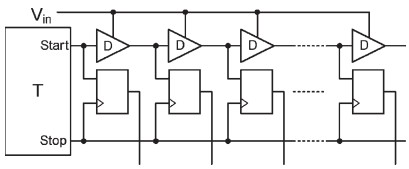

Fig. 3. Illustration of voltage-to-delay-to-digital ADCs.

number of delay cells the signal passes through in a constant time window is proportional to the input voltage. A recent work [10] has reported a 14-bit 10-kS/s ADC, which embodies this idea. A parallel version achieves 12 mV/LSB, 40 MS/s, over a 600-mV full-scale voltage [14]. In this brief, we will discuss the tradeoffs between speed, resolution, and linearity, particularly in high-speed implementations. As an illustration, we will present a 4-bit, 1-GS/s ADC simulated in 0.13-μm and 65-nm CMOS processes, which shows compatibility with technology scaling.

A major advantage of the delay-line-based structure lies in its all-digital implementation, which makes it compatible with technology scaling. In addition, the delay-line structure introduces time-domain amplification into the design and potentially leads to better solutions. In particular, signal can be "amplified" in the time domain by simply extending the time window, in contrast to voltage amplification involving a complicated analog amplifier. This is particularly attractive to weak-signal acquisition and will be discussed in more detail.

The rest of the brief is organized as follows: In Sections II and III, we will talk more about the voltage-to-time-to-digital and the voltage-to-delay-to-digital ADCs, respectively. In Section IV, we will discuss a few advanced structures based on delay lines. In Section V, we will talk about the effect of jitter and mismatch. In Section VI, a prototype implementation is described. Finally, we conclude this brief in Section VII.

II. Voltage-to-Time-to-Digital ADCs

As mentioned in Section I, there are several structures of delay-line-based TDCs. It is desirable to compare them in the context of ADC (Fig. 2). Functionally, the vernier and the pulse-shrinking delay lines are the same, whereas the time-interpolation structure can be considered to be the same as the basic structure but with a smaller delay per stage [3]. Hence, we only need to compare the basic and the vernier delay lines.

Consider quantizing voltage $V_{\rm in} \in [V_a, V_b]$ with an R-bit resolution. Assume that the intermediate time window $T(V_{\rm in}) \in [T_a, T_b]$ is a linear function of $V_{\rm in}$. For the basic structure

$$T_b - T_a = D \cdot 2^R \tag{1}$$

where D is the delay per buffer. Thus, omitting pre- and postprocessing, the conversion time is given by the longest time window $\Delta + T_b = \Delta + T_a + D \cdot 2^R$, in which Δ is the time taken by the voltage-to-time converter to generate the "Start" signal. Similarly, for the vernier structure, we have

$$T_b - T_a = \delta \cdot 2^R \tag{2}$$

and the conversion time is $\Delta + T_b(D/\delta) = \Delta + T_a(D/\delta) + D \cdot 2^R$. Interestingly, although the vernier structure achieves a higher resolution in the time domain, and thus the intermediate time window $T(V_{\rm in})$ can be smaller than the basic delay-line case, this does not mean that it is faster in completing conversion.

In addition, the vernier structure suffers more from mismatch and jitter. Assume that, in a single delay line with noise and mismatch, the timing error of the rising edge arriving at a certain stage is τ. In the basic structure, this is equivalent to an input voltage error of LSB $\cdot\, \tau/D$; in the vernier structure, as two delay lines are used, the input-referred error is LSB $\cdot\, \sqrt{2}\tau/\delta$. This error is interpreted as nonlinearity or input-referred noise, which will be discussed in more detail in Section V.

III. Voltage-to-Delay-to-Digital ADCs

As shown in Fig. 3, denote the delay per cell by $D(V_{\rm in})$, which is modulated by the input voltage. In T seconds, the signal passes through $N_Q(V_{\rm in}) = \lfloor (T/D(V_{\rm in})) \rfloor$ delay cells, in which $\lfloor x \rfloor$ is the integer part of x. Generally, $D(V_{\rm in})$ is monotone in the range of interest $[V_a, V_b]$, and $N_Q(V_{\rm in})$ ranges between $\lfloor N(V_a) \rfloor$ and $\lfloor N(V_b) \rfloor$. Thus, the number of bits is

$$R \approx \log_2 T |V_a - V_b| \cdot \left| \frac{1}{D^2(V)} \frac{dD(V)}{dV} \right|_{V=V^*} \tag{3}$$

where V^* is a constant in $[V_a, V_b]$. A similar expression is also mentioned in [10] and [11]. Equation (3) shows that a delay block with a small delay and sensitive to the control voltage is desirable to achieve a high resolution. More importantly, (3) reveals the basic tradeoff between time and resolution. That is, the number of bits R can be increased at the cost of a larger time interval T, which is a kind of amplification in the time domain. This is useful for weak-signal acquisition, where resolution is the primary concern, whereas the sampling rate can be relatively low.

In terms of linearity, it is desirable to have delay cells with $D(V_{\rm in}) = (D_0/(V_{\rm in} + V_0))$, where D_0 and V_0 are constants. Efforts have been made to design delay cells achieving better linearity [11]–[13]. However, it is usually the case that this relation can only be approximated within a relatively small range. In this case, another tradeoff between speed and linearity comes into play: As revealed by (3), high conversion speed requires the time interval T to be small, whereas good linearity requires the dynamic range $|V_a - V_b|$ to be small.

IV. Advanced Structures Based on Delay Lines

Based on the foregoing discussion, the length of the delay line exponentially grows with the number of bits R, such as in Flash ADCs. The relationship causes some difficulties in implementation. For example, the sample-and-hold (S/H) circuit needs to drive a large number of voltage-controlled delay cells, which makes it difficult to deliver the control signal on-chip, particularly for high-speed applications. In addition, as will be discussed in Section V, nonlinearity due to mismatch linearly grows with the length of the delay line. Hence, it is desirable to reduce the length of the delay line. A ring delay line [10], [11] provides a good solution. Specifically, the output of the last delay cell is fed back to the first stage to form a loop, and a counter is used to count the number of cycles. As will be discussed in Section V, the linearity of a ring delay line is superior to that of a single long delay line.

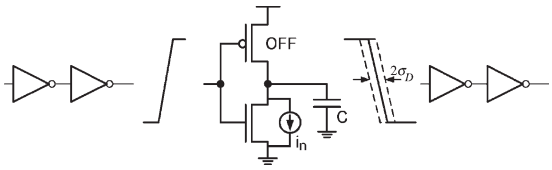

Fig. 4. Jitter in inverter-based delay lines.

As discussed earlier in this brief, the speed and resolution tradeoff is given by $R \propto \log_2 T \propto \log_2(1/f_s)$, where R is the number of bits, T is the time required to complete conversion, and f_s is the sampling frequency [10], [11]. Clearly, increasing the resolution by one bit doubles the conversion time T and, thus, lowers the sampling frequency f_s by half. This is a constrain set by the delay cells. In addition to designing delay cells with a shorter delay, parallel [14] and pipeline structures can relax this constrain: In n-channel parallel ADCs, it is $R \propto \log_2(n/f_s)$, and in n-stage pipeline ADCs, it becomes $R \propto n \log_2(1/f_s)$. Both methods are widely used to build high-performance ADCs from simpler ones, but we will not go into details here.

V. Jitter and Mismatch

In real systems, nonideal factors such as noise and mismatch put a constrain on the best achievable performance. In the context of delay lines, noise leads to uncertainty in the propagation delay, namely, jitter (Fig. 4), whereas mismatch between delay cells distorts the transfer function and impairs linearity. In this section, we will evaluate these effects. The analysis is largely based on the *voltage-to-time-to-digital* case, but it can easily be extended to the *voltage-to-delay-to-digital* case.

A. Jitter and Resolution

Jitter is widely studied in the design of ring oscillators [15]. When white noise dominates,[1] the jitter introduced by each stage is independent of one another, and the variance of jitter in T seconds is $\sigma_T^2 = \kappa^2 T$ [16]. That is, jitter linearly accumulates with the number of delay cells the signal passes through. In ADCs, as D corresponds to LSB, this jitter is equivalent to an input voltage noise of power $\text{LSB}^2 \cdot \sigma_T^2/D^2$.

Delay lines based on inverters and differential inverters were studied in [15]. For the inverter in Fig. 4, the delay is given by $D = CV_{\text{DD}}/I_N$, and the jitter is $\sigma_D^2 = D \cdot 4kT\gamma_N/I_N(V_{\text{DD}} - V_{\text{th}})$, in which $I_N = (1/2)\mu_n C_{\text{ox}}(W/L)(V_{\text{DD}} - V_{\text{th}})^2$. It follows that the largest input-referred voltage noise is

$$\text{LSB}^2 \cdot \frac{N \cdot \sigma_D^2}{D^2} = \text{LSB}^2 \cdot \frac{8kT\gamma_N \cdot N}{C \cdot V_{\text{DD}}(V_{\text{DD}} - V_{\text{th}})}. \quad (4)$$

In addition, it is easy to find that the energy consumed per AD conversion is $N \cdot CV_{\text{DD}}^2$. For a given process, to reduce the input-referred noise power by half, one needs to double C and, thus, double the energy consumption. Fortunately, this does not necessarily increase D, which depends on I_N and C.

It is worth comparing the delay line with the resistor ladder in Flash ADCs. Assume that the input capacitance of comparators in Flash ADCs is C and that $\text{LSB} = V_{\text{DD}}/N$. The input-referred noise induced by the resistor ladder is $(4k/C) = \text{LSB}^2 \cdot (N^2/V_{\text{DD}}^2) \cdot (4k/C)$. In comparison with (4), the delay-line-based ADC generally shows smaller input-referred noise, particularly for large N.

[1]Low-frequency noise such as flicker noise slowly varies over a long time and can be treated in the same way as mismatch here.

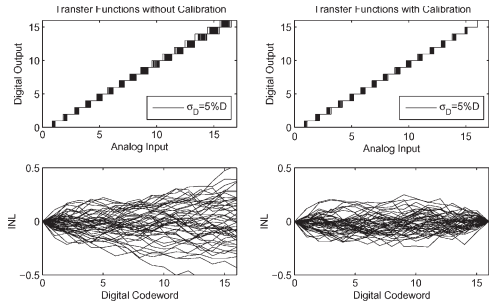

Fig. 5. Nonlinearity due to mismatch: (left) without and (right) with calibration. The x-axis, labeled "Analog Input," refers to the time window $T(V_{\text{in}})$ or, equivalently, the input voltage V_{in}, which are linearly related in the voltage-to-time-to-digital design.

To get a quantitative idea about the achievable performance in state-of-the-art designs, we draw on published data on the phase noise of ring oscillators. Phase noise describes the same phenomenon as jitter, but in the frequency domain. Specifically, due to noise, the output spectrum of the oscillator spreads around its fundamental frequency, instead of being a single tone. The power spectrum density at $f_0 + \Delta f$ is expressed as "decibels below the carrier per hertz," which is denoted by $L\{\Delta f\}$. It was proved in [16] that $\kappa = (\Delta f/f_0) \cdot 10^{-L\{\Delta f\}/20}$, by which jitter can be derived from the reported phase noise. Twenty-six low-phase-noise ring oscillators were reported in [16], which are built on inverters, current-starved inverters, and differential inverters, respectively. Take design No. 11 as an example, which is in a 0.25-μm, 2.5-V CMOS process. It consists of $N = 19$ current-starved inverters and consumes a 3.9-mA current. $f_0 = 959$ MHz, and $L\{\Delta f = 1\text{ MHz}\} = -110.9$ dBc/Hz. Thus, the delay of each stage is $D = (1/Nf_0) = 55$ ps, and $\kappa = 3.3 \times 10^{-9}$ $\text{s}^{0.5}$. Using such delay cells in ADCs, the largest input-referred noise power is

$$\text{LSB}^2 \cdot \frac{\sigma_T^2}{D^2} = \text{LSB}^2 \cdot \frac{\kappa^2 \cdot ND}{D^2} = 2N \times 10^{-5} \cdot \text{LSB}^2.$$

For $N = 2^{15}$, $\sigma_T^2/D^2 = 0.66$, and for $N = 2^{10}$, $\sigma_T^2/D^2 = 0.02$. Thus, more than a 10-bit resolution is possible with this delay cell.

B. Mismatch and Nonlinearity

Due to local variation in temperature and process,[2] the delay of a delay cell can be different from one another, which leads to unequal separations between thresholds and impairs linearity. This is illustrated in Fig. 5, in which the transfer functions and integral nonlinearity (INL) curves of 50 random samples are plotted.

Consider a chain of N delay cells. Denote the actual delay of the nth cell by $D_n = D + \Delta D_n$, where D is the nominal delay,

[2]Global variation affects all delay cells in the same direction and does not impair linearity. It changes the slope of the transfer function (i.e., LSB) [14], which can be calibrated by means of delay-locked loops [3] or digital calculation [14].

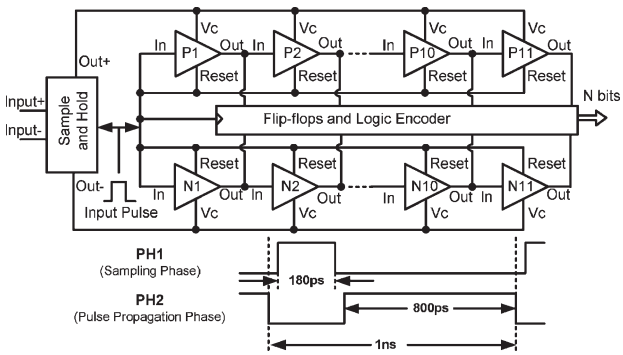

Fig. 6. Block diagram of the delay-line-based ADC and timing phases.

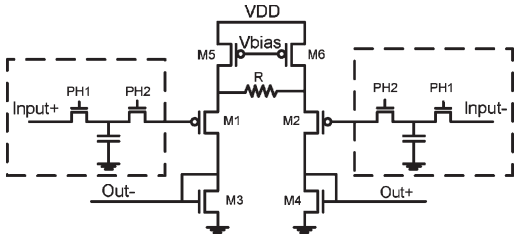

Fig. 7. Input S/H and voltage-to-current converter.

and ΔD_n is a zero-mean random error with variance σ_D^2. As D corresponds to LSB, it is easy to get $\mathrm{DNL}_k = \Delta D_k / D$ and $\mathrm{INL}_k = \sum_{n=1}^{k} \Delta D_n / D$ for the kth codeword, with variances $\sigma^2_{\mathrm{DNL}_k} = \sigma_D^2/D^2$ and $\sigma^2_{\mathrm{INL}_k} = k \cdot \sigma_D^2/D^2$, respectively. As illustrated in Fig. 5, $\sigma^2_{\mathrm{INL}_k}$ accumulates and is maximized at $k = N$. For $\sigma_D = 5\%D$, $\sigma^2_{\mathrm{DNL}_k} = 1/400$ and $\sigma^2_{\mathrm{INL}_k} = k/400$. That is, for 5% mismatch, a chain of less than 400 stages can keep INL below 1 with a high probability.

When calibration measures such as delay-locked loops [3] are taken, the total delay of the chain $ND + \sum_{n=1}^{N} \Delta D_n$ is adjusted to a reference ND. Thus, the actual delay becomes

$$D_n = \frac{ND \cdot (D + \Delta D_n)}{ND + \sum_{n=1}^{N} \Delta D_n} \approx D + \Delta D_n - \frac{1}{N} \sum_{n=1}^{N} \Delta D_n.$$

In this case, for the kth digital codeword

$$\mathrm{DNL}_k = \frac{\Delta D_k - \frac{1}{N} \sum_{n=1}^{N} \Delta D_n}{D} \qquad \sigma^2_{\mathrm{DNL}_k} = \frac{N-1}{N} \frac{\sigma_D^2}{D^2}$$

$$\mathrm{INL}_k = \sum_{m=1}^{k} \mathrm{DNL}_m \qquad \sigma^2_{\mathrm{INL}_k} = \frac{(N-k)k}{N} \frac{\sigma_D^2}{D^2}.$$

In contrast to the previous case without calibration, the maximum $\sigma^2_{\mathrm{INL}_k}$ is $(N/4) \cdot \sigma_D^2/D^2$ and occurs at $k = N/2$, which is shown in Fig. 5. For 5% mismatch, the chain can be as long as 1600 stages while keeping INL below 1.

At this point, it is worth mentioning the improvement in linearity due to the ring structure. Assume that a ring delay line consisting of M delay cells is used in place of a delay line of length $N = M \cdot K$. After calibration, the delay of K cycles in the loop is equal to the reference $N \cdot D$, and thus, the delay of one cycle is equal to $(N \cdot D)/K = M \cdot D$. Thus, in terms of linearity, this loop is equivalent to a delay line of length M, with $\max\{\sigma^2_{\mathrm{INL}_k}\} = (M/4) \cdot \sigma_D^2/D^2$. This is only $1/K$ of that of a delay line of length $N = M \cdot K$.

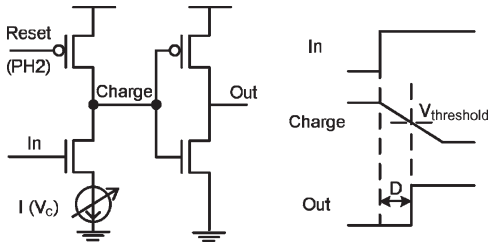

Fig. 8. Illustration of the delay cell.

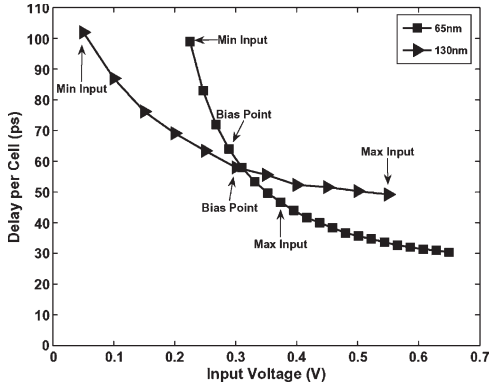

Fig. 9. Delay characteristics of a delay cell in 0.13 μm and 65 nm.

VI. Prototype Implementation

As an illustration, a 4-bit, 1-GS/s *voltage-to-delay-to-digital* ADC was designed in both 0.13-μm and 65-nm CMOS processes. To make a fair comparison, we use the same circuit blocks for the two processes, but they are optimized in each process for minimum power consumption.

As shown in Fig. 6, we use a differential structure to achieve better linearity, in which two identical delay lines are controlled by differential voltages. Each conversion period has two phases: 1) sampling phase and 2) pulse propagation phase. In the sampling phase, S/H gets new samples, and the delay cells are reset. In the pulse propagation phase, the input rising edge propagates in the delay line at a speed determined by the sampled voltage.

The S/H circuit shown in Fig. 7 consists of the input switching network and differential inputs that convert the input voltage difference to differential voltages applied to the positive and negative delay lines. The bias point of the delay cell and the conversion gain (determined by R) are optimized for the highest possible linearity.

The delay cell is shown in Fig. 8. The input node of the inverter, which is denoted by "Charge," is precharged to the high level by reset (PH2). When a rising-edge signal comes to the input of the delay cell, the voltage-controlled current source begins to discharge the "Charge" node. The voltage goes down at a rate proportional to the current $I(V_c)$. When the voltage falls below a threshold, the output of the inverter goes high. The delay is controlled by V_c, which comes from the S/H circuit. To have a large dynamic range, the intrinsic delay of the inverter is made much smaller than the time required to discharge its input node. The delay characteristic of this cell and the bias point and the delay swing for the delay cells in the two designs are plotted in Fig. 9.

Simulation results are summarized in Table I. In particular, the INL and differential nonlinearity (DNL) of the 130-nm

TABLE I
PROTOTYPE PERFORMANCE SUMMARY

Technology	0.13μm CMOS	65nm CMOS
Sampling Rate	1GS/s	1GS/s
Differential input range	1V p-p	0.3V p-p
Resolution	4 bits	4 bits
ENOB	3.42 bits	3.01 bits
SNDR(@ 1GS/s)	22.37dB	19.9dB
SFDR(@ 1GS/s)	28.2dB	25.2dB
Supply Voltage	1.2V	1.2V
Total Power	2.4mW	1.02mW
Area	$100 \times 150\mu m^2$	-

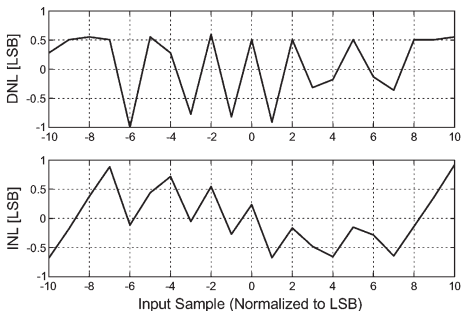

Fig. 10. INL and DNL of a delay-line-based ADC prototype.

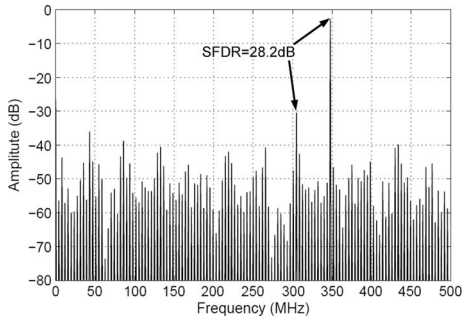

Fig. 11. Output spectrum for a 350-MHz sinusoid input.

ADC are shown in Fig. 10. The fact that INL exceeds 0.5 LSB causes the effective number of bits (ENOB) of the ADC to degrade to less than 4 bits. High-frequency simulation is also done by applying a 350-MHz input. The 512-point fast Fourier transform shown in Fig. 11 shows a total signal-to-noise-plus-distortion ratio (SNDR) of 22.37 dB, which provides an ENOB of $((\text{SNDR} - 1.76)/6.02) = 3.4$.

The delay-line ADC is compared with other reported ADCs using the figure of merit (FOM) proposed in [17], i.e.,

$$\text{FOM} = \frac{\text{Power}}{2^{\text{ENOB}} \times \min(2f_{\text{in}}, f_{\text{sample}})}.$$

As shown in Fig. 12, the new structure shows high power efficiency. The authors acknowledge that the comparison becomes more accurate with chip measurement results. However, the fact that the ADC becomes more power efficient with scaling is illustrated in the comparison and strongly supports the scalability of the delay-line-based ADC and its better performance in further scaled CMOS.

VII. CONCLUSION

We have discussed the delay-line-based design of ADC, which is mainly implemented using digital blocks and is compatible with process scaling. It also introduces a new degree of freedom of amplifying signals in the time domain.

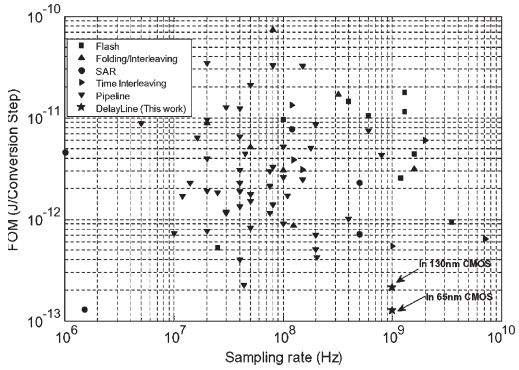

Fig. 12. Comparison of the proposed ADC with other reported ADCs.

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