A 48-dB DR 80-MHz BW 8.88-GS/s Bandpass ΔΣ ADC for RF Digitization with Integrated PLL and Polyphase Decimation Filter in 40nm CMOS

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Abstract

A 2.22GHz 4th-order BP ΔΣ ADC has been realized in 40nm CMOS. The test chip contains a complete system consisting of the ADC core, the PLL with clock generation network, and the digital decimation filters and downconversion (DFD). The quantizers are 6 times interleaved enabling a polyphase structure for the DFD and relaxing speed requirements. Sampled at 8.88GS/s the ADC achieves a DR of 48dB in a band of 80MHz with an IIP3 of +1dBm.

Keywords: ΔΣ ADC, RF bandpass filters, decimation

Introduction

As technology scaling continuously improves the performance of digital circuitry, there is a strong drive towards real software radios where most of the functionality is implemented in the digital domain [1]. Within the paradigm of a software receiver, the ADC is shifted towards the antenna. Although the requirements regarding dynamic range and linearity are prodigious, this work shows the feasibility of such systems by implementing a complete CT BP ΔΣ ADC including PLL and digital post-processing in a 40nm digital CMOS technology whereas SoA RF BP ΔΣ ADCs only report the modulator design (e.g., [2]–[4]]). Compared to previous prototype [3] which only contained the core ADC, the quantizers and FB path are redesigned for operation at 8.88GS/s.

Architecture overview

In Fig. 1, a schematic representation of the RF ΔΣ ADC is depicted. The 4th-order BP filter contains two G_m-*LC* resonators with a center frequency f_c of 2.22GHz, and a feedforward path with an addition operation embedded in the comparators. The effective sampling rate of $4f_c$ = 8.88GS/s is realized by interleaving 6 quantizers of 1.5 bit. Their parallel outputs are fed into a polyphase downconversion filter.

In the feedback path, the outputs of the comparators are multiplexed to form the input stream for the single DAC with NRZ pulses. A retiming operation at half the clock speed minimizes the impact of comparator metastability. The clock signal is generated by an on-chip PLL [5] with programmable division factor *N* using a 60MHz reference.

The center frequency, quality factor and gain of the resonators, the threshold levels of the quantizers and the output levels of the DAC are tuned by a controller for calibration. Further, to ensure loop stability, a variable loop delay (τ) is available realized by delaying the sampling clock with respect to the clock used to generate the DAC pulses.

Implementation of building blocks

A. Loop filter

The two resonator tanks of the loop filter are built with standard 4nH 4-turn differential inductors in parallel with a MoM capacitor and binary-weighted NMOS varactors to adjust the center frequency. Tunable negative resistances made of cross-coupled NMOS pairs compensate for tanks losses and enhance the quality factors. The complete filter achieves 40dB in-band gain and can be adjusted to different center frequencies from 2.2GHz up to 2.4GHz.

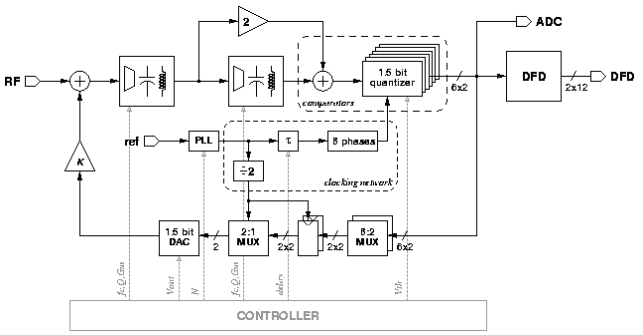

Fig. 1: Architecture of the continuous-time bandpass ΔΣ ADC.

B. Quantizer and feedback path

Details of the quantizers and circuits in the feedback path are shown in Fig. 2. The high sampling speed required a new approach for this path compared to previous implementations. For the 1.5-bit quantizer, two times 6 comparators are interleaved. A binary-weighted capacitor bank on the preamplifier output nodes sets the threshold level. Parallel PMOS input pairs in the preamplifier realize the weighted addition of the feedforward path. By avoiding an extra adder stage, loop delay is minimized and power consumption is reduced.

The duty cycle of the quantizer clocks is 33% which allows performing a 6-to-2 multiplexing by NANDing three non-overlapping outputs from the 6 interleaved comparators. After retiming, the two interleaved streams are multiplexed again by multiplying them with a clock signal at half the sampling frequency. The 4-quadrants multiplier faces a tunable resistor as load and acts as a Swing-Reduced Driver ensuring the DAC switches remain in saturation. For proper behavior of the common source node, the DAC uses a switched NMOS current source topology with paths to the positive, negative and supply nodes.

C. Clocking network

The clock generation circuit receives the 8.88GHz signal from the on-chip PLL which is divided by two for the DAC and retiming latches. A variable delay line made of digitally programmable NMOS capacitors is used to set the loop delay to 4 feedback clock cycles to stabilize the loop. The six-phase clock for the comparators is generated with a similar ring of 12 high-speed flip-flops as used in [2].

D. DFD

Based on the RF BP ΔΣ ADC architecture, it is natural to derive an architecture for the DFD with a quadrature mixer (driven by a digital LO at $f_S/4$) followed by two decimations to bring the sample rate from 1.48Gs/s to 185Ms/s (Fig. 3). The decimation filters are based on CIC filters because their

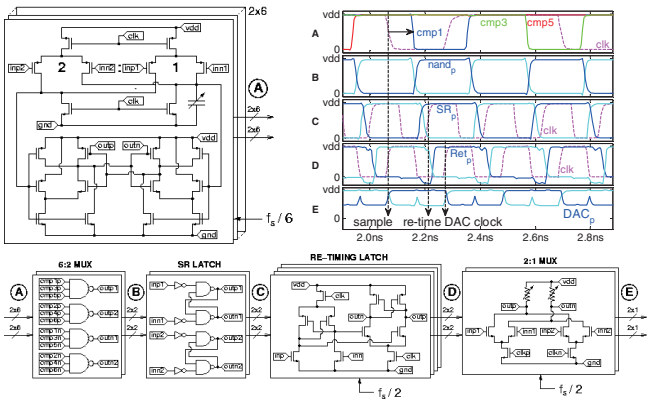

Fig. 2: Details of quantizer and feedback path with typical signals.

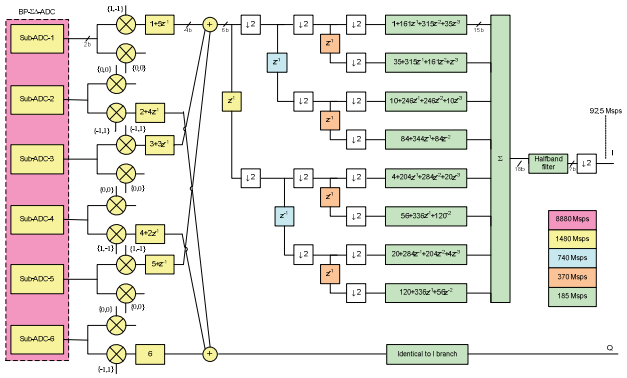

Fig. 3: Architecture of DFD.

coefficients are all 1s which are equivalently implemented with FIRs or IIRs filters. The quadrature mixer and decimation stages lend themselves to a very efficient implementation [6], which minimizes the power consumption. The first decimation filter consists of 2 CIC-6 filters. These filters and the mixers are jointly implemented in a polyphase structure exploiting the interleaved ADC output. The second decimation filter consists of 4 CIC-8 filters implemented with an alternate simpler form which is only possible for decimations by a power of 2. After the two decimation stages, a halfband filter provides the required selectivity to extract the desired band.

Measurements

Fig. 4 shows the micrograph of the system implemented in 40nm LP CMOS technology. This technology has been chosen for the low power and low leakage aspects, as the design is always on and lacks clock gating possibilities. The core ADC (filter, comparators, DAC and clock network) and PLL consume 109mA and 48mA from a 1.5V supply, respectively. The digital core consumes 13mA, operating at 1.1V. The PLL has a measured integrated phase noise of -25dBc.

The outputs of the comparators or the DFD were measured with a high-speed logic analyzer. For testing purposes, the input of the DFD could also directly be applied.

In Fig. 5, the SNDR and SFDR of the core ADC are plotted as a function of the input power for a BW of 80MHz. Two tones 5MHz apart are used as RF inputs to evaluate nonlinear effects. The DR is as high as 48dB. Fig. 5 also depicts an output spectrum with the in-band noise and spurious tones shown in different color. Main performance limitation is noise caused by jitter originating from pseudo-differential implementation of clocking circuitry and buffers.

Fig. 6 shows the SNDR measured at the output of the ADC for a single tone swept over the entire 80MHz band. As the actual

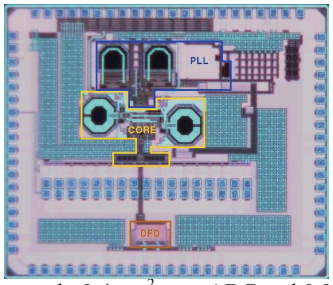

Fig. 4: Chip micrograph: 0.4mm^2 core ADC and 0.06mm^2 DFD.

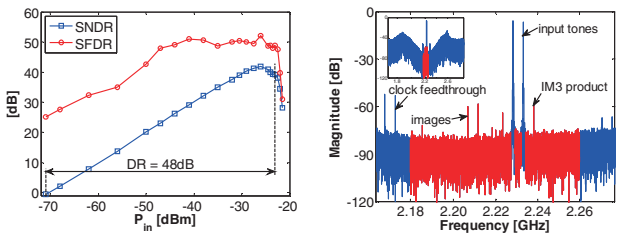

Fig. 5: Measured SNDR and SFDR and two-tones output spectrum.

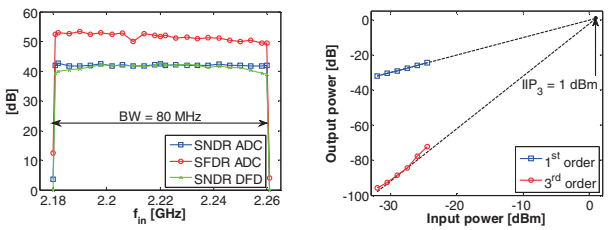

Fig. 6: SNDR variation with input frequency and IIP3 measurement.

DFD implementation suffers from an overflow, the results of a DFD simulation incorporating saturation logic are shown in Fig. 6 using the measured ADC outputs as input. The limited SNDR degradation shows that the DFD architecture is a good approach for this system. An IIP3 of 1dBm was measured for the ADC as shown in Fig. 6.

Conclusions

An RF BP ΔΣ ADC in 40 nm digital CMOS has been presented. The chip contains also the PLL for generating the 8.88GS/s sampling clock, and the digital post-processing for downconversion, filtering and decimation. Furthermore, the system is made very tunable to compensate for inevitable process variations. Despite some performance limitations, these properties make it a demonstrator for the feasibility of full software receivers in deep submicron technologies.

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