A 20GS/s Low-Power BiCMOS Comparator Using an Active Inductor Load

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***Abstract*-A 20GS/s BiCMOS latched comparator for high-speed, low-power Analog-to-Digital Converter (ADC) is proposed. The resister load of conventional current-steering comparator is replaced by an active inductor load made by a MOS transistor and a resister. This solution extends the bandwidth of the circuit without excessive power dissipation. Implemented in 0.35μm SiGe BiCMOS technology, this comparator only occupies a die area of 97×67 μm2 with a power dissipation of 31 mW from a 3.3-V power supply. Operating with an input frequency of 2 GHz, the circuit can oversample up to 20 GS/s with 4 bits of resolution; while operating at Nyquist, the comparator can sample up to 20 GS/s with 3 bits resolution. This design achieves a considerable trade-off between power, speed and resolution.**

I. INTRODUCTION

Silicon germanium (SiGe) heterojunction bipolar transistors (HBTs) have become attractive for high-speed and millimeter wave (mm-wave) applications. The high cutoff frequency of advanced SiGe HBTs has led to a new breakthrough in speed-record being reported.

In general, high- f_T HBT technology can bring much higher speed at the cost of power and area[2][3][12]; while the power dissipation of CMOS comparators is much less than HBT comparator but with poor sampling rate [4][5]. To date, few effective methods have been proposed to reduce the power consumption in high-speed SiGe HBT designs. As reported, comparators in BiCMOS technology used for this work could be exploited to achieve the trade-off between operating speed and power dissipation [1][6][10][11].

In this paper, the design and implementation of a high-speed comparator working at a sampling rate of 20 GHz with a resolution of 4 bit is presented. The comparator consists of a pre-amplifier stage, a core latching comparator and an output buffer. The pre-amplifier is designed with high- f_T (~55 GHz) HBT to lessen the overdrive recovery time and offer sufficient gain for the latch (short for latching comparator). The latch, which consists of two stages, amplification and regenerative, is designed to compare two voltage levels and produce the digital decision speedily as possible. In order to reduce the regeneration time and tracking time, an active inductor is placed as the load. The output buffer made up of a differential amplifier is designed to produce well defined digital data.

The details of the comparator design are discussed in Section Ⅱ. Section Ⅲ describes the layout of the comparator. Simulation results of the comparator are presented in Section Ⅵ, followed by a conclusion.

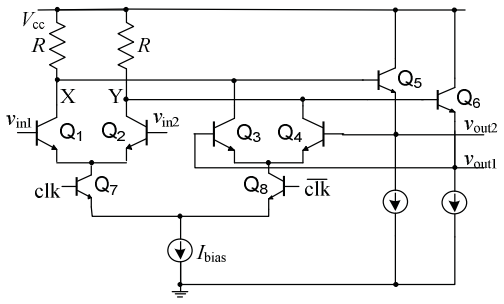

Figure 1. Schematic of the conventional D-Latch

II. HIGH-SPEED LATCHED COMPARATORS

A. BiCMOS D-Latch

In order to improve the speed of comparator, circuits with positive feedback are commonly used, like the well-known D-Latch of Fig. 1[8].

When *clk* is in high level namely the latch operates in tracking phase, the latch tracks the amplified input signal available at pre-amplifier output. Meanwhile, Q_3~Q_6 not work. When *clk* turns to low level, the latch runs in regenerative mode and produces digital decision in high speed as possible. During this period the pre-amplifier also has enough time for overdrive recovery and re-setup before the next tracking phase.

It has been reported [7] that the maximum sampling rate of the latch is determined by the recovery time t_{rec}, which is defined as the time required by the gate differential pair's output voltage to change from a stable logic state to the midpoint of the logic state when the latch is switching from the latching mode to tracking mode. The recovery time and the bandwidth of the differential amplifier (f_{3dB}) can be expressed as [8][14]

$$t_{rec} = R_L C_{total}\left(1+\frac{1}{\tanh(delt(V_{in})/2V_T)}\right) \quad (1)$$

$$f_{3dB} \approx 1/2\pi R_L C_{total} \quad (2)$$

where R_L is the load resistance, C_{total} is the total capacitance at collector of differential pair (Q_1-Q_2), ΔV_{in} is the differential input voltage of the latch, and V_T is the thermal voltage. As well, the expression of regeneration time constant τ_{reg} and tracking time constant τ_{tra}, is [13]

$$\tau_{reg} = \frac{R_L C_{total}}{g_m R_L - 1} \quad (3)$$

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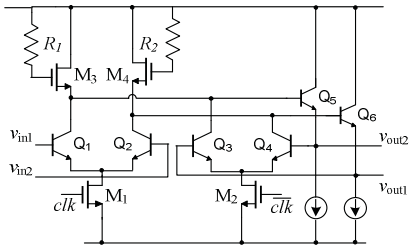

Figure 2. Schematic of proposed D-Latch with an active inductor load

$$\tau_{tra} = R_L C_{total} \tag{4}$$

where g_m is the transconductance of the HBTs in the second differential pair (Q_3-Q_4). According to the two expressions, a small R_L will shorten the recovery time but limit the output swing, thus degrade the latch's operation. On the contrary, a large R_L can bring a considerable output swing at the cost of increasing recovery time [9]. As the same, a small size of Q_3~Q_6 means small C_{total} and will reduce recovery time, whereas results in small gain [1]. In fact, recovery time and output swing pose conflicting requirements on the load resistance, so that higher sampling frequencies can only be achieved by increasing current consumption.

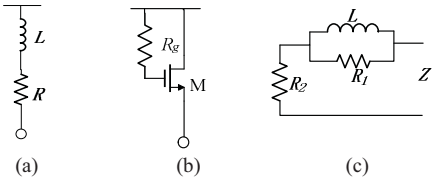

Figure 3. Inductors and their equivalent circuit
(a)Spire inductor; (b) Active inductor; (c) Equivalent circuit of (b)

With reference to previous works, e.g., [13] and [14], the regeneration time constant τ_{reg} and the tracking time constant τ_{tra} can be reduced by placing inductors in series with the load resistors, thereby increasing the maximum sampling speed for a given power consumption. According to [13], the regeneration time constant (τ_{reg}) with an inductance L is given by

$$\tau_{reg} = \frac{2}{(\frac{g_m}{C_{total}} - \frac{R_L}{L}) + \sqrt{(\frac{g_m}{C_{total}} - \frac{R_L}{L})^2 + 4(\frac{g_m R_L - 1}{LC_{total}})}} \tag{5}$$

The tracking time constant (τ_{rec}) with an inductance L is given by

$$\tau_{tra} = \frac{R_L C_{total}}{\sqrt{(\frac{-m^2}{2} + m + 1) + \sqrt{(\frac{-m^2}{2} + m + 1)^2 + m^2}}} \tag{6}$$

with

$$m = R_L^2 C_{total} / L \tag{7}$$

As area required for passive inductor is always very large, and the inductance of passive inductor is hard to change, active inductor becomes the most promising component to realize the configuration mentioned above.

As showed in Fig. 3, (a) is a normal spire inductor. The inductance is L, and R is the equivalent resistor of the spire inductor. Fig. 3(b) is an active inductor made up of an nMOS and a resistor. Fig. 3(c) is the simplified equivalent circuit of (b). According to (b), the equivalent input impedance can be show as [15]

$$Z = \frac{1 + R_g s C_{gs}}{g_m + s C_{gs}} \tag{8}$$

According to (8), when s=0, $|Z|$=$1/g_m$; when s=∞, $|Z|$=R_g. Thus if $R_g \gg 1/g_m$, $|Z|$ will increase with the raising of frequency. This means the combination of nMOS and resistor present the characteristic of inductor. The equivalent circuit of the active inductor is shown in Fig. 3(c). The expressions of L, R_1 and R_2 are shown as follows [15]:

$$L \approx C_{gs}\left(G_g - 1/g_m\right)/g_m \tag{9}$$

$$R_1 \approx R_g - 1/g_m \tag{10}$$

$$R_2 \approx 1/g_m \tag{11}$$

As the value of $1/g_m$ is usually very small, R_1 is about the same with R_g. Thus, according to (9), we can obtain a required inductance of L by choosing a suitable R_g.

The proposed BiCMOS D-Latch, illustrated in Fig. 2, is an innovation of the conventional scheme. This new D-latch is formed with two cross-coupled differential pairs (Q_1~Q_4) activated by 2-φ current switching clocks. The resistor load is replaced by an active inductor mentioned above. The full-rate clock is applied to the input device with the lower f_T, nMOS differential pair (M_1 & M_2). A smaller time constant at this node is more important in maximizing the switching speed. As having higher slew rate which result in fast rise and fall times, HBTs are used for the upper level signal inputs.

The simulation result shows that, with eclectic R_1, R_2, M_3 and M_4, the recovery time is brought down to 9.6 ps, which is sufficient for operation at a 20 GHz sampling rate.

B. Pre-Amplifier

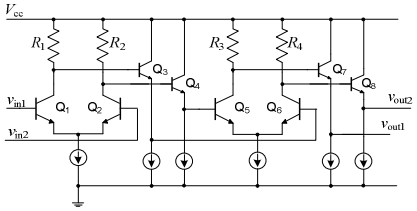

Figure 4. Schematic of two-stage pre-amplifier

Pre-amplifier is introduced to improve sensitivity to small input signals by suppressing the kick-back noise created by the switching of the latch and decreasing the offset voltage due to device mismatch of the following stages. The gain expected of the pre-amplifier is determined by the substantial offset voltage and noise accumulated by the latch. With higher differential voltage to the CMOS latch, the regeneration time of the latch can be reduced and accordingly the conversion speed can be improved.

The schematic of pre-amplifier is shown in Fig. 4. Two different amplifiers in cascade are used to produce a high GBW with a gain distribution of ~14dB and ~26dB. To give a faster response and shorter recovery time, the gain of the first stage is designed lower than the second one. With two stages, the pre-amplifier can achieve not only high gain, but also a suitable bandwidth and a small input capacitance which is

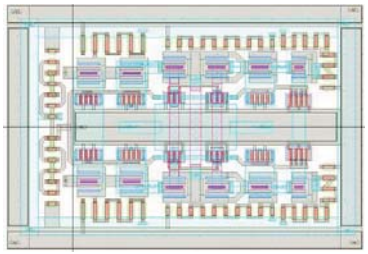

Figure 5. Layout of the comparator

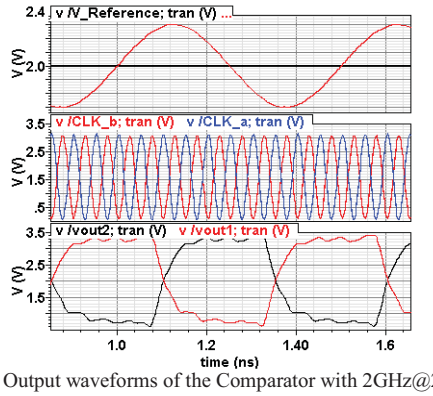

Figure 6. Output waveforms of the Comparator with 2GHz@20GS/s

expected at high operating speed. To mitigate the thermal mismatch of the input differential pair (Q_1-Q_2 and Q_5-Q_6) that may cause undesirably large input offset, a large emitter size and low current density were desired for the input transistor. A larger emitter size also results in a better physical matching of the transistor pair. However, larger emitter size means lower conversion speed. Thus a compromise should be made with the size of Q_1-Q_2 and Q_5-Q_6. Simulation results show the pre-amplifier delivering over ~40dB of gain and over ~22 GHz of -3dB bandwidth.

C. Output Buffer

From the output of the latch to the digital encoder of the comparator, an output buffer is required. The output buffer is made up of a simple differential amplifier. To ensure the gain of the buffer and mitigate the device self-heating, a large tail current and a large emitter size are provided for the

III. LAYOUT

The proposed comparator is laid out in double poly four metal 55 GHz, 0.35 µm BiCMOS technology. The use of differential signal in both the data and the clock paths leads to a fully symmetrical topology. To have better match between the devices, common centroid layout technique is adopted. Some dummy devices are placed around to provide an identical environment to reduce the random offsets caused by mismatch. The micrograph of the comparator is shown in Fig. 5 which takes an active area of 97×67µm^2.

IV. SIMULATION RESULTS

The simulation results, using SPECTRE (Cadence 5.1), show that, when operating of a 3.3V power supply, the comparator dissipates a total power of 31mW. With sine wave input and

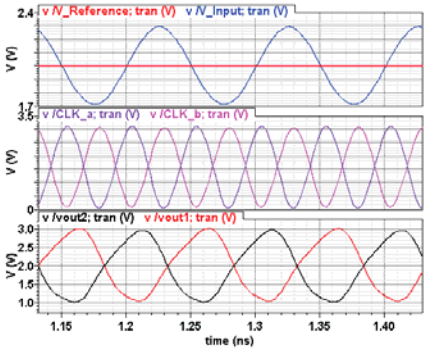

Figure 7. Output waveforms of the Comparator with 10GHz@20GS/s

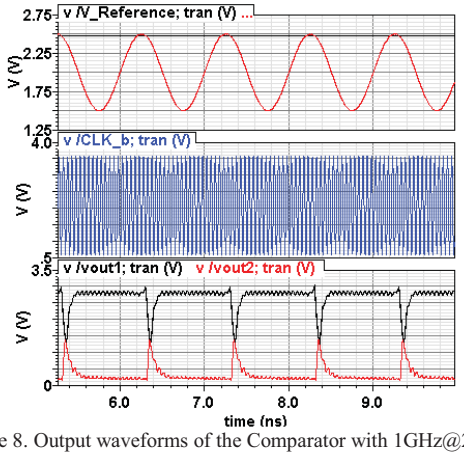

Figure 8. Output waveforms of the Comparator with 1GHz@20GS/s

Note: Simulation results under the critical condition

clock, the comparator was simulated under two differential conditions: (1) a 2 GHz input oversampled up to 20 GS/s; and (2) full Nyquist with sampling rate up to 20 GS/s. The output waveforms of the first condition are shown in Fig. 6. The output waveforms of the second condition are shown in Fig. 7. Fig. 8 shows the performance of the comparator operating under the most critical condition, which the DC voltage is very close to the peak of the sine wave when the input sine wave is 1GHz and the sampling clock is 20 GHz. This demonstrates that the comparator is well-suited for high-speed medium-resolution flash ADCs.

TABLE I
PERFORMANCE SUMMARY OF THE COMPARATOR

Parameters	Value
Supply voltage	3.3 V
Power Consumption	31 mW
Input Range	500 mV_{pp} max
Sampling Rate	20 GS/s max
Input Offset Voltage	<8 mV up to20 GS/s
Input Sensitivity	<10 mv (in/clk=10 GHz / 20 GS/s)

The performance of the comparator is summarized in Table Ⅰ. Comparisons of this work to other high-speed comparators are shown in Table Ⅱ.

TABLE Ⅱ

PERFORMANCE COMPARISON WITH PUBLISHED COMPARATORS

Ref.	Maximum Sampling rate [GS/s]	Sensitivity@ Input/Clock [@GHz/GS/s]	Supply Voltage [V]	Total Power Consumption [mW]	SiGe Process/fT [-/GHz]	Active Area [mm^2]
[2]	12.5	4mv@3.125/12.5	3.3	150	0.25μm HBT/190	0.0252
[3]	20	8.9mv@3/18	3.5	82	0.18μm HBT/120	0.0455
[6]	5	<4mv@1/4	3	89.04	0.5μm HBT/55	0.0582
[8]	32	<37mv@32	3.5	405	SiGe HBT/200	0.0226
[11]	12.5	N/A	2	1.09	0.12μm BiCMOS	N/A
[12]	16	N/A	N/A	80	0.5μm HBT/55	0.096
This work	20	<10mv@10/20	3.3	31	0.35μm BiCMOS/55	0.0065

V. CONCLUSION

In this paper, a high-speed, low power comparator has been designed and implemented in a 55 GHz 0.35μm SiGe BiCMOS technology. The comparator can provides good performance when oversample a 1 GHz input up to 20 GS/s or sample at Nyquist up to 20 GS/s, attaining 4.0 bits resolution. It can be opined that this design achieves a considerable trade-off between power and speed.

ACKNOWLEDGMENT

This work was sponsored by the Ph.D. Programs Foundation of Ministry of Education of China under 2009009211001; international cooperation projects in science and technology (2011DFA11310); National High Technology Research and Development Program "863" (2011AA10305); Natural Science Foundation of Jiangsu Province (BK2010411); and the industry support project of Jiangsu Province (BE2010008).

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