A 40 Gs/s Time Interleaved ADC Using SiGe BiCMOS Technology

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***Abstract*—The search for high speed, high bandwidth A/D converters is ongoing, and techniques to push the envelope are constantly being developed. In this paper an open loop, scalable, time-interleaved ADC architecture is presented, as well as a 60 GHz Colpitts oscillator. With the use of double-sampling, the timing skew requirements between channels is greatly relaxed, allowing sampling rates of up to 40 Gs/s at 4-bits of accuracy. This circuit is implemented using the IBM 8HP SiGe technology, with fT of 210 GHz. The performance of the 8HP ADC is validated by measurement. In addition, simulations with an experimental 8XP transistor model provided by IBM with a 350 GHz fT suggest that 30% more circuit speed is possible by just swapping the transistors.**

***Index Terms*—SiGe, ADC, BiCMOS, interleaved, flash, converter.**

I. Introduction

VERY high-speed, low-resolution A/D converters have applications primarily in wideband communications and instrumentation. These areas include software defined radio and measurement equipment such as high speed oscilloscopes. Software defined radio makes use of direct RF sampling, allowing the conversion of RF signals to baseband without using analog components such as LNA's and mixers. High speed oscilloscopes require internal circuitry that runs at very fast sampling rates so that high speed signals can be captured.

A combination of circuit techniques are used in this design, including serial sampling and high speed latching to achieve the target speed while minimizing power consumption. The concept of serial-sampling and interleaving to multiple channels allows for a great deal of flexibility in the back-end conversion methodology. The most common approach is to use the interleaving as a means to demultiplex data so that the acquired signals can be processed by low cost conventional Si CMOS, but one can also multiplex individual channels together to form a very high speed data stream output that otherwise could not be captured using a single channel converter due to settling time constraints.

In this paper, a 4-bit 40 Gs/s 4-way interleaved fully differential ADC design using the IBM 8HP SiGe technology is presented. This converter further extends the performance of ADC's on the Walden chart [8].

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Section II provides an overview of the converter architecture. Section III describes traditional time interleaving and the advantage provided by this approach. The ultra high speed sample-and-hold architecture is presented in Section IV. Detailed block diagrams of the sub-A/D converters and channel recombination techniques are described in Sections V, VI, and VII. Finally clocking techniques and measurement results are presented in Sections VIII and IX.

II. Architecture Overview

This ADC uses a front end 40 Gs/s sample-and-hold amplifier followed by four interleaved channels with secondary sample-and-hold (S/H) amplifiers clocked at 10 Gs/s. The front end sample-and-hold amplifier operates at full speed and is used to capture the incoming waveform. Secondary sample-and-hold amplifiers subsequently sample the output of the primary S/H amplifier in a circular fashion, where each channel runs at 1/n frequency of the front sample-and-hold amplifier. Fig. 1 shows a block diagram of our interleaved ADC system in a 4-way interleaved configuration.

The primary amplifier uses a standard 50/50 duty cycle clock, where as each secondary sample-and-hold amplifier uses a 25–75 clocking scheme as presented in [7], so that only one amplifier is sampling while the remaining three are in hold mode. This 50% increase in conversion time over the standard 50/50 clocking ratio has several benefits, including reducing the load on the primary sample-and-hold amplifier and also increasing the stabilization time for the conversion process. Simulated waveforms of the front-end sampler and secondary samplers are shown in Fig. 2. Each individual ADC channel uses a 4-bit flash converter for maximum speed.

To generate the equidistant phases for clocking, a looped differential two-stage shift register circuit is used. By using digital logic techniques, a 25–75 clocking scheme can be derived to drive the sub-ADC channels. This method for multiphase clock generation is highly flexible, as phases for more channels can be added by increasing the number of stages in the shift register.

III. Time Interleaving

Since Black and Hodges proposed the first interleaved ADC in 1980 [2], many methods to improve the technique have been presented [3]–[5]. It has been shown that time interleaving can be used to extend the utmost performance of A/D converters through increased sampling rates by staggering individual converters and post processing the individual outputs.

This performance benefit is not without drawbacks however. In addition to the increased power consumption and physical layout area that accompany a larger design, there are some

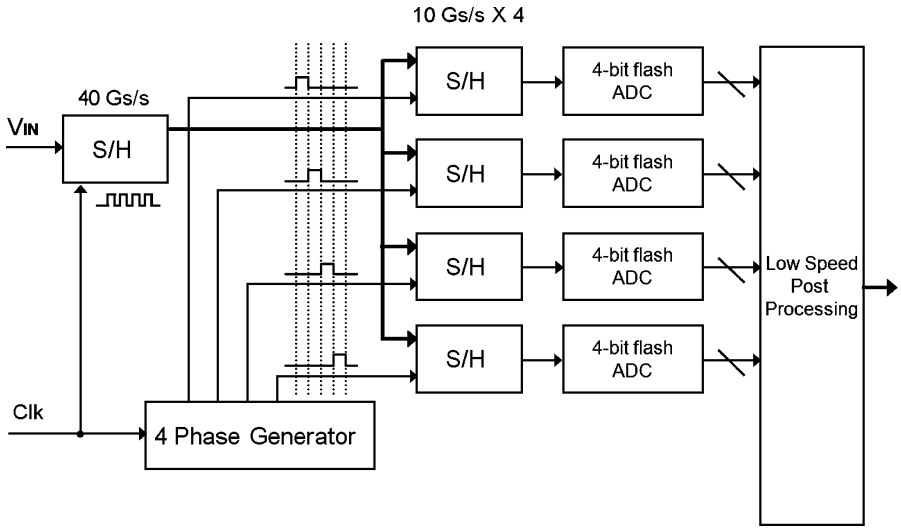

Fig. 1. Detailed ADC architecture.

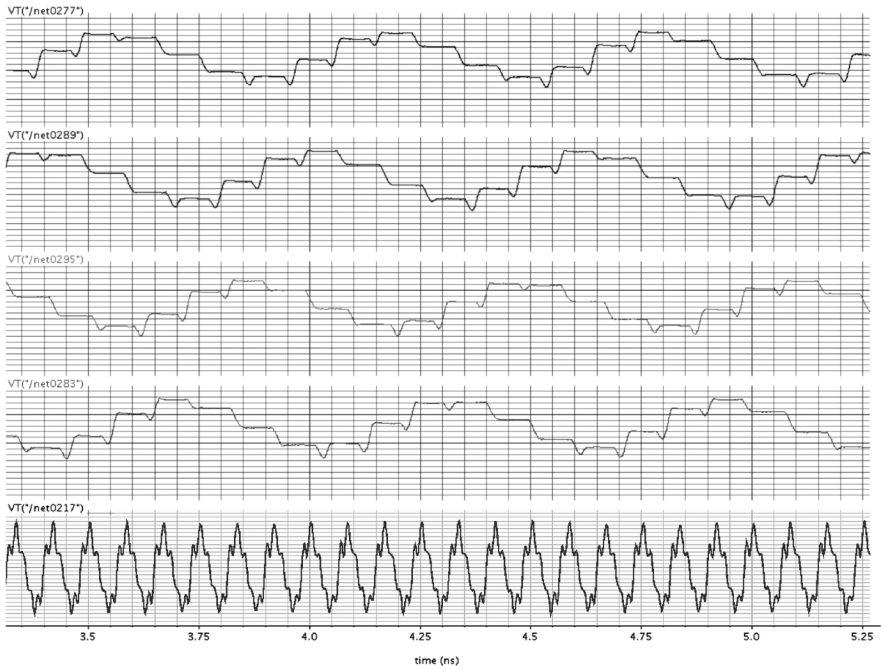

Fig. 2. Simulated output waveforms from full speed sample-and-hold amplifier (bottom) and the four interleaved secondary sample-and-hold amplifiers (8HP).

issues that are unique to time interleaving. These problems degrade the accuracy of the interleaved system, and include gain errors, offset errors, and phase skew. Errors such as non-linearity mismatches and bandwidth differences between the parallel channels are also present; however they are found in other ADC topologies and thus are not specific to interleaved converters.

Phase skew can be a serious problem with conventional time interleaved architectures, leading to degradation of the signal-to-noise-and-distortion ratio (SNDR). To alleviate this effect, a front end sampler operating at the full Nyquist rate is used in series with the individual sample-and-hold amplifiers of the interleaved channels. For traditional designs, problems as simple as input signal wire length differences from channel to channel can cause skew among the channels with respect to when each channel samples the data. With a full speed front end sampler, all values of the incoming signal are held for the secondary clocks, so slight differences in timing will result in small voltage errors equal to the droop rate of the front S/H amplifier. As long as the sub-ADCs sample the output of the full speed S/H amplifier during its hold stage, small amounts of skew between the individual sub-ADC channels does not affect the SNDR in a 4-bit system.

Traditional interleaving architectures use input buffers in front of each channel. Gain and offset errors often occur in these buffers due to differences amongst the amplifying transistors during the fabrication process. The sharing of the front-end sampler amongst the secondary channels as first demonstrated in [7] reduces the effect of these errors, as the analog signal to all four channels passes through the same amplifier.

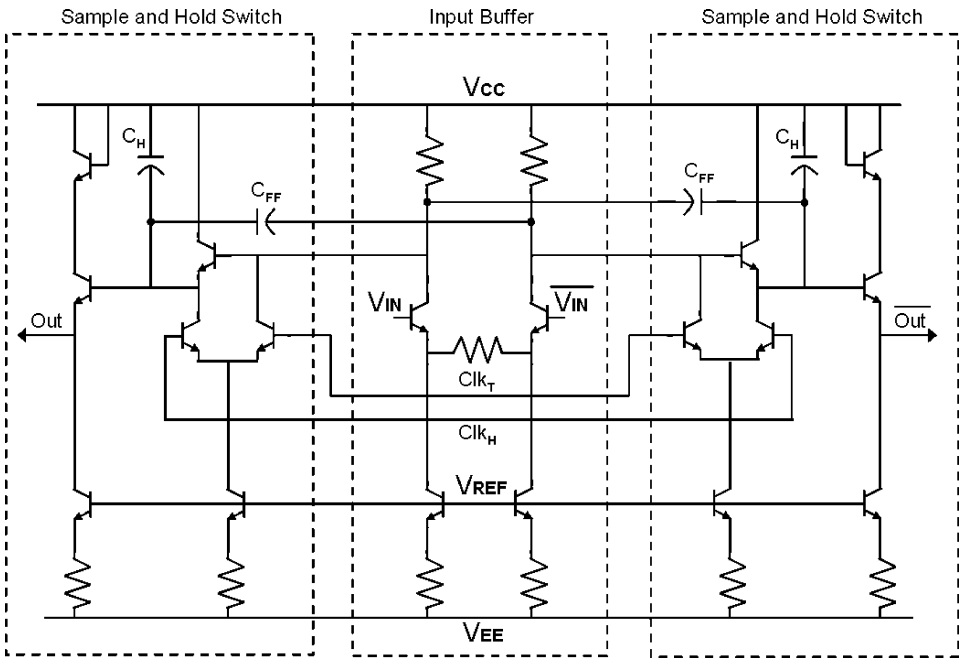

Fig. 3. Simplified schematic of SiGe sample-and-hold amplifier.

IV. Sample and Hold Architecture

The front end sample-and-hold amplifier was designed for 60 Gs/s but was only measured at 40 Gs/s due to testing equipment limitations. The fastest SiGe S/H amplifier previously reported was also 40 Gs/s in [6], at 3-bits of accuracy. For maximum speed, an open loop switched emitter follower (SEF) architecture has been used.

When used as the front end of an ADC system, the S/H amplifier determines the maximum performance of the system. Fig. 3 shows the schematic of the sample-and-hold amplifier. The same design was used for both the full speed and single channel sampler with the differences being values of the hold capacitors, for lower bandwidth but improved hold pedestal droop on the slower sampler. Hold capacitances of 105 fF were used on the 40 Gs/s samplers and 230 fF were used on the 10 Gs/s samplers. The value of the holding capacitor determines the voltage droop rate of the circuit's hold performance and its bandwidth.

To maintain the wideband nature of the design, a resistor is used to connect the emitters of the input transistor pair and provide degenerative feedback to maintain the linearity of the input buffer. The differential output is passed to the sample- and-hold switch, which consists of 3 transistors, a charge holding capacitor, and a current source controlled by a reference voltage. This architecture does not suffer the same *RC* delay limitations as the integrating S/H design presented in [3], since it is a voltage based approach and hence not necessary for the capacitor to fully discharge before each new sample. It acts like a switch, tracking the analog voltage while it is in sample mode and latching onto the voltage when the clock changes to hold.

As presented in [1], cross-coupled feed forward capacitances (C_{FF}) have been added from the input buffer to the emitter follower output of the transistor switch. These cross coupled capacitances allows cancellation of the base-emitter capacitances, which greatly reduces the analog feed-through of the input signal to the output during the hold mode. An emitter follower stage has been added to each of the differential outputs, for improved driving capability.

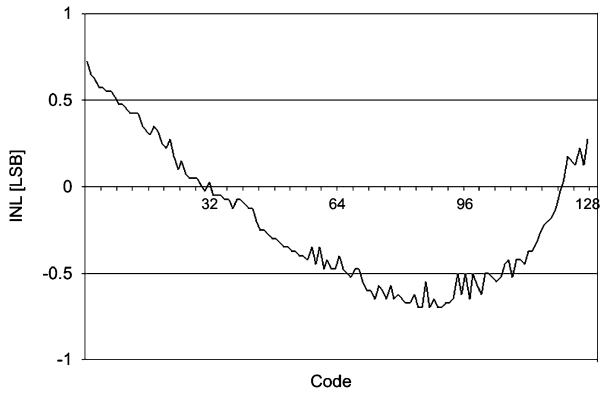

Fig. 4. INL plot at 7 bits of accuracy (8HP).

The static performance of the amplifier shows an Integral Non-linearity (INL) of less than 1 LSB at 7 bits of accuracy, presented in Fig. 4. With the desire to minimize power and maintain compatibility with SiGe digital design, the voltage supply headroom has been fixed at 3.4 V. This value determines the maximum input voltage swing that is acceptable for a given accuracy of the sample-and-hold amplifier.

With a differential design, the second harmonic can be ignored. To calculate the effects of the third harmonic (HD_3), we use the equation from [1] where f_{in} is the input frequency, I_c is the bias current, V_p is the peak amplitude, V_T is the thermal voltage, and C_s is the sampling capacitance.

$$HD_3 = 20\log\left[\frac{1}{12}V_p^2 V_T\left(\frac{2\pi f_{in} C_s}{I_c}\right)^3\right] \quad (1)$$

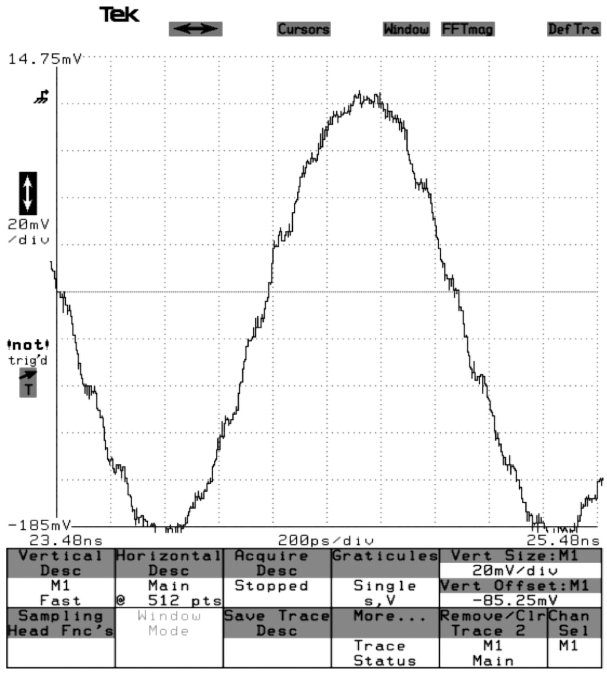

Fig. 5. Measured S/H output waveform at 10 Gs/s.

Substituting values of $\mathrm{Ic} = 12\,\mathrm{mA}$, $\mathrm{Vp} = 500\,\mathrm{mV}$, $\mathrm{Vt} = .65$, $\mathrm{F_{in}} = 20\,\mathrm{GHz}$, and $\mathrm{C_s} = 105\,\mathrm{fF}$, the 3rd harmonic is calculated to be -34.9 dB.

Due to the speed of this amplifier and the synchronization issues associated with capturing sample-and-hold circuit waveforms with sampling oscilloscopes, capturing a full speed waveform of the design has not been accomplished. Fig. 5 shows the 10 Gs/s sampler measuring a 1 GHz waveform, which is the fastest that was achievable using the available testing equipment.

The IBM 8XP library has HBTs with fT of up to 350 GHz. The 8XP kit is an early preview of the HBT transistors found in the upcoming IBM 9HP BiCMOS kit. Early models have been provided to us and simulations have been run to show the potential performance increase of this sample-and-hold design. The 8XP simulations presented in this paper were run by using the new transistor model on the existing design, and show roughly a 30% performance in frequency response. The biasing resistors have not been re-tuned for optimal biasing current, which should yield further speed improvements. Fig. 6 shows the cutoff frequency (fT) compared to the current densities of the 7HP, 8HP, and 8XP kits. Typically for fastest speed the HBT's are biased at their peak current. The figure shows tradeoffs that can be made with a faster kit. By using the 8XP transistors as drop-in replacements in an 8HP design, the performance moves from the starting point to the point indicated by #1. If the current was biased optimally for 8XP, the speed improvements would move towards the point indicated by #2 and to maintain the same performance levels as 8HP using 8XP transistors, we could save a significant amount of power and move toward point #3 on the graph.

Figs. 7 and 8 present the same sample-and-hold architecture simulated using the 8HP and 8XP HBT models, to show the performance increase that the new kit may yield. Fig. 7 is the bandwidth plot of the sample-and-hold amplifier simulated under the different conditions. The baseline simulations use the standard

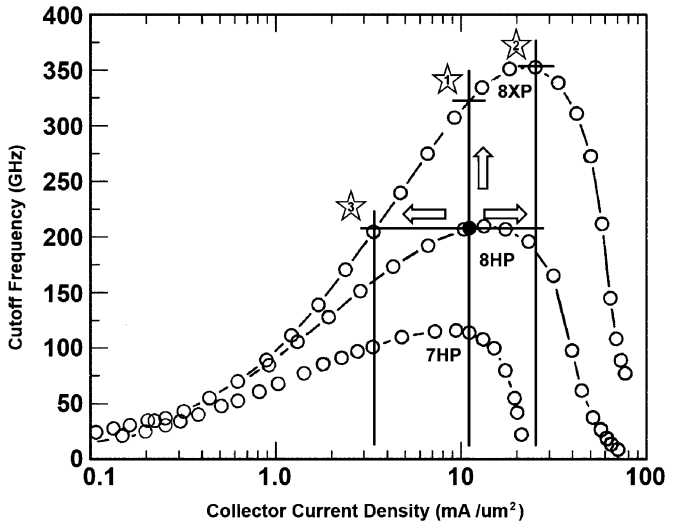

Fig. 6. fT vs current density curves of 7HP, 8HP, and 8XP and their power/speed tradeoffs.

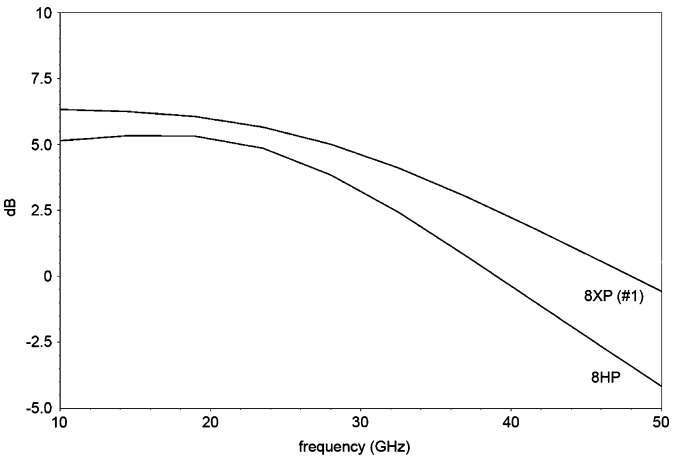

Fig. 7. Simulated bandwidth plots of the sample-and-hold amplifier using 8HP and 8XP kits.

8HP technology. The line marked 8XP (#1) is the 8XP HBT transistors used as a drop-in replacement for the 8HP design. It would match point #1 in Fig. 6.

Fig. 8 shows the transient simulations of a differential simulation between 8HP and 8XP at sampling rates of 40 Gs/s and 60 Gs/s. The benefits of a much flatter pedestal due to the increased switching speed of the 8XP models are clearly visible in each case.

A plot showing the simulated spurious free dynamic range (SFDR) of the sample-and-hold amplifier at 60 Gs/s and 80 Gs/s using the 8HP and 9HP kits is shown in Fig. 9. Again the effect of the faster switching of the 8XP transistors can be seen in the results.

V. Flash Architecture

The interleaved technique presented can be used with a number of sub-A/D topologies, depending on the desired speed versus accuracy tradeoff. The work presented has strived for maximum possible speed, so a fully differential flash converter with a front-end sub-S/H amplifier has been used.

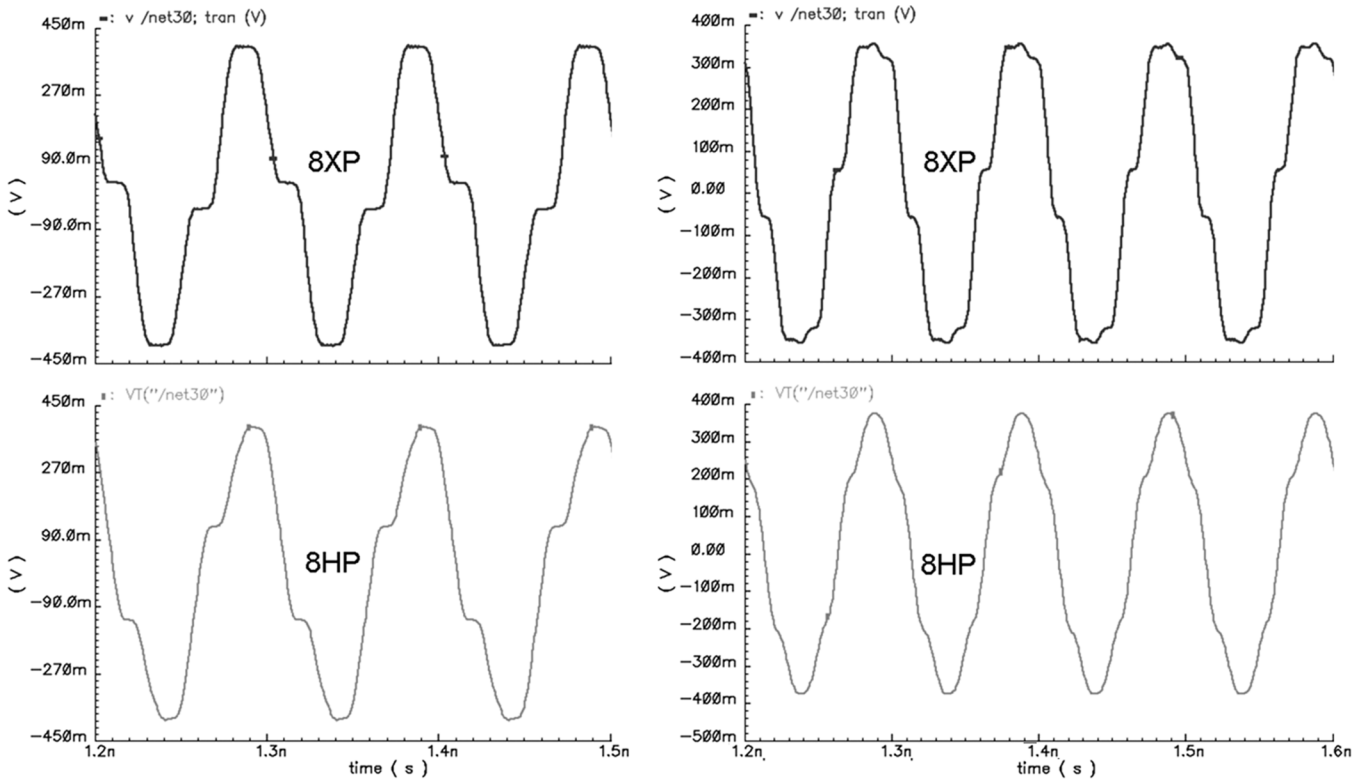

Fig. 8. Transient simulations at 40 Gs/s (a) and 60 Gs/s (b) of a 10 GHz input sine wave.

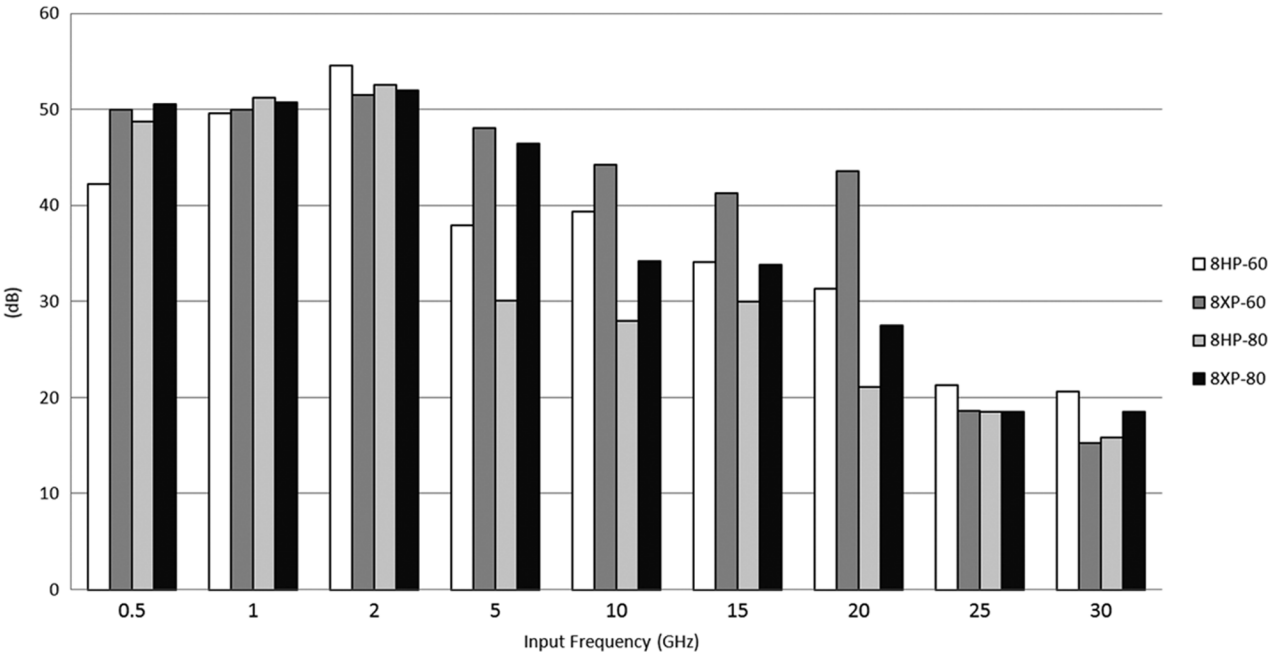

Fig. 9. IBM 8XP simulated SFDR comparison.

To minimize the effect of input capacitance from large numbers of pre-amplifiers on the sample-and-hold amplifier, the technique of interpolating preamplifier outputs has been applied to generate intermediate crossover points to double the effective resolution from 3 bits to 4 bits without the use of additional pre-amplifiers.

With the flash architecture, the comparator performance determines the maximum speed of the sub-ADC. The 25–75 clocking scheme helps by increasing the stabilization time at 10 GHz (40 GHz/4) to 75 ps from 50 ps. The graph shown in Fig. 10 indicates the performance of the comparator.

Using a maximum input voltage swing of 500 mV, (2) finds the maximum voltage difference where a determination can be made given an amount of stabilization time.

$$\frac{V_{\text{in}}}{2^n} = \Delta V_{\text{difference}} \tag{2}$$

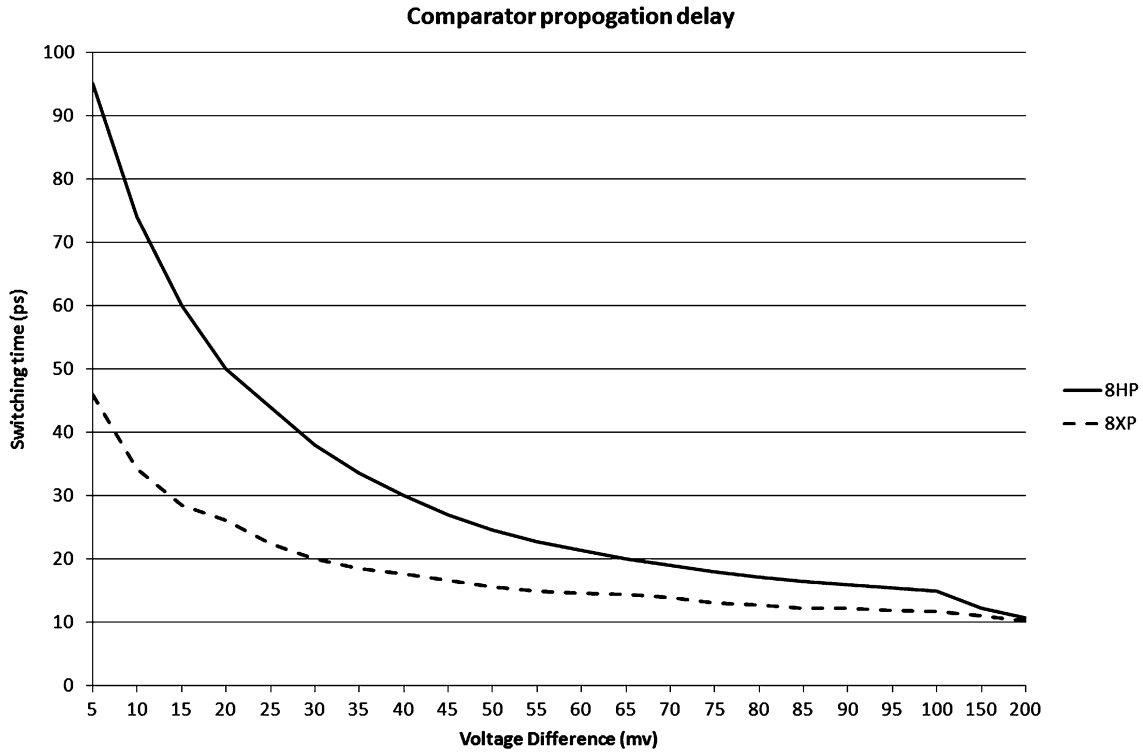

Fig. 10. Comparator performance comparison.

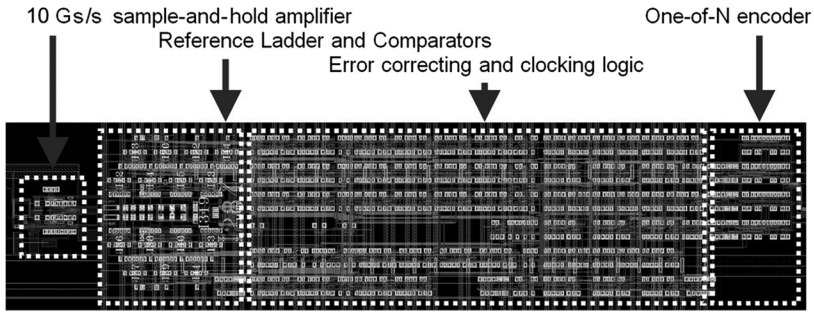

Fig. 11. Close-up view of the single channel ADC layout.

This result can then be compared to the comparator performance to see the maximum speed versus accuracy that the A/D can obtain. With a 75 ps window, the minimum voltage step that will yield a determinate value by the comparator in 8HP is 12 mV. When entered in the equation it equals 5.3 bits. At 4 bits, the minimum voltage difference is 31.25 mV for which a valid result can be achieved with only 30 ps of settling time; which is well within the margin of error.

As expected, the 8XP model simulations show faster switching times for small input voltage differences than 8HP. Switching times as low as 30 ps for 12 mV input voltage difference are presented. For an identical input voltage swing, 8XP devices should be able to resolve 6 bits at the same frequency.

With the goal of maximum speed, a simple bubble suppressor with a one-of-n encoder was used for the final binary encoding of the comparator output. Fig. 11 presents a layout view of all the major components in each of the ADC channels.

VI. DAC

A 4-bit R-2R DAC has been implemented using 8HP technology. It has been included in the test chip to demonstrate the functionality of the front end ADC. The schematic of the DAC, shown in Fig. 12, consists of identical transistors with equal emitter resistors and a R-2R collector network to create the binary division of the collector currents. This approach is advantageous to a current steering DAC with the R-2R configuration in the emitter network, since scaling of the transistor pairs and the associated problems (large capacitances, area) is not needed to maintain proper biasing at the peak fT of the devices.

VII. Post Processing

The time interleaved sample-and-hold system allows for several different possibilities in the back end, including recombining the channels into a high speed stream, allowing the data from the slower speed channels to be processed by a CMOS

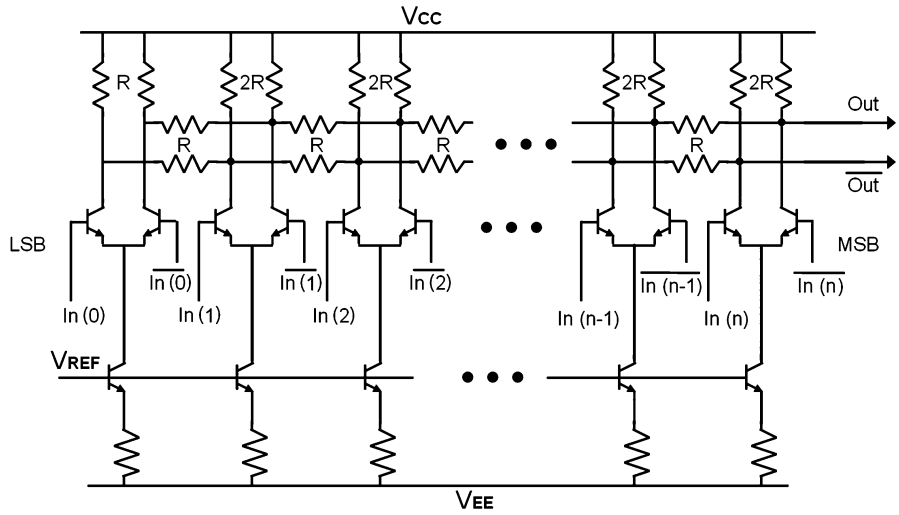

Fig. 12. Simplified schematic of R-2R DAC.

back end, and increasing the amount of interleaving in exchange for increased accuracy.

Channel Recombination: Recombining the individual interleaved channels to form a single high speed data stream requires high speed multiplexers to adequately switch the outputs of the channels. With the digital output, timing differences caused by slight phase offsets of the clock do not pose a significant problem, as they do in the analog realm. However, the switching noise caused by digital latches and multiplexers at speeds past 40 GHz can contribute to bit errors and degradation in the output of the converter system.

At speeds upwards of 40 GHz, the switching noise introduced by the traditional master-slave flip-flop (MSFF) architecture becomes significant enough to exceed the error thresholds of the 250 mV swing of CML digital logic. The cause of this switching noise is twofold—it has been shown that latching transistors that are smaller than the primary transistors allow for faster operation of the latch. However, HBT transistors of different emitter sizes have different current levels for their peak fT operation, thus by using differently sized transistors; neither can be biased at their optimal fT current when sharing a single current source at the bottom of a CML tree. For a brief operating range above that of the traditional MSFF design, the switching noise level remains low, however the noise scales with the frequency of the signal and soon becomes intolerable as the frequency is increased.

A modified master-slave flip-flop first presented in [16] has been used in the design of the interleaved ADC. It exchanges the current tree paths at the clocking transistor level so that both the latching transistor pairs will use a current tree, and the primary transistor pairs will use their own current tree. With this method, both trees can be biased at their optimal currents, allowing for faster operation with less power consumption in addition to greatly reduced switching noise.

Channel Dispersion: The interleaved architecture is well suited for the dispersion of the converted signals of lower speed technology families. As the output is already at 1/n speed of the sampling rate, further demultiplexing of the interleaved channels can be easily accomplished with minimal circuitry to speeds within the capabilities of Si CMOS technology. This will drastically lower the overall cost to convert high frequency signals using low cost technology, with a relatively small amount of SiGe as the intermediary between the two.

Applications for direct conversion using FIR filters have been reported in [17].

Accuracy From Additional Channels: The maximum accuracy of the system is dictated primarily by the accuracy of the full speed sample-and-hold amplifier and to some degree the secondary sample-and-hold amplifiers as well. However, the overall frequency of the individual converters also plays a role in the maximum accuracy of the overall system. As shown in Fig. 10, even with the flash converter, there is a tradeoff between the available settling time and the minimum voltage difference (LSB) that a comparator can differentiate.

Each increase in interleaving halves the operating speed of the individual channel, and thus relaxes this settling time versus LSB tradeoff. The complexity of the system and layout area requirement doubles with each increase in interleaving as well, but the power requirements do not since the CML collector bias current of all the non-critical digital logic trees can be turned down as the operating speed decreases.

VIII. Clocking and Jitter

At high frequencies the influence of clock jitter on the accuracy of the ADC becomes increasingly severe, making the ADC performance dependant on the purity of the clock source more than any other factor.

With the intention of operating the ADC system at 60 GHz, a 60 GHz LC-tank oscillator was designed as a clock source for the interleaved system. The low Q of on-chip inductors results in a design with much higher phase noise than commercially available off-chip clock generators, so an external clock signal is preferred for phase noise performance at high frequencies. However external signal generators operating up to 60 GHz are difficult to obtain, so both an on chip 60 GHz voltage-controlled-oscillator (VCO) and an external high frequency port for an external signal generator were designed into the test chip.

TABLE I
RELATION OF FREQUENCY, JITTER, AND ENOB

Sampling Frequency (at Nyquist rate)	Jitter (ps)	Maximum ENOB	Jitter (ps)	Maximum ENOB	Jitter (ps)	Maximum ENOB
1 Gs/s	1.24	8	5.05	6	21.2	4
2 Gs/s	0.624	8	2.53	6	10.6	4
4 Gs/s	0.312	8	1.26	6	5.31	4
8 Gs/s	0.156	8	0.631	6	2.65	4
10 Gs/s	0.124	8	0.505	6	2.12	4
20 Gs/s	0.0624	8	0.253	6	1.06	4
40 Gs/s	0.0312	8	0.126	6	0.531	4
60 Gs/s	0.0208	8	0.084	6	0.354	4
80 Gs/s	0.0156	8	0.063	6	0.265	4

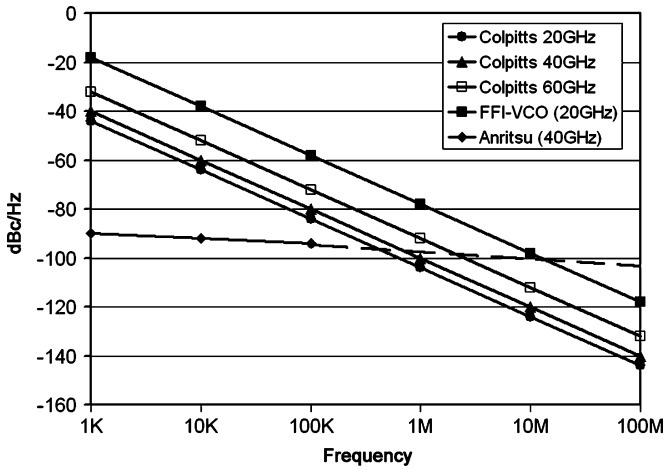

Fig. 13. Phase noise of various clock sources.

Fig. 13 shows a plot of parasitic simulations of on-chip Colpitts oscillators at various frequencies compared to the published phase noise numbers of a commercially available Anritsu 68369 A/NV 40 GHz signal generator.

Phase noise is related to clock jitter as dictated by the linear piece wise function below. f_c is $1/2$ the sampling frequency, a_i and b_i are points on the phase noise plot, with f_i and f_{i+1} their respective frequencies [11].

$$\sigma_{\mathrm{RMS}} = \left(\frac{1}{2\pi f_C}\right) \sqrt{2\sum_{i=1}^{K-1} 10^{\frac{b_i}{10}} f_i^{-\left(\frac{a_i}{10}\right)} \left(\frac{a_i}{10}+1\right)^{-1} \left[f_{i+1}^{\left(\frac{a_i}{10}+1\right)} - f_i^{\left(\frac{a_i}{10}+1\right)}\right]} \tag{3}$$

Taking into account the LSB step size, frequency, and full scale voltage, an approximation of the relationship between jitter, accuracy, and frequency can be gathered by

$$t_q = \sin^{-1}\left[\frac{\left(\frac{1}{2^n-1}\right)}{2\pi f_O}\right] \approx \frac{\left(\frac{1}{2^n-1}\right)}{2\pi f_O}. \tag{4}$$

Combining these two equations, Table I presents the maximum ENOB at varying sampling frequencies. From this chart, it is obvious that the jitter requirements at upwards of 40 GHz are best measured in femtoseconds—something that is out of the reach of current on-chip oscillators given the Q values of available components.

Using the equations above, the Anritsu signal generator has the lowest amount of RMS jitter, at 0.23 ps. The Colpitts oscillator at 60 GHz has jitter numbers of around 1.1 ps. From Table I, it is clear that in the ideal case, the Anritsu is capable of clocking the ADC system at 40 GHz with sufficient margin, while use of the on-chip Colpitts oscillator will result in reduced ENOB due to jitter.

One other option for an ultra-pure clock source are commercially available dielectric resonating oscillators (DRO's). They are currently the most readily available devices to achieve the phase noise needed for achieving ENOB's of 4 bits and up at sampling frequencies upwards of 60 GHz. When coupled with Oven controlled crystal oscillators (OCXO's), they can achieve phase noise levels below -110 dBc/Hz at 1 KHz offsets. Unfortunately, at this time they are only available in frequencies of around 30 GHz.

It is clear that the clocking jitter requirements at 60 Gs/s are severe, and it is not something that has a complete solution at this time while maintaining a fully monolithic design.

IX. MEASUREMENT RESULTS

A test chip containing a 4-way interleaved ADC and supporting circuitry was fabricated using the IBM SiGe 8HP technology and occupied 7.5 mm^2 of area, using 2.1 A of current, including 400 mA per sub-ADC channel. The supporting circuitry includes a 60 GHz Colpitts oscillator, input for an external clock source, and output DACs. Its micrograph is shown in Fig. 14.

The 60 GHz VCO had a measured frequency of 60.8 GHz, which was within 10% of the simulated frequency. The digital oscilloscope used to capture the waveform is a Tektronix 11801C, which is a sampling scope that has a 50 GHz bandwidth but requires a 2 GHz trigger signal. We have found that a slower trigger signal results in a cleaner waveform, so a divided-by-96 output was used on the test chip. Its waveform is shown below in Fig. 15.

Measuring the performance of an entire interleaved ADC system can typically be achieved by capturing the digital output of all 4 channels simultaneously and analyzing the data using

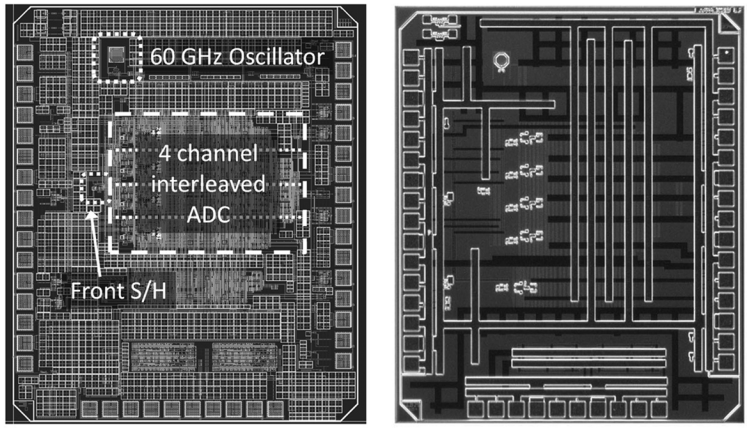

Fig. 14. Layout (a) and Die Micrograph (b), containing 6600 transistors (both 8HP).

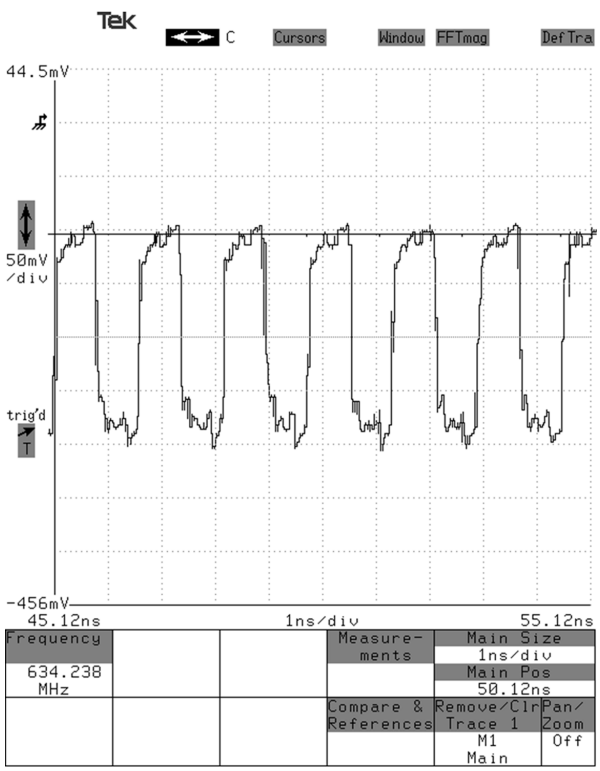

Fig. 15. Measured divide-by-96 output waveform of 60 GHz VCO.

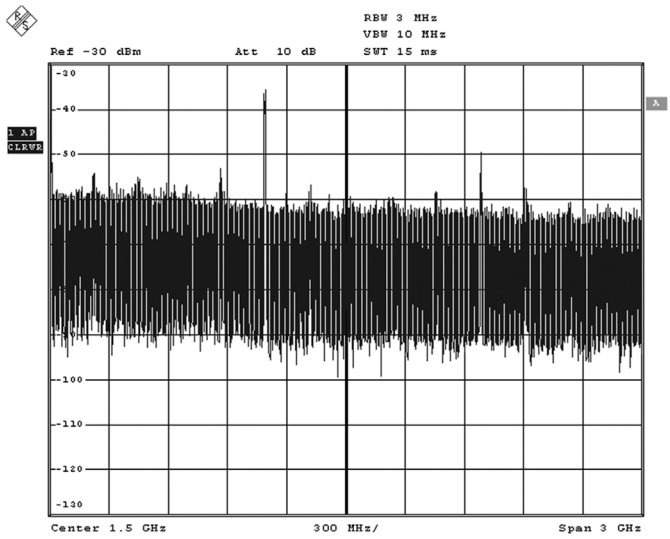

Fig. 16. Measured output spectrum of a single channel.

software such as MATLAB. However at 15 Gs/s per channel, the ability to capture and save such quantities of parallel data simultaneously is not possible with the current generation of commercially available logic analyzers—the speed is simply too fast. A technique that multiplexed the data to a 60 GHz stream for use with a 60 GHz DAC at the 4:1 multiplexed output of the ADC system was used instead. To verify the individual channel performance, the system was also configured to have a DAC output for each channel. The use of a DAC in ADC performance measurement presents a performance penalty on the accuracy of the final ADC output; however it is a viable method for showing the functionality of the design with respect to the front end sample and hold performance given the speed of the circuit and test equipment available to us. A sine wave input generated by a Rhode & Schwartz SML-01 (1.090.3000.11) signal generator was used as the input for the ADC, and the onboard DAC output was measured by the Rohde & Schwartz FSP-40 (1164.4391.38) spectrum analyzer capable of 40 GHz input.

The output of the 60 GHz on chip oscillator was determined to be too noisy due to the low Q of on chip inductors to be used as a clock for the ADC, so the Anritsu 68369A/NV signal generator was used to generate a 40 GHz input clock into the test chip instead. Output from each individual channel was measured using the spectrum analyzer, and was found to have similar performance characteristics. The DAC output is shown in Fig. 16 of the ADC response to a 1.1 GHz input sine wave, showing an ENOB of about 3.5 bits for a single channel. The output of the 60 GHz interleaved DAC, while functional in simulation, did not perform on silicon so measurement of the entire interleaved system performance was not accomplished using this test chip. However, the outputs of the single channels show that front end sample and hold configuration is functional. The measured performance summary of the system has been provided in Table II.

TABLE II
ADC PERFORMANCE SPECS

ADC Performance Summary	
Sampling Rate	40Gs/s
Resolution	4 bits
ENOB	3.5 bits
SFDR	22dB
ADC Core Area	1.4mm^2
Technology	IBM 8HP
FOM (Power/2^{ENOB+1}*BW)	10pJ/sample

X. CONCLUSION

A 40 Gs/s 4-bit time interleaved analog to digital converter has been designed and fabricated using IBM SiGe 8HP technology. A 60 GHz Colpitts oscillator has also been developed and shown to operate at 60.8 GHz. Output of the individual ADC channels have been presented using a 40 GHz clock, as well as an analysis of jitter requirements for high speed converters. Measured results show an ENOB of 3.5 at 10 GHz/channel. Simulated results show an ENOB of 3.2 for the entire system at 15 GHz/channel, however this could not be verified in measurement due to the lack of a clean 60 GHz clock source and ability to capture digital data simultaneously at such high speeds. This interleaved system shows that 0.13 um SiGe is a viable option in terms of power, size, and speed when compared to other technologies for high speed mixed signal circuit design.

Simulations of the circuits using the IBM 8XP HBT models as drop in replacements have been included and show a substantial improvement in the performance and speed of the sample-and-hold amplifier and comparator circuits, allowing for up to 30% increase in speed without reconfiguration of circuits for optional current biasing.

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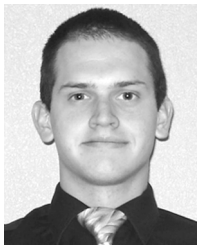

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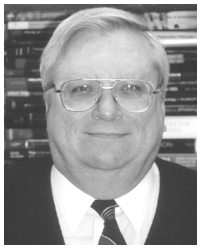

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