A novel switching scheme for offset storage cancellation technique, for GS/s range ADCs

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Abstract— **A novel switching scheme for the common capacitor offset cancellation technique is presented. The new switching scheme uses the capacitors not only for offset cancellation but also for sampling of the input signal. The number of capacitors is minimized by incorporating a two stage amplifier per offset cancellation stage, a technique used for the first time, in our knowledge, in this specific offset cancellation architecture.**

Keywords- A/D converter; Highs peed; High dynamic range; Output offset cancellation; Millimeter-wave

I. INTRODUCTION

As digital processing spreads increasingly in all the fields of technology, so does the need for fast and accurate circuits to convert the analog signal into the digital domain. The development of deep-submicron CMOS processes increased the interest toward millimeter-wave broadband wireless systems. The embedded ADC in those systems should achieve a sampling rate to the order of GS/s and 4-6 bits of resolution, which is a challenge considering the increased mismatch of transistors in these technologies and the lower headroom, which minimizes the input range, leading to even smaller least significant bit (LSB) values.

There are a number of ways to minimize offset of comparators in ADCs [1], with the most popular being resistive averaging [2, 3, 4, 5] and digital trimming [6, 7], especially in high speed design. Both of these techniques increase design complexity and add extensive interconnect network. A more straightforward way to minimize offset is to sample it by capacitors and then subtract it from the input signal. Two techniques are in use to accomplish this operation. Input offset storage (IOS) and Output offset storage (OOS) [1].

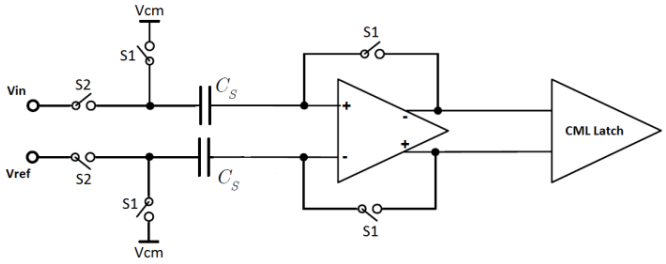

Figure 1. Input offset storage (IOS)

IOS technique [8, 9] closes a unity gain loop around the amplifier and samples the input offset voltage in phase S_1 and in phase S_2 the offset is subtracted from the input (Fig. 1). Using IOS a residual offset remains equal to $\frac{Voos}{1+A}$ where Voos is the output offset voltage of the amplifier and A its gain.

OOS technique uses capacitors to sample the output offset of the amplifier [10, 11, 12]. While at phase S_1 the inputs of the amplifier are shorted and the offset is stored in the capacitors. At phase S_2 the input signal is amplified and the offset is subtracted from the output (Fig. 2). The OOS technique leaves no residual amplifier offset, but care must be taken in the gain of the amplifier. If the output offset, $A \times Vos$ is big enough to saturate the output then the offset voltage would not be correctly stored.

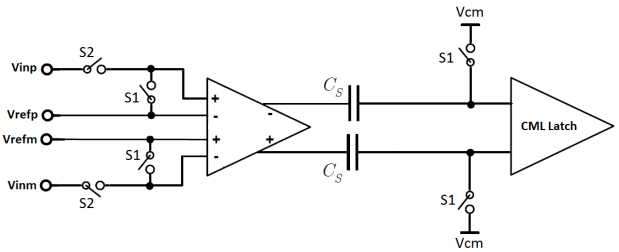

Figure 2. Output offset storage (OOS)

In both of these techniques the offset of the latch comparator is not canceled.

This work presents a novel switching scheme for the OOS cancellation technique described above. It offers substantial increase in SINAD and SFDR when used in High speed A/D converters over the usual clocking method, moreover, this is achieved with no additional current consumption.

In the next section the novel clocking scheme will be discussed in comparison with the common way of clocking. Also the comparator architecture of the A/D converter used to make the comparative study will be presented. In Section III the simulation results will be presented and finally a conclusion will be formulated.

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II. ADC ARCHITECTURE

A. Proposed Clocking Scheme

The proposed clocking scheme is illustrated in Fig. 3.

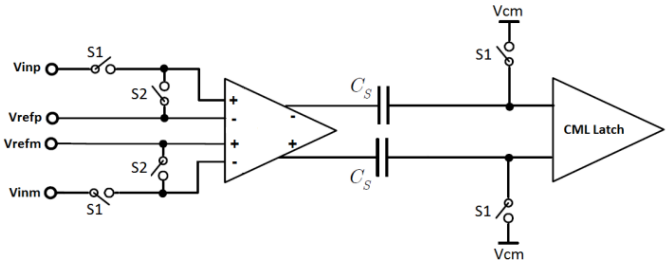

Figure 3. Comparator with novel switching scheme

This technique is based on OOS, but uses different switching order. At phase S1 the amplified input voltage is sampled by the capacitors. At phase S_2 the inputs short to the reference voltage and the amplifier, amplifies its offset voltage, shifting the output and cancelling the offset voltage. The main attribute over the common OOS technique is the sampling of the amplified input voltage. This sample-and-hold (S/H) operation is the main contribution of this work. It offers a substantial improvement in dynamic behavior, and alleviates the need for an additional S/H circuit, saving in area, current consumption, and design time.

To further explain the difference between the two methods the output voltage for both techniques is illustrated in the first graph of Fig. 4. In both cases, while the clock is low the sampling capacitors are connected to a common voltage and thus the differential output is zero. In this phase the capacitors for the proposed clocking scheme, sample the output voltage instead of the offset. While the clock is high the already sampled voltage is shifted by the amount of offset and settles. In the conventional OOS technique the output is not held to a specific value, and follows the variations of the input voltage. The sampling operation is clearly seen at points A and B, where the output stays fixed for the proposed clocking scheme (dotted line), but changes for the conventional OOS technique (solid line).

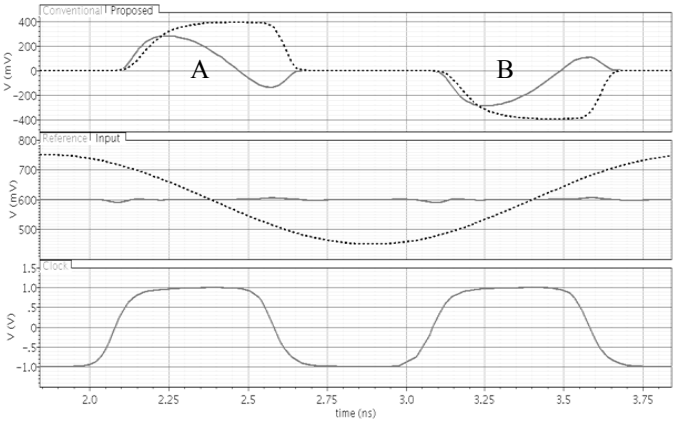

Figure 4. Transient response of the common and proposed clocking scheme

B. Proposed ADC Comparator

Fig. 5 illustrates the architecture of the A/D converter design to test the proposed switching scheme. It is classic 6-bit flash ADC, composed of 63 comparators with linearly incremental voltage threshold each. The comparison results are fed into a thermometer-to-binary converter with a 6-bit output.

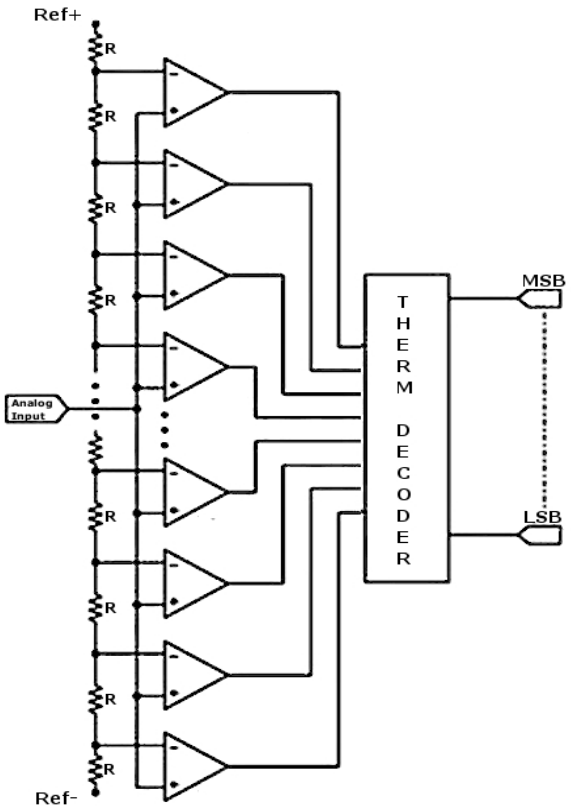

Figure 5. Flash A/D converter Architecture

The comparator used in this ADC consists of a chain of low gain preamplifiers, followed by a latched comparator. The preamplifiers are used to increase gain in order to minimize the latched comparator's offset effect to the total input referred offset of the chain. The total comparator offset equals to:

$$V_{\text{off}} = \text{V}_{\text{off}_1} + \frac{\text{V}_{\text{off}_2}}{\text{A}_1} + \frac{\text{V}_{\text{off}_3}}{\text{A}_1 \times \text{A}_2} + \frac{\text{V}_{\text{off}_N}}{\text{A}_1 \times \text{A}_2 \times \cdots \times A_N} + \frac{V_{ioff\ latch}}{A_1 \times A_2 \times \cdots \times A_N} \quad (1)$$

Where:

V_{off_N}	the Nth preamplifiers input referred offset
$V_{ioff\ latch}$	the latched comparator input referred offset
A_N	the gain of the Nth preamplifier

To minimize the offset of the amplifiers in the chain the proposed switching scheme described before is used here as well, in a multi-stage version, as illustrated in Fig 6 [13].

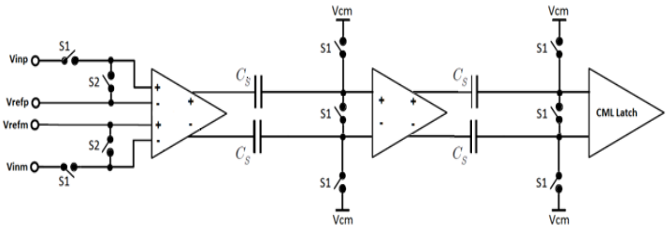

Figure 6. Proposed comparator chain

While at phase S1 the amplified input signal is sampled by the first set of capacitors. At the same time the other set of capacitors samples the output offset of the second amplifier stage. At phase S2 the sampled voltage is shifted by the amount of offset of the first amplifier, effectively eliminating it, while the second stages further amplifies the output voltage. At phase S2 instead of shorting the Vin and Vref terminals to a common voltage for all the comparator chains in a Flash ADC, each chain shorts to its specific reference voltage, this accomplishes a faster settling for the Vref when the switches change state, thus improving the high sampling speed dynamic behavior of the ADC.

III. SIMULATION RESULTS

The proposed clocking scheme is employed in a 6-bit 1.7GS/s Flash ADC, designed for a 1.2-V 60 GHz Transceiver, implemented in a 90nm CMOS process [13]. The differential input range equals to 600mVp-p, and each comparator chain consumes 1.75mA.

The performance of the ADC and the proposed clocking technique was verified using FFT analysis, running a specific Monte Carlo transient simulation to include the effect of mismatch and process variation. Fig. 7 illustrates the output spectrum at 1.7GS/s and 400MHz input signal frequency, using the novel clocking technique, while Fig. 8 shows the exact same output spectrum when using the common clocking technique.

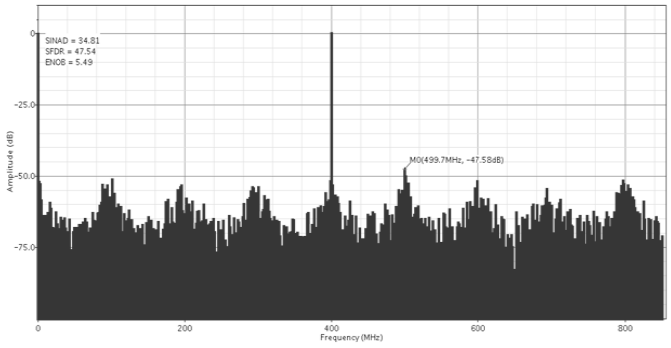

Figure 7. Output Spectrum utilizing novel switching scheme

A substantial improvement on the dynamic characteristics of the ADC is achieved using the proposed technique. Comparative results are presented in Table I. In Table II transient simulation results, disregarding mismatch effects are presented. Examining this results, the effects of mismatch in the performance of the A/D converter can be appreciated.

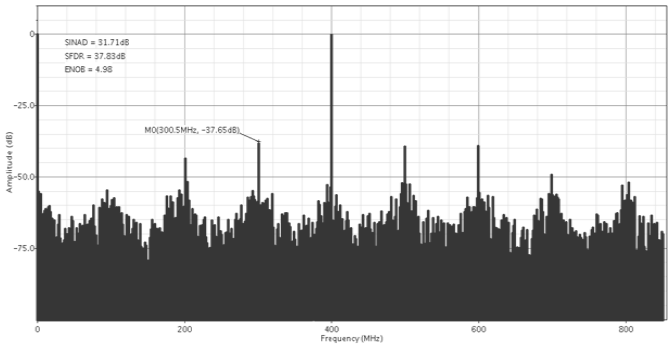

Figure 8. Output spectrum utilizing common clocking scheme

TABLE I. MONTE CARLO SIMULATION RESUTLS

Monte Carlo Simulation results	Proposed Technique	Conventional Technique
SINAD [dB]	34.81	31.71
SFDR [dB]	47.54	37.83
ENOB [bits]	5.49	4.98

TABLE II. TRANSIENT SIMULATION RESULTS

Simulation results	Proposed Technique	Conventional Technique
SINAD [dB]	37.29	33.41
SFDR [dB]	47.76	39.22
ENOB [bits]	5.90	5.26

Fig. 9 illustrates the Signal-to-noise and distortion ratio (SINAD) for various input signal frequencies, while fig. 10 and fig. 11 illustrate the Effective number of bits (ENOB) and Spurious free dynamic range (SFDR) respectively. The proposed clocking scheme offers an improvement up to 4dB in SINAD and up to 12dB in SFDR. The novel A/D converter presents an 0.7 bit increase in ENOB.

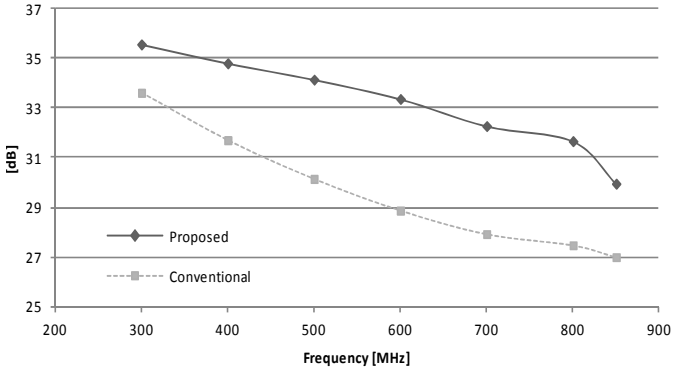

Figure 9. Signal-to-noise and distortion ration (SINAD)

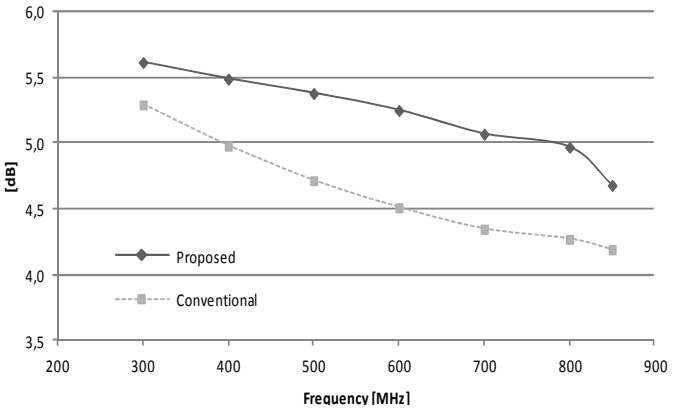

Figure 10. Effective Number of Bits (ENOB)

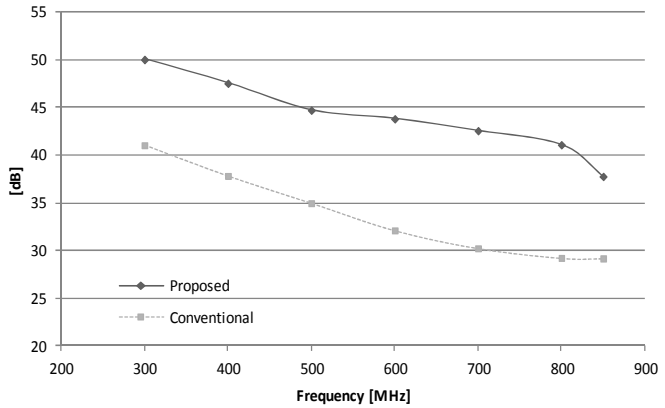

Figure 11. Spurious Free Dynamic Range (SFDR)

The superiority of the proposed technique can also be appreciated by figures 12, 13 and 14 for SINAD, SFDR and ENOB respectively. In these figures the performance at various sampling rates is presented, ranging from 400MHz to 2000MHz. It is apparent that the proposed clocking technique can highly enhance the performance of an A/D converter especially in high speed sampling rates. Specifically, a 5bit ENOB can be maintained over the 2GS/s mark instead of the approximately 1350MS/s achieved using the conventional technique.

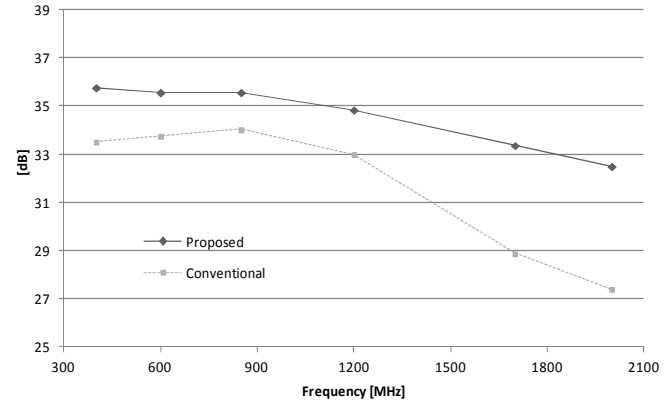

Figure 12. SINAD vs Sampling Frequency

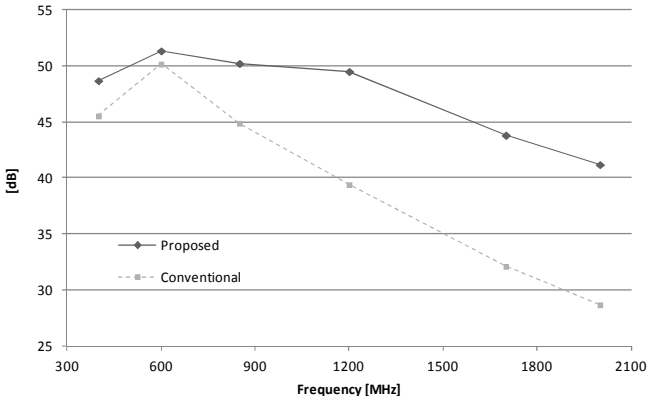

Figure 13. SFDR vs Sampling Frequency

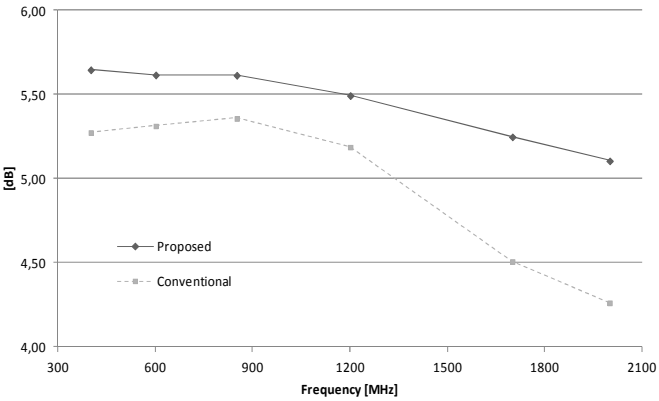

Figure 14. ENOB vs Sampling Frequency

IV. CONCLUSIONS

In this work, a novel switching scheme for the common offset cancelation technique is presented. The proposed technique offers significant advantages for high-speed A/D converters. Comparative simulations between the proposed and the conventional clocking scheme, using the exact same ADC design, confirm the superiority of this work.

ACKNOWLEDGMENT

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