A 0.13-μm 1-GS/s CMOS Discrete-Time FFT Processor for Ultra-Wideband OFDM Wireless Receivers

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***Abstract*—A discrete-time (DT) fast Fourier transform (FFT) processor is presented as an architectural approach to Fourier transform processing multigigahertz of spectral bandwidth. The processor is considered with the specific application of demodulating orthogonal frequency-division multiplexing (OFDM) modulation. The processor enables increased receiver linearity beyond that which is typically limited by the signal-to-noise-and-distortion ratio of high sample rate ADCs by performing OFDM demodulation in the DT domain. The circuit design of the prototype DT-FFT processor is presented and measurement results from the CMOS 0.13-μm test chip are shown. Results show that the processor demodulates OFDM at 1 GS/s with an accuracy better than 2.8% error vector magnitude while drawing 25 mW from a 1.2-V power supply. The processor demonstrates a measured dynamic range of 49 dB, a 13-dB improvement over that of a 6-bit quantization limited all-digital FFT processor and ADC pair. The DT-FFT is also shown to better tolerate large blocking signals with an 8-dB dynamic range improvement. The DT-FFT core area is 450 μm $\times$ 450 μm.**

***Index Terms*—Analog multipliers, CMOS analog integrated circuits, discrete Fourier transforms, mixed analog–digital integrated circuits, orthogonal frequency division multiplexing (OFDM), signal processing, ultra-wideband (UWB).**

I. Introduction

As DIGITAL wireless communication systems utilize increasingly wider spectral bandwidths, the required operating speed of the baseband signal processing and ADC stretch the ability of traditional architectures to provide robust radio performance [1]. In ultra-wideband (UWB) orthogonal frequency-division multiplexing (OFDM) wireless systems, the additional operational bandwidth increases the likelihood of encountering narrowband blockers, which must be removed while still recovering most of the valuable spectral content. The ability to remove these blockers from the desired receive channel would ensure optimal receiver performance in the most challenging environments.

In narrowband systems, radio selectivity is typically attained through a cascade of filters including: RF *band select* filters, analog/mixed-signal *channel select* filters, and digital *channel select* filters. While *digital* channel select filters provide sharp attenuation from high-order filtering, *analog/mixed-signal* channel select filters have the principal purpose of reducing out-of-channel blockers to a magnitude within the dynamic range of the ADC. When a blocker is not sufficiently attenuated, the ADC is either overloaded, causing significant distortion, or the automatic gain control (AGC) reduces the blocker to the full-scale level of the ADC and the desired channel is pushed below the quantization noise floor of the ADC.

In UWB systems, when blockers lie within the target channel, the ADC cannot benefit from the dynamic range of the channel select filter and must either have exceptional dynamic range or suffer significant data loss when in-channel blockers are present. To exacerbate the problem, high-speed UWB capable ADCs reported in the literature with low power consumption ($\leq$100 mW) have not demonstrated a signal-to-noise-and-distortion ratio (SNDR) in excess of 38 dB [2]–[5]. Indoor multipath channel environment studies for UWB have shown that for high data-rate reception, the receiver's ADC needs at least 31 dB of SNDR [6]. With a margin added for blockers, an ideal ADC might have 51 dB or more SNDR. To address this problem, the use of tunable RF notch-filters has been proposed [7], [8]. In this work, an analog/mixed-signal sub-channel filtering approach is proposed based on a discrete-time (DT) fast Fourier transform (FFT) processor.

The advantages of a DT-FFT processor were first studied in [9] and [10] where an improved receiver architecture was presented that performs OFDM demodulation in the DT domain ahead of the point of digitization (the ADC). As shown in Fig. 1, in the receiver, the point of digitization is moved further back in the system, allowing the FFT processor to better isolate narrowband blockers within the sub-channels and remove them, acting as a multiinput multioutput filter. System simulations of a DT-FFT processor for future generation UWB OFDM transceivers processing multigigahertz of spectrum demonstrated an improved linearity and system selectivity through system level simulation results. These simulations show that the dynamic range increases from 35 to 54 dB, and that large full-scale narrowband blocking signals can be rejected by a DT-FFT processor. Synchronization was shown in [9] to remain unchanged for established OFDM synchronization techniques utilizing 2- or 1-bit quantization such as pseudonoise sequence preambles.

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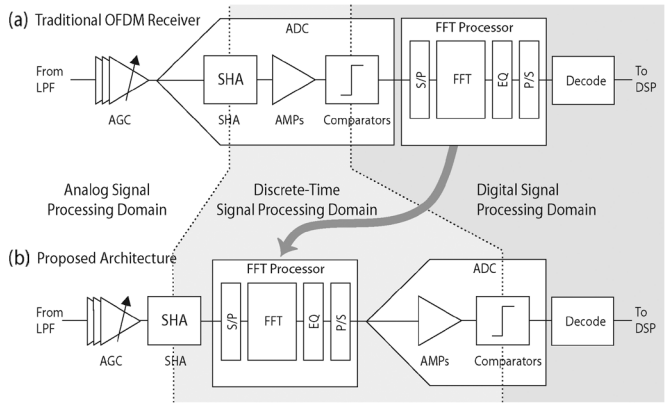


Fig. 1. Block diagram of the baseband signal processing portion for a: (a) traditional OFDM receiver and (b) the proposed modified OFDM receiver. Three different signaling domains separate the circuit functions.

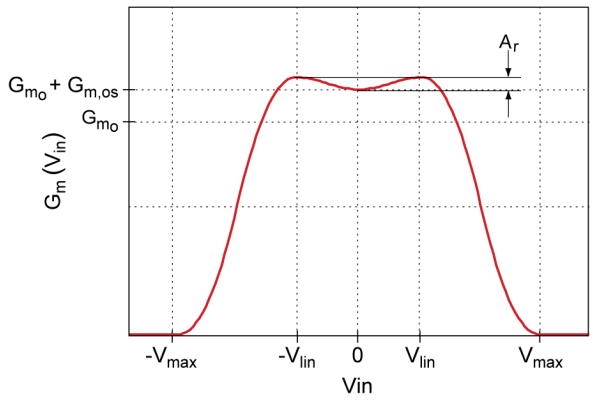


Fig. 3. Key parameters in the multiplier transconductance function. A_r, amplitude ripple, $V_{\rm lin}$ quasi-linear voltage range, and $G_{m,os}$ transconductance offset.

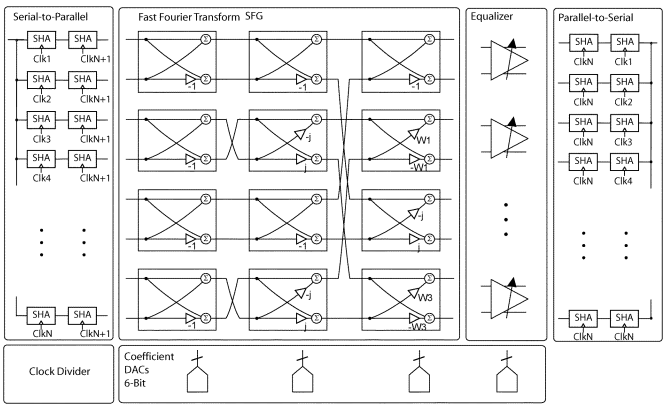


Fig. 2. Partitioning of the DT-FFT processor functions.

The advantages of the DT-FFT processing approach are improved dynamic range, improved receiver performance in crowded wireless environments, and high speed potentially beyond 5 GS/s. The disadvantage compared to the all-digital approach is the increased design complexity of analog/mixed-signal design versus all digital design. In this paper, the DT-FFT processing approach first described through system simulations in [9] is built upon through the integrated circuit design of a functioning CMOS prototype and measurement results demonstrating the DT-FFT processor's SNDR and dynamic range while operating at the full 1-GS/s data rate.

This paper is organized as follows. In Section II, the DT approach to implementing the FFT processor is described and circuit topologies are selected and designed to implement the necessary circuit functions [multipliers, adders, and sample-and-hold amplifiers (SHAs)]. In Section III, integrated circuit layout, floor planning, and instrumentation circuitry to interface with 50-Ω test equipment are discussed. In Section IV, measurement results of the CMOS 0.13-μm test chip are presented and the improvement to receiver selectivity is analyzed. Conclusions are drawn in Section V.

II. Circuit Design and Layout

The block diagram of the DT-FFT processor functions is shown in Fig. 2. The processor consists of six primary functions: *serial-to-parallel converter*, *FFT signal flow graph* (SFG), *equalizer*, *clock divider*, *coefficient bias DACs*, and *parallel-to-serial converter*. The inputs to the DT-FFT processor are sampled symbols from a high-speed SHA that are converted (down-sampled) in the *serial-to-parallel converter* to a set of parallel symbols of $N_{\rm FFT}$ longer than the sample period. The FFT SFG is a radix-2 decimation in time configuration comprised of repeatable butterfly structures based on analog G_m cell multipliers and linear adders. The coefficients required by each butterfly structure are set by static 6-bit coefficient bias DACs. The outputs of the FFT SFG are $N_{\rm FFT}$ parallel sub-channels that are passed to the *equalizer*. In the *equalizer*, attenuation or amplification of the individual sub-channels is applied to eliminate blocked sub-channels and provide preliminary equalization, which reduces the dynamic range requirements of the ADC. The output of the *equalizer* is passed to the *parallel-to-serial converter* and then sent to a low bit order ADC. The output can either be serial or parallel depending on whether or not the ensuing ADC is time interleaved.

The results of extensive system simulations in [9] demonstrated that the DT-FFT processor could be constructed from simple repeatable circuits: SHA, coefficient multiplier, and linear adder each with reasonable parasitics. High linearity or complicated feedback structures are not needed. Rather, circuit topologies based on power-efficient open-loop single-pole topologies yield acceptable DT-FFT processor performance. As a means to parameterize the large-signal transconductance transfer function for the multipliers, several metrics were introduced and are repeated here in Fig. 3: $V_{\rm lin}$, the range of voltage inputs where the transconductance function is quasi-linear, $V_{\rm max}$, the approximate range of voltage inputs with positive transconductance, $V_{\rm lin}/V_{\rm max}$, the fraction of the voltage range that is quasi-linear, A_r, the normalized peak-to-peak transconductance ripple in the quasi-linear region, σ_{A_r}, the standard deviation of amplitude ripple, $\sigma_{G_{m,os}}$, the standard deviation of the small signal transconductance, $\sigma_{V_{\rm in,os}}$, the standard deviation of input offset voltage. Table I, lists the design goals for each of these parameters necessary to implement a DT-FFT processor with dynamic range greater than 50 dB. The design strategy is to implement the entire possessor based on numerous instances of a few fundamental circuit blocks.

TABLE I
DESIGN GOALS FOR COMPONENTS OF THE 1-GS/s DT-FFT PROCESSOR

Parameter	Description		Value
V_{lin}	quasi-linear range of G_m		maximize
V_{max}	positive range of G_m		
V_{lin}-to-V_{max}	quasi-linear fraction of G_m	$\geq$	0%
A_r	amplitude ripple	$\leq$	10%
min G_{m_o}	Min. tuning range of G_{m_o}	$\leq$	5 $\mu A/V$
max G_{m_o}	Max. tuning range of G_{m_o}	$\geq$	100 $\mu A/V$
σ_{A_r}	std. dev. of amplitude ripple	$\leq$	10%
$\sigma_{G_{m,os}}$	std. dev of G_{m_o}	$\leq$	10%
$\sigma_{V_{in,os}}$	std. dev. input offset voltage	$\leq$	0.5 mV
I_{bias}	multiplier bias current	$\leq$	80 μA
f_c	3 dB corner frequency	$\geq$	700 MHz
clock jitter	jitter	$\leq$	10 pSec

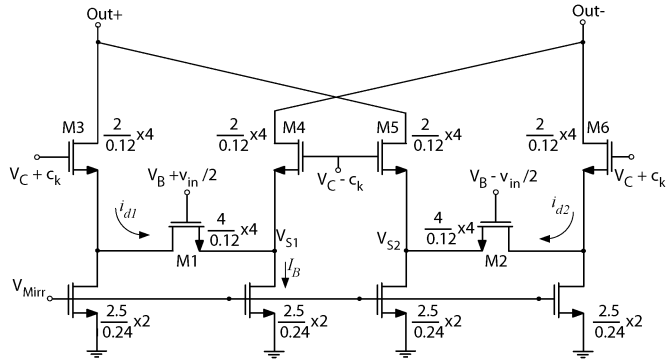


Fig. 4. Coefficient multiplier circuit based on a linear transconductor is used in the construction of the FFT butterfly structure.

A. Coefficient Multiplier

The multiplier is one of the most important functional blocks of the DT-FFT processor. It can be implemented as a linear transconductor with variable coefficient c of the form $Y = c \cdot X$. Since the direct conversion receiver is quadrature (Q), four phase signaling, differential in-phase (I) and differential Q is required to implement complex multiplication. There are many circuit topologies found in the literature that implement four quadrant multiplication, $Y = X_1 \cdot X_2$, and coefficient multiplication, $Y = c \cdot X$ [11]–[18]. A number of multiplier topologies rely on circuit feedback loops to linearize the response; however, due to the speed requirements of this work, open-loop topologies with a single pole are better suited for baseband bandwidths exceeding 500 MHz [18], [19]. To maximize the output voltage swing, the number of transistors stacked vertically should also be kept to a minimum. Given a 1.2-V supply, a linear multiplication range of 400 mV_{pk-pk} is feasible [18], [20], [21].

To determine the target bias current, it is noted that the power consumption of typical all-digital FFT processors is in the range of 24–36 mW at 1 GS/s when scaled to $N_{\text{FFT}} = 8$, 0.13-μm technology, and $V_{dd} = 1.2$ V [22], [23]. In order to improve upon these levels, the total target power for the DT-FFT processor is 10 mW. Based on the need for 104 multipliers and a 1.2-V supply, 80 μA of current is available to the design of each multiplier.

The transconductor circuit shown in Fig. 4 is well suited to meet the above goals. It uses only two transistors stacked vertically and all of the transistors are biased in weak inversion to take advantage of a higher g_m/I_d, making them power efficient. The circuit basically consists of two differential pairs formed by M3–M6, which steer signal current through M1 and M2, and set a desired V_{ds} on M1 and M2, ensuring they are biased in the subthreshold region. When a differential voltage, $\pm c_k$ is placed on the gates of M3–M6, the sources are imbalanced so that V_{s4}, V_{s5} are lower than V_{s3}, V_{s6}. This results in a difference voltage $V_{\text{ds}} \approx 2c_k$ on M1, M2. The drain current for subthreshold MOSFETs with $V_{\text{ds}} < 200$ mV is given in the BSIM4 model by

$$I_{\text{ds}} = I_0' \left[1 - \exp\left(\frac{-V_{\text{ds}}}{\nu_t}\right)\right] \exp\left(\frac{V_{\text{gs}}}{n\nu_t}\right) \tag{1}$$

resulting in

$$i_{\text{ds1}} = I_{0,1}' \left[1 - \exp\left(\frac{-2c_k}{\nu_t}\right)\right] \exp\left(\frac{V_B + v_{\text{in}}/2 - V_{s1}}{n_1\nu_t}\right) \tag{2}$$

where V_B is the dc bias voltage applied to M1, M2. To find i_{ds1} as a function of V_{in}, the term V_{s1} must be resolved. In other words, the degeneration impedance looking into the source of M4 must be accounted for in (2). Although small-signal analysis gives straight forward results for $V_{\text{in}} = 0$, in order to predict the third-order input intercept point (IIP3) for larger V_{in}, a large signal solution for i_{ds1} is sought.

Summing the currents at V_{s1} gives $i_{\text{ds4}} = I_b - i_{\text{ds1}}$ and

$$i_{\text{ds4}} = I_{0,4}' \exp\left(\frac{V_C - c_k - V_{s1}}{n_4\nu_t}\right) \tag{3}$$

where I_b is the dc bias current provided by the current mirrors and V_C is the dc bias current applied to M3–M6. Solving for V_{s1} and substituted into (2) gives

$$i_{\text{ds1}} = I_{0,1}' \left[1 - \exp\left(\frac{-2c_k}{\nu_t}\right)\right] \times \exp\left(\frac{v_{\text{in}}/2 + V_b - V_C + c_k + n_4\nu_t \ln\left(\dfrac{(I_b - i_{\text{ds1}})}{I_{0,4}'}\right)}{n_1\nu_t}\right). \tag{4}$$

The first-order Taylor series of (4) is taken with respect to i_{ds1} since no direct solution of (4) exists. This gives

$$i_{\text{ds1}} \approx \frac{\Psi \exp\left(\dfrac{V_{\text{in}}}{2n_1\nu_t}\right)}{\frac{n_4}{n_1 I_b}\Psi \exp\left(\dfrac{V_{\text{in}}}{2n_1\nu_t}\right) + 1} \tag{5}$$

where the constant

$$\Psi = I_{0,1}' \left[1 - \exp\left(\frac{-2c_k}{\nu_t}\right)\right] \times \exp\left(\frac{V_B - V_C + c_k + n_4\nu_t ln\left(I_b/I_{0,4}'\right)}{n_1\nu_t}\right). \tag{6}$$

It can be seen that the magnitude of i_{ds1} is set by c_k, through Ψ. Furthermore, i_{ds2} is identical to (5) with opposite sign for V_{in}.

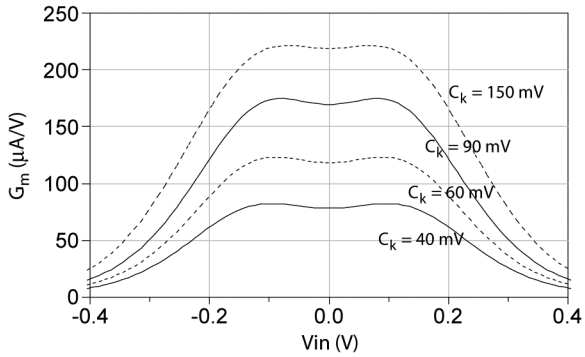


Fig. 5. Circuit simulation shows transconductance of the coefficient multiplier is adjusted through bias C_k.

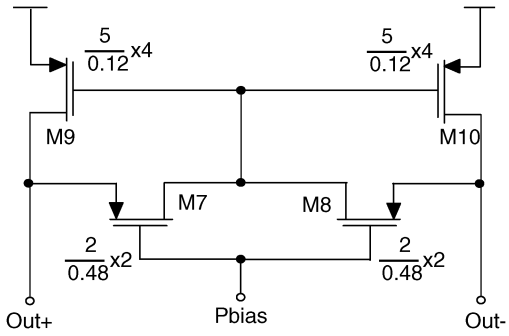


Fig. 6. Adder circuit used in the construction of the FFT butterfly circuits. The current inputs and voltage outputs use the same node since the circuit is transresistive in nature.

Summing the currents at the output nodes, $I_{\text{diff}} = 2i_{d1} - 2i_{d2}$, the differential output current is given as

$$I_{\text{diff}} \approx \frac{2\Psi\left(\exp\left(\frac{V_{\text{in}}}{2n_1\nu t}\right) - \exp\left(\frac{-V_{\text{in}}}{2n_1\nu t}\right)\right)}{\left[\frac{n_4}{n_1 I_b}\Psi\exp\left(\frac{V_{\text{in}}}{2n_1\nu_t}\right)+1\right]\left[\frac{n_4}{n_1 I_b}\Psi\exp\left(\frac{-V_{\text{in}}}{2n_1\nu_t}\right)+1\right]}. \tag{7}$$

Equation (7) serves as a good large-signal approximation of the circuit in Fig. 4 through the quasi-linear region. Quick empirical analysis using (7) and its derivatives allows large-signal transconductance and IIP3 to be analyzed while making sizing and biasing decisions about the circuit that will maximize IIP3 over the quasi-linear region. The amplitude ripple A_r, from the behavioral model presented in [9], is also a good approximation of IIP3 and is given as

$$A_r = \left(\frac{4a}{\pi}\frac{1}{10^{\text{IIP3}/20}}\right)^2. \tag{8}$$

In general, minimizing A_r results in optimal IIP3 and minimal nonlinear distortion.

Fig. 5 shows a plot of G_m versus V_{in} for this circuit for several values of c_k. The transconductance remains quite linear over the range of 250 mV_{pk-pk} with $A_r \leq 4\%$. Outside of the quasi-linear region, the exponential behavior of either M1 or M2 saturates and the transconductance decreases. This is seen in the denominator of (5), which results in a nearly linear roll-off of the transconductance with increasing V_{in} and causes large signals to be compressed gradually rather than being hard clipped, thus reducing harmonic distortion and improving performance. For the simulation shown in Fig. 5, this occurs at V_{in} of ± 150 mV. Thus, the circuit demonstrates suitable characteristics for a programmable coefficient multiplier.

The bias voltage V_C, and the multiplication coefficient c_k are applied by a DAC to the inputs of M3–M6. Low-speed 10-kS/s 6-bit DACs c_k provide enough resolution to vary G_{m_0} from 0 to 200 μA/V and to drive the target $\sigma_{G_{m,os}}$ level to below 1% while consuming less than 25 μW per DAC in 0.13-μm technology [24]–[26].

B. Adder

The adder acts as a transresistor, summing the input currents and converting them into an output voltage at the desired common-mode level. The simplest way to do this is with passive lumped element resistors [18]. However, this approach does not have the flexibility of setting the common-mode bias level independent of the resistance so this topology limits the bias current and operating speed to one value. A method that separates the common- and differential-mode resistance allows more flexibility in adjusting the differential resistance level independent of the bias current [27].

In this work, the adder is a transresistive circuit that adds multiple differential current signals together to create a single differential output voltage. The adder circuit shown in Fig. 6 has the features of small size, adjustable differential resistance, and common-mode feedback to stabilize the common mode bias in the G_m multipliers. The inputs to the circuit are differential currents applied to the ports Out+ and Out−, coming from the preceding G_m stages. The output of the circuit is the differential voltage between the same nodes Out+ and Out−. Thus, the input and output are physically at the same location, but the signaling domain changes from current to voltage.

Normally, transistors M7 and M8 operate in the linear resistive region, while M9 and M10 operate in saturation as current sources. The linear resistors M7 and M8 provide the resistance needed to convert the differential input currents to voltage signals. The value of their resistance can be tuned by adjusting P_{bias}. For simplicity, P_{bias} can be connected to ground; however, for the prototype design, it is brought off-chip as another means of fine tuning the circuitry.

The differential resistors M7 and M8 also operate to average the voltages on Out+ and Out−, providing the common-mode value that is fed back to the gates of the current source transistors M9 and M10. The common-mode feedback allows the circuit to tolerate variations in the bias current from the G_m multipliers without affecting the common-mode output voltage and enables the circuit to maintain an optimal wide voltage swing. Fig. 7 shows the simulated resistance versus V_{in} of the adder for several values of P_{bias}. When the differential input current is large, the transistors M7 and M8 saturate, and the differential resistance of the adder circuit increases creating a nonlinearity. This can be clearly seen in the case of $P_{\text{bias}} = 200$ mV; at higher values of P_{bias}, this effect grows worse. Thus, low values of

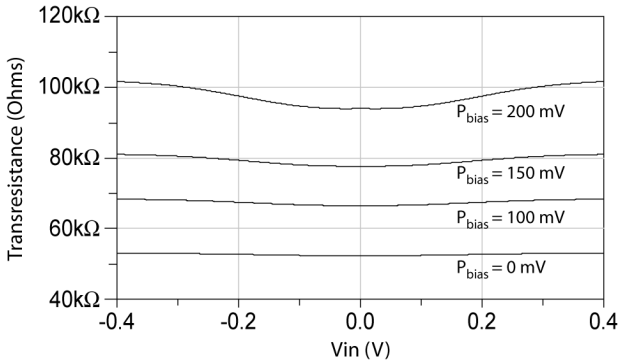


Fig. 7. Circuit simulation of the transresistance of the adder circuit.

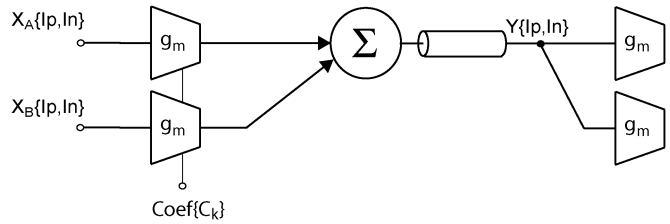


Fig. 8. Half butterfly circuit used in circuit simulations of the multiplier and adder.

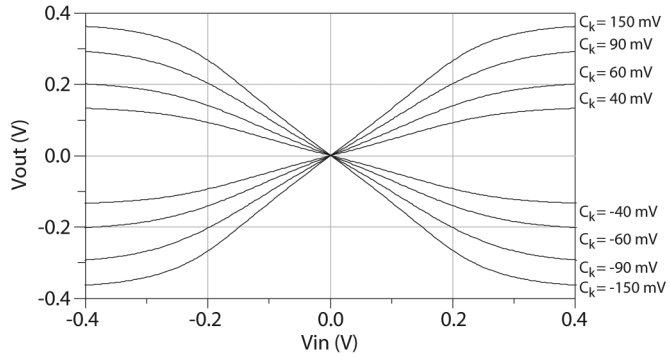


Fig. 9. Simulated voltage-in voltage-out transfer function of the half butterfly circuit.

$P_{\rm bias}$ are used so that the adder can implement a wide linear resistance with values of $R_{\rm add,diff}$ between 5–10 kΩ.

C. Half Butterfly Circuit Simulation

Within the FFT lattice, each adder is driven by two or three multipliers, and in turn drives two multipliers at the next stage. A simulation testbench to test the performance of a single coefficient multiplier and adder circuit working together is set up as shown in Fig. 8. Using this testbench, the swept voltage response is simulated and shown in Fig. 9. The maximum output voltage swing, $V_{\rm max}$, for the circuit at the unity gain value, c_k of 90 mV, is $\pm$300 mV.

The frequency response of the half butterfly circuit is given by (9)

$$\frac{V_{\rm out}}{V_{\rm in}} = \frac{G_{m_0} R_{\rm eq}}{s\frac{R_{\rm eq}}{2}(4C_{dd,M3}+C_{\rm wire}+2C_{dd,\rm add}+2C_{gg,M1})+1} \tag{9}$$

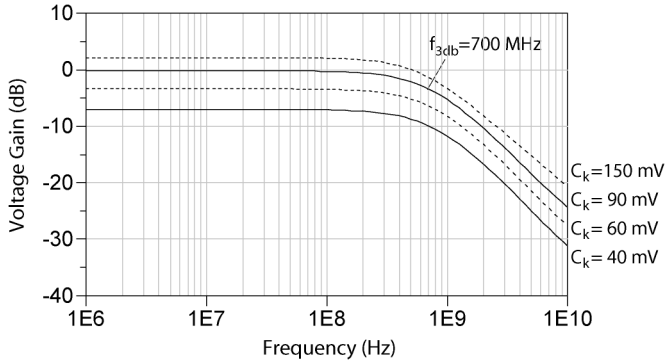


Fig. 10. Simulated frequency response of the half butterfly circuit with loading.

where $R_{\rm eq} \cong (R_{\rm add,diff}||(R_{{\rm ds},M3}/4))$ and $C_{\rm wire}$ accounts for the wiring capacitance of the connections between the one butterfly stage and the next. A design tradeoff exists between sizing the multiplier output n-channel field-effect transistors (NFETs) M3–M6 in that a large width and length make a linear response, but lower the corner frequency. The simulated frequency response of the half butterfly circuit is shown in Fig. 10. The 3-dB bandwidth of the circuit is seen to pass 700 MHz, which meets the goals set in Table I for a 1-GS/s DT-FFT processor.

D. Sample-and-Hold Amplifiers

Sample-and-hold amplifiers are used to implement the serial-to-parallel function and parallel-to-serial function. High-speed SHAs are typically open loop and utilize a single switch, a shunt charge holding capacitor and a unity gain amplifier [28]–[30]. Several methods are applied to reduce the charge pedestal, such as the use of an opposite phase dummy switch [31] or the use of feedback circuits that sense clock feed-through and drive a cancellation signal into the gate of the switch [28], [30]. In this design, the dummy switch approach is chosen to keep the circuit compact.

Fig. 11(a) shows one-half of the pseudodifferential SHA based on an NFET switch. The dual of this SHA with a p-channel field-effect transistor (PFET) switch is also used in the design, shown in Fig. 11(b). The SHA operates in two modes controlled by the sampling clock. In the tracking mode, the switch M1 is closed and the hold capacitor charges to the input voltage level and then tracks it. In the hold mode, the switch M1 is placed in a high-impedance state and the voltage on the capacitor $C_{\rm hold}$ ideally remains fixed. In both states, the source follower M3 acts as a buffer amplifier to read out the voltage on the hold capacitor.

The capacitance $C_{\rm hold}$ is sized large enough to meet the hold requirements and reduce the parasitic capacitive variation of M1. The buffer amplifier is designed to drive the load capacitance of the following stage with good linearity over a voltage swing of 400 mV$_{pk-pk}$ and a rise time better than 0.5 ns.

In Fig. 12, a simulation of the PFET switch differential SHA shows that the pedestal offset is negligible near zero input voltage, yet at wide voltage swings, near $V_{\rm in} = -400$ mV, the pedestal offset is 40 mV. This is due to the small contribution of nonlinear capacitance in M1 and M2. The pedestal will contribute minor distortion to the DT-FFT processor at larger

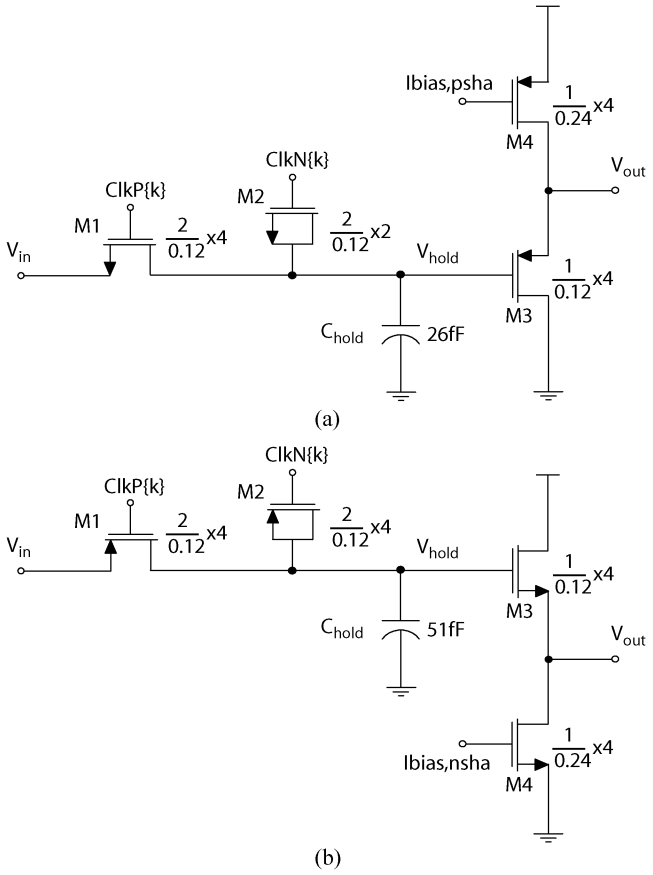


Fig. 11. NFET- and PFET-switch-based sample-and-holds with source following amplifier. (a) One half of NFET-switch-based SHA. (b) One-half of PFET-switch-based SHA.

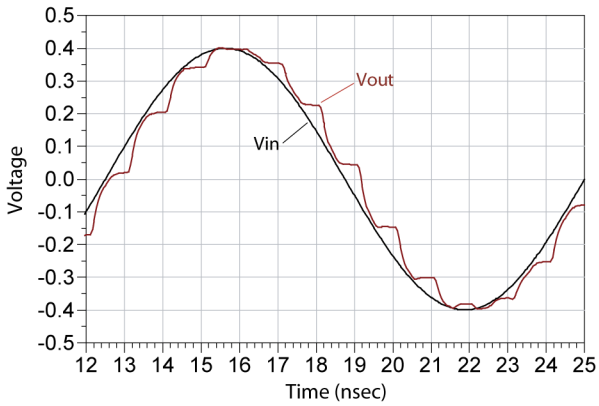


Fig. 12. Simulation results of an 800-mV$_{pk-pk}$ 80-MHz sine-wave passed through the differential track-and-hold with 1-GHz clock.

signal magnitudes. The total power consumption of the SHA operating at 1 GS/s is found in simulation to be 117 μW.

E. Clock Generation Circuitry

To provide the necessary clock signals to the serial-to-parallel converter and parallel-to-serial converter, the input clock is derived into N_{FFT} clock phases with the clock divider of Fig. 13. To account for the cyclic prefix specific to OFDM demodulation, two additional clock phases clk8 and clk9 are added to initiate a wait time while the cyclic prefix passes between the OFDM symbols.

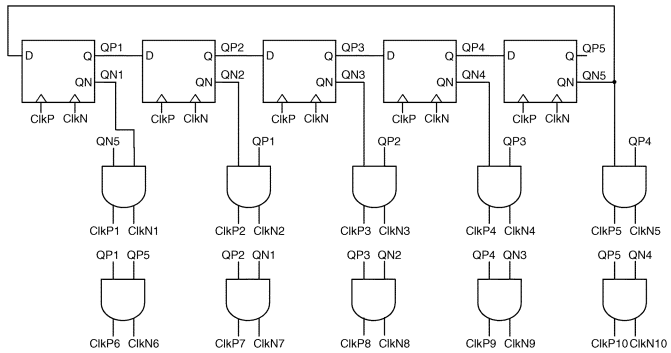


Fig. 13. Ten-phase clock divider used by the serial-to-parallel function.

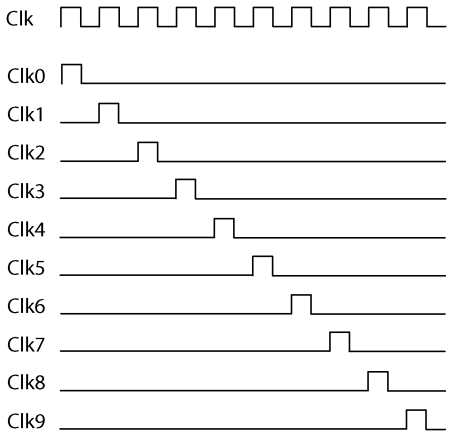


Fig. 14. Ten clock phases used for processor timing. Eight phases are used for the serial-to-parallel function and two are aligned to the cyclic prefix.

A shift register is created by chaining five D-flip-flops (DFFs) together and gating their outputs to create ten sequenced phases with NAND gates [32]. Fig. 14 shows the timing generated by the clock divider. The DFFs are based on the "Power-PC" master–slave architecture [33], [34] and simulated to operate with up to 2-GHz input clock.

III. Implementation

The prototype FFT processor is constructed using coefficient multiplier and adder circuits to synthesize the FFT SFG, SHAs to implement the serial-to-parallel function, and clock divider to create the necessary clocking scheme, as shown in Fig. 2. These functions constitute the processor core. The first FFT prototype design was limited to $N_{\mathrm{FFT}} = 8$ in order to minimize the chance of implementation errors and to validate the proposed approach. Higher order DT-FFTs can be implemented based on this eight-point core in a manner similar to the all digital FFT approach used in [35]. Furthermore, it is also straightforward to extend this work to perform the IFFT function using the same FFT core by re-programming the transconductor coefficients.

In order to test the processor chip, additional interface circuitry is necessary. *RC* filters are placed on all of the bias inputs to reduce noise coupling from the test cabling, 50-Ω terminations are provided for the high-speed inputs and 50-Ω output drivers are provided to interface the weak on-chip signals to test equipment. To filter bias voltages, 10-pF capacitors are placed

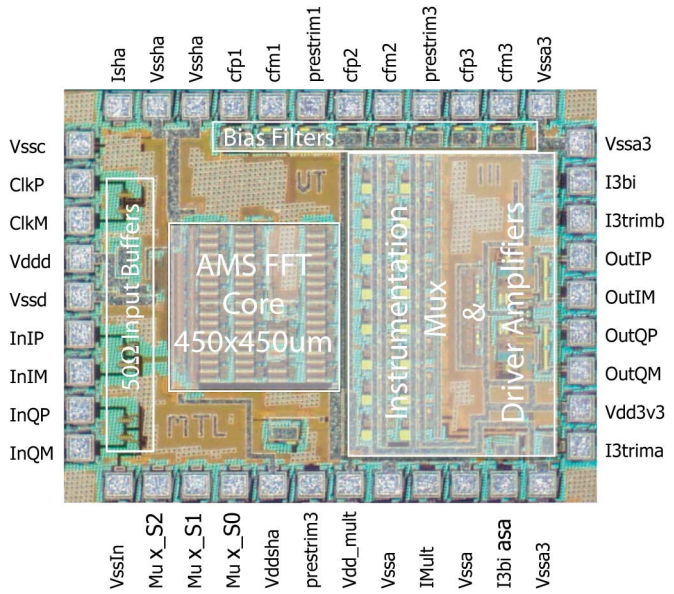


Fig. 15. Die photograph of the DT-FFT processor prototype with pins and sections labeled.

near the bias pads and 10-kΩ resistors are placed in series between the off-chip DAC and the multipliers on-chip. To filter bias currents, 10-pF capacitors with 100-Ω resistors are placed between the pad and current mirrors. A parallel bank of instrumentation buffer amplifiers, designed to have wide-bandwidth and low input capacitance, are placed at the outputs of the processor core. The outputs of the parallel instrumentation buffer amplifiers are switched to drive the large input capacitance of the 50-Ω driver amplifiers. The 50-Ω driver amplifiers are designed to have a bandwidth greater than 700 MHz and a wide output swing so as to not affect the measurements of the FFT processor and to be stable with 50-Ω loads. Together, the 50-Ω input terminations, bias filters, instrumentation MUX, and 50-Ω driver amplifiers are added to the FFT core in the final test chip.

The test chip was designed and fabricated in the Jazz CA13 0.13-μm CMOS process, which has a single poly and six metal layers. Fig. 15 shows the fabricated die with the key sections labeled. The processor core is contained within the 450 μm $\times$ 450 μm block labeled "AMS FFT Core." The interface circuitry is also shown. Ultimately, the die is pad limited, and thus there are several areas of metal fill around the bias filters and driver amplifiers. A full custom layout methodology was used with extensive reuse of hierarchical blocks to minimize layout time. Common centroid layout techniques were used to reduce mismatch in the multipliers, adders, and SHAs. Three separate power domains were used to separate the digital, mixed, and analog signal processing circuits. Substrate guard rings were placed between these domains to isolate switching noise from coupling into the analog circuits. In Section IV, the measurement setup and results of the test chip are presented.

IV. Measurement Results

A. Setup

The goal of the test setup is to apply full data-rate signals to the processor that emulate the expected conditions seen in a typical UWB direct conversion receiver. For the purposes of measuring distortion contributed by the processor, stimulus signals are created in MATLAB and applied both to the physical measurement setup and also to an ideal FFT within MATLAB. After passing through the physical measurement setup, equalization, frame, and symbol timing recovery are performed. These measured results are then compared against the ideal case. Equation (10) is used as follows to calculate the SNDR based on this approach:

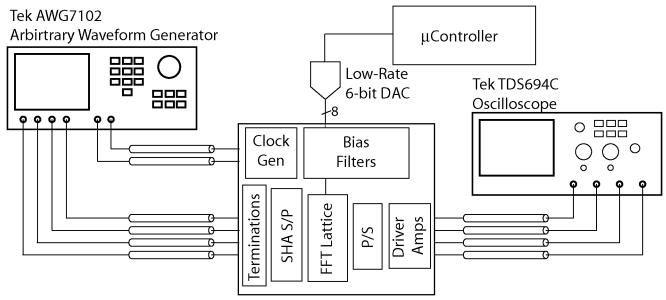


Fig. 16. Physical measurement setup used to measure the DT-FFT processor.

$$\mathrm{SNDR} = 20\log 10 \frac{\sqrt{\frac{1}{N}\sum_{k=1}^{N} V_{\mathrm{ideal}}(k)^2}}{\sqrt{\frac{1}{N}\sum_{k=1}^{N} \left(V_{\mathrm{meas}}(k) - V_{\mathrm{ideal}}(k)\right)^2}}. \tag{10}$$

When the input magnitude of the sub-channels are swept versus SNDR values, the measure of dynamic range can be found. Dynamic range is defined as the range of input magnitudes for which the SNDR is sufficient to ensure a bit-error rate (BER) of less than 1×10^{-5} (7 dB for quadrature phase-shift keying (QPSK) coded OFDM) [6].

Fig. 16 shows the physical measurement setup used for the measurements. Differential I and Q signals are generated in the Tektronix AWG7102 arbitrary waveform generator (AWG). A differential clock signal is also derived from the AWG. To provide the target data rate of 1 GS/s to the DT-FFT processor, the AWG is oversampled and clocked at 2 GS/s to provide sharp rectangular symbols to the processor inputs that emulate those that would be found inside the receiver at the interface to the DT signaling domain.

To control the output MUX, set the bias levels and control the coefficients used in the FFT SFG, a micro-controller is connected to the two DACs. Three registers within the micro-controller contain the multiplication coefficients of the FFT SFG. Eight additional registers are used to set bias voltages and currents within the test chip and allow flexibility in the setting of operating conditions. The instrumentation output multiplexer is also controlled by the micro-controller. Although the micro-controller and DACs would typically be found on-chip in a fully integrated transceiver, in this proof-of-concept work they were left off-chip to reduce complexity and implementation risk. Fig. 17 shows a photograph of the printed circuit board containing the test chip, micro-controller, two eight-channel low data-rate bias DACs, voltage regulators, and decoupling capacitors.

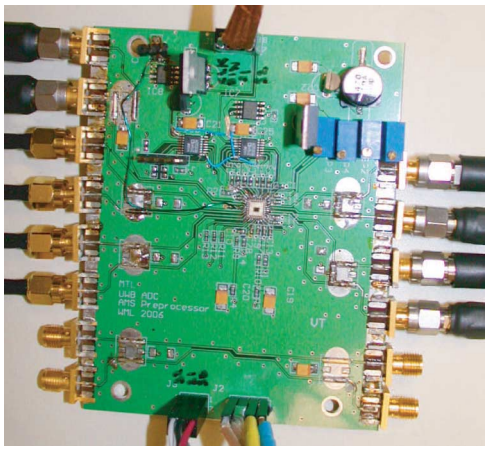


Fig. 17. Printed circuit board with the test IC, bias DACs, and voltage regulators.

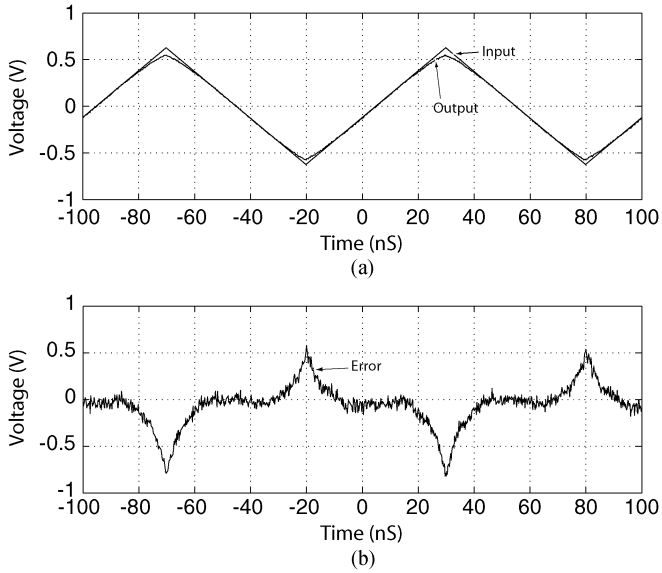


Fig. 18. Measurement results of a 10-MHz 600-mVpk triangle wave applied to the instrumentation amplifier. The Input and Output signals are shown in (a) and the difference, or error signal, is shown in (b).

The parallel output channels from the FFT processor are routed through the on-chip analog multiplexer and driver amplifiers to the Tektronix 694 C oscilloscope. The differential I and Q signals are combined and the parallel-to-serial function implemented in post-processing to avoid nonidealities that would be contributed by the use of off-chip baluns in the test setup. The output signal measurement requirements are less stringent than the input requirements due to decimation in time created in the processor's serial-to-parallel operation and a parallel output in the test chip. Thus, a factor of 10 downsampling reduces the symbol-rate at the oscilloscope to a 100-MS/s rate when the processor is operating at 1 GS/s and clocked at 1 GHz. However, to fully capture the harmonics associated with any potential distortion caused within the processor, a 1-GHz analog bandwidth is required of the oscilloscope.

Another critical piece of the test setup is the RF cabling. It is required to maintain better than 18° matching at 1 GHz between the four RF input cables and the two clock input cables. This value will ensure that the I and Q symbols are well aligned and that the clock is being phased at the correct sample point in each symbol. 18° at 1 GHz is less than 5 mm in a typical coaxial cable. Since this is difficult to achieve with off-the-shelf matched coaxial cables, adjustable in-line coaxial delay elements were also used.

To calibrate the test setup, three chip variants were laid out and fabricated: two calibration chips and the proof-of-concept DT-FFT chip. The first calibration chip is a through chip with only input buffers and output instrumentation amplifiers and driver amplifiers, the second calibration chip additionally contains the serial-to-parallel function with clocking serial-to-parallel block.

B. S-Parameters Measurement of Through Path Circuit

The first chip variant was used to calibrate the instrumentation amplifiers and driver amplifiers. Using an Agilent E8364B vector network analyzer, with baluns and bias-tees in place of the AWG and oscilloscope in Fig. 16, S-parameter measurements were taken. The S-parameters were measured at several different signal levels to ensure that the output drivers could faithfully reproduce large signals. As shown in Fig. 20, the measured $S11$ was less than -10 dB to 2 GHz allowing for a flat frequency response and accurate symbol transfer between the 50-Ω test equipment and the processor IC. The $S21$ response of -1.8 dB was flat, ensuring minimal attenuation of high frequencies by the instrumentation amplifiers during measurements.

C. Measurement of the Serial-to-Parallel Function

The second chip variant was used to measure the timing and verify the function of the serial-to-parallel function. Using the test setup as shown in Fig. 16, a 10-MHz 600-mV$_{pk}$ triangle wave was generated in MATLAB and applied from the AWG to the prototype IC. The measured response was captured by the oscilloscope and returned to MATLAB where the differential I and Q symbols from the four oscilloscope channels were converted to a single complex symbol array. The input and output signals are shown in Fig. 18(a); the error voltage between them is shown in Fig. 18(b). The amplitude is compressed near the maximum and minimum values of the triangle wave, which indicates that the input range of 720 mV$_{pk-pk}$ is the maximum linear range of the driver amplifier. Thus, a full-scale magnitude of 400 V$_{pk-pk,\mathrm{diff}}$ is selected for the DT-FFT processor to ensure minimal distortion.

To verify the decimation function of the serial-to-parallel conversion, a second test was performed with QPSK encoded, $N_{\mathrm{FFT}} = 8$, OFDM pseudorandom data. The OFDM symbol stream was applied to the input and each of the decimated sub-channels was verified to have better than 35-dB SNDR. For OFDM demodulation, the removal of the cyclic prefix using the wait states was also verified. Fig. 19 shows a screen shot from the I+ channel of the decimated OFDM input symbol stream. Each symbol was flat and did not show measurable charge pedestal or glitching.

Having verified the correct functionality of the instrumentation amplifiers, and the serial-to-parallel function, the next step

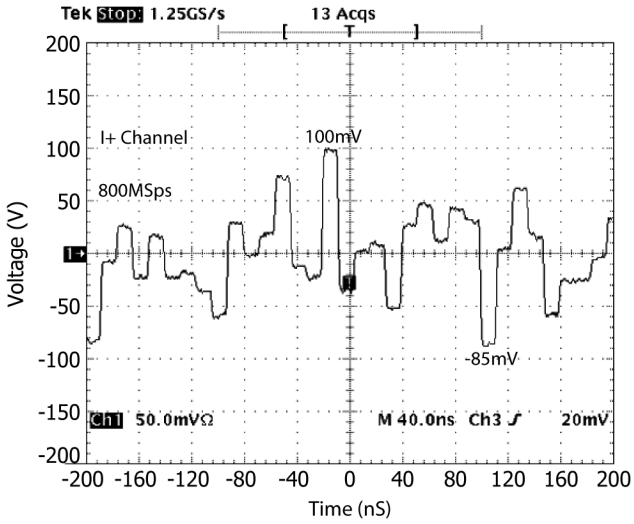


Fig. 19. Measured output of the serial-to-parallel function with OFDM stimulus: a down-sampled OFDM symbol stream.

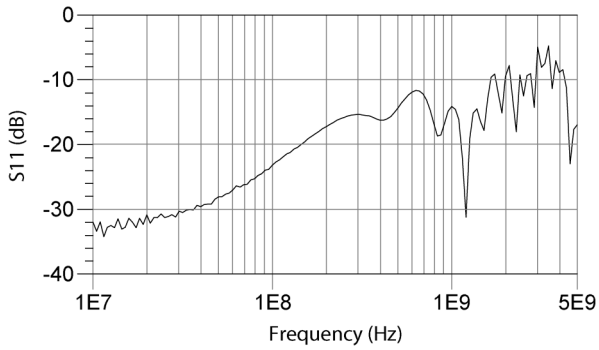


Fig. 20. Measured $S11$ of the test setup with baluns, bias tee, test board, and package demonstrates a good match to 2 GHz.

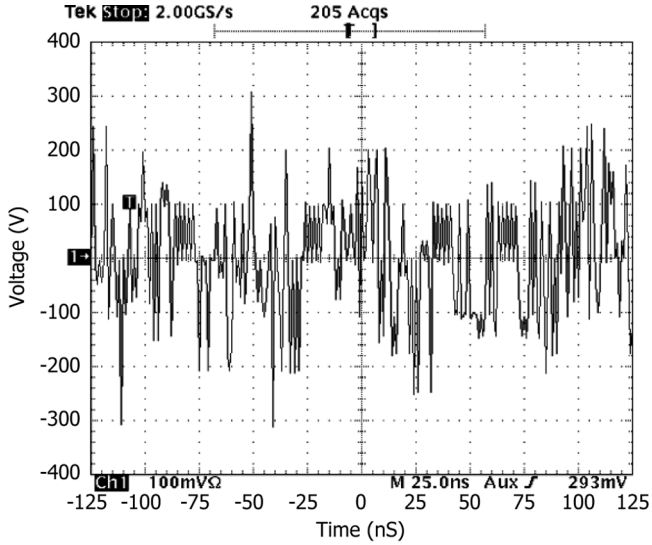
was to test the proof-of-concept IC variant containing the full processor core.

D. OFDM Demodulation

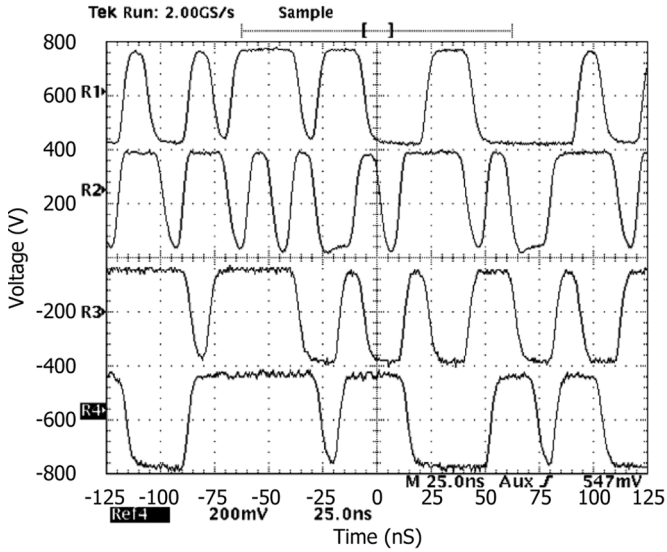
To measure the performance of the DT-FFT processor demodulating OFDM signals, the test setup of Fig. 16 was again used and an I and Q differential OFDM stimulus signal was applied to the processor and compared to simulation results from [9]. Fig. 21(a) shows the I+ channel of the stimulus signal. The stimulus signal is a 1-GS/s binary phase-shift keying (BPSK) modulated OFDM signal with eight mapped sub-channels containing pseudorandom data. BPSK modulation was chosen for initial tests over QPSK modulation because it is easier to interpret visually when viewed on the oscilloscope.

The oscilloscope screen capture of Fig. 21(b) shows four of the eight sub-channels demodulated to BPSK and measured at the I+ output of the processor. The rise time of the output symbols is measured to be 4.9 nS. This figure shows that the DT-FFT processor is able to demodulate OFDM symbols successfully at a rate of 1 GS/s.

Fig. 22 shows one of the measured BPSK sub-channels after recombining the differential signals in post-processing. The post



(a)



(b)

Fig. 21. (a) 1-GS/s OFDM input signal as applied to the input of the OFDM processor. (b) Four of the eight parallel demodulated outputs.

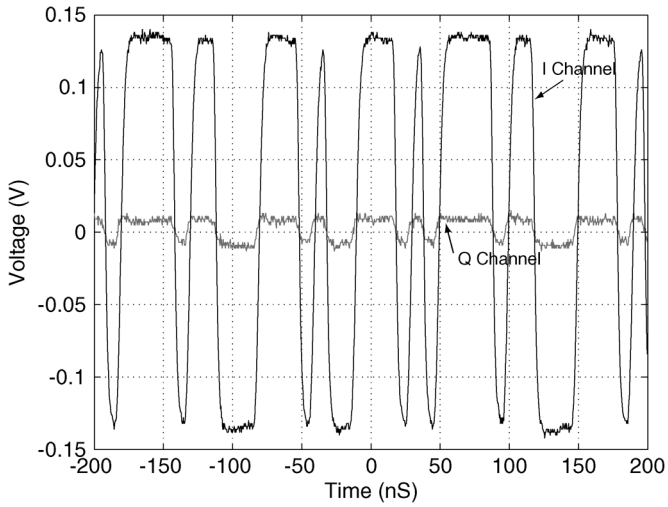


Fig. 22. Measurement results after being captured on the oscilloscope and recombined in MATLAB for a single demodulated output channel from the FFT processor.

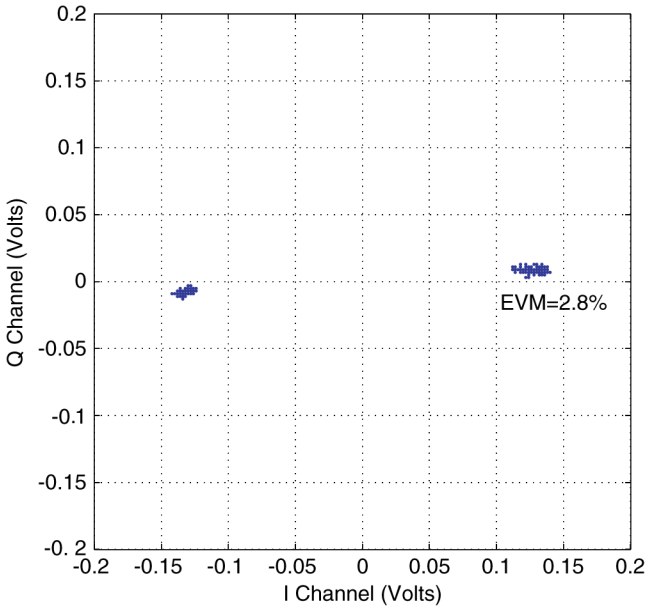


Fig. 23. Measurement results after symbol timing recover in MATLAB of a single demodulated output channel displayed in XY format.

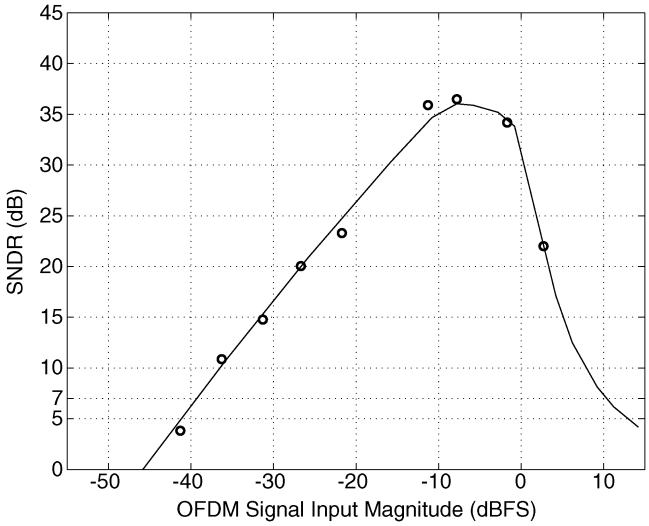


Fig. 24. Measurement results for the DT-FFT processor show a peak SNDR of 36 dB and a dynamic range of 49 dB.

processing in MATLAB includes differential recombining, equalization of sub-channels, and symbol timing recovery. Fig. 23 shows the constellation diagram of this measured signal in an XY format. A 1.9° phase rotation can be seen in the output, due to the imperfect matching of the output cable lengths. The error vector magnitude (EVM) was measured at 2.8%.

Next, the dynamic range of the processor was measured by sweeping the input signal magnitude of the OFDM sub-channels and measuring the SNDR using (10). The sweep results in a curve in Fig. 24, shows the dynamic range, measured between the 7-dB points on the SNDR curve, is 49 dB and the peak SNDR is 36 dB. A data fit curve is shown as the heavy line. Comparing the measured results in Fig. 24 with the quantization limited digital FFT processor of [9], the measured dynamic range of the DT-FFT processor is equivalent to 8.4 bits.

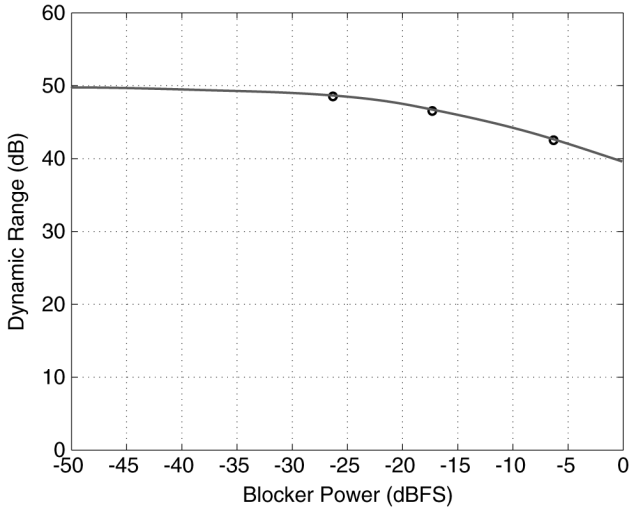


Fig. 25. Measurement results for the DT-FFT processor dynamic range after rejecting sinusoidal blocker of varied input magnitude.

E. Blocker Suppression

Fig. 25 shows the measurement results of a 345-MHz blocker tone added to the 1-GS/s OFDM input signal at various magnitudes of −26 dBFS, −17 dBFS, and −6 dBFS. The full-scale value of 400 $\mathrm{mV}_{pk-pk,\mathrm{diff}}$ is assumed to be the maximum value set by the receiver's AGC. For each blocker measurement, the corrupted sub-channel containing the blocker is attenuated and the remaining sub-channels are used to calculate SNDR. The high linearity of the half butterfly circuit enables the DT-FFT to tolerate large blockers with minimal degradation in dynamic-range performance.

The results of the blocker simulations are plotted versus dynamic range in Fig. 25. A curve fit of the data shows that the DT-FFT processor can effectively remove large blockers while maintaining good dynamic range up to the full-scale magnitude of the DT-FFT.

F. Performance Summary

The processor consumes a total power of 25 mW from a 1.2-V supply. 3.6 mW was consumed in the serial-to-parallel converter, 2.4 mW in the clock divider, and 19 mW in the FFT SFG. There are a total of 104 multipliers in the processor, resulting in 180 μW per multiplier. This is a factor (4×) larger than the design value of 40 μW; due to a mistake in the layout, the adder current mirrors were sized four times too small so that the current in the multiplier was forced to be adjusted four times larger in measurements to compensate. Without this error, the processor would have consumed only 11 mW.

Since no other DT-FFT processors exist in the literature, power consumption is compared to all digital FFT processors. To scale results in the literature from larger technology nodes down to the 0.13-μm technology node, it is necessary to account for process constants using the typical proportionality factor CfV^2 [36]. To scale the prototype $N_{\mathrm{FFT}} = 8$, a complex radix-2 DT-FFT processor for comparison with the $N_{\mathrm{FFT}} = 128$, radix-4 real digital FFT processors that were built for MB-OFDM, it is noted that radix-R FFT processors are

TABLE II
COMPARISON OF FOM FOR FFT PROCESSOR, ADC PAIRS

FFT Processor	Proposed DT FFT	FFT Ring [23]	MRMDF FFT [22]
Sample Rate	1000 MSps	200 MSps	1000 MSps
Technology	0.13 um	0.25 um	0.18 um
FFT Order, N_{FFT} type	8 point complex	128 point real	128 point real
FFT Processor Power Consumption	25* mW	305 mW	175 mW
FFT Power Consump. normalized to V_{dd}=1.2V, 0.13μm 128 pt. real, 1 GSPS	77 mW	182.7 mW	56.2 mW
Dynamic Range	49 dB	35 dB	35 dB

*Processor power consumption would be 11 mW with correction of adder current mirror in layout

TABLE III
SUMMARY OF MEASUREMENT RESULTS

Process	CMOS 0.13μm
Supply Voltage	1.2 V
Size	0.203 mm^2
Total Power Consumption	25 mW @ 1 GSps
SHA Power Consumption	56μW @ 1 GSps
Serial-to-Parallel Converter Power Consumption	3.6 mW @ 1 GSps
Analog Multiplier Power Consumption	1.8 mW @ 1 GSps
Clock Divider Power Consumption	2.4 mW @ 1 GSps
Input Range	400 mV$_{pk-pk,diff}$
Output Range	400 mV$_{pk-pk,diff}$
Interleaver Ratio	1:8
EVM	2.8% @ 1 GSps
Peak SNDR	36 dB
Dynamic Range	49 dB
ENOB	8.4 bits

shown in [37] to have computational complexity proportional to $N_{\mathrm{FFT}} \log_R N_{\mathrm{FFT}}$ and that the computational complexity of a complex number processor is twice that of a real number processor. Increasing from a complex eight-point FFT to a real 128-point FFT with a radix-2 FFT SFG results in a complexity increase by a factor of $128 \log_4 128/(2 \cdot 8) \log_2(2 \cdot 8)$ or 7. Thus, the expected power consumption of a 128-point real radix-4 DT-FFT processor in 130 nm would be approximately $(11 \cdot 7)$ or 77 mW. Thus, the power consumption of the DT-FFT approach is of similar magnitude to all digital FFT processors when scaling to 128-point realizations.

Meanwhile, the dynamic range of the traditional all digital FFT processor and ADC pair is limited by the SNDR of ADC, typically limited to 35 dB, for UWB capable ADCs [2]–[5]. This was validated through simulation in [9]. Comparing the results in Table II, it can be seen that the DT-FFT approach has significantly greater dynamic range.

Table III presents a summary of the measurement results. The DT-FFT processor achieves the design goals of high operating speed, and high linearity. The full-scale signal range is 400 mV$_{pk-pk,\mathrm{diff}}$ both in and out of the processor. The area occupied by the processor is 0.2 mm^2. The EVM for BPSK coded OFDM was 2.8%. With dynamic range of 49 dB and an effective number of bits (ENOB) of 8.4.

V. CONCLUSION

This paper has presented an experimental demonstration of a DT-FFT processor as a proof-of-concept for an improved architectural approach to OFDM receivers. The processor is a good candidate for future leading data-rate UWB OFDM systems operating on multigigahertz of spectrum. The architecture performs the FFT required for OFDM demodulation in the DT domain. The measured results demonstrate that the DT-FFT processor successfully demodulates a 1-GS/s OFDM signal with a dynamic range of 49 dB, versus 35 dB with an all digital approach. This improvement in dynamic range increases receiver performance by allowing detection of weak sub-channels attenuated by multipath. The measurements also demonstrate that the processor rejects large narrowband blockers, while maintaining significant dynamic range, which improves receiver performance. Future work will focus on high-order FFTs adapting split radix SFGs to the DT implementation, bi-directionality, and efficient DT equalizer implementations.

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