## WE4D: High-speed Signal Processing Circuits for Wireless and Optical Communication Systems

Wednesday 26 May 2010

Time 15:30 - 17:10

Room: 207C

**Chair:** Koichi Murata, *NTT Photonics Labs.*

**Co-Chair:** Edward Gebara, *Georgia Institute of Technology*

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**WE4D-1** **3:30 PM**

### A 50-GS/s 5-b ADC in 0.18-um SiGe BiCMOS

*J. Lee, Y. Chen, Alcatel-Lucent, Murray Hill, United States*

A 5-b 50-GS/s ADC is presented in 0.18-um SiGe BiCMOS. The two-channel interleaved flash architecture is used to increase the conversion rate. The front-end three-stage distributed track-and-hold amplifier is devised to improve the dynamic performance. The ADC features SNDR as high as 23.1 dB with 20 GHz sine wave input at 50 GS/s conversion rate, and the third harmonic distortion is -36.5 dBc. It shows the measured resolution bandwidth of 18 GHz and the FOM of 9 pJ per conversion step with power consumption of 5.4 W.