Design of a CMOS Track-and-Hold Amplifier for a 6-bit 1-GS/s Interpolating Flash ADC

Kevin B. Geoghegan[1, 2], Perry L. Heedley[2], Thomas W. Matthews[2] and Sherif Michael[1]
[1]Department of Electrical and Computer Engineering, the Naval Postgraduate School, Monterey, CA 93943
[2]Department of Electrical and Electronic Engineering, the California State University, Sacramento, CA 95819

***Abstract*—The design of a CMOS track-and-hold amplifier (THA) for a 6-bit 1-GS/s interpolating flash ADC is presented. Since the goal of the overall project was to determine the performance of a new ADC calibration architecture, the THA was prohibited from being the limiting factor in the performance of the ADC; consequently the THA was required to have at least 56dB of signal-to-noise and distortion ratio (SNDR) at the Nyquist frequency. The THA architecture, design methodology, and supporting simulation results will be presented.**

I. INTRODUCTION

Data sampling circuits such as track-and-hold amplifiers are ubiquitous in data converter and signal processing applications. Therefore design methodologies for THAs are of interest, particularly with regard to meeting relevant specifications such as the SNDR. This THA was designed as an input sample-and-hold for a 6-bit, 1-GS/s interpolating flash ADC designed in a 0.18-µm CMOS technology. Since the objective for this ADC was to study a new calibration technique, the THA was not permitted to be a significant source of error in the overall performance of the ADC. It was therefore a requirement that the THA have a minimum SNDR of 56dB at the Nyquist frequency, accommodate the input common-mode voltage needed for the preamplifier array, achieve a minimum bandwidth of 2.2GHz while driving an expected load of 300fF, and dissipate less than 35mW.

II. TRACK AND HOLD AMPLIFIER

In order to meet these requirements, two track-and-hold amplifier architectures were considered. The first architecture was a traditional closed-loop switched-capacitor sample-and-hold amplifier (SC-SHA) and the second was an open-loop source-follower (SF) THA employing a bootstrapped NMOS switch to reduce distortion by maintaining a constant V_{GS} [4]. It was determined that in order for the SC-SHA to be a viable option, the unity-gain bandwidth of the operational amplifier needed to exceed 5.5GHz in order to compensate for the feedback factor and achieve the desired 2.2GHz closed-loop bandwidth required for complete settling of the output. In addition, a literature search produced no prior work in existence for a closed-loop SC-SHA providing better than 6-bit performance at or above 1-GS/s. For these reasons, focus was placed on the design of the pseudo-differential source-follower THA architecture shown in Figure 1 for which a number of examples exist in the literature [1-3]. Moreover, the source-followers can be implemented with significantly less circuitry.

A. Bootstrapped versus simple NMOS sampling switch.

Once the THA architecture was selected, the next step was to examine the performance of the sampling switch, S_1. To accommodate the high input common-mode voltage required by the preamplifier array, a PMOS source-follower with an active PMOS load was selected. This in turn determined the input common-mode voltage requirement for the sampling switch, given the gate-to-source bias voltage, V_{GS}, of the PMOS source-follower. V_{GS} was determined based on bandwidth considerations as discussed in the section to follow.

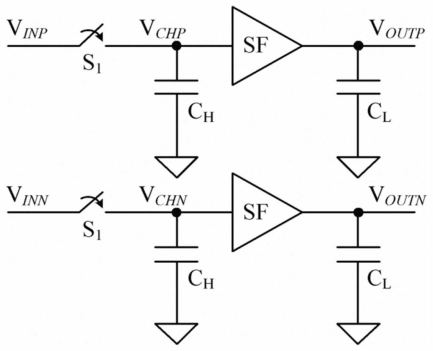

Figure 1. The Proposed THA Architecture

In the case of the bootstrapped switch, initial simulation results demonstrated its effectiveness in reducing distortion due to signal-dependent charge injection [4-5]. However, it was observed that the performance of the THA degraded at lower input common-mode voltages. This degradation may have been a consequence of the capacitance associated with S_1 rivaling that of the hold capacitor, C_H, resulting in an excessive, charge-injection induced, pedestal error on C_H at the time of switch opening. This pedestal error, in conjunction with a low input voltage, could potentially drive the drain of S_1 below the gate of S_1 by a sufficient amount leading to a significant reduction in the off resistance of the switch. The bootstrapped switch performance was then compared to the performance of a simple NMOS switch which was better suited for the relatively low input common-mode range. Ultimately, given the low input common-mode voltage requirement and the small signal swing relative to the supply voltage, $200mV_{p\text{-}p}$, it was determined through simulations that

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the bootstrapped switch was not required and that a simple NMOS switch with a charge-canceling transistor could achieve the desired specifications. The implication being that an NMOS switch with a low common-mode input voltage and small signal swing will have sufficient V_{GS} to minimize distortion due to signal-dependent charge injection. This choice of topology also eliminated the need for the non-overlapping clock generator required by the bootstrapped switch as the simple NMOS switch, shown in Figure 2, can be driven from a single clock.

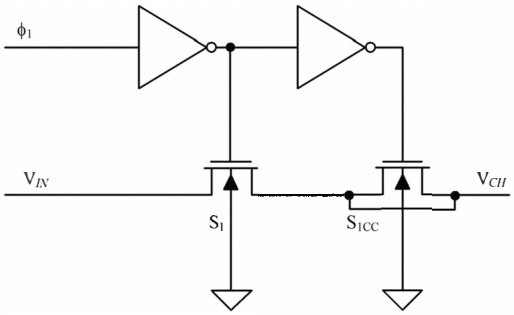

Figure 2. Proposed THA Switch Architecture.

In order to address the signal-dependent charge injection from S_1 onto the signal node, V_{CH}, when the switch opens a charge canceling transistor, S_{1CC}, was added and sized to have one-half the W/L of S_1. In employing this technique it is necessary that the falling clock edge applied to the gate of S_1 be fast enough such that the channel charge stored in S_1 splits evenly between the source and drain when S_1 is turned off [7]. When this is the case, S_{1CC} is ideally sized to compensate for the charge injection caused by S_1 onto the hold capacitor.

B. PMOS source-follower buffer.

As a consequence of the high input common-mode requirement of the preamplifier array, a PMOS source-follower with an active PMOS load represented in Figure 3 was implemented to track, hold, and buffer the input signal. S_1 is representative of the NMOS switch architecture previously described. Since the PMOS source-follower has a lower bandwidth compared to its NMOS counterpart due to the differences in carrier mobility, a significant design challenge presented itself in achieving the required minimum 2.2-GHz bandwidth needed to realize the desired 99.8% settling ($1/8^{th}$ LSB for a 6-bit ADC) at the output of the THA. Detailed analysis and design of the PMOS source-follower closely followed the examination given in [6] and was corroborated through simulation. The design emphasis was placed on selecting the optimal effective gate-source voltage, $V_{eff} = V_{SG} + V_{tp}$, and the drain-source bias current, I_{bias}, to achieve the desired frequency response (output bandwidth) given the hold capacitor C_H and effective load capacitance C_L. In order to ensure that the time-constant of the input lowpass network formed by the switch resistance, R_{IN}, of S_1 and the capacitance of C_H was not a limiting factor in the performance of the THA, R_{IN} and C_H was chosen for a minimum input bandwidth of 4.5GHz.

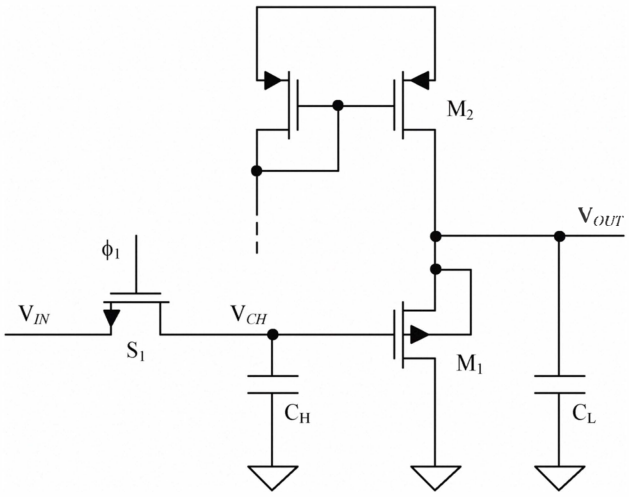

Figure 3. Simplified PMOS source-follower THA.

In order to meet the bandwidth objective of the THA, it was necessary to select an optimal value for the effective gate-source voltage, $V_{eff} = V_{SG} + V_{tp}$, of transistor M_1 that would simultaneously accommodate the desired input and output common-mode voltages with signal swing while meeting the 56-dB SNDR requirement. A transistor's unity-gain bandwidth, f_T, increases with an increasing V_{eff}. However, this increase in bandwidth comes at the expense of signal headroom for the source-follower amplifier. Taking this tradeoff into consideration, analysis determined that a V_{eff} in the range of 200 to 275mV would satisfy both the headroom and bandwidth requirements. Analysis of the source-follower amplifier was then performed to demonstrate the design objectives could be met while ensuring that the overshoot and ringing inherent in source-follower amplifiers was manageable. In [6] this was achieved by evaluating the small-signal model to develop the transfer function, *A(s)*,

$$A(s) = A(0)\frac{N(s)}{1+\frac{s}{\omega_O Q}+\frac{s^2}{\omega_O^2}}.$$

A(0) is the dc gain of the source-follower amplifier, which is approximately unity, and the numerator, *N(s)*, includes a high-frequency zero located at $\omega_Z = -g_{m1}/C_{gs1}$. Q is referred to as the quality factor, or Q-factor, and ω_0 is the pole frequency. Respectively, ω_0 and Q are represented by the equations in [6]

$$\omega_0 = \sqrt{\frac{G_{IN}(g_{m1}+G_{S1})}{C_{gs1}C_S + C'_{in}(C_{gs1}+C_S)}}$$

$$Q = \frac{\sqrt{G_{IN}(g_{m1}+G_{S1})[C_{gs1}C_S + C'_{in}(C_{gs1}+C_S)]}}{G_{IN}C_S + C'_{in}(g_{m1}+G_{S1}) + C_{gs1}G_{S1}}.$$

The parameters used in the equations for ω_0 and Q relate to the circuit shown in Figure 3 as shown in Table 1.

TABLE 1. DEFINITION OF CONDUCTANCE AND CAPACITANCE TERMS.

Parameter	Definition
g_{m1}	Transconductance of M_1
G_{tN}	Conductance of switch, S_1
C_{S1}	Capacitance of switch, S_1
G_{S1}	$G_{S1} = g_{ds1} + g_{ds2} + g_{s1}$
C_S	$C_S = C_L + C_{db2} + C_{NWell}$
C'_{in}	$C'_{in} = C_H + C_{gd1} + C_{S1}$

It is well known that for values of Q less than 0.707 the transfer function will be a maximum at dc and exhibit no peaking in the frequency response assuming $|\omega_Z|$ is much greater than ω_0 which is typically the case. In addition, if Q=0.707, ω_0 will be equal to the minus 3-dB frequency, ω_{-3dB}. In order to eliminate the body effect of M_1, the source of M_1 was tied to the N-well and therefore the contribution of the g_{s1} component to G_{S1} could be ignored. Therefore G_{S1} was assumed to be small compared to g_{m1}, and thus was neglected in the calculation of ω_0 and Q. The plot of Figure 4 is a graph of the pole frequency, f_0, and Q as a function of I_{bias} for a fixed value of V_{eff}.

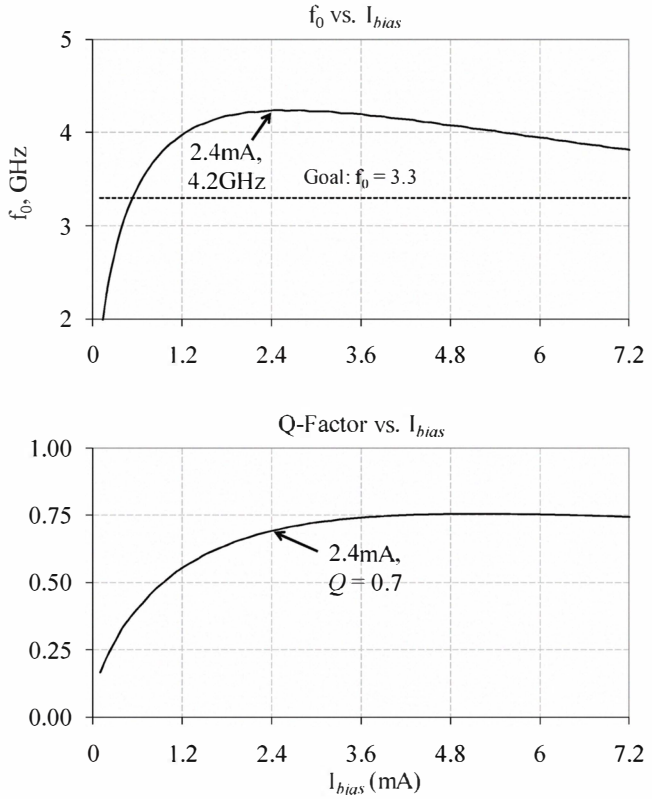

Figure 4. f_0 and Q as a function of I_{bias} for a fixed V_{eff}.

To fix V_{eff}, the I_{bias} /(W/L) relationship was held constant in the equation for V_{eff},

$$V_{eff} = \sqrt{\frac{2I_{bias}}{\mu_p C_{ox} W/L}}.$$

Based on the plots of Figure 4, the value of Q versus I_{bias}, and power dissipation constraints, a value of I_{bias} = 2.4mA was selected which resulted in a Q = 0.7, a corner frequency of $f_0 = f_{-3dB}$ = 4.2GHz, and an overall power dissipation of less than 10mW. It should be noted that I_{bias} was selected to be to the right of the peak in the f_0 vs. I_{bias} plot. This was done to avoid encountering the "cliff" to the left of the peak as process variations could push the design over the edge. Figure 5 gives the overall frequency response for $A(s)$ for the preferred values of Q and f_0.

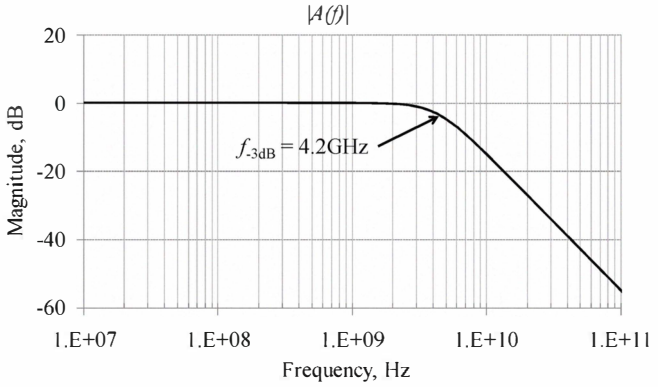

Figure 5. $|A(f)|$ for the desired values of I_{bias}, V_{eff}, and Q.

III. SIMULATION RESULTS

Based on the analysis in section II the THA was designed and then tested through simulations over process, temperature, and supply variations. The simulation test bench included estimates of package and bondwire parasitics on the signal and power supply pins. In addition, the output of the THA was loaded with the transistor-level schematics of the preamplifier array and a lumped RC network to model the interconnect parasitics between the THA and the preamplifier array. A clock model which introduced jitter was also included in the simulation test bench to introduce sample-time uncertainty. Figure 6 shows the simulated ability of the THA to track and then hold the input signal under typical conditions. All signals shown are differential in nature. The input signal to the THA is given by V(VINDIFF); V(VINCHDIFF) represents the signal taken across C_H; and, V(VOUTDIFF) represents the signal taken at the output of the THA. Figure 7 gives the FFT of the THA under the expected worst case conditions demonstrating a SNDR of 58dB with F_S = 1.25GS/s and F_{IN} just less than $F_S/2$. The spur seen at 588MHz is the third harmonic aliased back to a lower frequency.

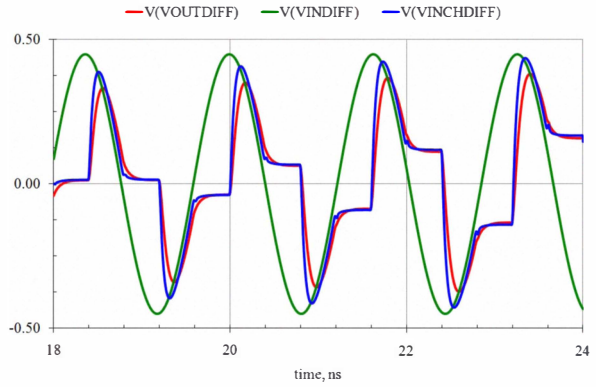

Figure 6. Simulated response of THA with F_S = 1.25GS/s.

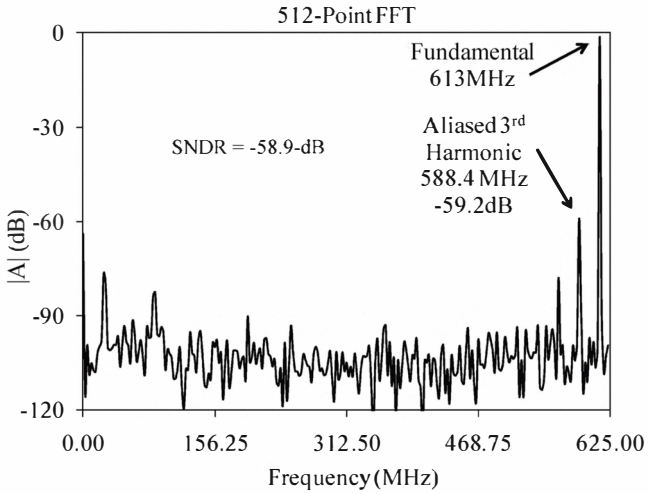

Figure 7. THA FFT with F_S = 1.25GS/s, F_{IN} = 613MHz.

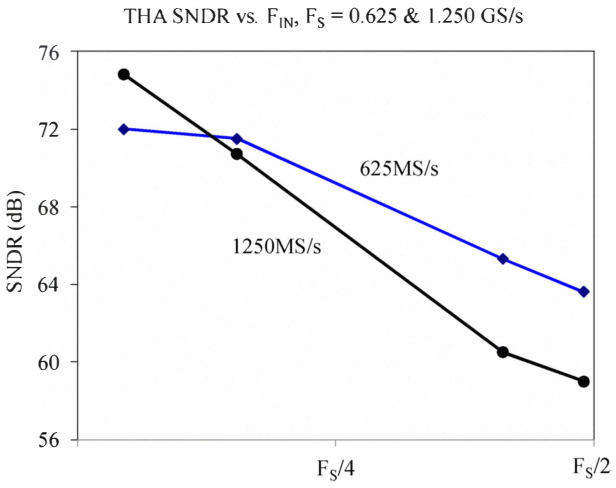

Figure 8. SNDR vs. F_{IN} for F_S of 625MS/s and 1.25GS/s.

Figure 8 demonstrates the THA SNDR performance for varying F_{IN} at F_S of 625MS/s and 1.25GS/s. Table 2 summarizes the performance of the THA simulation results at the expected worst-case process corner (slow-slow) at high temperature (85° C). The addition of the bondwire and package networks had the effect of reducing the input bandwidth and introducing overshoot into the THA response. No attempt was made to mitigate these effects as at the time of evaluation the package type and bonding options had not been chosen. In addition, the THA appeared to have no problem settling at the correct value as no discernable deterioration in the SNDR was observed. However, the importance of taking into consideration the THA's sensitivity to input loading became obvious and warrants an extension of the analysis performed in [6].

TABLE 2. SUMMARY OF THA PERFORMANCE.

Parameter	Spec	Actual	Units
Input Bandwidth	4500	4200	MHz
THA output bandwidth (minimum)	2200	2200	MHz
SNDR at Nyquist (F_S = 1.25 GS/s)	56	58	dB
Supporting accuracy (bits)	9.0	9.34	ENOB
Settling time (1/8 LSB)	450	300	ps
Power dissipation	< 35	<10	mW
Area estimate	0.025	0.015	mm^2

IV. CONCLUSION

The successful design of a track-and-hold amplifier with a minimum 58-dB SNDR for a 6-bit 1-GS/s interpolating flash ADC was presented. The key to the successful implementation involved the careful design of a PMOS source-follower with a simple NMOS switch employing charge injection cancellation. This maximized the frequency response of the overall THA architecture while mitigating the potential for overshoot and ringing in the design.

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