A Fully Integrated and Reconfigurable Architecture for Coherent Self-Testing of High Speed Analog-to-Digital Converters

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***Abstract*—This paper presents a reconfigurable architecture for coherent built-in self-testing (BIST) of high speed analog-to-digital converters (ADCs) with moderate resolutions. The proposed system is suited to be fully integrated with the ADC and, besides a low jitter clock reference, no other external high quality generators are required. The complete system comprises two synchronized phase-locked loops (PLLs), one based on a two-integrator oscillator capable of providing low distortion outputs and another based on a relaxation oscillator providing low jitter squared output, to allow coherent sampling. A detailed description of the building blocks of both PLLs is given as well as the techniques used to minimize area of the loop filters (LFs), to stabilize the output amplitude of the two-integrator oscillator to a known value, and to improve the total harmonic distortion (THD) of this oscillator. Post-layout simulations, in a 0.13 μm CMOS technology, of the proposed BIST scheme applied to a case-study 6-bit 1 GS/s ADC are shown and validate the proposed test methodology.**

***Index Terms*—Analog-to-digital converters (ADCs), built-in self-test (BIST), coherent test, phase-locked loops (PLLs).**

I. Introduction

MODERN CMOS technologies allow the design of very high speed analog-to-digital converters (ADCs) with moderate resolutions (in the range of 6 to 10 bits). Currently, a strong effort has been done to develop new circuits and new techniques to reach such high conversion rates, without investing a similar effort in the research of new and efficient testing methodologies.

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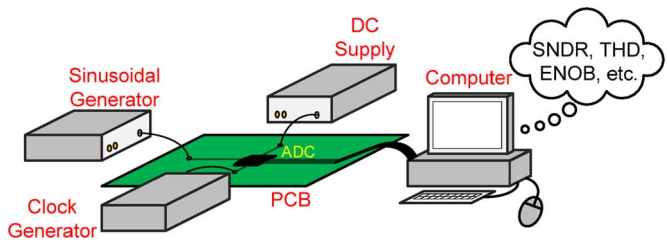

Fig. 1. General setup for ADC dynamic functional testing.

This lack of effort is clearly highlighted by the International Technology Roadmap for Semiconductors (ITRS), which states that analog and mixed-signal design-for-testability (DFT) and built-in self-testing (BIST) techniques are lagging, and more research in this area is required [1]. As a matter of fact, these researches should lead to new techniques enabling the reduction of the test instrument complexity or even the elimination of the need for external instrumentation.

Testing during mass production is very time consuming and represents a significant percentage of the total cost of an ADC [2], [3]. With sampling frequencies increasing toward the giga samples per second (GS/s) range, this cost will be critical in the near future. In conventional dynamic testing of ADCs we must provide, off-chip, an input test stimulus (usually a sine wave with enough spectral purity) and a clock signal [Fig. 1]. External signal generators with the required accuracy and bandwidth, which must exceed the device under test (DUT) specifications, are very expensive. Transformers, usually used for single-ended to differential conversion, are difficult to implement and have limited frequency range. The printed-circuit board (PCB) layout must be done with special care to avoid mismatches in path length and associated parasitics.

The above challenges can be addressed by means of a fully integrated BIST technique. Owing to the low cost and reliability of CMOS technology, it is possible to integrate on-chip efficient and cost-effective circuits specifically intended for testing. The aim of this paper is to present a fully integrated and reconfigurable architecture for dynamic functional BIST of high speed ADCs which can attenuate the current limitations and be an interesting candidate for the next generation of ultrahigh speed ADCs.

Techniques applied to ADC testing may range from purely *structural* (open box testing) to entirely *functional* (closed box testing). In the former case, the testing is more concerned in the faulty behavior of the DUT rather than in some performance

metrics. Contrasting to this, in this paper we are interested in some performance metrics of the ADC and, therefore, the functional testing is of concern. In this type of testing, two possible scenarios exist: *static* or *dynamic* testing, which basically differ in the amplitude and frequency of the input signal exciting the ADC [4]. In static testing, the input signal varies slowly with respect to the clock transitions. In dynamic testing, however, the input varies substantially from one clock cycle to the next, thus revealing the response of the ADC to rapidly changing signals. For high speed ADCs the dynamic testing produces a more useful picture of the performance, and hence, it is widely adopted.

In the current literature, several integrated schemes exist for ADC static and dynamic functional BIST. An accurate on-chip sine wave generator accompanied by a digital signal processor (DSP) for frequency-domain test of delta-sigma converters is proposed in [5], but this is not suitable for high frequency testing and leads to a large area overhead. In [6], an on-chip read-only memory is used to store the input samples and a digital-to-analog converter (DAC) followed by an amplifier and a filter converts the digital bit-stream into the analog sine wave; however, there is a large area overhead and the dynamic range is low. In static testing, several techniques have been proposed to generate on-chip a linear ramp to perform monotonicity and histogram testing of ADCs [7], [8], but the results depend largely on the accuracy of the additional components in the test circuitry. Linearity characterization of an ADC excited by noise is obtained in [9], [10], but these techniques are not applicable to ADC dynamic testing. In summary, although several schemes exist and have been proposed over the past years, none of them gained wide acceptance and/or proved to be a practical alternative to high speed moderate resolution ADC testing.

In this paper, we extend our results presented in [11] by demonstrating an attractive solution for dynamic functional testing of high speed ADCs that relies on a fully integrated, reconfigurable, and low cost architecture. The architecture is based on two phase-locked loops (PLLs) synchronized by a single and stable external reference signal which enables coherent sampling.

The organization of the paper is as follows. In Section II, the requirements for the dynamic functional testing are given and the proposed BIST architecture is presented. Section III deals with the building blocks of the architecture with especial emphasis on the voltage-controlled oscillators (VCOs). Section IV presents the BIST architecture design for a case-study application: the test of a 6-bit resolution 1 GS/s sampling rate ADC, and in Section V post-layout simulations of this design are given. Finally, Section VI draws the main conclusions.

II. Proposed ADC BIST Architecture

To evaluate the dynamic performance, e.g., signal-to-noise ratio (SNR), total harmonic distortion (THD), spurious-free dynamic range (SFDR), signal-to-noise and distortion ratio (SNDR) and the effective number-of-bits (ENOB) of an ADC, it is usually stimulated by a sine wave and the converted samples set is translated to the frequency domain by means of a DSP performing the Fourier transform. By analyzing the resulting spectral content the dynamic parameters are obtained. Sinusoidal waveforms are the preferred choice to stimulate the input of an ADC for several reasons: a) they are well defined in both time and frequency domains and approach their ideal form by proper filtering, b) their nonidealities, that is, distortion and noise, can be easily measured by means of spectral analysis, c) they provide a single frequency component that can be varied to reach half of the clock rate, thereby giving accurate information about the frequency response of the ADC, and d) the output response to a complex input waveform can be expressed as the sum of the responses to the sinusoidal components comprising that input, assuming the ADC holds the properties of a linear system [4].

The Fourier transform assumes that the waveform is continuous from $-\infty$ to $+\infty$, and an incorrect result arises if the waveform is not sampled over an integer number of periods. To solve this problem, either windowing or coherent sampling can be used. Windowing originates, among others undesired effects, spectral spreading (the energy of the main frequency component spreads to adjacent bins) and requires additional mathematical processing to derive the spectral content [12]. When possible, it is preferable to avoid windowing by employing a sampling technique known as coherent sampling, which is achieved by having [13]

$$\frac{f_{\text{in}}}{f_s} = \frac{N_p}{N_s} \tag{1}$$

where f_{in} is the sine wave input frequency, f_s is the sampling frequency, N_p is the integer number of periods from which we take samples, and N_s is the total number of samples taken. The best results are obtained if N_p is integer (so that the input waveform continuity is guaranteed) and N_s is a power of two to allow the use of the efficient fast Fourier transform (FFT) algorithm. For efficiency and to reduce test time, the ratio N_p/N_s must be irreducible so that no redundant samples are collected [13]. The total number of samples N_s must be chosen judiciously in order to obtain the actual performance of the ADC. For this purpose, it is desirable to get at least one representative sample from every ADC code. This requirement, for an ideal ADC in the absence of random noise and operating under the coherent sampling principle described above, is fulfilled by [see Appendix]

$$N_s > \pi \cdot 2^N \approx 2^{N+2} \tag{2}$$

where N is the ADC resolution in number of bits. The result in (2) is also suggested in [14].

Analyzing (1) we can see coherent sampling relies on two frequency multiplications (or divisions), which have a well-defined relationship. Two widely used frequency multiplication concepts are PLL and delay-locked loop (DLL), in which a low frequency is multiplied by a factor to result in a higher frequency. The main advantage of a DLL is that no jitter is accumulated at the output over multiple cycles of operation [15]. However, the frequency multiplication circuitry is difficulty to implement and large multiplication factors are not possible. More recently, it was shown that depending on the loop bandwidth of the PLL and the type of VCO employed this solution can even

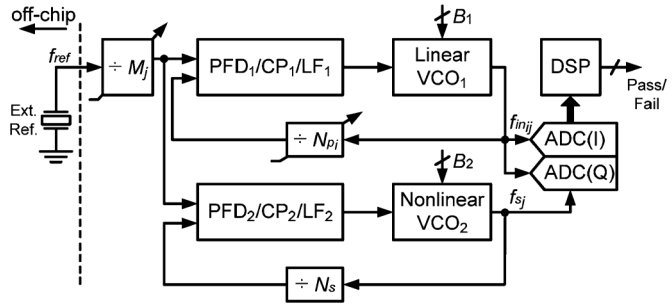

Fig. 2. Proposed architecture for coherent BIST of high speed ADCs.

TABLE I
PROGRAMMABLE PARAMETERS AND FREQUENCY MAP FOR A 6-BIT ADC (ALL FREQUENCIES ARE IN MHz / MS/s)

$f_{ref} \equiv 4$ MHz		$\hat{f}_{s_1} \equiv 250$	$\hat{f}_{s_2} \equiv 500$	$\hat{f}_{s_3} \equiv 1000$
$N \equiv 6$ bits	$N_s = 256$	$M_1 = 4$	$M_2 = 2$	$M_3 = 1$
		$f_{s_1} = 256$	$f_{s_2} = 512$	$f_{s_3} = 1024$
$\hat{f}_{in_1}/f_s \equiv 1/2$	$N_{p_1} = 127$	$f_{in_{11}} = 127$	$f_{in_{12}} = 254$	$f_{in_{13}} = 508$
$\hat{f}_{in_2}/f_s \equiv 1/4$	$N_{p_2} = 63$	$f_{in_{21}} = 63$	$f_{in_{22}} = 126$	$f_{in_{23}} = 252$
$\hat{f}_{in_3}/f_s \equiv 1/8$	$N_{p_3} = 31$	$f_{in_{31}} = 31$	$f_{in_{32}} = 62$	$f_{in_{33}} = 124$

outrun the jitter performance of a similar DLL-based implementation [16]. Based on this scenario, in this work we propose coherent self-testing of ADCs through a fully integrated architecture built around PLLs. Another interesting fact that favors the use of PLLs is the continuous and huge development/improvement being undertaken in this field, which resembles that occurring in ADCs.

The proposed BIST architecture, depicted in Fig. 2, is composed of two PLLs (PLL_1 and PLL_2) that share the same external reference signal to ensure coherent sampling. Each PLL is built with a phase/frequency detector (PFD), a charge pump (CP), a loop filter (LF), a VCO and a frequency divider. PLL_1 generates low distortion in-phase and quadrature-phase (IQ) sine wave signals and PLL_2 generates a square wave (nonlinear) clock signal, which are used to test the IQ ADCs. As we will see later, this IQ signaling is an inherent feature of the employed VCO_1, and allows the simultaneous testing of two ADCs, which are common in many communication applications. The converted N_s samples (for each ADC) are then processed by a DSP to calculate the dynamic performance parameters of the ADCs. The results are then compared with different effective resolution thresholds (for example, 6, 7, and 8 bits) up to the maximum resolution allowed by the self-testing system and, for each comparison, a pass or fail indication is shown. With this, ADCs having different resolutions are separated and also it is possible to check the performance degradation during the ADCs life time.

When the two PLLs are in lock, the input and sampling frequencies of the ADCs are, respectively

$$f_{in_{ij}} = N_{p_i} \cdot \frac{f_{\mathrm{ref}}}{M_j} \tag{3}$$

$$f_{s_j} = N_s \cdot \frac{f_{\mathrm{ref}}}{M_j} \tag{4}$$

where f_{ref} is a stable external reference frequency (e.g., produced by a crystal oscillator) and M_j and N_{p_i} $(i, j = 1, 2, \ldots)$ are programmable frequency divider values, which enable different frequencies for the input and sampling signals. From (3) and (4) we obtain (1), i.e., coherent sampling is performed.

The architecture parameters N_s, N_{p_i}, and M_j should be selected according to the resolution of the ADCs under test, the external reference frequency, the desired sampling frequencies $(\hat{f}_{s_j})$ and the desired normalized input frequencies $(\hat{f}_{in_i}/f_s)$. N_s is a power of two given by expression (2). N_{p_i} $(i = 1, 2, \ldots)$ is given by

$$N_{p_i} = \left\{ \left(\frac{\hat{f}_{in_i}}{f_s} \right) \cdot N_s \right\} \tag{5}$$

where $\{x\}$ means the nearest odd integer value of x. Note that odd integer values for N_{p_i} ensure irreducibility with respect to N_s. M_j $(j = 1, 2, \ldots)$ is given by (6), where $\langle x \rangle$ is nearest integer value of x

$$M_j = \left\langle \frac{f_{\mathrm{ref}} \cdot N_s}{\hat{f}_{s_j}} \right\rangle. \tag{6}$$

As a hypothetical example, Table I gives the architecture parameters and the resulting frequency map for a 6-bit ADC with $f_{\mathrm{ref}} = 4$ MHz, $\hat{f}_{s_j} = 250$, 500, and 1000 MS/s, and $\hat{f}_{in_i}/f_s = 1/2$, 1/4, and 1/8. We can see that the actual input and sampling frequencies are slightly different from the desired ones, but this is not a limitation and it is, in fact, required to guarantee coherent sampling.

III. BUILDING BLOCKS

A. Voltage-Controlled Oscillators

The proposed BIST architecture requires an oscillator to generate low distortion sinusoidal signals and a second one to generate a low jitter clock signal. In this subsection we present the topologies chosen for the oscillators. Since these blocks are the most critical in the proposed testing scheme, we start with a brief comparison of current oscillator topologies that are suitable to be fully integrated in CMOS technology.

Oscillators Comparison: There are a variety of oscillators topologies in the current literature and, probably, the most used in CMOS technology are listed in Table II. The *LC* oscillator is widely used mainly because of its superior phase noise performance, the best among the topologies listed. However, for a practical BIST scheme, which must be as compact as possible, this oscillator has a remarkable drawback: the large area occupied by the integrated inductors. This single reason is sufficient to discard the use of this topology. Furthermore, if special RF options are not available (e.g., several metal layers with a thick top metal), the quality factor of the inductors are reduced and the phase noise performance is somewhat worsened. Another shortcoming of *LC* oscillators is the narrow tuning range, which

TABLE II
COMPARISON OF FULLY INTEGRATED CMOS OSCILLATORS

Oscillator Topology	Phase Noise	Output Distortion	Tuning Range/Linearity	Area
LC tank	Lowest	Low	Smallest/Low	Largest
Ring	Medium	High	Large/Medium	Small
Relaxation	Medium	High	Large/Medium	Small
Two-integrator	Medium	Low [a]	Large/Medium	Small

[a] When operated in the linear regime.

would pose some restrictions when generating a variety of frequencies, as it is required by the proposed architecture. The remaining three topologies shown in Table II may be classified as RC-type oscillators, and therefore, have relatively poor phase noise performance. However, if this phase noise is still adequate for a given application, this class of oscillators offers a unique feature: they are extremely compact (occupy small silicon area) and are easily integrated in standard CMOS technologies.

Furthermore, it is well-know that the phase noise of an oscillator trades off with the power dissipation. In a BIST scheme the power dissipation is not the main concern, since all the testing circuitry can be powered-down after the test procedure. Therefore, it is possible to reduce the phase noise at the expense of higher power dissipation. Other useful properties of *RC* oscillators are wide tuning range and improved tuning linearity.

Among the *RC* oscillators presented, only the two-integrator oscillator can generate low distortion sinusoidal signals. The reason for this is that the topology can operate in linear regime [17]. Additionally, the two-integrator oscillator has inherent IQ outputs that can be used to test two ADCs concurrently and, more important, be used in an efficient automatic amplitude control (AAC) loop that stabilizes the oscillator amplitude to a reference (well-known) value after start-up [18], [19]. For these reasons, we choose the two-integrator oscillator topology to generate spectral purity sine waves in PLL_1. A more detailed discussion regarding this oscillator will be given later within this subsection.

The implementation simplicity of ring and relaxation oscillators makes them the preferred choice to generate the clock signal. In [20] it is shown that practical ring oscillators have a slightly better phase noise performance than practical relaxation oscillators for a given power dissipation. Despite this known advantage, the relaxation oscillator is adopted here because, in addition to a "square" wave, this oscillator produces a "triangular" waveform which can also be used to calibrate timing errors either in IQ or in time-interleaved ADCs (however, this aim is out the scope of this paper and is currently being investigated). Moreover, as previously mentioned, the phase noise can be improved by increasing the dissipated power in the oscillator. In the next paragraphs we discuss the relaxation oscillator in more details.

Relaxation Oscillator (VCO_2)*:* The schematic of the voltage-controlled relaxation oscillator is shown in Fig. 3. The oscillator is composed of a floating timing capacitor, C, connected to a nonlinear structure that behaves like a Schmitt trigger. This nonlinear structure is formed by two current sources I_t, obtained through M_{2a} and M_{2b}, a cross-coupled pair of transistors, M_{3a} and M_{3b}, which steers the currents I_t

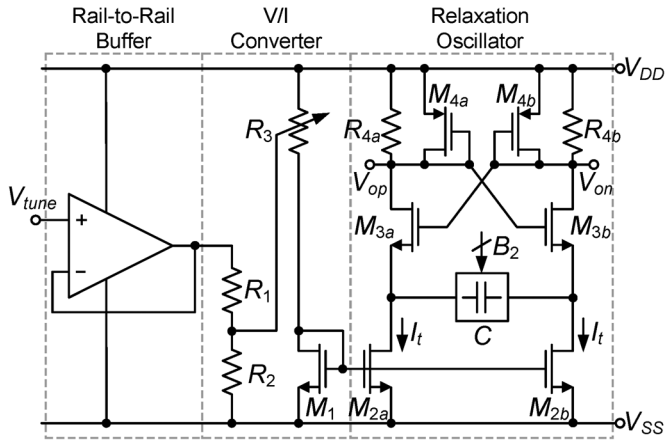

Fig. 3. Simplified schematic of the relaxation oscillator (VCO_2).

between the two branches, two load resistors, R_{4a} and R_{4b}, and two diode-connected devices, M_{4a} and M_{4b}, which clamp the output nodes and create a strong I_t versus oscillation frequency dependence.

The oscillation frequency is given approximately by [21]

$$f_{osc} \approx \frac{I_t}{4 \cdot C \cdot V_c} \tag{7}$$

where V_c is the amplitude of the voltage swing across the floating timing capacitor. In most practical cases, this oscillator is tuned by changing C and/or I_t. Here, in order to widen the tuning range without excessively increase the VCO gain, K_{VCO}, we use a combination of discrete and continuous tuning modes [22]. A switched-capacitor (SC) array controlled by B_2 bits selects a given tuning characteristic, and continuous variations within this characteristic are obtained changing the magnitude of the current sources I_t. The continuous tuning is performed in the current domain because in this way it is possible to achieve wider tuning range and better tuning linearity. In fact, current advanced CMOS technologies do not offer high quality varactors [22].

The output of the loop filter in both PLLs is a voltage, hence a voltage-to-current (V/I) converter is needed to convert this voltage into the tuning currents I_t. Additionally, in a low voltage environment it is important to use the entire voltage swing available by the charge pumps ($V_{\mathrm{DD}} - V_{\mathrm{SS}} - 2|V_{DSsat}|$, where V_{DSsat} is the drain-to-source saturation voltage, see Fig. 5) to further minimize the K_{VCO}, thus an input rail-to-rail buffer is required. This buffer in conjunction with resistors R_1 and R_2 adjust the controlling voltage of R_3 to be in the desired range needed for implementing this variable resistor with active pMOS devices.

Two-Integrator Oscillator (VCO_1)*:* The schematic of the voltage-controlled two-integrator oscillator is depicted in Fig. 4. The two integrators are realized by two differential pairs, transistors $M_{4a} - M_{4d}$, and two capacitors, C_a and C_b. Two additional differential pairs, comprising transistors $M_{5a} - M_{5d}$, with the outputs cross-coupled to the inputs, implement negative resistances to compensate the losses due to resistors $R_{4a} - R_{4d}$ and make sustainable oscillation possible. These additional pairs are also used for amplitude control of the output signals.

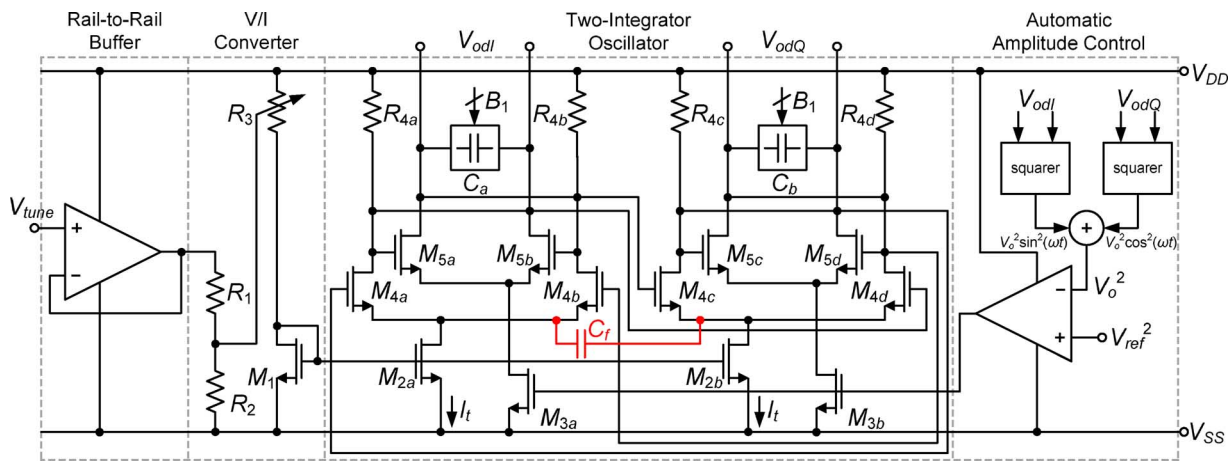

Fig. 4. Simplified schematic of the two-integrator oscillator (VCO_1).

As mentioned earlier, this control is extremely important in this application for two reasons: a) it allows the oscillator to operate in the linear regime resulting in low distortion output sinusoidal signals, and b) it stabilizes the output amplitude to a known set value, which is of particular interest when testing ADCs (note this value can be matched to the ADC reference voltage). The AAC operates as follows [18]. The two-integrator oscillator inherently produces IQ output signals that may be expressed as

$$V_{odI} = V_o \sin(\omega \cdot t) \tag{8}$$

and

$$V_{odQ} = V_o \cos(\omega \cdot t) \tag{9}$$

where it is assumed the signals have the same amplitude V_o for simplicity. If these signals pass through squarer circuits and are summed up, from Pythagoras' law follows that

$$V_o^2 \sin^2(\omega \cdot t) + V_o^2 \cos^2(\omega \cdot t) = V_o^2. \tag{10}$$

This squared output amplitude can now be compared with a reference voltage V_{ref}, also squared, and the result applied to the cross-coupled differential pairs through transistors $M_{3a} - M_{3b}$. These differential pairs will act forcing the output amplitude to approach V_{ref}. If V_{ref} is not excessively high, the oscillator operates in the linear regime.

In linear operation, the oscillation frequency is given approximately by [17]

$$f_{osc} \approx \frac{g_{m4}}{2 \cdot \pi \cdot C} \tag{11}$$

where g_{m4} is the transconductance of each integrator's differential pair and $C = C_a = C_b$. The transconductance g_{m4} can be varied by means of the currents I_t. For the same reasons discussed for the relation oscillator, we combine both discrete and continuous tuning. The discrete tuning is performed by two SC arrays comprising C_a and C_b and controlled by B_1 bits. On the other hand, the continuous tuning is realized by the currents I_t which are produced by the V/I converter also shown in Fig. 4.

To further reduce the output distortion of the two-integrator oscillator, an extra capacitor C_f can be placed between the drains of transistors M_{2a} and M_{2b}, as shown in Fig. 4. According to simulations, this capacitor attenuates the amplitude of the dominant second harmonic present on these nodes by a low-pass filtering action. This causes the oscillator operation to be more linear and, consequently, the output distortion is improved. A somewhat related technique intended for phase noise reduction rather than for output distortion improvement is proposed in [23].

B. Charge Pump and Loop Filter

The charge pump and loop filter used in both PLLs is shown in Fig. 5. In order to reduce the total capacitance of the integrated loop filter, which is desirable to reduce its area overhead, a capacitance multiplication scheme as proposed in [24] is used. This scheme uses a main charge pump connected to the resistor side of the loop filter as in a conventional design. In addition, an auxiliary charge pump with a smaller current ($\beta < 1$) is connected to the node between resistor R_1 and capacitor C_1. The "up" and "down" switching signals of the two charge pumps are arranged in such a way that, when the main charge pump is sourcing current, the auxiliary one is sinking, and vice versa. With this arrangement, the entire current of the main charge pump flows through the resistor, whereas the current difference of the two charge pumps flows into the capacitor [24]. For example, if we choose $\beta = 0.8$, the capacitance value of C_1 is only 20% of the same capacitor in the conventional approach.

The loop filter used has a third-order transfer function, with three poles and one zero, given by

$$\frac{V_{\mathrm{out}}}{I_{cp}} = \frac{1+sR_1C_1}{s(C_1+C_2+C_3)} \times \frac{1}{\left[1+s\frac{R_1C_1(C_2+C_3)+R_2C_3(C_1+C_2)}{C_1+C_2+C_3} + s^2\frac{R_1R_2C_1C_2C_3}{C_1+C_2+C_3}\right]}. \tag{12}$$

This loop filter better attenuates the effects of charge pump imbalance than the second-order loop filter obtained by removing R_2 and C_3, and, if properly designed, it affects the loop bandwidth and phase margin negligibly. This enhanced attenuation

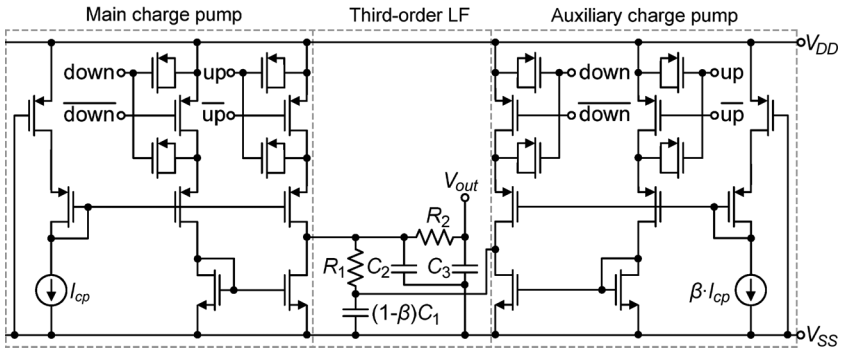

Fig. 5. Schematic of the charge pump and third-order loop filter.

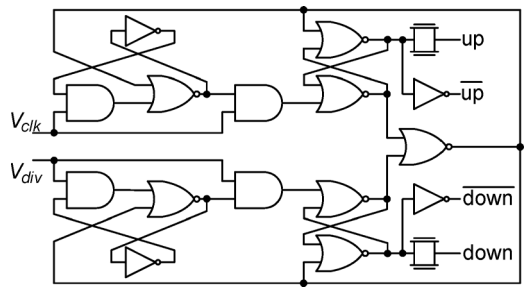

Fig. 6. Schematic of the phase and frequency detector.

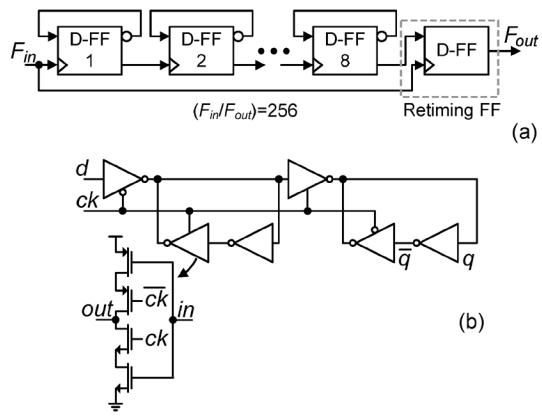

Fig. 7. Schematic of the fixed divider (a) and D flip-flop (b).

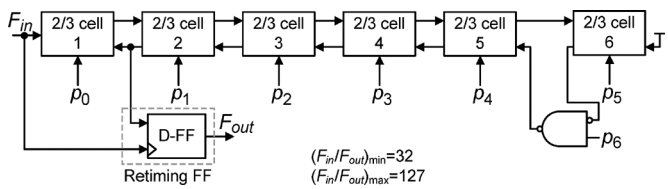

Fig. 8. Schematic of the programmable divider.

improves the jitter performance and suppresses spur tones at the output of the PLL.

The auxiliary charge pump is a scaled version of the main charge pump. The circuitry of these charge pumps is similar to the one proposed in [25], except that here we use two pMOS and one nMOS current mirrors. Through simulations, it is possible to observe that this solution has a slightly better up and down currents matching. The switches include dummy devices to cancel out the charge injection.

C. Phase and Frequency Detector

The schematic of the sequential three-state PFD used in this work is shown in Fig. 6 [26]. The circuit is based on a dual D-type flip-flop (D-FF) structure and uses an asynchronous race-free design. Compared to the conventional NAND-based design, this PFD minimizes the perturbation in the loop filter voltage by reducing the simultaneous activation of the "up" and "down" signals during the steady state operation of the PLL. As a result, the jitter performance of the PLL is improved.

D. Dividers

In the proposed BIST architecture it is needed two programmable dividers and one fixed divider [see Fig. 2]. The fixed divider simply implements a division by a power of two (N_s), hence it can be implemented simply by cascading divide-by-two D-FF stages. In Fig. 7(a) such a divider topology is shown for a division ratio of 256, which can be used when testing 6-bit ADCs. A well-known problem associated with asynchronous dividers is jitter accumulation as the input signal pass through the dividing stages. To remedy this undesirable effect, a retiming D-FF is often used. With this practice the only jitter source of the divider is the retiming D-FF.

Fig. 7(b) shows the schematic of the D-FF used. It is based on two static latches formed by standard CMOS inverters and clocked inverters. Due to the relative low switching frequencies used in this application, dynamic latches, although smaller, are not suited.

The two programmable dividers are based on a modular structure consisting of a chain of 2/3 divider cells connected like a ripple counter [27]. In Fig. 8 an example is shown for a divider, programmed through the binary word $p_0, p_1, \ldots, p_6$, having division ratios in the range of 32 to 127. This design avoids the presence of long delay loops (each cell interacts adjacently only), and facilitates the layout work because cells are identical. Each 2/3 divider cell is built using four D-FFs and three AND gates [27].

In some cases, as the one presented in Table I, the division by M_j can be straightforwardly implemented as a cascade of divide-by-two D-FF stages followed by a multiplexer.

IV. Architecture Design

As a proof of concept, the proposed BIST scheme was designed targeting a 6-bit 1 GS/s ADC. In this particular application, we have adopted the following architecture parameters: $f_{\rm ref} = 4$ MHz, $N_s = 256$, $N_{p_{1,2}} = \{63, 127\}$, and $M_{1,2} = \{1, 2\}$. As a result, the possible clock frequencies are 512 and 1,024 MHz, and the input frequencies are 126, 252, 254, and 508 MHz. In order to accommodate the clock frequencies, the relaxation oscillator is designed with two discrete tuning characteristics selected according to the division ratio state of programmable divider M_j. Likewise, the input frequencies are accommodated in the two-integrator oscillator with three discrete tuning characteristics, which are selected considering the division ratio states of dividers N_{p_i} and M_j.

The main and auxiliary charge pump currents used are 50 and 40 μA, respectively, leading to $\beta = 80\%$. Using these current magnitudes, the total capacitance of the two LFs is around 110 pF. If on one hand the BIST architecture area is strongly dependent on the LFs area, on the other hand the power dissipation is mainly imposed by the VCOs. The total average power dissipation of the BIST architecture operating at the highest speed is about 26 mW from a 1.2 V supply, of which $\rm VCO_1$ and $\rm VCO_2$ dissipate 14.7 mW and 6.8 mW, respectively. Both PLLs are designed with a loop bandwidth of 200 kHz. All blocks are designed in a standard 0.13 μm 1.2 V CMOS technology ($L_{min} = 0.12$ μm) without any special options (e.g., low- or high-threshold voltage MOS devices).

The layout of the BIST architecture, excluding the DSP, is illustrated in Fig. 9 and occupies a total area of 0.033 mm^2. In a wide range of applications, where DSP resources are already available on-chip, this represents the additional area required by the proposed BIST solution. In this case, the DSP resources are reused (e.g., during the power-on of the system) for testing, and freed after that for normal operations. In other demanding applications, where the requirements on the ADC clock are tight, a PLL is often employed to produce a precise clock. In this situation, the PLL used for clock generation could play the role of our $\rm PLL_2$. Briefly, depending on the application, the BIST architecture proposed here may demand only a single PLL, that responsible for generating the input signal of the ADCs ($\rm PLL_1$), or, in the other extreme, demand two PLLs and a dedicated DSP for digital post-processing.

During the layout phase, some critical issues were identified and are given as guidelines in the following: a) the layout of the two oscillators should be as symmetrical as possible, especially that of the two-integrator oscillator, since any asymmetries raise the even harmonics considerably; b) in the LFs, MOS capacitors should be used to reduce the area, since these devices offer the highest effective capacitance per unit area. However, in finer technologies (especially beyond the 0.13 μm node) the gate leakage current should be considered carefully in advance, since it may make part of the charge pumps' currents useless and change the LF behavior; c) the layout of the two D-FFs forming the PFD should be perfectly matched; and d) since we used minimum transistor sizes in the digital circuits to reduce both peak and average currents, the interface signals of these circuits should be appropriately buffered to overcome any parasitic loading.

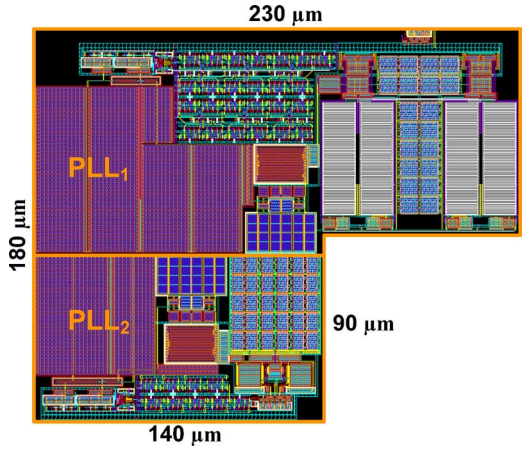

Fig. 9. Layout of the BIST architecture, excluding the DSP, occupying a total area of 0.033 mm^2.

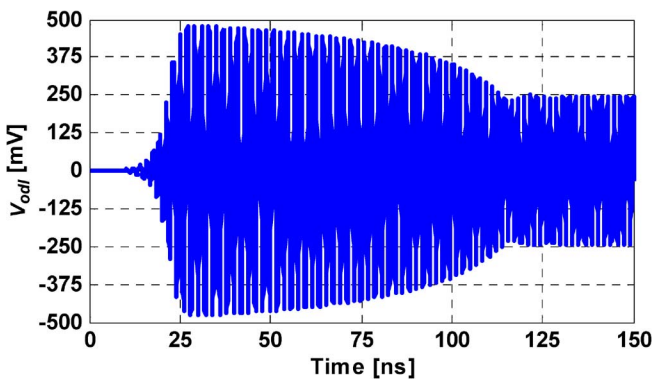

Fig. 10. Start-up of the two-integrator oscillator showing the AAC response.

V. Post-Layout Simulations

In this section post-layout simulations of the designed BIST architecture, given in the previous section, are presented, followed by a table comparing the proposed approach with other solutions available in the open literature.

A. Automatic Amplitude Control Response of the Two-Integrator Oscillator

The start-up of the two-integrator oscillator is shown in Fig. 10, where it is possible to observe the AAC response. With $V_{\rm ref}^2$ set to $(250\ {\rm mV})^2$, the AAC loop stabilizes the differential output amplitudes, V_{odI} and V_{odQ}, to approximately 250 mV within 125 ns.

In Fig. 11 the output amplitude of the two-integrator oscillator is plotted versus the oscillation frequencies of the higher discrete tuning characteristic, the one that encompasses the input frequency of 508 MHz and ranges from 460 to 560 MHz. For the other two tuning characteristics, the simulated performance is similar. It is worthwhile to note that, due to the AAC loop, the amplitude varies less than approximately 1 mV within the entire frequency range.

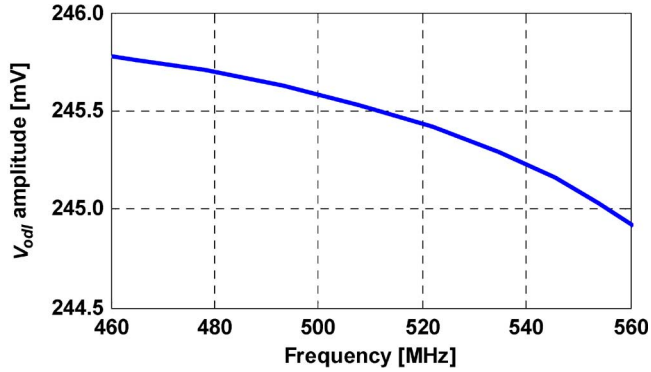

Fig. 11. Output amplitude of the two-integrator oscillator versus frequencies within the higher discrete tuning characteristic.

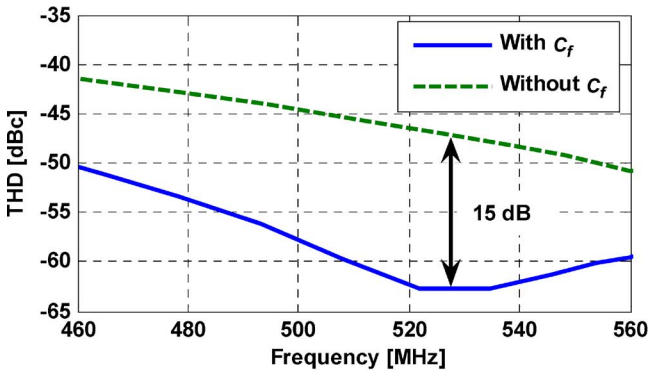

Fig. 12. THD at the output of the two-integrator oscillator with and without filtering scheme versus frequencies within the higher discrete tuning characteristic.

B. Output Distortion of the Two-Integrator Oscillator

One of the important requirements of the two-integrator oscillator, VCO_1, is high linearity. The THD of this oscillator with and without the proposed filtering scheme (capacitor C_f) is illustrated in Fig. 12. The distortion is mainly caused by third and fifth harmonics, since the oscillator has differential outputs and its layout is carefully made symmetrical. Considering a reasonable output voltage swing of 500 mV peak-to-peak differential and no filtering, the THD hardly exceeds -50 dB, which is the maximum allowed distortion when testing a 6-bit ADC. (For safe margin purposes, we are considering that the THD is 2-bit better than the ideal SNR for this ADC, i.e., $-6.02 \cdot (6+2) - 1.76 \approx -50$ dB.) Employing the proposed filtering scheme, $C_f = 5\,\mathrm{pF}$, the THD improves substantially reaching a maximum enhancement of 15 dB. The resulting distortion level is adequate for the intended application.

C. Phase Noise and Output Jitter of PLL_2

The phase noise of the relaxation oscillator free-running at 1,024 MHz is shown in Fig. 13 together with the corresponding phase noise when it is inserted in the PLL. Up to the PLL bandwidth, approximately 200 kHz, the oscillator phase noise is attenuated significantly, and, at higher frequency offsets, the phase noise is mainly imposed by the oscillator. The resulting rms jitter integrated above 4 MHz is only 1.3 ps, which is about three times smaller than the maximum tolerable value (≈4 ps)

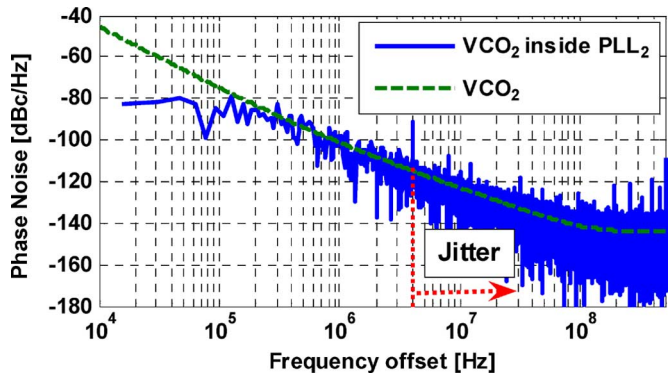

Fig. 13. Phase noise of the relaxation oscillator running in open loop (dashed line) and inside PLL_2 (continuous line) with frequency of 1,024 MHz.

to accurately test 6-bit ADCs with input frequencies up to 508 MHz. The lower integration limit used (4 MHz) is set by the inverse of the observation time, i.e., f_s/N_s (1,024 MHz/256). This observation time corresponds to the duration interval needed to collect N_s samples with a sampling rate f_s. Note that close-in phase noise fluctuations with frequency offsets lower than f_s/N_s will affect the clock signal transitions only negligibly within the observation time.

In all PLL-related simulations reported in this work, we are assuming that the external reference clock has a sufficiently low phase noise profile, which, for the intended application, may be easily obtained by a crystal oscillator. Actually, the phase noise of the reference clock will raise the phase noise of the PLL mainly at frequency offsets up to the PLL bandwidth. At higher frequency offsets, the phase noise contribution of the reference clock will be attenuated by the PLL.

D. Output Spectrum

Fig. 14(a) shows the spectrum at the output of an ideal 6-bit ADC stimulated by sampling and input frequencies of 1,024 MS/s and 508 MHz, respectively, when the two PLLs are in lock state. This spectral content is obtained by applying FFT over 1,024 consecutive digitized samples (we used more samples than the minimum 256 to become the spectrum easily readable). In Fig. 14(b) a similar spectrum is depicted, however for an input frequency of 252 MHz. The ENOB of both spectrums approach the theoretical value of 6 bits indicating that the noise and the distortion of the BIST scheme are at acceptable levels. The SNRs of both simulations are around 37 dB, mainly limited by the quantization noise. The SFDRs are 49.7 and 48.3 dB for the input frequencies of 508 and 252 MHz, respectively, and they are limited by the reference spurs. It is noticeable from the spectrums of Fig. 14 that coherent sampling is occurring.

A fair comparison of the proposed BIST architecture with others approaches is not straightforward, mainly for the following reasons: a) most of the works for dynamic functional BIST of ADCs do not deal with the clock generation, i.e., they only address the analog input generation, and b) BIST requirements are strongly dependent on the application and on the specifications of the ADC under test, which vary considerably. Nonetheless, attempting to confront the performance metrics

TABLE III
PERFORMANCE SUMMARY AND COMPARISON WITH PRIOR WORKS

		This Work	[6]†	[28]†	[29]†
Technology	[µm]	0.13	0.13	0.13	0.8
Area	[mm^2]	0.033	0.51‡	0.186	0.833
Power	[mW]	26.0	39.5	4.04	36.5
Supply Voltage	[V]	1.2	1.4	1.2	N/A
ADC Input Voltage	[mV_{pp}]	500	149	228	N/A
ADC Input Frequency	[MHz]	508	312	10	40
SFDR	[dB]	49.7	25.3	74.1	65.4§
ADC Clock Frequency	[MHz]	1,024	N/A	N/A	N/A
ADC Clock Jitter (RMS)	[ps]	1.3	N/A	N/A	N/A

†This work does not deal with the clock signal generation.
‡Area of the read-only memory not included.
§ SFDR measured at 1 MHz frequency.

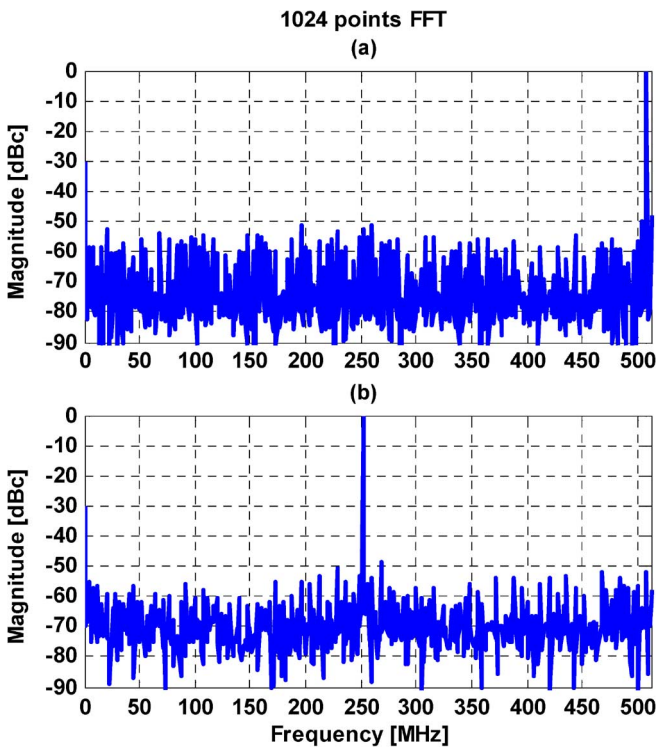

Fig. 14. Output spectrum of an ideal 6-bit ADC stimulated by the two PLLs in lock state. The sampling frequency is 1,024 MS/s and the input frequencies are 508 MHz (a) and 252 MHz (b).

obtained in this work with previous efforts, Table III is given. From this table it is possible to observe that in terms of area, the proposed BIST architecture has a remarkable advantage, even including the area of the PLL responsible for the clock generation. This feature is useful for any BIST method, since it is highly desirable to reduce the area of the BIST circuitry with respect to the DUT. In terms of power dissipation, the proposed approach is comparable to most of the other works. In [28] merely 4.04 mW are dissipated, however the focus of this work is to improve the THD of the input signal for testing a 10-bit ADC at a relatively low frequency (10 MHz).

Regarding the magnitude, frequency, and accuracy (distortion) of the input signal, it is noticeable the challenge of increasing the frequency while maintaining the same magnitude and distortion. For example, in [6] a high frequency (312 MHz) is achieved, but the SFDR is only 25.3 dB and the input voltage magnitude is 149 $\mathrm{mV_{pp}}$. In [28], [29] low distortion signals are achieved, but the frequencies are limited to tens of MHz. In the proposed BIST architecture, higher frequencies and larger magnitudes can be generated without deteriorating the distortion severely.

VI. CONCLUSION

We presented a fully integrated, low cost, and reconfigurable architecture for coherent self-testing of high speed and moderate resolution ADCs. Two synchronized PLLs, one for ADC input signal and other for the clock signal, are used to allow coherent sampling. Techniques to reduce the LFs area, to stabilize the outputs of $\mathrm{VCO_1}$ to a known set value, and to reduce the output distortion of the two-integrator oscillator are presented. A simple filtering capacitor applied to the two-integrator oscillator enhances the THD up to 15 dB. A case-study application, the dynamic functional testing of a 6-bit 1 GS/s ADC, is used as vehicle to highlight the properties of the proposed BIST solution, and post-layout simulations of the architecture, in a 0.13 μm CMOS technology, validate and show the usefulness of the proposed test methodology.

APPENDIX

This appendix derives the minimum number of samples that must be collected in order to get, at least, one representative sample from every ADC code when the converter is sampling an ideal full-scale sinusoidal. In the derivation that follows we consider the following assumptions: a) the ADC has an ideal transfer characteristic, b) no random noise sources are present,

and c) the ADC is working under coherent sampling with irreducible N_p/N_s. With this we can write the input sinusoidal as

$$V_{\rm in}(t) = \frac{V_{FS}}{2}\sin\left(2\pi\frac{N_p\cdot f_s}{N_s}t\right). \tag{13}$$

By sampling this sinusoidal waveform at a given rate f_s, the worst case situation occurs when the waveform assumes the highest frequency in the Nyquist band, which happens when $N_p = N_s/2 - 1$. If N_s is a power of two the N_p/N_s irreducibility is preserved. Applying this in (13), we obtain

$$V_{\rm in}(t) = \frac{V_{FS}}{2}\sin\left(\pi\cdot f_s\cdot t - \frac{2\pi\cdot f_s\cdot t}{N_s}\right). \tag{14}$$

Using the trigonometric identity $\sin(\alpha-\beta) = \sin(\alpha)\cos(\beta) - \sin(\beta)\cos(\alpha)$ and $t = n/f_s$ for $n = 0, 1, 2, \ldots$, (14) can be written as

$$V_{\rm in}[n] = -\frac{V_{FS}}{2}\cos(\pi\cdot n)\sin\left(\frac{2\pi\cdot n}{N_s}\right). \tag{15}$$

Since $\cos(\pi\cdot n) = (-1)^n$, the maximum absolute sample-to-sample variation near the zero-crossing of (15) is

$$|\Delta V_{\rm in}|_{\max} = \frac{\pi\cdot V_{FS}}{N_s}. \tag{16}$$

This variation must be less than the least-significant bit (LSB) voltage, $V_{LSB} = V_{FS}/2^N$, in order to get at least one representative sample in the midrange coding of the ADC, which is the critical situation (the samples per code increase as the codes approach the end points of ADC transfer characteristic, resembling a "bathtub" shape). Therefore, we obtain

$$\frac{\pi\cdot V_{FS}}{N_s} < \frac{V_{FS}}{2^N} \tag{17}$$

and, finally

$$N_s > \pi\cdot 2^N \approx 2^{N+2}. \tag{18}$$

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