A 5-Bit 10GS/s 65nm Flash ADC with Feedthrough Cancellation Track-and-Hold Circuit

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***Abstract*— A 10GSamples/second (GS/s) 5-b flash analog-to-digital converter (ADC) that includes a feedthrough cancellation track and hold amplifier (THA) is presented. The proposed 10GS/s switched source follower (SSF) THA removes the input feedthrough error during the hold mode, which dramatically improves the settling behavior than previous designs. The proposed track and hold circuit achieves a total harmonic distortion (THD) of -37.3dBc at 10GS/s and an input frequency of 4GHz, which is 4.5dBc lower than the THD of traditional SSF THAs. The THA core only consumes 26mW and this is the minimum power consumption of THA above 10GS/s ever reported. In addition, a proposed comparator array to address the overdrive recovery issue is implemented for very high speed ADC. A reference ladder with source followers is applied to reduce the pre-amplifier feedthrough distortion by 10 times. This design is implemented in IBM 65nm CMOS technology with 1.4V power supply, 1.2V peak-to-peak differential input amplitude, and 1V peak-to-peak clock swing.**

I. Introduction

A new trend towards high-speed circuit design is to replace binary front-ends with analog-to-digital converters (ADCs) in backplane-based computer and communications systems. Analog front-end blocks, such as mixers and filters are gradually replaced by high speed ADCs and digital signal processing (DSP) circuits. By moving high-speed ADCs closer to the antenna, more DSP functionalities can be included afterwards and therefore increasing the system robustness, scalability, and flexibility [1]–[3].

With CMOS feature sizes scaling down to nanometer dimension and cutoff frequencies exceeding 200GHz, MOSFETs have become a promising candidate for high speed ADCs beyond 10Gb/s. The fastest CMOS flash ADC reported is a 3.5GS/s 5-b Flash ADC in 90nm CMOS [4]. However, the design used a pair of inductors which takes up large area.

In this paper, we present a 10GS/s 5-bit flash ADC prototype implemented in IBM 65 nm CMOS technology with a 4GHz instantaneous input bandwidth. We proposed a new switched source follower (SSF) track and hold amplifier (THA) with feedthrough cancellation that dramatically improves the settling behavior of the THA and achieves a better harmonic distortion performance. Moreover a new comparator array is designed that can be applied to applications with sampling rates beyond 10GS/s. This flash ADC consists of an array of 31 differential preamplifiers with 6 dummy ones sitting at each side and averaging resistive networks are used to lower the impact of FET mismatch and consequently improve the differential nonlinearity (DNL) performance [5].

The paper is organized as follows. The proposed SSF THA is presented and analyzed in Section II. Section III discusses the comparator array. The ADC architecture is shown and design tradeoff is analyzed in details in Section IV. Simulation result is discussed in Section V. Finally, Section VI is the conclusion.

II. Track and Hold Amplifier

THAs are an integral part of most high-performance ADCs, especially for ultra-high-speed design. It is challenging to generate a low jitter, low skew, and high swing clock signals for ultra-high-speed ADCs because jitters are already comparable to the clock period. An ADC without THAs often has limited signal to noise-plus-distortion ratio (SNDR) due to comparably large clock jitters. Therefore, THA is becoming the essential part in ultra-high-speed ADC design.

In general, a THA can either adopt a close loop or an open loop architecture. The close loop architecture can achieve a higher resolution due to its bottom-plate sampling technique. However, it suffers from a relatively low sampling frequency. The open loop architecture is a better choice for high speed ADC design. The switched series transistor approach and the switched source follower approach are two main choices in the open loop architecture. The switched series transistor architecture needs voltage boost to eliminate the nonlinearity, which is impossible for a speed range of 10GS/s. Thus, the switched source follower approach becomes our final choice.

The schematic diagram of traditional switched source follower THA is shown in Fig. 1 [6]. As shown in Fig. 1, the THA includes a differential input, two pairs of control switches, and an output follower. In the track mode when Track signal is high. M_7 and M_{10} are turned on to pull the source voltage of M_{sf} low. The M_{sf} pair are source followers and the output follows exactly the differential input signal. In the hold mode when Hold signal is high, the tail current I_1 flows through the differential pair R to pull the gate voltage of M_{sf} low. The resistance of R is chosen such that the voltage drop along R can sufficiently turn off the transistor pair M_{sf}. Then the differential capacitors hold the sampled value until the next clock.

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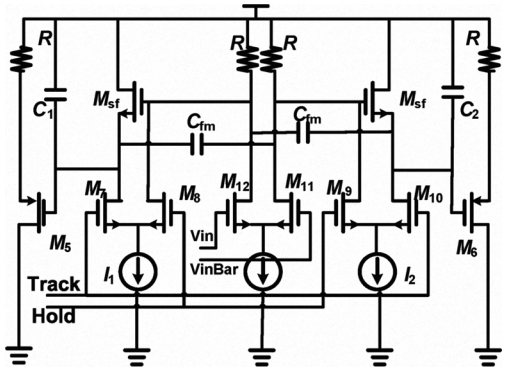


Fig. 1. Traditional switched series follower THA.

However, this architecture suffers from two serious artifacts. The first one is the decay of the output signal as energy is lost from the storage element (usually a capacitor) within the track and hold circuit. However, this droop problem is usually not a challenge for CMOS amplifiers with infinite DC input impedance. The second important artifact is the feedthrough in the hold mode. Input signals can still change the held values at the output nodes through the parasitic gate-source overlap capacitor C_{gso}. As a consequence, the output signals of the M_{sf} pair in Fig. 1, which are supposed to keep the sampled data, may have significant shift due to this feedthrough. Previously a fixed capacitance C_{fm} whose value is equal to C_{gso} of M_{sf} is used to match and then cancel this feedthrough [6]. The capacitance C_{gso} of M_{sf} is voltage independent. During the track mode, M_{sf} is on and the gate source capacitance C_{gs} of M_{sf} consists of the gate-channel-source capacitance C_{gcs} and the gate overlap capacitance C_{gso}. During the hold mode, the M_{sf} pair is off and C_{gs} is only the overlap capacitance C_{gso} in M_{sf}. Because C_{gso} is process dependent, a constant capacitor cannot perfectly match its value.

Therefore, we propose a new technique to cancel the hold mode feedthrough effect as shown in Fig. 2. As mentioned earlier, when THA works in the hold mode, M_{sf} is off. The feedthrough capacitor becomes the gate-source overlap capacitance C_{gso}. The output still changes because the charge goes through the overlap capacitance C_{gso}. Thus, we can use an off state transistor to perfectly match the feedthrough capacitor. As Shown in Fig. 2, M_3 and M_4 are off state transistor and their source voltage will follow drain voltage through M_3 and M_4's overlap capacitor C_{gso}. Therefore, if we can subtract M_3 and M_4's source voltage from THA output and the feedthrough impact can be theoretically removed from the THA output.

The outputs of THA with and without feedthrough cancellation circuit are compared in Fig. 3. As shown in Fig. 3(a), when a traditional SSF THA works in the hold mode, the held voltage is not constant and it still follows the input signal through the parasitic capacitor between the input and output nodes. In our proposed SSF THA shown in Fig. 3(b), the output voltage keeps constant during the hold mode due to the feedthrough cancellation.

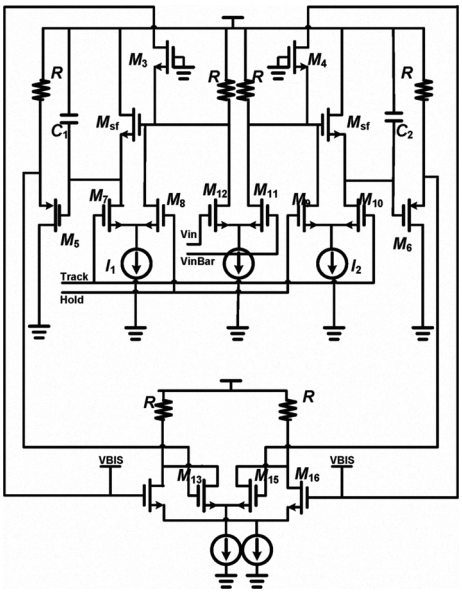
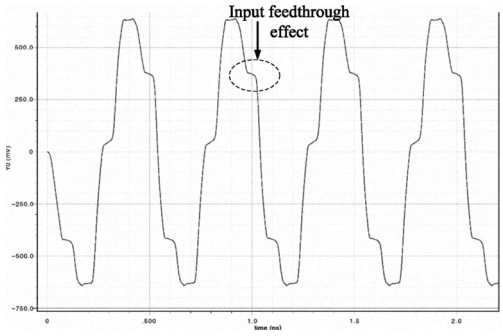
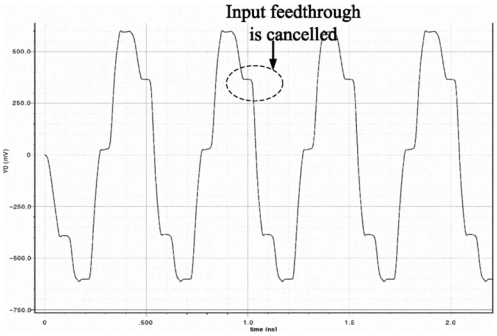


Fig. 2. The proposed THA with feedthrough cancellation.



(a) Input Frequency of 2GHz and a sample clock@10GHz without feedthrough cancellation



(b) Input Frequency of 2GHz and a sample clock@10GHz with feedthrough cancellation

Fig. 3. Comparison of the sample-and-hold with/without feedthrough cancellation.

III. High Speed Comparator Array Design

The comparator structure, shown in Fig. 4, is fully differential and consists of 4 stages. The first stage is a four input low gain pre-amplifier. The pre-amplifier is utilized to reduce input

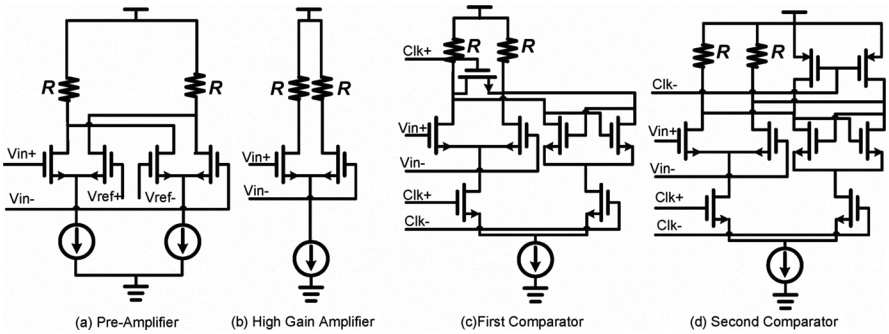


Fig. 4. The comparator array.

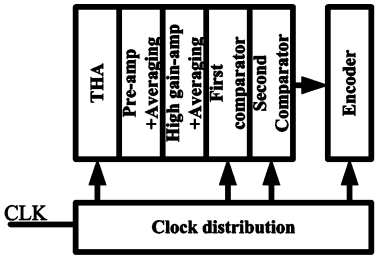


Fig. 5. Flash ADC with resistance averaging.

offset by applying large size input transistors. The second stage is a high gain amplifier to reduce the effect of latch offsets. The third stage is a current mode logic (CML) latch with a reset switch to remove the comparator overdrive recovery. However, for comparator speed over 10GS/s with a 1.2V differential input range, the traditional CML latch cannot overcome the overdrive recovery distortion challenge. The simulation result is shown in Fig. 7. To address this issue, we propose a new comparator as shown in Fig. 4(d). The output node is reset to the supply voltage V_{DD} when the comparator is not making the decision. In comparison with the previous comparator array used in the 5-bit ADC [4], this design consumes less area and successfully overcomes the overdrive recovery distortion.

IV. Flash ADC Architecture with Averaging

Fig. 5 shows the architecture of the 5-bit flash ADC. This ADC uses resistor averaging in two places to filter out random mismatch between arrays of differential pairs, substantially improving the accuracy of small MOSFETs with low input capacitance [5]. With the proper number of dummy preamplifiers at the end of each array, the optimized averaging network can lower the integral nonlinearity (INL) by 3.3X. To obtain the same linearity without averaging, the transistor W/L ratio and therefore power dissipation must be scaled up by 10X. In our case, the optimal choice is 6 dummy preamplifiers at the end of each array and the Ramplifier/Ravg is chosen to be 0.25.

In this design, the reference voltages for all the comparators are generated from a resistor ladder, the input signal and the reference voltage are connected directly to the differential pair of the 1st preamplifier. The differential pair couples the input signal and the reference voltage through the capacitance C_{gs} of each MOS transistor, since the source terminals of the transistors are tied together. To avoid significant reference ladder feedthrough, a source follower is put between reference voltage tap and pre-amplifier, which reduces feedthrough distortion by more than 10 times compared to the one without source followers as shown in Fig. 8.

V. Simulation Result

Fig. 6 shows the comparison of total harmonic distortion (THD) performance between traditional SSF THA and proposed feedthrough cancellation SSF THA. The frequency of the analogue sinusoidal input is varied from 500MHz to 5GHz. The measurement results reveal that the T/H circuit achieves 6-bit effective number of bits (ENOB) at 10GSamples/s and an input frequency of 4GHz. Table I summarizes the performance and comparison with previous work.

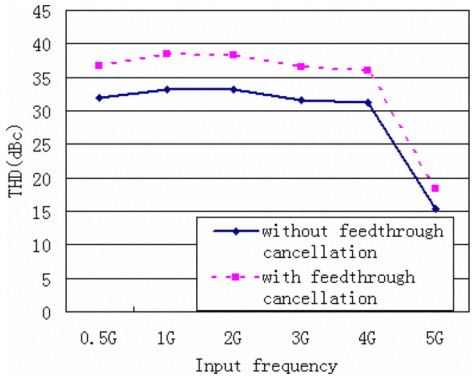


Fig. 6. THD total harmonic distortion comparison.

Fig. 7 shows the overload recovery simulation with the worst case input signal (the rail-to-rail swing). The input signal is shown in Fig. 7(c). As shown in Fig. 7(a), an error is generated in the first comparator due to its weak reset ability. After the second comparator, the original input signal is recovered.

Fig. 8 shows the comparison of pre-amplifiers' feedthrough effect with and without source followers. Since the signal feedthrough is the maximum at the middle of the ladder, only

TABLE I

PERFORMANCE SUMMARY

	[7]	[8]	[9]	This work
Technology	SiGe HBT	InP DHBT	0.18μm CMOS	65nm CMOS
Sampling Rate	8GS/s	12GS/s	10GS/s	10GS/s
Input Frequency	4GHz	2GHz	2.5GHz	4Ghz
THD (dBc)	-30	-31	-36	-37.5
ENOB (bit)	4.7	4.7	5.7	5.9
Supply Voltage	5.2V	5.2V	1.8V	1.4V
power Consumption(mW)	550	390	200	26

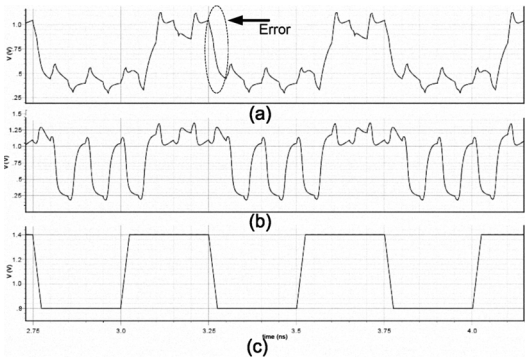


Fig. 7. Overload Recovery simulation with worst case signal.

middle references are collected to check the performance of reference source followers.

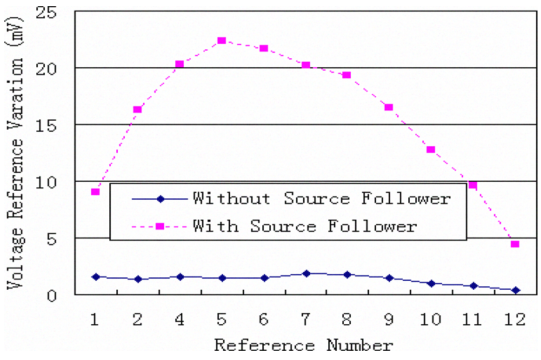


Fig. 8. Pre-amplifier feedthrough distortion simulation.

As shown in Fig. 8, if the voltage reference is followed by a source follower, the voltage reference ripple is dramatically decreased. The maximum ripple is 1.5mV, which is smaller than 1LSB (18.75mV). The layout of SSF THA circuit is shown in Fig. 9.

VI. CONCLUSION

A proposed switched source follower THA with feedthrough cancellation is presented and applied to a 5-bit 10GS/s flash ADC. The proposed SSF THA dramatically improves the settling behavior and achieves a THD of -37.5dBc at the sampling rate of 10GS/s with an input frequency of 4GHz. The THA core only consumes 26mW. Moreover, a new comparator with a reset switch is designed to remove the overload recovery effect, which is suitable for high speed ADC. Resistance averaging network is used to improve the ADC INL performance. A reference ladder with source followers is applied to dramatically reduce the pre-amplifier feedthrough distortion for more than 10 times.

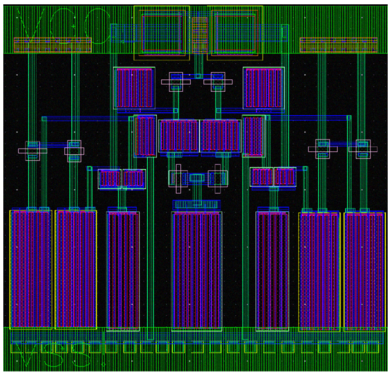


Fig. 9. The proposed SSF THA layout with a dimension of 32μm×33μm.

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