A 0.35-1 V 0.2-3 GS/s 4-bit Low-Power Flash ADC for a Solar-Powered Wireless Module

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***Abstract*- This paper reports a 4-bit flash ADC with a supply range from 0.35 to 1 V. The corresponding sampling rates are 0.2 to 3 GS/s. This low-voltage low-power ADC is a feasible building block for a solar-powered wireless module. Passive subtraction by resistor ladders replaces active subtraction by 4-input preamplifiers since the linearity of ladders is independent of supply voltage. Passive subtraction and low-threshold devices enable low-supply operation. At 1.2 GS/s, the ADC consumes 1.93 mW from a 0.6-V supply. The ENOB is 3.60 bit and ERBW is 550 MHz, resulting in an FOM of 145 fJ/conversion-step.**

I. Introduction

A modern house requires many wireless modules like sensor nodes and transceivers to perform data transmission, device control and safety sensing [1]. Compared to wired solutions, wireless modules do not have signal routing. If these modules are powered by solar cells, the supply routing can be further avoided. These wireless modules are either placed inside or outside a house. If the modules are placed on the roof or attached to the outer wall, the open circuit voltage of a solar cell changes with the weather. At 25°C cell temperature, a high quality monocrystalline silicon solar cell may produce 0.6-V open-circuit voltage. Even with 25°C air temperature, the cell temperature in a full sunlight environment will probably be close to 45°C, reducing the open-circuit voltage to 0.55 V per cell. Inside a house, the voltage is even lower due to the weak light environment. For identical cells, a cell with twice the surface area of another will, in principle, has double reverse saturation current because it has twice the junction area. Our target is to drive these modules with small size solar cells to reduce the cost per module.

As depicted in Fig. 1, a wireless module generally consists of four basic blocks: RF frontend, data converter, baseband and power supply. In digital communication systems, ADCs convert RF or IF signals into digital form for subsequent digital processing. In addition to accuracy and operation speed, power consumption and supply voltage are the primary concerns in portable communication devices. A feasible ADC must be low voltage and low power simultaneously to satisfy all the requirements for a solar-powered wireless module. The implementations of low-voltage analog [2], RF frontend [3][4] and digital circuits [5][6] have been demonstrated in recent publications. Some publications also show the implementation of low-voltage data converters [7][8][9]. Low supply voltage often leads to low operation speed. So far, the maximum sampling rate of very low voltage ADCs is limited less than 100 MS/s.

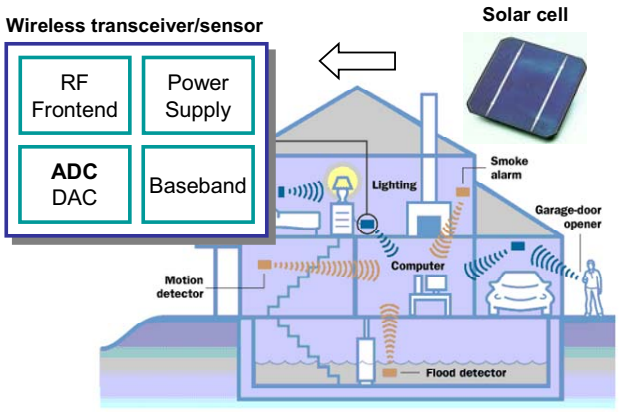


Fig. 1. The roles of wireless modules in a modern house and the conceptual block diagram of a wireless module.

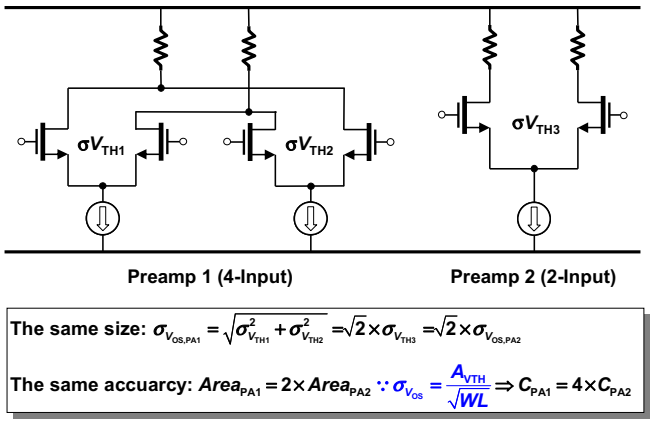


Fig 2: Comparison of 4-input and 2-input differential pairs.

This paper reports a high-speed 4-bit flash ADC with a supply voltage range from 0.35 V to 1 V. In other words, this ADC can be directly powered by solar cells without additional power management circuits or rearrangement of cells, e.g., serial connection, to boost supply voltage. The remainder of the paper is organized as follows: Section II discusses the architecture of the ADC and implementation of building blocks. Section III describes the measurement results of the proposed ADC. Finally, Section IV is the conclusion.

II. ADC Architecture and Building Blocks

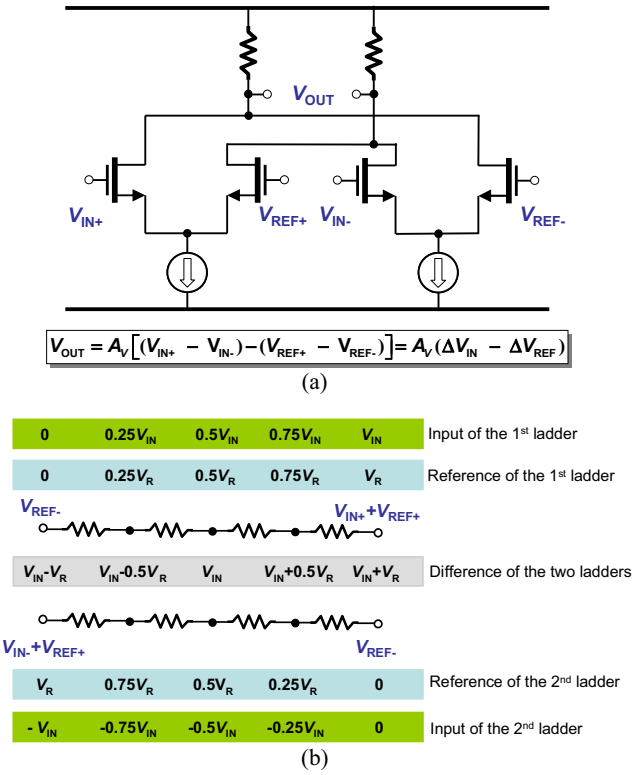


Fig. 3. (a) Active signal subtraction. (b) Passive signal subtraction.

In recent GS/s flash ADCs, both the input and reference signals are usually differential to obtain better immunity against supply and substrate noises. To perform the subtraction of the input signals from reference voltages, the 1st-stage amplifiers are often 4-input preamplifiers or comparators. The random offset of paired transistors is inversely proportional to the square root of device size. Because of two input pairs (two mismatch sources) in a 4-input amplifier, the device sizes of a 4-input amplifier should be two times larger than that of a 2-input one to achieve the same accuracy. Furthermore, there are two transistors connected to an output node of a 4-input amplifier. Consequently, the output parasitic capacitance of a 4-input amplifier is four times lager than that of a 2-input one. Enlarging device sizes or utilizing calibration techniques enhances the matching properties. Nonetheless, enlarging sizes increases power consumption and limits operation speed. Calibration techniques complicate ADC design.

In [10], 2-input comparators with internal reference levels replace conventional 4-input comparators. To generate the internal reference level, the transistor sizes of an input pair are designed to be imbalanced. The innovative design does not require external reference voltages. However, the input range of the ADC is fixed once the input transistor sizing has completed. In conventional flash ADCs, reference ladders only provide reference voltages. In bipolar flash ADCs, reference ladders and source followers are combined to perform signal subtraction [11]. In the proposed ADC, the input signals and reference voltages are directly connected to

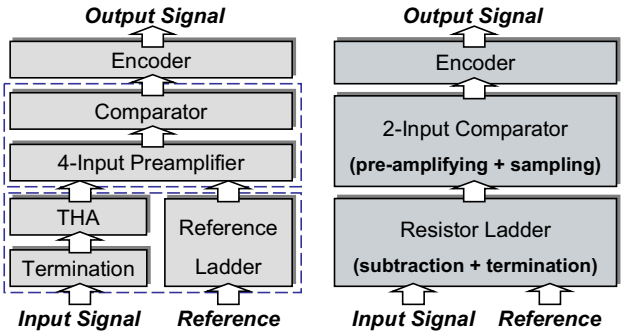


Fig. 4. (a) A conventional flash ADC. (b) The proposed ADC.

the resistor ladders. Fig. 3(a) and 3(b) depict the concepts of active signal subtraction by a 4-input amplifier and passive subtraction by resistor ladders, respectively. The passive case shows a simplified example. The distribution of the reference and input signals is illustrated according to the superposition theorem. The resultant tap voltages of the ladders are the differences between the input and reference signals. Consequently, the resistor ladders perform the same function as the 4-input amplifier. Compared to active signal subtraction by a 4-input amplifier, the passive subtraction is more accurate since the matching property of poly resistors is better than that of transistors in advanced CMOS processes. In addition, design parameters of an amplifier are sensitive to supply voltage while the linearity of passive subtraction is independent of supply voltage scaling. In flash ADCs employing 4-input amplifiers, two input nodes of an amplifier are connected to static voltage levels. In other words, two input transistors do not generate any transconductance, resulting in small voltage gain. In high-speed ADCs, an on-chip resistive input termination stabilizes the amplitudes of input signals. The resistor ladders in this design also serve as input termination devices. Fig. 4(a) and 4(b) show the simplified block diagrams of a conventional flash ADC and the proposed one, respectively. In this work, building blocks like THA and 4-input amplifiers are removed. Required functions are merged into the remaining blocks.

The proposed ADC consists of 2 resistor ladders, 15 comparators and a 15-bit to 4-bit ROM-based encoder as illustrated in Fig. 5 where each comparator is composed of two class-AB latches and a sense-amplifier-based flip-flop (SAFF). Fig. 6 shows the schematic of the class-AB latch with a static preamplifier and the sense amplifier of the SAFF. To reduce the voltage headroom, the biasing and loading transistors of the preamplifier are biased at V_{DD} and ground, respectively, to be in the linear region. Consequently, no extra bias voltage is required in this design. For low voltage operation, the preamplifier is composed of low threshold voltage transistors (around 0.15 to 0.2 V). A ROM-based encoder converts 15-bit thermometer codes into 4-bit Gray codes. Then, TSPC flip-flops clocked at full sampling speed synchronize the output codes. For measurement, the

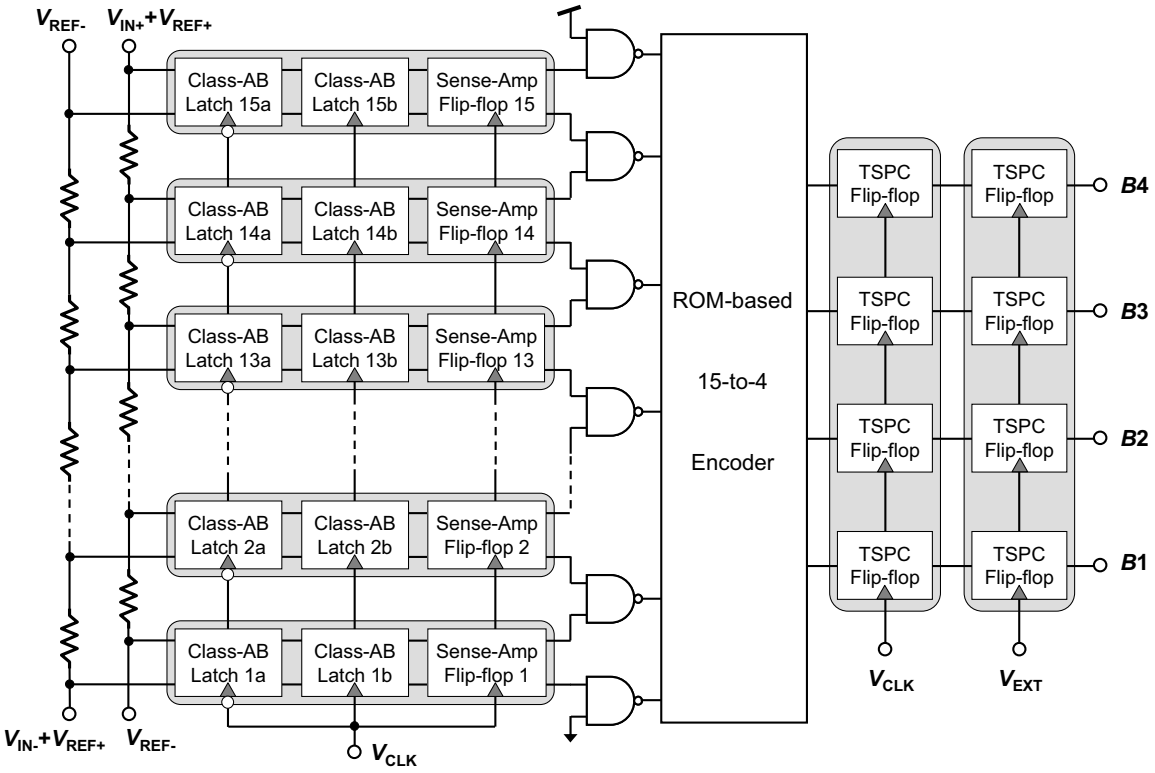
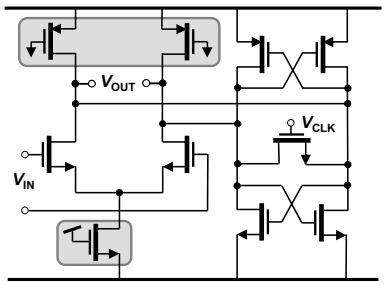


Fig. 5. The block diagram of the proposed 4-bit flash ADC.



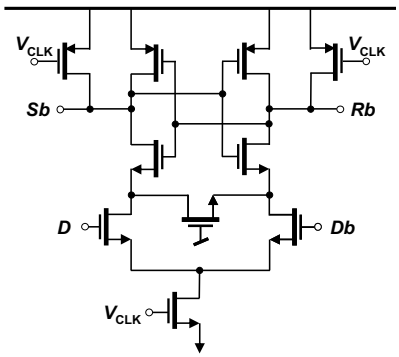


Fig. 6. Class-AB latch (left) and sense amplifier of SAFF (right).

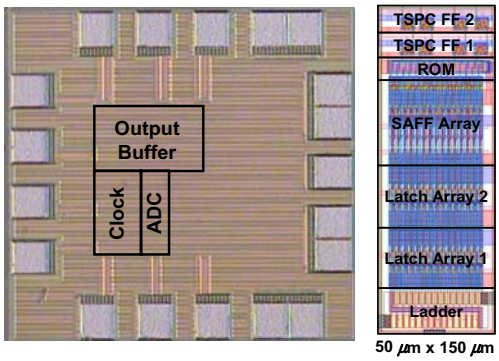


Fig. 7: Chip micrograph and zoomed core layout view.

synchronous data are then sampled by TSPC flip-flops triggered by an external clock signal.

III. Experimental Results

This ADC is fabricated in a 1P9M 90nm CMOS process. Fig. 7 shows the micrograph and zoomed core layout view. The ADC core only occupies an active area of 50×150 μm^2. Fig. 8 shows static and dynamic measurement results where the peak DNL is 0.57 LSB and INL is 0.39 LSB. Table I shows the specification summary at different supply voltages and comparison to state-of-the-art high-speed low-resolution ADCs. The lowest supply voltage of these state-of-the-art works is 0.8 V. On the other hand, the supply voltage of this work is in the range of 0.35 to 1 V and the corresponding sampling speed is 0.2 to 3 GS/s. At 1.2-GS/s operation, this ADC only consumes 1.93 mW from a 0.6-V supply. The low input frequency ENOB is 3.60 bit and the ERBW is 550 MHz. The resultant FOM is 145 fJ/conversion-step.

IV. Conclusion

This work shows a high-speed ADC with very low supply voltages. Compared to conventional flash ADCs, inessential building blocks are removed and remaining blocks are merged, leading to a compact structure. The passive signal subtraction and low-threshold transistors enable low supply voltage operation. Although the operation speed decreases

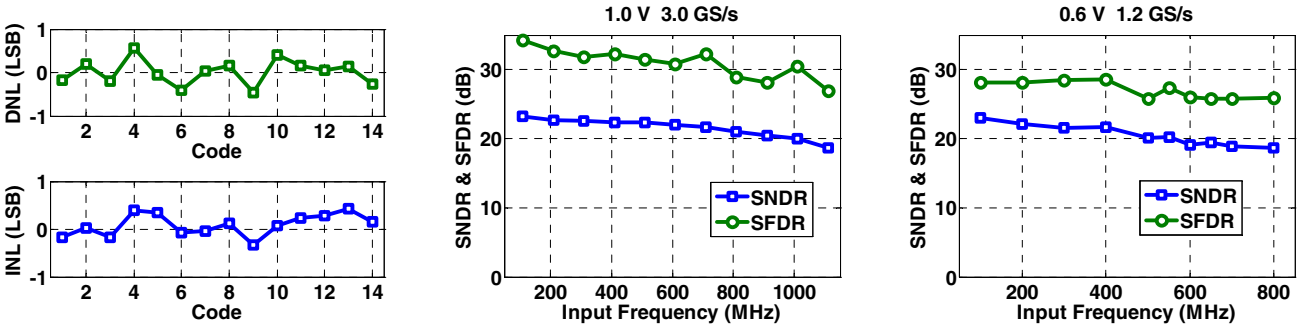


Fig. 8. Measured static and dynamic performance.

TABLE I SPECIFICATION SUMMARY AND COMPARISON TO STATE-OF-THE-ART WORKS

Specification (Unit)	ISSCC'06	VLSI'06	ISSCC'08	ISSCC'08	This Work					
Supply Voltage (V)	1.2	1.2	1	0.8	1	0.8	0.6	0.5	0.4	0.35
Power (mW)	2.5	5.92	2.2	1.2	8.49	4.76	1.93	1.37	0.60	0.54
Sampling Rate (GS/s)	1.25	0.5	1.75	0.25	3.0	1.8	1.2	0.8	0.3	0.2
ENOB (bit)	3.7	4.4	4.67	4.6	3.57	3.56	3.60	3.50	3.41	3.03
ERBW (MHz)	3300	250	878	125	1000	700	550	450	300	150
FOM (fJ/conv.-step)	160	755	50	197	357	288	145	152	188	330
Architecture	Flash	SAR	Folding	SAR	Flash					
Resolution (bit)	4	5	5	5	4					
Technology	90 nm	65 nm	90 nm	65 nm	90 nm					

with the downscaling of the supply voltage, the accuracy roughly maintains the same level. This work occupies a small chip area ($50 \times 150\ \mu m^2$), achieves high operation speed (up to 3 GS/s) and has a very low supply voltage (as low as 0.35 V). For ADCs with sampling speed over 1 GS/s, the lowest supply voltage previously reported is 0.8 V. This ADC operates at 1.2-GS/s sampling speed with a 0.6-V supply voltage.

ACKNOWLEDGMENT

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