56Gs/s ADC : Enabling 100GbE

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Abstract: A 100G coherent receiver needs 4 56Gs/s ADCs and a tera-OPs DSP which dissipate only tens of watts. This paper discusses the forces pushing towards a single-chip CMOS solution, and the challenges in realising this.

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1. Introduction – ADCs for 100G systems

To provide a long-haul 100Gb/s optical transport network with maximum reach and immunity to optical fibre non-idealities, the industry has settled on dual-polarisation quadrature phase-shift keying (DP-QPSK) as a modulation method, which means that a coherent receiver is required. The biggest implementation challenge resulting from this decision is the need for low-power ultra-high-speed ADCs, and their technology requirements define the way that such a receiver can be implemented.

Without suitable ADCs – especially with low enough power consumption – it is impossible to produce a 100G coherent receiver suitable for a commercial optical network, as opposed to prototype systems only suitable for demonstration in the lab. Also, in future such ADCs will be required for higher-speed short-haul links, where low power and cost become even more important because the number of these links is much larger than long-haul ones.

These ADCs need sampling rates of at least 56Gs/s and resolution of 6 bits or more, with power consumption of no more than a few watts each to fit within the power constraints imposed by the system. To do this with sufficient dynamic range for input signals up to 15GHz and higher, it was thought that this would require technology such as very advanced SiGe or ultra-small-geometry CMOS (40nm or smaller). By extrapolating from historic advances in ADC design it was predicted at the end of 2008 that suitable ADCs would not be available until 2013 [1].

However, the development of new circuit techniques means that these ADCs actually became available in 2009 using 65nm CMOS [2]. This brought forward the date at which single-chip 100G coherent receivers became technically and economically feasible, and has caused a significant change in the industry roadmap for these devices.

2. The drive towards a single-chip CMOS ADCDSP

A DP-QPSK coherent receiver needs 4 ADC channels since there are two optical polarizations and each needs two ADCs to digitize an I/Q signal. To achieve 100Gb/s net line rate, a baud rate of at least 28Gbaud/s is used to allow for overhead, which needs 56Gs/s ADCs. The system SNR requirements mean that 6 bit resolution is typically required to allow some margin for added noise and distortion, so for 4 ADCs the output data rate to the DSP is 1.3Tb/s – or 1.8Tb/s if 8 bit resolution is used to allow more margin and/or digital AGC after the ADC.

If the ADCs are not integrated with the DSP then this huge amount of data has to be transmitted between chips, which is not only difficult to implement (very large number of channels with high data rate) but costs a lot of power for serialization and de-serialization as well as actually transmitting the data – even using an optimistic figure of 100mW/ch for an 11Gb/s channel (ADC transmit + DSP receive) this means 3-4W per ADC is needed just to transfer the data. This is acceptable for a prototype or demonstrator, but not for a production solution.

A 100G receiver DSP – which performs functions such as equalization, chromatic dispersion compensation, and data recovery – needs of the order of 50M gates, which mandates the use of CMOS. The system power requirement for a complete coherent receiver is only a few tens of watts; since a 40G ADCDSP chip in 90nm already dissipates more than 20W [3] geometries of 65nm or smaller are needed for a 100G receiver, as well as power-efficient design techniques.

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This implies that the ADC should also use CMOS; though this means the design is extremely challenging, a single-chip solution is really the only viable way forward, especially so that we can take advantage of future CMOS technology improvements – though this does assume that the ADC performance scales similarly to digital circuits, which may not be true for conventional ADCs. Even if a multi-chip solution can be built – for example, using SiGe ADCs together with a CMOS DSP in a multichip module (MCM) – then not only will the overall power be higher, but the production cost will be greater and the yield of such a complex solution will inevitably be lower. This also does not give a good roadmap towards even lower power and cost solutions for short-haul and beyond 100G.

3. 56Gs/s CMOS ADC challenges

Designing a 56Gs/s 6-8b ADC in any technology presents major difficulties, and these are made even worse here because available power for the ADC+DSP is limited both by supply capability and thermal dissipation. A reasonable target is 10W or less for a complete 4-channel ADC, which means little more than 2W per ADC cell. Conventional ADCs with this level of performance dissipate much more power than this, due to the high power needed for the wideband sampling/demultiplexing front-end and clock circuits as well as the back-end ADC power.

To achieve such high speed and resolution multiple lower-rate interleaved ADCs are used, driven by one or more wideband sample-and-hold (S/H) circuits, usually with more demultiplexing in between. The S/H circuits need very wide bandwidth and low distortion, which is why either SiGe or very small geometry CMOS (40nm or smaller) is normally said to be needed for 56Gs/s. However, with the sub-1V supply voltages imposed by 40nm CMOS it is very difficult to design a S/H with reasonably large signal swing (to preserve SNR) and linearity (to preserve THD); higher-voltage SiGe avoids these problems, but at the cost of much higher power dissipation.

The very small device sizes available in modern CMOS processes do combine low power consumption and high density with high speed, but this comes at the price of increased noise and mismatch. The normal solution to this is to increase transistor sizes (gate length and/or width), but this is not possible here because we cannot afford to reduce bandwidth or increase power consumption. Small transistors mean poor matching in both S/H and ADC, not just in the signal paths but also in the clock paths, where 100fs clock skew causes -40dBc distortion for a 16GHz input signal. The only feasible way to reduce these mismatch-induced errors is by widespread on-chip calibration.

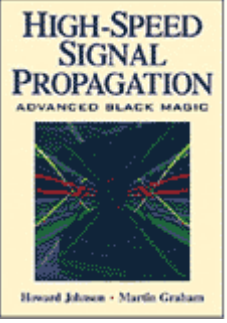
Providing clock skew adjustment is not so difficult in theory; measuring and calibrating skew down to sub-picosecond accuracy is a much bigger problem, especially being able to maintain this accuracy over time and environmental variations without either being able to take the ADC off-line for calibration or needing a huge amount of complex data analysis to calculate the errors.

4. CHArge-mode Interleaved Sampling (CHAIS) ADC

To overcome these challenges, one solution is to use a new sampler/demultiplexer architecture [2] which gives the linearity, noise and bandwidth required without needing extremely short-channel (40nm or below) transistors, allows simple calibration of amplitude and timing errors during operation, and dissipates <0.5W. Instead of a conventional S/H using analogue switches and sampling capacitors, the CHAIS circuit generates controlled-shape constant-area (charge) sampling pulses which are then demultiplexed to drive a large array of 8b SAR ADCs (320x175Ms/s).

Using SAR ADCs instead of full-flash means that increasing resolution from 6b to 8b has only a small penalty in power and area, but the increased resolution reduces quantisation noise and allows more margin for other noise contributions. It also opens up the possibility of doing some AGC digitally after the ADC instead of in the optical front-end, which has the advantage of perfect channel matching even with rapid gain changes to track optical power variations. SAR ADCs also scale very well with smaller technology since most of the power is digital.

The high circuit density of CMOS is used to good effect by having a large number of calibration DACs (more then 400 per ADC) to trim out all significant device mismatches in the signal path, including timing errors (skew) as well as amplitude errors (gain and offset). The way that the CHAIS circuit works means that all these errors can be calculated in real-time in the background by simple analysis of all the ADC digital output data; this analysis is done inside the ADC, the results are then read out at a much lower rate (microseconds to tens of milliseconds) and used to drive a low-complexity convergence algorithm with a time constant of typically less than a second, which provides convergence at power-up and also continuously during operation to track any parameter drift.



5. DSP and integration issues

Realising the DSP for a 100G coherent receiver is hardly trivial, not just because of the extremely high processing power required (12 TOPS were needed [3] for a 40G receiver) but the very wide datapaths (thousands of bits wide) needed to keep clock rates reasonably low in order to improve power efficiency – high clock rates need more latches to reduce logic depth, which leads to increased power consumption.

The design problem then becomes one of interconnect, not gate count. Unfortunately design tools (and designers) tend to design the circuits first and just accept the interconnect that results, where really this should done be the other way round – or you can end up with a DSP design which is difficult (or even impossible) to lay out.

Even assuming that you can design the ADC and DSP separately, there are other major problems to be overcome when integrating the two in a single chip 100G coherent receiver. Noise coupling between digital and analogue is one obvious issue, and by looking at approximate numbers the sheer scale of the problem becomes apparent.

We now have a very large DSP with peak switching currents of ~100A (and perhaps ~100mV supply noise) on the same die as ADCs which need to have jitter of the order of 100fs. Assuming a reasonable supply noise delay sensitivity of 1ps/mV for the clock path, the analogue supply noise needs to be ~0.1mV, which means ~60dB isolation between analogue and digital regions.

This might not seem so difficult until you realise that the bandwidth of this noise coupling is many GHz because – unlike "normal" analogue or RF circuits – there's nothing to band-limit the noise, and at these frequencies noise isolation methods such as triple-well are no longer effective. In fact, given the frequencies and bandwidths involved and the jitter requirements, the noise coupling problem is probably more difficult than on any previously realised mixed-signal chip – but it can be solved by very careful design, some new noise isolation techniques, and maybe a touch of "black magic" [4].

It is obviously undesirable to allow large DSP current spikes to get out of the package and into the PCB, both for good EMC performance and to prevent them interfering with the analogue circuits. Relying on PCB decoupling also gives the end user a perfect opportunity to get this wrong and degrade the performance in an unpredictable manner.

Ultra-low-inductance decoupling inside the customised flip-chip package and on the chip solves this problem, but any resonances between the internal L and C are then very high Q and always fall in the hundreds of MHz region. So just adding decoupling on the "more is better" principle can do more harm than good; simulations of the entire chip and package together are needed, and it will usually be necessary to take steps to damp the power-supply resonances such as damped on-chip decoupling and/or controlled-ESR ceramic decouplers in the package.

6. Conclusions

New ADC techniques have made it feasible for the first time to design single-chip 100G coherent receivers in 65nm CMOS which meet the performance and power requirements of long-haul optical systems, and provide a way forward for short-haul and higher-rate applications in future with migration to 40nm and beyond.

Being able to design a suitable ADC only solves part of the problem of producing such an ADCDSP; the mixed-signal integration issues are at least as challenging, but can still be solved by sufficiently "intelligent design".

7. References

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