# A 1.8V 6-bit 1GS/s 60mW CMOS Folding/Interpolation ADC Using Folder Reduction Circuit and Auto Switching Encoder

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***Abstract* - In this paper, CMOS analog-to-digital converter (ADC) with a 6-bit 1GS/s at 1.8V is described. The architecture of the proposed ADC is based on a folding type ADC using resistive interpolation technique for low power consumption. To reduce the power consumption, a folder reduction technique to decrease the number of folding blocks (NFB) by half of the conventional ones is proposed. Further, a novel layout technique is introduced for compact area. With the clock speed of 1GS/s, the ADC achieves an effective resolution bandwidth (ERBW) of 200MHz, while consuming only 60mW, of power. The measured INL and DNL were within ± 0.5LSB, ± 0.7LSB, respectively. The measured SNDR, was 33.82dB, when the fin=100MHz at Fs=500MHz. The active chip occupies an area of 0.27mm$^2$ in 0.18μm CMOS technology.**

## I. INTRODUCTION

The demands for digital multimedia broadcasting (DMB) receiver, ultra wideband (UWB) system, GPS are now being increased. These communication systems ADC need a high speed and low power consumption. In the field of high speed ADC, full flash type architecture is known to be the most popular one. However, it consumes large chip area and power dissipation, because of many comparators. In order to overcome the drawbacks of the flash type ADC, folding and interpolation techniques are proposed [1]-[6]. For that reason, we proposed three techniques by using folding and interpolation type ADC. First, to maintain the linearity of analog signals source-degeneration preamplifier is used. Second, power consumption is minimized by use of folder reduction technique. This technique was reduced a half of preamp and number of folder (NFB). Finally, for high speed operation, auto-switching encoder without switching block is proposed. As a result of theses proposed technique, ADC has a high speed like a flash type ADC and low power consumption. The contents of the paper are as follows. In section II, the architecture of the ADC is described. In section III, circuit design of the proposed block is discussed. The fabrication results and experimental results are described in section IV. Finally, the conclusions are summarized in section V.

## II. ARCHITECTURE

First consideration of design folding and interpolation ADC is deciding structure. Specially, decide a folding rate (FR) is most important thing for high speed. The 6-bit folding and interpolation ADC's characteristic summary is described in table I. 2+4 structure has increase of folding frequency by equation (1). It has a limitation of input frequency. Accordingly optimized structure is 1+5 for high speed.

TABLE 1. CHARACTERISTIC SUMMARY OF THE 6-BIT F/I ADC

| Structure | FR | NFB | IR | Preamp |
|---|---|---|---|---|
| 1+5 | 2 | 4 | 8 | 12 |
| | | 2 (with folder reduction technique) | | 6 |
| 2+4 | 4 | 4 | 4 | 20 |

$$f_{fold} = \frac{\pi}{2} \times FR \times f_{input} \quad (1)$$

Throughout the proposed folder reduction technique, NFB has reduced a half of conventional structure. This is maintained a linearity of analog final output signal. This paper proposed ADC structure is 5-bit folding factor by FR=2, NFB=2, interpolate rate (IR) 8, but it has satisfied 6-bit resolution. The block diagram of the proposed ADC is shown in figure 1. This ADC consists of a pre-processing block, folding block, interpolation block, and digital signal processing block.

## III. CIRCUIT DESIGN

### A. *Source-degeneration preamplifier*

The linearity preamplifier output is very important in the folding ADC. In order to increase the linearity, source-degeneration preamplifier is used. Figure 2 shows a source-degeneration preamplifier. Preamplifier is maintained the regular current by $R_s$ then it is reduced the mismatching of resistance. Figure 3 shows a principal of source-degeneration preamplifier. To maintain the output signals linearity, $R_s$ is increasing the input range. As shown figure 3(c), the input range is increased when $R_s \neq 0$. Regular current by feedback is maintaining the linearity.

### B. *Folder-Reduction Technique*

The optimized structure of folding and interpolation ADC is FR=2, NFB=4, IR=8 for high speed as shown section II. This paper proposed folder reduction technique to reduce a half of preamp number and NFB. Folder reduction technique satisfied 6-bit resolution by maintain FR=2, IR=8, but NFB=2. The proposed low power consumption folder reduction technique is shown in figure 4. Folder reduction circuit consists of 2 phase shift stage by equal resistance. The input of first phase shift stage has 90° phase difference between adjacent signals. This signals change 45° phase difference through the first phase shift stage[6].

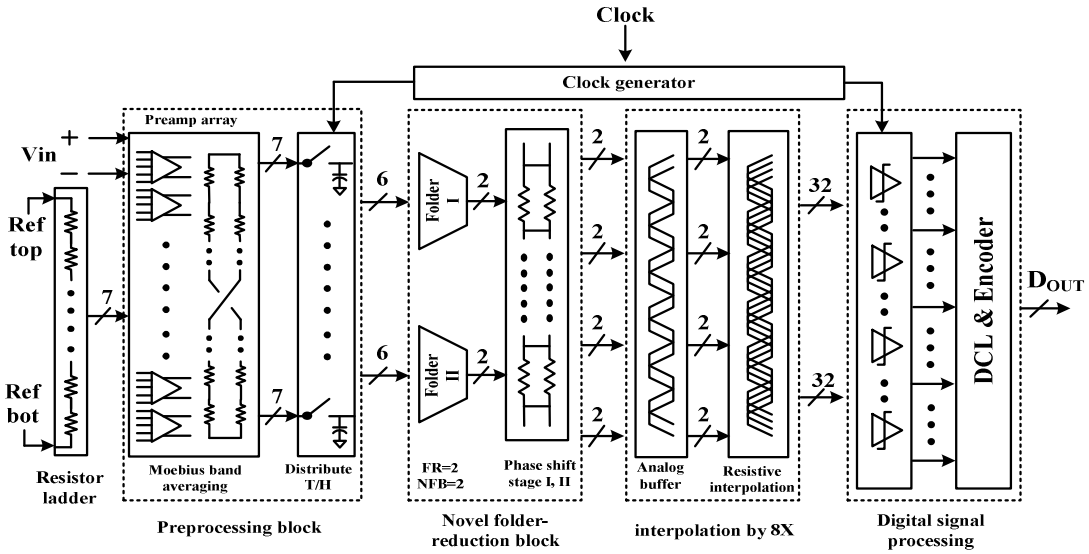


Figure 1 Block diagram of proposed ADC

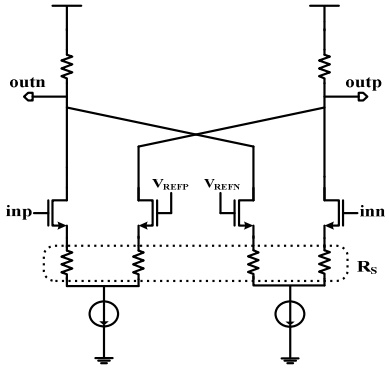


Figure 2 Source degeneration preamplifier

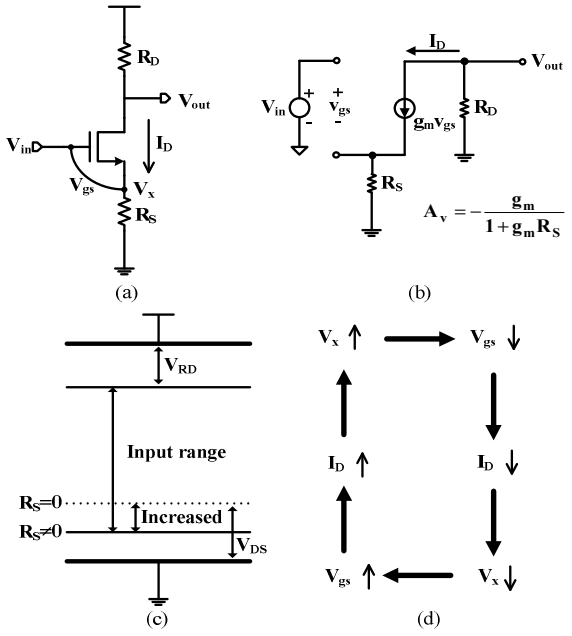


Figure 3 Principal of source-degeneration preamplifier

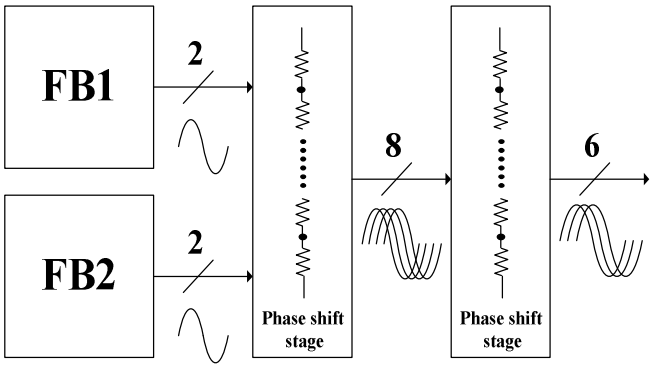


Figure 4 Folder reduction technique

But 45° phase different signals compare to primary signals, it moves 22.5° phase. The output of first phase shift stage generate the maintaining 45° phase difference and averaging signal by equal resistance through the second phase shift stage. As a result of 2 phase shift stage generated 45° phase different signals by maintaining the same phase with a input signals. These signals have same linearity compare to output of NFB=4.

### *C. Auto-Switching Encoder*

Conventionally, the output of the folding block has the reverse-thermometer codes in the folding-interpolation ADC. Thus the digital block of the folding-interpolation ADC must include a switching block for the conversion of the reverse-thermometer code. However, it is very complicated and hard to implement. In this paper, a novel auto-switching encoder to convert the reverse-thermometer code into the binary code proposed. The efficient digital algorithm used in the proposed auto-switching encoder is described in figure 5.

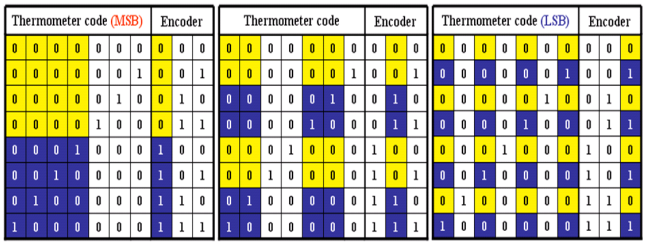


Figure 5 The proposed Algorithm

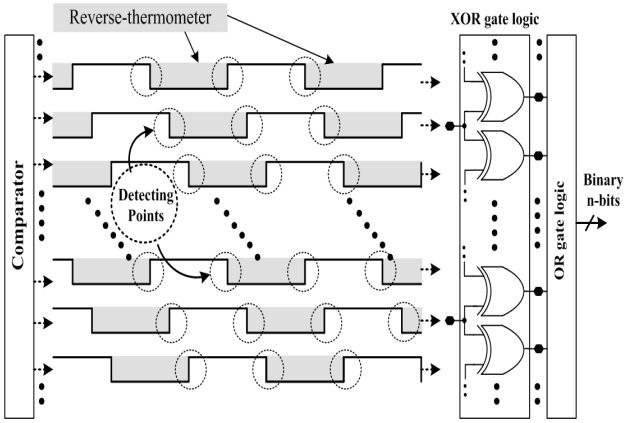


Figure 6 Auto-switching encoder

It is a simple example for an algorithm of 3-bit auto-switching encoder. Initially, the thermometer codes, the outputs of comparator, are converted to "1" at the boundary of "0" and "1" by an XOR gate. As shown in figure 6 then, the converted digital code generates the output code through an OR gate logic. Consequently, the proposed algorithm generates the desired digital output code without any unnecessary switching blocks.

*D. Layout floor plan*

The 6-bit 1GS/s folding-interpolation ADC was implemented in a 0.18μm CMOS process with a 1.8V analog and digital power supply. The floor plan of the ADC is shown in figure 7. The pre-amplifier array and distributed T/H array are of only one block, and the folder, folder reduction circuit and 2nd pre-amplifiers are merged. Especially, the analog and digital blocks are separated form each other in order to reduce the interference error by power guarding. In figure 7, further, the technique of a novel layout technique is introduced. Folding interpolation ADC has small area analog block better than digital block. Moreover after adopted folding reduction technique, area has more small than before. The sequential layout between preprocessing block and folding block is remained extra area with IR drop because of long metal routing. To reduce unnecessary area, 2nd pre-amplifier arranged between folding blocks. Throughout this novel layout technique, ADC area has decreased of 20%.

## IV. Experimental Results

The proposed folding-interpolation ADC was fabricated with the 0.18μm 1-poly 5-metal CMOS technology, with the help of Samsung Semiconductor Co. Ltd. Figure 8 represents the layout drawing of the ADC. The active area was 0.27mm$^2$. As shown in figure 9, the measured signal-to-noise-distortion-ratio (SNDR) was 33.82 dB when the input frequency was 100MHz at 500MHz clock frequency.

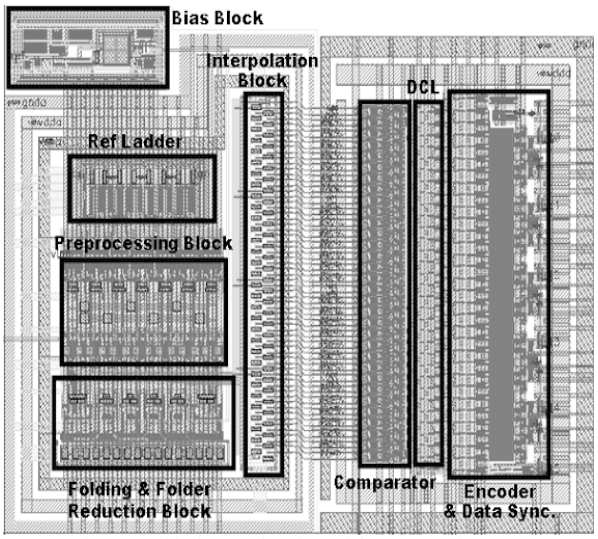


Figure 8 Chip layout drawing of the proposed ADC

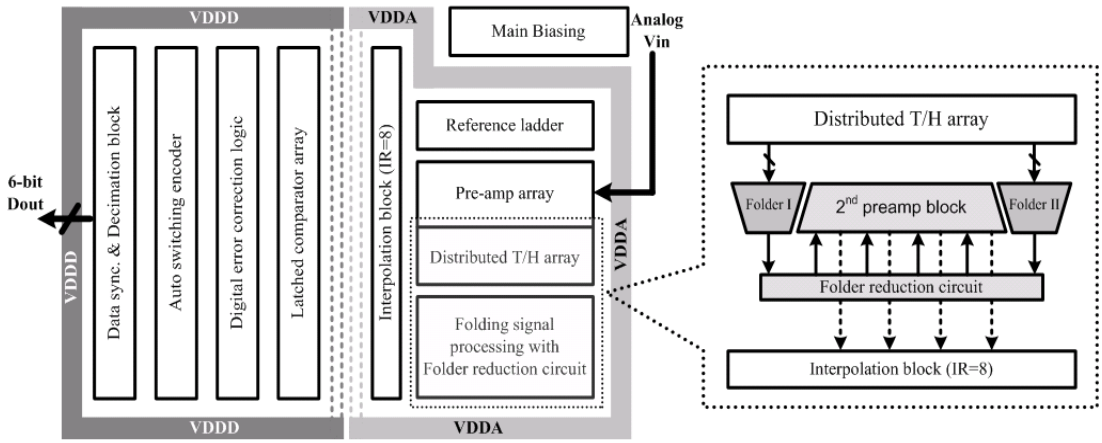


Figure 7 Proposed ADC layout floor plan

Figure 10 shows the measured results for integrated non-linearity error (INL) and differential non-linearity error (DNL). The INL is ±0.7LSB and the DNL is within ±0.5LSB.

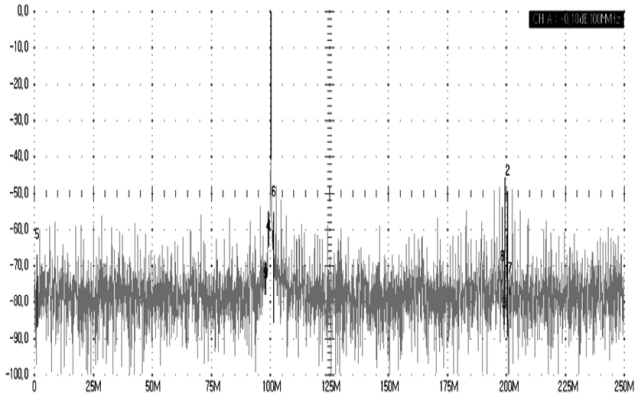

Figure 9 Measured FFT result

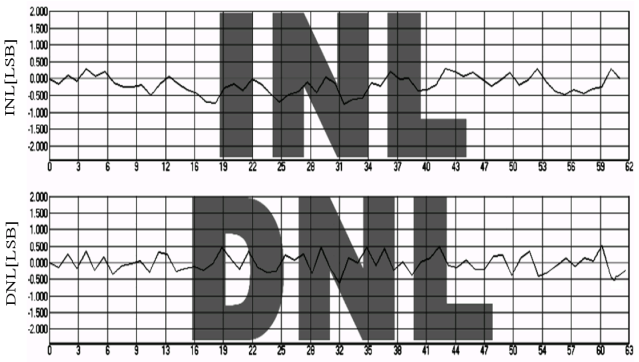


Figure 10 Measured INL and DNL

Figure 11 shows measurements of SNDR and spurious-free dynamic range (SFDR) versus input frequency at a conversion rate of 500MHz. The plot shows that SNDR is above 36.55dB from 1MHz up to 10MHz and is above 33.82dB up to 100MHz. SFDR is above 43.71dB from 1MHz up to 100MHz. Further, the ADC consumes only 60mW form 1.8V supply when the clock speed is 500MHz. The measured power dissipation is below 120μW/MS/s.

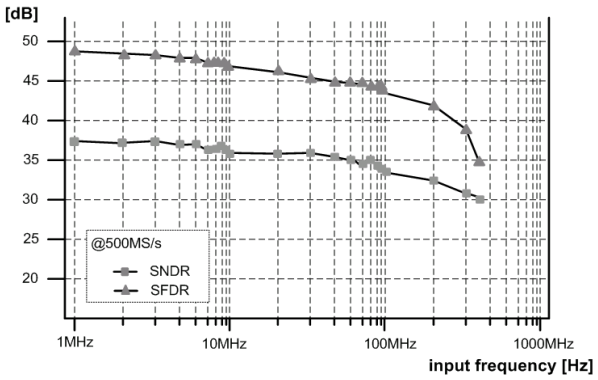


Figure 11. Measured SNDR & SFDR (@500MS/s)

## V. CONCLUSION

A 1.8V 6-bit 1GS/s CMOS ADC has been described. The architecture of the proposed ADC was based on a folding ADC using a resistive interpolation technique. The self-linearized pre-amplifier with source degeneration technique, the folder reduction technique and an auto-switching encoder were discussed for the desired performance of the ADC. The effective chip area was 0.27mm$^2$, the ADC consumed 60mW at 1.8V power supply and 500MS/s. The measured SNDR of the proposed ADC was 33.82dB when the input frequency was 100MHz at 500MS/s. The measured results of the ADC are summarized in Table 2.

TABLE 2. PERFORMANCE SUMMARY OF THE PROPOSED ADC

| | |
|---|---|
| Resolution | 6-bit |
| Sampling Freq. | 1GHz |
| Power Supply | 1.8V (Analog + Digital) |
| Analog Input Range | Diff. 0.5Vpp |
| DNL / INL (Measured data) | ±0.5LSB / ±0.7LSB |
| SNDR (Measured data) | 36.55dB (Fin<10MHz at 500MS/s)<br>33.82dB (Fin<100MHz at 500MS/s) |
| SFDR (Measured data) | 45.32dB (Fin<10MHz at 500MS/s)<br>43.71dB (Fin<100MHz at 500MS/s) |
| Power | 60mW (ADC core + digital buffer) |
| Core Area | 460um × 600um (0.27mm$^2$) |
| Process | 0.18μm 1 poly 5 metal N-well CMOS |


## ACKNOWEDGEMENT

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