Exploiting Combinatorial Redundancy for Offset Calibration in Flash ADCs

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***Abstract*—Process variations in advanced CMOS nodes limit the benefits of scaling for analog designs. In the presence of increasing random intra-die variations, mismatch becomes a significant design challenge for circuits such as comparators. In this paper we describe and demonstrate the details of a statistical element selection (SES) methodology that relies on the combinatorial growth of subsets of selectable circuit elements (e.g., input transistors in a comparator) to provide redundancy for post-manufacturing calibration of specifications (e.g., offset). A test chip consisting of an array of digitally calibrated comparators with built-in combinatorial redundancy was manufactured in 65 nm bulk CMOS. Over 99.5% of the comparators satisfy the given offset specification compared to 15% for Pelgrom-type sizing. A second test chip in the same process consists of an 8-bit, 1.5 GS/s flash ADC and achieves 37 db SNDR at low frequencies. The total power is 35 mW, 20 mW in the S&H and 15 mW in the ADC core. The figure of merit is 0.42 pJ/conv.**

***Index Terms*—ADC, analog-to-digital converter, calibration, combinatorial redundancy, comparator, flash ADC, statistical element selection.**

I. Introduction

CONTINUOUS advancement of CMOS process technology over the past four decades has made inexpensive integrated circuit products with significant processing capabilities an everyday reality. Cost pressures have resulted in substantial integration of analog and digital blocks on the same die, forcing analog designers to adapt to processes that were built for digital systems [1], [2]. As we rapidly approach the physical limits of scaling, one of the major challenges for analog circuits has been to ensure consistently high yield in the presence of increasing variability in these nanoscale CMOS processes.

In this paper we explore the benefits of a statistical element selection (SES) methodology for analog circuits that is based on exploiting combinatorial redundancy for post-manufacturing tuning [3], [4]. Combinatorial redundancy (CR) exploits inherent random variations to improve the matching of transistors and to increase yield for matching-critical circuits such as comparators. A subset of k elements is selected among an identically laid out set of N elements to provide the best matching performance. As the number of non-empty subsets among a set of N elements increases combinatorially $(2^N - 1)$, it is possible to achieve impressive matching performance with near-minimum size unit elements. The elements can be individual transistors, pairs of transistors, or passive components to best achieve the design specifications.

We present an SES methodology to determine the appropriate (N, k) numbers and the size of the unit element to ensure that a desired matching specification is met. We present measurement results from a 65 nm bulk CMOS test chip using CR-configurable comparators to validate the model predictions [5]. The generalized methodology can be used for a wide variety of analog circuits—such as current sources, differential amplifiers and comparators—that rely on precise matching of components. A second test chip in the same process that uses a modified version of the comparators implements an 8-bit, 1.5 GS/s flash ADC where SNDR is limited by the comparator noise [6].

In Section II, main sources of variation in modern CMOS processes and their effects on analog circuits are described, along with the CR basics and SES methodology. Section III presents the details of the comparator array test chip and measurement results. Section IV presents the details of the flash ADC test chip and measurement results. Section V presents the conclusions.

II. Statistical Element Selection

A. Process Variations

Manufacturing variations are a significant problem for both digital and analog circuits in advanced CMOS process nodes and they are expected to grow in importance with each new generation. Variations in modern CMOS nodes can generally be classified into two categories, systematic and random. Many of the dominant systematic variations can be predicted and addressed by using careful circuit design and layout techniques. Random variations are unpredictable and can cause significant mismatch among devices. It is the latter variability that is actually exploited by CR and the SES approach to tune the circuits after manufacturing.

1) Systematic Variations: Systematic variations can be broadly classified into two sub-groups [7]:

- Across-field effects that are caused by lithography or etching. Location of the die on the wafer can lead to a sys-

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tematic shift in device parameters. All devices in the same vicinity are affected the same way due to these effects.
- Layout dependent effects that result in different characteristics of identical devices in the same vicinity in the wafer. An example is variation due to the well proximity effect where threshold voltage of a MOS device close to an n-well can be different from an identical MOS device far away from n-wells. Other major sources are due to the polysilicon surrounding of the gates and STI stress [8]–[10].

Restricted design rules with fixed gate lengths, high regularity in diffusion, poly and metal layers, single poly orientation and lithography solutions such as double patterning and optical proximity correction are already proposed techniques to alleviate the systematic effects in leading edge CMOS processes [11], [12]. Although these methods are mainly discussed for logic gates and memories, analog designs will ultimately need to use the same rules for highly integrated CMOS chips.

2) Random Variations: Random variations are due to unpredictable and unrepeatable sources of variation in manufacturing. Random dopant fluctuation (RDF) in the transistor channel is an example of this type of variation [13]. Several new technologies such as undoped channels, high-k metal gates, thin SOI and FinFETs are being evaluated, but tens of millivolts of variation in threshold voltage is still expected [14]–[18].

Another source of random variation is line edge roughness (LER). Microscopic deviations in the poly line forming the gate can lead to uneven channel length across the width of the device. These variations can lead to an effective difference in the conductance constant ($\beta = \mu C_{ox}(W/L)$) and adversely affect matching.

Random sources of variation cannot be alleviated by following restricted design rules. Increasing the device size to average out the random variations improves matching only by $1/\sqrt{Area}$ [19]. This poor return with increasing device size (and hence total area and power) is problematic for many analog circuits, such as comparators in flash analog to digital converters (ADCs).

B. High Speed ADCs

Multi-GS/s, low-to mid-resolution ADCs are required for various applications, such as high-speed wireless and wireline communications, digital oscilloscopes, and radar. Flash and time-interleaved architectures are typically used for high-speed ADCs. The flash ADC architecture is a purely parallel architecture, using multiple comparators sampling simultaneously. The time-interleaved ADC is a more general approach, in which multiple slower ADCs are operated in parallel and their sampling time-interleaved. However, time-interleaving can result in spurious tones created by mismatch between channels, which requires significant expenditures of design time, power, and area for calibration [20].

The flash ADC is attractive because of its simplicity; a single bank of comparators is clocked at full-rate to digitize the analog input signal. However, flash ADCs suffer from random mismatch as each comparator has a unique random offset resulting from random mismatches between devices. These offsets create nonlinearity in the ADC transfer function, thereby distorting the output. Control of comparator offsets is essential to creating accurate flash ADCs. Ideally, each comparator offset should be smaller than 0.5 LSB. One-bit increase in resolution tightens the comparator matching requirements by $2\times$, since LSB is halved. To achieve this requirement by simple sizing based on the well known Pelgrom's model [19], we would need to increase the comparator sizing by roughly $4\times$, increasing the power/area penalty. Moreover, the number of comparators rises exponentially with the resolution for a flash ADC; i.e., a 1-bit increase in resolution will require doubling of the number of comparators. This leads to further doubling of the power and area consumed by the comparators. Increased input capacitance of the comparators puts significant pressure on keeping the same sampling rate. In many cases, power hungry input sampling switches and preamplifiers might be required in order to keep the same sampling rate.

Due to the poor scaling of $1/\sqrt{Area}$, analog tuning and calibration techniques were developed to address random mismatch. [21] introduced averaging, which has been used in recent flash ADCs [22]–[24], often combined with interpolation [25]–[29] and folding [30]–[32]. Another technique is auto-zeroing [33], which has also been implemented in recent flash ADCs [30], [34], [35].

A significant drawback of all analog techniques is the static power consumption of the analog front-end. Even after careful optimization, the power efficiency at a given CMOS process node is only on par with digital calibration at the previous node [29]. At constant speed/bandwidth, digital power scales with κ^{-2} [36], while analog power of CMOS flash ADCs scales with κ^{-1} [37] (where κ is the scaling factor). Because digital power scales faster than analog power, the use of digital logic to reduce analog complexity is far more attractive.

Recent flash ADCs use digital calibration to overcome random mismatch in the comparators [38]. Typical digital calibration techniques include DAC-based calibration [39]–[47] and redundancy [40], [48], [49]. CR and SES are extensions to redundancy to exploit selection among nominally identical but randomly varying devices to achieve precise tuning. Unlike redundancy as described in [50], however, it is the exponential population of aggregate subcomponents that are used to search for a configuration that meets the required specifications.

C. Statistical Element Selection Using Combinatorial Redundancy

1) Basics: Statistical Element Selection (SES) was recently proposed to alleviate the problems caused by extreme variability in advanced CMOS processing nodes [3]. The basic concept is to use N identically laid-out elements for a given circuit block (e.g., branches of input transistors in a comparator) and use one subset among the $2^N - 1$ available subsets such that the chosen subset will satisfy the desired specification (e.g., input offset voltage).

In order to understand the main difference between scaling, redundancy and CR/SES, consider the differential amplifier in Fig. 1. N pairs of input NMOS transistors are labeled as $M1a\backslash M1b$ through $MNa\backslash MNb$. Each pair has its own tail NMOS transistor with gates tied to digital control signals $Sel1$ through $SelN$. Each pair can be turned on or off as desired by

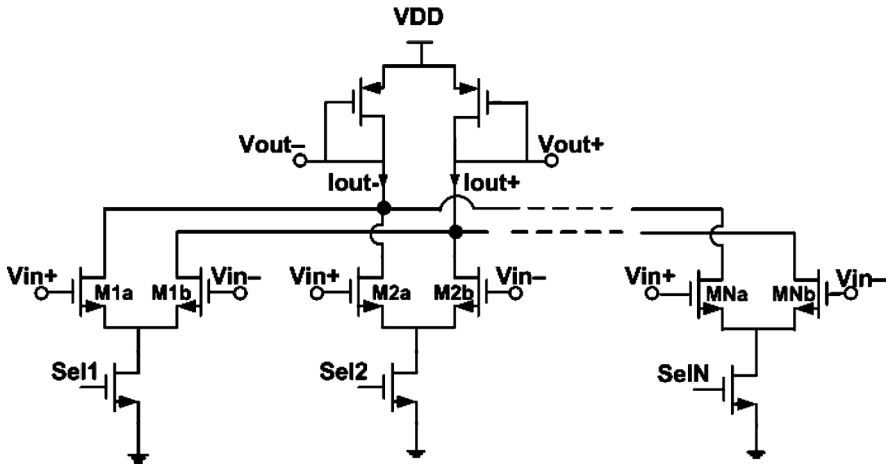

Fig. 1. SES based differential amplifier.

$Sel\langle 1:N\rangle$. Each transistor has different characteristics due to the manufacturing variations, and the mismatches between the pair transistors result in non-ideal effects such as input offset voltage. In *scaling*, all branches from 1 to N are selected. All signals $Sel\langle 1:N\rangle$ are connected to the same line during the design phase. The averaging effect introduced by the selection of all mismatched branches results in a lower amount of effective variation, and yields an improvement of $1/\sqrt{N}$ in matching standard deviation [19]. No calibration is done after manufacturing.

For previous work that has been referred to as *redundancy*, branches are grouped into predetermined identical blocks during the design phase. Only one block can be selected at a time during post-manufacturing calibration. For example, assume that each pair in Fig. 1 forms one block, for a total of N blocks. Among the available N combinations, the one with the best offset specification is selected. If $N/2$ branches form one block, there are only 2 combinations to select from during calibration.

CR/SES is an extension of redundancy. Rather than grouping the branches into predetermined blocks, each pair is allowed to be individually selected. This is essentially a finer grain redundancy that must be carefully designed based on the statistical parameter models and the different methods that can be used for efficient digital selection of the "elements." If a total of $N/2$ pairs is desired, the selection can be made among the $\binom{N}{N/2}$ subsets that can be formed using the control signals. This combinatorial search space is a significantly larger than that for redundancy. If $N = 16$ and 8 pairs form one block, only two blocks are available for selection in redundancy. If any subset of size 8 can be selected (SES), 12870 combinations are available. If the subset size is not constrained to $N/2$, any subset among $2^N - 1$ can be selected. This exponential increase in the number of combinations results in a significant improvement in finding a low offset combination.

Input offset voltage (V_{os}) of the differential amplifier in Fig. 1 is defined as the $V_{in} = V_{in+} - V_{in-}$ at which the output branch currents (I_{out+}, I_{out-}) are equal. If all the transistors in the circuit are perfectly matched, $V_{os} = 0$. In practice, mismatch in threshold voltage (V_{th}) and conductance constant $(\beta = \mu C_{ox}(W/L))$ of transistors result in unequal currents through the branches of the pairs when an equal voltage is applied to both V_{in} terminals. If the input offset of ith input pair is $V_{os,i}$ and the transconductances of all pairs are the same, then the input offset voltage of the differential amplifier is [51]:

$$V_{os} = \frac{1}{N} \times \sum_{i=1}^{N} V_{os,i}. \tag{1}$$

If we consider the case that only a subset of the N pairs is chosen, the resulting input offset voltage is:

$$V_{os} = \frac{1}{\sum_{i=1}^{N} k_i} \times \sum_{i=1}^{N} k_i V_{os,i} \tag{2}$$

where $k_i = 1$ if the ith pair is chosen, and $k_i = 0$ otherwise.

V_{th} mismatch generally dominates β mismatch and we can write $V_{os,i} = \Delta V_{th,i}$ [52]. Systematic sources of variation and gradient variations can be minimized by using a fully symmetrical layout and closely spaced transistors. In addition, if the input transistors are the dominant source of mismatch, the $V_{os,i}$ distribution is centered at 0 and can be estimated as a gaussian normal distribution with $\mathcal{N}(0, {\sigma_{os,i}}^2)$. Using (2), we can determine that the input offset voltage of the amplifier is $\mathcal{N}(0, {\sigma_{os}}^2)$ where $\sigma_{os} = \sigma_{os,i}/\sqrt{\sum_{i=1}^{N} k_i}$. This follows a close resemblance to the result found in [19], where matching of MOS devices in close proximity has been shown to improve by $1/\sqrt{Area}$.

$\sigma_{os,i}$ can be determined from Monte Carlo SPICE simulations for the given circuit. The easiest method to improve matching, and hence achieve a desired input offset specification with an arbitrarily large probability, is to increase the size of input transistors. This could be done by increasing width and/or length of each device or by adding more branches in parallel. Unfortunately, the $1/\sqrt{Area}$ relationship makes "select all" method (*sizing*) very costly in terms of area and power.

For *redundancy*, consider the circuit on Fig. 1 where only one element is selected at a time so that the best selection among N available can be done after manufacturing (N-times redundancy). Statistical Element Selection with Combinatorial Redundancy takes this concept one step further: If designed so

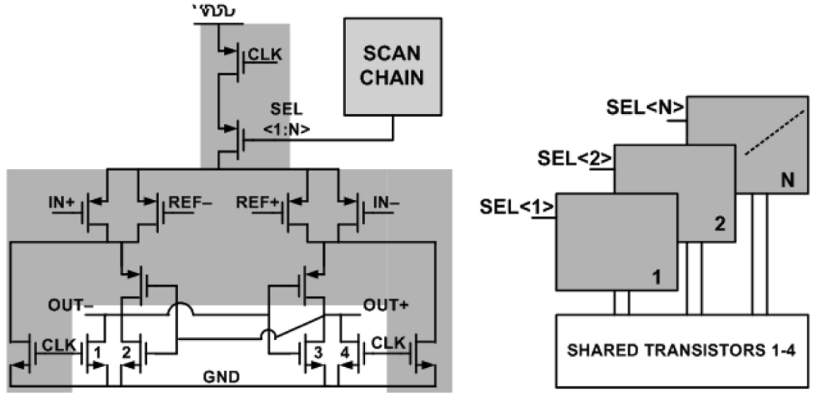

Fig. 2. SES-based latch type comparator.

that any subset among all available elements can be selected, $2^N - 1$ combinations are available. Fig. 2 depicts CR/SES for diff-amp portions of a comparator that is implemented by multiple "elements".

SES can be applied to a variety of circuits other than differential amplifiers (e.g., current mirrors, comparators) where matching is critical. It can also be applied to passive element matching in capacitors and resistors. The main goal in SES is to achieve a target specification such as input offset voltage with arbitrarily high probability (e.g., 99.5%) with lowest possible power and area. The basic parameters to determine are:

- Total number of selectable elements (N)
- The number of elements selected (k)
- Size of each element
- Total number of sets among $\binom{N}{k}$ that will be tried, determining calibration time

Since different circuits and applications require different trade-offs among these parameters, a methodology to determine the values of the basic parameters is needed.

2) Methodology: Fig. 2 shows a latch type SES-based comparator where the dark sections are replicated N times. Each section can individually be turned on or off using digital select signals $(\mathrm{SEL}\langle 1:\mathrm{N}\rangle)$ from an on-chip scan chain or memory. Assume that each selectable element on Fig. 2 has an offset distribution that follows normal $\mathcal{N}(0, \sigma_{os,i})$ and only one element among the N is selected. The probability that this element has an absolute offset smaller than a given specification $spec$ is

$$p_{success} = erf\left(\frac{spec}{\sigma_{os,i} \times \sqrt{2}}\right) = 1 - p_{fail}. \tag{3}$$

p_{fail} denotes the probability that this element will fall out of the given offset specification $(spec)$ and erf is the Gauss error function. To ensure good linearity of the ADC, $spec$ should be less than ± 0.5 LSB. Since the offset of each element is independent, one can calculate the probability that each and every one of the available N elements will fall out of the desired offset specification as

$$p_{fail,total} = (p_{fail})^N. \tag{4}$$

This is a classical example of redundancy with N elements, where only one out of N identical elements can be selected.

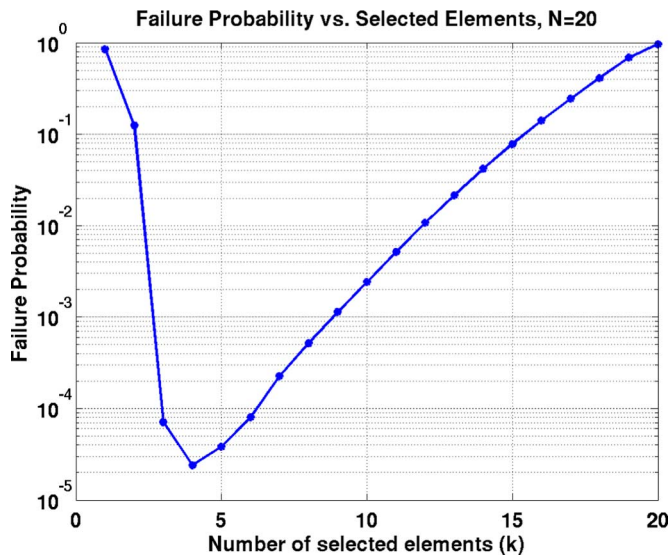

Fig. 3. Failure probability for $N = 20$, $\sigma_{os,i} = 1$, $spec = 10^{-2}$.

If each element fails the specification, post-manufacturing calibration will not be successful. Let us now consider that all N elements are chosen. In this case, the offset distribution follows $\mathcal{N}(0, \sigma_{os,i}/\sqrt{N})$. The probability that the offset is within $spec$ (denoted by $p_{fail,N}$) can be calculated simply by substituting $\sigma_{os,i}$ in (3) with $\sigma_{os} = \sigma_{os,i}/\sqrt{N}$. This is a classical example of Pelgrom type sizing to reduce variability and results in lower failure probability than using only one element.

Redundancy and Pelgrom-type sizing are the two extremes for SES. Rather than selecting one at a time (redundancy), or all at once (sizing), k elements among N are selected at a time $(1 \leq k \leq N)$. Fig. 3, generated using 1×10^6 Monte Carlo samples in MATLAB, shows the failure probability $(p_{fail,total})$ as k is varied when $N = 20$, $\sigma_{os,i} = 1$ and offset specification $(spec)$ is 10^{-2}. In other words, we are trying to achieve an absolute offset less than 1/100th of the standard deviation of each element, a very ambitious target. p_{fail} for each element can be calculated from (3) using $\sigma_{os,i} = 1$ and $spec = 10^{-2}$. The leftmost point in the contour shows the case of redundancy, where we have 20 independent subsets of only one element each $(k = 1)$. The failure probability at this point in the contour can be calculated simply by $p_{fail,total} = (p_{fail})^{20}$. The rightmost

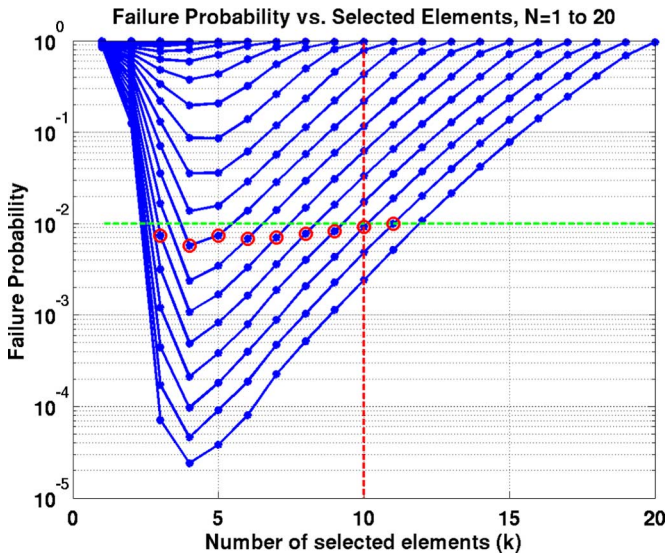

Fig. 4. Failure probability for $N = 1$ to 20, $\sigma_{os,i} = 1$, $spec = 10^{-2}$.

point corresponds to the case where we have only one subset of 20 elements (select all elements, $k = N = 20$). Probability of failure for this subset, p_{fail}, can be calculated from (3) again, with $spec = 10^{-2}$ and $\sigma_{os,i} = 1/\sqrt{20}$; because we know that standard deviation decreases by $1/\sqrt{Area}$. The failure probability at the right end of the contour is simply $p_{fail,total} = p_{fail}$, since there is only one subset of size 20. This point corresponds to Pelgrom-type sizing ($k = N = 20$). Clearly, orders of magnitude of improvement in failure probability is achievable compared to both redundancy and Pelgrom-type sizing if we allow k to be anywhere between these two extremes; i.e., $1 < k < 20$.

Minimum failure probability is observed when $k = 4$; however, this may not be the optimum point when one considers that 16 unused elements are contributing to the parasitics. In the comparator example, this would slow down the circuit. In most cases it is desirable to minimize the number of unused elements, or simply maximize the k/N ratio while achieving the required offset specs.

Fig. 4 shows the plots when both N and k are varied. Each blue contour corresponds to a different N value ($1 < N < 20$), and the x-axis shows how many elements (k) are selected among N ($k \leq N$). As the previous case, each selectable element follows $\mathcal{N}(0,1)$ and $spec = 10^{-2}$. A good way to visualize the improvement in failure probability is to look at a vertical line at a given k (shown for $k = 10$), and determine the intersection points between this line and each contour. We increase N until we reach the failure probability target $p_{fail,total}$ (shown for $p_{fail,total} = 10^{-2}$). In this example, target is reached when $N = 18$. One can select any N above 18, but at the expense of increasing the number of unused elements. Fig. 4 helps us answer the following question: Given a fixed element size ($\mu_{element} = 0$ and $\sigma_{element} = 1$) and an offset specification ($spec = 10^{-2}$ for Fig. 4), what are the possible (N, k) pairs that will satisfy a given failure probability specification $p_{fail,total}$? A MATLAB script can search through the data, find the appropriate (N, k) pairs, and produce the highest k/N ratio for each k. In Fig. 4, these points have been marked

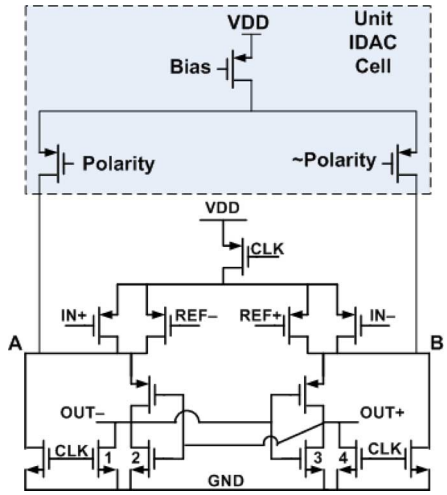

Fig. 5. IDAC calibrated comparator.

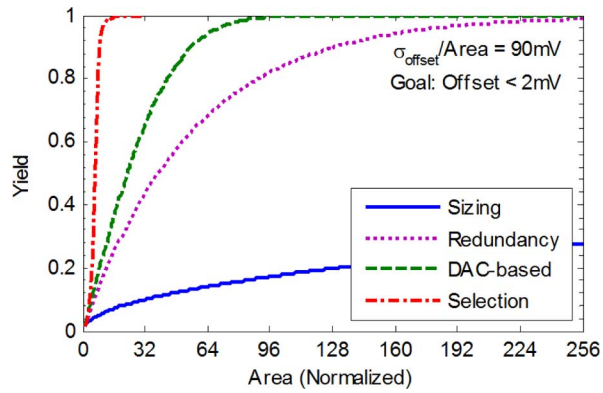

Fig. 6. Comparison of SES, redundancy, scaling and DAC based calibration.

with circles for each k where the $p_{fail,total}$ specification can be met. Although not fully monotonic due to the discrete nature of the problem, we observe higher k/N ratios as k increases. In other words, red circles to the right have, in general, better utilization of elements compared to the ones on the left. It should be noted that any deviation from monotonicity with increasing k is small.

DAC-based calibration could be implemented with low overhead by adding a thermometer-coded IDAC tapping into the A and B nodes (Fig. 5). The injected current changes the offset voltage. Each unit cell consists of three near-minimum size transistors: two switches to control polarity and a current source. The yield for DAC-based calibration is

$$p_{success} = erf\left(\frac{spec + LSB_{DAC} \times (2^{n-1} - 1)}{\sigma_{os,i} \times \sqrt{2}}\right) \quad (5)$$

where $spec$ is the target offset, LSB_{DAC} is the calibration step size, and n is the DAC resolution. $LSB_{DAC} = LSB_{ADC}/3$, as discussed in [44]. Fig. 6 shows a comparison of these methods as N (normalized area unit) is varied. Each selectable element offset is assumed to follow a normal distribution $\mathcal{N}(0, 90\text{ mV})$ with $spec = 2$ mV. Only half of all elements are allowed to be selected for CR/SES ($k = N/2$). For redundancy, each element forms one block (N redundant blocks). The yield for CR/SES is found by MATLAB Monte Carlo simulation (10,000 samples);

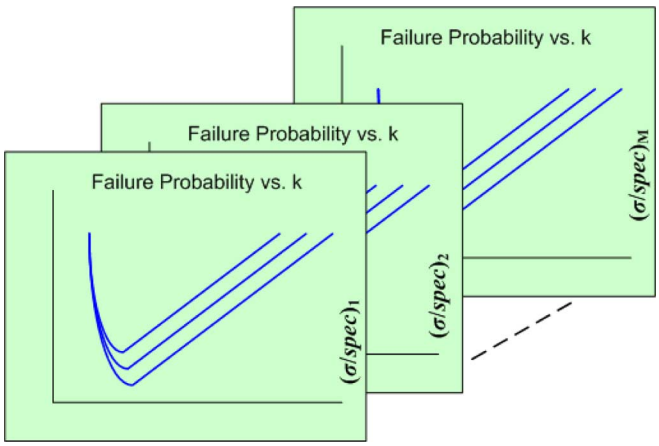

Fig. 7. Decision cube.

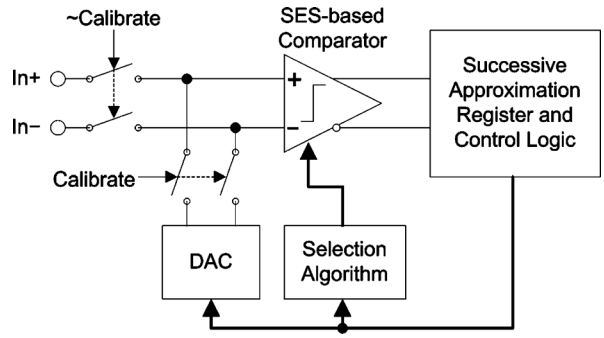

Fig. 8. On-chip calibration architecture for SES-based comparators.

all others are calculated from their yield equations. Dramatic improvement in success probability can be seen with CR/SES compared to the other methods.

Although the previous scenario is informative, it might not be completely realistic. In most cases, designers are not restricted to choose a fixed element size; they can choose among fewer but larger elements (e.g., $\mu_{element} = 0$, $\sigma_{element} = \sigma_{os,i} < 1$). For the comparator example, assume that all transistors in the replicated section have a minimum length (L). Consider the following two cases:

- Case 1: N_1 total elements; in each element, all the transistors have width W_1, giving a standard deviation of σ_1. We are selecting k_1 elements among N_1.
- Case 2: N_2 total elements; in each element, all the transistors have width W_2, giving a standard deviation of σ_2. We are selecting k_2 elements among N_2.

For a fair comparison, assume that the total area in two cases is the same, i.e., $N_1 \times W_1 = N_2 \times W_2$, ignoring routing area and the storage for configuration bits. We want to determine which case has better resource utilization (has higher k/N ratio). In order to achieve this goal, we first regenerate the plot in Fig. 4 for different $\sigma_{element}/spec$ ratios to normalize it to $spec$. Fig. 7 shows these individual plots forming the slices of a "decision cube." Using the decision cube, the designer can evaluate tradeoffs between differing element sizes for a given $spec$. Each slice of the cube corresponds to a different element size. The decision cube is built only once for a predetermined range of (normalized) $\sigma_{element}/spec$ ratios (where $spec$ is the offset specification). Each $\sigma_{element}/spec$ plot forms one slice of the cube. The same cube can be used for different designs with different resolutions or process technologies. In most practical applications, desired $\sigma_{element}/spec$ ratios would be from 10^{-1} to 10^{-3}. An arbitrary number of slices can be formed between these points, but 100 slices are generally enough to converge on a decision of (N, k, σ) triplets that will satisfy the failure probability $(p_{fail,total})$ target. A simple design recipe is:

1) Specify the offset specification $spec$.
2) Specify the failure probability target $p_{fail,total}$ for each comparator. For example, if we would like to find a configuration that will satisfy the spec 99.5% of the time, $p_{fail,total} = 5 \times 10^{-3}$.
3) Specify the offset standard deviation $(\sigma_{element,i})$ for each type of selectable element. For example, assume that the basic selectable element is a single transistor. The first selectable element type could be a transistor with width W_1 with standard deviation $\sigma_{element1}$, and the second selectable element type could be W_2 with standard deviation $\sigma_{element2}$. These values can be determined by running circuit simulations for the design in the given process technology.
4) Calculate the ratio $\sigma_{element,i}/spec$ for each selectable element type.
5) Input the results in steps 2 and 4 to a MATLAB script. For each selectable element type $(\sigma_{element,i})$, the script will produce all the (N, k) pairs that will satisfy the requirements in steps 1 and 2 using the cube in Fig. 7. Since the decision cube is pre-built, this is an efficient process step.
6) Now choose between the $(N, k, \sigma_{element,i})$ triplets that satisfy the requirements in steps 1 and 2 for the specific application. We have observed that in many cases, selecting half the total available elements $(k = N/2)$ results in a good trade-off between resource utilization and the number of configuration bits.

The decision cube in Fig. 7 assumes that all available subsets are searched for a given set of N elements. If there is enough processing power available to perform an intelligent search, it is possible to search through all $2^N - 1$ available combinations. An easier but less optimal option is a greedy search, where random combinations are uploaded to the differential amplifier until a successful combination is found. We can limit the number of trials to ensure that calibration time is not very long at the expense of a lower probability of finding a good combination. The maximum allowable trials can be added as a fourth dimension to the decision cube on Fig. 7, allowing the designer to evaluate the calibration time trade-off in addition to the $(N, k, \sigma_{element})$ triplets.

3) On-Chip Calibration: SES is ideally performed with on-chip calibration. On-chip calibration allows periodic recalibration, allowing one to overcome slow changes in offset due to temperature or aging. A general architecture for on-chip calibration is shown in Fig. 8. The same binary search principle as a SAR ADC is used to measure the comparator's offset for each subset of elements. The selection algorithm controls the search for the optimal subset. The cost of the on-chip calibration circuitry varies with the choice of selection algorithm. The

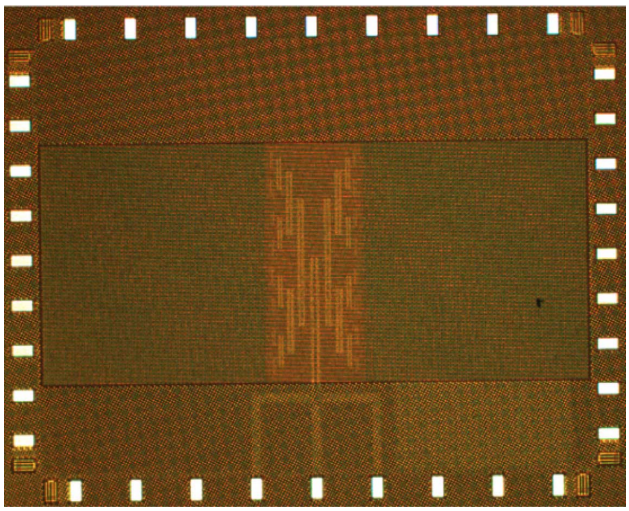

Fig. 9. Die photo of 65 nm test chip.

selection algorithm can be exhaustive or greedy and the DAC measurements high- or low-resolution. These choices affect search time, implementation cost, and solution quality.

III. Comparator Array Test Chip

A. Test Chip Architecture

A test chip consisting of comparators in 65 nm bulk CMOS was designed and fabricated in order to verify the modeling results. The comparator in Fig. 2 with 32 selectable elements has been used as the basic building block, out of which 16 are chosen. There are 32 flip-flops for each comparator to store the desired configuration. Flip-flops for all the comparators are connected in a scan chain to scan in the configuration bits from off-chip. Selection is performed only on the comparators and the following circuits do not incorporate any reconfigurability. Each die includes 255 comparators, intended to be used for an 8-bit ADC (Fig. 9). The architecture of the test chip and the timing diagram for calibration is given in Fig. 10. The number of available selectable elements, the subset size and the size of each element have been determined by using the methodology in the previous section. Maximum allowed calibration steps per comparator is chosen as 10,000. The full scale range (FSR) of the intended 8-bit ADC is 1 V differential peak-to-peak, giving a least significant bit (LSB) of 3.9 mV. A comparator is defined as "within the specification" if at least one combination among the 10,000 steps results in an input offset voltage amplitude smaller than 0.5 LSB. The design point is chosen so that all 255 comparators will be within the specification with 99.5% probability. During the design of the comparator, transistors in the shared block are sized such that their effect on the overall offset is much smaller than the replicated transistors. The offset distribution of the comparator was obtained by running a Monte Carlo simulation during the design phase. Threshold voltage mismatch in the input transistors ($\Delta V_{th,in}$) and the shared transistors ($\Delta V_{th,shared}$) were noted for each run. Using an approach similar to [4], a linear offset model was built from the Monte Carlo simulation results:

$$Offset = (a \times \Delta V_{th,in}) + (b \times \Delta V_{th,shared}). \quad (6)$$

The sizes of the transistors in the replicated section are increased until their effect on the offset is much smaller than the input transistors ($b \ll a$). The total width of the shared transistors is comparable to the sum of the widths of the replicated transistors.

There are $8160 (= 255 \times 32)$ select flip-flops that store the configuration bits for the 255 comparators. The differential output (2 bits) of each comparator is stored in 2 scan flip-flops, yielding a total of 510 output scan flip-flops. In order to find the input offset of each comparator, the timing diagram on Fig. 10 needs to be examined. In region 1, configuration bits are scanned into the select flip-flops by using Scan In input and running Select Clk. Scan Enable is held low during this period. After all the selection bits are scanned in, Core Clk for the latch type comparator is run a few times to allow the outputs of the comparators to settle and clear any metastability in the latches (region 2). Comparator outputs are then loaded to the output scan flip-flops, which are subsequently put into scan mode by raising Scan Enable (region 3). The differential output for each comparator is then read from Scan Out by toggling Scan Clk. The inputs ($V_{in\pm}$) are swept in small steps and the outputs of the comparators are read for about 50 times through the output scan chain. At each input step, the number of times that each comparator outputs a value of 1 is noted. The input voltage vs. number of 1's curve is then fitted to a Gaussian cumulative distribution function, whose mean is used as the input offset voltage of the comparator for the given configuration.

B. Test Setup

The test setup for the measurements is shown on Fig. 11. The setup is automated using built-in MATLAB toolboxes on the PC. Keithley 2400 sourcemeters with high precision are used for input voltages, and Agilent E3648A DC sources are used to supply the power to the core, I/Os, and the voltage references for the resistor ladder on the die. Core power supply is set at 0.8 V and both ends of the resistor ladder are set at 0.4 V. The chip is bonded in a QFN package and connected to a PC board using a compatible socket. Using the test socket, packaged die can be changed easily for statistical data collection. Only a maximum of 10,000 calibration steps per comparator is allowed among more than 600×10^6 available combinations for each comparator. Since it is not possible to go through each of the 10,000 combinations per comparator due to measurement time constraints, the following method is applied to find the best sets:

1) Randomly determine 10,000 subsets of size $k = 16$ that each comparator can be configured to. These are the same for all comparators.
2) Determine a number of these subsets (X among 10,000) to be loaded to each comparator. Store these subsets in a selection matrix:

$$Sel_{X\times N} = \begin{pmatrix} S_{1,1} & S_{1,2} & \cdots & S_{1,N} \\ S_{2,1} & S_{2,2} & \cdots & S_{2,N} \\ \vdots & \vdots & \ddots & \vdots \\ S_{X,1} & S_{X,2} & \cdots & S_{X,N} \end{pmatrix}.$$

Each row of the matrix contains the configuration bits for each of the $N = 32$ elements. If element e of subset s is selected, $S_{s,e} = 1$, and 0 otherwise. The sum of each row is $k = 16$.

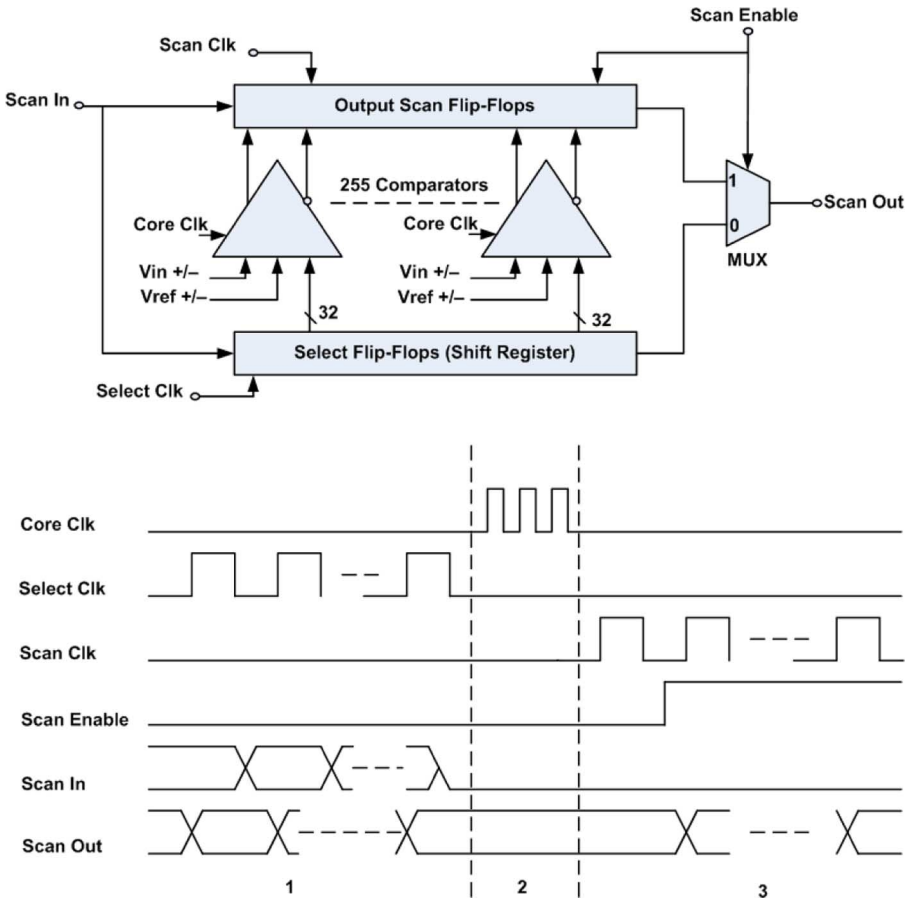

Fig. 10. Comparator array test chip architecture.

3) Measure the offset of each subset in the selection matrix and store it in a measured offset vector:

$$MO_{X\times 1} = \begin{pmatrix} mo_1 \\ mo_2 \\ \vdots \\ mo_X \end{pmatrix}$$

4) Find the estimated offset of each element in each comparator using the least squares solution in MATLAB:

$$IO_{N\times 1} = \frac{1}{k} \cdot (Sel_{X\times N})^{-1} \cdot MO_{X\times 1} \tag{7}$$

5) Using the estimated offsets of each element, in MATLAB find the T best subsets among the subsets that are predicted to have less than 0.5 LSB offset.
6) Upload the T subsets for each comparator to the test chip, and record the measured offset for each trial. For each comparator, select the subset that gives the lowest measured offset.

One can select the number of training sets (X) greater than the number of unknown variables (N) to build a linear model approximating the response. Although the linear model has error associated with it, X can be increased to build a more robust fit. Furthermore, using T best guess combinations for each comparator greatly increases the probability of finding a good combination.

C. Measurement Results

Comparator offsets from 13 different die (3315 comparators) were measured and calibrated using the methodology described above. We used $X = 100$, $T = 20$ for $N = 32$ elements. Measurements show that over 85% of the tested best guesses satisfy the specification. Using this result, the probability that all 20 guesses will fail for one comparator is $(1\text{–}0.85)^{20}$ $(< 10^{-12})$, verifying that the offset estimation procedure outlined in the previous section is practically feasible.

Fig. 12 shows the histograms before and after SES has been applied to the comparators. The top plot shows the offset histogram when all 32 laid out elements are turned on (no selection). The bottom plot shows the resulting histogram after SES has been applied to find the best subset among 10,000 allowable for each comparator. Subset size is $k = 16$. Close to two orders of magnitude is improvement in σ_{offset} is observed, from 11.21 mV to 0.35 mV. Fig. 13 shows the histograms for 2X and 4X redundancy as applied to the comparators. For 2X redundancy, 32 elements in each comparator are divided into two blocks of 16 (the first 16, and the last 16). The block with the lower offset is selected. For 4X redundancy, 32 elements are divided into four blocks of 8 elements, and the lowest offset combination among the 4 is selected. Although improvement is observed compared to select all (32/32), it is less effective than combinatorial redundancy in terms of performance. Redundancy results are collected from a smaller test sample of 5 die (1275 comparators).

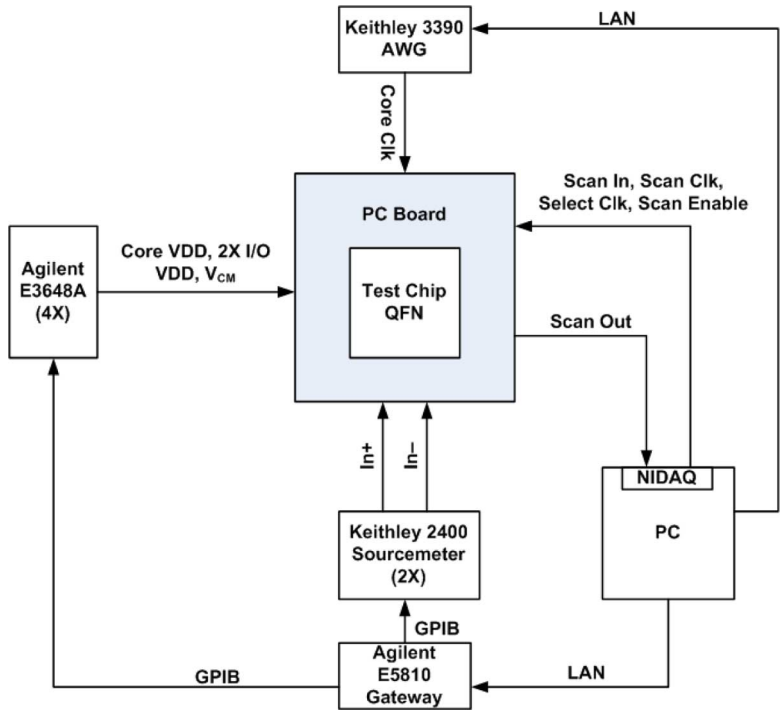

Fig. 11. Measurement setup.

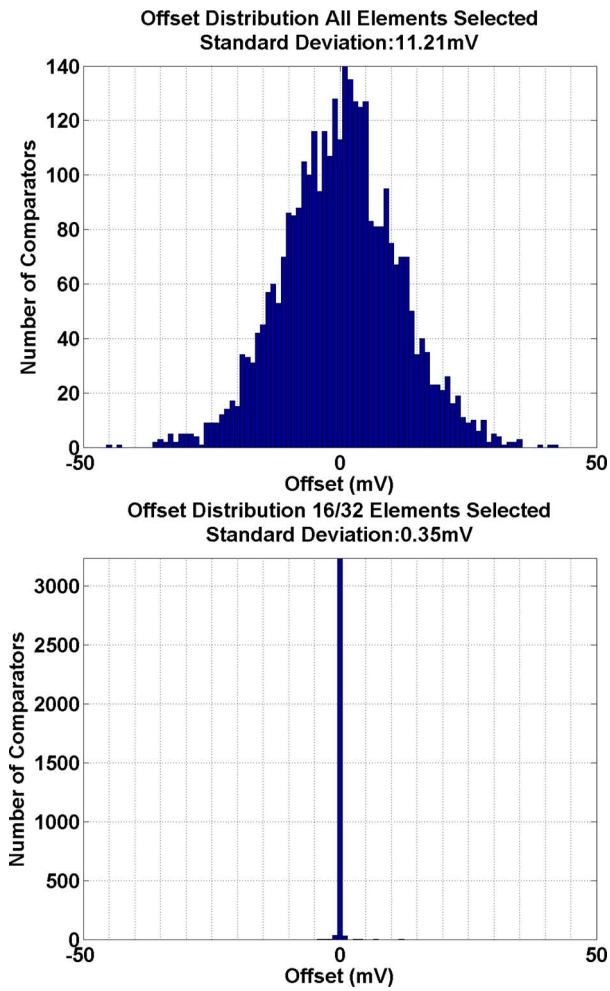

Fig. 12. Measured offset histograms before and after SES (3315 comparators).

Success probability, defined as the number of comparators that have less than ± 0.5 LSB offset, is 15% for "select all"(32/32). Success probability for 2X and 4X redundancy is 25% and 28%, respectively. SES gets 99.5% success for select 16 over 32 as expected by modeling.

Fig. 14 shows the SES success probability and 95% confidence intervals as N is varied from 16 to 32. $k = N/2$ for each N. Number of tested comparators is 3315. Success probability increases almost monotonically with increasing N, and above 98% success is observed for all cases. Fig. 15 compares the measured and MATLAB-simulated σ_{offset} values when selecting 1 to 14 of 14 elements. The 32 elements were grouped into 16 pairs, of which 14 pairs were selectable (switched on and off as a pair) and the remaining 2 disabled. 255 comparators on 1 chip were measured. The MATLAB-simulated σ_{offset} values are scaled to match the measured value for 14 choose 14. Measurement and simulation largely agree when selecting 1 element and 7 to 14 elements. Discrepancies are noted when selecting between 2 and 6 elements, likely due to measurement inaccuracy for $|V_{offset}| \ll 1$ mV, high kurtosis, and small sample size. The measurement results experimentally verify the MATLAB Monte Carlo simulation results.

IV. 8-bit Flash ADC

A. Comparator Design

Based on the results from the first test chip, an 8-bit flash ADC was designed in the same process using a slightly different comparator. The new comparator is a pseudodifferential NMOS-input latch-based dynamic comparator (Fig. 16). The design was chosen primarily to reduce kickback from the comparator (a major concern for the 8-bit flash ADC for which this comparator was designed) at the expense of poor common mode

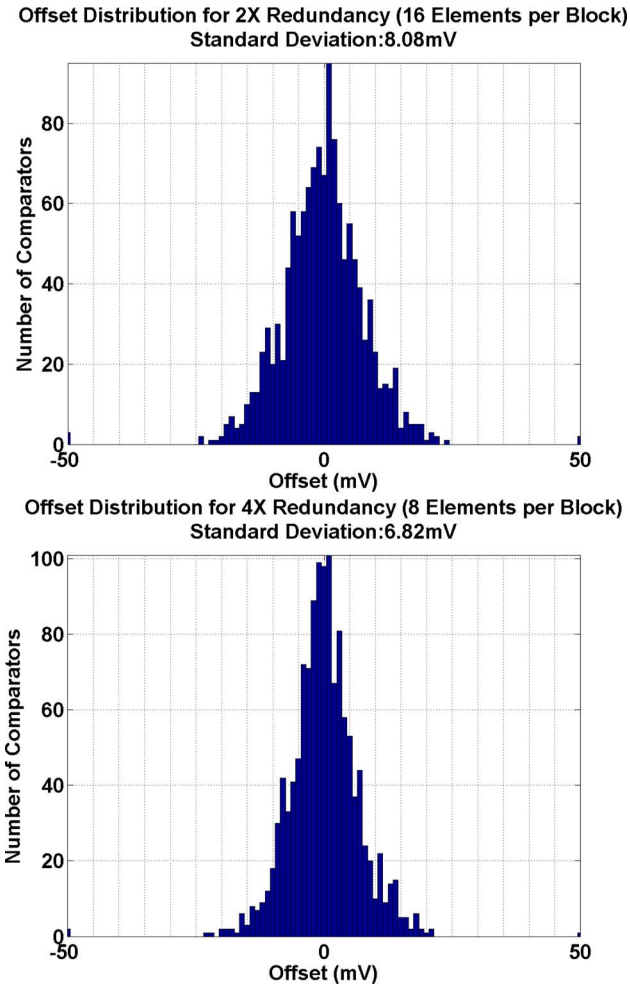

Fig. 13. Measured offset histograms for redundancy (1275 comparators).

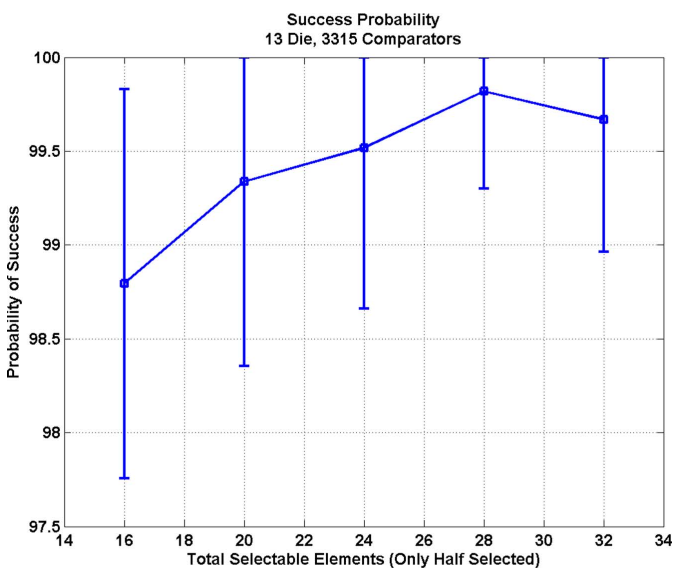

Fig. 14. Measured Success Probability for SES, $N = 16$ to 32 (3315 Comparators).

and power supply rejection. Identical copies of transistors M1 to M4 (the dominant sources of offset) are connected in parallel, each branch forming a selectable element. M15 and M16 are

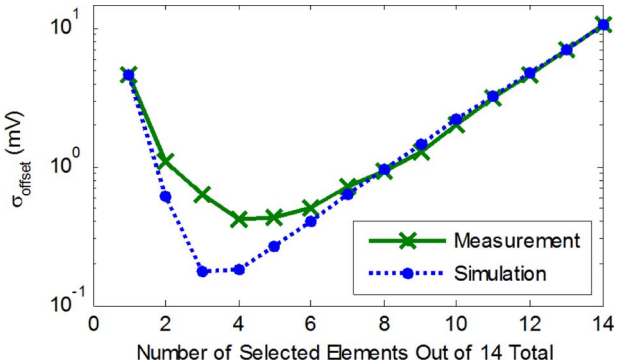

Fig. 15. Measured Offset Standard Deviation Contour, $N = 14$ (255 comparators).

added to select/deselect elements by the Select signals. M5 to M14 are shared, as they have the least effect on offset in simulation. All transistors in the selectable elements (M1 to M4, M15, and M16) have minimum length. Widths are slightly larger than the minimum available by the process to optimize the manufacturability of the design. Other transistors (i.e., M5 to M14) are sized to balance speed and power while minimizing their contributions to offset.

Clock-to-Q delay of the comparators (related to the latching time constant) is measured in transient simulations to ensure that latching time of the comparators is sufficient for 1.5 GS/s operation. The unselected elements in comparator design 2 have little effect on power or speed: in pre-layout simulation, removing the unused elements changes the clock-to-Q delay and the power by less than 1%. The precharged nodes have no additional capacitance from the unused elements, keeping the dynamic power consumption equal to the standard design. The comparison time is primarily controlled by the pulldown current, which is set by the sizing of M1 to M4 in the standard comparator or by the number of selected elements in the SES-based comparator.

Comparator design 2 is designed as 16 choose 5 elements to achieve very low offset with minimal area and a reasonable balance of speed and power. As a consequence of the small size of input transistors (M1–M4), estimated individual element $\sigma_{offset} = 92$ mV. Combinatorial redundancy meets tight offset specifications even with extremely small devices, and helps limit the amount of input parasitic capacitance due to the unused branches. A major advantage of this topology is the drastically reduced kickback into the ADC input and the reference ladder. Drain voltages of the unused pairs do not swing during normal operation, and the kickback due to the parasitic gate to drain capacitance of input transistors in unused pairs is not significant. After SES, the simulated yield is $> 99.9\%$ for offset < 2 mV and $\sigma_{offset} = 0.3$ mV. The comparator occupies 22.84 μm $\times$ 7.48 μm and the memory (scan chain flip-flops) occupies 43.25 μm $\times$ 4.7 μm.

B. Noise Implications of CR/SES Based Design

Statistical selection facilitates significant improvements in offset, thereby making the thermal noise an important, even limiting factor in comparator performance. In [52], it is demonstrated that CMOS device mismatch imposes a minimal power limit that is typically 1 to 2 orders of magnitude greater than the

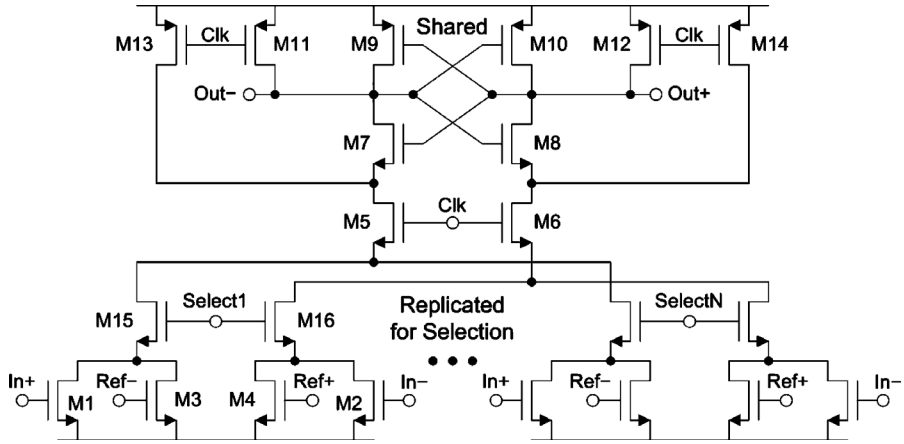

Fig. 16. NMOS-input comparator.

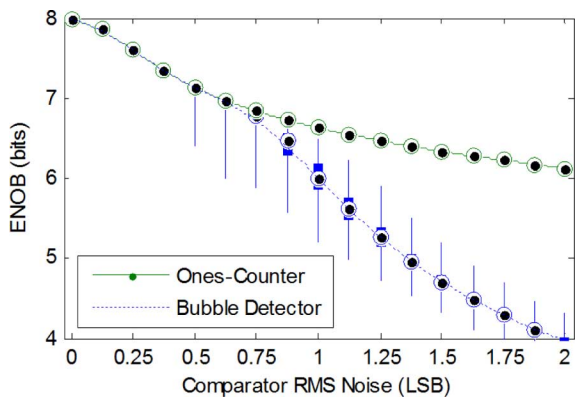

Fig. 17. Comparator RMS noise v. ENOB for 8-bit flash ADC.

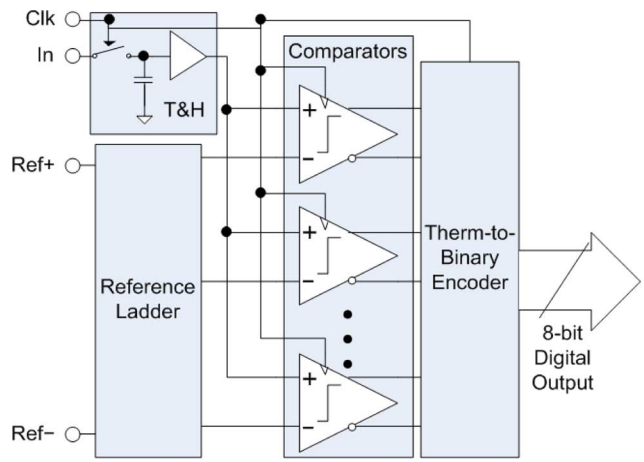

Fig. 18. 8-bit flash ADC test chip architecture.

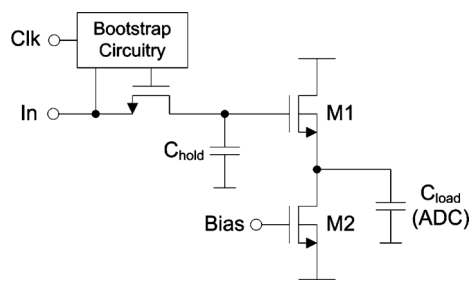

Fig. 19. Front-end track-and-hold.

limit imposed by thermal noise. For example, moving from a random set of 5 elements to the best subset of 5 from 16 improves offset by a factor of 150. This improvement in offset causes the comparator to approach the thermal noise minimal power limit. Comparators using DAC-based calibration have also been reported to encounter thermal noise limitations [53], [54]. An analysis of the thermal noise of dynamic comparators is found in [55].

Monte Carlo simulation in MATLAB (10,000 samples) was used to analyze the effect of comparator thermal noise on the ENOB of flash ADCs. Two thermometer-to-binary encoders were simulated: a bubble detector encoder [56] and an ones-counter encoder [57]. Fig. 17 shows the results. A box plot depicts the median (dots), 25% to 75% range (filled box), and maximum and minimum data points (whiskers). A spline fit approximates the average ENOB (lines). The thermometer-to-binary encoder plays a significant role in the comparator noise tolerance of flash ADCs. The ENOB of the ones-counter encoder degrades gracefully in the face of comparator noise. The ENOB of the bubble detector encoder degrades gracefully until the RMS noise exceeds 0.5 LSB, at which point the probability of multiple noise-induced bubbles becomes large and glitches occur in the output code. For RMS noise levels above 0.5 LSB, a noise-robust encoder (e.g., ones-counter) is necessary to avoid severe losses in the ENOB.

C. Architecture

Fig. 18 shows the flash ADC architecture, depicted as single-ended for clarity. The front-end T&H minimizes sampling time errors caused by clock and input distribution skew. The reference ladder is a resistor ladder. 255 SES-based comparators of design 2 convert the sampled analog signal to digital thermometer code. The thermometer-to-binary encoder provides the 8-bit output. Selection was performed using scan chains similar to Fig. 10. The T&H consists of a bootstrapped NMOS switch, a hold capacitor, and a well-tied NMOS source follower buffer (Fig. 19). Two copies of the T&H are used pseudodifferentially. The bootstrap switch design is from [58]. The bootstrapped switch provides

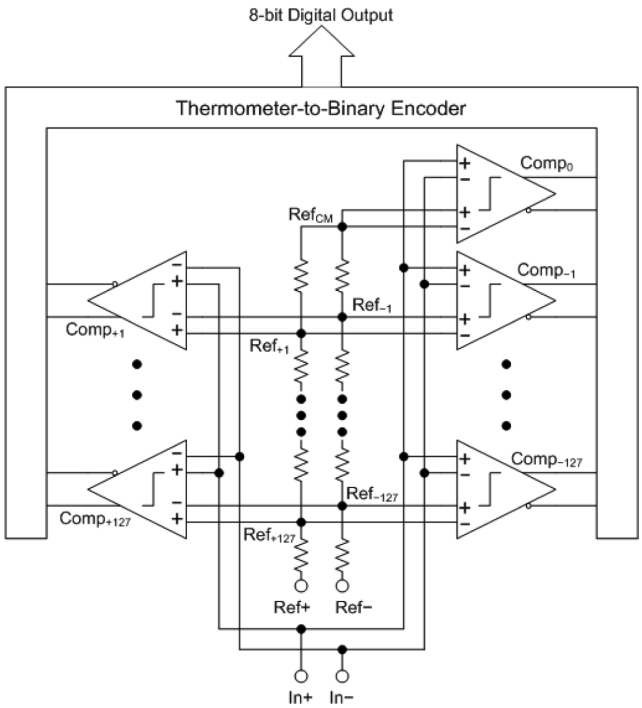

Fig. 20. Reference ladder, comparators, and thermometer-to-binary encoder.

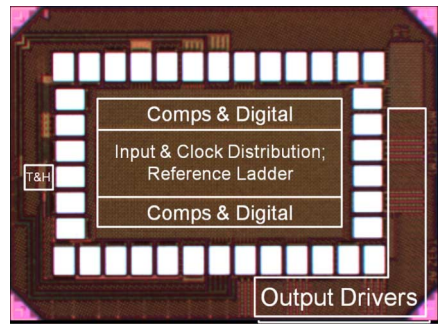

Fig. 21. 8-bit flash ADC die photomicrograph.

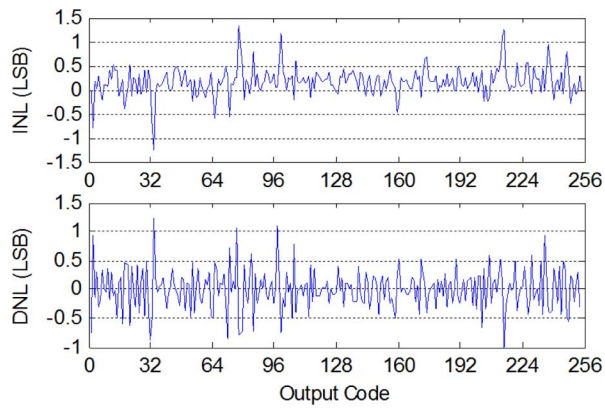

Fig. 22. INL and DNL after selection.

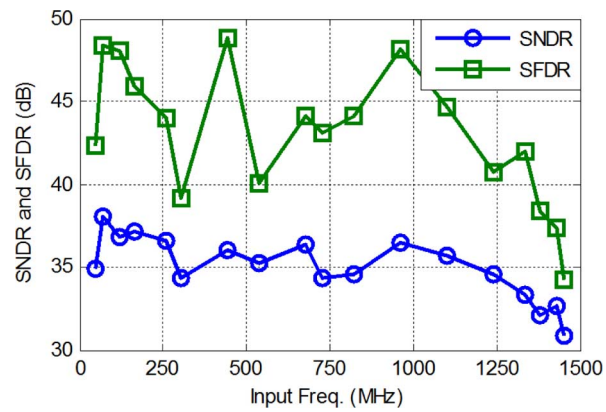

Fig. 23. SNDR and SFDR v. input frequency at 1.5 GS/s.

constant-V_{GS} when sampling, avoiding distortion caused by input-dependent charge injection. A well-tied NMOS source follower was chosen for simplicity and ability to meet the $>$ 8-bit distortion requirement. Fig. 20 shows the reference ladder, comparators, and thermometer-to-binary encoder. The reference ladder is a single string of polysilicon resistors, folded once. The fold ensures that any distortion in the reference voltages becomes a third-order distortion in the ADC transfer function. The ladder's total resistance is 384 Ω and each node has $\geq$ 50 fF decoupling capacitance. The CR/SES-based comparators are design 2 with 16 choose 5 elements. To determine the effect of the post-SES offset distribution on the ENOB performance of an ADC, Monte Carlo simulations were conducted in MATLAB using a model of the 8-bit flash ADC. A total of 10,000 ADCs with 255 uniquely generated comparator offsets were simulated. Provided that the thermometer-to-binary encoder can gracefully handle individual high-offset comparators ($|V_{offset}| > 2$ mV), the ENOB remains above 7.5 bits.

The thermometer-to-binary encoder design is two-stage, first the bubble detector from [56] followed by an OR-gate one-hot-to-binary encoder. The bubble detector was chosen because it is lower cost than more complex encoders—such as the ones-counter—and accommodates individual high-offset comparators with a maximum error of 1 LSB. The bubble detector works well with the distribution of offsets after selection but fails when confronted with high comparator noise.

D. Measurement Results

The 8-bit flash ADC is fabricated in 65 nm digital CMOS and occupies an area of 0.5 mm^2, excluding I/O and decoupling (Fig. 21). The T&H occupies 2.4%, comparators 10%, input and clock distribution 12%, thermometer-to-binary encoder 12%, configuration memory 18%, and reference ladder 45% of the area. Comparator design 2 was used with 16 choose 5 elements. Probe testing was conducted at 1.5 GS/s and 1 V VDD on a typical, randomly selected chip. The sampling rate was limited by a MSB glitch at sampling rates $>$ 1.5 GS/s. The FSR is 1.06 V_{ppd}. The total power consumption (excluding I/O) is 35 mW, the T&H using 20 mW and the ADC core (comparators, clock distribution, and thermometer-to-binary encoder) 15 mW.

After selection, the INL is 1.32 LSB and the DNL is 1.23 LSB (Fig. 22). 232 of 255 comparators (91%) have offset $<$0.5 LSB. The comparator yield is slightly lower than expected and may be due to error from comparator noise and the least squares estimation. For offset $<$1 LSB, the yield is 250 of 255 comparators (98%). One comparator has a very large offset resulting in a missing code. The ADC is monotonic. Fig. 23 shows the

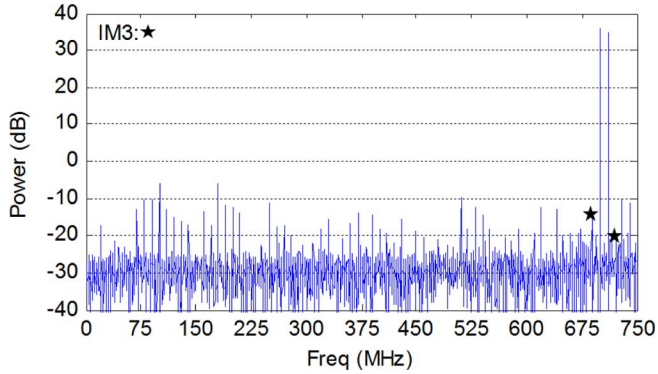

Fig. 24. FFT plot of two tone IP3 test.

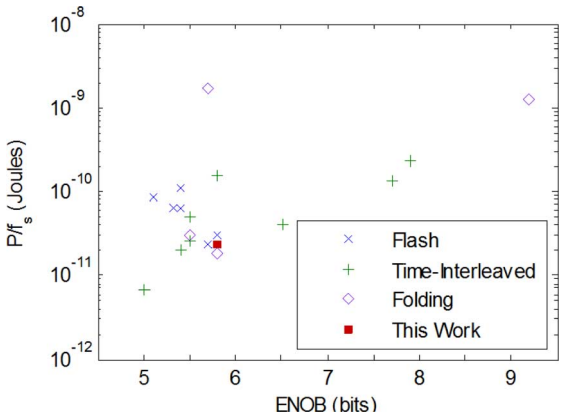

Fig. 25. Comparison of ≥ 1 GHz, ≥ 5-bit ENOB ADCs published 2007-2010 for ENOB v. power/sampling rate.

measured SNDR and SFDR vs. input frequency at 1.5 GS/s. The SNDR is 37 dB at low frequency, corresponding to 5.8 bits ENOB. Average comparator noise is 5 mV rms (1.3 LSB), significantly degrading SNDR. The ERBW is 1.3 GHz. The SFDR is 43 dB at Nyquist. A MATLAB model of the ADC using the measured comparator offsets predicts $\mathrm{SNDR} = 46.9$ dB and $\mathrm{ENOB} = 7.5$ bits without comparator noise. From the model and the previous noise simulations, the comparator noise is responsible for a loss in ENOB of approximately 1.7 bits.

Fig. 24 is an FFT plot of a two tone IP3 test. The input tones are 700 MHz and 710 MHz, each at half the full-scale input power. The IM3 tones are -50 dBc. The IIP3 is 23.5 dBm. A commonly used figure of merit (FoM) is

$$FoM = \frac{P}{2^{ENOB} \times \min(f_s, 2 \times ERBW)} \tag{8}$$

where P is power, ENOB is the effective number of bits for low-frequency inputs, f_s is the sampling rate, and ERBW is the effective resolution bandwidth [29], [46]. To avoid overstating the capabilities of the ADC, $\min(f_s, 2 \times ERBW)$ is used. The FoM is 0.42 pJ/conv.

Fig. 25 compares this work to other recently-published ≥ 1 GHz flash ADCs for ENOB v. P/f_s (suggested by [38]) [22], [26]–[29], [31], [41]–[43], [46], [47], [59]–[64]. This work has comparable performance to state-of-the-art averaging, interpolating, and folding flash ADCs despite having a basic flash ADC architecture. In addition, the nearest flash ADCs on Fig. 25 are 6-bit converters, while this design is an 8-bit converter. Scaling this work to 6-bit would decrease the power by a factor of 4 while maintaining a similar noise-limited ENOB. The limiting factors on the performance of this ADC are the comparator noise and the T&H power consumption. The comparator noise severely limits the ENOB and can be improved by redesigning the comparator (likely increasing power consumption as well). A noise-robust thermometer-to-binary encoder can improve the ENOB by approximately 0.8 bits without changing the comparator noise. The T&H is a simple, power-hungry design and more complex designs have been proposed with the potential of reduced power [60]. As the T&H consumes 57% of the total power, a significant improvement in power is possible.

V. Conclusions

This work presents a digital calibration methodology based on statistical element selection to exploit combinatorial redundancy. It was demonstrated for comparator offset calibration in flash ADCs. CR/SES exploits selection among randomly varying circuit elements to achieve precise tuning. Monte Carlo simulation of CR/SES demonstrates multiple orders of magnitude of improvement in σ_{offset}. Compared to DAC-based calibration and redundancy, the yield of CR/SES improves considerably faster with respect to area.

Two test chips were implemented in 65 nm digital bulk CMOS. Measurement results from the first design verify the Monte Carlo simulation results and demonstrate improvements in σ_{offset} (11 mV to 0.3 mV) and yield (15% to 99.5%).

An 8-bit 1.5 GS/s flash ADC in 65 nm CMOS was designed and fabricated using a CR/SES-based comparators. After SES, 91% of the comparators have offset <0.5 LSB and 98% have offset <1 LSB. The FoM is 0.42 pJ/conv. The performance and power efficiency are limited by the comparator noise and the T&H power consumption. CR/SES for offset calibration in flash ADCs and other applications can reduce mismatch to the point where noise becomes the primary concern.

Acknowledgment

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References

[1] M. Jeong *et al.*, "A 65 nm CMOS low-power small-size multistandard, multiband mobile broadcasting receiver SoC," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2010, pp. 460–461.

[2] C. Lee *et al.*, "A multistandard, multiband SoC with integrated BT, FM, WLAN radios and integrated power amplifier," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2010, pp. 454–455.

[3] X. Li, B. Taylor, Y. Chien, and L. T. Pileggi, "Adaptive post-silicon tuning for analog circuits: Concept, analysis and optimization," in *IEEE Int. Conf. Comput.-Aided Des. Dig. Tech. Papers*, Nov. 2007, pp. 450–457.

[4] L. Pileggi *et al.*, "Mismatch analysis and statistical design at 65 nm and below," in *Proc. IEEE Custom Integrated Circuits Conf.*, Sep. 2008, pp. 9–12.

[5] G. Keskin, J. Proesel, and L. Pileggi, "Statistical modeling and post manufacturing configuration for scaled analog CMOS," in *Proc. IEEE Custom Integrated Circuits Conf.*, Sep. 2010, pp. 1–4.

[6] J. Proesel, G. Keskin, J.-O. Plouchart, and L. Pileggi, "An 8-bit 1.5 GS/s flash ADC using post-manufacturing statistical selection," in *Proc. IEEE Custom Integrated Circuits Conf.*, Sep. 2010, pp. 1–4.

[7] K. Agarwal and S. Nassif, "Characterizing process variation in nanometer CMOS," in *Proc. ACM/IEEE Design Automation Conf.*, Jun. 2007, pp. 396–399.

[8] G. Scott *et al.*, "NMOS drive current reduction caused by transistor layout and trench isolation induced stress," in *IEEE Int. Electron Devices Meeting (IEDM) Dig. Tech. Papers*, Dec. 1999, pp. 827–830.

[9] H. Fukutome *et al.*, "Carrier profile designing to suppress systematic V_{th} variation related with device layout by controlling STI-enhanced dopant diffusions correlated with point defects," in *IEEE Int. Electron Devices Meeting (IEDM) Dig.*, Dec. 2009, pp. 53–56.

[10] P. Gupta and F.-L. Heng, "Toward a systematic-variation aware timing methodology," in *ACM/IEEE Design Automation Conf. Dig. Tech. Papers*, Jun. 2004, pp. 321–326.

[11] C. Webb, "45 nm design for manufacturing," *Intel Technology J.*, vol. 12, pp. 121–130, Jun. 2008.

[12] T. Jhaveri *et al.*, "Co-optimization of circuits, layout and lithography for predictive technology scaling beyond gratings," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 29, no. 4, pp. 509–527, Apr. 2010.

[13] J. T. Watt and J. D. Plummer, "Dispersion of MOS capacitance-voltage characteristics resulting from the random channel dopant ion distribution," *IEEE Trans. Electron Devices*, vol. 41, no. 11, pp. 2222–2232, Nov. 1994.

[14] N. Sugii *et al.*, "Local V_{th} variability and scalability in silicon-on-thin-BOX (SOTB) CMOS with small random-dopant fluctuation," *IEEE Trans. Electron Devices*, vol. 57, no. 4, pp. 835–845, Apr. 2010.

[15] T. Matsukawa *et al.*, "Comprehensive analysis of variability sources of FinFET characteristics," in *IEEE Symp. VLSI Technology Dig.*, Jun. 2009, pp. 118–119.

[16] M.-H. Chiang, J.-N. Lin, K. Kim, and C.-T. Chuang, "Random dopant fluctuation in limited-width FinFET technologies," *IEEE Trans. Electron Devices*, vol. 54, no. 8, pp. 2055–2060, Aug. 2007.

[17] Y. Li, C.-H. Hwang, T.-Y. Li, and M.-H. Han, "Process-variation effect, metal-gate work-function fluctuation, and random-dopant fluctuation in emerging CMOS technologies," *IEEE Trans. Electron Devices*, vol. 57, no. 2, pp. 437–447, Feb. 2010.

[18] K. Cheng *et al.*, "Extremely thin SOI (ETSOI) CMOS with record low variability for low power system-on-chip applications," in *IEEE Int. Electron Devices Meeting (IEDM) Dig.*, Dec. 2009, pp. 49–52.

[19] M. J. M. Pelgrom, A. C. J. Duinmaijer, and A. P. G. Welbers, "Matching properties of MOS transistors," *IEEE J. Solid-State Circuits*, vol. 24, no. 10, pp. 1433–1439, Oct. 1989.

[20] F. Maloberti, *Data Converters*. Dordrecht, The Netherlands: Springer, 2007.

[21] K. Kattmann and J. Barrow, "A technique for reducing differential non-linearity errors in flash A/D converters," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 1991, pp. 170–171.

[22] M. Choi, J. Lee, J. Lee, and H. Son, "A 6-bit 5-GSample/s Nyquist A/D converter in 65 nm CMOS," in *IEEE Symp. VLSI Circuits Dig. Tech. Papers*, Jun. 2008, pp. 16–17.

[23] X. Jiang and M.-C. Chang, "A 1-GHz signal bandwidth 6-bit CMOS ADC with power-efficient averaging," *IEEE J. Solid-State Circuits*, vol. 40, no. 2, pp. 532–535, Feb. 2005.

[24] S. Sheikhaei, S. Mirabbasi, and A. Ivanov, "A 43 mW single-channel 4 GS/s 4-Bit flash ADC in 0.18 μm CMOS," in *Proc. IEEE Custom Integrated Circuits Conf.*, Sep. 2007, pp. 333–336.

[25] P. C. S. Scholtens and M. Vertregt, "A 6-b 1.6-Gsample/s flash ADC in 0.18 μm CMOS using averaging termination," *IEEE J. Solid-State Circuits*, vol. 37, no. 12, pp. 1599–1609, Dec. 2002.

[26] A. Ismail and M. Elmasry, "A 6-bit 1.6-GS/s low-power wideband flash ADC converter in 0.13-μm CMOS technology," *IEEE J. Solid-State Circuits*, vol. 43, no. 9, pp. 1982–1990, Sep. 2008.

[27] K. Deguchi *et al.*, "A 6-bit 3.5-GS/s 0.9-V 98-mW flash ADC in 90-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 43, no. 10, pp. 2303–2310, Oct. 2008.

[28] B.-W. Chen, S.-K. Hsien, C.-S. Chiang, and K.-C. Juang, "A 6-bit, 1.2-GS/s ADC with wideband THA in 0.13-μm CMOS," in *Proc. IEEE Asian Solid-State Circuits Conf.*, Nov. 2008, pp. 381–384.

[29] P. Veldhorst *et al.*, "A 0.45 pJ/conv-step 1.2 Gs/s 6b full-Nyquist non-calibrated flash ADC in 45 nm CMOS and its scaling behavior," in *Proc. IEEE Eur. Solid-State Circuits Conf. (ESSCIRC)*, Sep. 2009, pp. 464–467.

[30] Y. Chen, Q. Huang, and T. Burger, "A 1.2 V 200-MS/s 10-bit folding and interpolating ADC in 0.13-μm CMOS," in *Proc. IEEE Eur. Solid-State Circuits Conf. (ESSCIRC)*, Sep. 2007, pp. 155–158.

[31] R. Taft *et al.*, "A 1.8 V 1.0 GS/s 10b self-calibrating unified-folding-interpolating ADC with 9.1 ENOB at Nyquist frequency," *IEEE J. Solid-State Circuits*, vol. 44, no. 12, pp. 3294–3304, Dec. 2009.

[32] B. Chan, B. Oyama, C. Monier, and A. Gutierrez-Aitken, "An ultra-wideband 7-bit 5-Gsps ADC implemented in submicron InP HBT technology," *IEEE J. Solid-State Circuits*, vol. 43, no. 10, pp. 2187–2193, Oct. 2008.

[33] C. Enz and G. Temes, "Circuit techniques for reducing the effects of op-amp imperfections: Autozeroing, correlated double sampling, and chopper stabilization," *Proc. IEEE*, vol. 84, no. 11, pp. 1584–1614, Nov. 1996.

[34] C. Sandner *et al.*, "A 6-bit 1.2-GS/s low-power flash-ADC in 0.13-μm digital CMOS," *IEEE J. Solid-State Circuits*, vol. 40, no. 7, pp. 1499–1505, Jul. 2005.

[35] Y. Creten *et al.*, "An 8-bit flash analog-to-digital converter in standard CMOS technology functional from 4.2 K to 300 K," *IEEE J. Solid-State Circuits*, vol. 44, no. 7, pp. 2019–2055, Jul. 2009.

[36] R. Dennard *et al.*, "Design of ion-implanted MOSFET's with very small physical dimensions," *IEEE J. Solid-State Circuits*, vol. 9, no. 5, pp. 256–258, Oct. 1974.

[37] P. C. S. Scholtens, D. Smola, and M. Vertregt, "Systematic power reduction and performance analysis of mismatch limited ADC designs," in *Proc. Int. Symp. Low Power Electron. Design (ISLPED)*, 2005, pp. 78–83.

[38] B. Murmann, "A/D converter trends: Power dissipation, scaling and digitally assisted architectures," in *Proc. IEEE Custom Integrated Circuits Conf.*, Sep. 2008, pp. 105–112.

[39] Y. Yao *et al.*, "A 3-bit 20 GS/s interleaved flash analog-to-digital converter in SiGe technology," in *Proc. IEEE Asian Solid-State Circuits Conf.*, 2007, pp. 420–423.

[40] S. Park, Y. Palaskas, and M. Flynn, "A 4-GS/s 4-bit flash ADC in 0.18-μm CMOS," *IEEE J. Solid-State Circuits*, vol. 42, no. 9, pp. 1865–1872, Sep. 2007.

[41] Y.-C. Lien and J. Lee, "A 6-b 1-GS/s 30-mW ADC in 90-nm CMOS technology," in *Proc. IEEE Asian Solid-State Circuits Conf.*, 2008, pp. 45–48.

[42] Y.-Z. Lin, C.-W. Lin, and S.-J. Chang, "A 2-GS/s 6-bit flash ADC with offset calibration," in *Proc. IEEE Asian Solid-State Circuits Conf.*, 2008, pp. 385–388.

[43] B. Verbruggen, P. Wambacq, M. Kuijk, and G. V. der Plas, "A 7.6 mW 1.75 GS/s 5 bit flash A/D converter in 90 nm digital CMOS," in *IEEE Symp. VLSI Circuits Dig.*, Jun. 2008, pp. 14–15.

[44] C.-Y. Chen, M. Q. Le, and K. Y. Kim, "A low power 6-bit flash ADC with reference voltage and common-mode calibration," *IEEE J. Solid-State Circuits*, vol. 44, no. 4, pp. 1041–1046, Apr. 2009.

[45] R. Kertis *et al.*, "A 20 GS/s 5-bit SiGe BiCMOS dual-Nyquist flash ADC with sampling capability up to 35 GS/s featuring offset corrected exclusive-or comparators," *IEEE J. Solid-State Circuits*, vol. 44, no. 9, pp. 2295–2311, Sep. 2009.

[46] B. Verbruggen *et al.*, "A 2.2 mW 1.75 GS/s 5 bit folding flash ADC in 90 nm digital CMOS," *IEEE J. Solid-State Circuits*, vol. 44, no. 3, pp. 874–882, Mar. 2009.

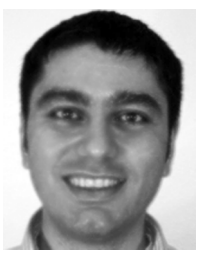
[47] Y. Nakajima *et al.*, "A self-background calibrated 6b 2.7 GS/s ADC with cascade-calibrated folding-interpolating architecture," in *IEEE Symp. VLSI Circuits Dig.*, Jun. 2009, pp. 266–267.

[48] I. Bogue and M. Flynn, "A 57 dB SFDR digitally calibrated 500 MS/s folding ADC in 0.18 μm digital CMOS," in *Proc. IEEE Custom Integrated Circuits Conf.*, Sep. 2007, pp. 337–340.

[49] D. C. Daly and A. P. Chandrakasan, "A 6-bit, 0.2 V to 0.9 V highly digital flash ADC with comparator redundancy," *IEEE J. Solid-State Circuits*, vol. 44, no. 11, pp. 3030–3038, Nov. 2009.

[50] M. Flynn, C. Donovan, and L. Sattler, "Digital calibration incorporating redundancy of flash ADCs," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 50, no. 5, pp. 205–213, May 2003.

[51] J. Proesel, "Flash analog-to-digital converter design based on statistical post-silicon calibration," Ph.D. degree, Carnegie Mellon Univ., Pittsburgh, PA, 2010.
[52] P. R. Kinget, "Device mismatch and tradeoffs in the design of analog circuits," *IEEE J. Solid-State Circuits*, vol. 40, no. 6, pp. 1212–1224, Jun. 2005.
[53] J. Craninckx and G. V. der Plas, "A 65 fJ/conversion-step 0-to-50 MS/s 0-to-0.7 mW 9b charge-sharing SAR ADC in 90 nm digital CMOS," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2007, pp. 246–247.
[54] V. Giannini *et al.*, "An 820 μW 9b 40 MS/s noise-tolerant dynamic-SAR ADC in 90 nm digital CMOS," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2008, pp. 238–239.
[55] P. Nuzzo, F. D. Bernardinis, P. Terreni, and G. V. der Plas, "Noise analysis of regenerative comparators for reconfigurable ADC architectures," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 55, no. 6, pp. 1441–1454, Jul. 2008.
[56] C. Mangelsdorf, "A 400-MHz input flash converter with error correction," *IEEE J. Solid-State Circuits*, vol. 25, no. 2, pp. 184–191, Feb. 1990.
[57] F. Kaess, R. Kanan, B. Hochet, and M. Declercq, "New encoding scheme for high-speed flash ADC's," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, 1997, pp. 5–8.
[58] A. Abo and P. Gray, "A 1.5-V, 10-bit, 14.3-MS/s CMOS pipeline analog-to-digital converter," *IEEE J. Solid-State Circuits*, vol. 34, no. 5, pp. 599–606, May 1999.
[59] G. V. der Plas, S. Decoutere, and S. Donnay, "A 0.16 pJ/conversion-step 2.5 mW 1.25 GS/s 4b ADC in a 90 nm digital CMOS process," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2006, pp. 2310–2310.
[60] H. Chung *et al.*, "A 7.5-GS/s 3.8-ENOB 52-mW flash ADC with clock duty cycle control in 65 nm CMOS," in *IEEE Symp. VLSI Circuits Dig.*, 2009, pp. 268–269.
[61] M. El-Chammas and B. Murmann, "A 12-GS/s 81-mW 5-bit time-interleaved flash ADC with background timing skew calibration," in *IEEE Symp. VLSI Circuits Dig.*, 2010, pp. 157–158.
[62] C.-C. Huang, C.-Y. Wang, and J.-T. Wu, "A CMOS 6-bit 16-GS/s time-interleaved ADC with digital background calibration," in *IEEE Symp. VLSI Circuits Dig.*, 2010, pp. 159–160.
[63] I.-H. Wang and S.-I. Liu, "A 4-bit 10 GSample/sec flash ADC with merged interpolation and reference voltage," in *Proc. IEEE Asian Solid-State Circuits Conf.*, 2008, pp. 377–380.
[64] M. Kijima, K. Ito, K. Kamei, and S. Tsukamoto, "A 6b 3 GS/s flash ADC with background calibration," in *Proc. IEEE Custom Integrated Circuits Conf.*, Sep. 2010, pp. 283–286.



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