A 22-mW 7b 1.3-GS/s Pipeline ADC with 1-bit/stage Folding Converter Architecture

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Abstract

We have developed a 7-b 1.3-GSa/s 1-bit/stage pipeline ADC with a folding characteristic that uses a polarity selecting technique. The ADC achieves an ENOB of 6.5-b and consumes only 22 mW from 1.2V supply. These results yield a figure of merit (FOM) of 190-fJ/conv.-step. It is implemented in 45-nm CMOS technology and occupies a core area of 0.023 mm^2.

Introduction

A low-power, medium-resolution (6–8 bit), Giga-sample ADC is a key component in future high speed communication systems based on digital signal processing (DSP) [1]. A full-flash ADC architecture is widely used in GHz-sampling ADCs, however, this requires high power consumption and a large area for the resolution. A SAR or pipeline architecture can be used to achieve medium resolution with low power, and a small area, though, the sampling frequency cannot exceed 1 GHz without time-interleaving, which increases the area required. In this paper, we propose a folding/interpolation pipelined ADC with open-loop sub-ADC stages using 1-bit zero-crossing (ZC) detection to overcome above tradeoffs.

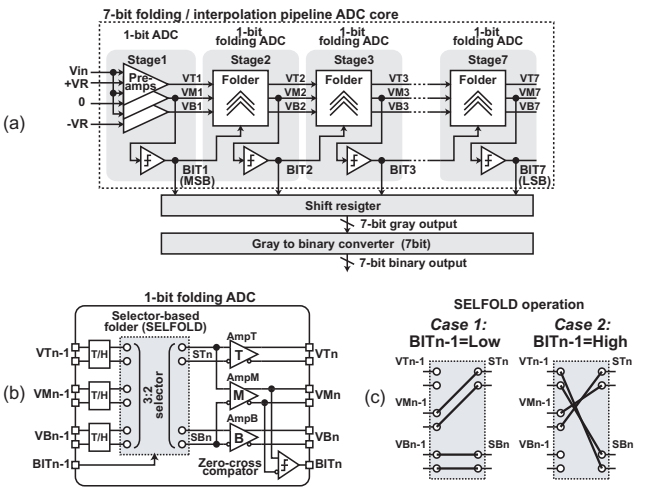

Fig. 1 (a) Block diagram of 7-bit Folding/Interpolation Pipelined ADC (b) Block diagram of selector based 1bit folding ADC (c) SELFOLD operation

Architecture

A block diagram of the proposed ADC is shown in Fig. 1(a). The converter consists of 7-cascaded pipeline stages with a 1-bit folding ADC for each sub-ADC. Since a conventional sub-ADC uses a closed-loop opamp in a residue amplifier, its conversion speed is limited due to the need for high linearity [2]. We overcome this limitation by using a simple ZC-detection-based ADC with three open-loop amplifiers as the sub-ADC, resulting in over GS/s one-bit conversion. The ZC detection with folding is achieved using a new folding interpolation technique consisting of (1) the ZC boundary generation by interpolation of two different transfer curves, and (2) selector based folder (SELFOLD) with dynamic switching of the signal paths between two options, case1 or 2 (Fig. 1(c)). Moreover, 7-bit gray code output from 7 folding sub-ADC stages is decoded to binary code.

A. Operating Principles

Figure 2 shows three different ADC configurations based on the ZC-detection algorithm and their operation behavior. Figure 2(a) shows that for conventional interpolation-flash ADC, which creates a ZC boundary from two adjacent amplifiers and then generates thermometer code using the output from $2^{(N\text{-bit})}$ ZCs. As a result, the total number of amplifiers grows exponentially with the ADC resolution. Figure 2(b) shows the configuration for a "sliding interpolation" technique, which effectively curbs the exponential growth [3]. This ADC reuses two reference amplifiers (AmpT and AmpB) and an interpolation amplifier (AmpM) for a ZC detection by switching the inter-stage paths of the signals in accordance with the bit decision in the previous stage. This technique, however, causes discontinuous DC transfer characteristics in each amplifier resulting in conversion errors during high-speed operation, as described later. Figure 2(c) shows the configuration of our proposed ADC. It uses a combination of inverse polarity and signal-path crossing, unlike the configuration shown in Fig. 2(b), which uses only sliding signal path operation. This combination results in a folded continuous DC transfer characteristic, which contributes to stability and an improved ENOB during high-speed operation.

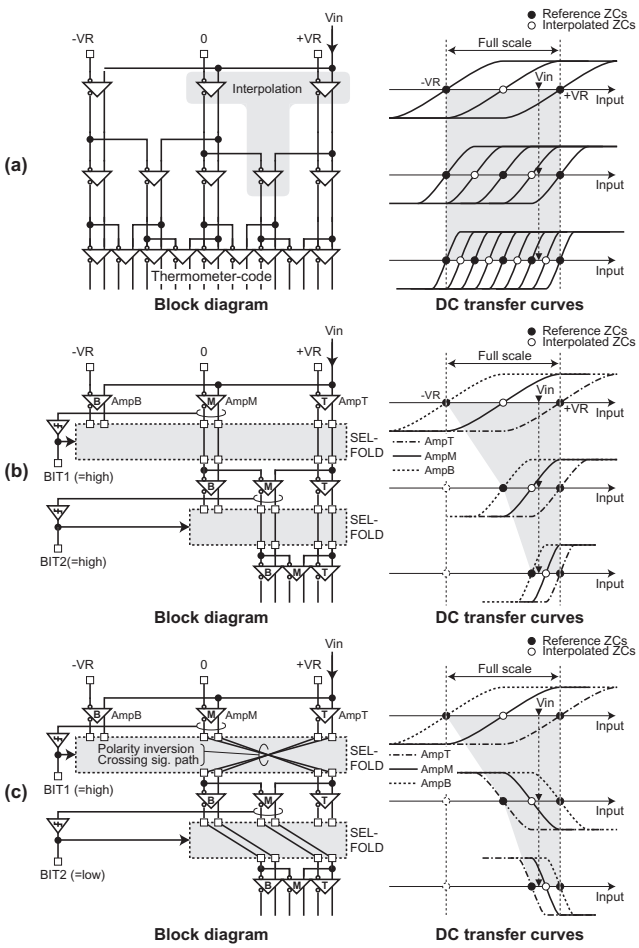

Fig. 2 Three different ADC configurations based on the ZC-detection algorithm and operation: (a) interpolation-flash (b) sliding interpolation (c) proposed folding interpolation

B. Advantage of Proposed Folding Interpolation Technique

The complete DC transfer curves for AmpM in the first three stages of the conventional binary and the proposed folding schemes are shown in Fig. 3(a). Comparing these curves, we see

that the one for conventional scheme has a sawtooth waveform with discontinuity in full scale input range. In contrast, the proposed one has triangle waveform with continuity. When the input voltage slightly changes from –ΔV to +ΔV, the sampling voltage for each stages changes from An to Bn. The conventional scheme has full-scale transitions between An and Bn, resulting in a settling error that leads to a conversion error, as shown in the time domain waveforms (Fig. 3(b)). In contrast, the proposed folded scheme reduces the probability of full-scale occurrence to half that of the conventional scheme so the errors are reduced. The diagrams in Fig. 3(c) show the ENOB degradation resulting from the settling error, as obtained by simulation using behavior models. Focusing on an input frequency of fs/2, which is most often seen in full-scale transitions, the folding scheme had a 1.0% wider margin than the conventional scheme for the settling error at 6.5 ENOB (resulting in a 0.5-bit ENOB improvement). Therefore, we aggressively use this settling error mitigation to reduce power consumption by 10% power reduction. In addition, in considering importance of the 1-2% error margin, this is large enough to degrade the resolution of ADC below 6-bit.

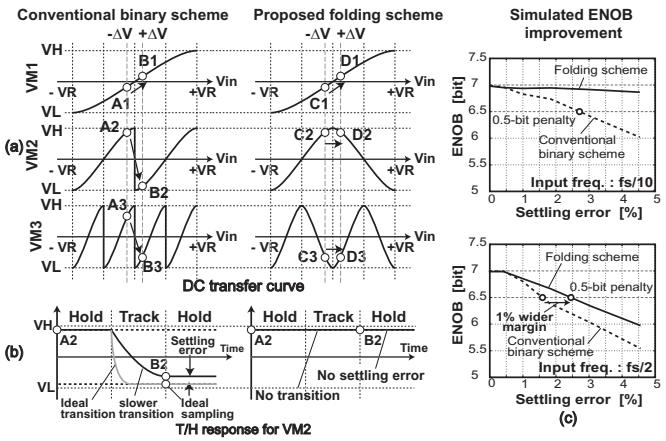

Fig. 3 (a) DC transfer curves comparison (b) T/H response for VM2 (c) Simulated ENOB improvement

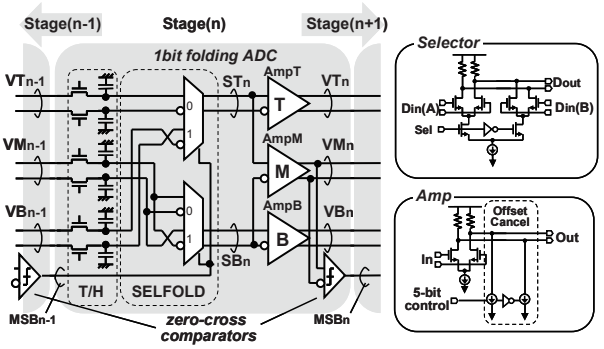

Fig. 4 Details of proposed 1bit folding stage and its circuits

Implementation of High-Speed Folding sub-ADC

As shown in Fig. 4, three differential input signals (VTn-1, VMn-1, VBn-1) are sampled by T/H circuits in each sub-ADC using MOS transfer gates and are folded by the following SELFOLD circuit. Then, three amplifiers (AmpT, AmpB, AmpM) generate two reference ZCs and one interpolated ZC, respectively, and a dynamic comparator makes a bit decision from the AmpM output (VMn). The SELFOLD consists of a high-speed CML based selector instead of simple MOS transfer-gates. This enables rejection of common mode level mismatches at the AmpM inputs due to signal-dependent charge injection and clock feed-through in the T/H circuit. Since AmpM creates an interpolated ZC from the positive node of the top selector outputs (STn) and the negative node of the bottom selector outputs (SBn), the common mode level mismatches between STn and SBn directly cause interpolation errors. The CML-based selector with its differential configuration effectively cancels out common mode errors. The use of a high-speed CML-based selector also prevents speed degradation due to series on-resistance of MOS transfer gates. Moreover, the CML implementation makes it easy to include an offset cancellation circuit. To avoid degradation of the analog-to-digital conversion accuracy, we implemented 5-bit offset control in each comparator. The offset cancellation at start-up greatly improves the integral and differential nonlinearities, as shown in Fig. 5. In addition, the offset cancellation enables the use of minimum-size transistor gates for the amplifiers and comparators and contributes to an increase in the sampling rates beyond the GHz level.

Measurements Results

The proposed ADC was fabricated using the 45-nm CMOS process. It consumes only 22 mW from 1.2 V supply voltage and occupies an active area of 0.023 mm^2. The estimated INL/DNL using a cumulative histogram test with a 10-MHz sinusoidal signal are shown in Fig. 5. Comparator offset calibration reduced the maximum INL and DNL values to less than +/-1.0 LSB. The input frequency dependency of ENOB and the 2048-point FFT plots for 100-MHz input are shown in Fig. 6. The measured ENOBs with calibration at low frequency and the Nyquist frequency (fs/2) were 6.5 and 5.2 bits, respectively, where fs is the sampling frequency. These results yield an FOM of 0.19-pJ/conv.-step. A die photograph and performance summary are respectively shown in Fig. 7 and Table 1. These results demonstrate that our proposed ADC is a promising architecture that enables a higher data rate and spectrally efficient communication system based on DSP.

References

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[3] Y. Wang and B. Razavi, "An 8-Bit 150-MHz CMOS A/D Converter," IEEE JSSC, vol.35, no. 3, pp. 308–316, Mar. 2000.

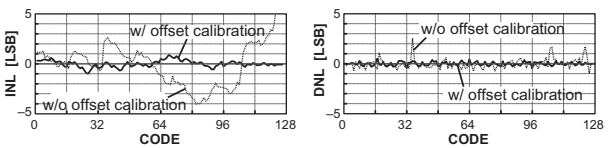

Fig. 5 Measured INL and DNL

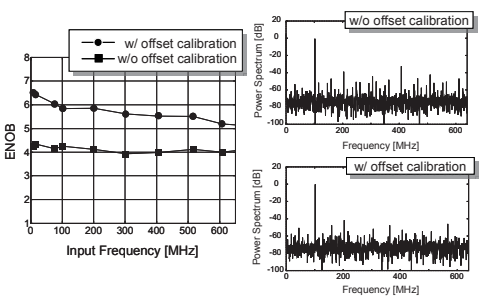

Fig. 6 Measured ENOB and output spectrums

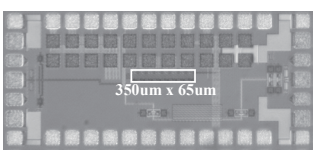

Fig. 7 Die photograph

Technology	45-nm CMOS
Resolution	7 bit
Conversion Rate	1.3 GS/s
ENOB (8MHz input)	6.5 bit
INL/DNL	<+/– 1.0 LSB
Supply Voltage	1.2 V
Power Dissipation	22 mW
Chip Area (ADC Core)	0.023 mm^2
Figure of Merit	0.19-pJ/conversion-step

Table 1 Performance summary