Low-Power 6-bit 1-GS/s Two-Channel Pipeline ADC with Open-Loop Amplification using Amplifiers with Local-Feedback

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***Abstract*—A low-power 1.2 V 6-bit 1-GS/s time-interleaved pipeline ADC designed in 130 nm CMOS is described. It is based on a new 2-channel 1.5-bit MDAC that performs open-loop residue amplification using a shared amplifier employing local-feedback. Time mismatches between channels are highly attenuated, simply by using two passive front-end Sample-and-Hold circuits, with dedicated switch-linearization control circuits, driven by a single clock phase. Simulated results of the ADC achieve 5.35-bit ENOB, with 20 mW and without requiring any gain control/calibration scheme.**

I. INTRODUCTION

Wireless short range connectivity with high data rate capabilities, is and will be one of major driven technology for the consumer electronics mass market. Wireless (USB) and Ultra Wideband (UWB) Bluetooth are examples of such technologies since they start from an installed base in the billions of ports. Software radio UWB receiver implementation has numerous potential benefits ranging from low-cost and ease-of-design to flexibility. However such approach implies analogue-to-digital converters (ADCs) capable of sampling rates in order of GS/s, which constitutes a technical challenge when using a low-cost pure digital CMOS technology.

Parallel pipeline ADCs have been used to achieve medium resolutions at very high sampling rates [1, 2]. Also sharing some common blocks between two or more parallel ADCs, in a time-interleaved fashion can reduce the total power. The closed-loop multiply-by-two residue amplifiers usually integrated in the pipeline ADCs can be replaced by open-loop amplifiers [3, 4], reducing global size and power. However, it becomes mandatory to employ either digital gain-calibration [3] or employ replica circuits for implementing global-gain control techniques [4].

This work presents a 1.2 V 20 mW 6-bit 1GS/s 2-channel pipeline ADC designed in a 1.2 V, 130nm 1P-8M CMOS technology. In each pipelined stage, the open-loop residue amplification is carried-out by using a shared amplifier between channels. This amplifier employs local-feedback in order to achieve constant closed-loop gain against Process-Supply-Temperature (PVT) variations and thus, avoiding the need of any digital self-calibration or gain-control techniques. Time skews between the 2 channels are highly reduced, by using two passive front-end Sample-and-Hold (S/H) circuits, with dedicated switch-linearization control (SLC) circuits [5], driven by a single clock phase [6]. Simulations reach a peak SNDR of 34 dB, a SFDR of 47 dB, a THD of -43 dB and 5.35-bit ENOB, for a power dissipation of 20 mW which corresponds to an energy efficiency better than 0.5 pJ per conversion. Moreover, all pipelined stages are made equal and no scaling is used which highly simplifies the layout effort.

In Section II the architecture of the ADC, the timing and the required circuits for clock-phase generation are presented. In Section III the basic building-blocks of the ADC are described namely, the S/H, the open-loop 1.5-bit multiplying-DAC (1.5-bit MDAC) residue amplifiers and the comparator used in the 1.5-bit flash quantizers (1.5-bit FQ). Simulated FFT results and the dynamic performance of the ADC are provided in Section IV, and the main achieved results are finally summarized in Section V where the conclusions are drawn.

II. ARCHITECTURE DESCRIPTION AND TIMING

Using two interleaved pipelined ADCs in parallel, the sampling rate is doubled. In Fig. 1, a block diagram the architecture of the overall 2-channel ADC is shown.

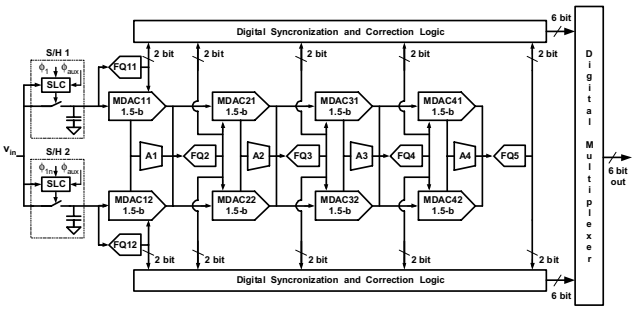


Figure 1. Block diagram of the architecture of the 6-bit 2-channel time-inteleaved Pipeline ADC.

Basically, the fully-differential structure of each pipeline ADC comprises a passive front-end sample-and-hold (S/H), followed by a cascade of four 1.5-bit stages and by a 2-bit flash quantizer at the end of the signal path. Each 1.5-bit stage comprises a 1.5-bit MDAC and a 1.5-bit quantizer. The 10 output bits provided by the 5 quantizers are then digitally synchronized and a net resolution (*N*) of 6 bits is available at the output after applying synchronization and standard digital correction (summing all five 2-bit words with 1-bit overlap). Each 1.5-bit MDAC block operates at 500 MS/s in order to relax the speed requirements of the amplifiers by a factor of 2. Since MDACs of the same stage, but of different channel, operate in opposite phases, they are able to share the same amplifier. Four equal sized amplifiers are, therefore, shared between channels, namely A1 to A4.

The 1.5-b quantizers FQ11 and FQ12, adjacent to the lower pipeline perform quantizations at 500 MHz. The other four 1.5-b quantizers namely, FQ2, FQ3, FQ4 and FQ5, operate at 1 GHz, since they are also shared between stages in order to reduce area. Finally, at the output, a digital multiplexer operating at full speed is used in order to provide the 6-bit digital output at a 1 GS/s clock rate.

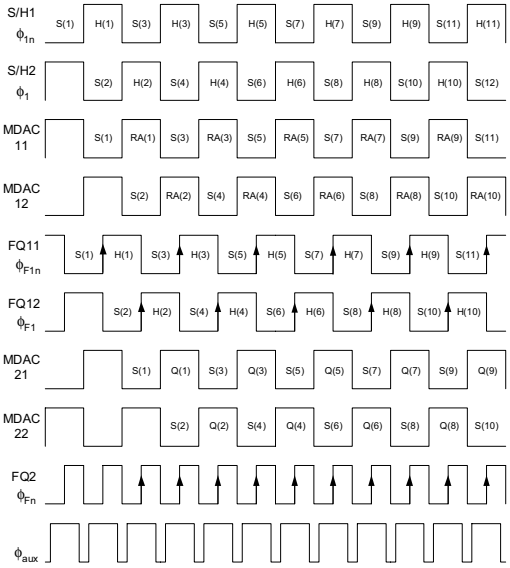


Figure 2. Control clock signals and architecture timing.

The control and timing signals are shown in Fig. 2. The single-phase technique described in [6] is used and, hence, only one clock phase is used, ϕ_1, and it complementary version, ϕ_{1n}. These complementary phases are used to drive the two S/H blocks and all 1.5-bit MDACs. Front-end quantizers FQ11 and FQ12 (operating at 500 MHz) are controlled by clock signals ϕ_{F1} and ϕ_{F1n} and, the remaining quantizers (operating at 1 GHz) are driven by phases ϕ_F and ϕ_{Fn}. In order to let the amplifiers to settle in a complete 2 ns time-slot, the quantization of all 1.5-bit flash ADCs is done in the middle of the sampling-phase of the 1.5-bit MDACs of the same stage. Finally, an auxiliary clock signal ϕ_{aux}, used to cancel the time-skew errors between the two channels, is also displayed.

All clock-phase signals are obtained from a 1 GHz master clock, *clk*, as depicted in Fig. 3. No non-overlapping clock-phase generators are used. The first D Flip-Flop (D-FF) is used to lower the frequency and obtain the 500 MHz, ϕ_1 and ϕ_{1n}, complementary phases. Using ϕ_1 and ϕ_{1n}, and the master clock the 90º phase-shift phases, ϕ_F and ϕ_{Fn}, to drive quantizers FQ2 to FQ5 are generated. Thought a second D-FF, phases ϕ_{F1} and ϕ_{F1n} are produced to drive quantizers FQ12 and FQ11, respectively. Finally, auxiliary phase ϕ_{aux} is generated as shown in Fig. 3 using a simple OR gate. All phases are properly buffered using digital buffers with the driving capability sized according to the load.

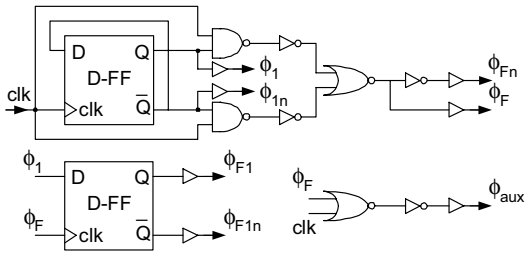


Figure 3. Clock signals generation.

III. Design of the Basic Building-Blocks

A. The 1.5-bit MDAC

Instead of using a closed-loop amplifier with high gain, as usually employed in the conventional schemes, it is used an open-loop amplifier in the MDAC stages [3, 4].

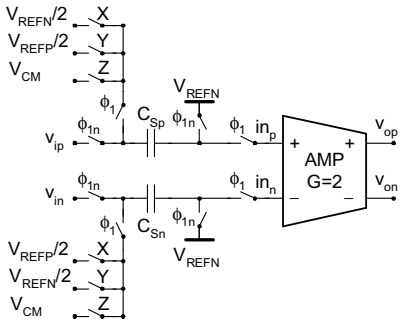


Figure 4. Fully-differential implementation of the 1.5-bit MDAC based on open-loop amplification.

As illustrated in Fig. 4, the input voltage, v_{ip}, is sampled into C_{Sp} (nominally set to 0.3 pF due to KT/C noise constraints) during phase ϕ_{1n}. During ϕ_1, the sampled signal is amplified by a gain of 2, and the output amplified residue is produced according to

$$v_{od} = v_{op} - v_{on} = -2\left(v_{id} + X\frac{V_{REFD}}{2} - Y\frac{V_{REFD}}{2} + Z \cdot 0 \right) \qquad (1)$$

where $v_{id} = v_{ip} - v_{in}$, $V_{REFD} = V_{REFP} - V_{REFN}$, and the digital signals *X*, *Y* and *Z* are provided by the local 1.5-bit quantizer and only one is active at a time. The residue amplification gain, *G*, needs to be made accurately equal to 2 (with an error smaller than ±1.56 % for 6-bit accuracy). The

reference levels $V_{REFP}/2$ and $V_{REFN}/2$ used are, respectively, 0.675 V and 0.425 V, corresponding to $V_{REFP} = 0.8\,\mathrm{V}$, $V_{REFN} = 0.3\,\mathrm{V}$ and to an output common mode level, V_{CM}, of 0.55 V (set to this value to allow operation down to 1.08 V).

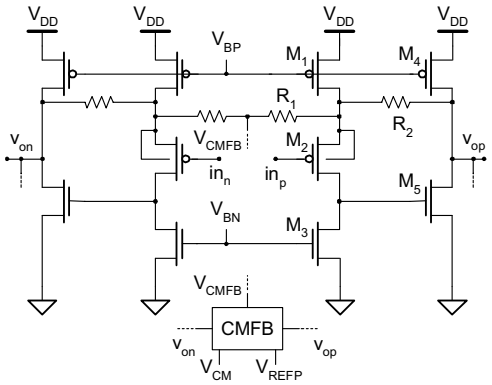


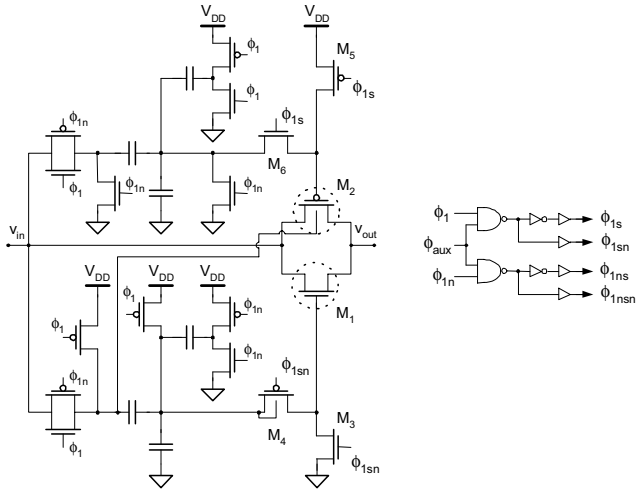
Figure 5. Fully-differential closed-loop amplifier.

The proposed amplifier structure based on local feedback is shown in Fig. 5. It is based on a two-stage amplifier (M_2 and M_5 devices) with no inverting feedback [7]. Transistor M_2 acts as a source follower, copying the input signal in_p to the resistor node. In the second stage, the transistor M_5 delivers the output voltage, v_{op}, and current. The input transistor is PMOS type with bulk shorted to its source to reduce body effect, and devices M_1, M_3 and M_4 operate as current sources. The bias circuit, not shown, provides the required bias voltages V_{BP} and V_{BN}. The gain is approximately equal to $1+R_2/R_1$, but the capacitive attenuation due to parasitics at the input (gate of M_2) reduces it. The sampling capacitor, C_{Sp}, together with the input parasitic capacitance defines a trade-off between linearity, speed and power dissipation. The overall voltage gain can be adjusted varying the value of R_1. The values of 315 Ω and 500 Ω, respectively for R_1 and R_2, are chosen. Input and output stages are biased with 100 μA and 500 μA, respectively. To avoid accumulation in the common-mode errors by cascading several pipeline stages, a common-mode feedback circuit (CMFB), is employed. It senses the two output voltages, compares their level with V_{CM} and adjusts the output common-mode voltage thought node V_{CMFB}.

Switches connected to the MDAC input signals are implemented with a CMOS asymmetrical transmission-gates (ATG) employing simple bulk-switching in the PMOS device. Dummy switches (half-sized) are used to minimize signal dependent charge injection. The remaining switches are implemented using single NMOS or PMOS transistors.

B. The Passive front-end Sample-and- hold circuits

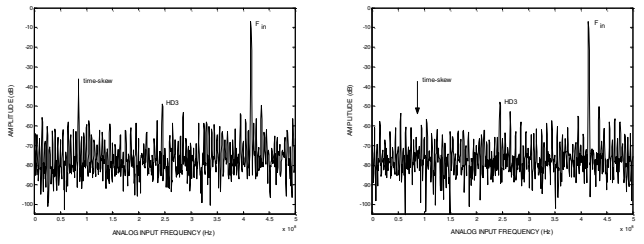
The two front-end fully-differential S/H circuits are based on a passive structure comprising two 4 pF sampling capacitors and two ATGs (*per* each S/H). Each ATG switch is driven by a dedicated switch linearization control (SLC) circuit, described in detail in [5]. The complete schematic of the SLC circuit, is shown in Fig. 6(a). The main transistors M_1 and M_2 form the CMOS switch, and are respectively sized with aspect ratios of 20/0.12 and 80/0.12. Their controlled gate voltages are function of the input voltage, v_{in}, resulting in very highly linear switch without having any reliability problems [5]. Note that the fact of connecting the MDAC sampling capacitors, C_S, charged with the input signal of the previous sample to the passive S/H, C_{SH}, only causes a low-pass filtering function of the type $H(z) = z^{-1/2}(C_{SH}/(C_{SH}+C_S))/(1-z^{-1}(C_S/(C_{SH}+C_S)))$. Since C_{SH} is made, at least, one order of magnitude larger than C_S, the attenuation at Nyquist frequency is below 1dB. At DC there is no attenuation. As long as the critical parasitic capacitances at the inputs of the amplifier of the MDAC are kept small, the distortion will be negligible at 6-bit level.



(a) (b)

Figure 6. (a) Schematic of the SLC circuit used to linearize CMOS (ATG type) input switches (M_1 and M_2); (b) Generation of syncronization signals.

It is known the clock signals, in this case ϕ_1 and ϕ_{1n}, might not have the same width, originating a sampling time error. This time-skew error [8, 9], produce in the output data spectrum of two interleaved structures, a frequency function of the input signal frequency, F_{in}, and function of half the sampling frequency, F_S, *i.e.* at $F_{in}+F_S/2$. Fig. 7(a) shows the simulated FFT spectrum of the output of the 6-bit ADC, without mismatch error cancellation, when a 415 MHz full-scale input signal is applied together with an intentionally set time-mismatch of 150 ps. The tone appears as a mirrored image of the main frequency, with centre at $F_S/4$.



(a) (b)

Figure 7. FFT spectrum of the output data of the ADC: (a) without mismatch time-skew cancelation; (b) with mismatch time-skew cancelation.

Using the same auxiliary clock signal, ϕ_{aux}, and two NAND gates, the original clock signals, ϕ_1 and ϕ_{1n}, can be converted into synchronized signals, ϕ_{1s} and ϕ_{1ns}, according to the circuit shown in Fig. 6 (b). A second synchronized pair is also obtained (complementary versions, ϕ_{1sn} and ϕ_{1nsn}) by this simple circuit. These signals are then used for locally and accurately control the gate voltages of the main CMOS sampling CMOS switch (M_1, M_2), acting through the SLC auxiliary transistors, M_3, M_4, M_5 and M_6, as displayed in Fig. 6 (a). The switches of the first S/H block, instead of sampling during phase ϕ_1, are sampling during ϕ_{1s}. Likewise, the CMOS input sampling switch of the second S/H block, samples during ϕ_{1ns}. When this technique is applied, there is an efficient cancellation of the time-skew effect, as shown in Fig. 7 (b) where the same time mismatch of 150 ps and the same input signal frequency are used.

C. The Flash Quantizer

Each 1.5-bit quantizer consists of 2 comparators followed by a thermometer-to-binary digital encoder and by an *X*, *Y*, *Z* encoder. Each comparator comprises an input switched-capacitor divider network to define the threshold level, followed by an ordinary dynamic preamplifier/positive-feedback latch. This comparator was optimized using exhaustive Monte-Carlo simulations in order to achieve low-offset, reduced kickback noise, high mean-time to failure, and low-power dissipation at the desired speed of operation.

IV. Simulation Results

The 1.2 V, 6-bit, 1 GS/s 2-channel pipeline ADC was fully designed and simulated at transistor level in a 130nm 1P-8M CMOS technology. In order to simplify the layout effort, all pipelined stages are equally sized, i.e. no scaling is applied to the 1.5-bit MDACs. A scaling-down approach would optimize further the overall power. Fig. 8 displays the FFT (1024 bins) of the ADC output clocked at 1 GHz when a full-scale input of 315 MHz is applied.

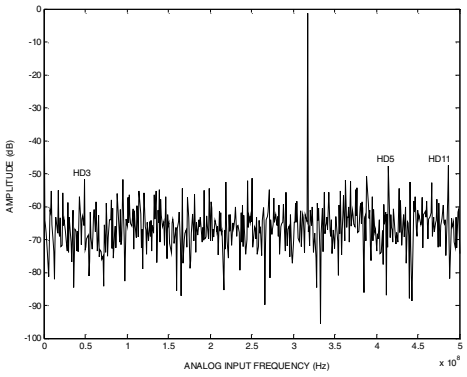


Figure 8. Simulated FFT Spectrum with 1024 bits for f_{clk}=1 GHz and f_{in}=315 MHz (coherent sampling).

A peak SNR of 34.6 dB is obtained through analytical calculations when 4 pF and 0.3 pF unit capacitors are used respectively in the S/Hs and 1.5-bit MDACs. Simulations show a THD of –43 dB, a SFDR of 47 dB, and a peak SNDR larger than 34 dB corresponding to an ENOB better than 5.35 bits. The Gain error/time-skew spur is 50 dB below the signal. Due to the single-phase scheme used, the highest harmonics are HD5 and HD11 rather than HD3.

The circuit dissipates less than 20 mW (11 mW analog and 9 mW digital) with 1.2 V and at 1 GS/s, corresponding to an energy efficiency better than 0.5 pJ. When comparing the energy efficiency with the state-of-the-art of low-resolution pipeline ADCs employing open-loop residue amplification [4] (ENOB=5.3 bits, Fs=800 MS/s, Power=105 mW), this work exhibits an improvement (based on simulation results) of a factor higher than 6.6. Furthermore, no calibration scheme is required.

V. Conclusions

A low-power 1.2 V 6-bit 1-GS/s time-interleaved pipeline ADC designed in 130 nm CMOS was described. It is based on a new 2-channel 1.5-bit MDAC that performs open-loop residue amplification using a shared amplifier employing local-feedback. Time mismatches between channels are highly attenuated, simply by using two passive front-end S/H circuits, with dedicated SLC circuits, driven by a single clock phase. Simulated results of the ADC achieve 5.35-bit ENOB, with less than 20 mW and without requiring any gain control/calibration scheme.

Acknowledgements

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