GHz Class Low-Power Flash ADC for Broadband Communications

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A low-power (~400mW) high-speed (2-4GS/s) 4-bit Analogue-to-Digital Converter (ADC) based on InP/InGaAs heterojunction bipolar transistors (HBT) has been designed and simulated. The technology utilised two novel developments. Firstly stoichiometric conditions permitted growth at a relatively low temperature (420°C) while conserving extremely high-quality materials. Secondly dimeric phosphorus generated from a gallium phosphide (GaP) decomposition source has lead to excellent device properties. The complete ADC shows state-of-the-art performance and includes an interface for connection to standard Digital Signal Processing (DSP) systems whilst dissipating only 400mW.

1. Introduction

High-speed, low-resolution analogue-to-digital converters (ADCs) have widespread applications in wired and wireless broadband communications [1], radar receivers [2], digital oscilloscopes [3] and millimetre arrays for radio astronomy [4]. The rapid scaling of transistor and interconnect dimensions has enabled increased chip complexity and performance. In terms of CMOS for example, improvements in high-k dielectric materials have pushed this technology to approach a maximum speed 10-20GHz [5]. However, for ultra-low power designs, alternative materials, such as SiGe or III-V compound semiconductor technologies are the only viable option [5].

For mixed-signal applications and high-speed digital logic design, closely matched devices are indispensable. The improved threshold voltage control of heterojunction bipolar transistors (HBT) compared to Field Effect Transistor (FET) devices, as well as their high linearity and fundamentally lower 1/f noise [6] make these an ideal choice. While SiGe HBTs can be used for speeds approaching 77GHz [5], its peak electron velocity occurs at a much higher electric field than InGaAs [7]. Hence to achieve comparable high-speed operation, SiGe HBTs require larger bias voltages which results in increased power dissipation. Also, the low bandgap InGaAs used in the base layer of InP/InGaAs or AlInAs/InGaAs HBTs reduce the turn-on voltage, and thus make these material systems suited for low-power applications.

This paper presents the continuing research into developing an ultra-low power ADC based on InP/InGaAs HBTs. The ultimate achievement is to fabricate a 4-bit Flash ADC that operates with a sampling frequency of 2-4GHz, and dissipates less than 400mW.

2. Material Growth and Fabrication

The epitaxial layers (shown in Table 1) were grown on a VG 90H solid-source molecular beam Epitaxy (MBE) system on Fe-doped semi-insulating (100) InP substrates. Growth was performed at a relatively low temperature of ~420°C and used stoichiometric conditions for both the Arsenide and Phosphide materials. Phosphorus was generated from a GaP decomposition source whose operational aspects are described elsewhere [8].

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Table 1: SHBT Epilayer Structure

Layer	Material	Doping (cm^{-3})		Thickness (Å)
Cap	$In_{0.47}Ga_{0.53}As$	n^+	1×10^{19}	1350
Emitter 1	$In_{0.47}Ga_{0.53}As$	n	1×10^{17}	1350
Emitter 2	InP	n	1×10^{17}	400
Spacer	$In_{0.47}Ga_{0.53}As$		Intrinsic	50
Base	$In_{0.47}Ga_{0.53}As$	p^+	1.5×10^{19}	650
Collector	$In_{0.47}Ga_{0.53}As$	n^-	1×10^{16}	6300
Sub-collector	$In_{0.47}Ga_{0.53}As$	n^+	1×10^{16}	5000
Buffer	$In_{0.47}Ga_{0.53}As$		Intrinsic	100
Substrate	Semi-Insulating InP			

3. Transistor Characterisation and Modelling

Simulated and measured common-emitter current-voltage (*I-V*) characteristics of a SHBT with an emitter area of $1.5\times5\mu m^2$ are shown in Fig. 1. Microwave S-parameters were measured on an HP8510C network analyser using on-wafer probing over the frequency range of 45 MHz to 110 GHz. Prior to current gain collapse (caused by self-heating and the Kirk effect) the current-gain cut-off frequency (f_t) and maximum oscillation frequency (f_{max}) were extrapolated to be 91GHz and 83GHz respectively at I_C=3.6mA and V_{CE}=1V.

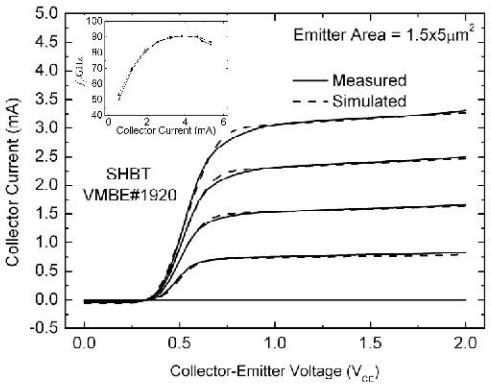

Fig. 1. Measured and Simulated I-V Characteristics and f_t for the SHBT

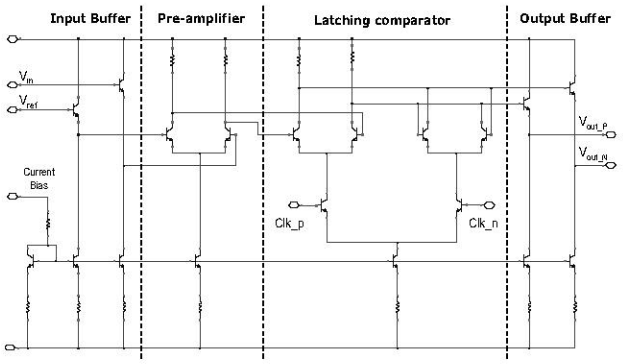

Fig. 2. Schematic of Comparator cell Dissipates 7.6mW for a 2GHz Sampling Rate

Parameters were extracted [9] from the transistor for non-linear modelling in Agilent's ICCAP and Advanced Design System (ADS) software. This software includes the small-signal University of San Diego (UCSD) for the HBT [10].

4. Comparator Design

The comparator cell shown in Fig. 2 is based on the low-power design proposed by Hotta et al [11]. It consists of an input buffer, preamplifier, latching comparator and output buffer. The main design objective is to maximise operational speed, without consuming excessive power or chip area. Thus Emitter Couple Logic (ECL) is used extensively with a minimum supply rail voltage of 3V to prevent devices entering saturation. The most important components of the cell are the pre-amplifier stage and the latching comparator. The latter is created via two cross-coupled differential pairs that can either sample or hold data depending

on the switching clocks (clk_p and clk_n). Since the gain of this stage is low, the recovery time can be substantial. It is well understood that the operational speed of this latch is roughly proportional to its current consumption. However, an alternative method to improve overall performance is to amplify the input signal before being fed into the latching comparator (pre-amplification). In this configuration it is possible to obtain the same performance, but at a much reduced power.

As stated previously, the speed of the latching comparator is determined mainly by its recovery time (t_r), which can be expressed by Eqn. (1). [11].

$$t_r = C_L R_L \equiv C_L \cdot \frac{\Delta V_O}{I_L} \tag{1}$$

where C_L is the collector load capacitance, R_L is the collector load resistance, I_L is the tail current and V_O is the output voltage swing. Thus to optimise the circuit for low power operation, it is desirable optimise all factors in Eqn. (1).

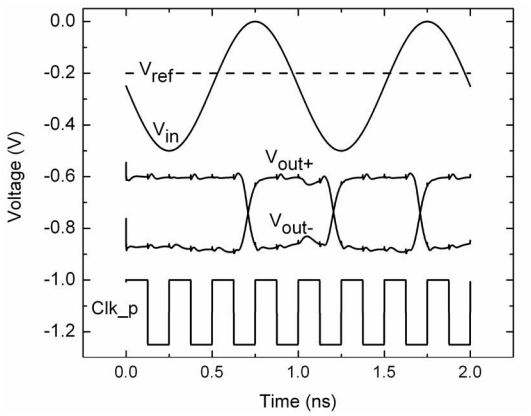

Fig. 3. Comparator Output Simulated with a 4GHz clock and 1GHz Input

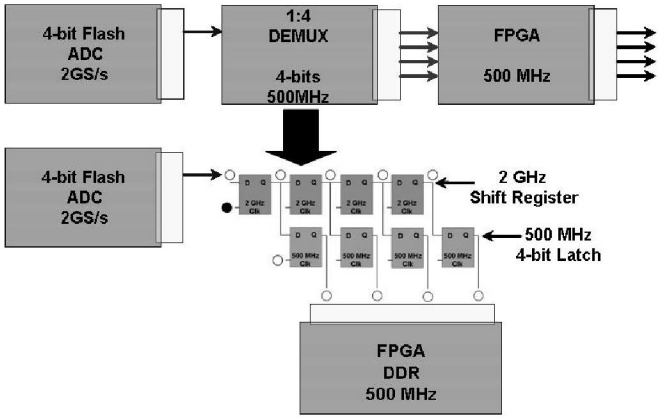

Fig. 4. Schematic of Complete ADC with 1:4 DEMUX for Compatibility to FPGA

For a digital system, the output swing must be larger than the thermal voltage (V_T) ~26mV. In this work we have designed a voltage swing of approximately 10 times V_T ~ 250mV to allow the comparator relatively high noise immunity. Simulations were then conducted on the latched comparator to decide on suitable load currents. To reduce the impact of meta-stable states, and improve sensitivity, a maximum recovery time of 60ps was chosen, setting the tail current to be ~520μA.

To optimise the input signal response, the pre-amplifier was designed to have the same time constant as that of the latching comparator [11]. The simulated negative level clock triggered the output of the optimised comparator as shown in Fig. 3, and produced state-of-the-art power consumption of 10.8mW at 4GS/s. The circuit was also re-optimised for a 2GHz clock, providing power reductions by 20% to ~7.8mW.

5. Interface

The ADC output is preceded by a DSP unit, either a Field Programmable Gate Array (FPGA) or Application Specific Integrated Circuit (ASIC) based solution. These operate at a standard 250 MHz clock or 500 MHz with Double Data Rate (DDR) interface. For ADC data clocked at 2GHz to communicate to this back-end logic operating at 500 MHz for example, a 1:4 Demultiplexer (DEMUX) is implemented to achieve 4-bit serial to parallel conversion at shown in the Fig 4. The DEMUX comprise of D-latches with LVDS compatible output levels.

The complete ADC consumes a total of 400mW requiring 960 transistors, 588 NiCr resistors and 15 decoupling capacitors.

Conclusions

The continuing research into the design an ultra low-power 4-Bit A/D converter for use in the upcoming Square Kilometre Array (SKA) is presented in this paper. The ADC operates at 2-4GHz sampling frequency with an analogue input bandwidth from DC to Nyquist frequency. To meet these targets, in-expensive optical lithographic techniques are required, in addition to designs that minimise both power dissipation and chip area. A prototype MMIC circuit using the above design is presently being built.

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