A 2-Bit 4GS/s Flash A/D Converter in 0.18 μm CMOS for an IR-UWB Communication System

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Abstract

A 4GS/s 2-bit non-time-interleaved flash ADC is designed for an IR-UWB (Impulse Radio Ultra Wide Band) receiver. In this flash ADC, implementing differential low-swing operation in analog part and CML (current mode logic) in digital part result in high-speed and low power consumption. Furthermore, because of the low-bit-sampling characteristic of the IR-UWB system, non-time-interleaved structure is used without digital calibration which largely saves the power consumption, chip area and cost. And a differential resistive reference ladder is designed to minimize the inaccuracy of the reference voltage. The proposed ADC dissipates 34mW power from a 1.8V supply while operating at 4GHz. This chip has been fabricated in 0.18 μm 1P6M CMOS process and the ADC achieves 1.86-bit effective number of bits (ENOB) for input signal of 1GHz at 4GS/s in simulation of FFT analysis.

Keywords: UWB, flash ADC, low-swing, CML

1. Introduction

UWB is an exciting new wireless technology that promises high data rates over short distance by employing sub-nanosecond pulses to carry information and bandwidths in excess of 1 GHz [1]. Due to the unique spectral characteristics of IR-UWB signals and their high instantaneous SNR (Signal-to-Noise Rate), it can be demonstrated that reliable detection of a UWB signal can be performed with very few bits of resolution in the ADC. In fact, earlier simulation work reveals that 2 bits is sufficient. The function of this ADC is receiving the impulse signals demodulated by down-mixer with bandwidth of 10M-1GHz.

The flash ADC is a suitable choice when high speed and low to moderate resolution is required. As the resolution required by this IR-UWB system is low, non-time-interleaved architecture is adopted in this design. Time-interleaved architectures usually require digital calibration methods because of the gain and offset mismatches among the different ADC channels, which significantly increase the power and area of the flash ADC [2, 3]. Therefore, no digital calibration is required, resulting in substantial saving in power and area.

In the proposed architecture, a speed of 4GS/s is achieved based on differential low swing operation in the analog part and CML in digital part. The differential output signals are then converted to LVDS logic level and feed into the FPGA in base band for further processing.

This paper is organized into 5 sections. The architecture of the ADC is presented in Section 2. Circuit descriptions are presented in Section 3. Simulation results are demonstrated in section 4. Finally, conclusions are drawn in section 5.

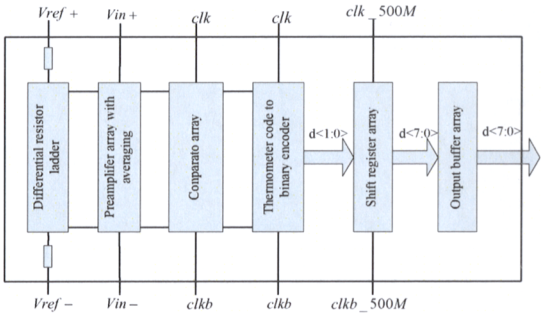

Figure 1. Architecture of the proposed ADC

2. Architecture of the proposed ADC

Fig. 1 presents a block diagram of the proposed 2-bit ADC and the output circuit. The differential resistive reference ladder generates tap voltages from two clean reference voltages, Gnd and Vdd. There are 3 comparators comparing the input in parallel with the tap voltages and generating the thermometer code. Then a current-mode logic (CML) encoder converts the thermometer code generated by all the comparators into a binary code that approximates the input signal every clock cycle through an intermediate code. In order to process the high-speed data in digital domain in base band, the output circuit converts the 4GHz signals into 500MHz signals after the conversion.

3. Circuit descriptions

3.1 Differential resistive reference ladder design

The resistance value of the ladder has to be small. The

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small the resistance, the less effect of the problem of ladder feed-through which is describes by Fig. 2 [4]. However, obviously a small resistance results in high power consumption. In the worst case, the feed-through from the input to the midpoint of the ladder can be calculated as follow [5, 6]:

$$\frac{V_{MID}}{V_{IN}} = \frac{\pi}{4} f_{IN} RC \qquad (1)$$

where C is the total capacitance from the input to the resistive ladder and f_{IN} is the input frequency. With this formula, the maximum ladder resistance can be calculated for which the feed-through does not degrade the performance and at the same time gives rise to certain minimum power consumption in the reference ladder. The total resistance of the ladder is approximately 400 Ω in this ADC.

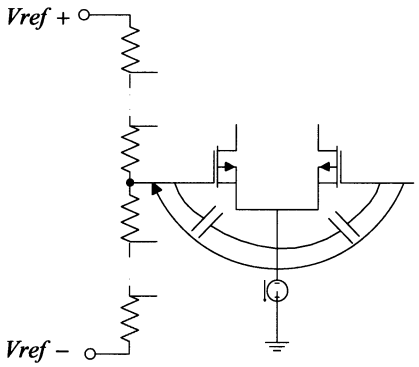

Figure 2. Illustration of the feed-through

In order to minimize the inaccuracy when generating the reference voltages, a differential resistive reference ladder has been designed on chip to decrease the effect of the feed-through. Fig. 3. presents the structure of the differential resistor ladder. Simulation of the reference voltage shows that the inaccuracy is controlled under several mVs. The effect of the feed-through has been counteracted as $Vref+$ and $Vref-$ tapped from the differential reference ladder, as Fig. 4. shows.

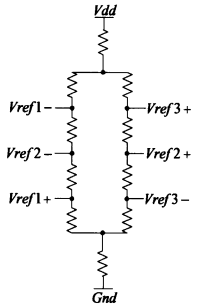

Figure 3. Architecture of the differential reference ladder

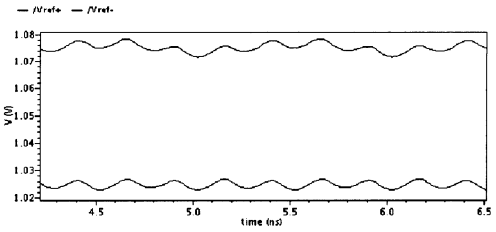

Figure 4. Simulation of $Vref+$ and $Vref-$

3.2 Comparator circuit

The basic idea of the comparator is sacrificing the gain to achieve wide bandwidth of input. To implement this idea, a dual differential preamplifier is chosen as shown in Fig. 5 [7]. The architecture shown has four inputs, two are from differential input signals and the others are the differential reference which is tapped off the differential resistive reference ladder. This architecture amplifies the differences of $Vin+$ minus $Vref+$ and $Vref-$ minus $Vin-$ respectively and then amplified to the output. Simulation result of the preamplifier shows the gain is about 3, and the -3dB bandwidth achieves 5GHz.

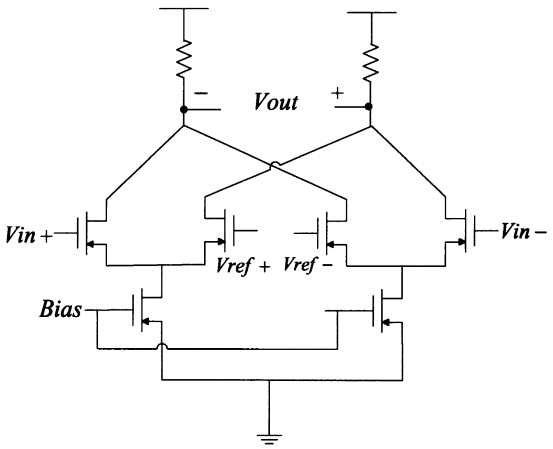

Figure 5. Schematic of the preamplifier

The outputs then feed into the first latch which also acts as a T/H which performs the function of dispute sampling. In the first latch, when the clock goes high, output follows the input. As the clock goes down, the amplified signal is sampled on the output. This process acts as a distributed sampling scheme for the proposed ADC. Due to amplifying-and-latching through the next two lathes the required low swing ($\pm 0.4V$) is achieved at the output of the comparator [7]. Fig. 6. shows the architecture of the latches.

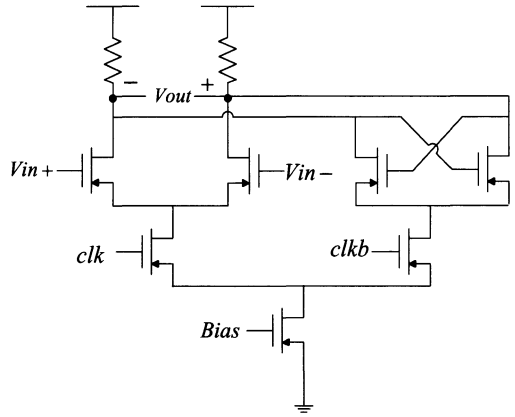

Figure 6. Schematic of the next 3 latches

3.3 Encoder circuit

The output of the comparators is known as thermometer code. For the purpose of minimizing the error of bubbles (or sparkles) in the thermometer code, the outputs first are converted to Gray code and then Binary code [8]. Table 1. shows the encoding process of the encoder.

Table 1. Requirements on text size

Thermometer code (T)	Gray code (G)	Binary code (B)
000	00	00
001	01	01
011	11	10
111	10	11

As the table shows, the encoding process could be summarized as follows:

$$G1 = T2 \qquad B1 = G1$$
$$G0 = T1 \bullet \bar{T3} \qquad B0 = G0 \oplus B1 \tag{2}$$

In order to achieve the high-speed and low-power consumption operation, the low swing circuit is implemented in the analog part and CML blocks in the digital part. The architecture in [8] was chosen which is shown in Fig. 7. The schematics of CML AND gate and XOR gate are presented in Fig. 8. and Fig 9.

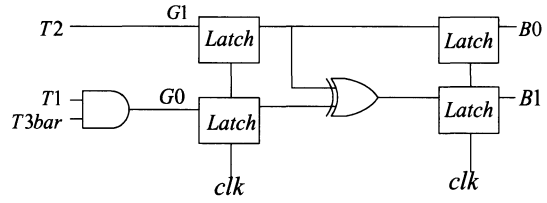

Figure 7. Architecture of the encoder

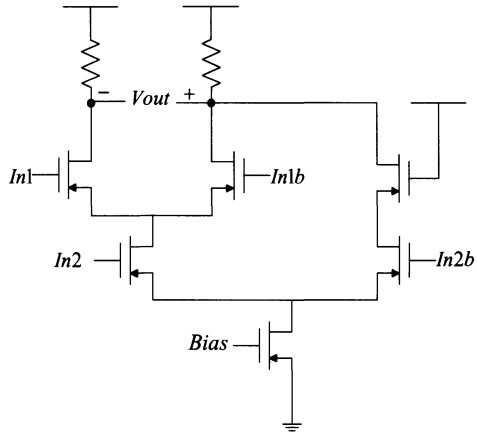

Figure 8. Schematic of the AND gate

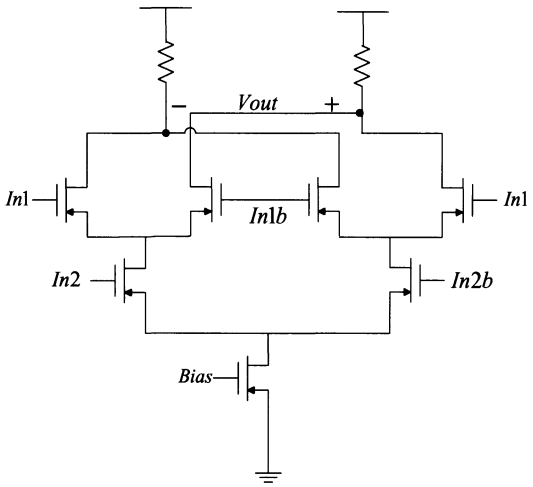

Figure 9. Schematic of the XOR gate

4. Simulation and measurement results

Transient simulation is performed and the result of 1GHz $1\,V_{P-P}$ sinusoidal differential input at 4GS/s is shown in Fig. 10.

Spectral analysis of digitized sine wave using FFT and Blackman window filtering indicate the ADC's dynamic performance consistent with 2-bit operation. For a 1GHz, differential sinusoid input ($1\,V_{P-P}$) quantized at 4GS/s, the SNDR (the ration of signal power to all other power in the output spectrum), is 12.96dB and the ENOB is 1.86bits, as shown in Fig. 11.

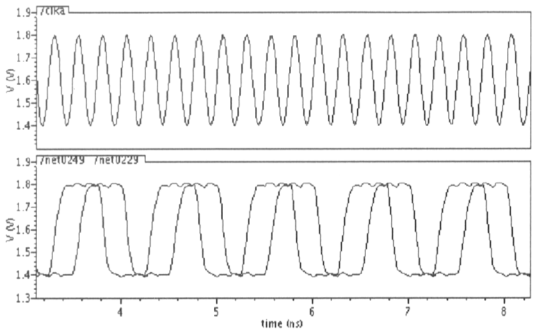

Figure 10. Transient response of when sampling a 1GHz sinusoidal input at 4GS/s

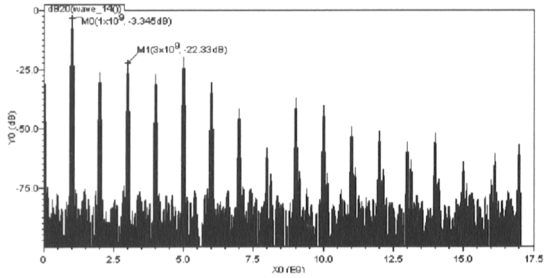

Figure 11. Digital output spectrum from A/D converter when sampling a 1GHz sinusoidal input at 4GS/s

Table 2 demonstrates the performance summary of the proposed ADC. Simulations predict a speed of 4GS/s with a power consumption of 34mW from a 1.8V supply, comparison of several flash ADCs is showed in table 2.

Table 2. Comparison of Performance

	The proposed ADC	ADC in [9]	ADC in [7]
Resolution	2bits	2bits	4bits
Sampling frequency	4GS/s	4GS/s	5GS/s
Power supply	1.8V	± 1.25V	1.8V
Power	34mW	650mW	67mW
Area	0.12 mm^2	5.4 mm^2	0.2 mm^2
SNDR	12.96dB@1GHz input	Not given	23.73dB@DC
ENOB	1.86bits@1GHz input	Not given	3.65bits@DC

5. Conclusion

In this paper, a non-time-interleaved 2-bit flash ADC is presented. Low-swing and CML operation allows easier achievement of high-speed and low power consumption. The proposed ADC achieves an ENOB of 1.86 in simulation of FFT analysis, while consuming low power and area. This design has been submitted for fabrication in SMIC 0.18μm CMOS technology.

Acknowledgments

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