A 1 GHz Bandwidth Low-Pass $\Delta\Sigma$ ADC With 20–50 GHz Adjustable Sampling Rate

Adam Hart, *Student Member, IEEE*, and Sorin P. Voinigescu, *Senior Member, IEEE*

***Abstract*—A low-pass continuous-time delta-sigma data converter with adjustable sampling rate from 20–50 GS/s has been demonstrated in a production 165 GHz-f_T 130-nm SiGe BiCMOS process. The ADC exploits the high transistor f_T of modern silicon technologies to achieve an ENOB of 7 bits over a 500 MHz passband and 6 bits over a 1 GHz passband while consuming 350 mW from a 2.5 V supply (650 mW including on chip clock distribution and output driver); marking the first delta-sigma ADC to reach a bandwidth of 1 GHz. At the system-level, the analysis of a detailed behavioral model brought to light the high dependency of modulator performance on metastability. An analytical expression linking quantizer gain and number of bits to performance was therefore derived and used to estimate the theoretical limitations imposed by metastability.**

***Index Terms*—Analog-digital conversion, continuous-time, delta-sigma, excess loop delay, low-pass, metastability, operational amplifier, radio receivers, SiGe BiCMOS.**

I. Introduction

While the unremitting progress in silicon technology allows for higher levels of integration and digital processing, there is a commensurate increase in performance demand on the ADC. As a result, realizing higher resolution over larger conversion bandwidths is vital to the progress of electronics. Looking at a snapshot of the state-of-the-art shown in Fig. 1, where ADCs are sorted according to resolution and conversion bandwidth, two distinct niches exist. On one side, oversampling converters can offer more than 14 bits of resolution over narrow bandwidths [1], [2] while Nyquist converters can achieve conversion bandwidths above 10 GHz but with significantly lower resolution [3], [4]. Beyond conversion bandwidths of 100 MHz, current ADCs are almost exclusively limited to Nyquist implementations. However, the continued drop in supply voltage and ever-increasing transistor speed of modern silicon technologies strongly favors the use of oversampling architectures which trade-off resolution in amplitude for resolution in time. Continuous-time (CT) delta-sigma modulators ($\Delta\Sigma$Ms), which have relaxed settling-time requirements compared to their discrete-time counterparts, are therefore excellent candidates for high sampling rate ADCs in the hundreds of megahertz passband range.

Manuscript received September 21, 2008; revised December 08, 2008. Current version published May 01, 2009.

The authors are with The Edward S. Rogers, Sr. Department of Electrical and Computer Engineering, University of Toronto, Toronto, Ontario, M5S 3G4, Canada (e-mail: sorinv@eecg.toronto.edu).

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Digital Object Identifier 10.1109/JSSC.2009.2015852

This paper describes the first delta-sigma ADC to reach 1 GHz of bandwidth and high enough resolution for 60 GHz OFDM radio applications. In addition to providing built-in antialias filtering, the CT $\Delta\Sigma$M achieves a comparable figure of merit (FoM) to flash and pipeline ADCs while employing a very simple architecture that requires no self-calibration or other schemes of the sort; demonstrating the first oversampling ADC to compete directly with Nyquist converters in this passband range. Use within a 60 GHz radio receiver employs two ADCs to digitize the I and Q signals; providing 1 GHz of bandwidth for 4 Gb/s 16 QAM. A CT $\Delta\Sigma$M with high sampling rate is particularly well suited for this application since a high frequency clock is already available from the 60 GHz front-end.

The paper is organized as follows. Section II begins with the system-level design of the ADC; presenting the loop filter architecture, a new high-speed integrator topology and a detailed behavioral model implemented in Matlab and Simulink. The section concludes with an analysis of metastability including the derivation of an analytical expression linking quantizer gain and number of bits to performance. In Section III, the schematic design of key circuit blocks is described followed by Section IV where measurement results of a SiGe BiCMOS ADC test chip and a comparison to other state-of-the-art ADCs are provided.

II. System-Level Design

A. ADC Topology

The system-level architecture of the ADC is shown in Fig. 2 and consists of two integrators with three feedback paths from a single-bit quantizer. In order to achieve 6 effective number of bits (ENOB) over a 1 GHz bandwidth, a theoretical oversampling ratio (OSR) of 12 is required [6]. Allowing for some margin, an OSR of 20 is used; corresponding to a 40 GHz sampling rate which is feasible in the 165-GHz f_T SiGe BiCMOS implementation technology. Employing a low-complexity single-bit, second-order topology greatly facilitates the circuit-level implementation of high-speed blocks at these frequencies. The corresponding noise transfer function (NTF) and signal transfer function (STF) are

$$\mathrm{NTF}(s) = \frac{s^2}{s^2(1+a_3) + a_2c_2s + a_1c_1c_2} \quad (1)$$

$$\mathrm{STF}(s) = \frac{c_1c_2}{s^2(1+a_3) + a_2c_2s + a_1c_1c_2} \quad (2)$$

respectively. Coefficients a_1 and a_2 set the poles of both the NTF and STF while a_3 is used to compensate for excess loop

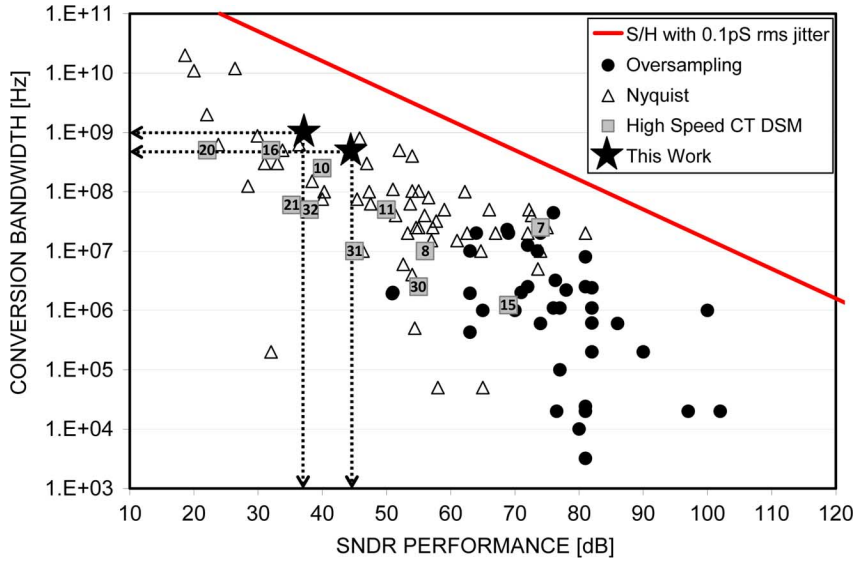

Fig. 1. ADC performance survey including all designs published in the International Solid-State Circuits Conference from 2003 to 2008 (adapted from [32]). Labels correspond to reference numbers and the benchmark corresponds to the maximum theoretical resolution possible using a sample and hold with 0.1 ps of rms jitter [33].

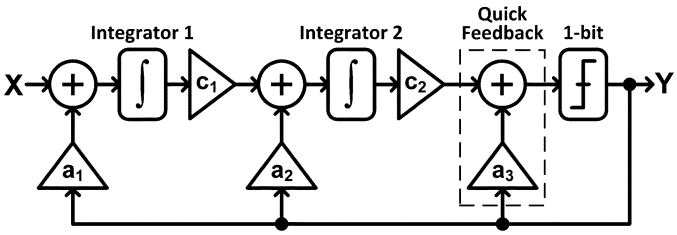

Fig. 2. Proposed second-order CT $\Sigma\Delta$ ADC architecture.

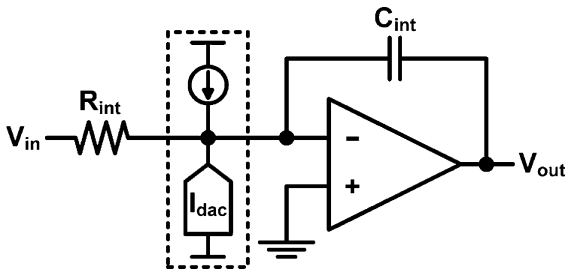

Fig. 3(a). Commonly used opamp-based integrator topology. The feedback DAC adds or subtracts a fixed current at the input of the integrator.

delay [5]. It is worth noting that this architecture does not support complex conjugate zeroes in the NTF since there is no local feedback path around the integrators. As a result, the NTF zeroes cannot be spread across the signal passband to minimize the quantization noise root-mean-square power. Employing optimally placed zeroes can increase the SQNR by up to 3.5 dB; nonetheless, they have a far more pronounced effect in higher order modulators [6]. On the other hand, having both NTF zeroes at DC allows for a programmable clock in the modulator because their location does not change with respect to the sampling rate.

B. High-Speed Integrator Topology

There are two common approaches to implement loop filters in CT $\Delta\Sigma$ modulators: active-RC using opamp-based integrators [7]–[9] and Gm-C using operational transconductance amplifiers (OTA) [10]–[12]. The main advantage of Gm-C filters is their amenability to high-speed design since their OTAs operate in open-loop. Unfortunately, nonlinearity is the major drawback of this approach [13] and has limited their use to InP and GaAs technologies where the absence of complementary devices often precludes opamps. With this in mind, a new opamp-based integrator topology is presented here that achieves two objectives: (i) is suitable for high-speed applications and (ii) can operate from a low power supply. A folded-cascode opamp is a good candidate for both criteria; however, it is not compatible with the feedback configuration shown in Fig. 3(a). Although widely used, this configuration requires a high DC voltage level at the input of the opamp so that there is enough headroom to operate the high-speed digital-to-analog converter (DAC). A more feasible location to connect the feedback is at the high impedance output node of the opamp, as shown in Fig. 3(b). In addition to providing ample voltage headroom for the feedback, this configuration merges the current sources for the opamp and feedback DAC. The current mismatch introduced by the DAC is corrected by the common-mode feedback of the opamp through transistors M1 and M2. Furthermore, the integration capacitor $C_{\rm int}$ is connected between the high-impedance node and analog ground, thus doubling as a compensation capacitance for the opamp. Another advantage of the topology is that the output is at the same common-mode voltage as the input; facilitating the cascading of stages without the need for level shifting.

The behavioral model of the opamp shown at the bottom of Fig. 3(b) is employed in system-level simulations. Parameters $R_{\rm o}$ and $C_{\rm o}$ represent the finite impedance and capacitance at nodes Von and Vop while $g_{\rm m}$ is the transconductance of the input transistors M5 and M6. The gain of the integrator is largely dependent on $R_{\rm int}$ and $C_{\rm int}$. Since noise added to the input of the

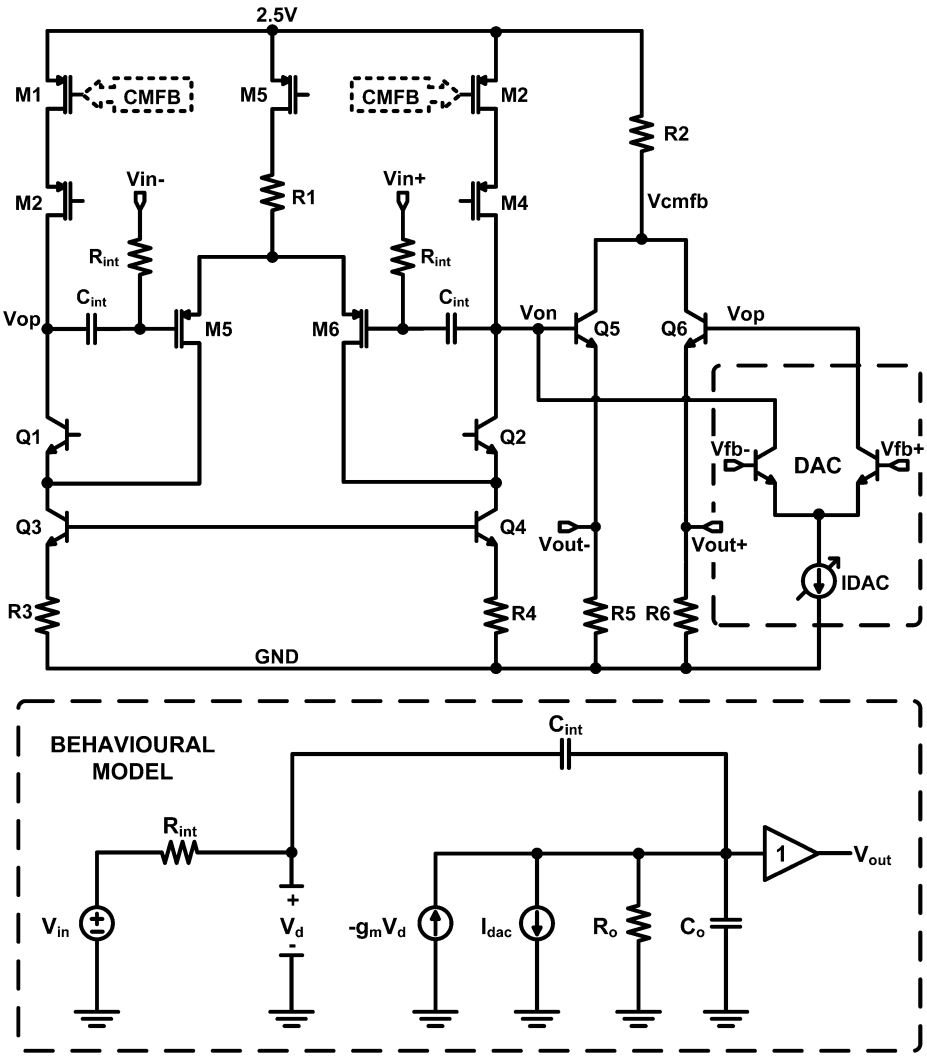

Fig. 3(b). Proposed opamp-integrator schematic and behavioral model.

circuit is not noise-shaped, $R_{\rm int}$ must be made as small as possible while the size of $C_{\rm int}$ must be limited in order to avoid slewing. In this design, both stages use 50 Ω resistors for $R_{\rm int}$ and have a g_m of 30 mS in combination with integration capacitors of 500 fF and 250 fF for the first and second stage respectively. The linear signal transfer function of the model is

$$V_{\rm out} = -\frac{V_{\rm in}\cdot g_m R_o + I_{\rm DAC}\cdot R_o(sR_{\rm int}C_{\rm int}+1)}{s^2R_{\rm int}C_{\rm int}R_oC_o+s(R_{\rm int}C_{\rm int}+R_oC_o+R_{\rm int}C_{\rm int}R_og_m)+1}. \quad (3)$$

Despite the extra pole and zero in (3), $R_{\rm int}$ and $C_{\rm int}$ can be designed to implement an integrator within a frequency range limited by the opamp gain and bandwidth.

C. Behavioral Model

A detailed behavioral model of the ADC is implemented in Matlab and Simulink in order to validate the design and study the impact of circuit non-idealities on performance. The model includes independently-controlled parameters for finite opamp gain, bandwidth and slew rate, quantizer gain and hysteresis, feedback delay, and finite voltage swing at critical nodes. All blocks are described in the discrete-time domain and are evaluated with a fixed-step solver in order to circumvent simulation errors. In order to accurately model the integrators, transfer function (3) is mapped to the discrete-time domain using the bilinear transform and incorporated into the behavioral model.

A single Matlab function is used to coordinate each step of simulation. The process begins by computing a target NTF with the Schreier toolbox [6] and mapping it into the feedback coefficients a_1a_2 and a_3 in (1) using the impulse invariant transform as described in [5]. Simulink then runs a transient simulation using the behavioral model and a coherent sinusoidal input (usually at one third the cutoff frequency so that second and third harmonics fall in-band), culminating in a pulse-width-modulated output stream that is fed back into Matlab for analysis. A Hann window is applied to the samples to subdue spectral leakage and the power spectral density is obtained as shown in Fig. 4 for the final system-level design.

D. Metastability Analysis

The behavioral model is used to evaluate the impact of each non-ideality on ADC performance. Among all the modeled pa-

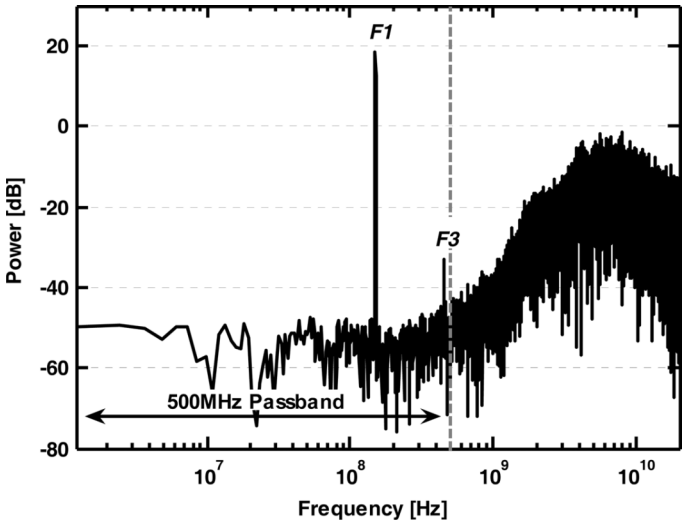

Fig. 4. Simulated power spectral density of the ADC output for a 150 MHz input and 40 GHz sampling clock ($N_{\mathrm{FFT}} = 32768$). In this simulation, the feedback coefficients are set for 500 MHz pass-band.

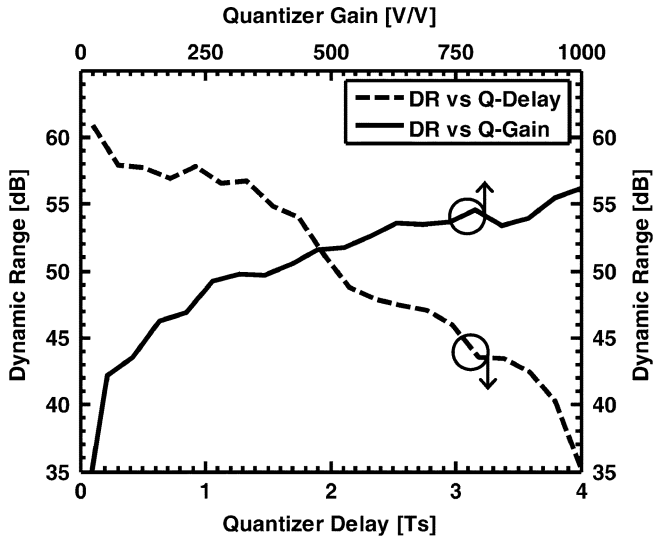

Fig. 5. Tradeoff between quantizer gain and loop delay on the ADC's dynamic range performance (note that both are plotted independently). Performance for a given quantizer gain and delay will be limited by the lesser value of their corresponding dynamic ranges. The optimum quantizer design can therefore be determined by establishing the gain and delay at which the dynamic range is limited equally by metastability and loop delay.

rameters, quantizer gain and delay are most critical and are plotted independently in Fig. 5. At low gain, the dynamic range is limited by metastability, especially because the quantizer is single-bit and samples at extremely high speed. As preamplifiers and latches are cascaded together to increase quantizer gain and improve metastability, the cumulative delay introduced by each block eventually limits performance. Optimizing the tradeoff between quantizer gain and delay is therefore paramount to achieving high performance at mm-wave sampling frequencies.

The problem of metastability in CT $\Delta\Sigma$Ms is well known [10], [14]–[16] and has been studied empirically in [17] by considering the effect of finite quantizer gain as a variation on the DAC zero-crossing time. In this section, we analyze metastability from the perspective of errors in the output bit-stream and derive, for the first time, an analytical expression which links quantizer gain to performance.

Metastability occurs when an input to the quantizer is so close to a decision level that neither a high nor low is reached at the output. As shown in Fig. 6 for a single-bit quantizer, there are two outputs which have not attained a valid logic level at the sample time $(\mathrm{T_{sample}})$. These in-between outputs are then fed back through the DACs in an analog fashion (i.e., without fully switching the DACs). Meanwhile, the decimation circuit will inevitably convert each metastable output to a valid digital level, essentially cleaning-up the output as illustrated in the third waveform in Fig. 6. Correcting metastable outputs turns out to be a major problem. The power spectral density of the difference between the analog and digital outputs (hereinafter called the residue) results in a white noise floor that falls in-band. The mean square power of this noise floor depends solely on the number of metastable outputs and their amplitude. To demonstrate this effect in a CT $\Delta\Sigma$M, the behavioral model is simulated with a finite quantizer gain of 800 V/V. Of the 32 768 output samples, only 153 (0.5%) fail to reach a digital logic level. If these metastable outputs are left uncorrected, the spectrum shown at the top of Fig. 7 is obtained and is denoted as the analog output because it includes metastable samples that are in-between valid logic levels. If the 153 metastable outputs are corrected, as they would be after passing through the digital circuitry which follows the ADC, a residue signal is obtained (consisting of the corrections). Unfortunately, this residue has a white power spectral density as shown in the second spectrum in Fig. 7. Once the metastable samples are corrected and the output is interpreted digitally, the residue noise floor is superimposed atop the analog spectrum; resulting in the severely degraded ADC performance shown at the bottom of Fig. 7.

The effect of metastability can be described analytically by assuming (i) signals at the input of the quantizer are randomly distributed between $\pm\mathrm{V_{FS}}/2$ where $\mathrm{V_{FS}}$ is the full-scale voltage, (ii) the quantizer can be approximated to have a linear gain[1] G_{Q}, and (iii) metastable outputs of the quantizer are eventually corrected to the nearest valid logic level by the digital circuitry that follows the ADC. The first assumption is verified with transistor-level simulations and makes sense intuitively because the feedback and integrators act in a way that decorrelates the quantizer input from the modulator input to the degree that it appears random [17]. A corollary of (i) is that inputs within the metastable region of the latch are uniformly distributed. Following a stochastic approach, the metastability error signal, $\mathrm{V_M}$, is characterized by a random variable uniformly distributed between $\pm\mathrm{V_{LSB}}/2$ where

$$V_{\mathrm{LSB}} = \frac{V_{\mathrm{FS}}}{2^N} \tag{4}$$

[1]The quantizer gain is defined as the voltage gain from input to output of the entire quantizer while operating in the metastable region (the gain will therefore depend on the gain of each stage, the number of stages, the regeneration time and clock period of the quantizer).

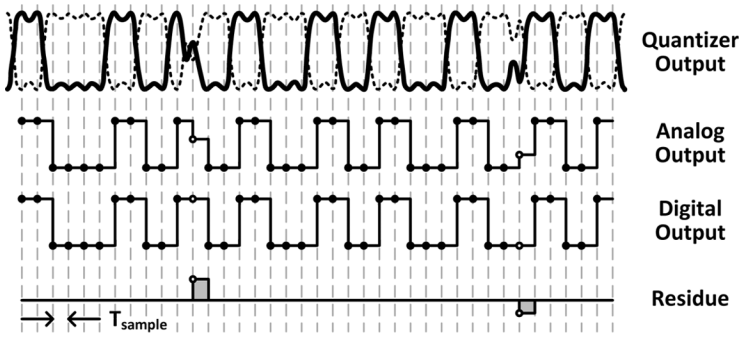

Fig. 6. From top to bottom: output waveforms of a single-bit quantizer with metastable outputs, analog interpretation (before metastable errors have been corrected), digital interpretation (after metastable outputs have been corrected to nearest digital level) and residue (difference between the analog and digital signals).

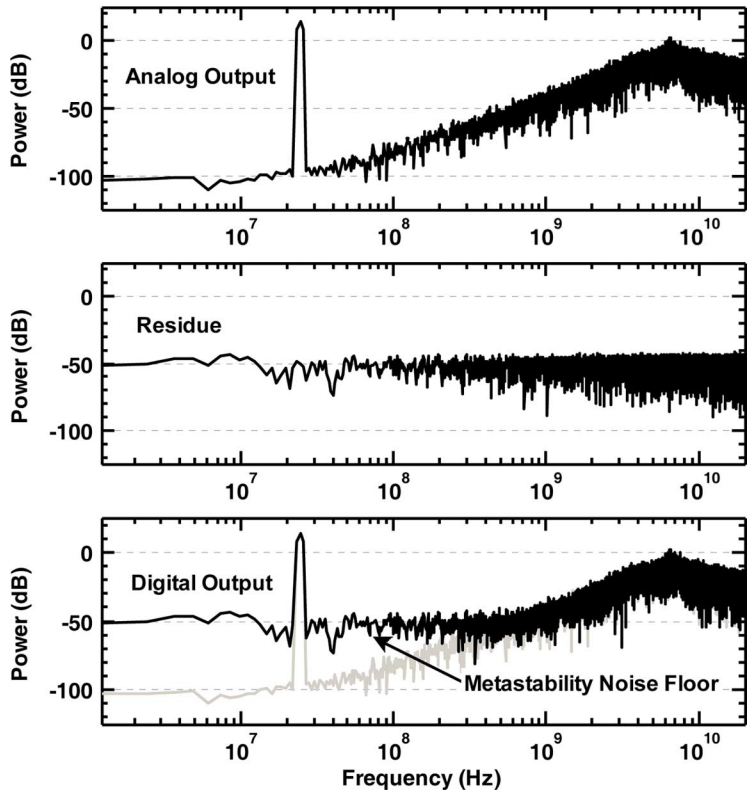

Fig. 7. Power spectral density of the analog output (top), residue (middle) and digital output (bottom). Note that correcting metastable outputs is equivalent to summing the top and middle spectra together to yield the digital output shown on the bottom. The spectra were obtained by simulating the behavioral model with $F_S = 40$ GS/s, $N_{\mathrm{FFT}} = 32768$, and $G_Q = 800$ V/V).

and *N* is the number of bits in the quantizer. The probability of obtaining a metastable output is

$$p_M = 1 - \left(\frac{V_{\mathrm{LSB}} - \frac{V_{\mathrm{LSB}}}{G_Q}}{V_{\mathrm{LSB}}} \right) = \frac{1}{G_Q} \tag{5}$$

which is independent of the logic level and number of bits. The corresponding probability density function $\mathrm{f_M(x)}$ is described by

$$f_M(x) = \frac{1}{V_{\mathrm{LSB}} G_Q} \text{ where } x \in \left[-\frac{V_{\mathrm{LSB}}}{2}, \frac{V_{\mathrm{LSB}}}{2} \right] \tag{6}$$

and the rms value of the metastability error signal is given by

$$V_{M(\mathrm{rms})} = \left[\int_{-\infty}^{\infty} x^2 f_e(x) dx \right]^{1/2} = \left[\frac{1}{V_{\mathrm{LSB}} G_Q} \int_{-V_{\mathrm{LSB}}/2}^{V_{\mathrm{LSB}}/2} x^2 dx \right]^{1/2} = \frac{V_{\mathrm{LSB}}}{\sqrt{12 G_Q}}. \tag{7}$$

Note that integrating (6) over the entire voltage range equates to p_M, the total probability of having a metastable output. It is now possible to relate metastability to performance assuming a

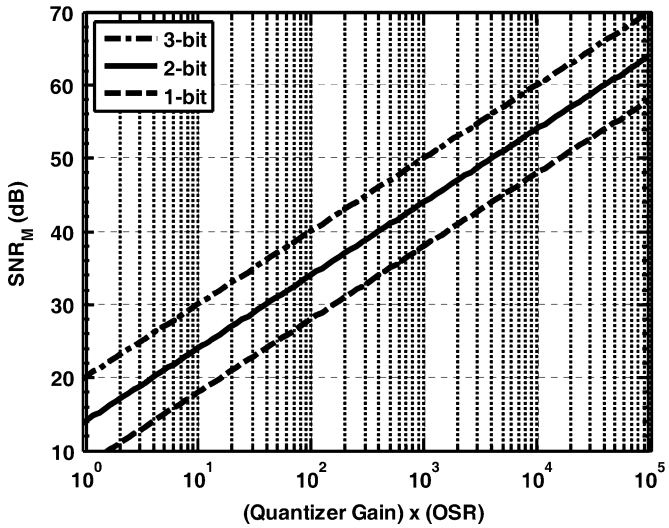

Fig. 8. Maximum achievable SNR for a given OSR, quantizer gain and number of bits.

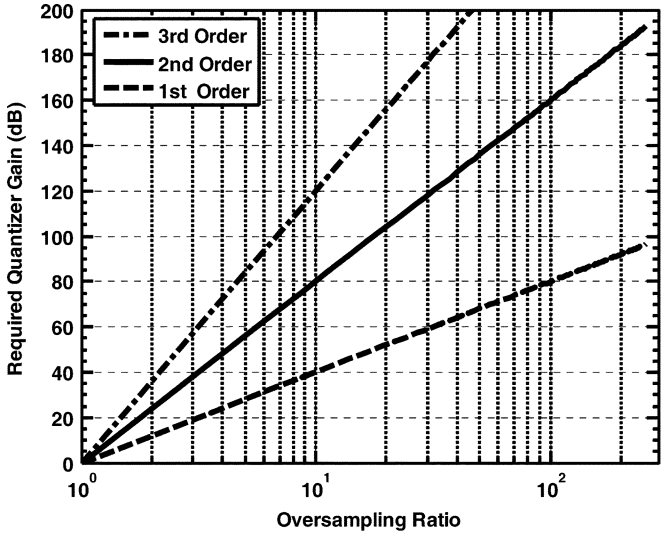

Fig. 9. Required quantizer gain to equate the metastability noise floor to the quantization noise floor for a given OSR.

full-scale sinusoidal input. The signal-to-noise ratio (SNR) due to metastability is given by

$$\begin{aligned}\mathrm{SNR}_M &= 20\log\left(\frac{V_{\mathrm{in(rms)}}}{V_{M(\mathrm{rms})}}\right)\\ &= 20\log\left(\frac{V_{\mathrm{FS}}}{2\sqrt{2}}\frac{\sqrt{12G_Q}}{V_{\mathrm{LSB}}}\right) \qquad (8)\end{aligned}$$

$$\mathrm{SNR}_M = 10\log(G_Q) + 6.02N + 1.76\ \mathrm{dB}. \qquad (9)$$

Since there is still a 3 dB per octave performance improvement from oversampling the white metastablity noise, the OSR is included in (9), producing

$$\mathrm{SNR}_M = 10\log(\mathrm{OSR}\cdot G_Q) + 6.02N + 1.76\,\mathrm{dB} \qquad (10)$$

which represents the maximum achievable SNR for a given OSR, quantizer gain and number of bits as plotted in Fig. 8. The overriding influence of metastability on CT $\Delta\Sigma$M performance is highlighted by the fact that (10) is independent of modulator order. The correction of metastable outputs, or equivalently, the modulation of the DAC zero-crossing times result in a white noise floor that is not shaped by the loop filter. As a result, the quantizer gain required to suppress metastability below the quantization noise floor is an exponential function of the OSR. Expressed mathematically, the signal-to-quantization noise ratio (SQNR) for a first order modulator [6] is equated to (10) and solved for G_Q:

$$\begin{aligned}&30\log(\mathrm{OSR}) + 60.2N - 5.17\\ &\quad = 10\log(\mathrm{OSR}\cdot G_Q) + 6.02N + 1.76\ \mathrm{dB} \qquad (11)\\ &G_Q = \mathrm{OSR}^2 + 0.304. \qquad (12)\end{aligned}$$

The relationship is generalized for an Mth-order modulator by

$$G_Q \cong \mathrm{OSR}^{2(M+1)} \qquad (13)$$

and is plotted in Fig. 9 for first, second and third order loops. The challenge of realizing high quantizer gain at GHz-sampling frequencies in addition to the limitations imposed by excess loop delay make CT $\Delta\Sigma$Ms impractical at high oversampling ratios. As was aptly noted in the performance survey of GHz-speed modulators in [18], there are diminishing benefits from oversampling beyond an OSR of approximately 15.

III. Circuit-Level Design

A block diagram of the ADC is shown in Fig. 10 where second-order noise shaping is achieved by cascading two opamp-based integrators (described in Section II.B) with feedback from DAC1 and DAC2. Two versions of the ADC are implemented in order to investigate the tradeoff between quantizer gain (metastability) and loop delay. As shown in the figure, *ADC1* has one more latch than *ADC2* with all else being equal. The 3-latch version is expected to be limited by metastability while the 4-latch version is expected to be limited by excess loop delay (refer to Fig. 5). To allow for adjustable sampling, the DAC currents are implemented with tuning so that stability and the desired NTF can be realized over a larger range of sampling frequencies. Measurement results presented in Section IV will demonstrate stable operation from 20–50 GS/s marking the highest sampling clock ever used in a $\Delta\Sigma$ ADC [19]–[21].

A. Operational Amplifier

The operational amplifier (opamp) is one of the most important building blocks in analog and mixed-signal circuits. In the ADC, it is used to implement the new integrator topology described in Section II.B. While nm-scale silicon technologies provide the opportunity for high operating speeds and integration, several major analog design impediments have come to a head: (i) the ever-increasing output conductance of the CMOS transistor leads to very low gain per amplifier stage, (ii) lower supply voltages reduce signal swing and (iii) increasing gate

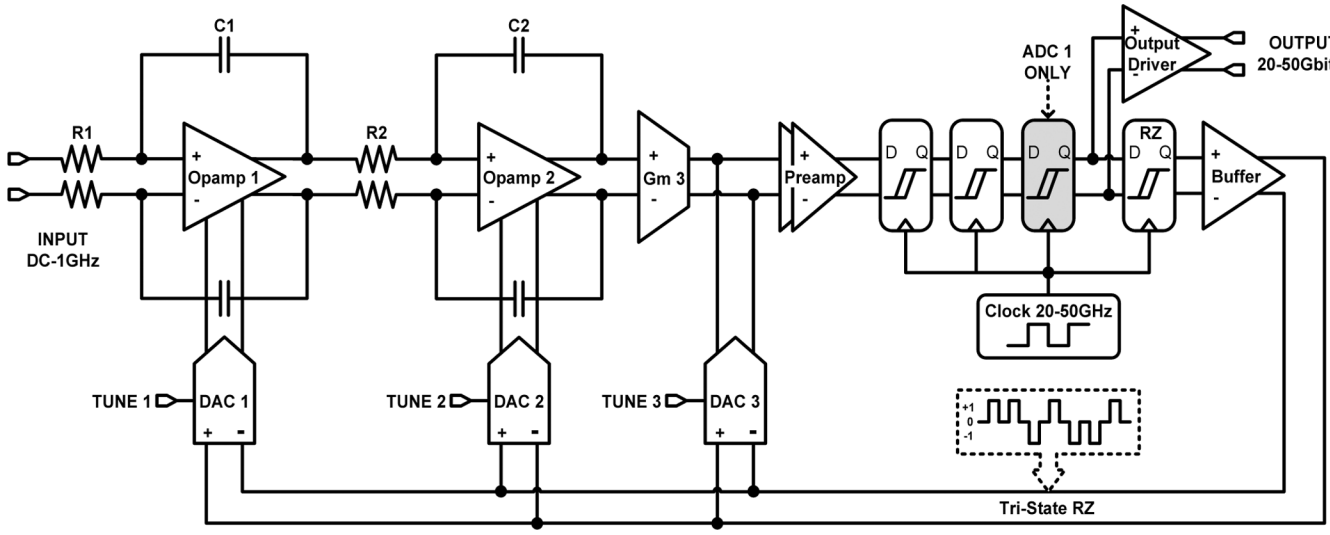

Fig. 10. Top-level block diagram of the 20–50 GS/s low-pass delta-sigma ADC.

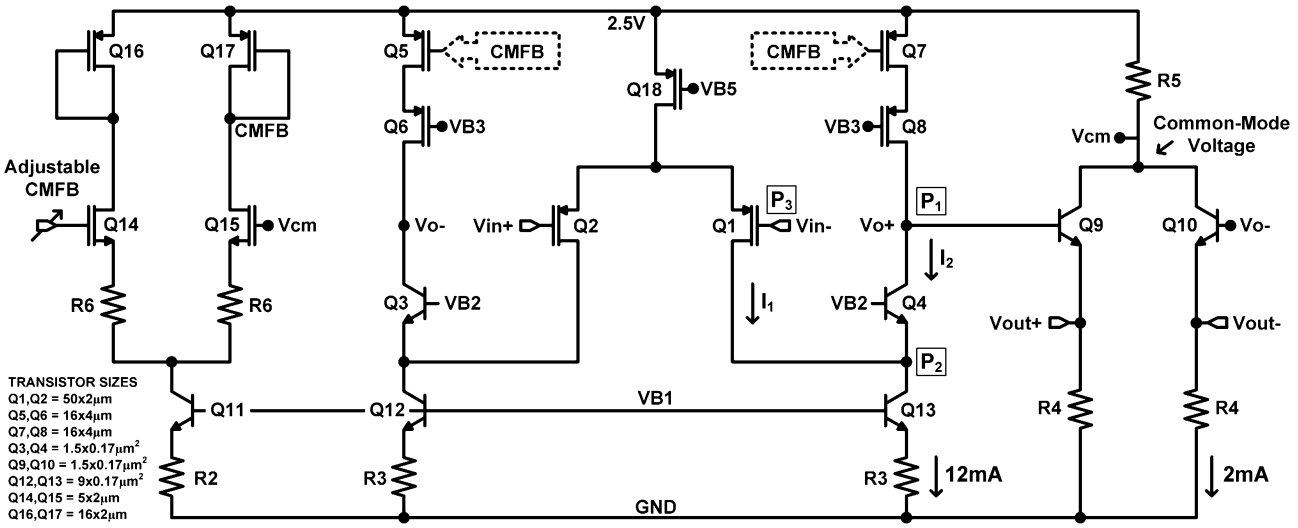

Fig. 11. Schematic of folded-cascode amplifier core (bias network not shown).

leakage currents exacerbate mismatch [22]. A BiCMOS technology is an attractive choice for implementing high performance opamps because the bipolar device can mitigate some of the aforementioned non-idealities and continues to have higher speed than 65-nm CMOS [23]. However, most BiCMOS HBT designs implemented to date require supply voltages of 3.3 V or more [24]–[26].

In this work, we modify the NMOS-HBT telescopic cascode topology described in [24] to operate from a 2.5 V supply. The new amplifier consists of a folded-cascode with pMOS inputs, an emitter-follower output stage and common-mode feedback (CMFB) as shown in Fig. 11. Despite the significantly lower speed and transconductance of the pMOS input transistors, the new design experiences a nominal degradation in bandwidth while consuming less power, achieving higher gain and operating from a lower supply. pMOS inputs must be used because an NMOS-HBT combination is not compatible with a folded design. Despite the lower transconductance of the pMOS transistors Q1 and Q2, a folded-cascode topology allows different values for bias currents I_1 (input MOSFETs) and I_2 (cascode HBTs). The transconductance is therefore easily compensated by increasing the bias current I_1. The current in the outer branch, I_2, must be large enough to meet the desired slew rate criteria but is otherwise minimized to reduce power consumption and parasitic capacitance at nodes P_1 and P_2. The ratio of I_1 to I_2 is therefore critical in determining the gain $(\mathrm{A_V})$, 3 dB-bandwidth (f_{P1}) and slew-rate (SR) of the amplifier as described by the following design equations:

$$Av = -g_{m,Q2}R_1, \quad f_{P1} = \frac{1}{2\pi \cdot R_1 \cdot C_1} \tag{14}$$

$$\mathrm{UGB} = \frac{g_{m,Q2}}{2\pi \cdot C_1}, \quad \mathrm{SR} = \frac{\min\{I_1, I_2\}}{C_1} \tag{15}$$

where the impedance and capacitance of the dominant pole at node P_1 are approximated by

$$\begin{aligned} R_1 &= R_{\mathrm{load}} || R_{\mathrm{cascode}} || R_{\mathrm{buffer}} \\ &\cong (r_{o7} r_{o8} g_{m8} || \beta \cdot r_{o2} || \beta(r_{E9} + R_4)) \end{aligned} \tag{16}$$

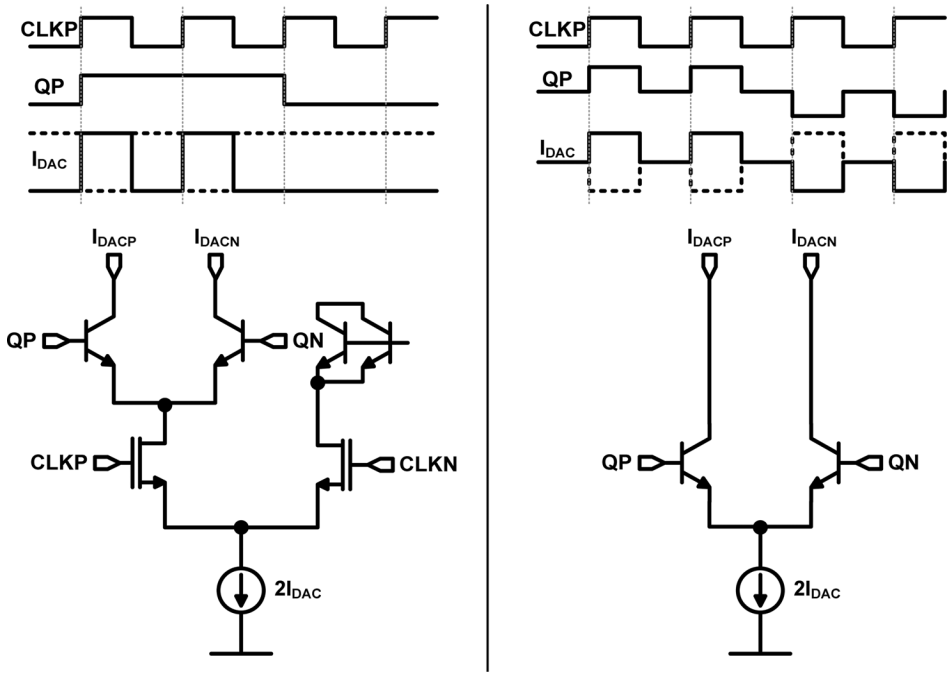

Fig. 12. Comparison between current steering DAC (left) and tri-state DAC (right).

$$C_1 = (C_{\rm DB} + C_{\rm GD})_{Q8} + (C_\mu + C_{\rm CS})_{Q4} + (C_\pi + C_\mu)_{Q9}. \quad (17)$$

In this implementation, a ratio of 5 is used where I_1 is 10 mA and I_2 is 2 mA.

The phase margin of the amplifier is limited by nodes P_2 and P_3 which introduce two parasitic poles described by

$$f_{P2} \cong \frac{1}{2\pi \cdot r_{E,Q4}[(C_{\rm DB}+C_{\rm GD})_{Q2}+(C_{\rm BC}+C_{\rm CS})_{Q13}+(C_{\rm BE})_{Q4}]} \quad (18)$$

$$f_{P3} \cong \frac{1}{2\pi \cdot (R_G+R_S)_{Q1}(C_{\rm GS}+C_{\rm GD})_{Q1}}. \quad (19)$$

In order to guarantee stability and maximize the unity-gain bandwidth of the opamp, the transistors in the signal path are biased at peak $f_{\max}$ current density [24] corresponding to 0.1 mA/μm for transistors Q1–Q2 and 6 mA/μm^2 for transistors Q3–Q4. The emitter followers Q9 and Q10 are biased at a slightly lower current density in order to avoid instability. Biasing at these current densities also helps to immunize the circuit against pMOS threshold voltage variations and improves the linearity of the amplifier [24]. As the current density through the active loads Q5–Q6 and Q7–Q8 increases towards peak $f_{\max}$, the parasitic capacitance introduced at P_1 is minimized (thereby increasing the opamp bandwidth) but the impedance of the load decreases (thereby decreasing the gain). The active loads are therefore biased at half peak $f_{\max}$ current density as a compromise between bandwidth and gain.

B. Digital-to-Analog Converter

Each of the three feedback paths in the ADC is implemented by a high-speed DAC which translates the digital output into a continuous-time current. For 40 GS/s operation, values of ± 2 mA, ± 3 mA and ± 2 mA are needed for the first, second and third stages respectively in order to realize the desired NTF and ensure loop stability. Careful implementation of the DAC is critical in $\Delta\Sigma$ modulators since nonlinearities, noise and offsets introduced in the feedback are not shaped away from the signal passband [5], [6]. Considering the very high sampling rate of the ADC, a simple and inherently linear single-bit return-to-zero DAC is employed.

There are two popular implementations: (i) the current steering DAC [10], [19] and (ii) the tri-state DAC [27], [28]. The functionality and characteristics of both topologies are compared in Fig. 12. The tri-state DAC is essentially a differential pair that is operated in three modes: (i) $2I_{\rm DAC}$ switched to one side, (ii) $2I_{\rm DAC}$ switched to the other side, and (iii) $2I_{\rm DAC}$ split evenly on either side. Switching between these states is achieved by embedding the clock into QP and QN with a tri-state latch (described in Section III.C). Despite perfect linearity, the current steering DAC requires a 40 GHz clock and consumes too much headroom to be used inside the integrator. Instead, the tri-state DAC is used to implement all three DACs where careful layout helps to minimize offsets introduced by process variation. Operation at 40–100 Gb/s is achieved by biasing the switching HBT transistors at 6 mA/μm^2 (when the current is switched to one side) with 1 V of $V_{\rm ce}$.

C. Quantizer

In Section II.C, metastability and loop delay are shown to have a major impact on modulator performance. System-level simulations stipulate a gain of at least 600 V/V and delay of no more than 1.5 $T_{\rm sample}$ are needed in order to reach the targeted performance (refer to Fig. 5). The quantizer shown in Fig. 12 consists of two (ADC2) or three (ADC1) latches followed by a return-to-zero latch and a buffer that drives the three DACs in

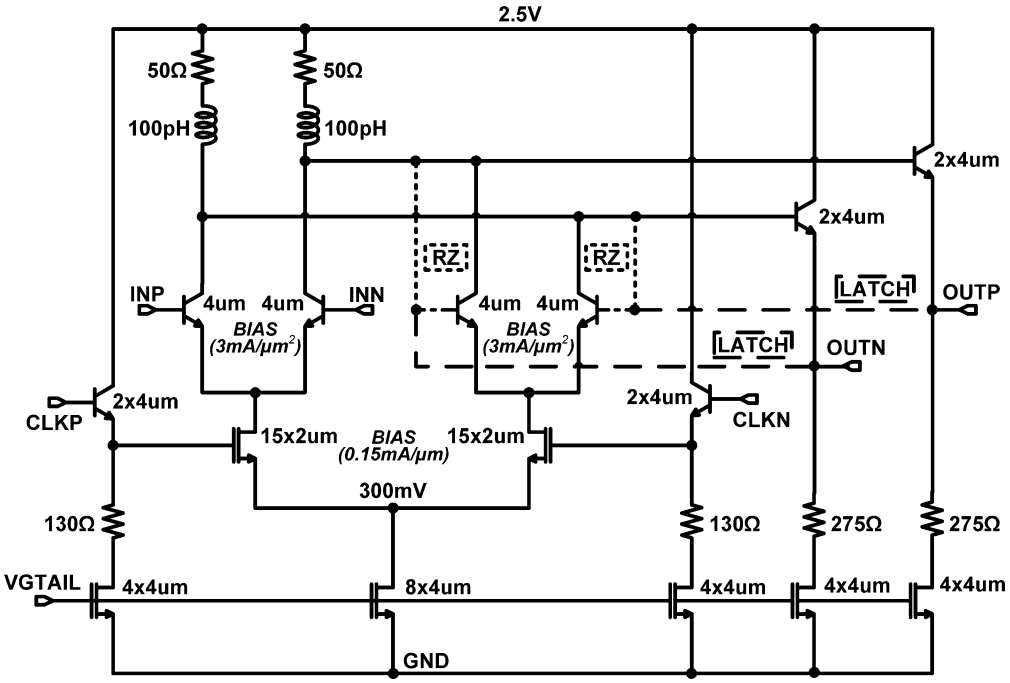

Fig. 13. Quantizer latch schematic (RZ configuration shown with dotted lines, latch configuration shown with dashed lines).

the feedback path. An output driver is connected before the RZ latch and delivers the 20–50 Gb/S NRZ digital signal off-chip.

A two-stage preamplifier serves two important functions: (i) for small inputs, it supplements gain to the quantizer and (ii) for large inputs, it limits the voltage swing so that the transistors in the first latch are not pushed out of the active region. The latter role is especially important since the voltage swing before the preamplifier is more than 1 $V_{\rm pp}$. Both stages are implemented as HBT-differential pairs with transfer function

$$A_V = \frac{g_{m,\rm eff}R_L}{1+s[R_\pi(C_\pi+C_\mu(1+g_{m,\rm eff}R_L))+R_L(C_\mu+C_{\rm CS}+C_L)]} \tag{20}$$

where the parasitic emitter resistance R_E of the HBT must be taken into account

$$g_{m,\rm eff} = \frac{g_m}{1+g_mR_E}. \tag{21}$$

Assuming an R_E of 9 Ω (typical of a 3.2 μm × 0.17 μm HBT), the preamplifier gain is

$$A_{\rm preamp} = 2\times\frac{g_mR_L}{1+g_mR_E} = \frac{15.2\,\rm V/V}{1.85} = 8.2\,\rm V/V. \tag{22}$$

Adequate bandwidth (beyond 40 GHz) is achieved by employing emitter followers and a peaking inductor of

$$L_P = \frac{C_LR_L^2}{3.1} = 200\,\rm pH. \tag{23}$$

A BiCMOS latch employing MOSFETs on the clock path and HBTs on the data path permits high-speed operation from a 2.5 V supply. If a 5 mA tail current, load $R_{\rm L}$ of 80 Ω and emitter resistance R_E of 9 Ω are employed, the latch gain is approximately

$$A_{\rm latch} = \frac{g_mR_L}{1+g_mR_E} = 4.3\,\rm V/V. \tag{24}$$

Note this calculation is pessimistic because it does not account for any regeneration in the hold phase of the latch. If three latches are used (ADC2), a gain of $8.2\times4.3^3 = 652$ V/V is realized whereas four latches (ADC1) yields a gain of $8.2\times4.3^4 = 2\,800$ V/V. Whether or not it is worth implementing the extra latch for more gain (at the expense of more loop delay) is discussed in Section IV with measurement results. The bandwidth of the latch must be large enough to accommodate the high-speed, CT input and is described by

$$\rm BW_{-3\,dB,LATCH} = 1.6\times\frac{1}{2\pi R_LC_L} = 50\,GHz \tag{25}$$

where peaking inductors are employed (accounted for by the factor of 1.6 in (25)) and

$$C_L = 2C_{\rm CS}+2C_\mu+C_{\rm EF}. \tag{26}$$

The emitter followers provide critical buffering from the latch feedback and next stage.

A tri-state RZ signal is realized in the last quantizer by diode connecting the latching pair [27] as shown in Fig. 13 with dotted lines (the latch is shown with dashed lines). To achieve optimal speed, the MOSFETs are biased at peak-f_T current density and the HBTs are biased at 1.5 peak-f_T current density when all the tail current is switched to one side [29].

IV. Measurement Results

A test chip including two versions of the ADC, a retimer breakout and device test structures was manufactured by STMicroelectronics in a production 130-nm SiGe BiCMOS process

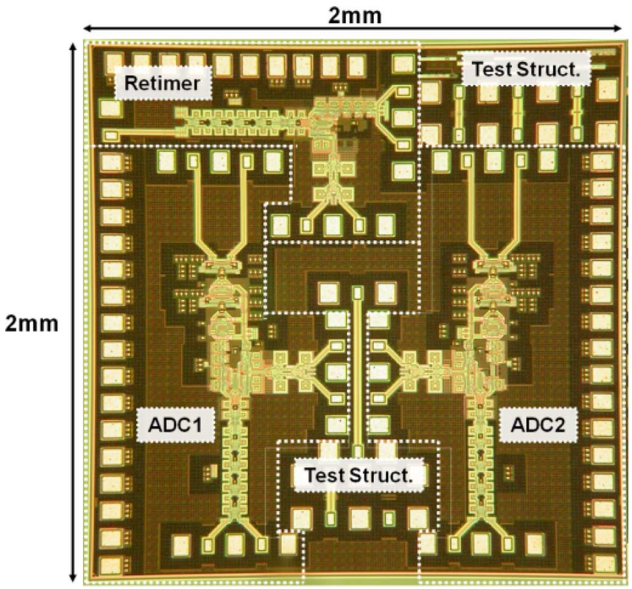

Fig. 14. Low-pass ADC test chip in 0.13-μm SiGe BiCMOS (ADC1 has four latches and ADC2 has three latches in the quantizer).

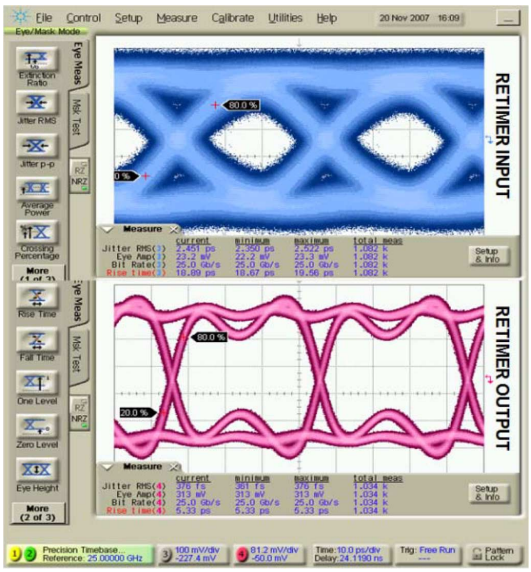

Fig. 15. Measured retimer input (top) and output (bottom) exhibiting less then 0.4 pS of rms jitter.

with 165-GHz f_T as shown in the chip micrograph reproduced in Fig. 14. The measured output eye diagram of the retimer breakout is reproduced in Fig. 15 where a 25 Gb/s input signal with 23 $\mathrm{mV_{pp}}$ amplitude is retimed by a 50 GHz clock. The rms jitter improves from 2.53 ps to 0.38 ps where the contributions from the test equipment have not been de-embedded. In light of this result, it is worth noting that the ADC performance benchmark used in Fig. 1 corresponds to an rms jitter of 0.1 ps instead of the 1 ps typically used to date. This modification was made in order to acknowledge the improvement in jitter of recent decision circuits to the sub-picosecond range.

A separate test chip containing the folded-cascode opamp was manufactured in the same technology as the ADC. The measured voltage transfer curve and DC gain is shown in Fig. 16

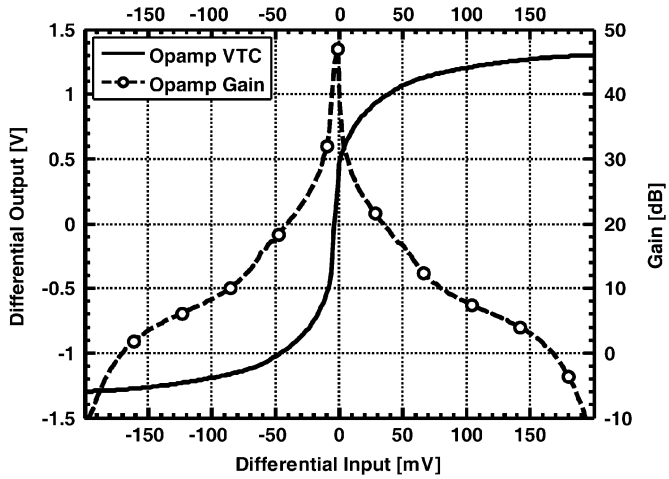

Fig. 16. Measured voltage-transfer curve for SiGe BiCMOS folded-cascode opamp.

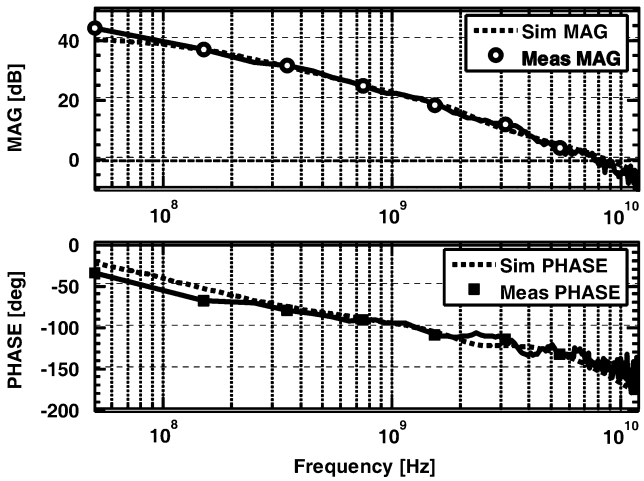

Fig. 17. Measured and simulated frequency response of the SiGe BiCMOS folded-cascode opamp.

where 42 dB of DC gain is achieved with a differential output swing of ± 1.35 V while operating from a 2.5 V supply. The measured frequency response is plotted in Fig. 17 alongside simulation results (note that measurements and simulations are single-ended). The unity gain bandwidth and phase margin are 9 GHz and 35° respectively. Assuming the differential magnitude response is 6 dB higher than the single-ended measurements, the unity gain bandwidth becomes 12 GHz. A compensation capacitor at node P_1 in Fig. 11 can be used to increase the phase margin of the amplifier at the expense of lower bandwidth.

The ADC was measured using the Agilent E8257D and E4422B signal sources to generate a 20–50 GHz clock and 0.1–1 GHz input respectively, and then directly connecting one end of the digital output to an Agilent E4448A power spectrum analyzer. This setup permits high-speed measurements directly on wafer and requires only one output pad. Nevertheless, gauging performance of the ADC with an analog spectrum analyzer driven by the digital output of the modulator, rather than by capturing the digital data and analyzing it digitally, leads to a number of inaccuracies which are inherent in the measurements. The effect of metastability will tend to be

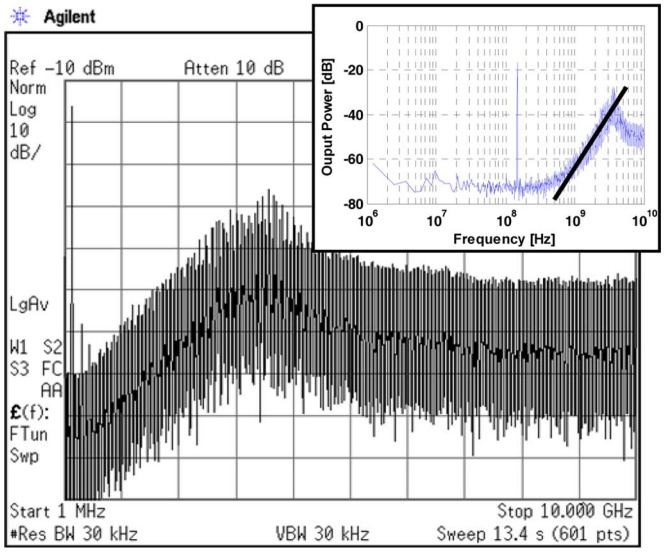

Fig. 18. Power spectral density from PSA (log-scale inset) of 3-latch ADC sampling at 40 GHz.

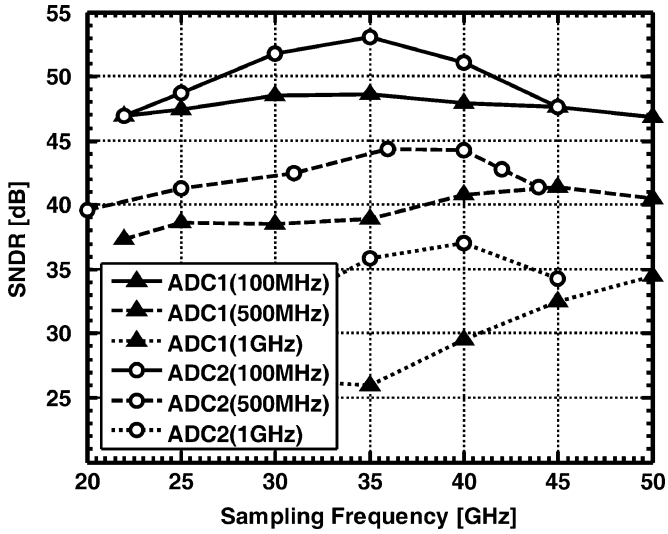

Fig. 19. Measured dynamic range versus sampling frequency.

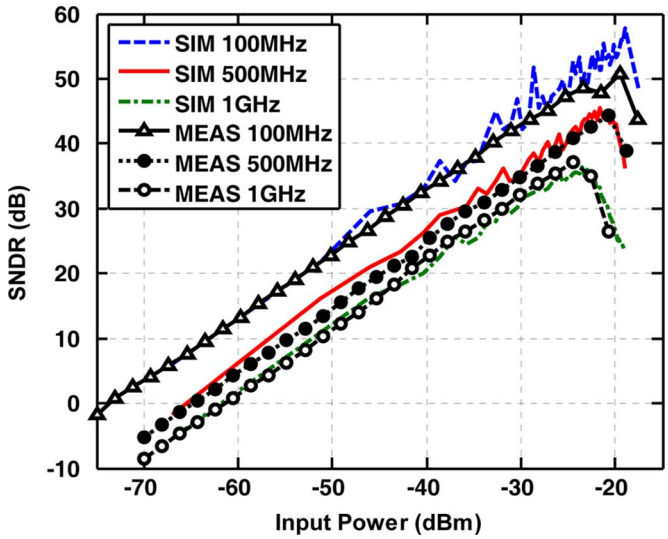

Fig. 20. Comparison between behavioral model simulations and measurements for dynamic range of ADC2.

subdued while any nonlinearity in the output buffer and test setup will degrade performance.

For any given passband (PB), the input frequency is at 1/3 PB so that the second and third harmonics are included in the integrated noise plus distortion measurement. The spectrum of ADC2 is shown in Fig. 18 for a 150 MHz input. The inset plots the spectrum on a log scale, confirming second-order noise shaping.

In general, both ADCs work from 20–50 GS/s by adjusting the DAC feedback currents to preserve stability and the desired NTF (DAC currents were within 10% of their design values). Fig. 21 compares the measured SNDR of both ADCs as a function of sampling rate for passbands of 100 MHz, 500 MHz, and 1 GHz. As the bandwidth increases, the peak SNDR occurs at higher sampling rates. For a passband of 1 GHz, increasing the sampling rate of ADC1 from 22 GHz to 50 GHz adds nearly 2 bits of resolution. These results emphasize the benefit of using mm-wave sampling rates for $\Delta\Sigma$ ADCs operating in the hundreds of megahertz passband range. While the ADC with three latches has higher peak performance over all bandwidths, the one with four latches is superior for sampling rates above 45 GHz. This suggests that peak performance of ADC1 is limited by loop delay while ADC2 is limited by metastability—as predicted by our system-level simulations.

The dynamic range of ADC2 is shown in Fig. 20; achieving a peak SNDR of 53.1 dB, 44.4 dB and 37.1 dB over a bandwidth of 100 MHz, 500 MHz and 1 GHz respectively. Included in Fig. 20 are simulation results of the behavioral model for the same range of input powers and bandwidths as the measured data. The excellent agreement suggests the model successfully captures the relevant non-idealities of the system. Moreover, the strong correlation between all levels of the design (behavioral model, transistor-level simulations, and measured data) demonstrates the utility of the top-down design methodology employed in this work towards the design of CT $\Delta\Sigma$Ms with mm-wave sampling clocks.

A summary of the measurement results is provided in Table I and a comparison of this work to the-state-of-the-art is demonstrated in Fig. 1. The comparison includes a survey of recently published CT $\Delta\Sigma$Ms (details found in Table II) in addition to ADCs of all other types. The figure of merit (using an input just below 1/3 BW) is defined as

$$\mathrm{FoM} = \frac{\mathrm{Power}}{2^{\mathrm{ENOB}} \cdot 2\,\mathrm{BW}} \tag{27}$$

and the ENOB as

$$\mathrm{ENOB} = \frac{\mathrm{SNDR} - 1.76}{6.02} \tag{28}$$

where this work represents the first $\Delta\Sigma$ modulator to achieve an ENOB of 6 bits at 1 GHz.

TABLE I
SUMMARY OF MEASURED ADC PERFORMANCE

Signal Bandwidth	100MHz	500MHz	1GHz
Sampling Rate	35GHz	37GHz	40 GHz
OSR	175	37	20
SNR	58.9 dB	45.9 dB	37.7 dB
SNDR	53.1 dB	44.4 dB	37.1 dB
ENOB	8.5 bits	7.1 bits	5.9 bits
SFDR	65 dB	63 dB	50 dB
Power	650 mW		
FoM	8.8 pJ/conv	4.48 pJ/conv	5.55 pJ/conv
Power†	350 mW		
FoM†	4.74 pJ/conv	2.58 pJ/conv	2.99 pJ/conv

† Assuming ADC is used inside a system with available clock.

TABLE II
SURVEY OF RECENTLY PUBLISHED LOW-PASS (LP) AND BANDPASS (BP) CONTINUOUS-TIME $\Delta\Sigma$ ADCS

Ref	Year	Type	Technology	Fs (GHz)	*fo* (GHz)	BW (MHz)	SNR (dB)	SNDR (dB)	Power (W)	FoM (pJ/conv)
[19]	2006	LP	200-GHz SiGe HBT	20	-	312.5	30.5	N/A	0.49	-
[34]	1994	LP	30-GHz GaAs HEMT	0.5	-	2.5	-	55	0.475	206.8
[35]	1996	LP	20-GHz Si BJT	1.28	-	10	-	45	0.5	61.6
[36]	1998	LP	31-GHz InGaAs HEMT	5	-	50	-	38	0.4	54.9
[16]	2001	LP	190-GHz InP	18	-	500	-	32	1.5	46.1
[10]	2003	LP	205-GHz InP	8	-	250	-	40	1.8	43.1
[11]	1995	LP	70-GHz InP	3.2	-	50	-	50	1	38.7
[7]	2003	LP	150-GHz InP	2.5	-	25	-	74	6	29.3
[8]	2004	LP	180nm-CMOS	0.16	-	10	-	56	0.122	11.8
[15]	2004	LP	180nm-CMOS	2	-	1.23	-	69	0.018	3.9
[7]	2003	BP	150-GHz InP	2.5	0.1	12.5	84.2	N/A	6	-
[37]	2007	BP	47-GHz SiGe BiCMOS	3.8	0.95	1	59	N/A	0.075	-
[38]	2004	BP	130-GHz InP	4	0.21	60	47.7	N/A	3.5	-
[39]	1997	BP	80-GHz InGaAs	4	0.055	62.6	44	N/A	1.4	-
[40]	1997	BP	40-GHz GaAs	4	1	60	47.4	N/A	3.2	-
[27]	1998	BP	50-GHz SiGe HBT	4	1	4	53	N/A	0.35	-
[41]	2006	BP	130-GHz InP	4	1.4	180	40.2	N/A	7.7	-
[42]	2003	BP	160-GHz InP	4.3	1.3	200	39	N/A	6.2	-
[21]	2007	BP	150-GHz SiGe BiCMOS	40	2	60	55	35.2	2.2	390
[20]	2008	BP	150-GHz SiGe BiCMOS	40	5	500	37.9	22.1	2.1	201.9

Note that many papers report SNR instead of SNDR (especially for BP implementations where a two-tone test is needed to properly measure the SNDR). In the event SNDR information is missing, the FoM is not computed and the entry is not included in Fig. 1.

V. CONCLUSION

A 20–50 GS/s continuous-time delta-sigma data converter intended for multi-gigabit mm-wave receiver applications has been demonstrated in a 130-nm production SiGe BiCMOS process. System-level simulations in Matlab and Simulink identified an important trade-off between metastabilty and loop delay; leading to the derivation and experimental verification of an analytical expression linking quantizer gain to modulator performance. Based on this analysis, the ADC effectively exploits the ever-higher f_T of modern transistor technologies to achieve a comparable FoM to flash and pipeline topologies while employing a very simple architecture. Although the work presented in this paper is exclusively realized in SiGe BiCMOS, the authors have implemented several of the key circuit blocks in 65-nm GP CMOS including the opamp [30] and retimer [31]. In light of these recent results, the prospect of an all-CMOS implementation not only seems feasible but will likely result in lower power consumption; making CT mm-wave $\Delta\Sigma$Ms in CMOS as well as SiGe BiCMOS an excellent candidate for current and future A/D applications.

ACKNOWLEDGMENT

The authors wish to thank B. Sautreuil and P. Chevalier for facilitating the technology access, S. Shahramian for help with measurements, T. Chalvatzis for providing invaluable design advice, and J. Pristupa and CMC for CAD tools. Equipment grants by NSERC, OIT and CFI, and VNA access from ECTI are also gratefully acknowledged.

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Adam Hart received the B.A.Sc. degree, with distinction, in honors electrical and computer engineering from McGill University, Montreal, QC, Canada, in 2006, and the M.A.Sc. degree in electrical engineering from the University of Toronto, Toronto, ON, Canada, in 2008. He is currently pursuing his degree in medicine (MDCM) at McGill University, Montreal, PQ, Canada.

His research interests are in the area of continuous-time delta sigma modulators and millimeter-wave IC building blocks.

Mr. Hart has received numerous scholarships, including the McConnell award for academic achievement, the undergraduate research award, and a post-graduate scholarship from the Natural Sciences and Engineering Council of Canada (NSERC).

Sorin P. Voinigescu received the M.Sc. degree in electronics from the Polytechnic Institute of Bucharest, Romania, in 1984, and the Ph.D. degree in electrical and computer engineering from the University of Toronto, Canada, in 1994.

From 1984 to 1991, he worked in R&D and academia in Bucharest, where he designed and lectured on microwave semiconductor devices and integrated circuits. Between 1994 and 2002 he was with Nortel Networks and Quake Technologies in Ottawa, Canada, where he was responsible for projects in high-frequency characterization and statistical scalable compact model development for Si, SiGe, and III-V devices. He later conducted research on wireless and optical fiber building blocks and transceivers in these technologies. In 2002 he joined the University of Toronto, where he is a full Professor. In 2008/2009 he spent a sabbatical year at Fujitsu Laboratories Inc. of America. He has authored or coauthored over 100 refereed and invited technical papers spanning the simulation, modeling, design, and fabrication of high frequency semiconductor devices and circuits. His research and teaching interests focus on nano-scale semiconductor devices and their application in integrated circuits at frequencies beyond 200 GHz.

Dr. Voinigescu received NORTEL's President Award for Innovation in 1996 and is a member of the TPCs of the IEEE CSICS and BCTM. He is a co-recipient of the Best Paper Award at the 2001 IEEE CICC and at the 2005 IEEE CSICS, and of the Beatrice Winner Award at the 2008 IEEE ISSCC. His students have won Student Paper Awards at the 2004 VLSI Circuits Symposium, the 2006 SiRF Meeting, RFIC Symposium and BCTM, and at the 2008 International Microwave Symposium.