DA and AD Converters for 25 GS/s and Above

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***Abstract* — This paper reports on the status of the design and expected performance of high speed AD and DA converters in SiGe bipolar technology for future 100 Gbit/s Ethernet systems.**

***Index Terms* — ADC, DAC, SiGe, Bipolar, Optical communications**

I. Introduction

NEXT generation optical data transmission systems will operate at 100 Gbit/s, using the Ethernet standard and efficient data transmission schemes (e.g. PM-QPSK or OFDM). Key components of such systems are analog-digital and digital-analog converters (ADC/DAC), with very high sampling rate (up to 60 GS/s) and a high resolution (effective number of bits – ENOB) up to 6 bit [1].

Up-to-date Silicon-Germanium (SiGe) bipolar technologies are well-suited to reach this goal. Their high speed capability (f_T, f_{max}) in combination with the immanent high transistor gain (g_m) and driving capability allows for high circuit speed [2] resulting in lower number of parallel paths needed to reach such high effective sampling rates. The paper presents some particular design considerations on ADC/DAC design in SiGe bipolar technology for very high sampling rates, as well as measurement results of prototypes, and gives some outlook on future developments.

II. Design Concept

Specifications of the electronic components required for the different data transmission schemes are still to be defined. In order to maintain a high degree of flexibility to accommodate change requests on functionality and performance, which e.g. arise from experimental results, alternative concepts or improved components, a cell based design concept was developed [2][3]. The cells are realized in high-speed SiGe bipolar technology and can be operated from dc up to data rates above 100 Gbit/s.

For all cells, versions with different speed levels are designed. Cells with the highest speed level are optimized for maximum speed only, while lower speed levels trade off speed for low power consumption and small chip area. Furthermore, these low-speed cells can be realized in a Structured ASIC approach that allows for fast realization and adoption of various rather complex types of interface logic between the converters and FPGAs or other signal processing circuits [2].

III. Circuit Design of ADC and DAC

The general structure of the DAC prototype design with 6 bit resolution is shown in Fig. 1. The 24 data input channels with up to 7.5 Gbit/s each (6.25 Gbits/s for 25 GS/s) are used as the interface to the FPGA. Four data channels each are multiplexed up to the desired data rate of 25 to 30 Gbit/s. For the generation of the analog output signal, weighted currents are summarized [4] using a common base stage as impedance transformation circuit in order to increase the output bandwidth.

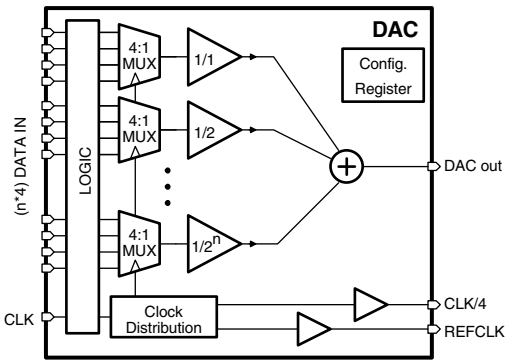

Fig. 1: Block diagram of the DAC prototype IC.

Due to the potential high skew between the FPGA data channels (up to 3.5 UI produced by FPGA), synchronization circuits with 120 gates in each channel have to be included. These can select the sampling clock phase in 90 deg steps and check for correct data channel alignment. Within the high speed part of the circuit, the clock distribution block is very timing critical. By the use of accurate retiming in the DAC core it is ensured that the 6 output currents are switched synchronous within a ±0.5 ps timeframe.

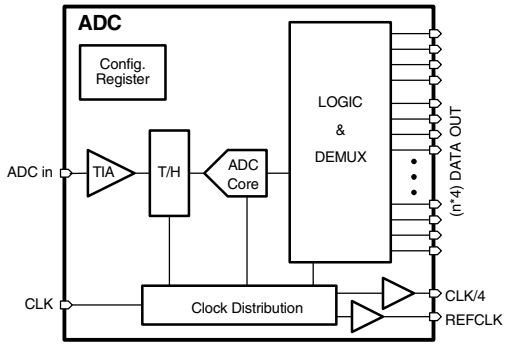

Fig. 2: Block diagram of the ADC under development.

The framework of the ADC, which is nearly complementary to the DAC, is shown in Fig. 2. For the ADC core two different approaches are under development. Thanks to the cell based design, they fit into the same IC framework, i.e. the only difference seen from outside will be in calibration and configuration routines.

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As a reasonable trade-off between high speed of a pure flash concept and low power, a combined pipeline-flash concept, which samples the signal by two succeeding stages with 3 bit each, appears to be promising. A fast DAC converts the first ADC binary output into a voltage to be subtracted from the input signal. After signal amplification, the residual signal is sampled in a similar way.

A second approach under investigation is the so-called folding concept [5], which directly generates a Gray-coded signal at the output. This reduces the complexity of the chip drastically, because no additional logic for the binary coding is needed. Furthermore, a higher resolution can be obtained easily by adding further folding stages, but for the cost of a reduced conversion rate. Due to significant influence of process variations, this concept needs to facilitate circuitry for extensive calibration.

In both concepts under investigation, the desired sampling rate cannot be reached with one single channel. Therefore, a concept with 4 (pipeline) or 8 (folding) interleaved ADC cores is used. Due to this measure, skew in the clock distribution network becomes critical and needs to be compensated for by calibration routines.

A very important circuit block for the performance of the whole ADC is the track and hold circuit (T&H) which is used at the analog inputs in both circuit concepts. Data settling time, level accuracy and drift during the hold phase are critical design data.

In order to allow the FPGA for receiving multi-channel data, the ADC also includes circuitry for generating and sending alignment patterns.

IV. Measurement Results

For concept and performance evaluation, prototype ICs have been fabricated using Infineon B7HF200 SiGe bipolar technology.

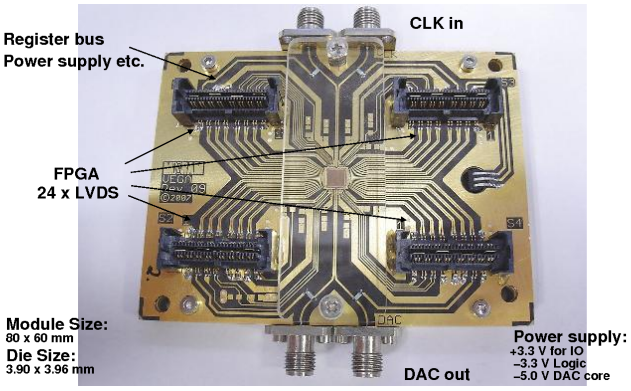

Fig. 3: Photograph of the realized DAC prototype module.

Fig. 3 shows a photograph of the DAC IC, mounted in a RF module. The chip can be driven by FPGA, but can also be used in a self-test mode, where a repeating sequence of up to 4 output voltage levels can be programmed. In Fig. 4, some examples for the output signal performance for different level steps are shown. The conversion rate is changeable from DC to 25 GS/s. The output signal amplitude is 800 mV_{pp} at 50 Ω load.

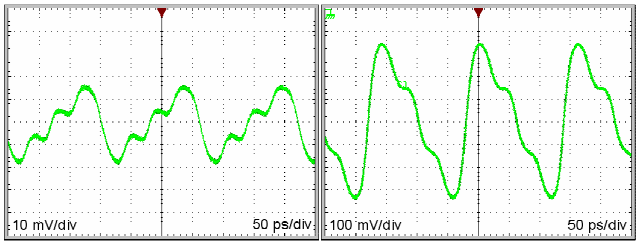

Fig. 4: DAC prototype in test mode at 25 GS/s programmed for 4 step ramp function. Left: LSB steps (12.5 mV), right: maximum output amplitude.

As an example for the ADC, the evaluation IC allows to characterize the most critical T&H circuit. In Fig. 5 (left), the output signal of the 20 GS/s T&H stage is shown for a 40 Gbit/s PRBS pattern at the data input. Fig. 5 (right) shows the output signals of a 20 GS/s T&H, followed by a 5 GS/s T&H, at 1 GHz input test signal. Track and hold periods can be clearly observed, however, also some input voltage dependent droop during the hold phase can be seen. The improvement of this T&H performance is one focus of the current developments.

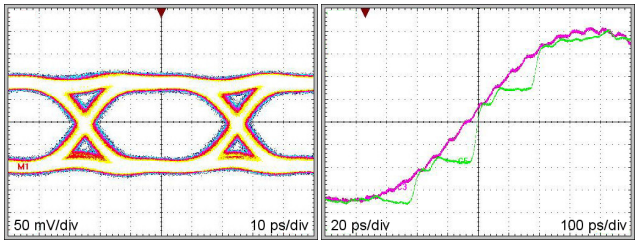

Fig. 5: Output signals of the T&H evaluation circuit for 20 GS/s sampling rate. Left: output eye pattern for 40 Gbit/s PRBS at the data input, right: output for 1 GHz sinusoidal input signal, sampled with a first 20 GS/s stage and a subsequent with 5 GS/s stage.

V. Summary

Based on the results from circuit simulations, proven by measurements on evaluation ICs, SiGe bipolar technology is well suited for realization of ADC/DAC ICs with very high sampling rates. From the results obtained so far, the next generation target with sampling rates about 60 GS/s and 5 bit resolution appears to be feasible.

References

[1] Peter J. Winzer and Greg Raybon, "100G Ethernet – A Review of Serial Transport Options", *IEEE LEOS Summer Topicals*, Portland 2007.

[2] M. Moller, "Efficient design of high-speed ICs beyond 100 Gb/s with special regard to SiGe-bipolar technology", SCD 2008, *Semiconductor Conference Dresden*, 2008.

[3] M. Moller, "Challenges in Cell-Based Design of Very-High-Speed Si-Bipolar IC's at 100 Gb/s", *IEEE Bipolar/BiCMOS circuits and technology meeting*, Boston 2007.

[4] D. McGhan et al., "5120-km RZ-DPSK Transmission Over G.652 Fiber at 10 Gb/s Without Optical Dispersion Compensation", *IEEE Photonics Technology Letters*, Vol. 18, No. 2, pp. 400-402, Jan. 2006.

[5] C. Moreland et al., "A 14-bit 100-Msample/s Subranging ADC", *IEEE Journal of Solid State Circuits*, Vol. 35, No. 2 pp. 1791-1798, Dec. 2000.