A 1 GS/s 6 Bit 6.7 mW Successive Approximation ADC Using Asynchronous Processing

Jing Yang, *Member, IEEE*, Thura Lin Naing, *Member, IEEE*, and Robert W. Brodersen, *Fellow, IEEE*

***Abstract*—An asynchronous 6 bit 1 GS/s ADC is achieved by time interleaving two ADCs based on the binary successive approximation (SA) algorithm using a series capacitive ladder. The semi-closed loop asynchronous technique eliminates the high internal clocks and significantly speeds up the SA algorithm. A key feature to reduce the power in this design involves relaxing the comparator requirements using an error correction technique, which can be viewed as an extension of the SA algorithm to remove degradation due to metastability. Fabricated in 65 nm CMOS with an active area of 0.11 mm^2, it achieves a peak SNDR of 31.5 dB at 1 GS/s sampling rate and has a total power consumption of 6.7 mW.**

***Index Terms*—Analog-to-digital conversion, asynchronous logic circuits, binary successive approximation algorithm, cognitive radios, metastability, semi-closed loop, series capacitor array, time-interleaving.**

I. Introduction

IT IS possible to use high-speed ($\sim$ GHz) medium-resolution low-power analog-to-digital converters (ADCs) to resolve the high dynamic range problems in highly flexible, very wideband radio front-ends such as required in cognitive and software defined radios [1]. These architectures use multiple ADCs as pipeline stages with significant digital processing to cancel strong interference [2]. Using these techniques, a dynamic range on the order of 70 dB can be achieved with multiple ADCs that have a moderate resolution of about 5 to 6 bits. Also as wireless data rates increase into the multiple Gbit/sec range in the millimeter wave regime (e.g., 60 GHz), ADCs with bandwidths of GHz and higher are required [3]–[5], which again only need moderate resolutions since the interference problem is not an issue at those frequencies [6]. These applications typically have severe power and cost constraints when achieved using a standard CMOS processes.

This work presents strategies and techniques to optimize the power and area efficiency of such an ADC using a power efficient semi-closed loop [7], successive approximation algorithm executed with asynchronous processing. A 65 nm low-leakage low-power (LP) CMOS process is used with particular attention paid to increase the conversion speed of the asynchronous feedback loop, which is complicated by the severely limited overdrive voltages due to the 1.2 V voltage supply and the high threshold of the transistors. Metastability issues are carefully addressed and an error correction algorithm is developed which can remove any potential degradation. This algorithm, however, requires constraints in the design which are carefully discussed. In particular, the critical loop is composed of intervals which have variable delay (the comparator decision) and other portions which are kept constant (e.g., DAC settling).

The prototype design has a sample rate of 1 GS/s ADC which achieves an ENOB of 5.0 at 1 GS/s with a power consumption of analog and digital processing of 6.7 mW. To achieve the rate at low power, two ADCs were interleaved, with each ADC only occupying an area of 0.35×0.16 mm^2 for a total area of 0.11 mm^2.

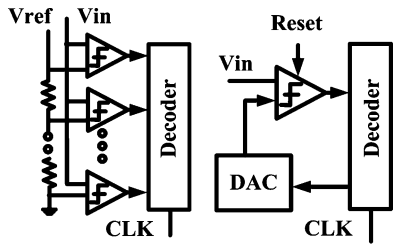

Fig. 1. High-speed ADC architecture. Left: Flash ADC; Right: SAR ADC.

II. ADC Architecture

A conventional flash ADC [Fig. 1(a)] might seem to be the preferred choice for the above specifications, considering its low latency and high-conversion speed since each conversion is completed in a single clock cycle [4], [8]–[10]. However, flash ADCs suffer from an exponential dependence of power and area on resolution and often require relatively difficult calibration for the many parallel signal paths [11]. The calibration becomes even more difficult as the process variation increases with technology scaling. In comparison, a successive approximation register (SAR) ADC only requires a single signal path, with one comparator, spreads one conversion over several cycles, and charges or discharges an internal DAC based on the decision made through the previous comparison [Fig. 1(b)] [12]. There is only a single comparator and DAC. Also, because the SAR resolves one bit, instead of one level per comparison, it is possible for the SAR to be implemented in a small area at low power. This characteristic also renders the architecture highly scalable and easier to calibrate.

In SAR implementations, as shown in Fig. 1(b), a reset signal at the comparator is required. It is timed so that a reliable

Manuscript received December 01, 2009; revised February 21, 2010; accepted March 25, 2010. Current version published July 23, 2010. This paper was approved by Guest Editor Anthony Chan Carusone. This work was supported by Center for Circuit and System Solutions (C2S2) Focus Center, one of five research centers funded under the Focus Center Research Program, a Semiconductor Research Corporation program and by industrial members of the Berkeley Wireless Research Center, and also by the National Science Foundation Infrastructure Grant 0403427. STMicroelectronics donated the chip fabrication.

The authors are with the Berkeley Wireless Research Center, University of California, Berkeley, CA 94704 USA (e-mail: yangjing@eecs.berkeley.edu).

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Digital Object Identifier 10.1109/JSSC.2010.2048139

comparison is performed in every comparison cycle. The SA algorithm evaluates the comparator output, generates the corresponding decision and the DAC settles with respect to that decision. In traditional designs, the reset phase terminates after the DAC is fully settled to ensure the comparator evaluation is performed on the correct input voltage [13].

A. Asynchronous Processing

The sequential operation of the SA algorithm has traditionally been a limitation on the high-speed applications, because a synchronous approach relies on a clock to divide the conversion phase into equally timed slots as the conversion proceeds from MSB to LSB [14]–[18]. This internal clock for N bit ADC would therefore operate at a frequency of at least $N\times$ the sampling clock, and if only the switching power is considered, would require at least $N\times$ the clock power of an asynchronous approach in which the sampling frequency sets the highest clock rate. It is estimated that in this design, if it were synchronous, the percentage of the total power for the clocks would rise from 15%, to above 50%.

The high-speed internal clock period in a synchronous design is chosen to accommodate the worst case scenario, including the comparator resolving time for a small residue voltage (usually below 1 $V_{\rm LSB}$, where $V_{\rm LSB}$ for an N bit ADC is $V_{\rm LSB} = \Delta = V_{\rm FS}/2^N$), the digital delay through the SA algorithm, and the maximum DAC settling time, even though the longest bit cycle seldom falls into this case.

Besides the problem of the high-speed internal clock, metastability is a fundamental issue associated with all the ADCs that rely on comparators for conversion. When in a metastable state, the comparator spends an unbounded time on resolving an arbitrarily small input. An error will then be created when the comparator input is below a certain minimum level depending on the design, resulting in a degradation of the effective number of bits (ENOB). Interestingly enough, as will be shown, the use of asynchronous processing with metastability detection allows for a simple SA algorithm extension which can essentially eliminate the errors arising from metastability. This approach allows a design in which the requirement for the comparator speed is reduced by allowing operation in a metastable state once each conversion, thus reducing its power consumption.

It is important to note that the analog input is synchronously sampled at a time interval of $t_{\rm samp}$, with only the subsequent conversion processing being asynchronous [Fig. 2(b)]. The execution of the SA algorithm precedes from MSB to LSB sequentially (and asynchronously) under control of locally generated *rdy* signals [13].

The asynchronous processing also makes the average total conversion time significantly shorter than using synchronous processing. The SA asynchronous conversion efficiently utilizes the faster comparison cycles for large comparator inputs, since only one of the residual voltages will fall within $1/2\,V_{\rm LSB}$ by nature. The amount of conversion time savings between asynchronous and synchronous processing, as previous research [13] has shown, is a function of the number of bits, the profile of input-dependent residual voltages and the allowed ENOB degradation.

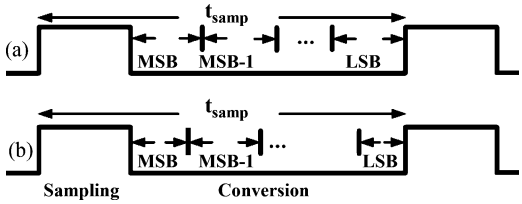

Fig. 2. (a) Synchronous processing with equally divided bit comparison time. (b) Synchronous sampling, asynchronous processing conversion with *unequal* time interval.

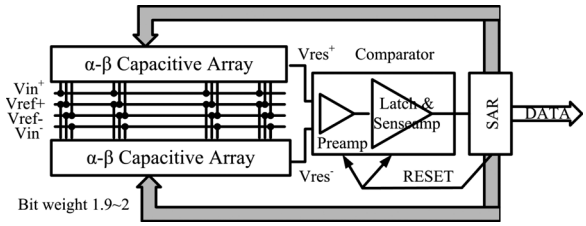

Fig. 3. Basic ADC architecture.

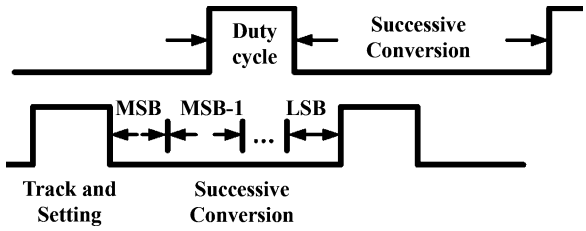

Fig. 4. Internal opposite phase clocks. Each clock has a tracking and settling phase followed by the successive approximation (SA) comparisons.

B. Architecture

Fig. 3 shows the circuit architecture with the key blocks of capacitor network, comparator, SA control and the basic processing loop [13]. The external square-wave clocks initiate a tracking and settling phase followed by the SA comparisons (Fig. 4). The analog input is sampled by the capacitor array with low input capacitance provided by the series non-binary C-2C capacitive ladder network [13]. The total input capacitance of the ladder is independent of the number of ADC bits due to the series connection. The input capacitance is significantly reduced compared to the conventional approaches of geometrically scaled or unitary capacitor arrays and enables an extremely high input bandwidth. The disadvantage of the series capacitor array is that the actual ratio of the capacitor network highly depends on the capacitance ratios and the parasitic capacitors associated with the interconnect circuitry, thus requires extra effort on the layout and calibration.

After tracking and settling phase of the input signal, the asynchronous SA proceeds from MSB to LSB, utilizing only one comparator. The single comparator design avoids the offset calibration between multiple comparators required in traditional flash ADCs. The offset from the comparator therefore becomes a global offset and this DC offset can be digitally removed. A completion or ready (*rdy*) signal is generated after completing the comparison. The corresponding rising edge of *rdy* triggers the dynamic asynchronous SA logic. As shown in Fig. 5, two major operations are involved to execute the algorithm initiated

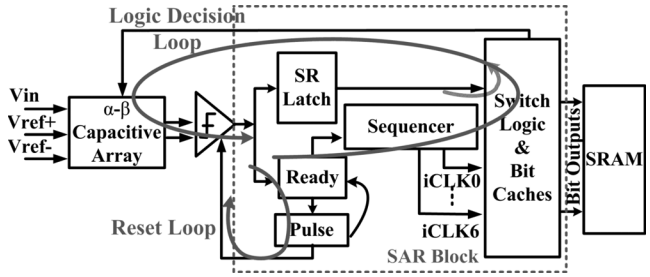

Fig. 5. Single-ended ADC architecture—details of SA blocks and data paths.

by the rising edge of the *rdy* signal: 1) a pulse is generated which controls the duration of the reset phase, so that the comparator could reset itself after each evaluation; 2) a set of sequencer signals are driven, each with monotonic switching, to provide multiple-phase clocks for the switch logic and bit caches to store the correct corresponding bit comparison results. The charge redistribution network, which is formed by the capacitor array, functions as a digital to analog converter (DAC) to subtract or add a fraction of the reference voltage, with the voltage increment of the DAC being controlled by the switch logic.

The duration of the *rdy* signal is set such that the capacitor array is settled reliably and a full reset of the comparator is finished, thus the evaluation could start again. Dynamic logic is used with the transistors sized optimally using logical effort [19] for dynamic gates to enhance the asynchronous processing speed.

In order to meet the speed specification of 1 GS/s, two parallel converters have been time interleaved, since this approach is especially attractive when a single ADC area is small, as in this design. Interleaving two ADCs using non-overlapping clocks achieves twice the sampling rate at twice the power and area with a slight additional penalty of power and area for the parallel paths synchronization and calibration.

III. Extension of the SA Algorithm to Include Metastability

A well-known issue related to SAR ADCs and flash ADCs is the metastability phenomenon. It is due to the occasional inability of a comparator to resolve a small differential input into a valid output logic level [20], [21]. This subtle characteristic of comparators can cause large errors (sparkle codes) in ADCs if not dealt with effectively. The probability of errors due to metastability increases exponentially with sampling frequency [21].

The residual voltage at bit i, V_{res_i}, is defined as the sampled input minus the summation of all the voltage steps up to that bit:

$$V_{\mathrm{res}_i} = V_{\mathrm{in}} - \sum_{k=1}^{i-1} V_{\mathrm{step}_k} \tag{1}$$

The resolving time of the comparator strongly depends on V_{res_i} as will be shown in Section IV. Unfortunately, over-designing the comparator to reduce the range of the metastable state results in increased power consumption and larger area.

The conversion time of the N bit ADC has the constraint, such that N comparisons, $(N-1)$ SA algorithm decisions, DAC settling, and finally sampling of the input, should be accomplished in one clock cycle. If the digital delay through the SA algorithm logic, t_{digital}, and the settling time for the DAC, t_{DAC}, is fixed, the constraint becomes

$$t_{\mathrm{samp}} \geq (N-1)[t_{\mathrm{DAC}} + t_{\mathrm{digital}}] + \sum_{i=1}^{N} t_{\mathrm{comp}_i} + T_{\mathrm{sw}} \tag{2}$$

where t_{samp} is the total clock period, t_{comp_i} is the resolving time spent on the comparison at bit i, and T_{sw} is the sampling pulse width.

The nature of the SA algorithm requires that there is going to be *one*, and only *one*, bit conversion for which $V_{\mathrm{res}} \leq V_{\mathrm{LSB}}/2$. Therefore, if the evaluation for each bit is reliable, only one conversion will be in the metastable state. Defining the threshold comparison time, $t_{\mathrm{comp}}(V_{\mathrm{comp\_th}})$, as the maximum delay through the comparator to ensure a full N bit output when a minimum input residue voltage is at $V_{\mathrm{comp\_th}}$. Then, if $V_{\mathrm{comp\_th}} \leq V_{\mathrm{LSB}}/2$, when $V_{\mathrm{res}} > V_{\mathrm{LSB}}/2$, no metastability will occur. However, when $V_{\mathrm{res}} \leq V_{\mathrm{LSB}}/2$, an extended evaluation time will be required for the comparator. It is possible that if the comparator input is below $V_{\mathrm{comp\_th}}$, the comparison time could be extended so much that not all bits can be determined. As opposed to a flash ADC or a synchronous SAR, that would generate an error, an asynchronous SAR simply produces an output that has less than N bits. By designing the comparator to have a maximum delay of $t_{\mathrm{comp}}(V_{\mathrm{LSB}}/2)$ for the slow corner, it is true across all process corners that an output of less than N bits can be inferred to mean the V_{res} for one of the evaluations was less than $V_{\mathrm{LSB}}/2$. Based on this knowledge, a simple extension to the SA algorithm can be made that can yield correct conversion code values, even if the comparator enters metastability (i.e., when the output has less than N bits).

If the metastable state is sufficiently long that there are no additional output bits after the metastable state is entered, then the SA algorithm extension can be implemented without any additional on-chip circuitry. This off-line correction starts by detecting that only M bits of data are output from the asynchronous loop (with $M < N$), so that we know the input to the comparator must be less than $V_{\mathrm{LSB}}/2$ from the voltage level defined by $\sum_{i=1}^{k} V_{\mathrm{step}_i}$ $(k = 1, 2 \ldots M)$. We can therefore determine the correct voltage level (within $V_{\mathrm{LSB}}/2$) since we assume that it is the last bit evaluation which took an extended time. A simple off-line algorithm is to just fill in the missing end bits with the complement of the last outputted bit. This algorithm was used in all the results presented.

For instance, in a binary 6-bit ADC with $V_{\mathrm{FS}} = 1$ V if $V_{\mathrm{in}} = 0.5\ \mathrm{V} - V_{\mathrm{LSB}}/16$, then $V_{\mathrm{res}} = V_{\mathrm{LSB}}/16$ and the comparison of the first bit will be extended, since $V_{\mathrm{LSB}}/16 \ll V_{\mathrm{LSB}}/2$. If it is assumed that only one bit is evaluated, the output of the ADC is a single "0". After the algorithmic extension described here, the code becomes the correct value 011111.

There is, however, an improvement on this algorithm that requires additional on-chip circuitry, which covers the case where one bit comparison takes a long time due to a small V_{res}, but leaves sufficient time for subsequent bit(s) evaluations. This means the assumption that the last bit output was the one within $V_{\mathrm{LSB}}/2$ was not true. The actual metastable bit can be detected

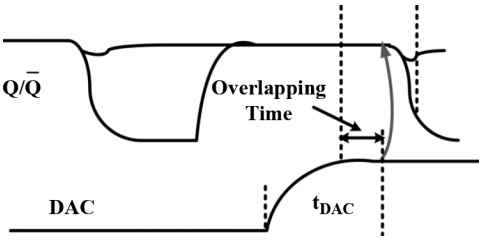

Fig. 6. Time overlapping between the comparator and the DAC.

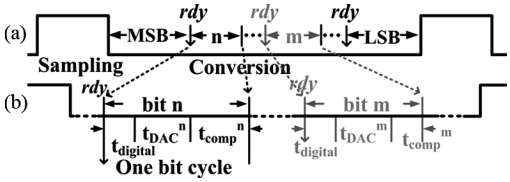

Fig. 7. (a) *rdy* signals. (b) critical delay components in different conversion bit cycles.

by creating a delayed version of the *Eq* falling edge signal. The delay $t_{\rm d\_comp}$ is slighter longer than $t_{\rm comp}(V_{\rm LSB}/2)$ When metastability (or more precisely when a long comparison time) occurs, both outputs of the comparator drop towards GND. An XOR output remains "0" unless the comparator outputs split. The delayed falling edge signal is used as an input control signal to a falling edge triggered register which latches the XOR output. The register's output, $\rm DM\langle \it i\rangle$, is precharged to 1 and will be discharged to 0 if bit i is in metastable state. $\rm DM\langle \it i\rangle$ $(i = 0, 1, \ldots 5)$ is further converted to a corresponding MUX output of 1 to 6. The *rdy* edge counter (REC) counts the actual evaluated number of bits. In a 6-bit ADC, the error correction flag (EC_flag) could be generated by comparing REC and the MUX output. When the comparator managed to resolve at least another bit after a metastable state incurred, MUX output $<$ REC, EC_flag is 0, thus the missing bits are filled the same as the last evaluated bit from the ADC. If MUX output $=$ REC, EC_flag is 1, the comparator barely finished a metastable bit, thus the missing bits should be the complement of the last evaluated bit. If MUX output $>$ REC, EC_flag is 2, the comparator is still converting the bit in metastability, an arbitrary filling of $011\ldots1$ or $100\ldots0$ is added as the missing codes.

Following our example above, instead of the last bit output being in metastability, we will assume a case in which the comparator is sufficiently fast that two more bits are evaluated after an initial long comparison time. The resulting output is then "011", REC $=$ 3, MUX output $=$ 1, and EC_flag $=$ 0. The code after the correction is then again the correct value of 011111. Although this example is only for the MSB being in a metastable state, the algorithm works for all cases where metastability could happen at any arbitrary bit. Therefore, metastability need not degrade the Effective Number of Bits (ENOB) when the comparator is designed to just meet the minimal timing requirement for $V_{\rm comp\_th} = V_{\rm LSB}/2$.

IV. Circuit Implementation

This section describes the design issues involved in each component of the critical delay path, including $t_{\rm digital}$, $t_{\rm DAC}$ and $t_{\rm comp}$. Moreover, to further enhance ADC speed, possible overlaps between $t_{\rm comp}$ and $t_{\rm digital}$, also $t_{\rm DAC}$ and $t_{\rm comp}$ (Fig. 6) have been exploited.

A. Critical Path and Reset Loop

After each comparison, based on the buffered comparator output and the multiple-phase clocks, the switch logic determines the DAC capacitors to be switched which are then connected to either the positive or negative reference voltage. The DAC capacitor is allowed to resettle and the next comparison starts.

There are two signal loops in the processing, the *logic decision* loop and the *reset* loop, as shown in Fig. 5. The logic decision loop executes the SA algorithm and the reset loop resets the comparator, the *rdy* signal, and other logic circuits, before the next bit cycle. Compared to the previous work [13], the reset loop in this design is semi-closed, in which a *rdy* triggered pulse, is used to reset both the comparator and the *rdy* signal itself. This semi-closed loop circuit facilitates a much earlier data reset, and gives extra time for the comparator to setup before making a reliable decision which increases the overall speed of the conversion. Also, using two different reset signals, *rdy* and *Eq*, in the two stages of the comparator, enhances the comparison speed by allowing the pre-amplifier to increase the voltage difference at the input of the dynamic latch, that will be further discussed in Section IV-B.

Starting each bit cycle with the *rdy* signal, the critical delay is composed of the digital delay through the SA algorithm, $t_{\rm digital}$, the DAC settling time, $t_{\rm DAC}$, and the resolving time spent on the comparison, $t_{\rm comp}$ (Fig. 7). While $t_{\rm digital}$ and $t_{\rm DAC}$ are designed to be relatively constant over each bit cycle, the comparison time is highly variable, since the comparator resolving time strongly depends on its differential input voltage level. To remove any memory effect between bit cycles, the comparator and *rdy* signal are reset, erasing the last comparison by pre-charging the differential outputs Q and $\bar{Q}$ to the same voltage and discharging the *rdy* signal to a logical level "0".

The comparator switches between two modes, reset mode and compare mode. As soon as the comparison is completed and the differential data has been reliably latched, the comparator turns into reset mode. The reset of the comparator is performed simultaneously with the decision logic and the DAC. An adequate DAC settling time is allowed to achieve a reliable comparison signal at the end of the reset phase, and the comparator switches back into the compare mode.

Timing to pull down the *rdy* is designed to insure there is enough time for a stable DAC output. In addition, a key function of the *rdy* signal is to hold the pre-amplifier in the reset phase. The reset switch *M6* (Fig. 8) that equalizes the pre-amplifier's outputs is designed such that the reset time of the pre-amplifier is shorter than the time required for subsequent charge redistribution.

B. Comparator Design

The comparator is composed of two-stages, a pre-amplifier followed by a dynamic regenerative latch [22] as shown in Fig. 8. The pre-amplifier gain is set to be 6 dB based on a Monte

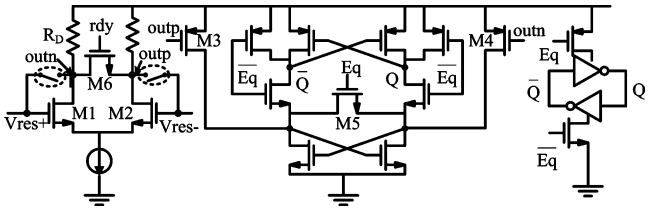

Fig. 8. Dynamic comparator circuit schematic. Pre-amplifier (left), dynamic latch (middle), and dynamic sense-amplifier (right).

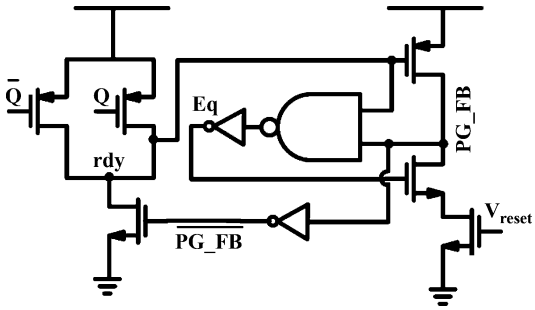

Fig. 9. Dynamic *rdy* acknowledge signal generator (left) and pulse generator *Eq* schematics (right).

Carlo simulation over process, so that the pre-amplifier can accommodate a 3σ gain error while allowing the comparator to respond to a minimum differential input of $V_{\rm LSB}$, with $V_{\rm FS}$ the full scale voltage of 1 Volt. The pre-amplifier is automatically biased during the sampling phase by connecting a pair of switches (Fig. 8), which are controlled by a delayed sampling clock, at the input and output of the pre-amplifier. To keep all devices in saturation, a cascode current source is avoided, due to the limited headroom available with the low supply voltage of 1.2 V. A simple current source is implemented to minimize the $V_{\rm ds}$ drop on the tail current source. $V_{\rm dsat}$ of the differential pair is designed to be slightly less than 100 mV to allow a minimum common mode voltage of 450 mV, as well as maintain a reasonable $g_{\rm m}/I_d$ ratio to improve the pre-amplifier's efficiency.

The necessary wide input bandwidth for the pre-amplifier could be achieved using poly-resistors to provide sufficient gain without the voltage drop of small W/L PMOS loads that is required to achieve the same gain. During auto biasing, a voltage drop of $I \times R_D$ is required from the supply, which is substantially less than $V_{\rm th} + V_{\rm dsat}$ of the PMOSs. Multi-finger poly-resistors provide good matching between *outp* and *outn*, and are therefore used for R_D's. This design yields a pre-amplifier with a gain-bandwidth product (GBP) of around 40 GHz.

M3 and *M4* in Fig. 8 are used to separate the pre-amplifier and the regenerative latch, so the charge from the data logic levels injected back to the input capacitor array is minimized [23]. The charge difference built up on the output of the pre-amplifier's results in imbalanced charge between the equalizing transistor (*M5*) source and drain. After each reset phase, when the *Eq* signal is pulled down, the charge will set one of the Q or $\bar{Q}$ to a logical level low.

Based on the regenerative latch resolving time[24], the comparator resolving time is found to be

$$t_{\rm comp} = \frac{1}{(\text{Gain} \cdot \text{BW})} \cdot \ln \frac{V_{\rm FS}}{\text{Gain}_{\rm preamp} \cdot V_{\rm res}} \qquad (3)$$

where $V_{\rm res}$ is the input voltage at the comparator and $\text{Gain} \cdot \text{BW}$ is the regenerative latch gain bandwidth product. Note that as $V_{\rm res}$ decreases, the comparison takes longer. As discussed in Section III, the speed requirement of the comparator could be reduced to a minimum of $t_{\rm comp}(V_{\rm LSB}/2)$. To achieve the 1 GS/s sample rate, the specification for the comparator would require a resolving time of approximately 60 ps with an input voltage of $V_{\rm LSB}/2$, accounting for more than 20% of the bit cycle. Compared to previous approaches [13], [25], which avoid metastability by increasing the comparator speed, this relaxes the comparator requirements which allows for a lower power design.

The dynamic sense-amplifier is added to boost the comparator gain during the dynamic transitions (Fig. 8). It significantly reduces the resolving time when sensing small inputs, which are the bottle-necks of most of the previous comparator designs. The dynamic sense-amplifier switches between standby and operating modes, resulting in minimum static power consumption.

C. Semi-Closed Loop Digital Circuits

To design the semi-closed loop digital circuits, first, we observe that both Q and $\bar{Q}$ are fully charged to $V_{\rm DD}$ at the end of each reset phase, thus, a voltage drop in either or both of them would indicate the start of a comparison. The *rdy* signal could therefore be generated ahead of the actual data completion time when the reliable data becomes available, and an approach for this is implemented as in Fig. 9. Detecting the start of the comparison shortens the overall delay of the critical path by allowing $t_{\rm comp}$ and $t_{\rm digital}$ to overlap, thus allowing an increased speed without the power penalty. Second, as the comparator switches into the compare mode, both Q and $\bar{Q}$ are pulled down together by the regenerative latch to a level much lower than the supply voltage before one of them is charged back to $V_{\rm DD}$ and the other is discharged to *GND* as shown in Fig. 10. Therefore, both PMOS transistors in the *rdy* acknowledge signal generator are on during the pull-down transition, resulting in a significantly reduced delay from the complementary data to the *rdy* signal.

The *rdy* signal triggers a pulse generator to create the reset phase. During the reset phase, the SA decision and the charge redistribution on the capacitor array is performed. If the settling error for the DAC is less than $V_{\rm LSB}$, the decision for the next comparison is reliable since further settling will not affect the result.

The circuit for generating the reset signal *Eq* is shown in Fig. 9. The rising edge of the *Eq* signal flags the beginning of the reset phase and the pulse duration is adjusted through a biased MOS transistor. The voltage, $V_{\rm reset}$, controls the duration of the reset phase by changing the delay from the equalizing clock (*Eq*) to the feedback node (*PG_FB*). Though $V_{\rm reset}$ is an externally fixed voltage in this implementation for testing purpose, it could also be set automatically using a 2–3 bit multiplying digital to analog converter controlled by a settling error sensing circuitry

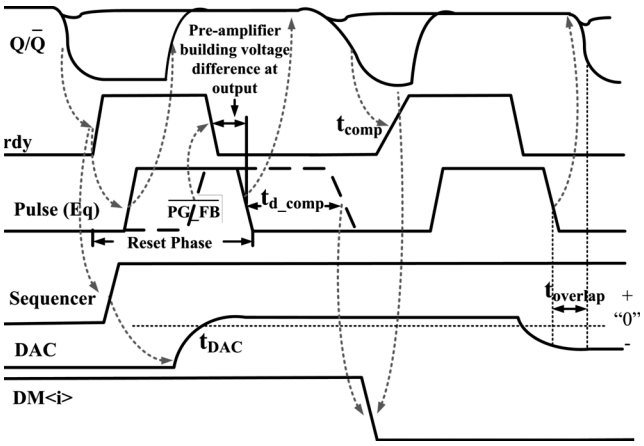

Fig. 10. Semi-closed loop timing diagram with extended reset phase—waveform illustration of dynamic *rdy* acknowledge signal generator, pulse generator, and metastability detection data generator $\mathrm{DM}\langle i\rangle$.

at the DAC's output, increasing the speed by 10–20%, at an estimated 10–15% power and area penalty.

The complimentary reset signal ($\overline{Eq}$) is used to reset the regenerative latch, charging both Q and $\bar{Q}$ to logical level high (Fig. 8). The feedback node (*PG_FB*) is used to reset the *rdy* signal shortly before the next comparison, such that the *rdy* signal turns off earlier than the equalizing clock, *Eq*. Because the *rdy* signal controls the reset switch in the pre-amplifier, the recovery phase is extended by allowing extra time for the DAC to settle towards the end (Fig. 10).

It is crucial that only the sign of the comparator differential input voltage matters, not the level. Towards the end of the DAC settling, when the input of the pre-amplifier is at a V_{res} level of a few millivolts, the pre-amplifier switches out of reset phase, starts to sense the DAC output (also noted as V_{res}) and tracks the settling direction. The pre-amplifier also monitors whether the V_{res} voltage changes its sign and accumulates charge at its output, in preparation for the latch operation. By allowing time overlapping of comparison and the DAC settling, the pre-amplifier's response time is merged with the DAC settling time. In this overlap time between t_{DAC} and the comparison time, the input voltage of the regenerative latch is significantly increased, so the resolving time is reduced, yet a reliable comparison is still guaranteed by controlling the latch with the *Eq* signal.

Towards the end of the current bit cycle if V_{res} is still relatively large (several tens of millivolts), then it is possible to allow time sharing, t_{overlap}, between the DAC and the pre-amplifier (Fig. 10) and thus relax the requirement of the DAC settling error to be larger than V_{LSB}, since it will not affect the current bit comparison result. Given that the entire bit conversion cycle is sufficiently long, this settling error will eventually diminish and have no effect on the next bit comparison. For a given bit, with the time overlapping and sufficient gain of the pre-amplifier, a larger V_{res} leads to a larger voltage difference at the pre-amplifier's output, thus helping the latch to evaluate the data faster, and reducing the resolving time.

The scheme of controlling the pre-amplifier and the regenerative latch separately helps to reduce the bit cycle substantially at both low and high V_{res} levels. The duration of a bit cycle thus mainly varies with the reset pulsewidth and the comparison time.

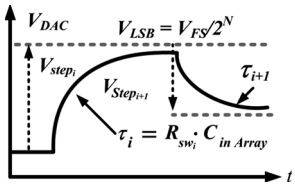

Fig. 11. Fixed DAC settling time by scaling switch sizes as opposed to the targeted step voltages.

D. DAC Design and Non-Binary Capacitance Array

Because the reset pulsewidth strongly depends on the DAC settling time, to achieve high speed, we explored two design options for the DAC: 1) using the same size switches with low equivalent resistance in the DAC for all bits, such that the DAC *R-C* time constant τ is reduced, and 2) equalizing the settling time from MSB to LSB with scaled switches.

If the time constant τ is designed to be the same for each bit, the DAC settling time to V_{LSB} level decreases from MSBs to LSBs. The longest bit cycle occurs when $V_{\mathrm{res}} = \pm V_{\mathrm{FS}}/4 \pm V_{\mathrm{LSB}}$, because the DAC settling step voltage is maximum and the residue input voltage of the comparator is minimum at this point. To achieve high speed, for LSBs, since the step voltage is small, the reset pulsewidth could be reduced to achieve higher speed. For MSBs, a detection circuit could be implemented, to sense the absolute value of V_{res} and the settling error ε at the end of each reset phase. Towards the end, if $V_{\mathrm{res}} \gg \varepsilon$, shortening the reset pulse enables an reliable early evaluation, because the voltage level is sufficiently high from changing the sign and the remaining settling of the DAC is allowed to happen together with the comparison and even extended into the next bit cycle. If V_{res} is small, the long pulsewidth is required to satisfy the worst case scenario, which needs to wait for ε to become less than V_{LSB}. The sensing and controlling circuitry could be quite complicated and power consuming. Therefore, after careful analysis of the trade-offs among speed, area and power, the settling time of the DAC, t_{DAC}, is chosen to be fixed for all bit cycles. Though it leads to a slight sacrifice in speed, it yields a simpler, compact and lower power design.

The settling time t_{DAC} is found to be

$$t_{\mathrm{DAC}} = \tau_i \ln \frac{|V_{\mathrm{step}_i}|}{V_{\mathrm{LSB}}} \tag{4}$$

where τ_i and V_{step_i} denotes the time constant of the ith bit and the voltage step size required for the ith stage to settle.

In order to equalize t_{DAC} for all bits, τ_i needs to be scaled with respect to the voltage step size V_{step_i} for each bit. Given

$$\tau_i = R_{\mathrm{sw}_i} \cdot \mathcal{C}_{\mathrm{in\,Array}} \tag{5}$$

where R_{sw_i} is the equivalent turn-on resistance of the switches in the DAC, the scaling of τ_i is accomplished by scaling the corresponding switch size. Shown in Fig. 11, as the step size becomes smaller for the LSBs, τ_i is increased. While the primary reason to scale the switch sizes is to keep τ_{DAC} constant, there is the usual substantial improvement in area in the DAC since the switch sizes for the LSBs are significantly reduced.

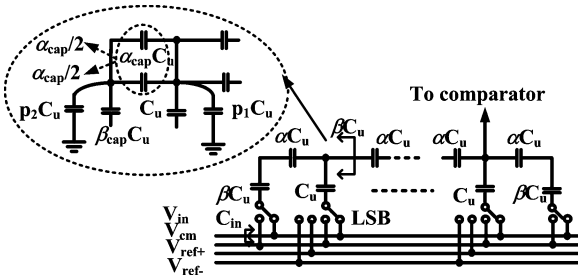

Fig. 12. Non-binary series capacitive ladder network: schematics and parasitic at the interconnects.

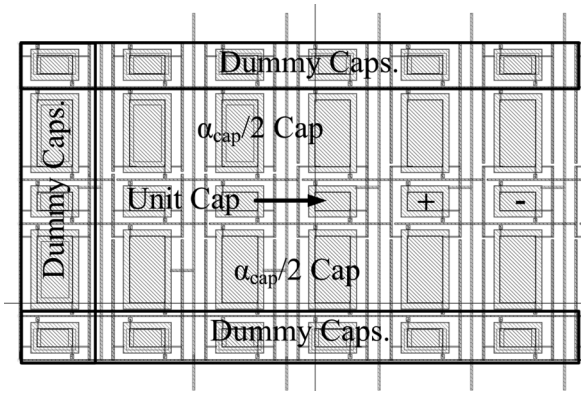

Fig. 13. Binary capacitive ladder with improved symmetry.

To reduce the input capacitor, a series non-binary capacitive ladder is used. The equivalent input capacitance is much lower than a parallel structure [14], [15]. An important disadvantage of the series ladder structure is its sensitivity to parasitic capacitance due to interconnects. This, however, can be taken into account. The basic approach for the design of this network is to have the equivalent capacitance at each floating node be identical. The ideal design equation is

$$\beta = 1 + \alpha \| \beta, \quad \text{radix} = 1 + \frac{\beta}{\alpha} \tag{6}$$

with α and β defined as the ratio between the ideal series capacitance and the unit capacitor [13] (Fig. 12). However, the parasitic capacitances must be taken into account, also as shown in Fig. 12, α and β above can be modified to be

$$\beta = \frac{\beta_{cap} + p_2}{p_1 + p_2 + 1} \; and \; \alpha = \frac{\alpha_{cap}}{p_1 + p_2 + 1} \tag{7}$$

with p_1, p_2 the ratio between the parasitic associated with these interconnects to the unit capacitance [13].

By iteratively estimating and simulating the capacitance at floating nodes and the corresponding ratio of α and β, for moderate resolution, the radix matching from bit to bit could be improved and compensated adequately over process.

The resulting input capacitance is only 84 fF, which significantly shortens the DAC settling time and increases the input bandwidth. The capacitor array is implemented with low-cost metal-oxide-metal plate-to-plate capacitors and particular care was taken to achieve adequate capacitor accuracy with layout. Each α capacitor is divided into two $\alpha/2$ capacitors, located at the top and bottom of a column cell (Figs. 12 and 13). This not only compensates for the vertical process variation, but also provides better differential matching by interleaving the positive-side and negative-side capacitor arrays. Dummy capacitances are placed on each side to further improve matching. α and β values are chosen such that the equivalent radix for the capacitive ladder is $1.9 \sim 2$ (essentially a binary network), but with the advantage of allowing some dynamic decision errors and avoiding missing codes. One bit redundancy is implemented for testing and to avoid significant bit weight loss. The passive bottom plate sampling network is combined with the binary capacitive ladder. Relatively small switches can be used but a high input bandwidth of greater than 10 GHz was still achieved.

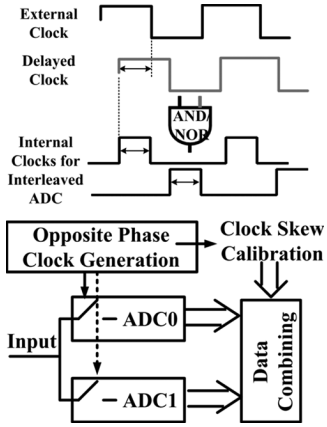

Fig. 14. Opposite phase clock generation for the time interleaving topology.

The unpredicted parasitic variation and capacitor mismatch results in a change of the effective radix for each bit. These discrepancies cause variations in the bit weights and lead to non-linearity of the ADC. This systematic error is, however, compensated by foreground off-chip calibration where a known full-range sinusoidal signal is injected. The converted digital outputs are used to reconstruct the initial input signal. The bit weights are then calibrated using an adaptive algorithm to minimize the mean-square error.

E. Opposite Phase Clocks for Time Interleaving

To perform time interleaving, pair of internal clocks are generated from a 50% duty cycle square wave off-chip sampling clock as shown in Fig. 14. The internal non-overlapping sampling clocks with 180 degree phase shift are generated on-chip for the time interleaving. The input clock is buffered and delayed on chip. Particular care was taken in the layout to generate and distribute the opposite phased clocks to ensure 180 degree phase shift. It has been observed that any imbalance from the two sampling clocks, as well as undesired clock jitter caused by the noise from the generation and distribution network will result in ENOB degradation [26].

V. Measurement Results

The converter is implemented in a 1.2 V 65 nm low-power CMOS process. Each ADC only occupies an area of 0.35×0.16 mm^2. The total die size is 1.6×1.4 mm^2 of which the active area occupies only 0.11 mm^2. The measured results show the ENOB of a single ADC scales from 5.6 bits at 100 MS/s to 5.0 bits at 500 MS/s (Fig. 15). The dynamic performance using input above Nyquist rate ranging up to 500 MHz shows the signal to noise and distortion ratio (SNDR) at different sampling frequency remains above 28 dB (Fig. 16). We believe the

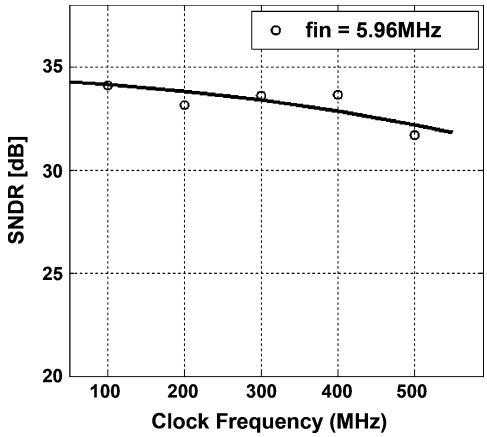

Fig. 15. Measured SNDR versus sampling frequency for one single ADC.

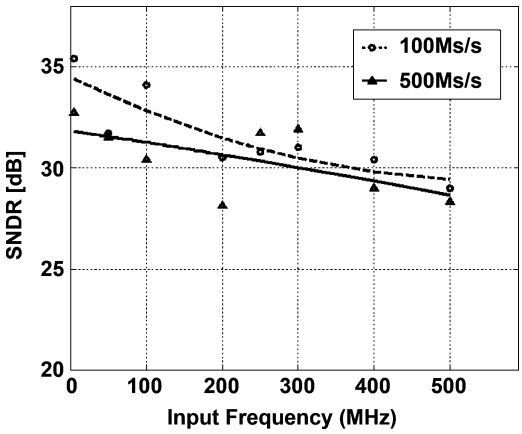

Fig. 16. Measured SNDR versus input frequency for one single ADC.

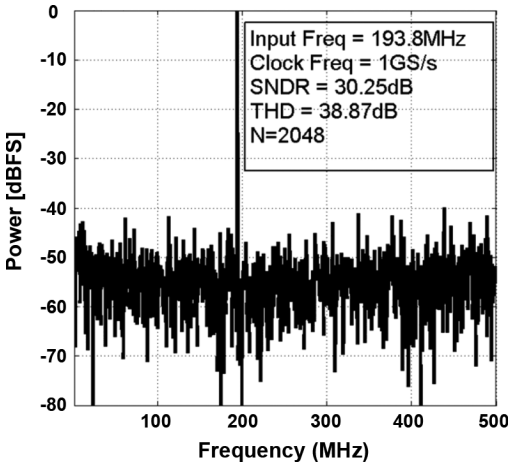

Fig. 17. Measured power spectrum for the interleaved ADC.

200 MHz degradation when sampling at 500 MS/s was due to a spur from an unknown source on the test circuit board. Figs. 17 and 18 show the time-interleaved ADC performance is increased to 1 GS/s at about twice the power and area. The static performance of the interleaved ADC is also characterized by DNL and INL measurements (Figs. 19 and 20).

Among our relatively small samples of chips, even with the capacitance and parasitic variance due to process, DNL and

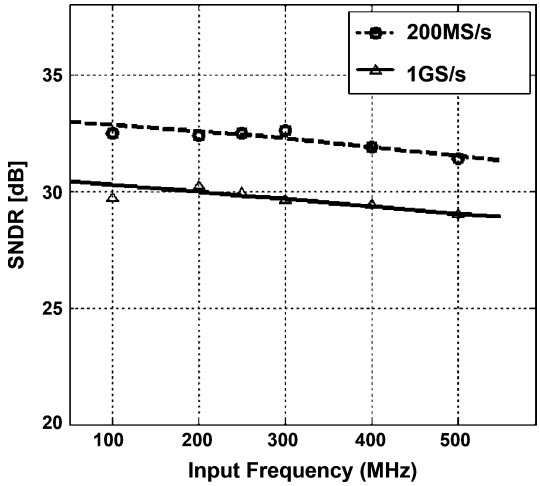

Fig. 18. Measured SNDR versus input frequency for the interleaved ADC.

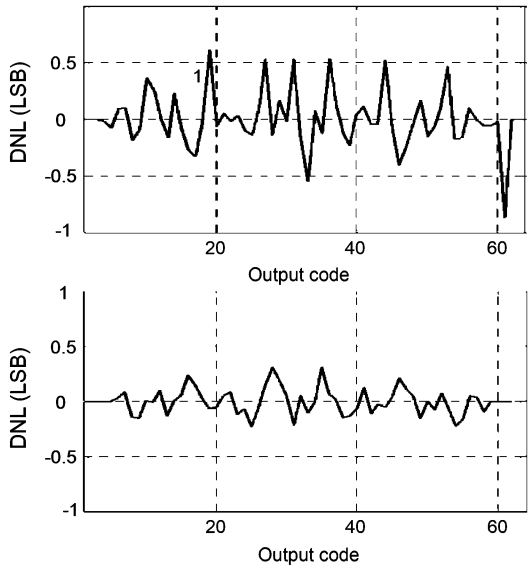

Fig. 19. DNL before and after calibration.

INL are only around 0.8 LSB. After the digital calibration for the bit weights and the subtraction of the offset, as mentioned in Section IV-C, DNL improves by almost half an LSB and INL improves by more than 0.4 LSB. This is equivalent to a 2–3 dB improvement in SNDR. The clock skew between the two high-frequency clocks is calibrated out, resulting in only 0.7 dB degradation in SNDR from a single ADC performance. The chip microphotograph is shown in Fig. 21. Two ADCs, the clock generation and distribution network, as well as the DC bypass capacitors were implemented. In order to facilitate measurements, a 1 K word memory is included on-chip. The total active area is 0.11 mm^2. The analog, digital and clock circuitry consumes 1.51 mW, 4.05 mW and 1.16 mW respectively at a sample rate of 1 GS/s. With the standard FOM for ADCs is defined as $\mathrm{power}/(2^{\mathrm{ENOB}} \cdot f_s)$, the time-interleaved ADCs achieve 0.21 pJ/conversion step, which compares favorably to other asynchronous architecture, SAR and high-speed ADCs [13], [27]–[31]. The performance results are summarized in Table I.

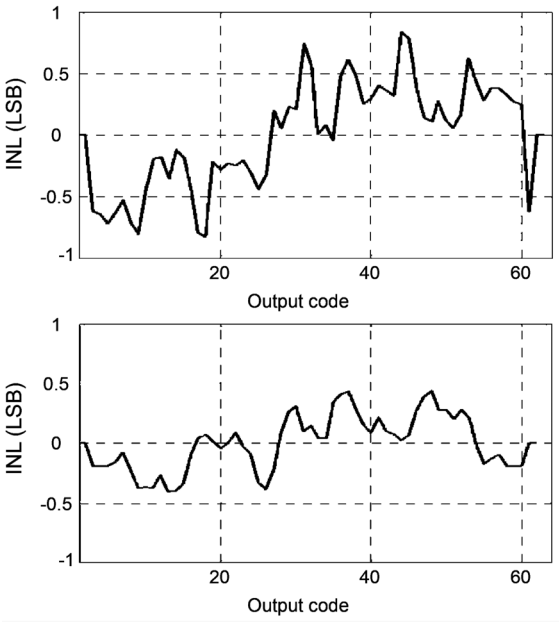

Fig. 20. INL before and after calibration.

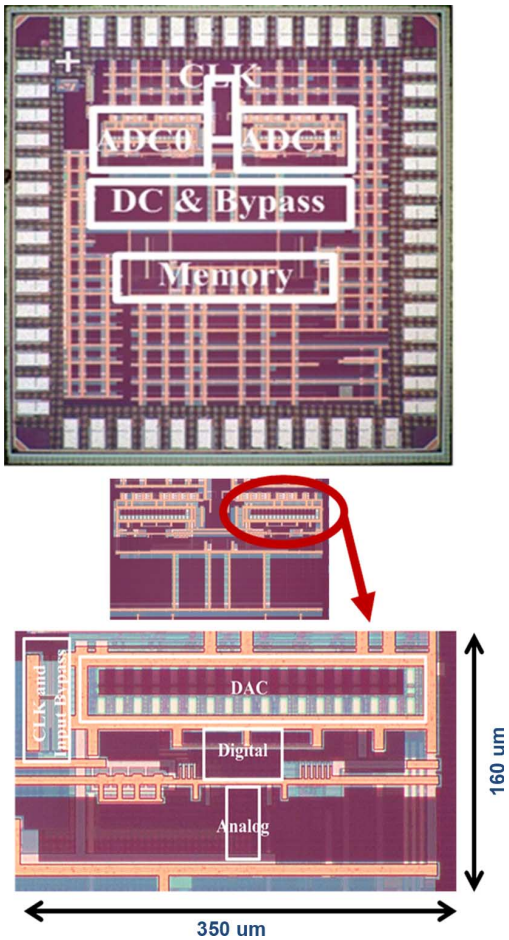

Fig. 21. Chip microphotograph.

TABLE I
PERFORMANCE SUMMARY

Technology		65nm 7M Low Power CMOS	
ENOB		5.0 bits	
Sampling rate		UP to 500 MS/s for single ADC (1GS/s with time interleaving)	
Supply voltage		1.2 V	
Peak SNDR		31.5 dB (f_S= 1GS/s for two ADCs)	
Area		0.11mm^2	
Figure of Merit		0.21 pJ/conversion step	
Power	Analog	1.51mW	Total (two ADCs): 6.27mW
	Digital	4.05mW	
	Clock	1.16mW	

VI. CONCLUSION

In the asynchronous SAR ADC design, to enhance the performance, it is crucial to design a fast resolving comparator, fast digital circuits and a quick settling DAC. A dynamic sense amplifier is used to boost the gain during the comparator transition without adding static power consumption. The semi-closed loop digital circuits allow a much faster successive approximation decision and the series capacitive ladder significantly reduces the equivalent input capacitance, hence benefitting both the input sampling and the DAC settling.

The asynchronous architecture not only achieves higher speed at lower power in comparison to a synchronous approach, but it allows the use of metastability detection which can be used with a simple extension to the SA algorithm to eliminate any ENOB degradation. This algorithm extension relies on the fact that there will only be one bit evaluation in metastability in an SAR architecture and thus metastability can easily be detected by simply determining if there is less than an N bit output. A simple algorithm was described which then creates the correct N bit code.

The proposed circuit implementation carefully addresses the asynchronous dynamic properties of the SAR design. The topology to generate completion signals is based on the analysis of the comparator dynamic transition, and the approach to create and optimize the overlap time between the DAC settling and the comparison, significantly increases the speed of the architecture.

A bit independent DAC settling was chosen, since reducing the switch sizes reduces the DAC area and a fixed time avoids complex DAC completion sensing circuitry, thus saving power with only a slight penalty in speed.

In summary, a time-interleaved asynchronous SAR ADC architecture has been demonstrated to achieve high power efficiency for a high-speed and medium-resolution converter requiring very small area in 65 nm CMOS. It not only achieves a FOM of 0.21 pJ/conversion step, but is believed to be an approach which will scale well into future technologies.

ACKNOWLEDGMENT

The authors acknowledge the contributions of Mike Chen, the NSF Infrastructure Grant 0403427, wafer fabrication donation of STMicroelectronics, and the support of the C2S2.

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Jing Yang (M'04) received the B.S. degree in automation from Tsinghua University, China, in 2001, and the M.S. degree in electrical engineering and computer sciences from the University of California, Berkeley, in 2004. She graduated with a Ph.D. degree from the University of California at Berkeley under Prof. Brodersen in 2010, where she was a member of the Berkeley Wireless Research Center.

Her research interests include architectures and implementation of active time domain interference cancellation for the future wideband radios, and analog/mixed signal front-end design for cognitive radio systems.

Ms. Yang was the recipient of the UC Regents Fellowship at Berkeley in 2002 and the Outstanding Graduate Instructor Award at UC Berkeley in 2007.

Thura Lin Naing (M'07) received the B.S. degree in electrical engineering and computer sciences from the University of California, Berkeley, in 2007, where he is currently working toward the Ph.D. degree in electrical engineering and computer sciences.

His research interests include mixed-signal integrated circuits, microelectromechanical circuits and systems (MEMS), and their application in wireless communication.

Robert W. Brodersen (F'82) received the Ph.D. degree from the Massachusetts Institute of Technology (MIT) in 1972.

He was with the Central Research Laboratory at Texas Instruments for three years. Following that, he joined the Electrical Engineering and Computer Science faculty of the University of California at Berkeley, where he now is an Emeritus Professor and Chairman of SiBEAM and BEECube. He has won best paper awards for a number of journal and conference papers in the areas of integrated circuit design, CAD and communications, including the IEEE Baker Award for Best Paper in the IEEE transactions the IEEE Morris Liebmann Best Paper award. In 1982 he became a Fellow of the IEEE and in 1988 he was elected to be member of the National Academy of Engineering. In 1986 he received the Technical Achievement awards in the IEEE Circuits and Systems Society and in 1991 from the Signal Processing Society. In 1996 he received the IEEE Solid State Circuits Award, in 1999 received an honorary doctorate from the University of Lund in Sweden and in 2000 he received a Millennium award from the Circuits and Systems Society and the Golden Jubilee award from the IEEE. In 2001 he was awarded the Lewis Winner Award for outstanding paper of the IEEE International Solid-State Circuits Conference and in 2005 he received the Jack Raper Outstanding Paper Award for that conference.