A Novel Low Power 1 GS/s S&H Architecture With Improved Analog Bandwidth

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***Abstract*—A new sample-and-hold (S&H) architecture is proposed for time-interleaved analog-to-digital converter (ADC). The use of this S&H circuit in front-end of a time-interleaved ADC system eliminates the need for sample-time calibration. Using the techniques of precharging and output capacitor coupling along with a new sampling technique called middle-plate-sampling can mitigate the stringent performance requirements for the opamp and sampling switches, resulting in low power consumption and allowing very high sampling rate. Simulated by HSPICE with a standard BSIM3v3 0.18 μm technology, the S&H achieves 10-12 bits resolution for a 1.6-V_{pp} output at 1-GHz sampling rate. The S&H dissipates 12 mW from a 1.8-V supply.**

***Index Terms*—Analog integrated circuits, analog-to-digital circuits (ADCs), CMOS analog integrated circuits, low power analog circuits, pipeline, sample-and-hold (S&H) circuits.**

I. Introduction

IN SOFTWARE-DEFINED radio (SDR) applications, a high-speed sampling analog-to-digital converter (ADC) is required for broadband multichannel base station communication systems. The requirement of medium-to-high resolution (10–14 bits) in addition to high sampling rate ($\sim$ 1 GS/s) and reasonable power consumption make the time-interleaved ADC architecture the most suitable choice for SDR applications. However, the time-interleaved architecture suffers from three major problems of gain error, offset error, and sample-time error of its time-multiplexed channels. The gain and offset errors can be sufficiently suppressed by using traditional calibration techniques [1]–[3], while sample-time errors are more difficult to mitigate, and thus impose stringent performance limitations on the time-interleaved architecture. In order to eliminate phase offset between the parallel channels, a single front-end sample-and-hold (S&H) is necessary, as in [4]. Trying not to use such a front-rank S&H as in [5] has caused other limitations such as low input bandwidth, and incapability of performing bottom-plate-sampling which causes further inaccuracy. Even in [4], in addition to the low analog bandwidth, the necessity of the use of Triple-well CMOS technology can reduce cost-efficiency.

A major speed limitation in conventional closed-loop S&H configurations is the output slewing of the opamp. Another important issue is the limited input bandwidth of the switched-capacitor (SC) sampling circuit due to the limited bandwidth of the inherent resistor–capacitor (RC) network. This paper presents a new S&H that takes advantage of two novel techniques to overcome these issues. The precharging technique introduced in [6] is modified in order to considerably reduce the slewing of the opamp for large S&H output swings. Furthermore, a new sampling technique is proposed which increases the input analog bandwidth of the S&H and makes the use of ordinary clock-boosted switches possible under 1-GS/s sampling rate.

In Section II, a modification to the precharging technique of [6] is proposed. In Section III, a new sampling technique called Middle-plate-sampling is proposed. The circuit realization of the proposed S&H is discussed in Section IV. Section V describes the circuit implementation. Simulation results are presented in Section VI and final conclusions are made in Section VII.

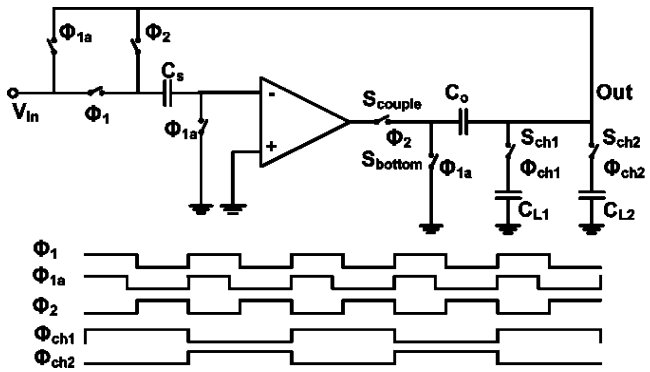

Fig. 1. Proposed precharged S&H circuit.

II. Precharged S&H

The proposed modification to the precharging technique of [6] is shown in Fig. 1. The additional clock phases, φ_{ch1} and φ_{ch2}, applied to switches S_{ch1} and S_{ch2}, represent two channels of a time-interleaved ADC.

During the channel-1 sample mode $(\varphi_1 = 1, \varphi_{ch1} = 1)$, the capacitors C_S, C_o, and C_{L1} are charged by the input. The signal is sampled on the three capacitors at the falling edge of φ_{1a}. In the hold mode $(\varphi_2 = 1)$, the S&H output settles to its final value in a much shorter time due to the precharging operation. During the channel-2 operation mode $(\varphi_1 = 1, \varphi_{ch2} = 1)$, the same operations are done for C_S, C_o and C_{L2}.

The circuit of Fig. 1 has two main advantages over that of [6]. First, in the circuit of Fig. 1, the opamp is not used in the sample mode. As a result, double-sampling can be used in the proposed circuit to further increase the sampling rate.

Second, in the circuit of [6], C_o and C_L are sampled at the falling edge of φ_1, while C_S is sampled at φ_{1a}; thus, the voltage

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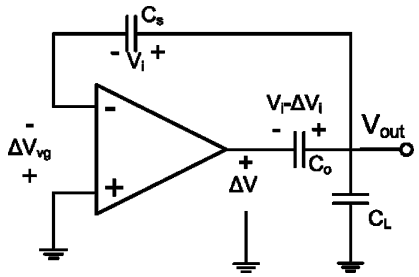

Fig. 2. Precharged S&H in hold mode; analysis of finite DC gain of opamp.

sampled in C_S is different from those in C_L and C_o, depending on the delay between φ_1 and φ_{1a}. Therefore, this technique is only suitable for slow varying inputs. However, in the proposed circuit, since the three capacitors are sampled at the same instant at the falling edge of φ_{1a}, the input signal is stored equally on all the capacitors. As a result, even for high frequency input signals, the difference that should be compensated by the opamp in the hold mode is very small.

A. Performance Analysis

It can be shown that the combination of output capacitor coupling by C_o [7] and precharging reduce the required dc gain and output swing of the opamp by a factor of k.

Fig. 2 shows the hold mode of the S&H of Fig. 1. V_i is sampled on C_S. Assuming that for any reason such as charge injection or RC delay, V_{Co} and V_{Cl} differ from V_i by ΔV_i, we have:

$$\begin{aligned} &V_i' = (1-\varepsilon)\times V_i, \quad \Delta V_i = \varepsilon V_i, \;\; 0 \le \varepsilon \le 1 \\ &C_o = \gamma \times C_L. \end{aligned} \tag{1}$$

Here V_i' is the voltage sampled on C_o and C_L, γ is the ratio of C_o to C_L, and ε represents the relative error of V_{Co} and V_{Cl} with respect to V_i. As shown in Fig. 2, the error referred to the input of the opamp is equal to ΔV_{vg}, which is given by

$$\begin{aligned} \Delta V_{vg} &\approx \left(1+\frac{1}{\gamma}\right)\times\frac{\varepsilon V_i}{1+A} \approx \frac{1}{kA}V_i \\ k &= \frac{1}{\varepsilon\left(1+\frac{1}{\gamma}\right)} \gg 1. \end{aligned} \tag{2}$$

As can be seen, ΔV_{vg} is k times smaller than in simple flip-around S&H (V_i/A). If the output node of the S&H is precharged suitably, ε is very small. Since the resolution of the S&H is proportional to the opamp virtual ground, ΔV_{vg}, for a specific resolution of the S&H output, an almost k times lower DC gain is required for the opamp, compared to the simple flip-around architecture.

It can be shown that the opamp output swing is also reduced to

$$V_{\text{swing,op}} = A \times V_{\text{err,in}} = \frac{V_i}{k}. \tag{3}$$

As can be seen, the output swing of the opamp is k times smaller than that of the S&H. In addition, the nonlinear slew behavior of the opamp is k times lower or even eliminated from the hold mode of the opamp. The smaller swing further reduces the nonlinearity introduced to the S&H by the opamp.

For a specific S&H resolution, and assuming a first-order settling, the relationship between the error voltage and settling times of a flip-around S&H and that of the new precharged S&H is given by

$$V_{\text{err,flip}} = V_i e^{-(t_{\text{flip}}/\tau)} \tag{4}$$

$$V_{\text{err,prch}} = \frac{1}{k}V_i e^{-(t_{prch}/\tau)} \tag{5}$$

where t_{flip} and t_{prch} are the settling times of the flip around and precharged configurations, respectively. For equal error voltages t_{prch} is given by

$$t_{\text{prch}} = t_{\text{flip}} - \tau \ln k \tag{6}$$

which shows the settling improvement of the proposed S&H. In this comparison, the time needed for large-signal slewing of the opamp in the flip around architecture is neglected; otherwise, the settling improvement in the precharged S&H would be much more significant.

In addition, due to the higher settling speed of the precharged architecture, smaller bandwidth is required for the opamp which results in smaller Noise Bandwidth (NBW) and smaller power consumption.

III. Middle-Plate-Sampling

Although the limitations of the opamp can be alleviated by the precharging technique, switches are still imposing major restriction on high speed sampling. A sampling SC circuit can be simply modeled by a passive RC network. Therefore, the sampled input signals with higher frequencies experience undesired amplitude attenuation and significant nonlinear phase distortion. The amplitude and phase degradation can be shown in terms of the input frequency and R, C values as follows:

$$A(j\omega) = \frac{1}{1+j\omega RC} \rightarrow \begin{cases} |A(j\omega_{\text{in}})| = \frac{1}{1+\omega_{\text{in}}^2 R^2 C^2} \\ \Delta\phi(\omega_{\text{in}}) = -\tan^{-1}\omega_{\text{in}} RC. \end{cases} \tag{7}$$

For instance, for a 500-MHz input signal and a sampling frequency of 1 GHz with 50-Ω total switch-resistance and 4-pF sampling capacitor, the signal is sampled with almost 15% amplitude degradation and 32° phase delay.

To have a more accurate sampling, it is desired to increase the bandwidth of the sampling RC network.

In a specific technology, the product of the parasitic capacitance of a switch and its ON resistance is almost constant as given by

$$\left.\begin{aligned} R &\propto \frac{1}{\frac{W}{L_{\min}}} = \frac{L_{\min}}{W} \\ C &\propto W \times 2\lambda \end{aligned}\right\} \rightarrow RC \propto L_{\min} \times 2\lambda \propto L_{\min}^2. \tag{8}$$

Here, λ is the minimum lithography resolution of the technology mask and $L_{\min}$ is the minimum allowable length of transistors. The almost constant value of the RC product shows that in bottom-plate-sampling with ordinary switches, for very high sampling rates (> 500 MHz), switch oversizing is no more a proper solution for improving the sampling performance and bandwidth.

In order to reduce the RC product, this work presents a novel sampling technique which is shown in Fig. 3. Two sampling capacitors are used instead of one. As shown in Fig. 3(a), in the

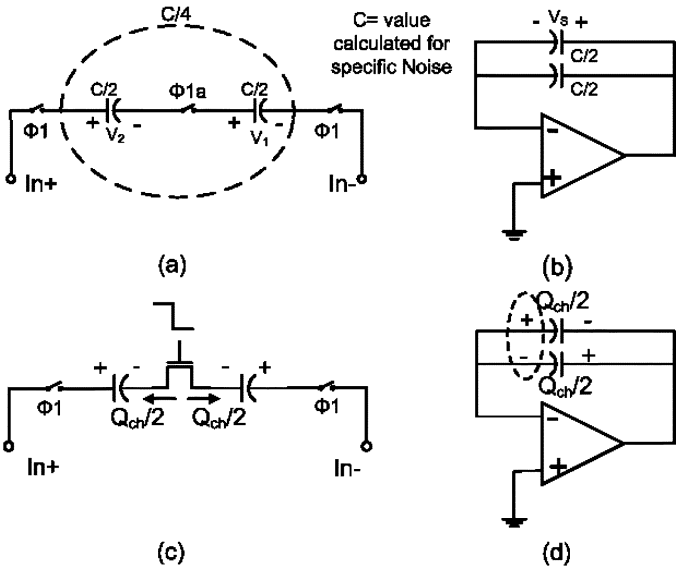

Fig. 3. Middle-Plate Sampling: (a) Sample mode. (b) Hold mode. (c) Charge injection due to the middle-plate switch. (d) Cancellation of charge injection.

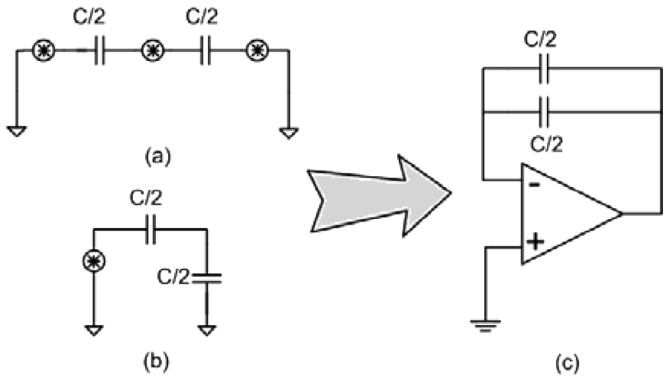

Fig. 4. Analysis of sampling noise in middle-plate sampling.

sampling phase, the capacitors are connected in series, between the positive and negative inputs of the S&H. As a result, the capacitors are charged with the differential input signals, since the voltage of the middle-plate node is virtually equal to the input common-mode level. In the hold mode as shown in Fig. 3(b), the capacitors are put in parallel with the same signal polarity. As a result, the sampled input signal is held across the opamp.

Similar to the concept of bottom-plate-sampling, in order to minimize the signal-dependent charge injection due to the sampling switches, a clock phase φ_{1a} with an earlier falling edge than that of φ_1 is needed to drive the switch in the middle. Since the sampling instant is controlled at the middle plates of the capacitors, this sampling technique is named "Middle-Plate-Sampling".

Using middle-plate-sampling, the RC product is reduced due to the series connection of the capacitors in the sampling phase. As will be discussed later in this section, the output noise due to the sampling switches remains the same as the case of bottom-plate-sampling. Thus, if a total hold capacitance of C is required for achieving a desired SNR, the two sampling capacitors used in middle-plate-sampling must simply have a value of $C/2$ as shown in Fig. 3. Thus, when the capacitors are connected in series in the sampling phase, an equivalent capacitance of $C/4$ is differentially seen by the input buffers. Having three switches $(3R)$ and an equivalent capacitance of $C/4$ in the RC path, middle-plate-sampling shows at least 8/3 times higher analog bandwidth compared to bottom-plate-sampling which uses two switches $(2R)$ and a sampling capacitor value of C. This improvement makes it possible to use conventional switches for very high-speed sampling and undersampling applications.

In Sections III-A–C, the effects of nonidealities on middle-plate-sampling are studied.

A. Sampled-Signal Validity

If the middle-plate switch were ideal, the input signal would be sampled equally on both capacitors. However, in the presence of the parasitic junction capacitors and mismatch, sampling might be performed unequally on the two capacitors, and thus the middle-plate voltage might deviate from its virtual common-mode level (CM) by a value of ΔV_{MP}. As expressed in (9), V_1 is sampled on C_1 and V_2 sampled on C_2, in which C_1 and C_2 are the sampling capacitors whose values are equal to C.

$$\text{sample: } \left.\begin{matrix} V_1 = V - V_{MP} \\ V_2 = V + V_{MP} \end{matrix}\right\} \rightarrow \text{hold: } 2CV_{\text{sample}} = C(V_1 + V_2)$$
$$V_{\text{sample}} = \frac{1}{2}(V - V_{MP} + V + V_{MP}) = V. \tag{9}$$

The signal corruption and middle-plate variations could be more accurately investigated by considering the effect of capacitor mismatch. If the capacitor values are different by ΔC, the signal held on the capacitors in φ_2 can be calculated as in (10), in which V_1, V_2 are the voltages stored on C_1, C_2 and V_{sample} is the final sample voltage held on the parallel capacitor.

$$\text{sample}: \begin{cases} C_1 = C + \frac{\Delta C}{2} \\ C_2 = C - \frac{\Delta C}{2} \end{cases} \rightarrow \begin{cases} V_1 = \frac{C_2}{2C} \times 2V_{\text{in}} \\ V_2 = \frac{C_1}{2C} \times 2V_{\text{in}} \end{cases}$$
$$\text{hold}: (C_1 + C_2) V_{\text{sample}} = C_1 V_1 + C_2 V_2 \rightarrow$$
$$2CV_{\text{sample}} = \left[\frac{C^2 - \left(\frac{\Delta C}{2}\right)^2}{C} + \frac{C^2 - \left(\frac{\Delta C}{2}\right)^2}{C} \right] V_{\text{in}} \rightarrow$$
$$V_{\text{sample}} = \left[1 - \left(\frac{\Delta C}{2C} \right)^2 \right] V_{\text{in}}. \tag{10}$$

Therefore, the sampled signal would be held on the sampling capacitors correctly with proper accuracy. This robustness to nonidealities is the main advantage of this sampling circuit over the open-loop S&H of [8].

B. Signal-Dependent Charge Injection

Another important issue in SC circuits is the charge injection due to the sampling switches which degrades the accuracy of the sampled signal. Interestingly, as shown in Fig. 3(c) and (d), the charge injection on the two capacitors—due to the middle-plate switch—will be neutralized in the hold mode. Therefore, the effect of charge injection is negligible even if a large middle-plate switch is used. This can further improve the analog bandwidth and sampling performance of the S&H.

C. Thermal Noise Effects

Considering the sampling noise issues as in Fig. 4, the thermal noise of the three input switches shown in Fig. 4(a) can be

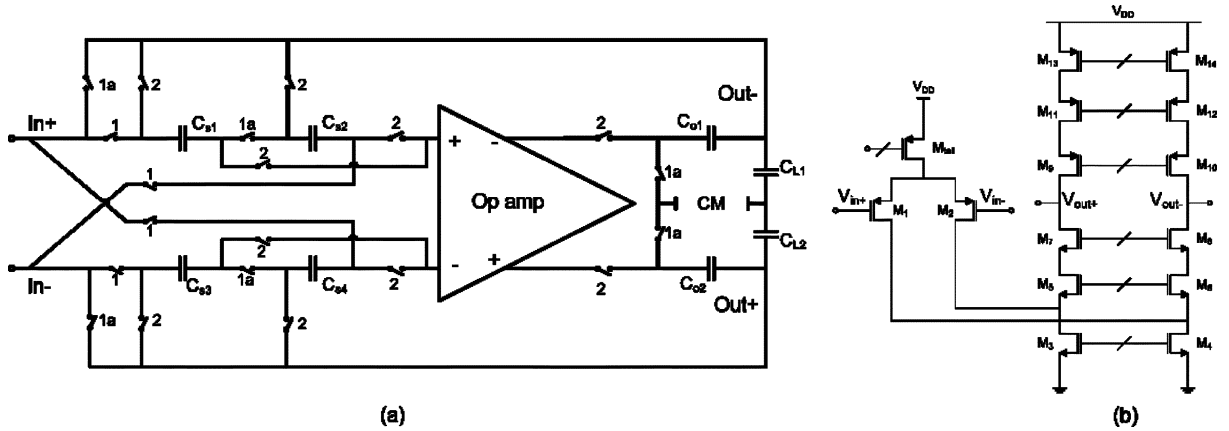

Fig. 5. (a) Proposed S&H using middle-plate sampling. (b) Folded-triple-cascode opamp.

simply modeled with an equivalent thermal noise source shown in Fig. 4(b). The equivalent noise source is sampled on an equivalent capacitor of $C/4$, with an rms of 4 kT/C. However, the sampled noise voltages see a gain of 1/2 in transition from the sample mode to the hold mode, since the noise voltages are fully correlated. Therefore, the sampling noise power in the output remains the same as the case of bottom-plate-sampling as

$$\left|\frac{V_{\rm no}}{V_{\rm ns}}\right| = \frac{1}{2} \rightarrow |H_n|^2 = \frac{1}{4}$$
$$\left|V_{\rm ns(rms)}\right|^2 = \frac{kT}{\frac{C}{4}} = 4\frac{kT}{C} \rightarrow \left|V_{\rm no(rms)}\right|^2 = \frac{kT}{C} \quad (11)$$

where $V_{\rm ns(rms)}$ is the rms thermal noise voltage of the switches sampled on the series sampling capacitors, and $V_{\rm no(rms)}$ is the output rms noise voltage due to the sampling switches.

As previously described, with the total hold capacitance of C required for a specific SNR and signal swing, the noise power due to the sampling switches would remain the same as the case of bottom-plate-sampling. Thus, the two capacitors used in middle-plate-sampling can be reduced to $C/2$ without any SNR degradation.

IV. Complete Precharged S&H With Middle-Plate-Sampling

By exploiting both precharging and middle-plate-sampling, a new sample & hold architecture is proposed in this section. Higher analog input bandwidth is achieved by middle-plate-sampling, while precharging technique along with output capacitor coupling relax the DC gain, bandwidth and output swing requirements for the opamp. The lower bandwidth requirement of the opamp also results in reduced power consumption. The fully-differential implementation of the proposed S&H circuit is shown in Fig. 5.

In the circuit shown in Fig. 5, the core opamp is only used in the hold phase (φ_2) and is idle in the sample phase (φ_1). By making use of the opamp in both phases sampling rate is doubled, while power consumption remains constant (double-sampling is not shown in Fig. 5 for simplicity).

For the implementation of double-sampling two groups of sampling capacitors are required, one sampled in φ_1 and the other sampled in φ_2. The time-interleaved architecture consists

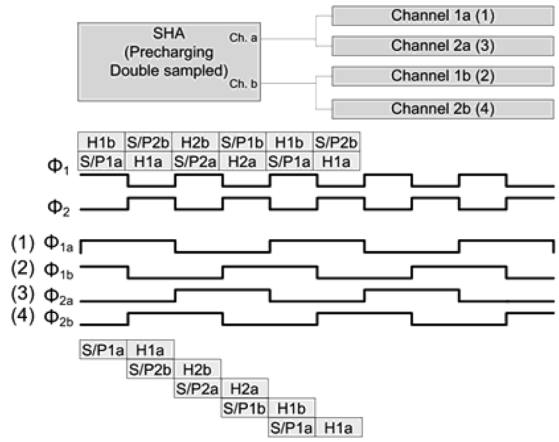

Fig. 6. Time-interleaved architecture; clocking scheme of precharging along with double-sampling.

of four channels, i.e. one pair of time-interleaved channels which are double-sampled. Fig. 6 shows the time-interleaved architecture and the clocking scheme needed for performing both precharging and double-sampling.

It is worth noting that double-sampling in this work is merely used to achieve the sampling rate of 1 GS/s with reasonable power consumption in the 0.18-μm technology. Although double-sampling reintroduces timing error to the interleaving structure due to the phase skew between φ_1 and φ_2; since only two clock phases are utilized, the timing error can be corrected with low complexity as described in [1]–[3].

V. Circuit Implementation

The differential version of the precharged S&H circuit of Fig. 1 and the proposed S&H of Fig. 5 are both simulated in a standard mixed-mode 0.18 μm CMOS technology, with 1.8 V supply voltage. Considering noise issues for a resolution of 12 bits with 1.5 bit gain-stages following the S&H, capacitor values are chosen to be: $C_L = 2.5$ pF, and $C_o = 2.5$ pF. The sampling capacitor is chosen to be $C_S = 2$ pF for middle-plate sampling, and $C_S = 4$ pF for precharged S&H of Fig. 1. Since two pairs of series sampling capacitors are being used, the total single-ended capcitive load seen by the input buffers has a value of $(C_S + C_L + C_o)$, which is equal to 9 pF in both cases.

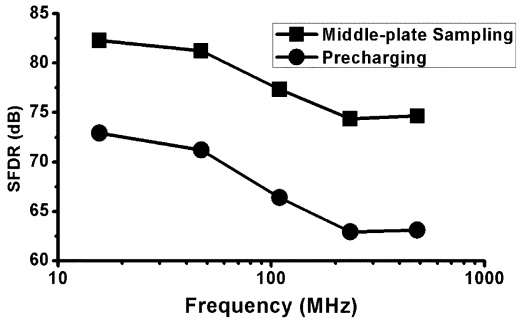

Fig. 7. SFDR versus input frequency for 1.6 V_{pp} swing.

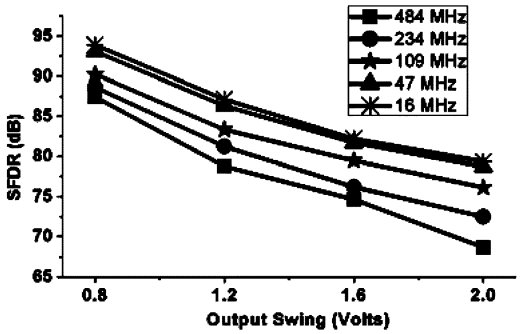

Fig. 8. SFDR versus output swing for different input frequencies for S&H with middle-plate sampling.

The proposed circuits are using a folded-triple-cascode opamp configuration shown in Fig. 5(b). Using this configuration, a DC gain of 74 dB is achieved which ensures that the accuracy is not limited by the finite DC gain of the opamp. The opamp experiences a total differential linear output swing of only 200 $\mathrm{mV_{pp}}$ for having a differential S&H output of $1.6\mathrm{V_{pp}}$.

The opamp has a unity-gain bandwidth (UGBW) of 600 MHz driving a 2.5 pF load and provides proper settling behavior for an accuracy of 0.03% in less than 1 ns, while dissipating only 12 mW. The analog switches are clock-boosted NMOS transistors which achieve higher switching speed and lower distortion.

VI. Simulation Results

The precharged S&H of Fig. 1 and the proposed S&H of Fig. 5 are verified by using the opamp described in the previous section, for 1-GS/s sampling rate which is achieved by performing double-sampling with a 500 MHz clock frequency. The input is a differential 1.6 $\mathrm{V_{pp}}$ sinusoid signal. The input frequency is swept from low frequencies to near 1/2 of the sampling frequency.

Compared to the case of precharging with simple bottom-plate sampling, almost 10 dB higher SFDR is achieved when precharging is accompanied by middle-plate-sampling. The precharged S&H with middle-plate-sampling shows higher than 74 dB SFDR which is suitable for 12 bits resolution in 1-GHz sampling rate. The SFDR results of the two structures are plotted in Fig. 7. In Fig. 8, SFDR in different input frequencies for the proposed S&H is plotted versus peak-to-peak S&H output swing. For higher input frequencies, larger output swings result in lower linearity.

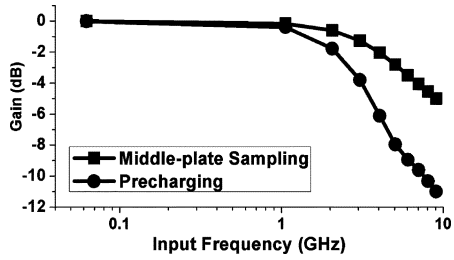

Fig. 9. Attenuation on input signal versus Input Frequency.

The gain of the sampled signal as a function of the input frequency is plotted in Fig. 9. Middle-plate-sampling shows less attenuation in particular where higher input frequencies are applied to the circuit, like in undersampling applications. As shown in Fig. 9, an improvement of twice wider bandwidth $(f_{-3\,\mathrm{dB}})$ is obtained by middle-plate-sampling $(f_{-3\,\mathrm{dB}} = 5.3\ \mathrm{GHz})$ compared to that of simple precharging $(f_{-3\,\mathrm{dB}} = 2.66\ \mathrm{GHz})$.

VII. Conclusion

In the design of a high-speed and high-resolution S&H, the application of both precharging and output capacitor coupling techniques can relieve the original stringent performance requirements for the opamp, such as dc gain, fast settling response, and linear output swing. Middle-plate-sampling introduces a technique to overcome the sampling limitations caused by the use of ordinary switches.

Combining the two techniques, a low power (12 mW) high-speed S&H was proposed which achieves 10–12 bits resolution at 1-GHz sampling rate with much smaller attenuation of the input signal implying almost twice wider bandwidth for the proposed structure compared to the precharging method.

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