A High-Speed and Low-Power Pipelined Binary Search Analog to Digital Converter

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***Abstract*— This paper presents a new analog to digital converter (ADC) architecture targeting ultra high speed and low power applications. The proposed ADC enables operation of SAR ADCs in a pipelined fashion trading latency for speed. Proposed ADC works based on binary search principle. The requirement for residue amplifier in conventional pipelined ADCs is eliminated by interleaved sampling of the analog input signal. Compared to an n-bit asynchronous SAR ADC, where the sampling rate is limited by *n* quantization delays and *n* DAC delays, the proposed ADC speed is only limited by two comparator delays and two DAC delays. A 6-bit 1 GS/s pipelined binary search (PBS) ADC was designed in 90nm CMOS process. Designed PBS ADC reaches a peak SNDR of 35.4dB consuming 3.8mW from a single 1.2V power supply.**

I. INTRODUCTION

In recent years the demand for medium resolution, low power analog-to-digital converters (ADC) with high sampling rates of 1GS/s or more for ultra wideband applications such as cognitive and software defined radios, and high speed serial links has increased. Traditionally, flash ADCs have been used in such applications. However, the power and area in flash ADCs have exponential dependence on resolution. On the other hand successive approximation register (SAR) ADCs are known as the most energy efficient ADCs, but the speed in SAR ADCs is limited to a few hundred mega hertz [1,2]. Hence, new ADC architectures enabling both high speed performance of flash ADCs and low power operation of SAR ADCs are currently being investigated [3-6].

In recent years asynchronous binary search/SAR ADCs were introduced to improve the speed performance of SAR ADCs [3-6]. Asynchronous SAR ADCs operate based on binary search principle like the conventional SAR ADCs. In a typical asynchronous SAR ADC, the feedback loop of the SAR ADC is opened and instead of one comparator, n comparators are used in an n-bit ADC. Output of each comparator is used as clock by the next one while searching the digital code from the most significant bit (MSB) to the least (LSB). Since the delay in the logic feedback path is relaxed, asynchronous SAR ADCs attain higher speeds. Sample rate in such ADCs is limited by *n* quantization delays of the comparators plus *n* DAC delays.

In this work a new pipelined ADC based on binary search algorithm is proposed that trades latency for speed. In the pipelined binary search (PBS) ADC, the residue subtraction and amplification which is used in conventional pipelined ADCs is eliminated and higher operation speed and lower power consumption is achieved.

This paper is organized as follows. The proposed new ADC architecture called pipelined binary search (PBS) based on successive approximation is introduced in section II. Design of a 6-bit PSAR ADC and its core building blocks is presented in section III. Simulation result for the proposed 6-bit 1GS/s ADC in 90nm CMOS process is shown in section IV. Section V is dedicated for conclusion.

II. PIPELINED BINARY SEARCH (PBS) ADC

In a typical n-bit asynchronous binary search ADC [5] the input is first compared with half reference voltage level ($V_{REF}/2$). Based on the output of the first comparator, b_{n-1}, the decision is made whether 1/4 or 3/4 of reference should be compared with the sampled input signal in next comparator to determine b_{n-2}. Next using b_{n-1} and b_{n-2}, a logic decides either 1/8, 3/8, 5/8, or 7/8 reference to be compared with the sampled input to determine b_{n-3}. This process is repeated until the least significant bit (b_0) is determined. All operations are synchronized by a single ADC clock while input signal is held when clock is active. When ADC clock is activated, the comparator clocks are generated asynchronously using the outputs of previous stages through a logic starting from MSB. Hence the speed of such ADC is limited by *n* comparators plus DAC delays. Now consider the configuration shown in Fig.1. This figure shows the conceptual architecture of an n-bit pipelined binary search (PBS) ADC. If the sampled input signal could be delayed in an analog delay line as shown in Fig.1, we would be able to operate the asynchronous binary search ADC in pipelined manner.

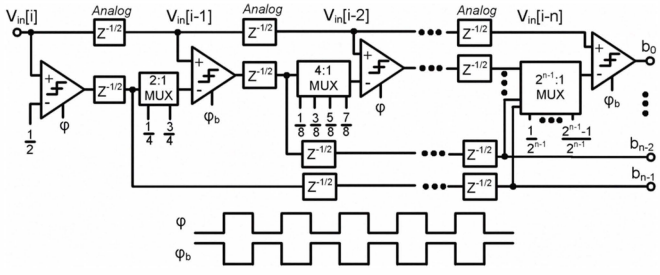

Figure 1. General architecture of an n-bit pipelined binary search ADC

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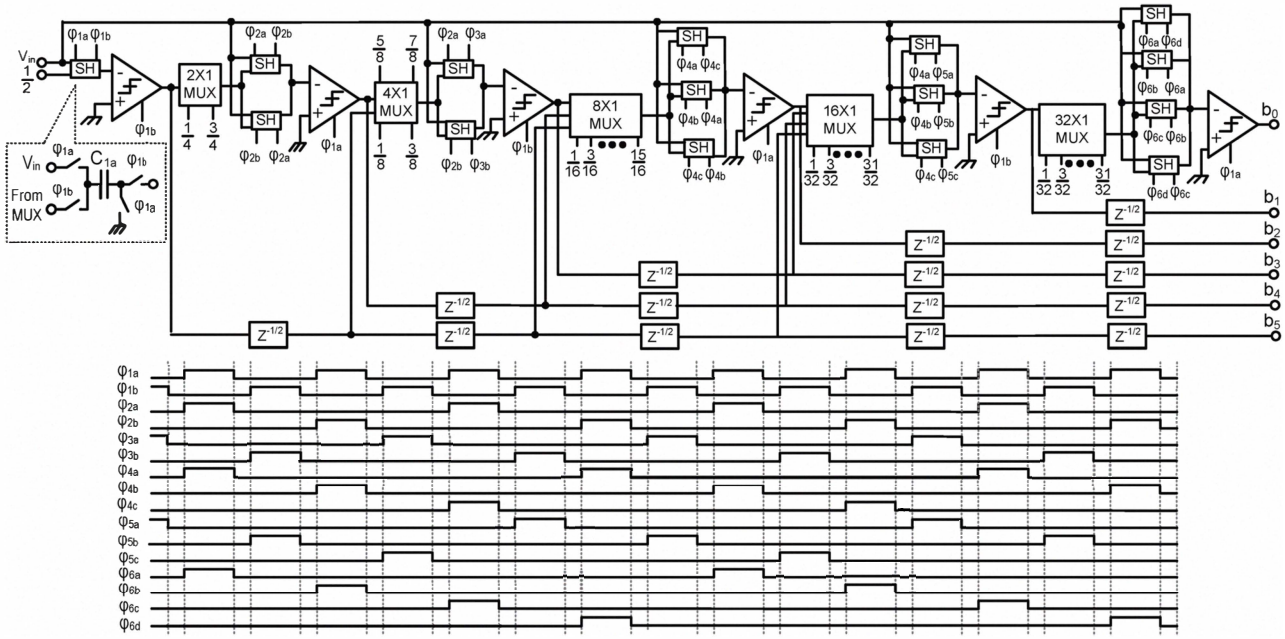

Figure 2. Circuit implementation and timing of a 6-bit PBS ADC.

The idea in PBS architecture is to evaluate the MSBs in the first stages of the pipelined ADC and use these MSBs to reconstruct the signal and compare it with delayed signal to determine the LSBs in the next stages of ADC. In the proposed ADC the sampled input $V_{in}[i]$ is first compared with the half reference voltage, 1/2, to determine the $b_{n-1}[i]$. The input signal, $V_{in}[i]$, and b_{n-1} [i] will then be delayed by half a clock cycle. In next clock phase, delayed $b_{n-1}[i]$ will decide which reference voltage should be compared with delayed $V_{in}[i]$ to evaluate $b_{n-2}[i]$ in the second comparator. Next, $V_{in}[i]$, $b_{n-1}[i]$, and $b_{n-2}[i]$ are delayed by another half clock cycle. In the next clock phase, these delayed digital codes will decide which reference voltage should be compared with delayed $V_{in}[i]$ to determine $b_{n-3}[i]$. At the same time the next MSB corresponding to next input sample, $V_{in}[i+1]$, is being evaluated in the first comparator. Hence in the proposed ADC, while the delayed digital codes are being used to decide which reference level should be compared with the delayed analog input at one stage, new input signal is being sampled and processed in the previous stages. The duration of each clock cycle is now only limited by two comparator delays and two logic delays improving speed roughly n/2 times compared to asynchronous SAR ADCs with the same resolution.

III. Circuit Implementation

The main challenge in circuit implementation of the proposed PBS ADC is delaying the analog input signals. One way to do this is to sample the analog input signal on a capacitor, hold it for the required delay. This sampled signal can be used when all the previous stages of the pipelined ADC are done processing it. This can be done by interleaved sampling of the analog input signal at the input of each comparator. Fig.2 shows the half circuit of a fully differential implementation of 6-bit PSAR ADC along with the timing diagram.

Let $V_{in}[i]$ be the i^{th} analog input sample. On the negative edge of φ, $V_{in}[i]$ is sampled on capacitors C_{1a}, C_{2a}, C_{3a}, C_{4a}, C_{5a} and C_{6a}. Here C_{ix} is the x^{th} sampling capacitor in the i^{th} stage of the pipelined ADC. This input is processed by the first comparator right after the sampling phase to find MSB, b_5. As shown in Fig.2, next digital output bits corresponding to the $V_{in}[n]$ will be evaluated after half, one, one and a half, two and two and a half clock cycles later by second, third, fourth, fifth, and sixth comparators, respectively. Hence, two different sampling paths are required at the input of second and third comparators, three different sampling paths are required at the input of fourth, fifth and sixth comparators. In each clock cycle, each path can be used to either sample or hold the input signal, or to evaluate previously sampled signal. An analog multiplexer can be used that decides which reference level must be compared with the sampled input based on delayed previous digital outputs. In the proposed pipelined ADC no residue opamp is used which enables higher speed, lower power and lower distortion compared with conventional pipelined ADCs.

Now, if more than one PBS ADC is time-interleaved, the same reference voltages can be shared by all the ADCs, reducing the total power consumption per conversion significantly. Finally, in comparison to asynchronous binary search ADCs, the power-speed trade off is expected to be better than linear.

The main building blocks of the proposed 6-bit fully differential PBS ADC are discussed in the following sections.

A. Dynamic Comparator

Six dynamic comparators are used in the proposed 6-bit PBS ADC. The comparators are clocked just as in the pipelined ADC. In the proposed ADC, comparators are the main source of power dissipation. Hence comparators without

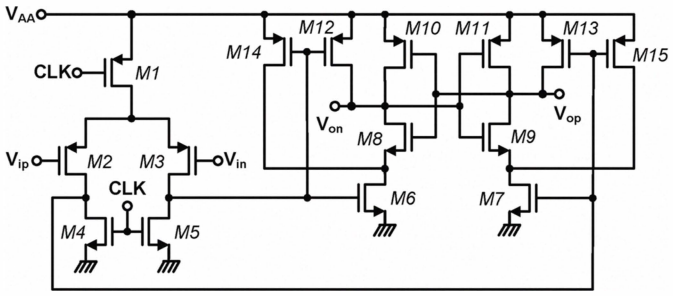

Figure 3. High-speed clocked comparator used in the PBS ADC.

static power consumption were used in the architecture of proposed ADC. Fig.3 shows the dynamic comparators used in the ADC [7]. An SR latch is used at the output of each comparator to keep the outputs constant during one whole period. The use of SR latch along with proper ordering of the inputs to the multiplexers speeds up overall ADC operation. The comparator inputs are connected to common mode voltage during the sampling phase to eliminate the memory effect in the pipelined ADC.

B. Analog Multiplexers

Six analog multiplexers are used in the ADC architecture. As we move from MSB to LSB the complexity of the multiplexers increase. Each 2^n to 1 MUX is consisted of a n to 2n decoder and 2n switches. The n bit control line to each decoder is the delayed outputs of previous comparators. Based on these outputs one of reference voltages from the resistor string is connected to the MUX output.

C. Timing Generator

The ADC timing circuit includes a four stage 1-GHz differential ring VCO, a histogram based phase calibration circuit and eight frequency dividers and non-overlapping clock generators each driven with one of the eight interleaving oscillator phases. The schematic of this timing circuit is shown in Fig.4. The histogram based phase calibration techniques [8, 9] can remove the static phase errors. The calibration tone is generated through another on-chip asynchronous VCO which is powered down following the initial power-up calibration. Since the same comparator pair is switched to all consecutive phase pairs, the offsets and other comparator non-idealities do not contribute to the final phase error.

IV. SIMULATION RESULTS

The proposed 6 bit PSAR ADC was designed in 90nm CMOS process with 1.2V power supply. Simulation results show that the proposed ADC achieves 35.4dB SNDR and 51.2dB SFDR. The core ADC consumes 3.82 mW power from a single 1.2V power supply. The simulated DNL was 0.38/-0.44 LSB and the INL was 0.44/-0.09 LSB as shown in Fig.5. Fig.6 shows the FFT spectrum of differential 1.2Vp-p sine wave input at 102.78MHz. The SFDR is 51.2dB. The proposed ADC achieves 78.3fJ/conversion step. Table I shows the comparison with other state-of-the-art high-speed, low power ADCs [3-7].

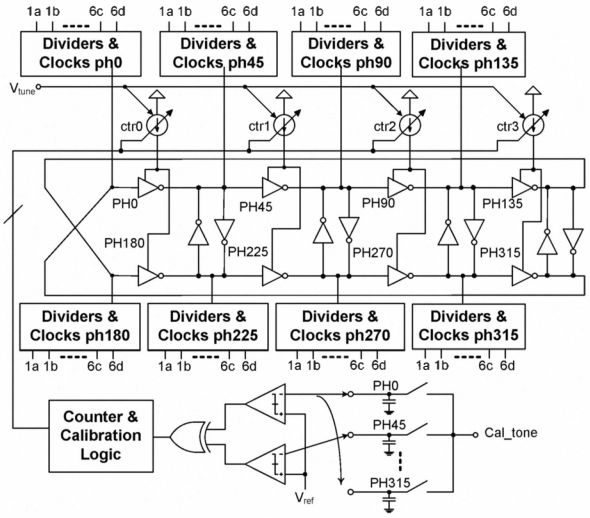

Figure 4. A differential ring-VCO based ADC timing generator.

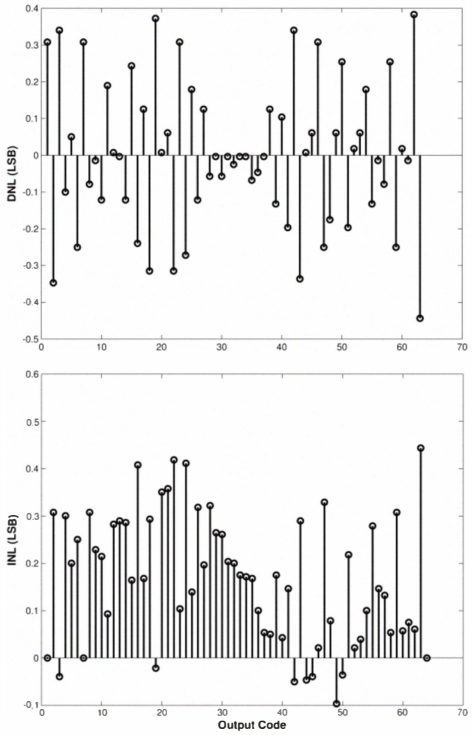

Figure 5. Simulation results. INL and DNL.

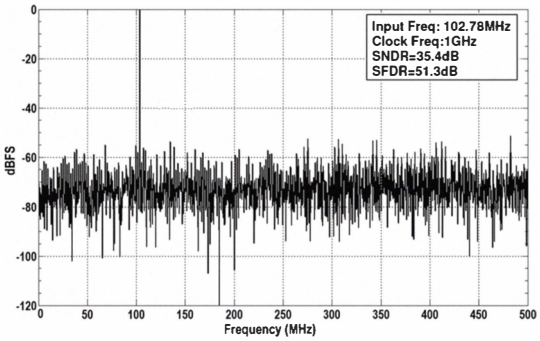

Figure 6. FFT spectrum of 6-bit PBS-ADC for 102.78MHz sinewave input.

TABLE I. PERFORMANCE COMPARISON

Parameters	Ref [3]	Ref [4]	Ref [5]	Ref [6]	Ref [7]	This work
Technology (nm)	130	65	65	65	40	90
Resolution (bits)	6	5	5	6	6	6
Supply (V)	1.2	1.0	1.0	1.2	1.1	1.2
Number of channels	2	1	1	2	4	1
Sampling Rate(MS/s)	600	600	700	1000	2200	1000
SNDR (dB)	34.0	31.6	26.9	31.5	31.6	35.4
Power (mW)	5.30	0.54	1.97	6.27	2.60	3.80
FoM (fJ/conv.code)	220	32	116	210	35	78

V. CONCLUSION

In this paper a new ADC architecture that enables binary search in a pipelined fashion was introduced. Since no opamp is used in the proposed ADC, it consumes lower power and operates at higher speed than conventional pipelined ADCs. Compared to an n bit asynchronous binary search ADCs where the sampling rate is limited by n comparator and n DAC delays, the speed of the proposed PBS ADC however is reduced to total of two comparator and two DAC delays. A 6-bit PBS ADC was designed in 90nm CMOS. The 6-bit design consumes 3.8mW from a 1.2 V supply voltage while operating at 1GS/s, achieving 5.6 ENOB and an energy efficiency of 78.3 fJ/conversion step.

REFERENCES

[1] Y. Zhu, et al. "A 10-bit 100-MS/s Reference-Free SAR ADC in 90 nm CMOS" IEEE JSSC, vol. 45, no. 6, pp. 1111–1121, June 2010.

[2] C. C. Liu, et al., "A 0.92 mW 10-bit 50-MS/s SAR ADC in 0.13 m CMOS process," in Symp. VLSI Circuits Dig. Tech. Papers, pp. 236–237, June 2009.

[3] S.-W. M. Chen and R. W. Brodersen, "A 6-bit 600-MS/s 5.3mW asynchronous ADC in 0.13-µm CMOS," IEEE JSSC, vol. 41, no. 12, pp. 2669-2680, Dec. 2006.

[4] Si-Seng Wong, et al, "A Power Effective 5-bit 600 MS/s Binary-Search ADC with Simplified Switching" in IEEE MWSCAS, pp. 80-81, Aug. 2010.

[5] Ying-Zu Lin, et al."An Asynchronous Binary-Search ADC Architecture With a Reduced Comparator Count" IEEE Tran. on Circuits and Systems I vol 57 pp 1829-1837 Aug. 2010.

[6] Jing Yang, Naing, T.L., Brodersen, R.W,." A 1 GS/s 6 Bit 6.7 mW Successive Approximation ADC Using Asynchronous Processing" in IEEE JSSC, vol. 45, no. 8, pp. 1469–1478, July 2010.

[7] B. Verbruggen, J. Craninckx, M. Kuijk, P. Wambacq, G. Van der Plas, "A 2.6 mW 6 bit 2.2 GS/s Fully Dynamic Pipeline ADC in 40 nm Digital CMOS" IEEE. JSSC, vol.45, no. 10, pp2080 – 2090, Oct. 2010

[8] D. Weinlader, H. Ron, C.-K. K. Yang, M. Horowitz, "An eight channel 35 Gsample/s CMOS timing analyzer," ISSCC Dig. of Tech. Papers, Feb. 2000.

[9] J. Wang, "Techniques for improving timing accuracy of multi-GHz track/hold circuits," Master's Thesis, Oregon State University Nov. 2008.