A 6-GS/s, 6-bit, At-speed Testable ADC and DAC Pair in 0.13μm CMOS

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***Abstract*— This paper demonstrates a 6-GS/s 6-bit flash ADC and current-steering DAC pair in 0.13μm CMOS. Averaging and interpolating techniques are applied to reduce the offsets and to save the power of the ADC. Current mode logics are used to achieve a high speed and to overcome the severe power bouncing issue. Design-for-testability circuits are added to conduct the at-speed tests by internally cascading the ADC and DAC. The cascaded ADC and DAC pair clocked at 6GHz achieves a 37.0 dB signal-to-noise ratio and a 26.0 dBc spurious-free dynamic range with the -1 dBFS, 502 MHz stimulus. The ADC and DAC consumes 655 mW and 115 mW from a 1.2-V supply, respectively.**

***Keywords*: flash ADC, DAC, at-speed tests, GS/s.**

I. Introduction

High speed data converters with a resolution no less than 6 bits are substantial for advanced applications such as software defined radio, UWB, disk read systems, radars, and instruments. In particular, the optical or wired serial links ask for the data converters with a sampling rate and a dynamic range as high as possible, so as to increase the data rate and to reduce the required channel bandwidth.

Conventional ultra-high speed data converters were realized using GaAs or SiGe technology [1], [2]. However, they usually cost several watts. In addition, it is desirable to implement the converters using standard CMOS processes such that we can integrate it with the flexible and powerful digital circuits.

Recently, several very high speed flash CMOS ADC designs have been published [3], [4]. They showed that using 0.13 μm or advanced CMOS technology can achieve a sampling rate higher than 1 GS/s and significantly and reduce the power consumption.

This paper demonstrates a fully integrated, non-interleaved, 6-GS/s, 6-bit ADC and DAC pair in 0.13 μm CMOS. Sec. II describes the circuit design and indicates the design challenges. We applied the interpolation and averaging techniques, wave-pipeline concept, and the current mode logic circuits to the design to make the data converters low-power, very fast, and having less noise. A test chip has been designed and fabricated. Sec. III shows the measurement results. Finally, we draw our conclusions in Sec. IV.

II. Circuit Description

Fig. 1 depicts the simplified block diagram of the test chip. The flash type ADC and the current steering type DAC are the record holders of the highest sampling rate data converters up to date. Therefore, we adopted the flash and the current-steering architectures for the ADC and DAC, respectively to achieve the 6-GS/s sampling rate. In addition, a design-for-testability block for at-speed tests was added to our design to address the difficulty in testing. All circuits including the analog and logic parts are realized using fully-differential structures to alleviate the common-mode interference and noise. The differential input range of the ADC and the differential output range of the DAC are all set to ± 400 mV.

A. ADC

The ADC comprises a track and hold (T/H) circuit, a resistor ladder, a Gilbert cell array, three averaging-and-interpolating pre-amplification (PreAmp) stages, and the following digital blocks as shown in Fig. 1.

The major design issues for the ADC are the non-zero offsets of the comparators and the possibly too high power. To address both issues, we used the averaging and interpolating techniques. In addition, the averaging termination method proposed by [5] was adopted to reduce the number of the over-range amplifiers and thus the total power.

The Gilbert cell array in Fig. 1 contains eleven Gilbert cells including two dummy ones. Each of them accepts the corresponding differential reference voltages generated by the resistor ladder and the differential output of the T/H circuit, and amplifies the difference between the two differential inputs. A resistive network is followed to average the outputs of the Gilbert cells and to interpolate the outputs by a factor of two.

The following three PreAmp stages ensure that the final current mode logic (CML) latches can resolve the correct digital outputs. They also employ resistive networks for averaging and interpolating their outputs by the same factor of two as shown in Fig. 2. Each of the amplifiers in the PreAmp stages has the same active-feedback configuration to extend their bandwidths [6]. Given the same power and gain constraints, the active-feedback amplifier can achieve a wider bandwidth than the conventional differential amplifier [6].

The OR array accepts the thermometer coded outputs of the latch array to eliminate the possible single-bubble errors. The thermometer-to-Gray encoder encodes the outputs of the OR array to produce the final 6-bit Gray-coded outputs. Using the Gray codes instead of traditional binary codes has the advantage of being more insensitive to the meta-stability of the comparators.

One of the major challenges in the design is to make the logic operation fast and quiet. Standard CMOS logic

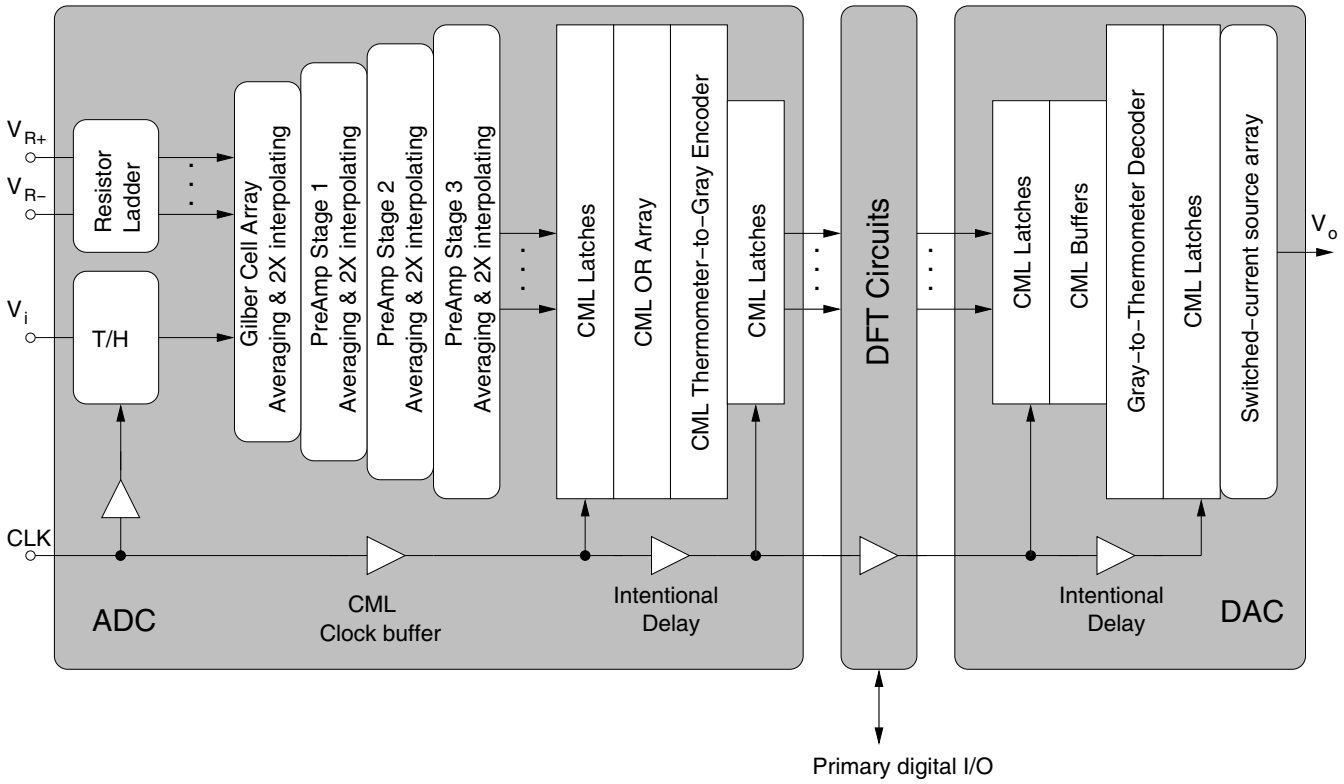

Fig. 1. Block diagram of the test chip.

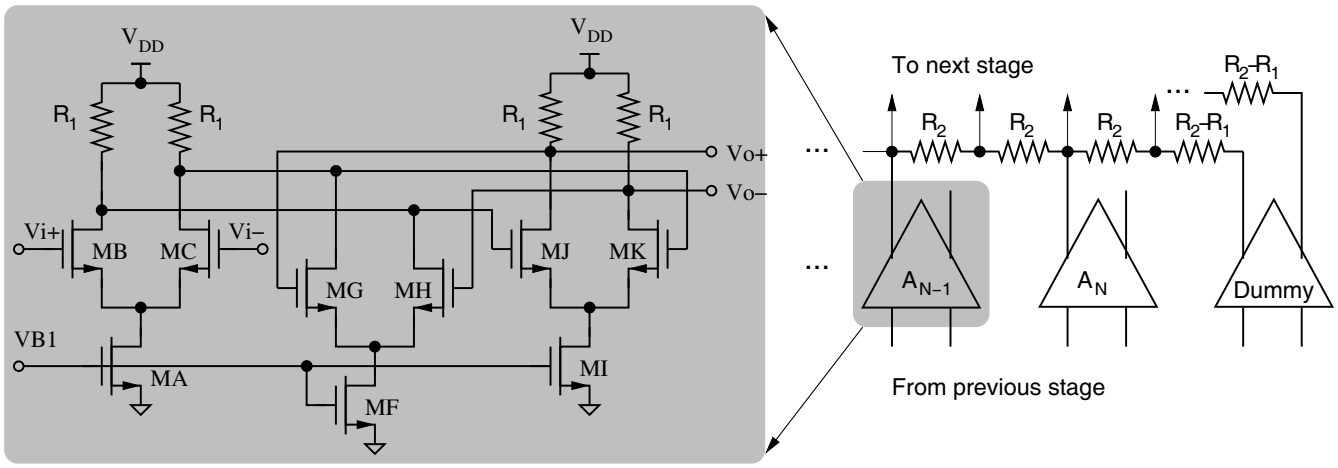

Fig. 2. Simplified schematic of the PreAmp stages.

gates will generate huge switching noise on the power rails. They also consume very large power when operating at 6-GHz because of their rail-to-rail input/output (I/O) swings. To address these issues, we used The CML family proposed in [7] to implement the logic blocks. The CML gates achieve faster logic switching since a small differential input voltage is sufficient to completely steer the tail current of the differential pair from one side to the other. They also consume less power when operating at 6-GHz because their I/O swings are not rail-to-rail. Besides, the constant tail current sources of the CML gates make the power bouncing much less significant.

Even with the CML circuits, the critical delay of the logic parts of the ADC is still over an half of the clock period. Therefore, the wave-pipelining technique [8] was used to address this issue. As shown in Fig. 1, the intentional clock buffers were added to gain some extra timing margins such that the logic outputs can be correctly latched.

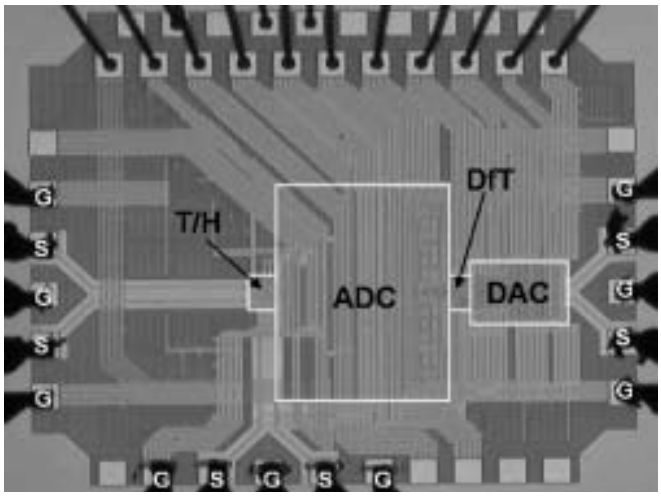

Fig. 3. Microphotograph of the test chip.

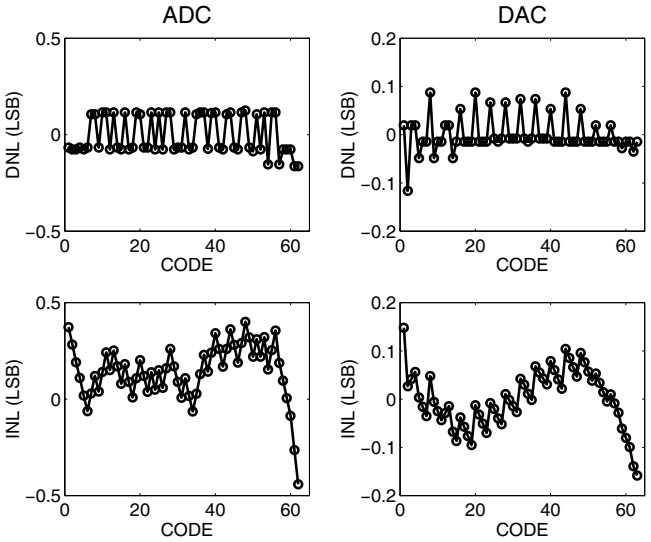

Fig. 4. Measured INL and DNL plots of the ADC and DAC.

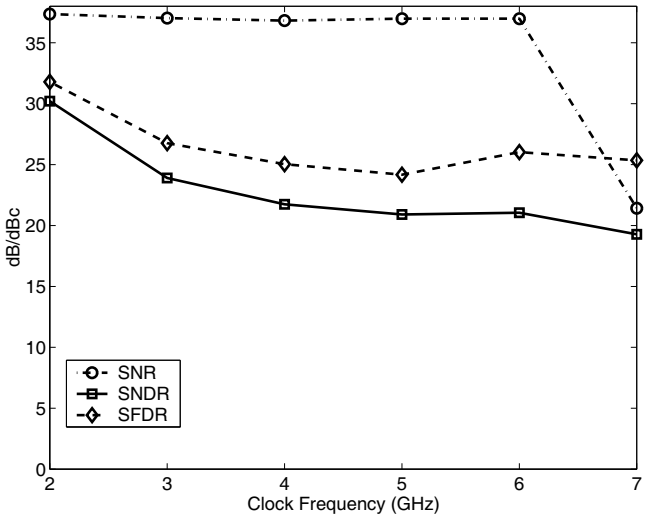

Fig. 5. Measured dynamic performance vs. sampling rate in the test mode C.

B. DAC

Refer to Fig. 1, the DAC is a conventional current-steering DAC. It composes of a hybrid Gary-to-thermometer decoder followed by the switched current source (SCS) array. In order to reduce the design area and complexity, the hybrid Gary-to-thermometer decoder is composed of a 4-bit MSB part and a 2-bit LSB part. The MSB part has a thermal-meter-decoded structure, while the LSB part has a binary-weighted one. The CML latches were inserted before every SCS cells to make sure that all SCS cells are simultaneously switched.

Similar to the ADC design, the wave-pipelining technique by adding some intentional delays on the clock path was also used to compensate for the too long critical delay of the DAC's logic parts.

C. Design-for-at-speed-Testability

Due to the lack of the logic analyzer and pattern generator that can operate at 6-GS/s, the design-for-testability (DfT) block shown in Fig. 1 was added to provide the test chip with three test modes including A, B, and C. In the test mode C, the ADC internally cascades the DAC. This test mode uses the digital loop-back technique to conduct the at-speed dynamic tests. We can measure the dynamic performance of the data converter pair using an analog signal generator and an analog spectrum analyzer.

On the other hand, the test modes A and B are used to measure the static parameters of the ADC and DAC, respectively.

III. Measurement Results

The ADC and DAC pair with the DfT function has been designed and fabricated in a 0.13μm CMOS process. Fig. 3 shows the micrograph of the test chip. The active areas of the ADC and DAC are 0.392 and 0.056 mm^2, respectively. The test chip occupies 2.31 mm^2. The test chip was directly mounted onto the print circuit board for measurement.

Fig. 4 shows the measured static parameters of the ADC and DAC. The measured DNL and INL of the ADC are -0.16 to 0.13 LSB and -0.44 to 0.4 LSB respectively, while the DAC has a DNL within -0.12 to 0.09 LSB and an INL within -0.16 to 0.15 LSB.

Fig. 5 depicts the measured SNR, SNDR, and SFDR values with the -1 dBFS, 502 MHz sinusoidal stimulus in the test mode C. It shows that the data converter pair can operate at 6-GS/s. The measured output spectrum of the test chip is shown in Fig. 6. The data converter pair achieves an SNR, SNDR, and SFDR of 37 dB, 21.2 dB, and 26.0 dBc, respectively. Fig. 7 shows the measured SNR and SFDR vs. different stimulus frequency. The -3 dB bandwidth of the data converter pair's SNR is around 2 GHz.

Table I lists the performance summary of the test chip and

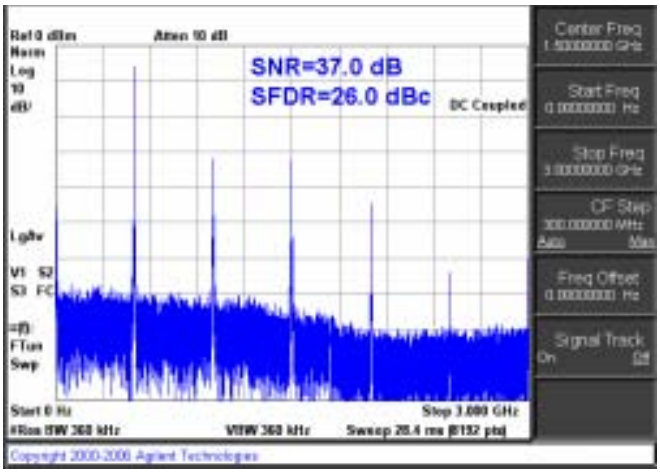

Fig. 6. Output spectrum of the test chip in the test mode C at 6-GS/s. The stimulus is a -1 dBFS, 502 MHz sinusoidal wave.

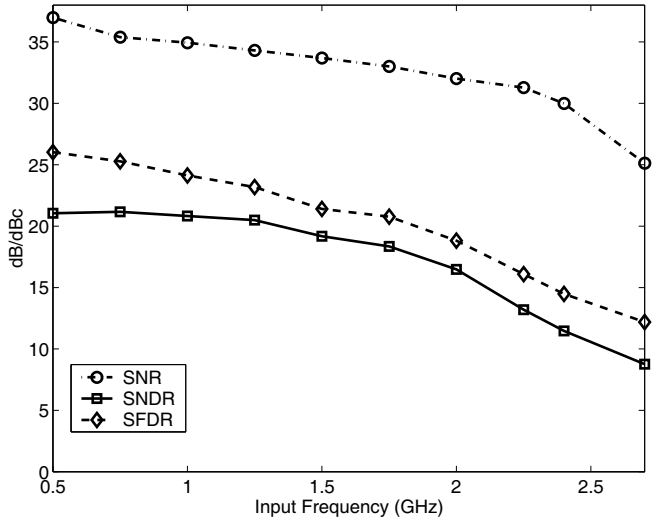

Fig. 7. Measured dynamic performance vs. stimulus frequency in the test mode C at 6-GS/s.

compares the results with those of the published works. Our design achieves the best DNL and INL among the three works, showing that the averaging and interpolating resistor networks do help. The SNDR and SFDR of the data converter pair is primarily limited by the harmonic distortion. The harmonics are less either when the clock rate is less or when the stimulus frequency is low. It seems that the stimulus inter-modulates itself because of some capacitive coupling paths. It will be our future work to address this issue.

IV. Conclusion

We demonstrate a 6-GS/s 6-bit flash ADC and current-steering DAC pair in 0.13μm CMOS. Averaging and interpolating techniques are applied to reduce the offsets and to save the power of the ADC. We applied current mode logics to achieve a high sampling rate and to overcome the severe power bouncing issue. In addition, the design-for-testability

TABLE I

PERFORMANCE SUMMARY AND COMPARISON

Sources	[3]	[4]	This work	
Process	90nm CMOS	130nm CMOS	130nm CMOS	
V_{DD}	0.9V	1.5V	1.2V	
Design	ADC	ADC	ADC	DAC
Active area	0.15 mm^2	0.50 mm^2	0.392 mm^2	0.056 mm^2
f_s	3.5-GS/s	4-GS/s	6-GS/s	
Resolution	6 bits	6 bits	6 bits	
DNL(LSB)	$-0.49/0.50$	$-0.23/0.91$	$-0.16/0.13$	$-0.12/0.09$
INL(LSB)	$-0.39/0.96$	$-0.98/1.20$	$-0.44/0.40$	$-0.16/0.15$
SNR	>31.18 dB	N/A	37.0 dB*	
SFDR	>38.67 dBc	31.18 dBc	26.0 dBc*	
Power	98 mW	990 mW	655 mW	115 mW

*Measured SNR @f_{in}=502MHz in the test mode C.

circuits are added to conduct the at-speed tests by digital loop back. The cascaded ADC and DAC pair clocked at 6-GHz achieves a 37.0 dB SNR, a 26.0 dBc SFDR, and a 21.2 dB SNDR with the -1 dBFS, 502 MHz stimulus. The ADC and DAC consumes 655 mW and 115 mW from a 1.2-V supply, respectively.

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