A 12-GS/s 81-mW 5-bit Time-Interleaved Flash ADC with Background Timing Skew Calibration

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Abstract

A 12-GS/s 5-bit time-interleaved flash ADC is realized in 65-nm CMOS. The design utilizes a background timing skew calibration technique to improve dynamic performance, and comparator offset calibration to reduce power dissipation. The experimental prototype achieves an SNDR of 25.1 dB at Nyquist and 27.5 dB for low frequency inputs. The circuit occupies an active area of 0.44 mm^2 and consumes 81 mW from a 1.1-V supply.

Keywords: A/D conversion, time-interleaving, calibration

Introduction

High-data-rate, DSP-based SerDes receivers rely on high-speed ADCs for baud rate digitization, typically requiring ~5 bits of resolution and sampling rates above 10 GS/s [1]. The time-interleaved flash-ADC proposed herein was designed to meet these requirements with low power dissipation through a parallel consideration of circuits, architecture and algorithms. First, each flash sub-ADC is built using offset calibrated dynamic comparators that employ near minimum size transistors. This reduces power in the active circuitry, as well as in the resistive reference ladder, which can be designed for higher impedance due to reduced kickback charge. Second, the architecture is 8-fold time interleaved, so that each sub-ADC runs at a clock rate that is relatively slow for the given 65-nm technology. This helps improve the power efficiency of the constituent circuitry.

A well-known challenge with high degrees of interleaving is the proper management of channel mismatches in offset, gain and sampling clock timing. For our specific design, clock timing is the most significant issue. Detailed analysis shows that for our target specs, the standard deviation in the timing skew must be less than 700 fs, which is difficult to achieve without calibration. In order to address this issue, our converter employs a background timing skew calibration technique.

Timing Skew Calibration

Fig. 1 shows the block diagram of the proposed ADC. The auxiliary comparator samples the input with a clock ϕ_{cal} whose edges periodically coincide with the ideal sampling instances for the sub-ADC clocks ϕ_1-ϕ_8, thus creating a timing reference grid. Any errors in the ADC sampling instances are minimized through a correlation-based algorithm. Digitally adjustable delay cells are iteratively tuned until the correlation of the auxiliary comparator output with each channel is maximized, forcing the sampling instances to approach their ideal locations. Since the auxiliary comparator lies outside the main signal path, its decision time need not be fast, and ϕ_{cal} can tolerate moderate amounts of random jitter that is subsequently filtered out by the algorithm. In a SoC environment where a full-speed clock is available, ϕ_{cal} can be generated using edge gating; else, a fractional clock multiplier can be used.

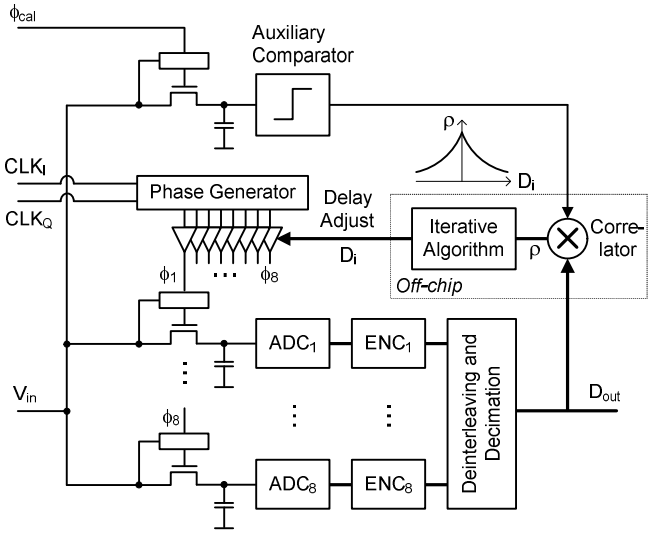

Fig. 1. ADC architecture.

Circuit Implementation

For simplicity in this prototype, ϕ_1-ϕ_8 are created by an on-chip phase generator that takes differential quadrature clocks from an off-chip balun. The delay cells consist of cascaded inverters, loaded by a programmable 7-bit MOS capacitor bank [2]. The bank is segmented (5 binary bits) and sized for tuning in 250 fs steps. Each sub-ADC is preceded by a passive, bootstrapped track-and-hold circuit. The thermometer outputs of each ADC are converted to a straight binary format using Wallace encoders and are subsequently decimated by a factor of 81. Each sub-ADC contains 31 dynamic comparators whose offsets are digitally tunable [3] through a 5-bit, segmented calibration DAC (see Fig. 2).

The clocked transistors labeled MC are included to minimize kickback [4]. Transistor MT is sized deliberately small to reduce the input referred offset. The lower bound on the size of MT is set by the sub-ADC clock rate, which is significantly reduced due to interleaving. The calibration DAC settings for each comparator are determined at start-up by shorting the inputs to the references and adjusting the trim code until the comparator toggles. Once calibrated, the offsets do not drift significantly relative to the LSB size of this converter (19 mV). For instance, any change in mobility due to temperature affects the input and calibration transistors alike, leading to acceptable temperature dependence.

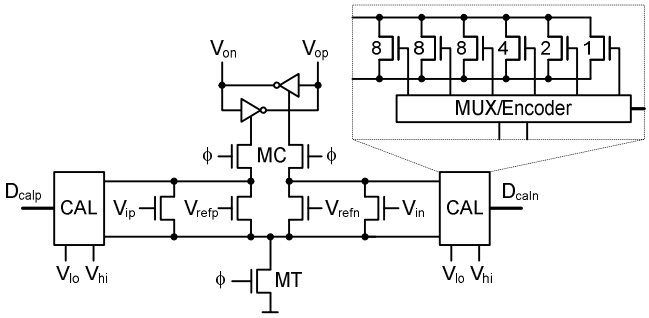

Fig. 2. Comparator schematic (reset transistors are not shown).

Measurement Results

Fig. 3 shows the measured SNDR during the initial convergence of the timing skew background calibration algorithm. This measurement is performed after the start-up calibration of the sub-ADC comparator offsets has been completed. The timing skew calibration improves the SNDR by approximately 12 dB. Fig. 4 shows a typical (decimated) output spectrum with and without timing skew calibration. The spurs due to timing skew are reduced by 10–30 dB and the remaining dominant spur in Fig. 4(b) is third order harmonic distortion (at -30.3 dB). Fig. 5 shows the SNDR of the converter versus input frequency. Without timing skew calibration, the performance degrades rapidly with f_{in}. With the skew calibration activated, the SNDR remains relatively flat, achieving SNDR = 23.8 dB at f_{in} = 8 GHz, and the ADC performance is no longer limited by timing-skew. The measured DNL and INL of the sub-ADCs decreases from approximately 2 LSB before start-up offset calibration to less than 0.5 LSB thereafter.

Fig. 6 shows a die micrograph of the proof-of-concept ADC, which has a total area of 1.3 mm^2 and an active area of 0.44 mm^2 in 65 nm CMOS technology. The power dissipation is 81 mW from a 1.1-V supply (excluding I/O, off-chip correlator/algorithm, and input clock buffers). For low input frequencies, the corresponding FOM = $P/(f_s \cdot 2^{ENOB})$ is 0.35 pJ/conversion-step. This number modifies to 0.46 pJ/conversion-step near Nyquist. This power efficiency compares favorably with that of most competing designs (operating at multi-GS/s speed) published to date.

Acknowledgements

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References

[1] M. Harwood, N. Warke, R. Simpson, et al., "A 12.5Gb/s SerDes in 65nm CMOS Using a Baud-Rate ADC with Digital Receiver Equalization and Clock Recovery," *ISSCC Dig. Tech. Papers*, pp. 436-437, Feb. 2007.

[2] K. Poulton, R. Neff, B. Setterberg, et al., "A 20 GS/s 8 b ADC with a 1 MB memory in 0.18 µm CMOS," *ISSCC Dig. Tech. Papers*, pp. 318-319, Feb. 2003.

[3] K.-L.J. Wong and C.-K.K. Yang, "Offset compensation in comparators with minimum input-referred supply noise," *IEEE J. Solid-State Circuits*, pp. 837-840, May 2004.

[4] T. Sundström and A. Alvandpour, "A kick-back reduced comparator for a 4-6-bit 3-GS/s flash ADC in a 90nm CMOS process," *Proc. MIXDES*, pp. 195-198, Jun. 2007.

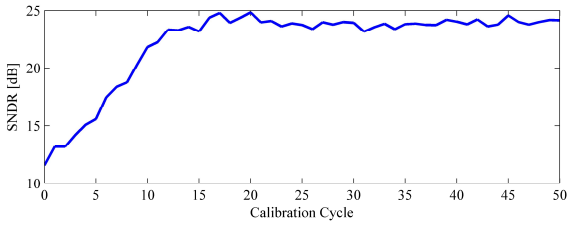

Fig. 3. Measured SNDR during convergence of timing skew calibration (f_{in} = 8 GHz and f_s = 12 GHz). The duration of each calibration cycle is 8 ms.

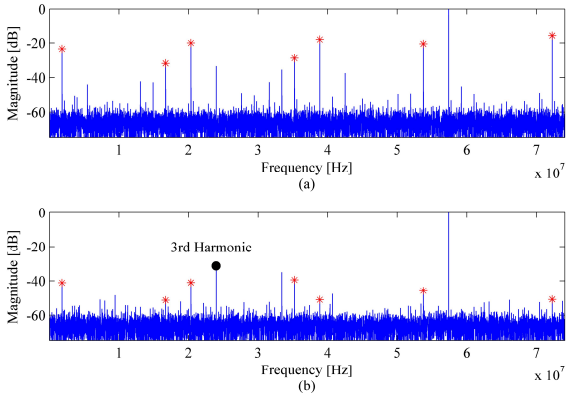

Fig. 4. Measured spectrum of the decimated output (f_{in} = 8 GHz and f_s = 12 GHz). (a) With timing skew calibration, and (b) without. The fundamental spurs due to timing-skew are marked (*).

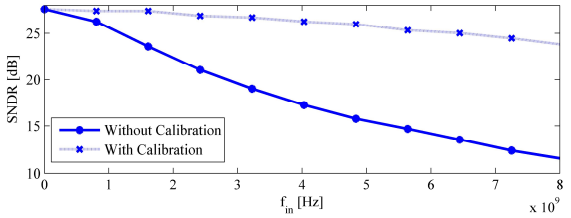

Fig. 5. Measured SNDR versus input frequency at f_s = 12 GHz.

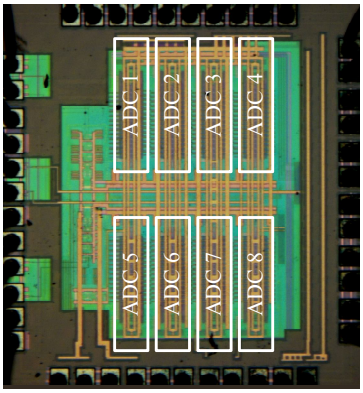

Fig. 6. Die micrograph.