A 6-bit 3.5-GS/s 0.9-V 98-mW Flash ADC in 90-nm CMOS

Kazuaki Deguchi, Naoko Suwa, Masao Ito, Toshio Kumamoto, and Takahiro Miki, *Senior Member, IEEE*

***Abstract*—A 6-bit 3.5-GS/s flash ADC is reported. A load circuit with a clamp diode and a replica-biasing scheme is developed for low-voltage and high-speed operation. An acceleration capacitor is introduced for high-speed overdrive recovery of a comparator. An averaging and interpolation network is employed in this ADC. The interpolation factor is optimized considering random offset, active area, and systematic offset to realize low offset and small active area. The ADC is fabricated in a 90-nm CMOS process and occupies 0.15 mm^2. It consumes 98 mW with a 0.9-V power supply. With Nyquist input, SNDR and SFDR at 3.5 GS/s are 31.18 dB and 38.67 dB, respectively.**

***Index Terms*—A/D converter, active load, ADC, flash converter, interpolation, offset averaging, overdrive recovery.**

I. Introduction

THE demand for high-speed ADCs continues to increase in various fields including disk systems and UWB communication systems. Recent high-density disk drive systems require an ADC with more than a 2-GS/s sampling rate and 6-b resolution or better. An attractive way to realize a power-efficient high-speed ADC is to interleave successive approximation ADCs [1], [2]. However, the interleaved successive approximation ADCs reported so far have not achieved such a high sampling rate. The sampling rate can be improved by interleaving flash ADCs [3]. However, using multiple flash ADCs results in large area or large power consumption. Non-interleaved ADCs with foreground calibration have also achieved the above sampling rate [4], [5]. However, foreground calibration requires a calibration period that imposes severe restrictions on system design and narrows application fields.

This paper describes a 6-b 3.5-GS/s 98-mW ADC with flash architecture without interleaving or calibration[6]. Since a fine process is mandatory to realize such a high-speed low-power ADC, we use a 90-nm CMOS process. To overcome the problem caused by the low-supply voltage of this process, a load circuit with a clamp diode and replica biasing is developed for a preamplifier and a first-stage comparator. A comparator with fast overdrive recovery is required to realize an ADC with high input bandwidth. In this ADC, an acceleration capacitor employed in the first-stage comparator realizes fast over drive recovery and achieves an SNDR of 31 dB at 3.5-GS/s with Nyquist input frequency. In addition, an averaging and interpolation technique is employed. The interpolation factor is optimized considering random offset, systematic offset, and active area to realize low offset and small active area.

In Section II of this paper, the architecture of this ADC is presented, and its major building blocks are discussed in Section III. In Section IV, optimization of the interpolation factor is discussed. Experimental results of this ADC are shown in Section V. In Section VI, its performances are compared with other 6-bit high-speed ADCs, and a conclusion is given.

II. Architecture

The architecture of the ADC is shown in Fig. 1. It has a track-and-hold circuit, 4-input preamplifiers, first-stage comparators, second-stage comparators, SR-latches, and a digital encoder. The track-and-hold circuit improves dynamic performance [7], [8]. By holding the input analog signal during quantization, the track-and-hold circuit reduces errors due to skews in the clock and in the input signal distributed to the multiple preamplifiers. In this ADC, the track-and-hold circuit with a pseudo-differential configuration [8] is employed as shown in Fig. 2. In order to reduce back-gate modulation, the back-gate nodes of transistors M01 and M02 are connected to their sources. The back-gate nodes of the other transistors are connected to the rails. The preamplifier array shown in Fig. 1 amplifies the difference between the differential input signal and the reference voltage. This preamplifier array is followed by a 4-time resistive interpolation network that also acts as the first averaging network. The next stage is the array of the first-stage comparator. To ensure fast overdrive recovery, the comparator must have small size transistors. However, they have large device mismatches. Another resistive averaging network is introduced to the first-stage comparator array [8] to reduce the random offsets caused by the device mismatch. A proper number of dummies is added to the first-stage comparator array to avoid the edge effect of the averaging network. The total number of preamplifiers and first-stage comparators including dummies are 19 and 75, respectively. To decrease the bit error rate, two more regeneration stages are added, the second-stage comparator and the SR latch shown in Fig. 1. The second-stage comparator provides rail-to-rail logic swing for the SR latch. The digital encoder consists of two-input NAND gates, a ROM-based quasi-Gray encoder, and a quasi-Gray-to-binary converter [9].

III. Circuit Description

A. Preamplifier for Low-Voltage and High-Speed Operation

Fig. 3 shows the preamplifier circuit used in this ADC. To receive differential signals, this preamplifier has two differential pairs. The pMOS switch M4 connected between the differential outputs moderates the bandwidth requirements [8]. Low-Vth

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The authors are with the Advanced Analog Technology Division, Renesas Technology Corporation, Itami, Hyogo 664-0005, Japan (e-mail: deguchi.kazuaki@renesas.com).

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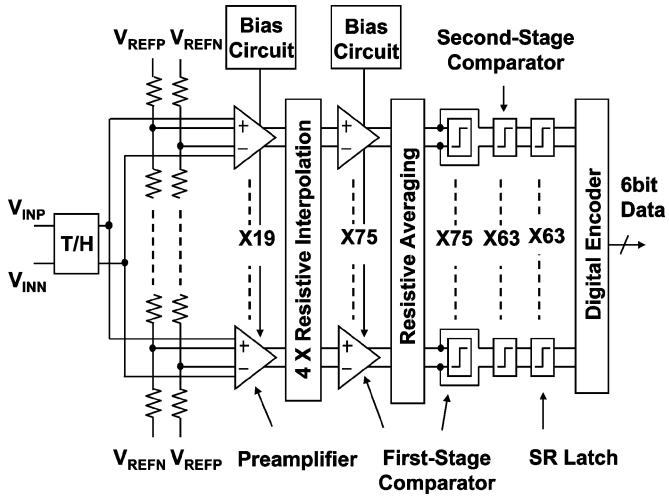

Fig. 1. Block diagram of ADC.

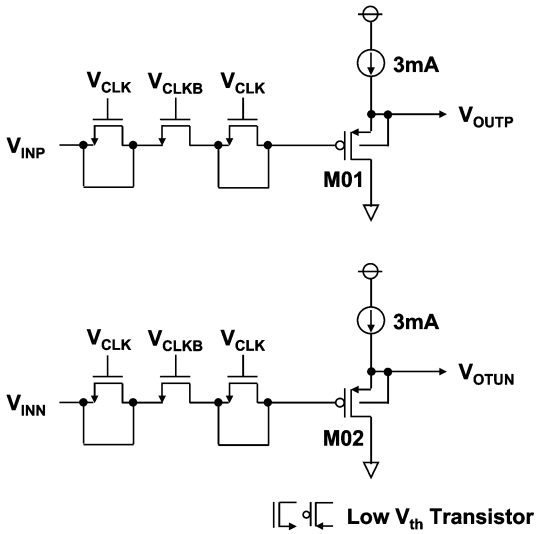

Fig. 2. Track-and-hold circuit.

transistors are used in the differential pairs to increase the input range. To minimize the channel resistance of the reset switch M4, a low-Vth transistor is also introduced.

In a conventional preamplifier, a diode-connected transistor is used as a load resistor [8], [10], [11]. However, this configuration lowers output common-mode voltage by Vth, which is problematic in low-voltage operation because the voltage headroom for the differential pair and the tail current in the preamplifier and for the tail current in the first-stage latch are significantly reduced. In this preamplifier, M1 is operated in the linear region and acts as a load resistor. Diode-connected transistor M3 acts as a clamp diode and suppresses the overswing of the output voltage. The preamplifier replica circuit sets the output common voltage near the rail to gain sufficient voltage headroom. This biasing scheme turns off transistor M3 when the output is balanced. Thus M3 neither disturbs small-signal amplification nor adds its gate capacitance to the load. Unlike a CMFB used in a high-gain operational amplifier, this circuit is not necessary in each preamplifier, because M1 biased in the

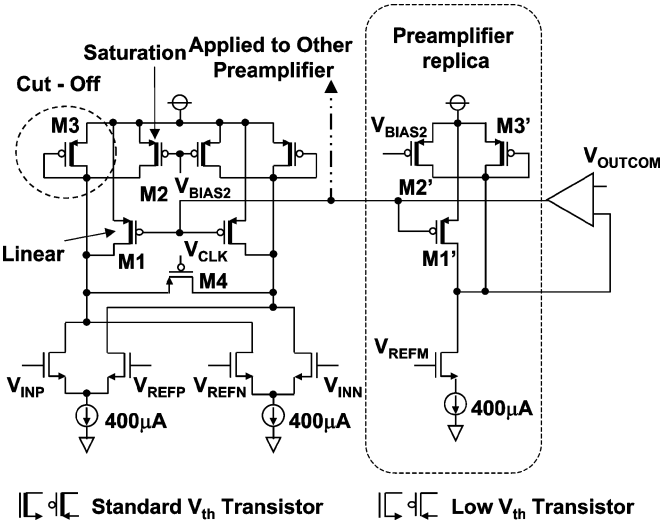

Fig. 3. Preamplifier circuit.

linear region lowers the common-mode gain of the preamplifier. Therefore its area and power consumption penalties are very small. Transistor M2, operated in the saturation region, is added and bypasses the current from the differential pair and enables independent optimization of the tail current, the load resistance, and the common-mode output voltage. This load circuit with the clamp diode and the replica-biasing scheme contributes to low-voltage and high-speed operation. The same technique is introduced into the load of the first-stage comparator.

B. First-Stage Comparator for Fast Overdrive Recovery

Fig. 4 shows the first-stage comparator used in this ADC. It consists of an input differential pair and a latch that share a load circuit with the same topology as the preamplifier described in the previous section. In the amplification phase, $V_{\rm CLK}$ is high and $V_{\rm CLKB}$ is low, and the differential pair is activated. The gain of the first-stage comparator during the amplification phase is dominated by the channel resistance of M6. When the latch phase starts, $V_{\rm CLK}$ becomes low and $V_{\rm CLKB}$ becomes high. This activates the latch, and regeneration starts based on the final output in the amplification phase.

The overdrive recovery acceleration capacitor shown in Fig. 4 is introduced to achieve fast overdrive recovery. In the following description of this capacitor's function, we assume that the preamplifier input is a large positive voltage in an amplification phase and changes to a small negative one in the following latch phase. When the next amplification phase starts, transistor M6 turns on, and $V_{\rm outp}$ swings downward from a high level. This injects a negative charge to the comparator input through acceleration capacitor C and accelerates the comparator input settling to a negative value. This topology has also been employed in a conventional ADC to cancel kickback [11]. In this comparator, however, more charge than that is injected to accelerate the overdrive recovery.

Note that excessive injection causes undesirable undershoot when the input changes from a large positive voltage to a small positive one, and this could result in incorrect results. Therefore, the acceleration capacitor for the charge injection must

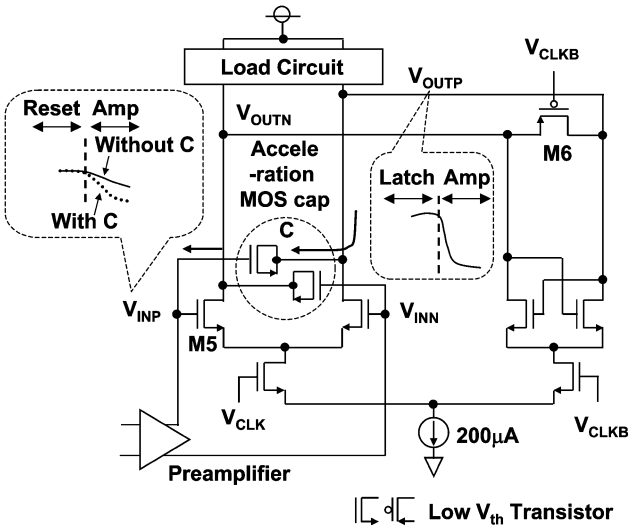

Fig. 4. First-stage comparator circuit.

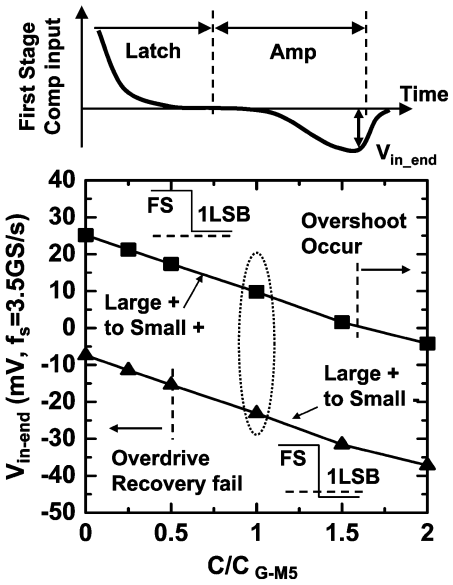

Fig. 5. Simulation result of overdrive recovery.

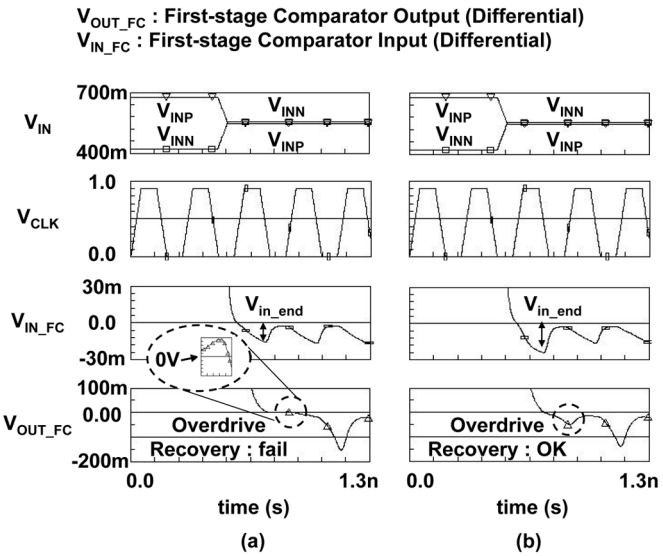

Fig. 6. Simulation waveform of overdrive recovery. (a) $C/C_{\mathrm{GM\_5}} = 0.5$. (b) $C/C_{\mathrm{GM\_5}} = 1.0$.

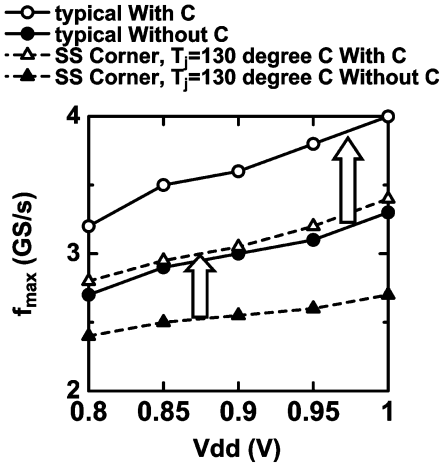

Fig. 7. Simulation result of maximum operating frequency of comparator.

be optimized. Comparator input voltage at the end of an amplification period $V_{\mathrm{in\_end}}$ is simulated. The summary of overdrive recovery simulation results is shown in Fig. 5. The y axis shows $V_{\mathrm{in\_end}}$, and the x axis shows the ratio of acceleration capacitor C to the gate capacitance of comparator input transistor M5 ($C/C_{\mathrm{G\_M5}}$). The lower curve shows $V_{\mathrm{in\_end}}$ when the preamplifier input changes from large positive to small negative voltage. When the capacitor ratio is less than 0.5, the comparator overdrive recovery fails. This is confirmed by more detailed simulation. Fig. 6(a) and (b) show waveforms at $C/C_{\mathrm{G\_M5}} = 0.5$ and 1.0, respectively. When $C/C_{\mathrm{G\_M5}} = 0.5$, the comparator output in regeneration period ($V_{\mathrm{CLK}} = \mathrm{L}$) has incorrect polarity although $V_{\mathrm{in\_end}}$ has correct polarity. However, when $C/C_{\mathrm{G\_M5}} = 1.0$, the polarity of the comparator output in regeneration period becomes correct as shown in Fig. 6(b). The upper curve in Fig. 5 shows $V_{\mathrm{in\_end}}$ when the preamplifier input changes from large positive to small positive voltage. Undesirable overshoot occurs when the capacitor ratio is more than 1.6. Considering these trade-offs, $C/C_{\mathrm{G\_M5}} = 1$ is chosen for this ADC. Fig. 7 compares the maximum operating frequency of the comparator with and without the acceleration capacitor. The plot includes the results in worst case (slow-slow corner and $T_j = 130$ degree C). This technique improves the operating frequency by 0.5–1 GS/s not only in the typical condition but also in the worst condition.

IV. Optimization of Averaging and Interpolation Network

In this section, the optimization of the interpolation factor is discussed. First, random offset at the output of the averaging and interpolation network is analyzed with various interpolation factors. Second, the dependence of the total area of the preamplifier array on interpolation factors is estimated. Finally, the effect of interpolation factors on systematic offset is investigated.

A. Analysis of Random Offset

Fig. 8(a) shows the preamplifier array with the averaging network. A single-ended circuit is shown for simplicity. To secure

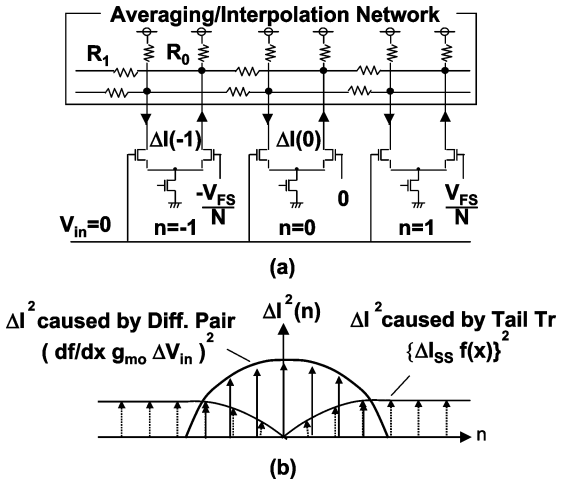

Fig. 8. Model for analysis of random offset. (a) Preamplifier with averaging/interpolation network. (b) Error current injected into averaging/interpolation network.

reasonable signal range in low-voltage operation, the overdrive voltage of the tail current as well as the differential pair must be reduced. However, this makes the tail current sensitive to the Vth mismatch. In this paper, random offsets, caused not only by the differential-pair mismatch but also by the tail-current mismatch, are analyzed. The analysis of random offsets is started by creating a model of error current injected into the averaging network.

Assuming the reference voltage applied to the preamplifier in the center of Fig. 8(a) is zero, the drain current of the nth differential pair $I(n)$ is obtained from the square law of MOS drain current as

$$I(n) = I_{ss} f(x) \tag{1}$$

$$f(x) \equiv \begin{cases} 1 & (x \geq \sqrt{2}) \\ x\sqrt{1-\frac{x^2}{4}} & (|x| < \sqrt{2}) \\ -1 & (x \leq -\sqrt{2}) \end{cases} \tag{2}$$

$$x = \frac{V_{\rm in} - \frac{nV_{FS}}{N}}{V_{ov0}} \tag{3}$$

where I_{SS}, $V_{\rm in}$, V_{FS}, N, and V_{ov0} are the tail current, an input voltage to the preamplifier array, the full scale voltage, the number of preamplifiers excluding dummies, and the overdrive voltage of the differential pair, respectively. Error current $\Delta I(n)$ injected into the averaging network is given by

$$\begin{aligned} \Delta I^2(n) &= \left(\frac{\partial I}{\partial V_{\rm in}}\Delta V_{\rm in}\right)^2 + \left(\frac{\partial I}{\partial I_{ss}}\Delta I_{ss}\right)^2 \\ &= \left(\frac{df}{dx}\right)^2 g_{m0}^2 \Delta V_{\rm in}^2 + f^2(x)\Delta I_{SS}^2 \end{aligned} \tag{4}$$

where g_{m0} is the transconductor of the differential pair at the balanced input and given by I_{ss}/V_{ov0}. Parameters ΔI_{SS} and $\Delta V_{\rm in}$ are the tail-current mismatch and input-equivalent offset of the differential pair before averaging, respectively. The first and second terms in (4) are the error currents caused by differential-pair and tail-current mismatches, respectively. If the input of the preamplifier located in the center is balanced ($V_{\rm in} = 0$), the error current caused by the differential pair has maximum value, while the tail-current mismatch does not cause error current as shown in Fig. 8(b). On the other hand, in the preamplifier far from the center, one of the differential-pair transistors is completely cut-off. In such a preamplifier, the differential-pair mismatch does not cause error current, while the error current caused by the tail-current mismatch has maximum value. Assuming η is the ratio of the tail-current mismatch to the drain-current mismatch of the differential pair, (4) results in

$$\Delta I^2(n) = \left\{ \left(\frac{df}{dx}\right)^2 + f^2(x)\eta^2 \right\} g_{m0}^2 \Delta V_{\rm in}^2. \tag{5}$$

If the current mismatch caused by $\Delta\beta/\beta$ is negligibly smaller than that caused by ΔV_{th}, η is approximated as

$$\begin{aligned} \eta^2 \equiv \left(\frac{\Delta I_{ss}}{g_{m0}\Delta V_{\rm in}}\right)^2 &= 4\left(\frac{S_d}{S_{SS}}\right) \cdot \left(\frac{A_\beta^2 + \frac{4 \cdot A_{V_{th}}^2}{V_{ovSS}^2}}{A_\beta^2 + \frac{4 \cdot A_{V_{th}}^2}{V_{ov0}^2}}\right) \\ &\cong 4\left(\frac{S_d}{S_{SS}}\right) \cdot \left(\frac{V_{ov0}}{V_{ovSS}}\right)^2 \end{aligned} \tag{6}$$

where A_β and A_{Vth} are the matching coefficients for $\Delta\beta/\beta$ and ΔV_{th},respectively. The parameters V_{ovSS} and (S_d/S_{SS}) are the overdrive voltage of the tail-current transistor and the ratio of the gate area of the differential-pair transistor to the tail-current transistor, respectively.

Once the model of stimulus is created, a random offset at the output of the averaging network can be calculated based on [12]. Briefly, the error currents shown in Fig. 8(b) propagate to the output node of the center preamplifier being attenuated by the averaging network. The random offset at the output node of the center amplifier is obtained from the sum of the square of these currents when $V_{\rm in} = 0$. In this analysis, the calculation of the random offset is carried out assuming that the total gate area of the preamplifiers including the dummy preamplifiers is constant. This assumption results in that $1/\Delta V_{\rm in}^2$, S_d, and S_{ss} are proportional to $\alpha N/(N+D)$, where D is the necessary and sufficient number of dummies to suppress the error caused by the edge effect less than a certain value obtained by numerical calculation. Note that αN is constant and 64 in the 6-bit ADC. In a practical interpolation, load capacitance per preamplifier is increased by interpolation factor α. Therefore the tail current of each preamplifier I_{ss} must be increased by α to maintain the signal bandwidth of the preamplifier with a constant overdrive voltage.

An example of random offset after averaging is shown in Fig. 9. The x axis shows the ratio of the averaging resistance to the load resistance. In Fig. 9(a), E_{ss} represents random offset caused by tail-current mismatch, and E_d represents offset caused by differential-pair mismatch. Both are normalized by the offset in a simple full flash ADC without averaging ($\alpha = 1$, $D = 0$, $R_1/R_0 = \infty$). As shown in Fig. 9(a), E_{ss} increases as α increases because ΔI_{ss} increases as α increases. To describe in detail, the gate area of tail-current transistor S_{SS} is approximately proportional to α. This makes $\Delta I_{ss}/I_{ss}$ approximately inverse proportional to the square root of α. On the other hand, I_{ss} is proportional to α. These result

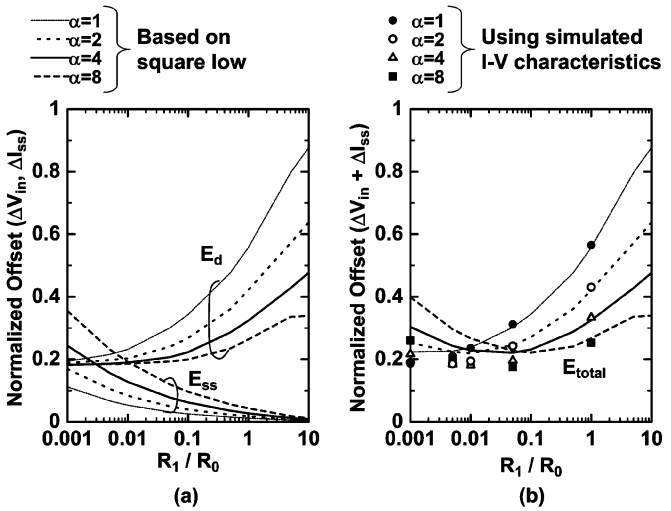

Fig. 9. Random offset after averaging ($\eta = 0.76$, $V_{FS}/V_{\rm OV0} = 5.68$). (a) Normalized random offset caused by differential pair mismatch E_d and tail current mismatch E_{ss}. (b) Normalized total random offset $E_{\rm total}$.

in ΔI_{ss} increasing with α. If R_1/R_0 is decreased, E_{ss} also increases because the attenuation in the averaging network is weakened as R_1/R_0 is decreased, and the averaging network picks up the ΔI_{ss} of more preamplifiers. These characteristics are opposite to those of E_d, as shown in Fig. 9(a). The curves in Fig. 9(b) shows the total random offset after averaging $E_{\rm total}$. The minimum value of $E_{\rm total}$ in each interpolation factor is approximately the same. Note that the points shown in Fig. 9(b) are obtained by using the I-V characteristic of the differential pair extracted by circuit simulation. They also prove that minimum value of $E_{\rm total}$ is independent of α even when the device characteristics of non-square law are taken into account. Therefore these results means that any interpolation factor α can be chosen if one considers only the random offset. In this ADC, however, the interpolation factor is optimized considering dead area in a layout and systematic error as discussed in Sections IV-B and C.

B. Analysis of Total Preamplifier Area

If smaller interpolation factor α is chosen, the preamplifiers must be broken into many smaller pieces. In an actual layout, this results in a larger dead area for isolation, interconnection, and so on. In our past layout of the preamplifier array of which interpolation factor is one, the dead area was approximately 40% of the transistor area. To estimate the total area of the preamplifier array with a given interpolation factor, the dead area per one preamplifier is assumed to be constant. Under this assumption, total dead area $S_{\rm dead}$ is given by

$$S_{\rm dead} = \frac{0.4 \cdot S_{\rm transistors}}{N(1) + D(1)} \{N(\alpha) + D(\alpha)\} \tag{7}$$

where $S_{\rm transistors}$ is the total area for the transistors and is assumed to be constant. This assumption is reasonable since the assumption of the constant total gate area is introduced in the previous subsection. Here the total number of normal preamplifiers N and the total number of dummy preamplifiers D are expressed as functions of interpolation factor α. The total area of the preamplifier array including the dead area is plotted in Fig. 10 and is normalized by $S_{\rm transistors}$. As interpolation factor

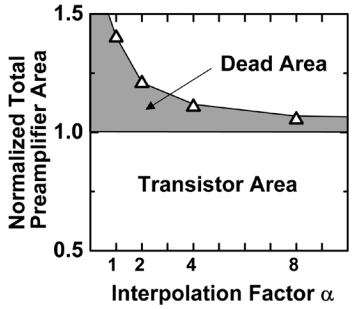

Fig. 10. Normalized total preamplifier area.

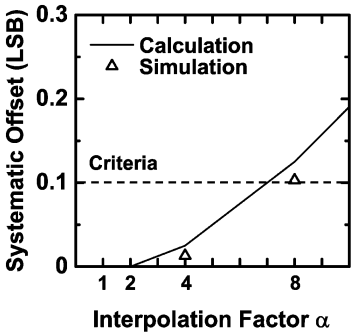

Fig. 11. Systematic offset caused by nonlinearity of differential pair.

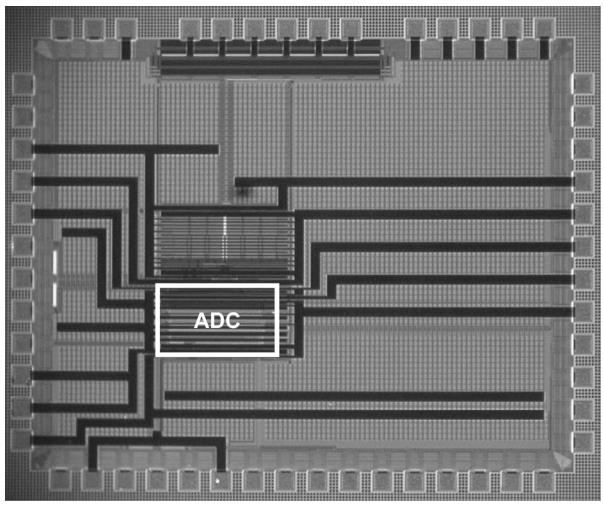

Fig. 12. Microphotograph of ADC test chip.

α increases, the total preamplifier area decreases. This estimation shows that the dead areas are 10.8% and 5.4% of the transistor area when α is 4 and 8, respectively.

C. Analysis of Systematic Offset

The systematic offset caused by the interpolation is also analyzed. This offset is caused by the nonlinearity of the I-V characteristics of the differential pair given by (1)–(3). $V_{\rm int}(i)$, which is the interpolated output of the ith tap between the kth and $(k+1)$th preamplifiers, is given by

$$V_{\rm int}(i) = R_0 \left(\frac{\alpha - i}{\alpha} J(k) + \frac{i}{\alpha} J(k+1) \right) \tag{8}$$

where $J(k)$ is the current flowing into the kth load resistance after averaging. As the currents caused by device mismatches,

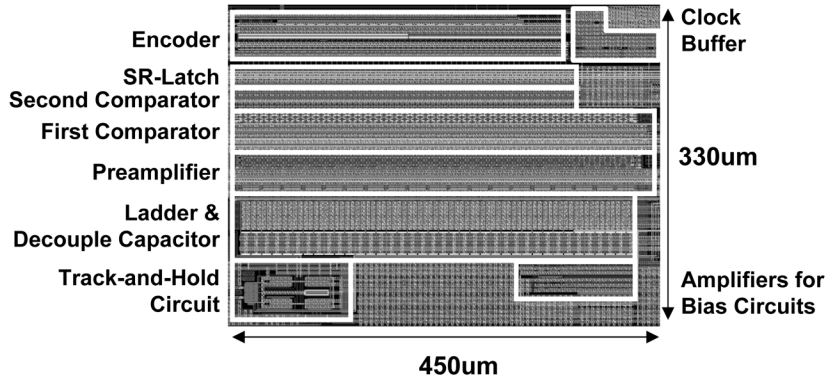

Fig. 13. Layout of ADC.

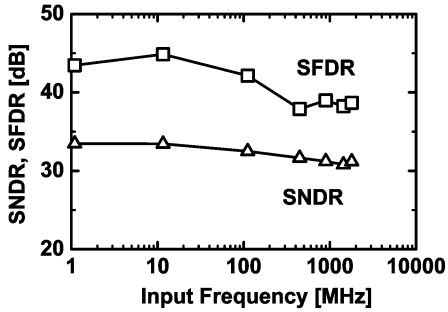

Fig. 14. Measured SNDR, SFDR ($f_s = 3.5$ GS/s).

TABLE I
PERFORMANCE SUMMARY (MEASUREMENTS)

Resolution	6 bit
Sample Rate	3.5GS/s
Input Voltage Range	560mVpp
Power Supply	0.9V
Power Consumption	98mW(@fin=nyquist)
Active Area	0.1485mm^2 (330μm * 450μm)
Technology	90nm CMOS
SNDR(@fin=nyquist)	31.18dB
SFDR(@fin=nyquist)	38.67dB
DNL(@fin=1MHz)	+0.50LSB / -0.48LSB
INL(@fin=1MHz)	+0.96LSB / -0.39LSB

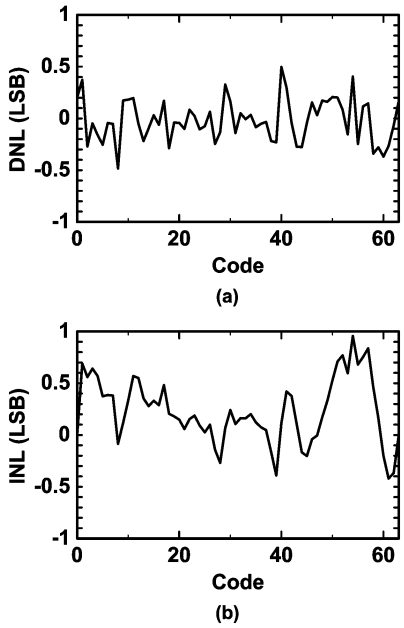

Fig. 15. Measured linearity ($f_s = 3.5$ GS/s, $f_{\rm in} = 1$ MHz). (a) DNL. (b) INL.

the drain currents of the differential pair given by (1)–(3) propagate to the kth output node attenuated by the averaging network. However, unlike random offset, $J(k)$ is given by simply summing these currents. The systematic offset is obtained by searching $V_{\rm in}$ when $V_{\rm int}(i) = 0$ and has maximum absolute value at $i/\alpha = 1/4$. Fig. 11 shows the dependence of the maximum systematic offset on interpolation factor α. The curve is obtained from analysis described above and the points are obtained by circuit simulations. When α is 1 or 2, this offset is zero. As α increases further, the systematic offset increases and is more than 0.1 LSB when α is 8 or more. Although $\alpha = 8$ gives a smaller area than $\alpha = 4$ as described in the previous subsection, we chose $\alpha = 4$ because the systematic offset of 0.1 LSB is not negligible in the error budget of this ADC.

V. MEASUREMENT RESULTS

The ADC test chip shown in Fig. 12 was fabricated in a 7-metal single-poly 90-nm CMOS process. Fig. 13 shows a layout plot of the ADC. The track-and-hold circuit, the preamplifiers, the first-stage comparators, the second-stage comparators, the SR latches, and the digital encoder are placed from bottom to top in the ADC core area. The resistor ladder is laid out from left to right, which pitch is the same as that of the preamplifiers. The device mismatch of the reference ladder resistors could increase the $\Delta V_{\rm in}$ in (4). However, it causes less than 0.01LSB and is negligible. A capacitor of 1 pF is placed in each reference ladder tap to minimize the reference voltage fluctuation. Moreover, the vacant area of the ADC is filled with on-chip decoupling capacitors inserted between the power supply and ground lines.

Fig. 14 shows the measured SNDR and SFDR at 3.5 GS/s as a function of input frequency. With low input frequency of 1 MHz, the ADC achieves SNDR of 33.47 dB and SFDR of 43.46 dB. Even with Nyquist input, SNDR and SFDR are as high as 31.18 dB and 38.67 dB, respectively. The track-and-hold

TABLE II
POWER EFFICIENCY COMPARISON

Papers	fs(GS/s)	Power(mW)	ENOB(bit)	fin(GHz)	FOM (pJ)
[3]	2.00	310	4.69	1.00	6.00
[5]	4.00	182	No Data	-	-
[13]	4.00	990	4.69	1.02	18.84
This work	3.50	98	4.89	1.75	0.95

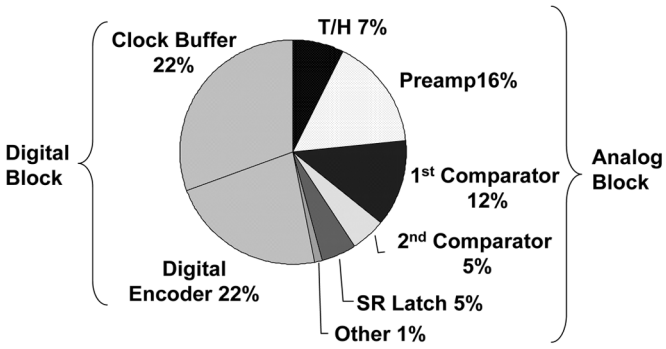

Fig. 16. Simulated power consumption ratio for each block ($f_s = 3.5$ GS/s, $f_{\rm in}$ = Nyquist, $V_{\rm dd} = 0.9$ V).

circuit and the fast over drive recovery of the comparator realize excellent input frequency dependence. Fig. 15 shows the measured differential nonlinearity (DNL) and integral nonlinearity (INL). They are measured at 3.5 GS/s with an input frequency of 1 MHz. DNL is within ± 0.5 LSB, and INL is within ± 1 LSB. The measurement results are summarized in Table I. The input voltage range of the track-and-hold circuit in the ADC is 560 mVpp. The input range of the preamplifier is 512 mVpp due to 9% loss of the track-and-hold circuit. This ADC has an analog power-supply pin and a digital power-supply pin and the measured power consumption of analog and digital blocks are 46 mW and 52 mW, respectively. The ratio of power consumed by each block is shown in Fig. 16.

VI. CONCLUSION

A 6-bit 3.5-GS/s flash ADC fabricated in a 90-nm CMOS process was described. The load circuit with the clamp diode and the replica-biasing scheme avoided overswing in the output of the preamplifiers without disturbing small signal amplification and realized high-speed operation under low supply voltage. The acceleration capacitor in the first-stage comparator accelerates overdrive recovery and achieves high conversion rate and high input resolution bandwidth. The averaging and interpolation network is optimized based on the analysis of random offset, active area, and systematic offset. The 3.5-GS/s ADC consumes 98 mW with 0.9-V power supply. The SNDR is over 31.0 dB with Nyquist input frequency. Table II compares the power efficiency of 6-bit ADCs over 2 GS/s reported in the past. In this table, the figure of merit (FOM) in terms of energy efficiency is defined as,

$$\mathrm{FOM} \equiv \frac{\mathrm{Power}}{(2^{\mathrm{ENOB}} \cdot f_s)}, \tag{9}$$

where ENOB is the effective number of bits measured with Nyquist input frequency at a sampling frequency of f_s. If ENOB is measured at less than Nyquist input frequency, the f_s value is replaced with two times the measured input frequency. As shown in Table II, this ADC achieved the best power efficiency among 6-bit ADCs operating over 2 GS/s.

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Kazuaki Deguchi was born in Hyogo, Japan, on February 15, 1978. He received the B.S. and M.S. degrees in electronics, information systems and energy engineering from Osaka University, Suita, Japan, in 2000 and 2002, respectively.

He joined Mitsubishi Electric Corporation, Hyogo, Japan, in 2002 and moved to the Advanced Analog Technology Division, Renesas Technology Corporation, Japan, in 2003. In these companies, he has been engaged in research and development of high-speed ADCs.

Naoko Suwa received the B.S. degree in solid-state physics from Osaka University, Japan, in 1986.

She joined Mitsubishi Electric Corporation, Hyogo, Japan, in 1986 and moved to the Advanced Analog Technology Division, Renesas Technology Corporation, Japan, in 2003. In these companies, she has been engaged in research and development of analog and mixed-signal circuits including A/D and D/A converters, and other analog circuits.

Masao Ito received the B.S. degree in electric and electronics engineering from Kobe University, Japan, in 1989.

In 1989, he joined the LSI Laboratory, Mitsubishi Electric Corporation, Itami, Japan. In 2003, he was transferred to Renesas Technology Corporation, Itami, Japan, which is a joint company of Mitsubishi Electric Corporation and Hitachi Ltd. in the semiconductor field. He has been engaged in research and development of CMOS A/D converters.

Mr. Ito is currently a technical program committee member of the Symposium on VLSI Circuits.

Toshio Kumamoto received the B.S. and Ph.D. degrees in electrical engineering from Osaka Prefecture University, Sakai, Japan, in 1983 and 1991, respectively.

In 1983, he joined the Mitsubishi Electric Corporation, Itami, Japan, where he had been engaged in research and development of high-speed ADCs. Since 1997, he has been engaged in development of delta-sigma ADCs and DACs. In 2003, he was transferred to Renesas Technology Corporation, Japan.

Dr. Kumamoto is a member of the Institute of Electronics, Information and Communication Engineers (IEICE) of Japan.

Takahiro Miki (M'05–SM'06) received the B.S., M.S., and Ph.D. degrees in electronics engineering from Osaka University, Japan, in 1980, 1982, and 1994, respectively.

He joined the LSI Research and Development Laboratory, Mitsubishi Electric Corporation, Japan, in 1982 and moved to Advanced Analog Technology Division, Renesas Technology Corporation, Japan, in 2003. In these companies, he has been engaged in research and development of analog and mixed-signal circuits including A/D and D/A converters, and wireless communication circuits.

Dr. Miki received the R&D100 Award in 1997 and the IEEE International Solid-State Circuits Conference Evening-Panel Award in 2007. He has presented more than 30 papers for technical journals and international technical conferences. He has served as a technical committee member of Symposium on VLSI Circuits, IEEE Asian Solid-State Circuits Conference, and IEEE Custom Integrated Circuits Conference. He is a member of the Institute of Electronics, Information and Engineering (IEICE) of Japan and a senior member of IEEE.