Clock Recovery for a 40 Gb/s QPSK Optical Receiver

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***Abstract*— A clock recovery circuit for a 40Gb/s optical coherent receiver realized in CMOS 90nm technology is presented. The core PLL generates less 0.3ps rms jitter for a bandwidth of 0.5MHz. This is mainly due to the on-chip differential LC VCO with power supply regulation. The VCO operates at 11.5GHz center frequency with a 25% tuning range. Its phase noise at 1MHz offset is better than -110dBc/Hz, and consumes 3mW of power. In tone acquisition mode the PLL is a regular charge pump PLL, while in data acquisition mode the DSP core corrects the frequency through the tuning ports. The presented PLL is one of the key components in the 24Gs/s ADC and coherent receiver chip.**

I. INTRODUCTION

Future competitiveness for optical communication systems entirely depends upon the development of new modulations and DSP to overcome the optical impairments. The performance of IMDD modulation at 40 Gb/s is very sensitive to noise, dispersion, PMD and PDL. The use of optical DCMs (dispersion compensation modules) to compensate for fiber dispersion is no longer viable. It is desirable to eliminate the use optical DCMs, and keep the 50 GHz WDM spacing, while achieving a 40 Gb/s line rate. One way to achieve this is to use the two polarization modes and coherent detection. Recent developments in electronic digital signal processing technology had enabled this new paradigm shift in fiber-optic communications. The integration of DSP engines, data conversion, and clock generation is clearly the winning recipe in controlling cost and increasing reach and throughput of optical communication systems [1] [2] [3][4]. The realization of high-speed data converters (ADCs and DACs), and digital signal processors has allowed advanced signal processing to offer substantial improvements in system performance [5].

The latest metro and long-haul terminals attack these challenges to obtain 40Gb/s system by leveraging the ever increasing computational speed and capacity of electronics − optical line complexity is minimized, agility and efficiency increased, while cost is reduced. It is done by employing Dual-Polarization Quadrature Phase-Shift Keying (DP-QPSK) modulation [1]. Compared with IMDD, QPSK sends twice as many bits per symbol. This information rate is doubled again to 4 bits/symbol by independent modulation of two orthogonal polarizations. To eliminate the optical DCMs, the linear digital dispersion compensation is performed in the receiver, due to coherent detection for DP-QPSK.

The 24Gs/s ADC and the clock recovery are the focus of this paper. They are keys in defining the system performance. Clock jitter, defines the certainty in the sampling moment and the effective number of bits (ENOB) of the interleaved 24Gb/s ADC [5]. We propose a frequency-synthesis block where the jitter performance in the OUT-2 band is less 0.3ps RMS for 0.5MHz bandwidth..

In section 2, we describe the 40Gb/s coherent transceiver architecture. The 24Gs/s ADC architecture, requirements and performances are presented in section 3. In section 4, we describe the clock recovery macro and the performance of each of its building blocks.

II. 40GB/S DP QPSK COHERENT SYSTEM

The quest for better performance in optical receivers has spurred the recent surge of interest in coherent detection. There are two fundamental advantages of coherent receivers over direct-detection receivers; first, they are more sensitive, second, coherent receivers are more selective because they can perform channel selection in the electrical domain. The selectivity promised by coherent receivers is key to exploiting the immense bandwidth of optical fiber.

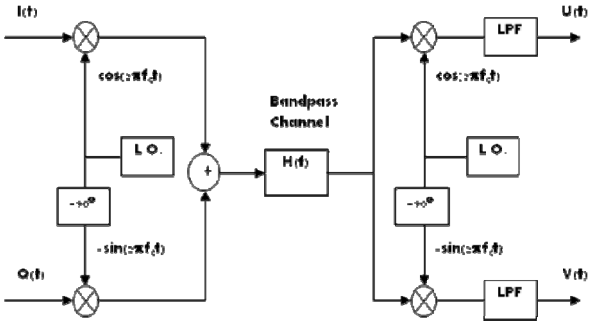

Figure 1. Coherent QPSK/QAM system

In coherent detection, the received optical signal is added to a local oscillator (LO) optical signal, and the combined light wave is directed towards a photo detector. The current produced by the photo detector is centered at an intermediate frequency (IF) equal to the difference between the LO and carrier frequencies where well-established signal processing techniques can be employed. Furthermore, the IF signal in a

coherent receiver is simply a frequency-translated replica of the original optical signal, opening the door to more sophisticated modulation schemes, such as frequency and phase modulation. Thus, just as heterodyne techniques have revolutionized radio communication, today coherent techniques are revolutionizing optical communication.

The combination of coherent detection, analog-to-digital conversion, and digital signal processing provides a powerful approach for mitigating transmission impairments and implementing required functions in a fiber-optic receiver [3].

We observed that, 40 Gb/s DP-QPSK has more or less the same performance as 10 Gb/s IMDD, but has 4 times the capacity [1]. This allows the overbuild of existing 10 Gb/s routes. Furthermore, when coherent detection is used, linear digital filters are effective to combat PMD [1].

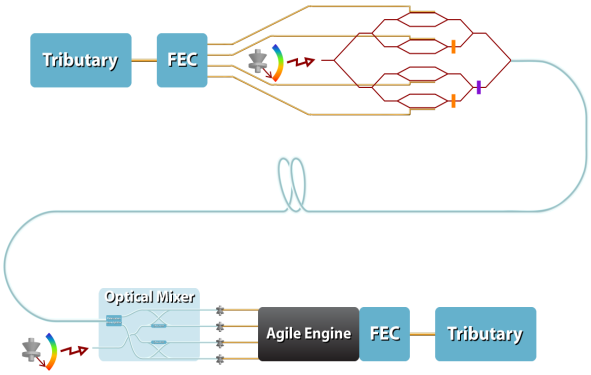

Figure 2. Top level block diagram of coherent modem.

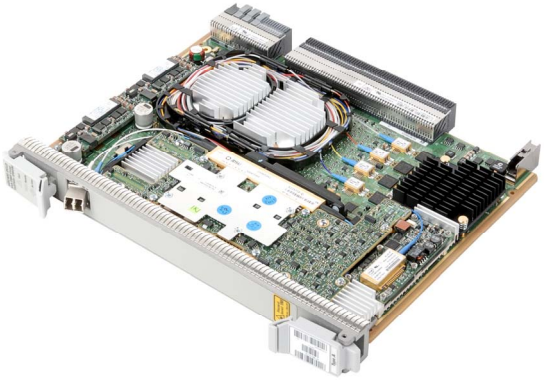

Figure 3. Photograph of the DP-QPSK coherent transceiver

Fig. 2 and Fig. 3 show the block diagram and the photograph of the DP-QPSK coherent transceiver. The polarization combiner accepts these two optical signals and adds them to produce a DP-QPSK optical signal. At the receive side, the receive signal is passed through a polarization beam splitter and decomposed into two orthogonal signals. Each orthogonal signal is fed into an optical hybrid together with the output of the local oscillator (a tunable laser) that is provisioned to select the WDM channel used by the transmitter and then controlled to be within a few hundred MHz of the carrier frequency.

The four resulting polarization and phase orthogonal signals are detected by individual photodiodes, amplified, filtered and then digitized using four 24 GS/s ADCs with 6-bit resolution. The ADCs and the overall receiver circuits have a net 3 dB bandwidth of 6 GHz. Clock recovery, carrier recovery, polarization and polarization mode dispersion (PMD) tracking and dispersion compensation are performed digitally, requiring 12 trillion integer operations per second.

A photograph of the Agile Engine's 20-million gate CMOS ASIC layout is shown in Fig. 4. The four analog-to-digital converters are the dark blocks on left side. The central black rectangle is the clock recovery macro that determines the sampling events. The ASIC is manufactured in 90-nm commercial CMOS technology, and is approximately 12 mm by 16 mm in size.

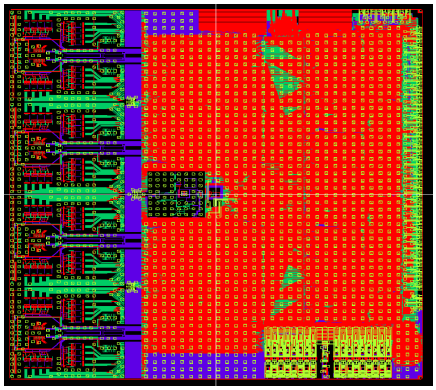

Figure 4. Photograph of Agile Engine CMOS ASIC layout.

III. 24Gs/s ADC

The ADC sampling rate is assumed equal to twice the baud rate of each format. A resolution of 6 bits is required for minimum OSNR penalty [3].

A. Architecture

For a CMOS ADC with sampling rates above 10GHz time-interleaved architecture is an effective approach exploiting the superior performance of CMOS switched capacitor circuits. Our ADC (Fig. 5) uses 16 interleaved 25mW 1.5GS/s 6b sub-ADCs preceded by T/H circuits. To reduce bandwidth degradation at the 50 ohm differential input, the T/H circuits are split into two arrays of 8 driven through a 6dB power splitter. Digitally controlled calibration circuits are used to correct for offset, gain mismatch and timing skew between the 16 channels.

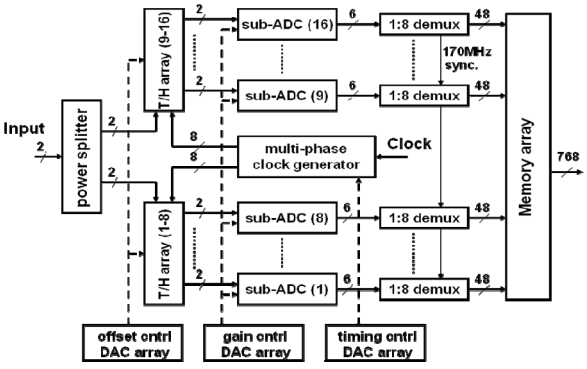

Figure 5. Interleaved ADC architecture

The 25mW sub-ADC is a 6b 1.5GS/s interleaved ADC composed of 10 elementary SAR converters running in

parallel at full clock rate as shown in Fig. 5. Each single SAR converter is using charge redistribution principle and requires 10 clock cycles to generate the 6b binary output data. With this architecture, the overall output data rate equals the clock rate.

B. Results

ENOB frequency characteristics are measured for two methods of calibration (Fig. 6). The reduction of ENOB at higher frequency is primarily due to clock jitter, uncompensated timing skew and T/H non-linearity. ENOB remains above 4.1b up to 8GHz and above 3.5b up to 12GHz input frequency. The periodic variation of ENOB curve (a) can be explained by the phase mismatch variation between T/Hs with input frequency. When calibration is performed at every frequency this variation is significantly reduced. Standard method for estimating the sampling jitter from ENOB variation at high frequency after removing all harmonics yields close to 0.4ps rms jitter generated by clock circuitry and the clock recovery PLL (estimated to be below 0.3ps rms).

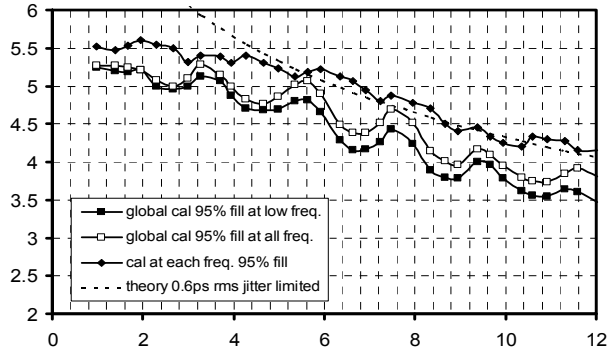

Figure 6. ENOB vs. input frequency at 24Gs/s

IV. CLOCK RECOVERY

In synchronous data communications systems, proper recovery and tracking of the symbol rate are of crucial importance for good performance. It defines the performance of the ADC and impacts the carrier and data recovery. Reducing jitter due to the VCO phase noise and coupling from the digital switching is the ultimate priority of clock recovery loop. Wide tuning range counter acts process variation and enables multi-rate multi protocol operations. The target jitter for this system is less 0.4ps rms.

The reduction of the jitter is tackled at four fronts; reduce the VCO phase noise, reduce supply variation, shield the VCO from the digital switching noise, and maximize and stabilize the loop bandwidth.

Next, we present a cross coupled VCO that generate less than -110dBc/Hz phase noise. Then the phase frequency detector and charge pump are presented. Results from different VCO's are also presented.

A. Cross coupled VCO

The VCO is an LC cross coupled differential resonator. In order to achieve good jitter performance, the loaded Q of tank is maximized by maximizing the Q's of both the inductor and the equivalent variable capacitor. To maximize the Q of the equivalent capacitor and have a differential tuning port, and the use NMOS and PMOS varactors for each the tuning ports, Fig. 7. This configuration allows for better phase noise by reducing the 1/f noise, better common mode power supply noise rejection, and extended tuning range. The noise rejection is further improved by regulating the power supply and providing programmability of the supply level, Fig. 7. By adjusting the level of the VCO supply the VCO gains can be adjusted, residual power supply noise can be rejected, and optimum voltage for minimum phase noise can found for each frequency. The VCO, the output buffer, and the regulator consume 15mA producing a phase noise ranging between -110dBc/Hz and -114dBc/Hz at 1MHz. Worst case supply pushing without the regulator is -0.8MHz/mV. Furthermore, in order to achieve a low phase noise, the varactor sizes are maximized and the inductor is minimized without affecting its Q factor.

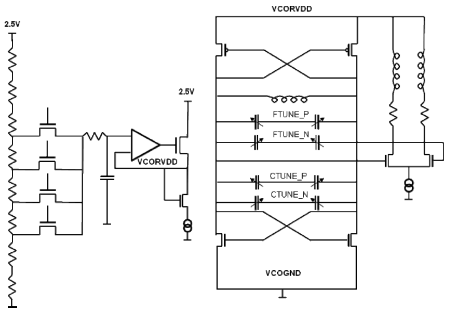

Figure 7. Cross-coupled VCO with power supply regulator

B. Phase detector and charge pump

The charge pump is a 2.5V differential circuit with common mode feedback and tri-state mode of operation, Fig. 4. The circuit consists of two matched pairs of 125uA NMOS and PMOS current sources driven from a common mode feedback circuit. The PMOS sources are shielded from the output voltage variation using a cascode block. The common mode is also set to minimize the phase noise and extend the tuning range of the VCO. The system requires a drift rate less than 100MHz/second when the charge pump is in neutral state. Due to leakage and different output voltages, the neutral state alone cannot guarantee this requirement. To meet the drift rate requirement a tri-state mode is implemented by shutting down the current sources.

The phase detector was modified to reduce the dead zone and increase the gain of individual cells. Reducing the PFD dead zone reduces the phase ripple and improves the PLL phase noise.

In order to simplify the testing of the clock recovery block, the 11.5 GHz PLL uses a half rate clock that can be generated by the tester. The charge pumps can be driven directly from the digital core in test mode to measure the up, down, and neutral current. Lock detector, frequency monitoring, and circuits for analog probing are also implemented. The structural measurements performed on these blocks are used to infer the functional characteristics of the PLL, such as bandwidth,

damping coefficient, tuning range, VCO gains, charge pump current, and drift rate.

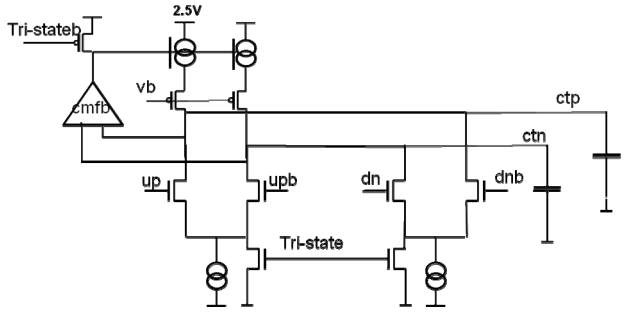

Figure 8. Charge pump with common mode feedback

C. *Experimental results*

Prior to the implementation of the final chip, a test chip was designed in order to de-risk the final implementation. Six PLL's were implemented in order assess phase noise, tuning range, center frequency, KVCO, supply pushing, charge pump drift rate, and other PLL and VCO metrics. Each PLL occupies an area of 1mm^2 and powered with 2.5 V supply for the charge pump and 1V for the remaining circuits.

TABLE I. TEST CHIP RESULTS

	Tuning range GHz	Center frequency GHz	Kvco [GHz/v]	Phase noise @ 1MHz	Supply pushing MHz/mV
PLL1	3.1	11.9	3.2	-99	-2.1
PLL2	3.2	11.5	3.3	-99	-1.7
PLL3	3.2	11.3	3.3	-100	-2.8
PLL4	3.2	11.2	3.2	-99	-2.6
PLL5	3.2	11,5	3.3	-100	-2.6
PLL6	***3***	***11.1***	***1.4***	***-110***	***-0.8***

PLL1 to 5 use cross coupled VCOs with single ended tuning control, and PLL6 uses a pseudo differential control using pairs of NMOS and PMOS varactors. The VCO alone achieves a Figure of Merit (FoM) of 189 at minimum power supply of 0.8V. To our knowledge, this FoM with the extended tuning range, places this VCO among the best reported ones [6] [7].

Table I summarizes the measured performances. From these measurements, it is clear that the VCO with NMOS PMOS differential control has better phase noise and supply pushing performances, but the center frequency is too low. In the final chip the center frequency was increased to 11.5GHz, and to further improve the supply pushing, a power supply regulator is also implemented. The achieved phase noise of the VCO at 1MHz offset is -110dBc/Hz, the power consumption of VCO is 3mW.

The clock recovery in the final chip occupies an area of 4mm^2, this area is needed for on chip decoupling and shielding the VCO from the digital noise.

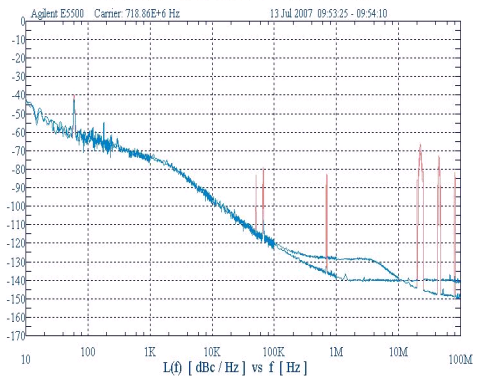

Figure 9. Reference and VCO Phase noise

Fig. 9 shows the measured phase noise of the coherent transceiver, the receiver clock phase noise is -110dBc/Hz at 1MHz offset from the carrier.

V. CONCLUSION

In this paper we presented a clock recovery maco generating less than 0.3ps RMS jitter for a bandwidth of 0.5MHz. In order to reduce jitter, we proposed a VCO architecture with a phase noise less than -110dBc/Hz at 1MHz offset. To further reduce the jitter, a supply regulator with programmable voltage is designed. The VCO and PLL are isolated from the digital core and other switching circuits using buffer zone that increases the impedance between analog and digital grounds. The clock recovery presented here is at the heart of the recently commercialized coherent optical transmission system at 40Gb/s. It enabled both the 24GS/s ADC conversion, where jitter is the bottleneck, and laser carrier recovery. With this system, we demonstrated that CMOS ASIC technology can manipulate the optical electrical field using data conversion and DSP.

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