A 1-V 1.25-GS/S 8-Bit Self-Calibrated Flash ADC in 90-nm Digital CMOS

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***Abstract*—We present an 8-bit 1.25-GS/s flash analog-to-digital converter (ADC) in 90-nm digital CMOS with wide analog input bandwidth and low power dissipation. The ADC employs two key techniques: a self-biased track-and-hold amplifier which enhances the ADC full-scale voltage and enables the converter operating under a single 1-V supply; and an improved calibration scheme based on reference pre-distortion to enhance the ADC linearity without sacrificing its sampling speed. The prototype converter thus achieves 7-, 6.9-, 6.5–bit ENOB at 1.25 GS/s for input signal frequencies of 10 MHz, 600 MHz, and 1.3 GHz, respectively, and better than 52-dB SFDR across the full Nyquist-band, while dissipating 207 mW from a single 1-V supply.**

***Index Terms*—Calibration, flash analog-to-digital converter (ADC), offset correction, source follower, unity-gain buffer.**

I. Introduction

HIGH-SPEED (2 to 10 GS/s), medium-resolution (6 to 8 bits) and low-power analog-to-digital converters (ADCs) are essential in realizing multi-Gb/s communication systems. Folding- and flash-ADCs are the primary candidates for such applications due to their high conversion rate and low latency. Although folding-ADCs use fewer comparators and simpler encoder circuits [1] than their flash counterparts, they demand larger voltage headroom and are more sensitive to device mismatch. With the CMOS technology scaling, comparators and encoder circuits consume less power and area, therefore, flash-ADCs can be pushed to achieve higher resolutions than their 6-bit prior arts [2], [3]. Owing to the extensive use of digital circuitry and the absence of high gain amplifiers, flash-ADCs are technology-scaling friendly.

Nevertheless, resolutions of flash-ADCs are plagued by the pronounced device mismatch in deep scaled CMOS technologies. To overcome this disadvantage, a self-biased track-and-hold amplifier (THA) is proposed to boost the size of LSB. An improved calibration scheme based on reference pre-distortion [2], [4], [5] is also implemented to correct the mismatch induced errors without sacrificing the sampling speed. With both techniques, the 8-bit full flash ADC is realized in the 90-nm digital CMOS technology. The prototype achieves 7-, 6.9-, 6.5-bit effective-number-of-bits (ENOB) at 1.25 GS/s for input signal frequencies of 10 MHz, 600 MHz, and 1.3 GHz, respectively, and better than 52-dB suprious-free dynamic range (SFDR) across the full Nyquist-band, while dissipating 207 mW from a single 1-V supply. Due to its large effective resolution bandwidth (ERBW) of 1.3 GHz, the ADC is capable of supporting subsampling systems. With two-channel time interleaving, the sampling rate can be doubled. The channel transfer function mismatch can be canceled by the presented calibration circuitry.

The converter architecture is described in Section II. The THA design and the self-biased pseudodifferential buffer are presented in Section III. Section IV describes the calibration scheme. The other critical ADC building blocks are addressed briefly in Section V. Section VI reports the experimental results and conclusions are drawn in Section VII.

II. Converter Architecture

The ADC, as shown in Fig. 1, contains a THA, an array of reference generators, four-stage pre-amps, comparators, an encoder, a calibration loop, a clock generator and output drivers. The cascaded pre-amps, instead of a single gain stage, sufficiently amplify the differences between the input signal and the references to overcome the dynamic offsets of the comparators. Interpolating allows the generation of intermediate zero-crossings (i.e., ZXs), which signify the input thresholds at which their corresponding pre-amps' outputs cross the zero voltage. Consequently, the input does not need to be compared with 255 distinct reference voltages, and thus reducing the total number of pre-amps and leading to a more compact layout and potentially higher bandwidth. The first two stages generate 33 ZXs, which are rectified by the calibration scheme. The resistive interpolation-by-2 and -by-4 networks at the outputs of the second and third stages, respectively, provide the remaining ZXs.

III. THA With the Self-Biased Buffer

The pseudodifferential open-loop THA, as illustrated in Fig. 2, is applied to prevent the signal-to-noise-distortion ratio (SNDR) roll-off with the increase of input frequency. It employs bootstrapped switches for better than 9-bit tracking linearity. A pseudodifferential pMOS source follower was typically used in the past as the buffer to drive the subsequent pre-amps with its highly linear and voltage level shifting characteristics. However, due to device short-channel effects, its output swing and the corresponding ADC full scale voltage were attenuated, which necessitated more power consumption of the ADC to achieve the intended accuracy. Cascode bias currents, the use of long channel length devices or dynamic biasing with feedback could improve the output swing and overall linearity. But they might demand larger voltage headroom and/or introduce speed penalty.

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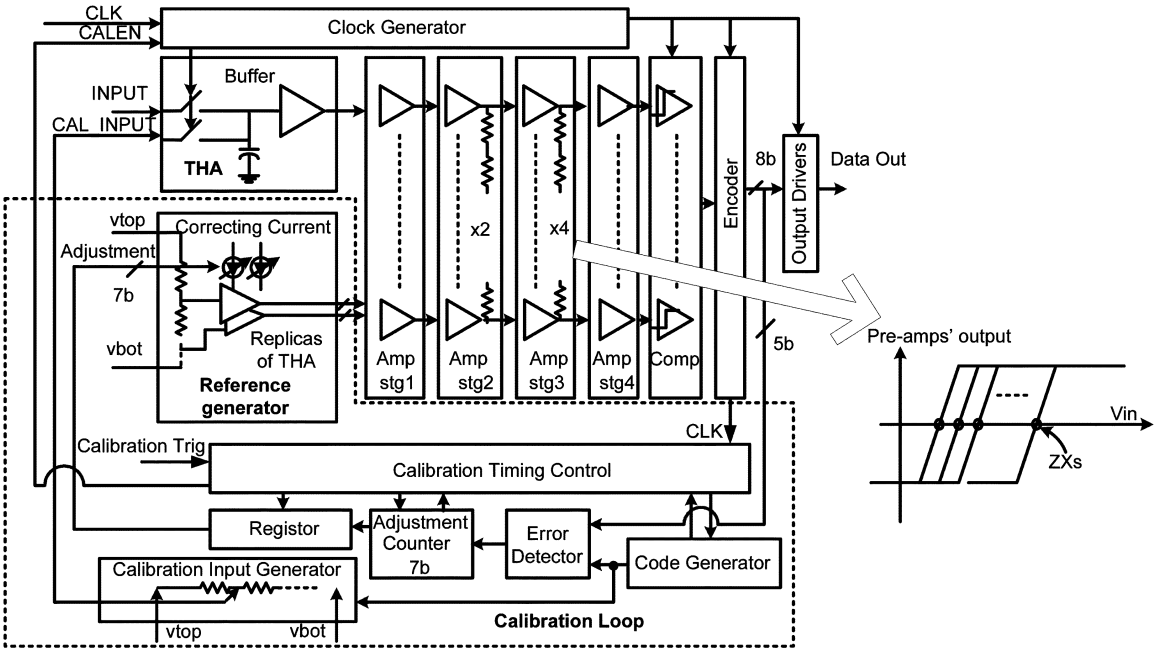


Fig. 1. Block diagram of the ADC.

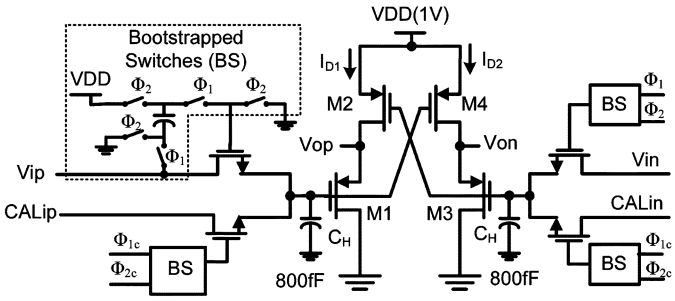
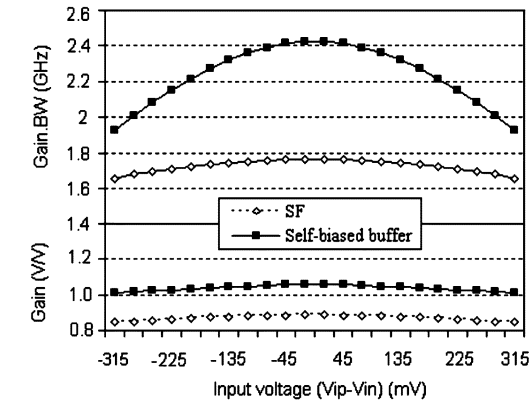


Fig. 2. THA with the self-biased buffer.

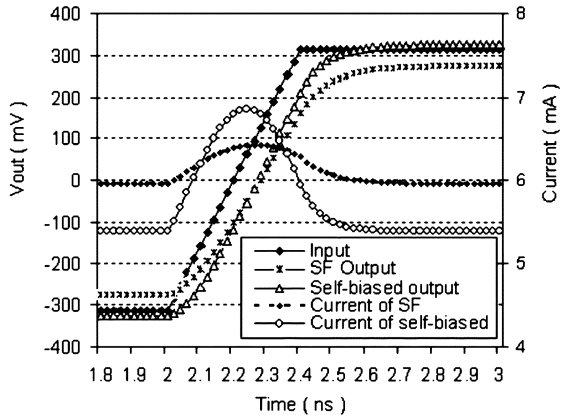
We mitigate this drawback by connecting the gates of M2 and M4 to the signal inputs, instead of a fixed bias voltage, as illustrated in Fig. 2. Here, M2 and M4 act as dynamically biased current sources for the source followers of M1 and M3. As the input $V_{\rm ip}$ increases, $I_{\rm D1}$ decreases due to the reduced drain–source voltage of M2; however, the complementary input $V_{\rm in}$ decreases to counter the drop of $I_{\rm D1}$. With this approach, the dc gain of the buffer exceeds unity with 0.8 $V_{\rm p-p}$ swing. Since the gain dependence on r_0 of M2 and M4 is relaxed, which allows the use of feature-size transistors, the buffer bandwidth is thus enhanced. Furthermore, the slew rate is also improved without dissipating additional static power due to the dynamic biasing.

The simulated comparisons of the small signal dc gain, gain bandwidth product and a step response between the self-biased buffer and the source follower are shown in Fig. 3, assuming both drive the same load with the same static power consumption. The common mode voltage is set as 0.25 V. The small signal gain and gain bandwidth product are plotted as a function of the differential dc input voltage. The gain, gain bandwidth product and the slew rate are improved by 20%, 40%, and 30%, respectively.

In this work, input signals are ac coupled with their common-mode voltage properly biased off-chip. As a result, the THA achieves wider than 2-GHz bandwidth while consuming 7 mW from a 1-V supply; this is 50% less power consumption compared to a conventional source follower design.



(a)



(b)

Fig. 3 (a). Comparison of the simulated gain and gain · BW. (b) Comparison of the simulated step response.

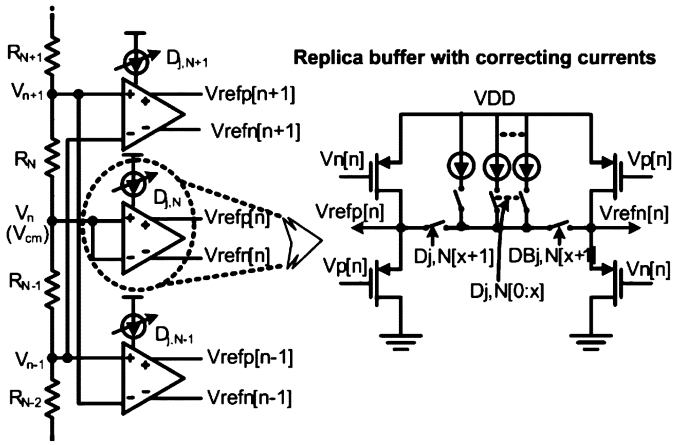


Fig. 4. Reference generation to compensate the THA buffer distortion and facilitate the calibration scheme.

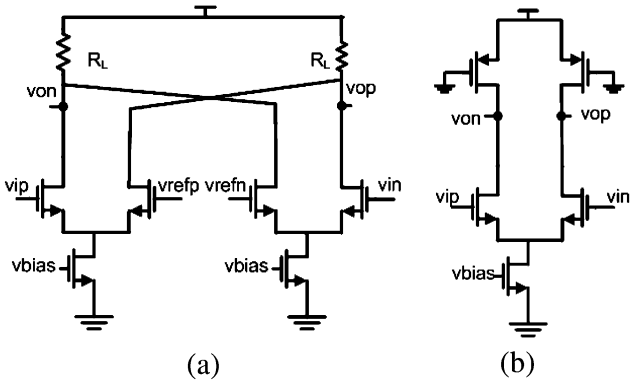


Fig. 5. Pre-amps design. (a). First-stage pre-amp. (b). Fourth-stage pre-amp.

However, the total harmonic distortion of the buffer is limited to about −50 dB. In order to attain the 8-bit resolution, the buffer distortion has to be compensated. As shown in Fig. 4, replica THA buffers are applied in the reference paths to pre-distort the references as the input signal; this was previously used in [4]. By sharing the same power/ground lines with the THA, the replicas can also partially track and offset the THA output changes due to the process, supply voltage and temperature variations.

The replicas can be 20 to 30 times smaller than the original THA buffer, since one replica only drives one pre-amp. The current through the resistor ladder can be reduced to counter the power increase caused by the replicas.

The mismatch between the THA and its replicas leads to INL errors. The intended calibration scheme is designed to resolve this issue and further correct the offsets of differential pairs along the data conversion path.

IV. Calibration Scheme

CMOS flash-ADCs suffer greatly from random ZXs offsets due to device mismatch in the pre-amps and comparators. Averaging networks can improve ADCs linearity. However, large MOSFETs are still required for the pre-amps. To overcome this obstacle, many calibration algorithms were proposed. Some of them had to insert calibration circuits within data conversion paths, which inevitably affected signal integrity [1], [4]; some could not remove random errors [2] and some had excessive implementation overhead and limited applications. This work proposes a calibration scheme based on reference pre-distortion. As illustrated in Fig. 4, the corrective currents are injected into the replica buffers to shift the references to the desired values, so that the cumulative ZXs errors introduced by the replica buffers, pre-amps, and comparators are corrected.

Reference pre-distortion schemes proposed in the past were either for compensating the THA distortion, such as that in ref [4], or for correcting comparator offsets, such as those in ref [2], [5]. This work naturally combines both features by using the identical replica THA buffers to further push the flash ADC performance.

In the calibration process, as illustrated in the dashed area of Fig. 1, a set of digital codes representing the desired ADC outputs are initialized serially by the code generator, which subsequently select the calibration input levels via switching a precisely tapped resistor ladder in the calibration input generator. According to the foundry reported resistor matching performance, this careful laid out resistor ladder can maintain at least 10-bit equivalent linearity. As shown in Fig. 2, Φ_{1c} and Φ_{2c} sample the CAL $_{\rm ip}$ and $\rm CAL_{in}$, while Φ_1 and Φ_2 disconnecting the $V_{\rm ip}$ and $V_{\rm in}$. The ADC quantizes the calibration input instead of the normal input. The corrective currents are then produced by comparing the actual ADC outputs with its anticipated outputs at the error detector. The current adjustable range and step size are dictated by the adjustment counter (7-bit in this design) and an off-chip tunable bias current. This design permits the error correction up to $\pm$ 10LSB with 0.2LSB/step. After the calibration is finished, the "CALEN" exchanges the Φ_1, Φ_2 with Φ_{1c} and Φ_{2c}, to resume the normal operation.

The maximum calibration cycle is about 0.12 ms with the process performed at 100 MS/s. The 31 ZXs, generated by comparing the input with the set of references, are calibrated. The errors of the interpolated ZXs, caused by the offset of pre-amps in the third and fourth stages and comparators, are not subject to the proposed calibration but suppressed by the gain of their preceding pre-amps. The ADC resolution, measured repeatedly after one calibration, does not show noticeable drift over time (longer than 24 h) and under various changes of sampling frequency. Since the calibration circuitry is implemented separately from the data conversion path, this ADC can therefore achieve higher sampling speed than the prior arts.

V. Other Key Circuits Descriptions

A. Pre-Amps

As shown in Fig. 1, the four-stage cascaded pre-amps provide a voltage gain greater than 32 to reduce the dynamic offsets of comparators and expedite their logic decisions. There are no reset-switches inserted, because of the following reasons: 1) the voltage swing of each stage is small which can be recovered quickly without the assistance of a reset-switch; 2) charge injection issues caused by reset-switches may degrade the ADC accuracy; 3) clock buffers to drive reset-switches are power hungry; and 4) routing of clocks may lead to cross-talk issues. As shown in Fig. 5, the first stage pre-amps convert the pseudodifferential THA outputs to true differential signals for improved supply rejection. Since there is no interpolation network applied in the fourth stage pre-amp array, small pMOS

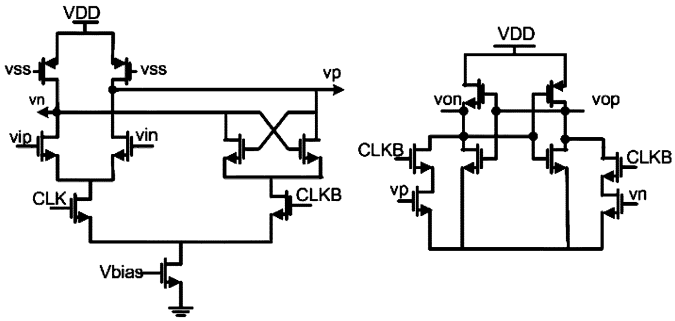


Fig. 6. Comparator design.

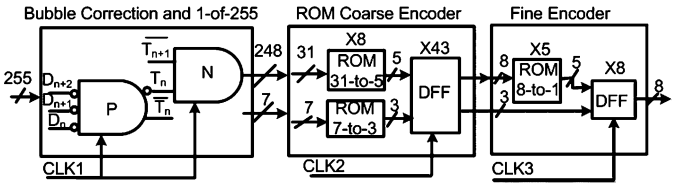


Fig. 7. Block diagram of the encoder.

transistors operating in triode region are utilized as the load resistors for more compact layout with lower parasitic capacitors. Each pre-amp achieves a gain between 2 to 3 and a bandwidth between 4 to 6 GHz. The pre-amps occupy a silicon area of 0.08 mm ^{2}, with about 120-mW measured power consumption.

B. Comparators

The high-speed current steering comparator design is shown in Fig. 6. The pre-amp and the cross-coupled regenerative latch share the same load and tail currents. The subsequent SR latch further pushes the output to swing rail-to-rail. Reset-switches are not applied because of the aforementioned reasons. The 255 comparators occupy a silicon area of 0.02 mm^2, with 24-mW measured power consumption.

C. Encoder and Output Drivers

Many encoding algorithms were developed in the past to suppress bubble errors. They either modified the one-of-N decoder to be insensitive to bubble errors, or inserted a Gray or qausi-Gray encoding stage before generating binary codes. Although a more sophisticated encoding scheme in principle is more effective in error correction, it inevitably requires extra digital operations, and in turn results in substrate and supply noise issues which adversely impact the high-speed ADC to achieve an optimal performance. Applying three-NAND gates before one-of-N decoder is an adequate bubble correction method for three reasons: signal skew introduced bubbles are removed by the front-end THA; offset errors are eliminated by the sufficient gain stages and the calibration; and meta-stable states of the comparators are prevented by cascading two latches.

As illustrated in Fig. 7, the encoder is pipelined in three stages. The bubble correction and one-of-N decoder are embedded into the true-single-phase-clocked (TSPC) registers, which reduces the number of transistors, delay and power consumption associated with the function.

The encoded outputs are decimated by 9 (the odd number is used to facilitate the output data MUX for the future two-channel time-interleaving design) on-chip to enable easy acquisition by a logic analyzer.

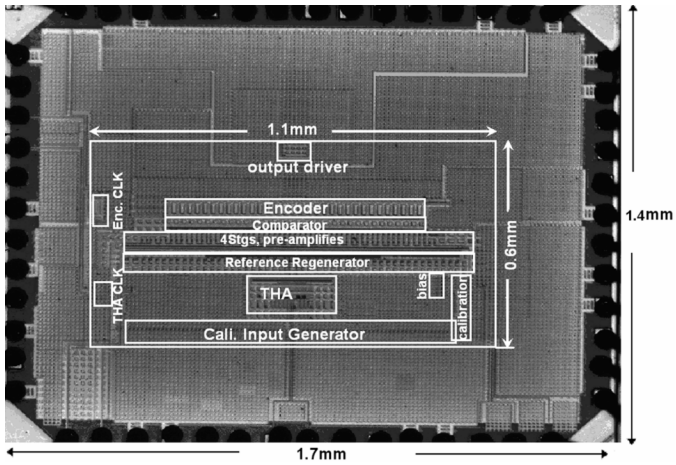


Fig. 8. ADC die microphotograph.

VI. Experimental Results

The prototype ADC is implemented in a 90-nm CMOS technology. The chip microphotograph is shown in Fig. 8. The sampling clocks are buffered separately from the clocks for the comparators and encoders, in order to minimize their rms jitter. It is extracted as 0.8 ps from a locked-histogram test, wherein the input signal of 800 MHz is synchronized to the sampling clock at 1.2 GS/s, so that the decimated outputs always occur at the vicinity of the level 128. The calibration circuitry is laid-out at the bottom right. The active area is 0.66 mm ^{2}. The chip dimensions are dominated by the number of pins, among which 34 pins are designated to power and ground for the purpose to minimize bond wire inductance. By filling the inactive area, large on-chip decoupling capacitors are obtained to suppress power-ground bouncing. The ADC chip is directly bonded on the evaluating printed circuit board.

Fig. 9 shows the measured DNL and INL profiles. They are extracted from the histogram of the 4M consecutive output samples in response to a 2.3 MHz sine-wave input at 1.25 GS/s. The peak DNL and INL with the calibration are recorded as 1.3 LSB and 1.1 LSB, respectively. The un-calibrated INL curve is typically less than 3.3 LSB. The relatively large DNLs and INLs are due to the errors of the interpolated ZXs. Reducing the interpolation factor and further increasing the ADC full scale range, which is permitted by the output swing of the THA buffer and the input range of the pre-amps, will enhance the linearity.

Fig. 10 plots the performance of the ADC as functions of input and sampling frequencies. Keeping the input signal frequency at 10 MHz, the ADC shows 6.9 bit ENOB up to a sampling rate of 1.5 GS/s. At 1.25 GS/s, the ENOB is 7.0 bit for 10 MHz, 6.9 bit for 600 MHz, 6.5 bit for 1.3 GHz, and 6.3 bit for 1.95 GHz. The SNDR drops by 3 dB at the ERBW of 1.3 GHz. The SFDR is always above 50 dB up to the ERBW, with a peak at 58 dB, thus proving the excellent linearity provided by the calibration.

The output spectrums at 1.25 GS/s with 600-MHz and 1.3-GHz input are shown in Fig. 11. The total power is 207 mW for the ADC at 1.25 GS/s with an active input, in which 141 mW is for the analog circuits, 24 mW for the comparators, 21 mW for the encoder and output drivers, and 21 mW for the clock buffers.

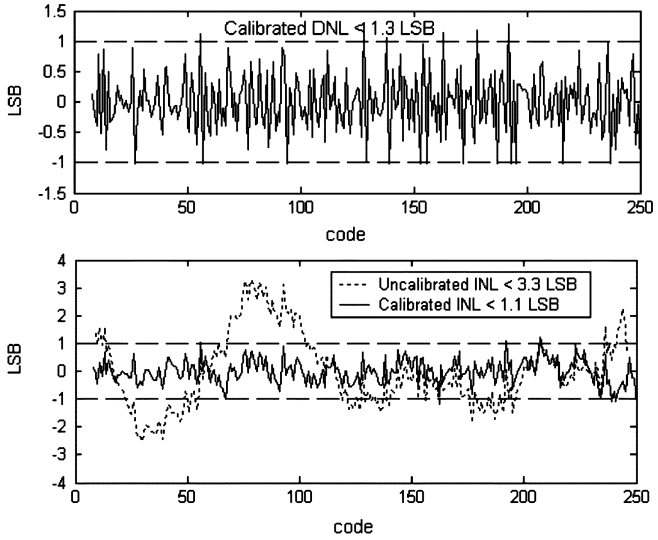


Fig. 9. Measured DNL/INL at 1.25 GS/s with a 2.3 MHz input.

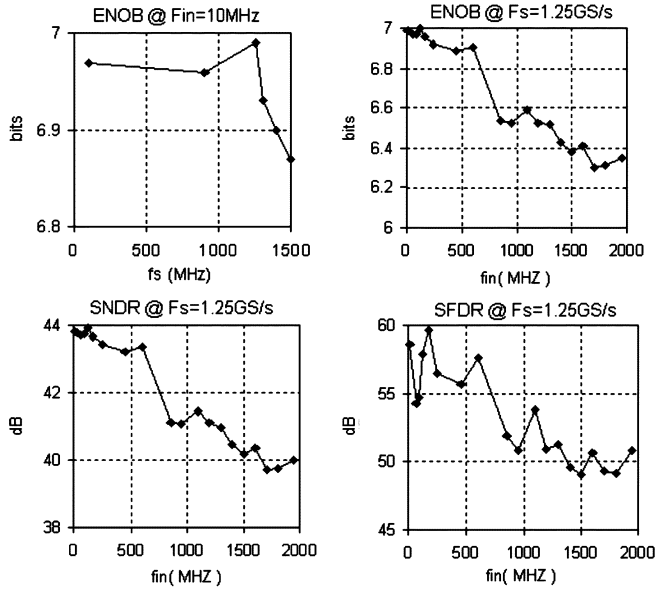


Fig. 10. Measured performance as functions of the sample rate and the input frequency.

The prototype ADC achieves a F.O.M. of 1.4 pJ/conv, which is calculated according to

$$\text{F.O.M.} = \frac{\text{Power}}{2^{\text{ENOB},\min(\text{ERBW},f_s/2)} \cdot \min(2\text{ERBW}, f_s)} = \frac{207\ \text{mW}}{2^{6.9} \cdot 1250\ \text{MHz}}.$$

VII. Conclusion

In this paper, the dynamically biased pseudodifferential THA buffer enables a larger output swing, higher voltage gain and faster settling speed compared to a conventional source follower. By using this THA design, the ADC achieves a large input full scale voltage and thus lowers the power consumption. The replica THA buffers in the reference paths compensate the THA distortion. With the calibration loop, they further improve the ADC linearity by enforcing the ZXs into their desired positions. The tested flash ADC performance validates the effectiveness of the proposed techniques in obtaining better than 6-bit resolution with low conversion energy (1.4 pJ/conv.).

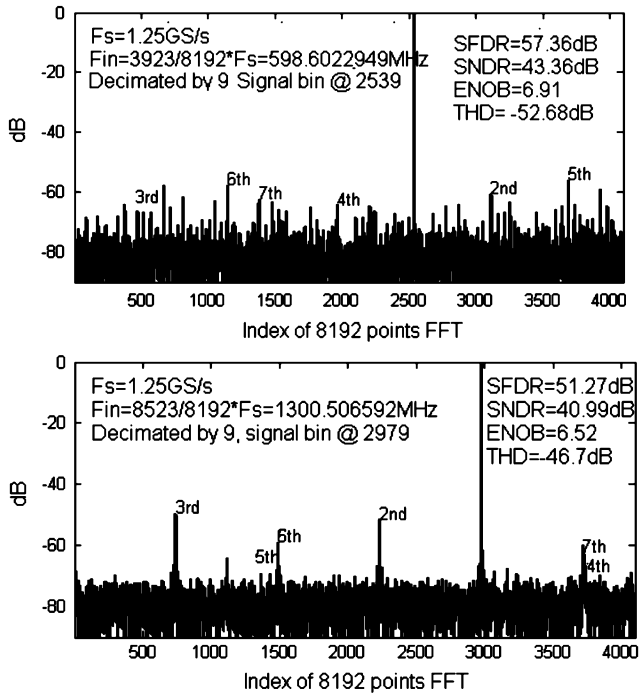


Fig. 11. Output spectra for 600 MHz and 1.3-GHz inputs at 1.25 GS/s.

References

[1] R. C. Taft, C. A. Menkus, M. R. Tursi, O. Hidri, and V. Pons, "A 1.8 V 1.6-G sample/s 8-b self-calibrating folding ADC with 7.26 ENOB at nyquist frequency," *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2107–2115, Dec. 2004.

[2] X. Jiang and M.-C. F. Chang, "A 1- GHz signal bandwidth 6-bit CMOS ADC with power-efficient averaging," *IEEE J. Solid-State Circuits*, vol. 40, no. 2, pp. 532–535, Feb. 2005.

[3] C. Sandner, M. Clara, A. Santner, T. Hartig, and F. Kuttner, "A 6-bit 1.2 GS/s low-power flash-ADC in 0.13 mm digital CMOS," *IEEE J. Solid-State Circuits*, vol. 40, no. 7, pp. 1499–1505, 2005.

[4] V. Srinivas, S. Pavan, A. Lachhwani, and N. Sasidhar, "A distortion compensating flash analog-to-digital conversion technique," *IEEE J. Solid-State Circuits*, vol. 41, no. 9, pp. 1959–1969, Sep. 2006.

[5] S. Park, Y. Palaskas, A. Ravi, R. E. Bishop, and M. P. Flynn, "A 3.5 GS/s 5-b flash ADC in 90-nm CMOS," in *Proc. Conf. 2006, IEEE Custom Integr. Circuits*, Sep. 2006, pp. 489–492.