3.4GS/s 3 Bit Phase Digitizing ADC and DAC for DRFM

Min Zhang * , Youtao Zhang, Xiaopeng Li, Ao Liu, and Feng Qian

Abstract — *This paper design and realize 3 bit phase digitizing analog-to-digital converter (ADC) and digital-to-analog converter (DAC) for Digital radio frequency memory (DRFM). The instantaneous bandwidth (IBW) of the DRFM is enhanced by high sampling rate. Test results show that the highest sampling rate is 3.4GS/s and the core power dissipation of ADC and DAC is 350mW and 300mW, respectively*[1].

Index Terms — Analog-to-Digital converter, Digital-to-Analog converter, phase digitizing, digital radio frequency memory.

I. Introduction

Digital radio frequency memory (DRFM), which is based on high-speed sampling and digital storage, can save and reconstruct the radio and microwave signal. So, it has become an effective method to interfere modern radar and has been developed into an essential part of modern electronic countermeasure (EMC) [1]-[7]. The key parameter is instantaneous bandwidth (IBW) which is determined by the bandwidth of ADC and DAC. The phase digitizing approach has some remarkable advantages over the conventional amplitude technique such as less comparators and direct digital phase modulation. Particularly, for 3-bit system, the near-harmonic suppression is improved; the worst-case harmonic for the phase digitizing approach is the seventh harmonic whereas for the amplitude approach is the second or third [3].The melioration is convenient for later signal processing.

This paper describes the design and realization of the phase digitizing ADC and DAC for 3 bit phase DRFM using standard semiconductor technology and measures 1.85 mm × 1.90 mm and 1.57 mm × 1.60 mm, respectively. ADC employs the structural which is similar to Flash architecture while DAC adopt current steering structural. To achieve the high sampling rate and lower the power dissipation, true single phase clocked (TSPC) architecture is used for inside trigger and divider.

II. Design and Realization of ADC

The detail block diagram of the 3 bit phase digitizing ADC is shown in Fig.1, including preamplifier (equivalent to THA in amplitude digitizing), single to differential converters, comparators, demultiplexer components, and output stages. This structural is similar to flash architecture.

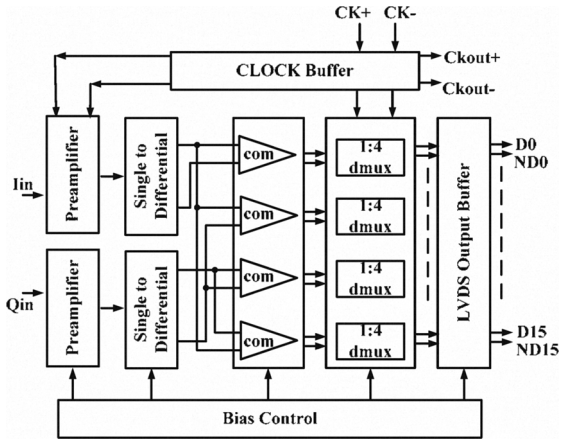

Fig. 1. Block diagram of the 3 bit phase digitizing ADC

A. Working Procedures by Steps

According to the principle of phase digitizing [1], [4]-[5], 2^3 equal phase regions are required in 2π range for 3 bit phase DRFM. Thus four digital streams at 45° with respect to each other which have the same frequency with analog input and 50% duty cycle are needed. Working procedures are as follows: first of all, orthogonal analog input signal I_{in} and Q_{in} are both amplified by preamplifier; secondly, they are converted from single-end to differential; then ,the most important step, different combination of two of the four sine waves are compared by four comparators which have same structure. Outputs of the four comparators are the data streams which want to be obtained. The timing diagram of 3 bit phase digitizing is shown in Fig.2, and the digital code of the output signal is listed in Table I. Finally, the demultiplexer components are used to reduce the date rates of the digital data streams into the digital memory.

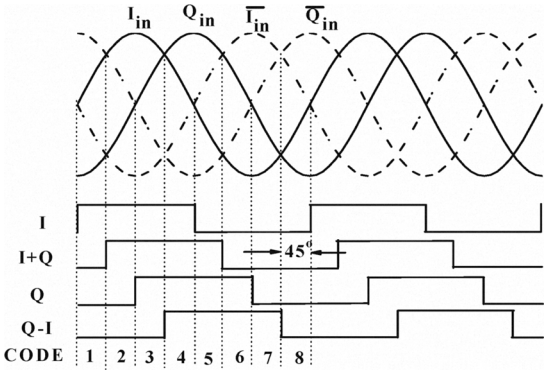

Fig. 2. Input and output timing diagram for 3 bit phase digitizing

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978-1-4244-3870-9/09/$25.00 ©2009 IEEE

TABLE I
DIGITAL CODE OF OUTPUT SIGNAL

CODE	1	2	3	4	5	6	7	8
I	1	1	1	1	0	0	0	0
I+Q	0	1	1	1	1	0	0	0
Q	0	0	1	1	1	1	0	0
Q-I	0	0	0	1	1	1	1	0

B. Design Outline

In accordance with the principle of the phase digitizing [5], the key parameters are phase accuracy and dynamic range. To attain a wide dynamic range, all parts before the demultiplexer components, especially the comparators must have large gain and satisfy the bandwidth requirement synchronously. The technique of limiting amplifier is mainly used. The classical ECL structural is adopted to realize the single amplifier of the comparator. Double guarding ring and deep nwell are employed to isolate the input stage and sequentially reduce substrate noise and upper the minimum limitation of dynamic range.

To satisfy the phase accuracy, the eight phase states after digitizing must be entirely sampled. Thus the sampling rate requires no less than eight times of analog input signal frequency. That is why the ADC bandwidth is much lower than the Nyquist frequency. High sampling rate can be obtained by using TSPC dynamic structural to implement inner divider and trigger. Reset function is also covered by the chip to guarantee multi-user. All the input and output interface obey standard LVDS transmission mode exclude analog input.

C. Realization

The 3 bit phase digitizing ADC is implemented in standard semiconductor technology. The die size restricted by many extra pads is 1.85 mm × 1.90 mm, as shown in Fig.3.

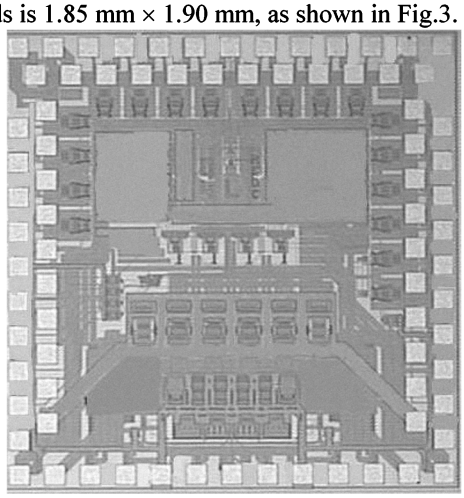

Fig.3. ADC Chip photograph

III. Design and Realization of DAC

The detail block diagram of the 3 bit phase digitizing DAC is shown in Fig.4, including LVDS input buffer, multiplexer components, switch amplifier, switch stages, and current steering parts. This configuration is named current steering structural.

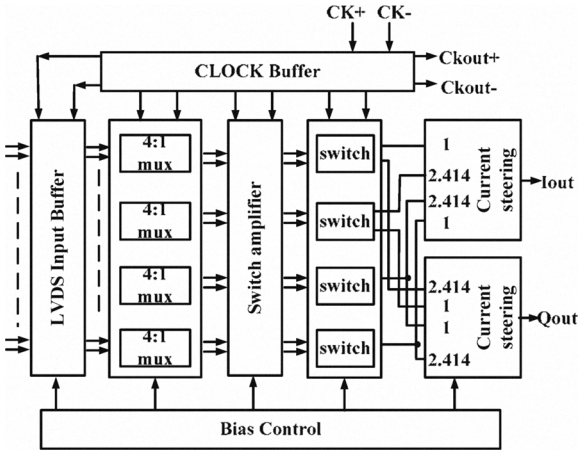

Fig. 4. Block diagram of the 3 bit phase digitizing DAC

A. Working Procedures by Steps

Phase digitizing DAC is the inverse function circuit of the above-mentioned ADC. By using a current steering structural, orthogonal analog signal can be regenerated by four data streams which are phase shifted in 45° increments. The current sources are weighted to minimize the Fourier expansion coefficient of Fourier series, thus minimizing the output spurious levels [3], [6]. Some paper has already published inferred that the most eminent current sources weight proportion is (1:2.414:2.414:1) for I_{out} and (2.414:1:1:2.414) for Q_{out} in engineering application [6]. Working procedures are as follows: firstly, the multiplexer components upgrade the date rates of the digital data streams out of the digital memory to obtain four proper data streams; secondly, amplify the data steams to ensure their drive capability; finally, these data streams switch the weighted current source and restructure the analog signals. The timing diagram of 3 bit phase digitizing is shown in Fig.5.According to the principle of regeneration, the worst-case harmonic of the reconstruct signal is the seventh harmonic, and the theoretic SFDR is -16.9dBc[3].

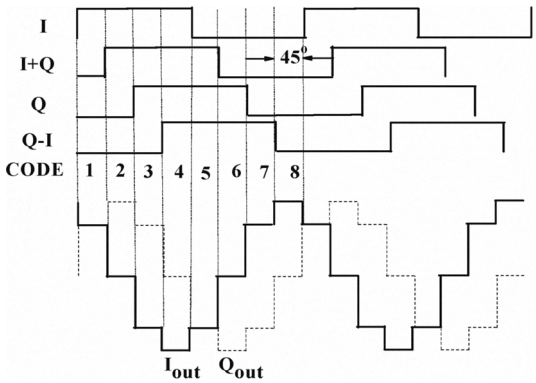

Fig. 5. Input and output timing diagram for 3 bit phase regeneration

B. Design Outline

The most important parameters are operating rate and

spurious of the regenerated signal. To ensure the former, the drive capability of switching data streams must be improved. The latter is determined by phase and amplitude ratio of the quantization states. In schematic, the circuit structure from input stages to switches is equal to each other and will never induce differences among switching date streams in time. But in layout, the parasitic effect will make these data streams asynchronously. So keep the length of signal wires approximately equal and the entire weighted current source must adopt common-centroid layout to satisfy strict matching request. Simultaneously, to avoid amplitude compress of the regeneration signals under the common mode voltage, a tradeoff between pull-up resistor and bias voltage of current source should be carefully considered. All the input and output interface obey standard LVDS transmission mode exclude analog input.

C. Realization

The 3 bit phase digitizing DAC is implemented in standard semiconductor technology. The die size is 1.57 mm × 1.60 mm, as shown in Fig.6.

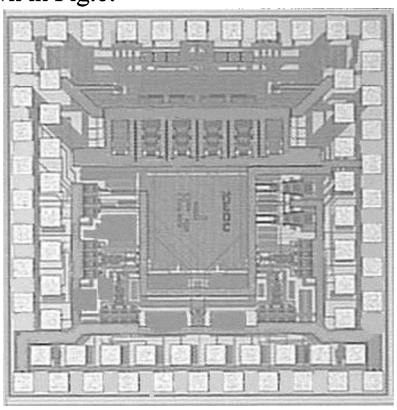

Fig.6. DAC Chip photograph

IV. EXPERIMENTAL RESULTS

Cascade connection of ADC and DAC is convenient for test ,so ADC and DAC are both assembled in 64-pin CQFP and then fixed on the PCB for all tests.. Excluding output buffers but including demultiplexer and clock buffer, ADC consumes about 350mW at 3.4GS/s sampling rate. The core power dissipation of DAC is about 300mW including multiplexer and clock buffer at 3.4GS/s sampling rate. Fig 7 shows the waveform and spectrum of DAC at 3.4GS/s sampling rate and 123MHz analog input signal. The SFDR of DAC is -16.98dBc and the worst-case harmonic is the seventh, which is coincident with the phase digitizing principle [3].

At 2GS/s sampling rate, test typical input amplitude point as the frequency increased from 100KHz to 250MHz. The SFDR of DAC output as a function of input frequency is shown in Fig 8. Take SFDR≥-12dBc as the criterion, test results show that ADC and DAC can work at 3.4GS/s sampling rate, the IBW of the DRFM cover them is high than 250MHz, and the dynamic range is wider than 20dBc. The IBW is much lower than the Nyquist frequency because of the phase accuracy requirement of ADC mentioned in Section B, Part II.

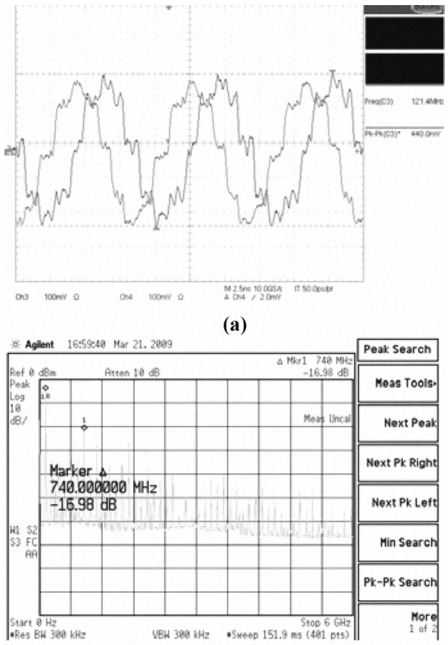

Fig.7. Test results of DAC output when both ADC and DAC working at 3.4GS/s sampling rate and the frequency of analog input is 123MHz (a) Waveform (b) spectrum

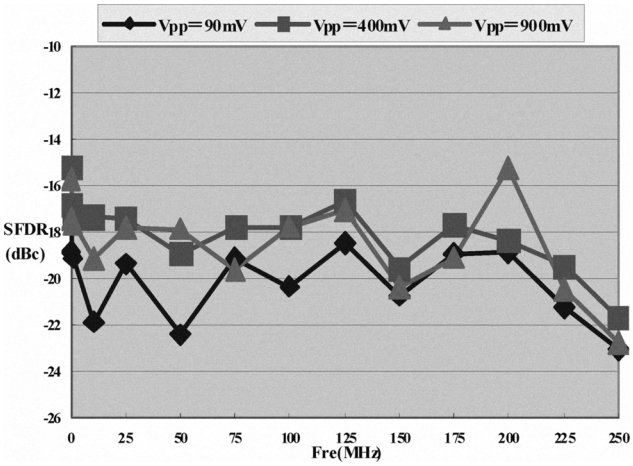

Fig.8. SFDR of DAC output as a function of input frequency

V. CONCLUSION

3.4GS/s 3 bit phase digitizing ADC and DAC for DRFM is implemented in standard semiconductor technology. The core power dissipation of ADC and DAC is about 350mW and 300mW, respectively. Take SFDR of DAC output higher than -12dBc as the criterion, ADC and DAC can work at 3.4GS/s sampling rate, the IBW of the DRFM cover them is high than 250MHz, and the dynamic range is wider than 20dBc. Test results show that the minimum limitation of the dynamic

range is about 90mV which is larger than the simulation results. The most probably reason is the electromagnetic interference (EMI) on the PCB. A wider dynamic range will be obtained by meliorate the test board.

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