RF-to-Baseband Digitization in 40 nm CMOS With RF Bandpass $\Delta\Sigma$ Modulator and Polyphase Decimation Filter

Ewout Martens, *Member, IEEE*, André Bourdoux, *Member, IEEE*, Aissa Couvreur, Robert Fasthuber, *Student Member, IEEE*, Peter Van Wesemael, Geert Van der Plas, *Member, IEEE*, Jan Craninckx, *Senior Member, IEEE*, and Julien Ryckaert, *Member, IEEE*

***Abstract*—A fourth-order continuous-time RF bandpass $\Delta\Sigma$ ADC has been fabricated in 40 nm CMOS for $f_s/4$ operation around a 2.22 GHz central frequency. A complete system has been implemented on the test chip including the ADC core, the fractional-N PLL with clock generation network, and the digital decimation filters and downconversion (DFD). The quantizers of the ADC are six times interleaved enabling a polyphase structure for the DFD and relaxing clock frequency requirements. This quantization scheme realizes a sampling rate of 8.88 GS/s which is the highest sampling speed for RF bandpass $\Delta\Sigma$ ADCs reported in standard CMOS to date enabling high oversampling ratios for RF digitization without compromising power-efficient implementation of the DFD. Measurements show that the ADC achieves a dynamic range of 48 dB in a band of 80 MHz with an IIP_3 of 1 dBm.**

***Index Terms*—Analog-to-digital converters, continuous-time $\Delta\Sigma$ modulation, decimation, polyphase filter, RF bandpass filters, RF digitization, software receiver.**

I. Introduction

THE STRONG growth in wireless applications and services in versatile environments is a driving force behind the development of flexible wireless transceivers. Innovative architectures should deliver low-cost solutions for mobile handsets that need to cope with various wireless standards like LTE/LTE Advanced, IEEE 802.11a/b/g/n/ac and Bluetooth. The availability of high-speed digital circuitry in deep-submicron technologies enables the use of digitally-intensive radio architectures for these applications.

Whereas earlier generations of receivers are dedicated to one or a few standards (e.g., see [1]), the paradigm of the *software-defined radio* (SDR) allows to implement a reconfigurable multistandard receiver [2]. By implementing flexible RF and analog building blocks for the signal conditioning and channelization, the radio can be programmed into different modes covering a wide frequency range [3]. As illustrated in Fig. 1, a *software receiver* shifts the functionality of these RF and analog parts completely toward the digital front-end (DFE) to maximally benefit from the computing possibilities offered by the technology scaling. The ideal software receiver should digitize the complete spectrum, enabling simultaneous reception of different channels within the same or different frequency bands [4]. Whereas implementation of this ideal software receiver with limited power consumption is not achievable with currently available technology, a *direct RF digitizer* makes the concept more realizable by directly converting one RF band to a digital baseband signal. Since all channels in the band are processed in parallel, the direct RF digitizer can be used as a multimode multistandard receiver for all wireless standards using a common RF band. To address multiple bands, several direct RF digitizers are placed in parallel to form a *digital-RF receiver* [5].

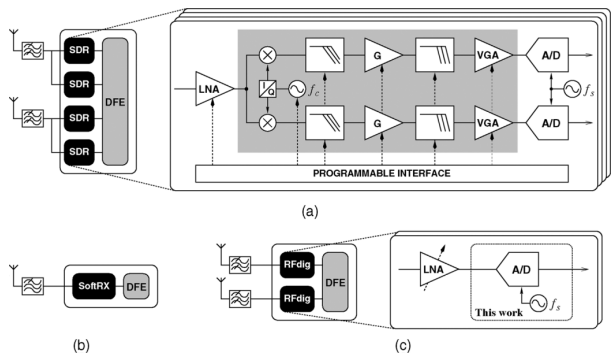

Fig. 1. (a) Receiver architectures based on the concept of software-defined radio. (b) Ideal software receiver. (c) Direct RF digitizer.

The benefits of digital processing come at the cost of tough requirements for the analog-to-digital converter (ADC). To detect signals with enough accuracy in the presence of in-band interferers, a large dynamic range and high linearity are indispensable. Wide-band operation is needed to cover the entire RF band resulting in a high-speed ADC. Whereas state-of-the-art flash ADCs can sample at GHz speeds, their limited resolution to 5–6 bit [6] makes them unsuited for direct RF digitization. Other ADC types like pipeline [7] or successive approximation [8] ADCs offer a higher resolution but at a much lower sampling rate. Subsampling could be employed but to avoid too much performance degradation due to noise aliasing, a high-quality bandpass (BP) anti-aliasing filter is needed [9].

The most promising type of ADC for the use in a software receiver is a continuous-time (CT) BP $\Delta\Sigma$ modulator [10] oper-

Manuscript received August 26, 2011; revised November 18, 2011; accepted December 10, 2011. Date of current version March 28, 2012. This paper was approved by Guest Editor Makoto Nagata. This work was supported in part by the European Union's Seventh Framework Programme (FP7/2007–2013) under Grant 248277.

The authors are with IMEC, 3001 Leuven, Belgium (e-mail: Ewout.Martens@imec.be).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/JSSC.2012.2185149

TABLE I
COMPARISON OF CONTINUOUS-TIME HIGH-SPEED BANDPASS ΔΣ ADCS WITH G_m-*LC* FILTERS

	[13]	[14]	[15]	[16]	[17]	[18]	[19]	[20]	This work
Topology	4^{th}-order	4^{th}-order	4^{th}-order	6^{th}-order	2^{nd}-order	4^{th}-order	6^{th}-order	2^{nd}-order	4^{th}-order
PLL/DFD	no	no	no	no	no	no	no	PLL	PLL+DFD
Technology	0.5 μm SiGe	0.25 μm SiGe	130 nm SiGe	90 nm CMOS	130 nm CMOS	40 nm CMOS	180 nm CMOS	130 nm CMOS	40 nm CMOS
Center Freq.	1 GHz	950 MHz	2 GHz	2.4 GHz	2.442 GHz	2.44 GHz	200 MHz	1.924 GHz	2.22 GHz
Clock Freq.	4 GHz	3.8 GHz	40 GHz	3 GHz	3.256 GHz	6.1 GHz	800 MHz	3.2 GHz	8.88 GHz
Mode	$f_s/4$	$f_s/4$	$f_s/20$	$4f_s/5$	$3f_s/4$	$2f_s/5$	$f_s/4$	$3f_s/5$	$f_s/4$
SNDR	37 dB	59 dB	52 dB	40 dB	34 dB	41 dB	68.4 dB	40 dB	42 dB
SFDR	48 dB	—	61 dB	62 dB	32 dB	65 dB	—	42 dB	50 dB
DR	40 dB	—	53 dB	—	—	43 dB	70 dB	—	48 dB
Bandwidth	20 MHz	1 MHz	120 MHz	60 MHz	25 MHz	80 MHz	10 MHz	1 MHz	80 MHz
IM_3	—	-62 dB	-59 dB	-51 dB	-25 dB	—	-73.5 dB	—	-52 dB
IIP_3	1 dBm	—	4 dBm	-9 dBm	—	-5 dBm	—	-7 dBm	1 dBm
Power ADC	450 mW	75 mW	1600 mW	40 mW	26 mW	52.8 mW	160 mW	30 mW	164 mW
Area	1.36 mm^2	1.08 mm^2	$\sim$1 mm^2	0.8 mm^2	0.27 mm^2	0.4 mm^2	2.5 mm^2	2.3 mm^2	0.4 mm^2
FoM [pJ/conv.]	194.5	51.5	20.5	4.1	12.7	3.6	3.7	183.6	10.0

ating at RF frequencies. A high-speed low-resolution flash converter is put inside a loop with an RF BP filter with a bandwidth large enough to embrace the complete RF band. With the high oversampling ratio (OSR) realizable in deep-submicron technologies, a high resolution is obtained within the RF band. By providing some tuning of the center frequency of the filter, the band of interest can be adjusted. Further, the filter acts as an inherent antialiasing filter.

In this work, a CT BP ΔΣ ADC is realized using a standard 40 nm CMOS process. The modulator digitizes a signal bandwidth of 80 MHz centered around 2.22 GHz with a clock frequency of 8.88 GS/s. With this high sampling speed, the architecture benefits from a high OSR but power-efficient implementation of the digital postprocessing and low-jitter clock generation becomes challenging. To address these issues, this design does not only focus on the ΔΣ modulator, but realizes a fully integrated system including the core ΔΣ ADC, a phase-locked loop (PLL), and the digital filtering and downconversion (DFD) stages. This paper extends the article presented in [11]. By application of the power-aware evaluation flow of [12] for the DFD design, the first implementation and feasibility of such a design is demonstrated.

The rest of this paper has been organized as follows. Section II reviews designs of RF ADCs reported in literature. An overview of the architectural choices made in this work is given in Section III. Details of the circuits of the ΔΣ modulator and of the DFD implementation are presented in Sections IV and V, respectively. Section VI summarizes the experimental results obtained from the chip implementation. Finally, conclusions are drawn in Section VII.

II. OVERVIEW OF RF ADCS

Over the last years, several RF BP ΔΣ ADCs have been reported [11], [13]–[20]. As shown in Table I, to realize the operation at high frequencies, CT modulators with an G_m-*LC* loop

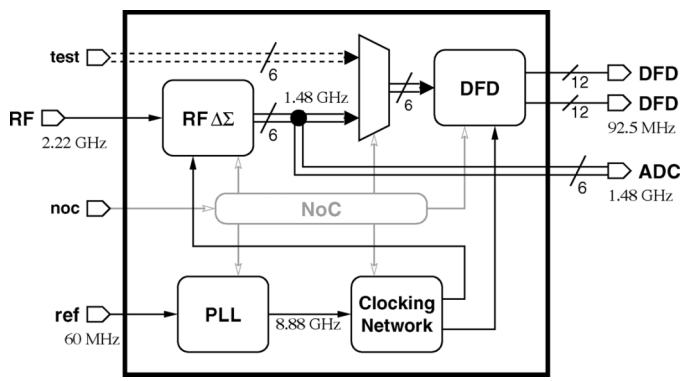

Fig. 2. Schematic representation of the complete system and its different components implemented in this work.

filter are adopted. A tunable tank capacitor enables a reconfigurable center frequency. To obtain a high resolution within a large bandwidth, a high OSR is required. Chalvatzis *et al.* [15] uses a sampling frequency of 40 GHz resulting in a signal-to-noise-and-distortion ratio (SNDR) of 52 dB in a 120 MHz band and a power consumption of 1.6 W. Lower clock frequencies f_s have been used in [13] and [14] to realize BP ΔΣ ADCs with center frequencies at $f_s/4$ of about 1 GHz. Cherry *et al.* [13] achieve a mere 37 dB in a band of 20 MHz whereas the SNDR in [14] is 59 dB within a limited bandwidth of 1 MHz. Furthermore, all these high sampling frequencies are realized in non-CMOS processes.

To realize RF BP ΔΣ ADCs in a standard CMOS process, subsampling techniques have been adopted [16], [17], [20]. Whereas prior designs had a fourth-order loop filter [13]–[15], Ryckaert *et al.* [16] compensate for the lower OSR with a sixth-order BP filter. This first CMOS RF BP ΔΣ ADC achieves 40 dB with a bandwidth of 60 MHz. Designs with only a second-order BP filter suffer from limited resolution or from a small bandwidth: Beilleau [17] *et al.* reports 34 dB

over 25 MHz whereas the design of [20] has a bandwidth of only 1 MHz. A high resolution of 68 dB is obtained by Lu *et al.* [19] in a 10 MHz band but at a moderate central frequency of 200 MHz. The currently highest bandwidth for an RF BP $\Delta\Sigma$ in CMOS is 80 MHz with an SNDR of 41 dB, reported by Ryckaert *et al.* [18].

As an alternative for RF bandpass $\Delta\Sigma$ ADCs, $\Delta\Sigma$ modulators which employ subsampling in the loop, have been proposed. Namdar *et al.* [21] uses a mixer followed by a lowpass (LP) loop filter. To reduce the errors of the sampler, the subsampler can be placed after a BP loop filter combined with an upconversion of the feedback signal either by a mixer [22] or by a high-speed digital-to-analog converter (DAC). This was proposed by Naderi *et al.* [23]. In [24], a $\Delta\Sigma$ modulator has been implemented with a combination of a LP and BP filter with a mixer between them and a DAC at full speed. The receiver of Winoto *et al.* [25] is a second-order $\Delta\Sigma$ loop with passive I/Q-downconversion mixers as first stage of the loop filter. A direct $\Delta\Sigma$ receiver has been demonstrated by Koli *et al.* [26] which use passive mixers to realize a fourth-order $\Delta\Sigma$ loop with a resonator, an I/Q-downconversion integrator and a second-order complex LP modulator. It achieves an SNDR of 56 dB in a 9 MHz bandwidth around 900 MHz. The main disadvantage of these frequency-translating loops is the folding of the noise inside the signal band. To limit this noise leakage from other frequencies, extra filtering or careful selection of the sampling and oscillator frequencies is required. Further, the nonlinearity of a mixer in the feedback path or in front of the loop filter degrades the SNDR.

Time-interleaved ADCs base on voltage-controlled oscillators (VCOs) have been suggested as yet another alternative for RF BP $\Delta\Sigma$ modulators [27]–[29]. Due to the first-order noise shaping, these systems suffer from a limited resolution or bandwidth. The most recent realization is the digitally-intensive system of Kim *et al.* [29] with a peak SNDR of 51 dB in a band of 10 MHz.

Finally, Lachartre [30] proposes an asynchronous RF BP quantizer as alternative for RF BP $\Delta\Sigma$ modulators. To complete the digitization, however, a sampling operation after the quantizer is still required. This operation causes noise folding and degrades the performance.

III. Architecture Overview

A. Overall System

Fig. 2 shows the different components of the system that has been implemented in this work. The RF input signal in an 80 MHz band around 2.22 GHz is converted by the RF $\Delta\Sigma$ ADC to 6 parallel bit streams each at 1.48 GHz. In contrast to previous demonstrators of RF BP ADCs [13]–[20], a DFD block has been added. It realizes the processing of the high-speed data including the shaped quantization noise of the $\Delta\Sigma$ modulator: downconversion to baseband, filtering and decimation. The DFD output is a 2×12-bit I/Q data stream at 92.5 MHz which provide an interface with a standard DFE. A multiplexer allows to directly feed data into the DFD for testing purposes. Further, a PLL is integrated on the chip to generate the 8.88 GHz sampling clock from a 60 MHz reference signal. The clocking network converts this signal to the different clock signals needed in the system. Finally, a network-on-chip (NoC) is used to reconfigure the system.

B. RF Bandpass $\Delta\Sigma$ Modulator

A more detailed schematic of the RF continuous-time bandpass $\Delta\Sigma$ modulator is depicted in Fig. 3. The loop filter is a fourth-order G_m-LC filter with a feedforward path. Although a higher-order filter would increase the resolution of the converter, it also considerably increases both area and power. For example, the sixth-order filter used in [16] requires four inductors and transconductances to stabilize the $\Delta\Sigma$ feedback loop. The center frequency f_c of the resonators is 2.22 GHz. By choosing a clock frequency of $4f_c = 8.88$ GS/s, the OSR becomes 55.5 for a signal band of 80 MHz. Despite the limited order of the loop filter, this high OSR should provide a high resolution.

To realize this high sampling speed in standard CMOS, six quantizers are interleaved. Hence, each operates at 1.48 GHz. A three-level quantization has been adopted as a compromise between a slightly higher SNDR and possible linearity problems of multibit DACs [10]. The parallel outputs of the 12 comparators are fed into the polyphase downconversion filter of the DFD.

The feedback signal is generated by a 1.5-bit DAC operating at the full speed of 8.88 GHz. To limit the SNDR degradation due to clock jitter [31], and to simplify high-speed circuitry, nonreturn-to-zero rather than return-to-zero pulses are preferred for the DAC. Its input signal is generated by multiplexing the outputs of the comparators in two steps. A retiming operation between the two multiplexers at half the clock speed is used to minimize the impact of comparator metastability and relax timing constraints.

To ensure stability in presence of excess loop delay, various compensation techniques exist, which add extra feedback paths [32] resulting in extra power-hungry addition operations at RF frequencies. Instead, a variable delay line (τ in Fig. 3) has been added to vary the loop delay. The minimum loop delay needed for negative feedback while providing enough time for all operations in the feedback path has been determined using a similar Z-domain analysis as in [16]. A margin of 4 feedback clock cycles is needed to stabilize the loop while taking the comparator latency into account and giving enough time for the multiplexing operation. Variation of the loop delay is better not placed on the DAC clock as it might introduce extra unwanted jitter on the feedback signal. Therefore, it is the clock fed to the quantizers which is delayed meaning that more delay actually shortens the loop delay.

With the NoC, the center frequency, the quality factor and the gain of the resonators, the threshold levels of the 1.5-bit quantizers, and the output levels of the DAC are tuned for reconfigurability and calibration.

C. DFD

1) Functionality and Reference Architecture: The DFD is fed by the BP $\Delta\Sigma$ ADC output, which is a digitized RF signal with a bandwidth of 80 MHz, centered at 2.22 GHz and sampled at a rate of $f_s = 8.88$ GS/s with a resolution of 1.5 bits. After processing, the DFD must output the useful signal downconverted

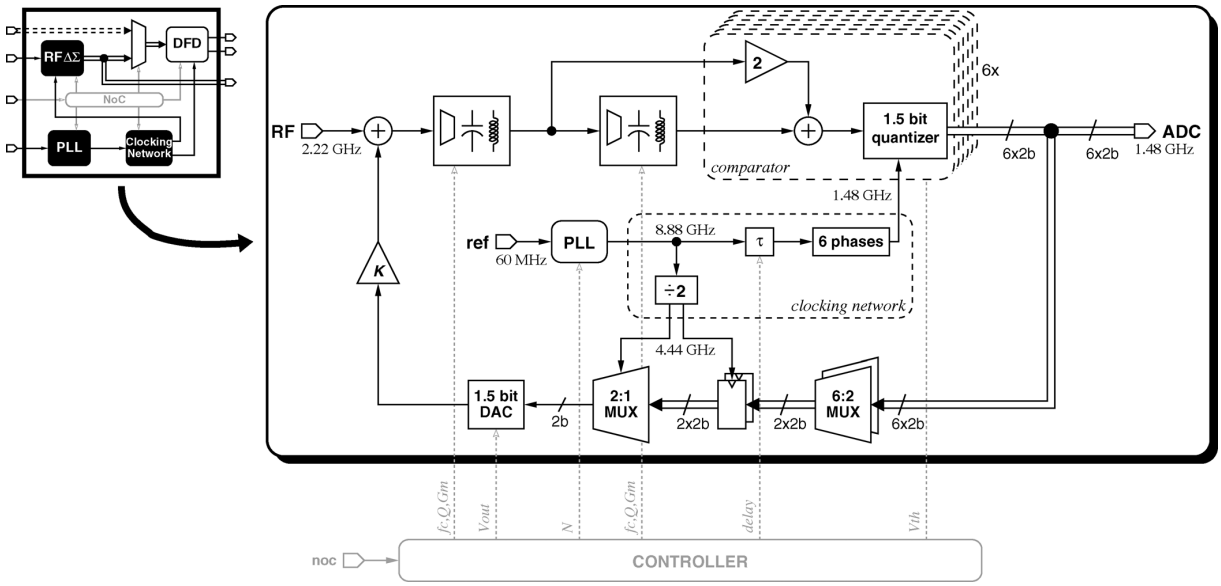

Fig. 3. Architecture of the continuous-time bandpass ΔΣ modulator.

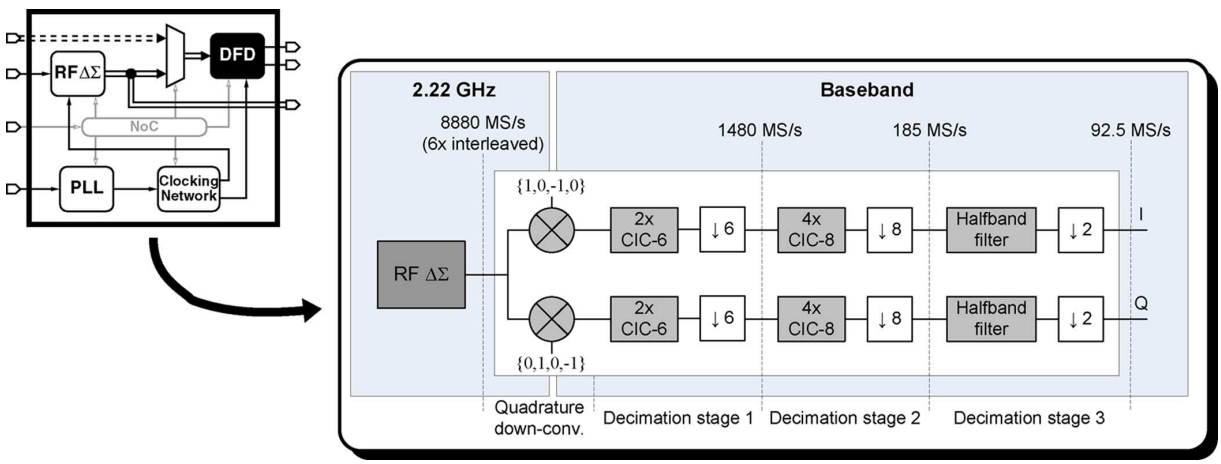

Fig. 4. Reference architecture of DFD.

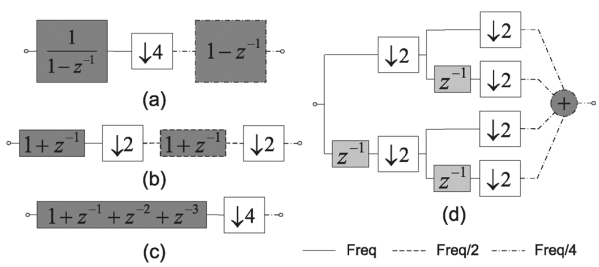

Fig. 5. Functionally equivalent implementation options of a 1xCIC-4 filter.

to baseband (-40 to $+40$ MHz), with 9 bits of resolution and downsampled to $f_s/96 = 92.5$ MS/s. Based on these specifications, the reference architecture shown in Fig. 4 was derived. It comprises the following elements:

- A quadrature mixer to baseband, with the frequency of the local oscillator (LO) set to exactly a quarter of the sampling rate. Hence, the real and imaginary values of the LO are from the set $\{1, 0, -1, 0\}$, which greatly simplifies the implementation cost of the downconversion step. This is now just an add/subtract with simple logic instead of a costly multiplier and a digital oscillator.
- Lowpass filter stages with cascade integrator-comb (CIC) filters and decimation by 48. CIC filters have all the coefficients equal to 1, thus no multiplication is involved. In order to achieve the required attenuation before decimation, the first decimation (by 6) is preceded by the cascade of two CIC-6 filters and the second decimation (by 8) is preceded by the cascade of four CIC-8 filters.
- A final lowpass filter with a finite-impulse response (FIR) half-band filter (HBF) and a decimation by 2. The half-band filter provides a better rejection of out-of-band noise and is computationally efficient because about half of the filter coefficients are zero, whereby only about half of the multiplications are required.

2) Considered Architecture Options: The reference architecture of Fig. 4 is, however, not optimal from an implementation point of view. For instance, the very high input sample rate would lead to a high power consumption. To tackle this problem, we modified the reference architecture and obtained

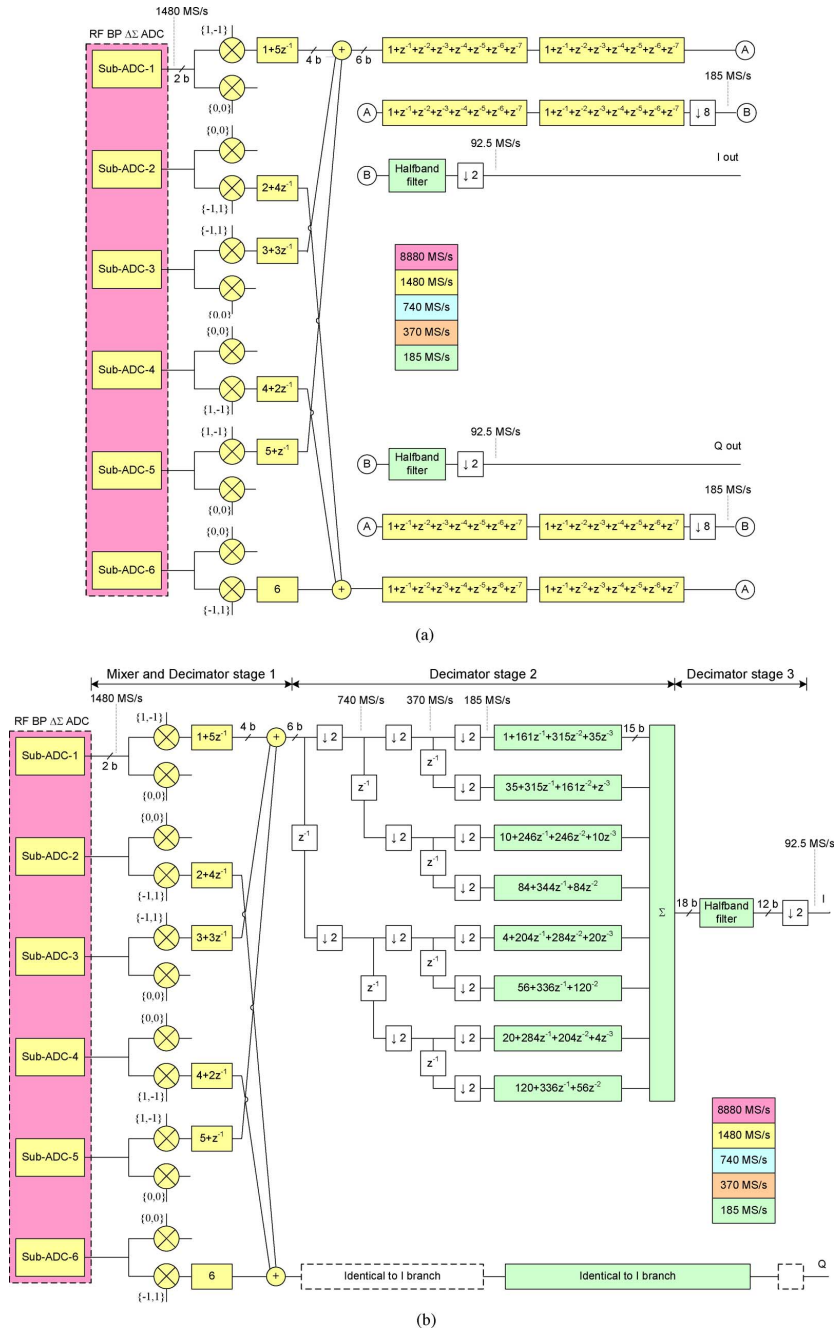

Fig. 6. Block diagram of two architecture options for the DFD. Different clock regimes are highlighted in different colors. (a) Architecture A. (b) Architecture E.

several architectures that are *exactly* equivalent at the functional level but have different area footprint and power consumption. The three main concepts that we used to modify the reference architecture are as follows:

- Exploitation of the polyphase concept [33] to implement filtering + decimation but also—and this is very uncommon—to implement mixing + decimation.
- Exploitation of the inherent interleaved ADC architecture. The ADC output comes from six subADCs sampled at one-sixth of the input sampling rate. Hence, it is much more economical to exploit the polyphase structure directly and use six independent paths at the downsampled rate. Not only does this result in simplified CIC-6 filters but also half of the mixer output branches are always zero, thereby reducing the downconversion complexity by half. This is visible in Fig. 6 were mixer 1, 3, and 5 have purely real outputs, summed into the I branch, and mixer 2, 4, and 6 have purely imaginary outputs, summed into the Q branch.
- The combination of the CIC filters and the decimators can be implemented in many different ways. As an illustration, Fig. 5 shows four exactly equivalent structures for a CIC-4 obtained through different algebraic transformations of the filter transfer function [34]: 1) is the typical CIC structure proposed in [35]; 2) is a nonrecursive structure that combines multiple stages of FIR comb filter followed by a decimation-by-2; 3) is a nonrecursive structure that combines

an initial FIR Comb filtering stage with a final decimation; and 4) shows the polyphase decomposition [34] of structure 3). Note that 2) is only possible for a decimation factor that is an integer power of 2.

Besides, within a given filter structure, multiple factorizations of the coefficient multiplications are possible and different pipelining schemes are possible for a given factorization choice. As a result, a particular DFD architecture, such as the one illustrated in Fig. 4, can be transformed into a large number of functionally equivalent implementations.

Seven functionally equivalent architectures—referred to as architecture "A" to "G"—are considered for implementation. They are summarized below together with the main concept(s) that they exploit:

- **A**: 6-(d) 2xCIC-6 + (c) 4xCIC-8 + HBF;
- **B**: 6-(d) 2xCIC-6 + (a) 4xCIC-8 + HBF;
- **C**: 6-(d) 2xCIC-6 + (b) 4xCIC-8 + HBF;
- **D**: 6-(d) 2xCIC-6 + 4-(d) 4xCIC-4 + (b) 4xCIC-2 + HBF;
- **E**: 6-(d) 2xCIC-6 + 8-(d) 4xCIC-8 + HBF;
- **F**: 12-(d) (2xCIC-6 + 4xCIC-2) + (b) 4xCIC-4 + HBF;
- **G**: 24-(d) (2xCIC-6 + 4xCIC-4) + (b) 4xCIC-2 + HBF.

Because of lack of space, it is impossible to illustrate all the seven architectures. We will illustrate two of them to highlight the main tradeoffs. Architecture A is shown in Fig. 6(a). At the left, the six sub-ADCs drive six quadrature mixers with LOs running at one-sixth of the LO rate. Therefore, the LO values are either from the set $\{-1, 1\}$ or $\{0\}$ and only half of the output branches must be processed. The mixer outputs are filtered by two CIC-6 filter in nonfactorized form, filtered by 4 CIC-8 filters in factorized form, decimated by 8 and finally filtered by the HBF and decimated by two. In Architecture A, everything from the DFD input up to the HBF input runs at $f_s/6 = 1.48$ GS/s. In contrast, Architecture E [see Fig. 6(b)] uses the same mixing and CIC-6 filtering as Architecture A but implements the 4 CIC-8 and the decimation by 8 using the polyphase approach [see (d) in Fig. 5].

In the considered DFD structures, the first decimation stage takes advantage of the polyphase decomposition to lower the operation frequency. Note that the output of the ADC contains 1.5 bits at 8.88 GS/s and any digital design in current technology at this frequency incurs in significant overhead in both design time (full-custom logic may be needed) and power. So, by leveraging on a polyphase decomposition, this 8.88 GHz are lowered to 1.48 GHz for the A-E variant and even to 740 and 370 MHz for the F and G, respectively. A half-band filter (HBF) of 21 taps is common for all the DFD structures as a final decimation by 2 stage.

Fig. 7 shows the number of taps required by the considered DFD structures. Besides the variation on the absolute number of taps, the number of taps per input sampling rate is also shown. However no conclusion on the optimal implementation structure can be derived from this figure. The reason is twofold. Firstly, the complexity of the taps across implementation variants differs due to the different tap coefficients and different bit-width requirements. Some tap coefficients are 1s and thus instead of a constant multiplication a simple addition is used. Multiple common subexpression elimination (CSE) factorizations are also possible for the more complex taps. Besides, the DFD

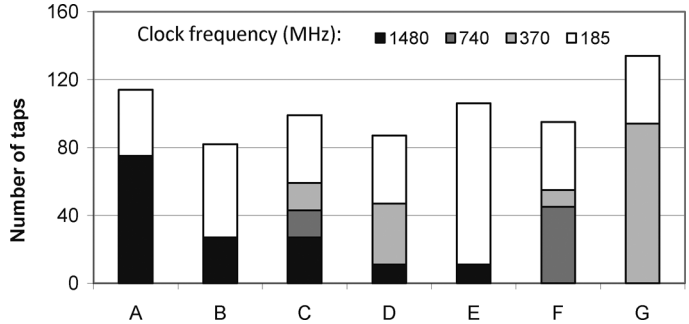

Fig. 7. Number of taps of the seven equivalent DFD structures.

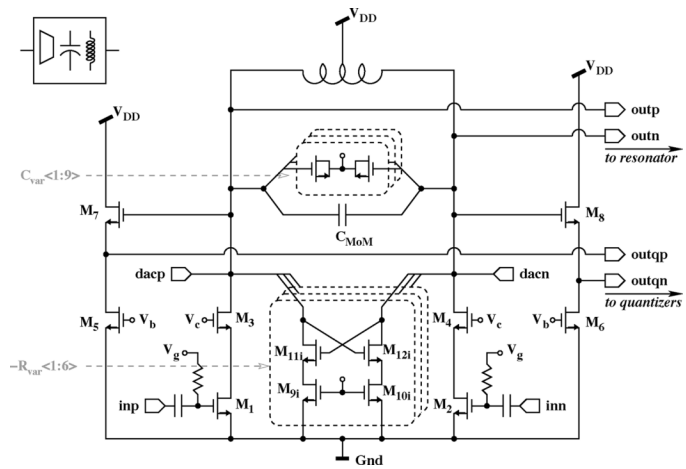

Fig. 8. Circuit schematic of a G_m-LC resonator.

input bit-width is 2 bits and throughout the processing grows up to 12 bits; this clearly has an impact on the tap complexity. Secondly, especially for high frequencies, the power consumption does not scale linearly with the frequency. Indeed, in case of high frequency operating conditions, the implementation technology requires significantly larger cells with high driving capability. As a result, beyond a certain frequency, the power consumption starts to grow exponentially. Another source of nonlinearity is the insertion of pipelining stages. Complex operations, such as constant multipliers are broken into multiple pipeline stages, which requires the insertion of extra registers. For those reasons, the selection of the best architecture for implementation requires an in-depth analysis, which will be exposed in Section V.

IV. Implementation of ΔΣ Modulator

A. Loop Filter

The circuit, used to implement both resonators of the loop filter, is shown in Fig. 8. The input transconductance consists of a cascoded pseudo-differential pair which can be tuned via bias voltage V_g. Thanks to this variability, the second resonator, which has relaxed noise requirements, can be biased with a lower current, thereby reducing its power consumption.

The resonator tank is built with 4 nH 4-turn differential inductors taken from the standard technology library in parallel with a MoM capacitor C_{MoM} and binary-weighted NMOS varactors to adjust the center frequency of the filter. Tunable nega-

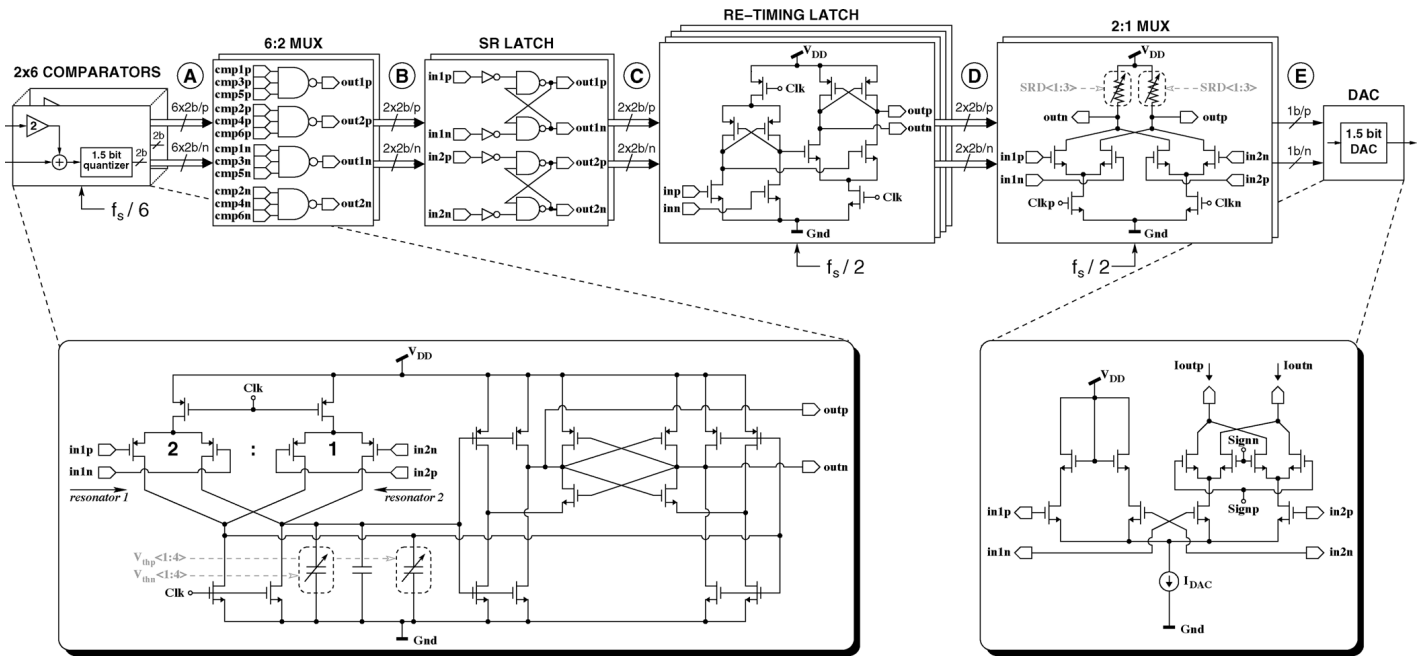

Fig. 9. Circuit schematics of the quantizers and the feedback path.

tive resistances made of cross-coupled NMOS pairs compensate for tank losses and enhance the quality factor. They can turn the negative resistance up to oscillation which allows the center frequency calibration of the resonator.

The output of the resonator tank is buffered by a source-follower before being fed into the quantizers. To minimize the loop delay, no buffering is inserted between the two resonators. As a result, the two resonators see a different load, which is compensated for by adjusting the value of C_{MoM} for the two resonators.

B. Quantizer and Feedback Path

The high sampling speed of the ADC requires a new approach for the feedback path compared to previous implementations [18]. Details of the circuits are shown in Fig. 9.

For the 1.5-bit quantizer, six 1.5-bit quantizers operating at $f_s/6$ are interleaved. Each subquantizer contains two comparators with different tunable threshold voltage resulting in two sets of six-times interleaved comparators. Their schematic is shown at the bottom of Fig. 9. The input consists of two PMOS input pairs in parallel. One pair is scaled with a factor two to embed the internal feedforward path of the loop filter inside the comparator core: the currents of the two paths are added before performing the regeneration. By avoiding an extra adder stage, loop delay is minimized and power consumption is reduced. To realize the three-level quantization, a built-in offset is created by an imbalance on the input pair as well as by adding a fixed MoM capacitor on one side of the output of the preamplifier. A binary-weighted capacitor bank on the preamplifier output nodes is used to adjust the threshold level for the comparator.

The duty cycle of the quantizer clocks is 33% which provides 1/3 of the time for comparison and the remaining for reset. Simulated waveforms are shown in Fig. 10. First signals Ⓐ are the (single-ended) comparator outputs of tile 1, 3 and 5 and the clock of the first one. During reset, both differential outputs

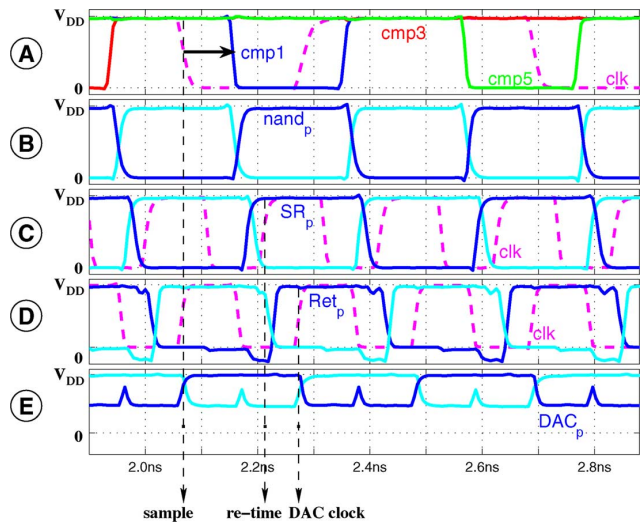

Fig. 10. Timing diagram of typical signals at different points in the feedback path of Fig. 9. The outputs of comparators 1 (0), 3 (1), and 5 (0) are first multiplexed before retiming and multiplexing with the outputs of the other comparators.

are pulled up to the supply voltage V_{DD} and in the comparison phase, the regeneration operation pulls down one of the two outputs depending on the input level. This allows performing a 6-to-2 multiplexing by NANDing three nonoverlapping outputs from the interleaved comparators with two outputs in the reset phase during the comparison of the third one. The resulting differential signals are shown in the second plot of Fig. 10 Ⓑ.

The multiplexed output streams of the NAND gates are latched by a Set-Reset (SR) latch Ⓒ and then retimed by a high-speed flip-flop to remove the effect of quantizer metastability. The multiplexing in two steps enables a retiming operation at half the clock speed. The corresponding differential signals as well as the clock signal are depicted in Fig. 10 Ⓓ

The two interleaved streams are then multiplexed again by multiplying them with an $f_s/2$ clock signal which is 90° out of phase with the retiming clock. When the clock is high, the first data stream is selected whereas the second one is taken when the clock is low. The multiplication is performed by a 4-quadrants multiplier with a tunable resistor as load. Hence, the signals are not full swing anymore as illustrated on the last plot Ⓔof Fig. 10 and the multiplier acts as a swing-reduced driver (SRD) ensuring the DAC switches remain in saturation.

The DAC uses a switched NMOS current source topology as shown at the bottom of Fig. 9. For proper dynamic behavior of the common source node, a zero path allows bypassing the tail current to the supply. The DAC switching transistors are cascoded with static switches that allow to open the loop or change the sign of the feedback.

C. PLL and Clocking Network

The high-frequency fractional-N PLL generates the 8.88 GHz clock on-chip from an input 60 MHz reference signal. This PLL is identical to the one used in the SDR of [36]. Implementation details can be found in [37]. It contains a high-band and low-band VCO to cover a frequency range of 6.2 up to 12.6 GHz where the required sampling frequency falls in the range of the low-band variant. The PLL has a measured integrated phase noise of -25 dBc.

The 8.88 GHz signal from the PLL is fed into the clock generation circuitry which generates all clocking signals needed in the quantizers and feedback path of Fig. 9. For the DAC and retiming latches, the 8.88 GHz clock is divided by two as shown in Fig. 3. For the six-phase clock signal of the comparators, the input clock is first delayed using a variable delay line made of digitally programmable NMOS capacitors which are used to stabilize the ΔΣ loop as explained in Section III.B. The delayed clock is then applied to a synchronous delay line loop made of 12 high-speed TSPC flip-flops [38] similar to the ring used in [18].

V. Implementation of DFD

As mentioned in Section III.C, several functionally-equivalent architectures have been selected as candidates for implementation. In this section, the architecture with the lowest relative power consumption is determined and selected.

A. Applied Evaluation Flow

In order to avoid the effort of implementing all considered architecture candidates, we apply a high-level power-aware evaluation flow to enable an early relative comparison [12]. In the following a summary of the applied flow, which is depicted in Fig. 11, is provided.

1) Coefficient Quantization: In this step the filter coefficients are converted from floating-point to fixed-point representation. Thereby, for a defined SNR degradation budget, the word lengths of the coefficients are optimized. For the complete DFD, including all coefficients and signals, the maximal acceptable SNR degradation was defined to be 0.1 dB.

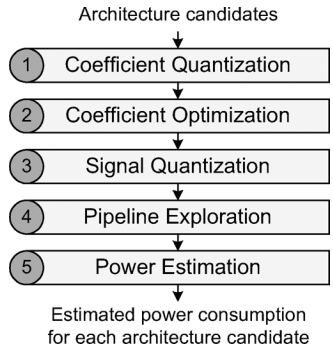

Fig. 11. High-level power-aware evaluation flow.

2) Coefficient Optimization: Since the coefficients of the filters are constant, costly multipliers can be replaced with series of shifts and additions/subtractions. Shifts are hardwired and require therefore no combinational logic. The number of required adders/subtracters for a multiplication is determined by the number of nonzero bits of the coefficient. To reduce the number of nonzero bits and hence the implementation cost, the canonical signed digit (CSD) representation of coefficients is considered. The CSD representation leads on average to a 33% lower number of nonzero bits compared to the 2's complement representation [39]. To further optimize the implementation cost, the joint optimization of multiple constant multiplications is considered. The CSE can be applied when a signal is multiplied with several constant coefficients. This is the case when filters with transposed-form structure are used.

3) Signal Quantization: At this step the fixed-point representations for all signals of the data-flow graph (DFG) are determined. This is done in 2 phases: In the first phase, based on the dynamic range growth, the required numbers of Most Significant Bits (MSBs) are calculated. In the second phase, based on the SNR degradation budget, the required numbers of Least Significant Bits (LSBs) are calculated. The final word length is then circumscribed based on the results of both phases.

4) Pipeline Exploration: In order to meet the targeted clock frequency and to optimize the implementation cost, pipeline registers may have to be inserted. Especially because of the previously applied transformations, the DFG of the design and the word length of the signals may be irregular. Therefore the optimal locations for pipeline registers are typically not obvious. During this step, possible locations for the pipeline registers are explored and evaluated. Thereby cost models of components, which show the tradeoff between delay and power for different word lengths, are used. To obtain these cost models, the generic VHDL description for each component (i.e., add, sub and register) was synthesized, placed and routed for different parameters of the tradeoff space.

5) Power Estimation: During this last step, the total power consumption of the architecture is estimated. This computation is essentially a summation of the power consumptions of all components. The estimation mainly neglects 1) the effect of global synthesis, placement and routing, 2) the actual switching activities and 3) the overhead of clock generation, clock tree and

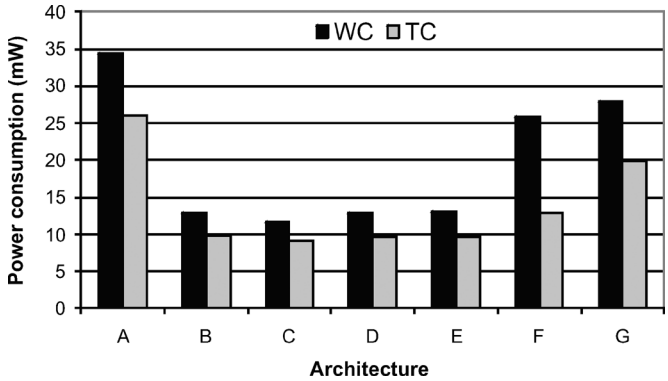

Fig. 12. Estimated worst case (wc) and typical case (tc) power consumption for each considered architecture variant.

test circuits. However, for a relative comparison, the introduced inaccuracies are typically acceptable.

B. Results of the Estimation Flow

The aforementioned evaluation flow has been applied for all 7 considered architectures using TSMC 40 nm LP LVT standard-cell technology. The power consumption was estimated for a realistic case (typical case) and for a conservative case (worst case). Both cases differ in selected process corner, temperature corner, switching activity and load at the output of the components. For each of the 7 architecture variants, the implementation with the lowest power consumption was selected. Fig. 12 shows the results of this estimation. The power consumption of all variants varies significantly: architecture A has an estimated worst-case power consumption of 34.4 mW whereas the estimation for architecture C is only 11.7 mW. This motivates the evaluation of the different architecture variants. Interestingly, although the structures are different, the power consumptions of the variants B-E are rather similar.

C. Implemented Architecture

The variants B-E consume the lowest power and are therefore the most interesting ones for implementation. To make a decision between these four architectures, the operating frequency was taken into account. Because most components operate at a low clock frequency, architecture E was finally selected for implementation. The selected DFD architecture, which is shown in Fig. 6(b), has been implemented in VHDL, synthesized with Synopsys Physical Compiler, and placed and routed with Cadence SoC Encounter. The power simulation with realistic stimuli reveals the following breakdown: 16% are consumed in the mixer and decimator stage 1, 36% are consumed in the decimator stage 2 and 48% are consumed in the decimator stage 3.

VI. Measurement Results

The total system was implemented in a 40 nm LP CMOS technology. This technology has been chosen for the low power and low leakage aspects, as the DFD design is "always on" and lacks clock gating possibilities.

As visible on the chip microphotograph in Fig. 13, there are two arrays of IO PADs inside the chip to facilitate the characterization of the system. Three different measurement set-ups are used. The first one evaluates the RF $\Delta\Sigma$ modulator alone using the comparator outputs available at the top part of the inner IO PADs. The second one uses the bottom array of PADs to apply the test signal of Fig. 2 and test the operation of the DFD. The final set-up just uses the outer IO PADs to characterize the complete system.

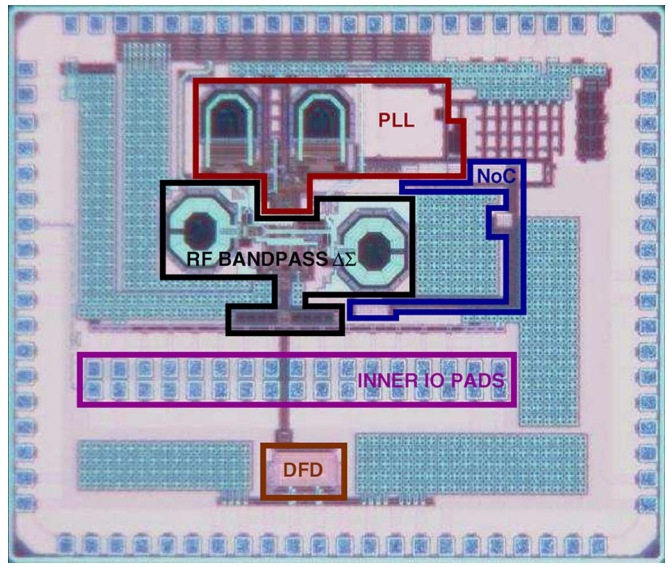

Fig. 13. Chip microphotograph.

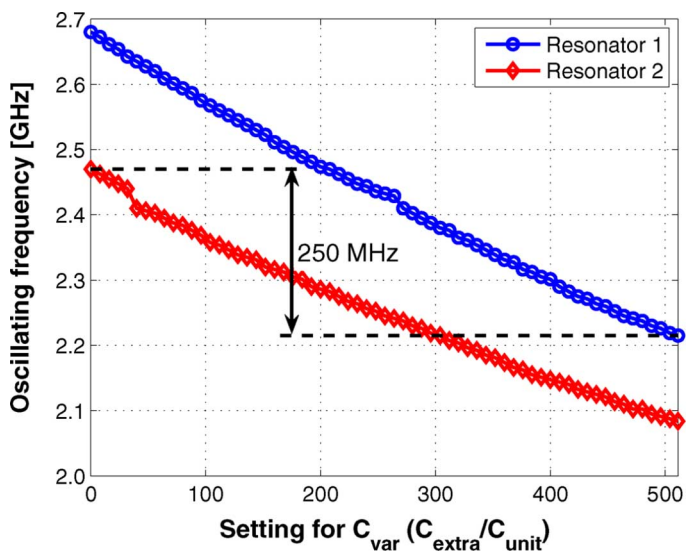

Fig. 14. Self-oscillating frequency of both resonators of the loop filter as a function of the varactor setting ($C_{unit} = 1.36$ fF).

By increasing the negative resistance in parallel with the resonator tanks, the resonators are individually put into oscillation to extract their center frequency from the open-loop transfer function. Fig. 14 shows the oscillation frequencies for different varactor settings for the two resonators. As can be observed, the asymmetric loading of both resonators results in a shift between the two curves, but both resonators can be aligned to a common center frequency over a range of 250 MHz around 2.35 GHz.

When the center frequencies of the resonators are tuned at 2.22 GHz, the negative resistance of both resonators is selected

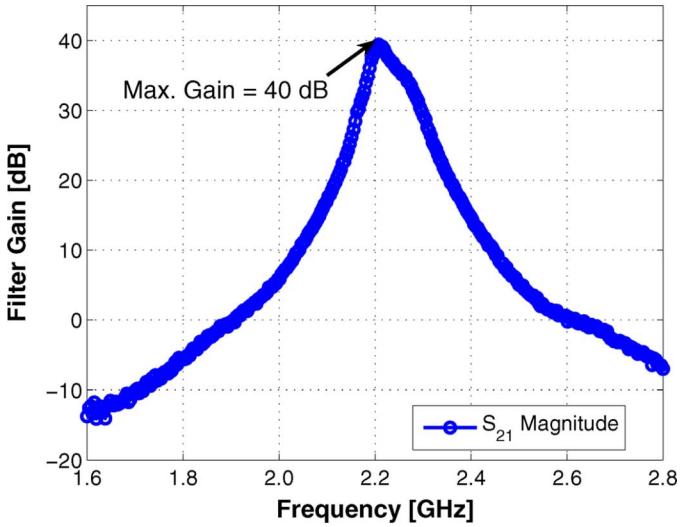

Fig. 15. Gain of the fourth-order loop filter around the center frequency $f_s/4 = 2.22$ GHz.

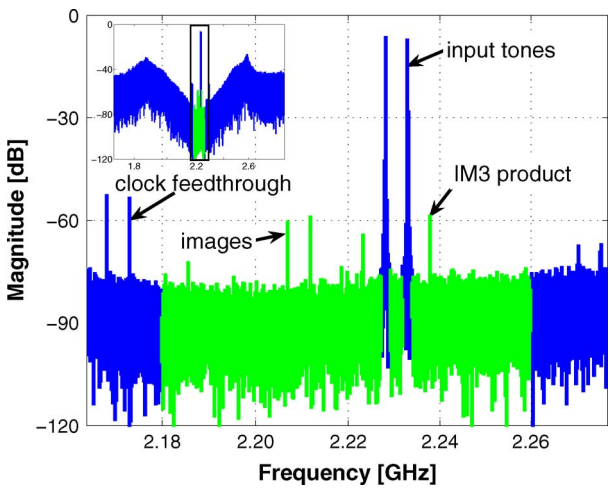

Fig. 16. Two-tones output spectrum of the RF BP ΔΣ ADC with details of the 80 MHz band around 2.22 GHz. In-band noise is denoted by a different color.

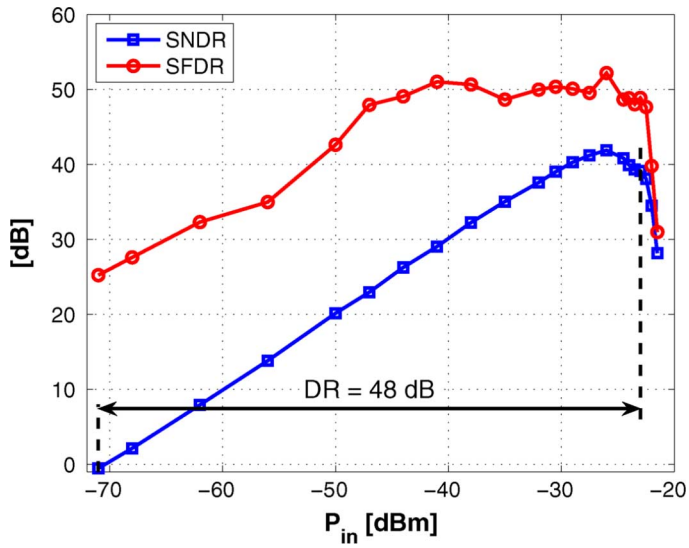

Fig. 17. Measured SNDR and SFDR of the RF BP ΔΣ ADC with two-tones RF input 5 MHz apart.

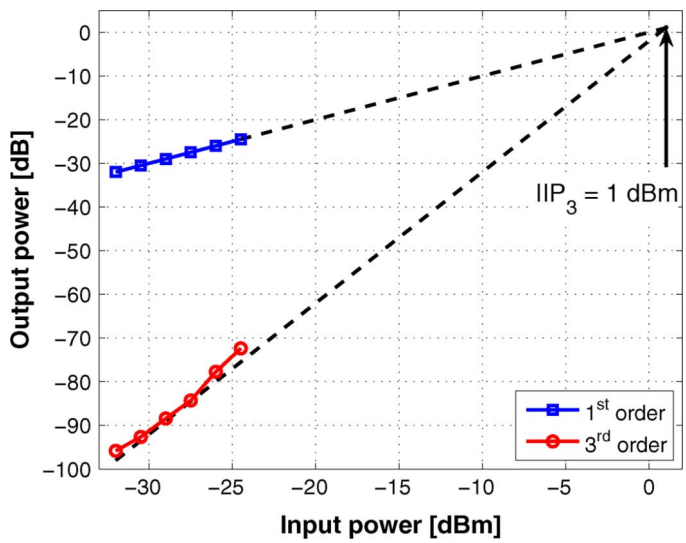

Fig. 18. Measurement of third-order distortion products with two RF input tones 5 MHz apart.

to obtain maximum gain without entering oscillation mode. The result is the open-loop transfer function of Fig. 15. A maximum in-band gain of 40 dB is achieved for the complete filter.

To evaluate the resolution of the RF bandpass ΔΣ ADC, two tones 5 MHz apart are applied at the RF input. The use of two tones is essential as it allows to evaluate distortion effects which otherwise would lie outside the band of interest in a single-tone test. Fig. 16 shows the 2^{21}-points FFT of the output of the comparators measured with a high-speed logic analyzer at maximum SNDR. As can be observed in Fig. 16, different spurious tones are present. First are the IM_3 products resulting from third-order nonlinearity in the loop filter. Images of the two tones appear at the opposite frequencies of $f_s/4$ and result from DAC mismatches between even and odd samples. They can be partially compensated on the output data by adding a correction factor between the odd and even samples. Finally, some clock feedthrough components are present at an offset from the input tones equal to the reference frequency and falling outside the signal band. Main performance limitation is the noise caused by jitter originating from pseudo-differential implementation of clocking circuitry and buffers. A solution would be to employ fully-differential logic to reduce the noise injected via supply and ground lines and consequently obtain a higher SNDR.

By sweeping the two tones in power, the plot of Fig. 17 is obtained. The maximum SNDR in the 80 MHz band is a bit higher than 42 dB (6.7 bit). The maximum spurious-free dynamic range (SFDR) is around 50 dB and is dominated by the image tones. The full dynamic range (DR) of the converter is as high as 48 dB or 7.5 bit. With the same sweep set-up, a IIP_3 of 1 dBm was measured for the ADC as shown in Fig. 18.

Fig. 19 shows the SNDR measured at the output of the ADC for a single tone swept over the entire 80 MHz band. As the actual DFD implementation suffers from an overflow, the results shown in Fig. 19 are obtained with a software model of the DFD incorporating saturation logic using the measured ADC outputs as input. It can be concluded that the SNDR is achieved over the

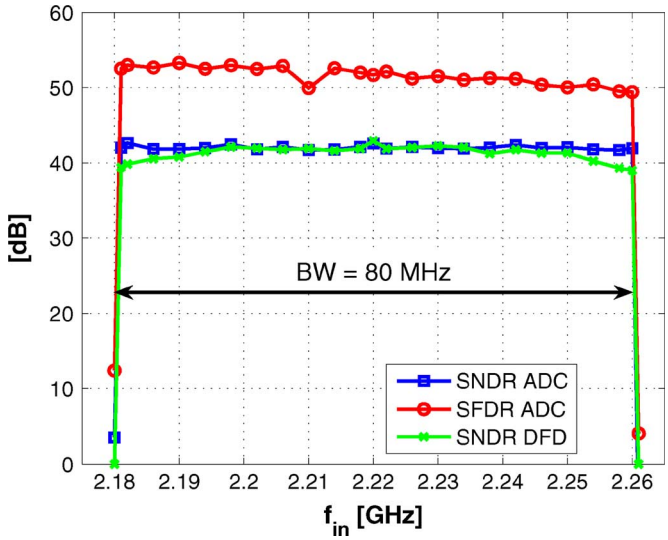

Fig. 19. Variation of the single-tone SNDR with input frequency before and after the DFD.

entire band at both the input and output of the DFD. The decimation filters of the DFD, however, cause a maximum degradation of about 2 dB near the edges of the band.

The current consumption of the RF BP $\Delta\Sigma$ ADC is 109 mA with 52% accounted for the loop filter and DAC and the rest for the quantizers and clocking network. The on-chip PLL consumes 72 mW. To ensure proper operation of the clocking network, all these blocks operate with a supply voltage of 1.5 V. The digital core consumes 13 mA, operating at 1.1 V. Considering that the power consumption of the clock and the test circuit was neglected, the obtained estimation was rather accurate. As shown in Fig. 12, the power for the implemented architecture E is 13 mW which is close to the measured power number of 14.3 mW.

The area of the core ADC (filter, comparators, DAC, and clocking network) and DFD is 0.4 mm^2 and 0.06 mm^2, respectively. Hence, the area of the DFD is almost negligible compared to the $\Delta\Sigma$ ADC.

Table I summarizes the properties of the RF BP $\Delta\Sigma$ ADC and compares them with some recent implementations. The figure-of-merit (FoM) used in this table is the classic FoM used for ADCs defined as [40]

$$\text{FoM} = \frac{\text{Power}}{2^{\text{ENOB}} \cdot 2 \cdot \text{Bandwidth}} \tag{1}$$

with ENOB computed as $(\text{SNDR}-1.76)/6.02$. This FoM, however, does not take into account the bandpass or RF properties of the $\Delta\Sigma$ modulator.

This work is the first reported CMOS implementation of a bandpass $\Delta\Sigma$ system operating around one-fourth of the sampling frequency of multiple GHz to achieve a high oversampling ratio and to simplify the architecture of the digital DFD. Furthermore, the design is the first demonstrator of a complete RF $\Delta\Sigma$ system including both PLL and high-speed digital postprocessing on chip. Its sampling rate of 8.88 GHz is the highest among CMOS implementations leading to a DR of 48 dB in a band of 80 MHz around 2.22 GHz center frequency. Hence, this design exploits the high-speed capabilities of deep-submicron CMOS more than previous implementations [16], [18] to achieve high resolution and it uses an architecture which enables low-power design of the DFD. The higher power consumption compared to these previous realizations is mainly due to the higher supply voltage needed for the clocking network to operate at 8.88 GHz. As explained above, higher resolution than measured with this design can be obtained by adopting a fully-differential implementation of the clocking circuitry and buffers which improves the power-resolution tradeoff without altering the architecture.

VII. Conclusion

RF bandpass $\Delta\Sigma$ ADCs are a key building block for software receivers used to directly digitize an RF band. While a high oversampling ratio is beneficial for achieving high resolution, a combination of a high OSR with the large width of the RF band results in a very high sampling speed. Realization of the digital logic needed to postprocess the signals at multiple GHz frequencies easily leads to power-hungry solutions. The implementation of an RF BP $\Delta\Sigma$ ADC in 40 nm digital CMOS proposed in this work demonstrates the feasibility of adopting high oversampling ratios for RF digitization without compromising the power efficiency of the digital postprocessing.

In contrast to previous reported realizations of RF BP $\Delta\Sigma$ ADCs, the test chip also contains the PLL for generating the high-speed clock signal as well as the digital part for downconversion, filtering and decimation. The $f_s/4$-mode of the RF $\Delta\Sigma$ modulator greatly simplifies the architecture of the downconversion stage. Further, by exploiting the interleaved structure of the quantizer, an efficient DFD architecture with polyphase filter can be adopted and the effective clock frequency for the DFD is reduced. These architectural choices make the implementation feasible in standard CMOS. Furthermore, the system is made very tunable to compensate for inevitable process variations.

Centered at 2.22 GHz and using a sampling rate of 8.88 GHz, a dynamic range of 48 dB is measured in an 80 MHz band. With a fully-differential implementation of clocking circuitry and buffers, a higher resolution can be obtained without changing the architecture of the system. A power-aware evaluation flow was adopted to realize an efficient implementation of the digital filters which process signals at 1.48 GHz with limited power consumption. As a result, this complete RF bandpass $\Delta\Sigma$ system efficiently combines a high oversampling ratio with a large bandwidth at RF and acts as a solution for RF digitization in standard CMOS.

Acknowledgment

The authors would like to thank J. Borremans and B. Verbruggen for fruitful technical discussions, and H. Suys for PCB design.

References

[1] T. Burger and Q. Huang, "A 13.5-mW 185-Msample/s $\Delta\Sigma$ modulator for UMTS/GSM dual-standard IF reception," *IEEE J. Solid-State Circuits*, vol. 36, no. 12, pp. 1868–1878, Dec. 2001.

[2] A. A. Abidi, "The path to the software-defined radio receiver," *IEEE J. Solid-State Circuits*, vol. 42, no. 5, pp. 954–966, May 2007.

[3] J. Borremans, G. Mandal, V. Giannini, T. Sano, M. Ingels, B. Verbruggen, and J. Craninckx, "A 40 nm CMOS highly linear 0.4-to-6 GHz receiver resilient to 0 dBm out-of-band blockers," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2011, pp. 62–63.

[4] J. Mitola, "The software radio architecture," *IEEE Commun. Mag.*, vol. 33, no. 5, pp. 26–38, May 1995.

[5] S. Sarwana, D. E. Kirichenko, V. V. Dotsenko, A. F. Kirichenko, S. B. Kaplan, and D. Gupta, "Multi-band digital-RF receiver," *IEEE Trans. Appl. Supercond.*, vol. 21, no. 3, pp. 677–680, Jun. 2011.

[6] B. Verbruggen, J. Craninckx, M. Kuijk, P. Wambacq, and G. Van der Plas, "A 2.2 mW 5b 1.75 GS/s folding flash ADC in 90 nm digital CMOS," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2008, pp. 252–253.

[7] B. D. Sahoo and B. Razavi, "A 12-Bit 200-MHz CMOS ADC," *IEEE J. Solid-State Circuits*, vol. 44, no. 9, pp. 2366–2380, Sep. 2009.

[8] Y.-Z. Lin, C.-C. Liu, G.-Y. Huang, Y.-T. Shyu, and S.-J. Chang, "A 9-bit 150-MS/s 1.53-mW subranged SAR ADC in 90-nm CMOS," in *IEEE Symp. VLSI Circuits Dig. Tech. Papers*, June 2010, pp. 243–244.

[9] S.-W. M. Chen and R. W. Brodersen, "A subsampling radio architecture for ultrawideband communications," *IEEE Trans. Signal Process.*, vol. 55, no. 10, pp. 5018–5031, Oct. 2007.

[10] R. Schreier and G. C. Temes, *Understanding Delta-Sigma Data Converters*. Hoboken, NJ: Wiley-IEEE Press, 2005.

[11] E. Martens, A. Bourdoux, A. Couvreur, P. Van Wesemael, G. Van der Plas, J. Craninckx, and J. Ryckaert, "A 48-dB DR 80-MHz BW 8.88-GS/s bandpass $\Delta\Sigma$ ADC for RF digitization with integrated PLL and polyphase decimation filter in 40 nm CMOS," in *IEEE Symp. VLSI Circuits Dig. Tech. Papers*, Jun. 2011, pp. 40–41.

[12] D. Novo, R. Fasthuber, P. Raghavan, A. Bourdoux, M. Li, L. Van der Perre, and F. Catthoor, "Power-aware evaluation flow for digital decimation filter architectures for high-speed ADCs," in *Proc. IEEE Workshop Signal Process. Syst. (SiPS)*, Oct. 2009, pp. 151–156.

[13] J. A. Cherry, W. M. Snelgrove, and W. Gao, "On the design of a fourth-order continuous-time *LC* Delta-Sigma modulator for UHF A/D conversion," *IEEE Trans. Circuits Syst. II, Analog Dig. Signal Process.*, vol. 47, no. 6, pp. 518–530, Jun. 2000.

[14] B. K. Thandri and J. Silva-Martinez, "A 63 dB SNR, 75-mW bandpass RF $\Sigma\Delta$ ADC at 950 MHz using 3.8-GHz clock in 0.25-μm SiGe BiCMOS technology," *IEEE J. Solid-State Circuits*, vol. 42, no. 2, pp. 269–279, Feb. 2007.

[15] T. Chalvatzis, E. Gagnon, M. Repeta, and S. P. Voinigescu, "A low-noise 40-GS/s continuous-time bandpass $\Delta\Sigma$ ADC centered at 2 GHz for direct sampling receivers," *IEEE J. Solid-State Circuits*, vol. 42, no. 5, pp. 1065–1075, May 2007.

[16] J. Ryckaert, J. Borremans, B. Verbruggen, L. Bos, C. Armiento, J. Craninckx, and G. Van der Plas, "A 2.4 GHz low-power sixth-order RF bandpass $\Delta\Sigma$ converter in CMOS," *IEEE J. Solid-State Circuits*, vol. 44, no. 11, pp. 2873–2880, Nov. 2009.

[17] N. Beilleau, H. Aboushady, F. Montaudon, and A. Cathelin, "A 1.3 V 26 mW 3.2 GS/s undersampled LC bandpass $\Sigma\Delta$ ADC for a SDR ISM-band receiver in 130 nm CMOS," in *Proc. IEEE Radio Frequency Integr. Circuits (RFIC) Symp.*, Jun. 2009, pp. 383–386.

[18] J. Ryckaert, A. Geis, L. Bos, G. Van der Plas, and J. Craninckx, "A 6.1 GS/s 52.8 mW 43 dB DR 80 MHz bandwidth 2.4 GHz RF bandpass $\Delta\Sigma$ ADC in 40 nm CMOS," in *Proc. IEEE Radio Frequency Integr. Circuits (RFIC) Symp.*, May 2010, pp. 443–446.

[19] C.-Y. Lu, J. F. Silva-Rivas, P. Kode, J. Silva-Martinez, and S. Hoyos, "A sixth-order 200 MHz IF bandpass Sigma-Delta modulator with over 68 dB SNDR in 10 MHz bandwidth," *IEEE J. Solid-State Circuits*, vol. 45, no. 6, pp. 1122–1136, Jun. 2010.

[20] S. Gupta, D. Gangopadhyay, H. Lakdawala, J. C. Rudell, and D. J. Allstot, "A QPLL-timed direct-RF sampling band-pass $\Sigma\Delta$ ADC with a 1.2 GHz tuning range in 0.13 μm CMOS," in *Proc. IEEE Radio Frequency Integr. Circuits (RFIC) Symp.*, Jun. 2011, pp. 1–4.

[21] A. Namdar and B. H. Leung, "A 400-MHz, 12-bit 18-mW, IF digitizer with mixer inside a Sigma-Delta modulator loop," *IEEE J. Solid-State Circuits*, vol. 34, no. 12, pp. 1765–1776, Dec. 1999.

[22] A. I. Hussein and W. B. Kuhn, "Bandpass $\Sigma\Delta$ modulator employing undersampling of RF signals for wireless communication," *IEEE Trans. Circuits Syst. II, Analog Dig. Signal Process.*, vol. 47, no. 7, pp. 614–620, July 2000.

[23] A. Naderi, M. Sawan, and Y. Savaria, "On the design of undersampling continuous-time bandpass Delta-Sigma modulators for gigahertz frequency A/D conversion," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 55, no. 11, pp. 3488–3499, Dec. 2008.

[24] H. Tao and J. M. Khoury, "A 400-Ms/s frequency translating bandpass Sigma-Delta modulator," *IEEE J. Solid-State Circuits*, vol. 34, no. 12, pp. 1741–1752, Dec. 1999.

[25] R. Winoto and B. Nikolić, "A highly reconfigurable 400–1700 MHz receiver using a down-converting Sigma-Delta A/D with 59-dB SNR and 57-dB SFDR over 4-MHz bandwidth," in *Proc. IEEE Symp. VLSI Circuits Dig. Tech. Papers*, June 2009, pp. 142–143.

[26] K. Koli, S. Kallioinen, J. Jussila, P. Sivonen, and A. Pärssinen, "A 900-MHz direct Delta-Sigma receiver in 65-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 45, no. 12, pp. 2807–2818, Dec. 2010.

[27] Y.-G. Yoon and S. Cho, "A 1.5-GHz 63 dB SNR 20 mW direct RF sampling bandpass VCO-based ADC in 65 nm CMOS," in *Proc. IEEE Symp. VLSI Circuits Dig. Tech. Papers*, Jun. 2009, pp. 270–271.

[28] J. Lee, J. Kim, and S. Cho, "A 1.8 to 2.4-GHz 20 mW digital-intensive RF sampling receiver with a noise-canceling bandpass low-noise amplifier in 90 nm CMOS," in *IEEE Radio Frequency Integr. Circuits (RFIC) Symp.*, May 2010, pp. 293–296.

[29] J. Kim, W. Yu, H.-K. Yu, and S. Cho, "A digital-intensive receiver front-end using VCO-based ADC with an embedded 2nd-order anti-aliasing sinc filter in 90 nm CMOS," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2011, pp. 176–177.

[30] D. Lachartre, "A 550 μW inductorless bandpass quantizer in 65 nm CMOS for 1.4-to-3 GHz digital RF receivers," in *IEEE Symp. VLSI Circuits Dig. Tech. Papers*, Jun. 2011, pp. 166–167.

[31] E. J. van der Zwan and E. C. Dijkmans, "A 0.2-mW CMOS $\Sigma\Delta$ modulator for speech coding with 80 dB dynamic range," *IEEE J. Solid-State Circuits*, vol. 31, no. 12, pp. 1873–1880, Dec. 1996.

[32] J. A. Cherry and W. M. Snelgrove, "Excess loop delay in continuous-time Delta-Sigma modulators," *IEEE Trans. Circuits Syst. II, Analog Dig. Signal Process.*, vol. 46, no. 4, pp. 376–389, Apr. 1999.

[33] J. Proakis and D. Manolakis, *Digital Signal Processing—Principles, Algorithms and Applications*, 4th ed. Englewood Cliffs, NJ: Prentice Hall, 2006.

[34] H. Aboushady, Y. Dumonteix, M.-M. Louërat, and H. Mehrez, "Efficient polyphase decomposition of comb decimation filters in $\Sigma\Delta$ analog-to-digital converters," *IEEE Trans. Circuits Syst. II, Analog Dig. Signal Process.*, vol. 48, no. 10, pp. 898–903, Oct. 2001.

[35] E. B. Hogenauer, "An economical class of digital filters for decimation and interpolation," *IEEE Trans. Acoust., Speech, Signal Process.*, vol. 29, no. 2, pp. 155–162, Apr. 1981.

[36] M. Ingels, V. Giannini, J. Borremans, G. Mandal, B. Debaillie, P. Van Wesemael, T. Sano, T. Yamamoto, D. Hauspie, J. Van Driessche, and J. Craninckx, "A 5 mm^2 40 nm LP CMOS transceiver for a software-defined radio platform," *IEEE J. Solid-State Circuits*, vol. 45, no. 12, pp. 2794–2806, Dec. 2010.

[37] P. Nuzzo, K. Vengattaramane, M. Ingels, V. Giannini, M. Steyaert, and J. Craninckx, "A 0.1–5 GHz dual-VCO software-defined $\Sigma\Delta$ frequency synthesizer in 45 nm digital CMOS," in *Proc. IEEE Radio Frequency Integr. Circuits (RFIC) Symp.*, June 2009, pp. 321–324.

[38] J. Yuan and C. Svensson, "High-speed CMOS circuit technique," *IEEE J. Solid-State Circuits*, vol. 24, no. 1, pp. 62–70, Feb. 1989.

[39] G. W. Reitwiesner, "Binary arithmetic," in *Proc. Adv. Comput.*, 1960, pp. 231–308.

[40] R. H. Walden, "Analog-to-digital converter survey and analysis," *IEEE J. Sel. Areas Commun.*, vol. 17, no. 4, pp. 539–550, Apr. 1999.

Ewout Martens (M'08) was born in Genk, Belgium, in 1978. He received the M.Sc. and Ph.D. (*summa cum laude*) degrees from the Katholieke Universiteit, Leuven, Belgium, in 2001 and 2007, respectively.

From 2001 to 2007, he was a Research Assistant with ESAT-MICAS Laboratories of the Katholieke Universiteit Leuven. His Ph.D. research was on modeling of Delta-Sigma modulators and RF front-ends. He joined IMEC, Belgium, in 2010 as a Design Engineer for WLAN transceivers. Currently he is working on development of innovative architectures for RF receiver front-ends.

André Bourdoux (M'94) received the M.S. degree in electrical engineering from the Université Catholique de Louvain-la-Neuve, Belgium, in 1982.

He joined IMEC in 1998 and is now a Principal Scientist in the Circuits and Systems for ICT group of the Smart Systems and Energy Technologies division of IMEC, Leuven. His current research interests include multidisciplinary, spanning the areas of wireless communications theory and signal processing, with a special emphasis on broadband systems and emerging physical layer techniques. He has authored more than 100 conference and journal papers and book chapters and is the inventor of several patents.

Aissa Couvreur received the M.Sc. degree from the Department of Industrial Sciences and Technologies, Katholieke Hogeschool Brugge-Oostende, Belgium, in 2001.

In 2001, she joined IMEC, Belgium, where she is currently a Development Engineer, focusing on RTL implementation for prototypes for software defined radios.

Robert Fasthuber (S'08) received the M.Sc. degree in hardware/software systems engineering from the University of Applied Science (FH) Hagenberg, Austria, in 2007.

In 2007, he became a Researcher at IMEC Belgium and at the Katholieke Universiteit (K.U.) Leuven. He is a Ph.D. student since July 2008. His research interests include on technology-aware low-power architectures for software defined radio and cognitive radio implementations.

Peter Van Wesemael received the B.Sc. and M.Sc. degrees in information and communication technologies from the Katholieke Industriële Hogeschool De Nayer, Sint-Katelijne-Waver, Belgium.

In 2001, he joined the Interuniversity Microelectronics Center, IMEC, Leuven, Belgium, where he is currently a Development Engineer, focusing on prototype development for software defined radio systems and digital compensation techniques for RF front-ends.

Geert Van der Plas (S'90–A'02–M'03) received the M.Sc. and Ph.D. degrees from the Katholieke Universiteit Leuven, Belgium, in 1992 and 2001, respectively.

From 1992 to 2002, he was a Research Assistant with ESAT-MICAS of the Katholieke Universiteit Leuven. He joined IMEC, Leuven, Belgium, in 2003, where he is a Principal Scientist. He has been working on energy efficient data converters, low-power scalable radios, power and signal integrity, and design technology for 3-D integration. He has authored and coauthored over 100 papers in journals and conference proceedings and serves on the technical program committee of the Symposium on VLSI Circuits.

Jan Craninckx (M'98–SM'07) received the M.S. and Ph.D. degrees in microelectronics (*summa cum laude*) from the ESAT-MICAS laboratories of the Katholieke Universiteit Leuven, Belgium, in 1992 and 1997, respectively. His Ph.D. work was on the design of low-phase noise CMOS integrated VCOs and synthesizers.

From 1997 until 2002, he worked with Alcatel Microelectronics (later part of STMicroelectronics) as a senior RF engineer on the integration of RF transceivers for GSM, DECT, Bluetooth, and WLAN. In 2002, he joined IMEC, Leuven, Belgium, where he currently is the Senior Principal Scientist of the analog wireless research group. His research focuses on the design of RF transceiver front-ends for software defined radio (SDR) systems, covering all aspects of RF, analog and data converter design. He has authored and coauthored more than 100 papers and several book chapters, and is the inventor of 10 patents.

Dr. Craninckx is a member of the Technical Program Committee for several conferences, was the chair of the SSCS Benelux chapter (2006–2011), and is an Associate Editor of the IEEE JOURNAL OF SOLID-STATE CIRCUITS.

Julien Ryckaert (M'07) was born in Brussels, Belgium, in 1977. He received the M.Sc. degree in electrical engineering from the University of Brussels (ULB), Brussels, Belgium, in 2000, and the Ph.D. degree (*summa cum laude*) from Vrije Universiteit Brussel in 2007.

He joined IMEC, Leuven, Belgium, in 2000 as an RF designer for WLAN transceivers. From 2003, he worked as a System Architect for low-power low-data-rate ultrawideband transceivers in which he completed his Ph.D. He is now heading a project on innovative wireless transceiver architectures for cognitive radio. He has authored or coauthored more than 30 articles in various IEEE conferences and journals.