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Low-power Architecture for A 6-bit 1.6GS/s Flash A/D Converter

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Abstract—A 6-bit, 1.6-GS/s, flash ADC with a low-power architecture is presented. The proposed low-power architecture based on an analog input pre-processing method reduces the total number of comparators to almost two-thirds of that required in a conventional 6-bit, flash ADC. The advantages of the analog input pre-processing method include the low power consumption and small area due to the reduced number of comparators. The proposed flash ADC consumes 240mW at a supply voltage of 1.8V when implemented in a 0.18-µm CMOS technology. The simulated SNDR is 32dB at an input frequency of 200MHz.

I. INTRODUCTION

Flash ADCs are required in high-performance systems such as disk-drive read channels and wideband wireless systems. However, the conventional 6-bit, flash ADC has significant weaknesses. In flash ADCs, one comparator is required for each threshold of the converter. Thus, the total number of comparators required is 2^n-1 (n: resolution). Therefore, the die area and power consumption increase exponentially with the resolution. The flash ADC with analog input pre-processing stage proposed in this paper can reduce the total number of pre-amplifiers and comparators, followed by pre-amplifier stages which consume a great deal of power, so as to guarantee the high-speed operation of the ADC. Also, a controlled comparator output (CCO) block is proposed to convert the 43 comparator outputs into 63 thermometer codes. In addition, to reduce the power consumption as well as to guarantee high-speed operation, a single-ended pass transistor pulsed latch (SPTPL) [1] and interpolation/ averaging network are adopted.

II. ADC ARCHITECTURE

The proposed 6-bit, 1.6GS/s ADC consists of an analog input pre-processing stage, four preamplifier stages, comparators, a controlled comparator output (CCO) and digital backend, as shown in Fig. 1. With the proposed analog input pre-processing stage, the analog input range can be reduced by half. As a result, the number of preamplifiers and comparators prior to the analog input pre-processing block is reduced by half (63+2→32+2 : 2 represents dummies). The reduction of the input range increases the instability of operation near the common mode voltage and an additional overlap comparator block is added to cover the non-linearity of the switches at a fast input frequency and compensate for the timing error in the analog input pre-processing block. The overlap comparator block consists of 9 preamplifiers with four stages and 9 comparators to compare the analog input

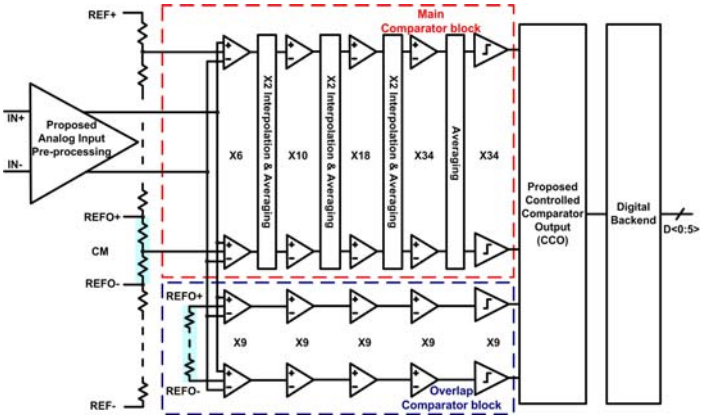

Fig. 1. Block diagram of the proposed ADC.

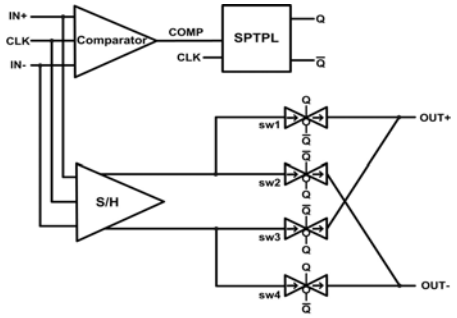

Fig. 2. Proposed analog input pre-processing block.

near the common mode voltage. Therefore, the total number of comparators and preamplifiers is reduced to two-thirds of that required in a conventional 6-bit, flash ADC (65→43), even when the overlap comparator block is included. Resistive averaging networks [2] are used at the output of each preamplifier stage, in order to reduce the offset, and factor of 8 interpolation is also adopted to reduce the power consumption.

III. PROPOSED LOW-POWER ARCHITECTURE OF ADC

A. Proposed Analog Input Pre-processing

The proposed analog input pre-processing stage consists of a comparator, sample and hold (S/H), flip-flop and four switches, as shown in Fig. 2. Differential inputs are applied to the comparator and S/H simultaneously and both blocks are synchronized to a 1.6GHz clock. Therefore, the comparator compares the differential inputs during the sample phase of the S/H. The output of the comparator is applied to an SPTPL which is suitable for high-speed operation, due to the negative setup time and simple topology. The flip-flop output Q controls the four switches followed by the S/H and four

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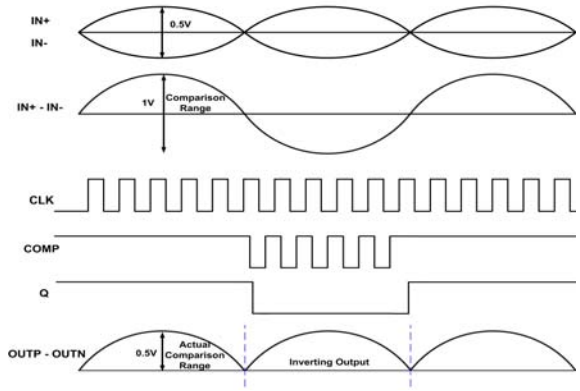

Fig. 3. Operation of proposed analog input pre-processing stage.

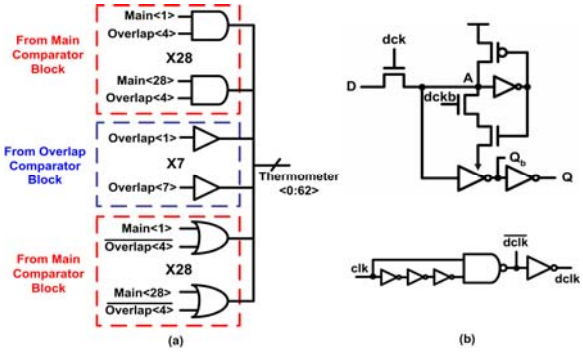

Fig. 4. (a) Proposed controlled comparator output(CCO). (b) SPTPL.

switches are operated correctly during the hold phase of the S/H. As a result, the proposed block does not experience any timing problems, because all of the operations of the block are completed in a single cycle clock.

The operation of the block is described in detail using the waveforms shown in Fig. 3. The top waveform is the differential input to the proposed block, and the comparison range is $1V_{pp}$. The comparator output COMP becomes 'high' when the positive input is larger than the negative input. In the opposite case, COMP is toggled from one to zero continuously, and it is converted to zero after passing through the flip-flop. The flip-flop output Q controls the four switches, and if Q is 'high', switches sw1 and sw4 in Fig. 2 are on, which means that the differential outputs of the S/H are directly applied to the following preamplifier stage and otherwise, if Q is 'low', switches sw2 and sw3 in Fig. 2 are on, which means that the differential outputs of the S/H are crossed, compared with the previous case. In this case, the output of the analog input pre-processing block is the inverted output of the S/H, as shown in the last waveform of Fig. 3. As a result, the input comparison range is reduced by half from the last waveform.

B. Proposed Controlled Comparator Output and SPTPL

Figure 4(a) shows the proposed controlled comparator output (CCO) block. The role of the proposed block is to convert the 43 comparator outputs to the 63 thermometer codes which are applied to the digital backend. It consists of simple logic gates to minimize the additional power consumption. Only 28 comparators of the main comparator

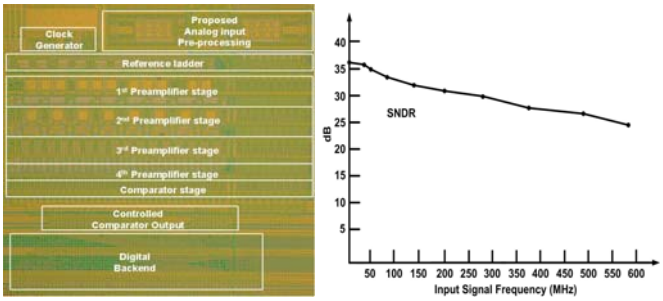

Fig. 5. (a) Die photo. (b) Simulated SNDR vs. input frequency.

Table I. Performance Comparisons

	[2]	[3]	[4]	This Work
Technology	0.35μm CMOS	0.18μm CMOS	0.18μm CMOS	0.18μm CMOS
Supply	3.3V	1.95V (Analog) 2.35V (Digital)	1.8V	1.8V
Resolution	6 bits	6 bits	6 bits	6 bits
Sampling Rate	1.3 GS/s	1.6 GS/s	2 GS/s	1.6 GS/s
Input Range	1.6 V_{pp}	1 V_{pp}	1 V_{pp}	1 V_{pp}
INL/DNL	0.35 LSB 0.2 LSB	0.42 LSB 0.4 LSB	0.5 LSB 0.32 LSB	0.5 LSB 0.32 LSB
SNDR	32 dB (@f_{in} : 650MHz)	31.6 dB (@f_{in} : 660MHz)	30 dB (@f_{in} : 941MHz)	32 dB (@f_{in} : 200MHz)
Power Consumption	545 mW	340 mW	310 mW	240 mW
Active Area	0.8 mm^2	0.12 mm^2	0.5 mm^2	0.49 mm^2
FOM	8.64pJ/step	4.09pJ/step	3.42pJ/step	3.31pJ/step

block are used and these are controlled by the signal Overlap<4> of the overlap comparator block, while the remaining 7 comparator outputs are replaced with the outputs of the overlap comparator block.

The schematic of the SPTPL is shown in Fig. 4 (b). The SPTPL is the most energy efficient type of flip-flop with a pulsed clock generator.

IV. IMPLEMENTATION RESULTS AND CONCLUSION

The 6-bit, 1.6GS/s, flash ADC was implemented in a 0.18um CMOS process and occupies 0.49 mm^2. The proposed ADC consumes 240mW at a supply voltage of 1.8V. The simulated SNDR is 32dB at an input frequency of 200MHz. The proposed ADC achieved a figure of merit (FOM), which is defined as Power/($2^{ENOB} * f_s$), of 3.31pJ/step. The ENOB is simulated at an input frequency of 200MHz. Table I shows the performance comparison with other 6-bit, flash ADCs.

V. ACKNOWLEDGEMENT

This work was supported by Samsung Electro-Mechanics.

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