A 1.0 GS/s 7bit Pipelined-Folding-Interpolating ADC with 6.0 ENOB at Nyquist Frequency

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***Abstract*—A single-channel 1.0 GS/s 7bit Pipelined-Folding-Interpolating analog-to-digital converter (PL-FAI-ADC) is presented. A fine and coarse joint encoding method is proposed to simplify the analog preprocessing of the coarse sub-ADC and to save power and chip area. Double-diode bootstrapped inter-stage switch is adopted to improve the overall efficiency of speed. The ADC implemented in 0.13-μm CMOS achieves SNDR of 37.89 dB and SFDR of 45.89 dB for 498MHz input frequency located at 1.0GS/s. The power consumption is 110mW with sampling rate of 1.0GS/s and supply voltage of 1.5/2.5 V.**

***Index Terms*—Folding and Interpolating, ADC and CMOS**

I. INTRODUCTION

Low-power ADC with GHz sampling frequency is the key part in broadband communication systems such as mm-wave receiver, UWB system, and future Optical Communication systems. These applications demand ultrahigh speed ADCs with low power and high bandwidth.

However, such kind of ADCs has been investigated with some focuses. Most designs focus on Time-Interleaved (TI) architecture with the sub-ADC of Pipelined or SAR ADC [4, 8] to increase the conversion rate. This kind of ADCs is able to achieve low power consumption by using the low power architecture as channel Sub-ADCs. However, TI ADC is suffered from mismatches among channels, so digital calibration is always needed in order to guarantee the performance. With the increase of the sampling rate, the number of channel Sub-ADCs embedded in TI architecture is also increased. As a result, it is more difficult and complicated to implement digital calibration, which leads to an extra area and power. Furthermore, the input bandwidth is not enough.

An efficient way to realize a gigahertz ADC adopted in this paper is folding and interpolating (FAI) ADC. In order to achieve the gigahertz sampling rate, a pipelined structure is applied in FAI-ADC [6]. Inter-stage sampling switch is one of the most important modules in the pipelined structure. For inter-stage sampling switches, the on-resistance of them should be small enough to make the signal delay introduced by sampling switches as short as possible. Furthermore, inter-stage sampling switches are used in an array. So the switch should be as simple as possible. In published works [6, 7], CMOS switches are used as inter-stage sampling switches. But for low-voltage applications, the overdrive voltage of a CMOS switch is reduced. So the on-resistance is increased which introduces a longer signal delay. As an alternative, a bootstrapped switch is useful to lower the on-resistance and reduce the signal delay in low supply voltage. But the complicated bootstrapped circuits [3] are not suitable for array mode in terms of chip area and power efficiency. In this paper, a new double-diode bootstrapped switch based on [2] is proposed.

Furthermore, a new fine and coarse joint encoding is proposed to simplify the course of analog pre-processing and to lower the chip power. In bit synchronization encoding [3], the number of signal channels in coarse sub-ADC is F, which is the total folding factor of the FAI-ADC. In this new encoding, the number of coarse pre-amplifiers is reduced to F_1-2. F_1 is the folding factor of the first folding-stage. Especially for the larger folding factor, the power of the pre-amplifiers of coarse sub-ADC would be saved.

II. ARCHITECTURE

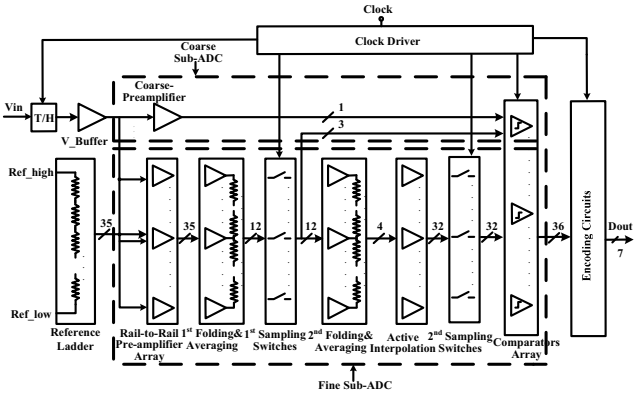

Fig. 1. Block diagram of the ADC

The block diagram of the analog to digital converter is shown in Fig. 1. It employs a single track-and-hold (T/H) block to isolate the input signal from the input capacitors of the preamplifier array, which adds up to a comparable value of the sampling capacitor. This block is composed of a bootstrapped switch and a source follower. The bootstrapped

switch holds the input signal on the sampling capacitor and the source follower avoids the kick-back noise from the inputs of pre-amplifier to the sampling capacitor. A resistor ladder between two reference voltages generates 35 tap voltages. They divide the whole quantified range into 34 sections for the pre-amplifier array which is composed by 36 overall differential rail-to-rail amplifiers with resistive load including dummies. Followed by is a 2-stage cascaded folder with folding factor 3× for each stage. Inter-stage sampling switches and an averaging resistor array are inserted between the two stages. 12 folded signals with 35 zero-crossings are interpolated by a 3-stages interpolating block. And the interpolating factor of each stage is 2. In order to reach substantial gain to weaken the offset voltage caused by comparators, active interpolating amplifiers are adopted in this design.[1] First, 5-bit cycle thermometer codes are generated after the 32 interpolating signals fed into 35 comparators which work like the traditional fine sub-ADC. At the same time, coarse sub-ADC adopted 3 folding signals from the output of the first folding stage and one signal from the only one coarse pre-amplifier to generate 4-bit cycle thermometer codes. After that, all of the cycle thermometer codes are merged together and translated into 7 bits binary codes by an encoder in the digital part.

One of the non-ideal factors of the ADC is the mismatch among folding signal paths. That can be reduced through some structural methods. Averaging resistor network is one of the best choices [5]. Offsets of the pre-amplifier array as well as those of the first stage folding array can be averaged through the joint resistors.

III. CIRCUITS IMPLEMENTATION

A. Fine and Coarse Joint Encoding

In the main FAI-ADC core, the cyclic outputs of the fine sub-ADC require the coarse sub-ADC to find the fold zone in which an input signal can be located. Generally, in bit synchronization encoding [3], F signal channels are needed in the coarse sub-ADC for the total folding factor F. In order to reduce the hardware consumption of the coarse sub-ADC without worsening the performance of encoding, a new method of fine and coarse joint encoding is proposed.

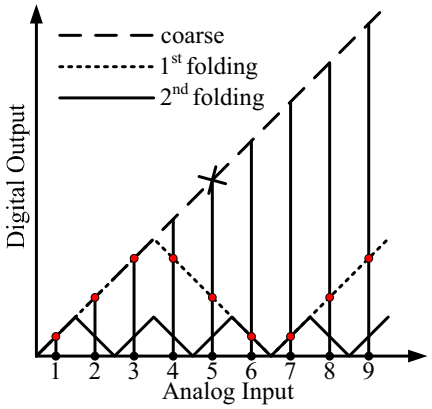

Fig. 2. Fine and Coarse joint encoding

Taking an example of a two-stage cascaded folding with the total folding factor F of 9, Fig. 2 illuminates the theory of the fine and coarse joint encoding. The black dots (1-9) need to be generated in coarse sub-ADC in traditional bit synchronization encoding. These inputs should also be quantized by 1st folding amplifiers. As a result, the outputs of 1st folding amplifiers with the folding factor F_1 of 3, as shown in red dots, are the quantization results of these nine inputs in circles. These outputs can be used to participate in coarse encoding in order to reduce the hardware consumption of the coarse analog preprocessing.

Nevertheless, the outputs of 1st folding amplifiers are cyclic. In order to distinguish the difference between the same outputs caused by different inputs, one signal channel is needed in the coarse sub-ADC, as shown in cross. Then, the nine fold zone can be differentiated.

By using the new fine and coarse joint encoding, the number of pre-amplifiers in coarse sub-ADC is reduced from F to F_1-2. In this design, the number is reduced from 9 to 1. It is very helpful to reduce power consumption of the coarse sub-ADC.

B. Double-Diode Bootstrapped Inter-Stage Switches

The 2-stage inter-stage sampling switches are used in this pipeline structure. One is inserted between the two stages of folding amplifiers, and the other is inserted between the interpolating stage and comparators array. The conversion time of the fine analog preprocessing is extended from half period to one. The critical path includes fine preamplifiers, 1st folding amplifiers and inter-stage sampling switches or 2nd folding amplifiers and active interpolation.

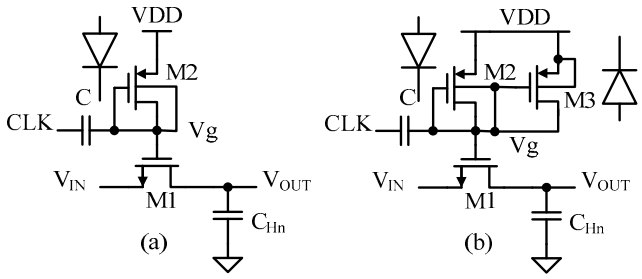

Fig. 3. (a) Single-Diode Bootstrapped Switch
(b) Double-Diode Bootstrapped Switch

One kind of Single-Diode Bootstrapped NMOS sampling switches is shown in Fig3 (a). [1] M1 is the NMOS switch and C_{Hn} is the next stage input capacitor. M2 and C compose the bootstrapped circuit. The substrate and the drain of M2 are connected together (N-well technology is adopted) so that M2 works as a diode. The positive terminal of the diode-connected M2 is lead to V_{DD} and the negative terminal is lead to the gate of M1, (V_g) which prevents the PN junction formed between the N-well and the P+ source diffusion to become forward biased, and therefore allows positive voltage swings larger than the threshold voltage of a PN junction over V_{DD}. That would increase the overdrive voltage of M1 and reduced the on-resistance of it. The analog signal-delay would be reduced.

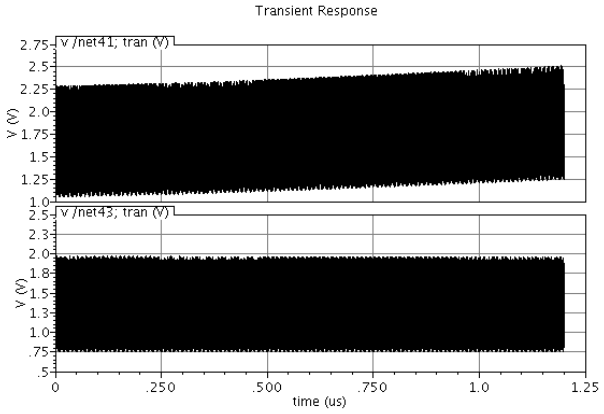

Fig. 4. (a) Cure of V_g with single-diode switch ($\Delta V_{g,r} > \Delta V_{g,d}$,)
(b) Cure of V_g with double-diode switch

But when CLK has a positive jump of ΔV_{clk}, V_g would have a positive jump of ΔV_g along with CLK and M1 would turn on. Similarly, a negative jump of CLK awakes a negative jump of V_g and M1 turns off. ΔV_g is given as

$$\Delta V_g = \frac{C}{C+C_g}\Delta V_{CLK} \quad (1)$$

In formula (1), C_g is the total parasitic capacitor of V_g and C is a coupling capacitor. Generally, the W/L of M1 should be larger to reduce the on-resistance, and the value of C is smaller. C_g mainly composes of two variable capacitors. One is the gate capacitor of M1, and the other is the PN junction's capacitor. They would change with the bias voltage of the net V_g. So C_g is variable at different cases which are positive jump and negative jump of the CLK. So $\Delta V_{g,r}$ and $\Delta V_{g,d}$ is different. If $\Delta V_{g,r}$ is larger than $\Delta V_{g,d}$, the extra charge would be accumulated at the net V_g. Then V_g would become larger and larger, and the M1 would be broken down. Fig. 4 (a) shows simulation results of the net V_g in the circuit of Fig. 3 (a) in a standard 0.13μm CMOS technology, when $\Delta V_{g,r}$ is larger than $\Delta V_{g,d}$.

In this design, an inter-stage double-diode bootstrapped NMOS sampling switch is proposed and shown in Fig. 3 (b). An extra diode-connected M3 is added. The substrate and the source of M3 are connected together to V_{DD} as negative terminal. The positive terminal of the diode-connected M3 is lead to V_g. The M3 makes V_g not to exceed V_{DD}-V_{thp}. V_{thp} is the threshold voltage of M3. Even though, the switch-off voltage is not zero, the inter-stage switch turnoff is decided by the input signal---V_{IN}. In this paper, the inter-stage switches sample the outputs of 1st folding amplifiers or 3rd interpolating amplifiers. In the typical folding amplifier and interpolating amplifier, a couple of resistors are used as loads. That is shown in Fig. 5. Thus, the output swing is usually given as

$$V_{DD}\text{-}IR \le V_{out+}, V_{out-} \le V_{DD} \quad (2)$$

In equation (2), where I is the bias current and R is the load resistance of folding or interpolating amplifiers. In order to make M1 turn off, V_{DD}-IR should be larger than V_{DD}-V_{thp}. It is easily fulfilled in low-voltage and high-speed applications. Fig. 4 (b) shows simulation results of the net V_g in the circuit of Fig. 3 (b) in a standard 0.13μm CMOS technology, when $\Delta V_{g,r}$ is larger than $\Delta V_{g,d}$.

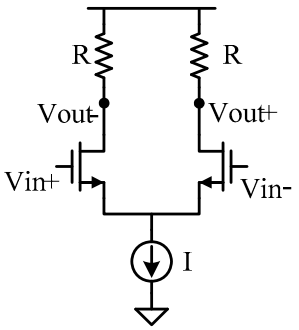

Fig. 5. Typical folding and interpolating amplifier

Compared with the CMOS switches, the complicated bootstrapped switches or a single-diode bootstrapped switch, the double-diode bootstrapped switch has a lower and invariable on-resistance, and it is simple and steady. Although the ΔV_{clk} is reduced, it has no effect on the performance of the inter-stage sampling switch. It is suitable to be used as inter-stage sampling switches array in PL-FAI-ADC.

IV. Measurement Result

A single-channel 1.0 GS/s 7bit PL-FAI-ADC is prototyped in 0.13-μm CMOS with a core area of 0.32 mm^2. The die microphotograph is shown in Fig. 6. Output data is down-sampled by a factor of five to ease testing data sampling. For easy testing, the ADC chip is mounted on a printed circuit board (PCB) with direct die-to-board wire bonding. Meanwhile, multi-wires are bonded on a pad in order to reduce the effect caused by the parasitized inductance of the bonding wires (about 1nH per-μm). Fig. 7 shows the DNL and INL performance for a lower frequency of 2.4-MHz input signal at a 1.0 GS/s sampling rate. The values lay in the range of -0.47 LSB to 0.45 LSB and -0.62 LSB to 1.14 LSB, respectively. Fig. 8 shows the measured SNDR/SFDR versus input signal frequency at 1.0 GS/s. SNDR/SFDR achieves 41.66 dB/50.4 dB at a 10.7MHz input and 37.89 dB/45.89 dB at a 498MHz input, respectively. Fig. 9 shows the measured ENOB versus input signal frequency at 1.0 GS/s. ENOB is maintained above 6.0 in the whole nyquist frequency range. The total power consumption is 110 mW. In detail, the high-performance voltage buffer used between the T/H stage and the pre-amplifiers array consumes about 50mW at a 2.5V supply voltage, and other blocks consume the rest of 60mW at a 1.5V supply voltage.

The performance summary of measured results compared with some published 7bit gigahertz ADCs are given in Table I. This work achieves the highest single-channel sampling rate of 1.0 GS/s and the largest ERBW of 450MHz with comparable power consumption and static performance. (Fom=$P_{diss}/(2^{ENOB}\times 2\times ERBW)$)

V. CONCLUSIONS

With the fine and coarse joint encoding and the double-diode bootstrapped NMOS inter-stage sampling switches, the proposed 7-bit signal-channel PL-FAI-ADC achieves a sampling rate of 1.0 GS/s and 110mW power consumption in a performance efficient way.

ACKNOWLEDGEMENT

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TABLE I. PERFORMANCE SUMMARY AND COMPARISON

Parameter	[3]	[5]	[2]	This work
Technology	0.35-μm	90-nm	90-nm	0.13-μm
Sampling Rate	300MS/s	800MS/s	1.1GS/s	1.0GS/s
Resolution	7bit	7bit	7bit	7bit
ENOB	6.02bit@ 60MHz 5.77bit@ 160MHz	6.14bit@ 10MHz 5.29bit@ 200MHz	6.5bit@ 29MHz 5.7bit@ 400MHz	6.63bit@ 10.7MHz 6.0bit@ 498MHz
ERBW (MHz)	60	200	300	490
DNL/INL (LSB)	0.6/1	0.80 /1.3	0.36 /0.46	0.47/1.14
Supply (V)	3.3V	1.2V/2.5V	1.3V	1.5V/2.5V
Power (mW)	200	120	92	110
Active Area (mm^2)	1.2	0.32	0.38	0.32
Fom (pJ/step)	25.6	4.25	1.69	1.13

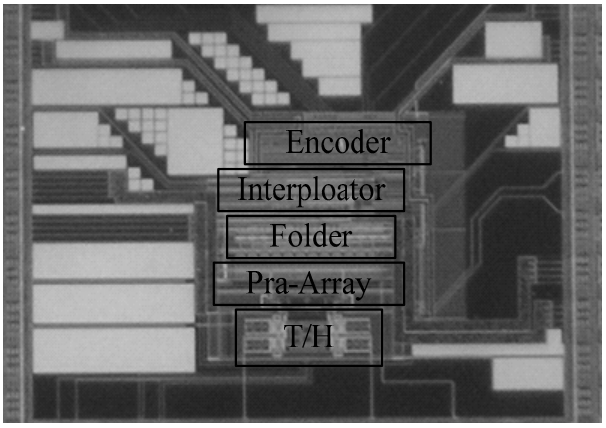

Fig. 6. The ADC microphotograph

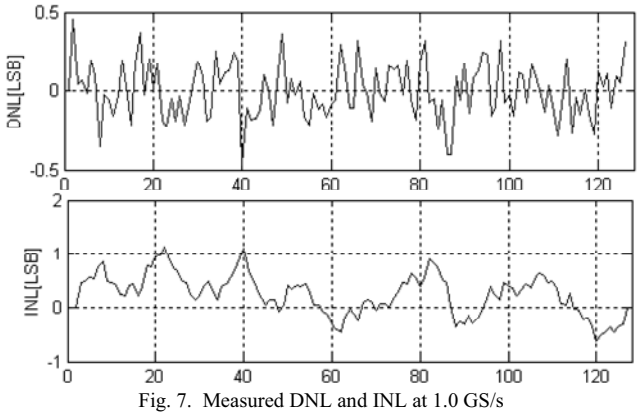

Fig. 7. Measured DNL and INL at 1.0 GS/s

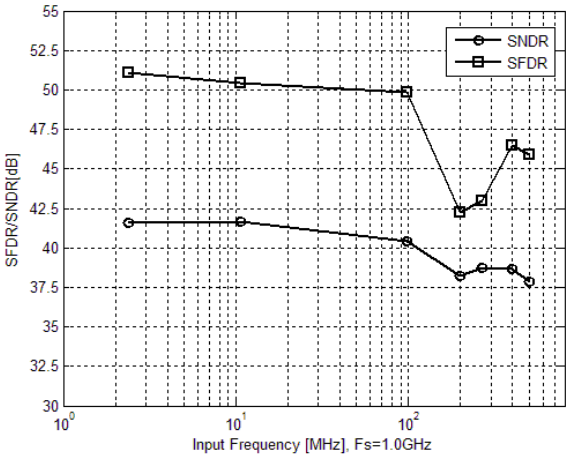

Fig. 8. Measured input frequency dependence of SNDR and SFDR

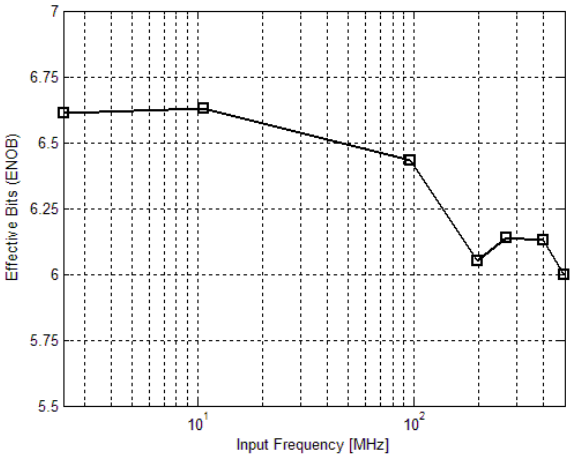

Fig. 9. Measured input frequency dependence of Effective Bits

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