A 40-mW 7-bit 2.2-GS/s Time-Interleaved Subranging CMOS ADC for Low-Power Gigabit Wireless Communications

I-Ning Ku, Zhiwei Xu, Yen-Cheng Kuan, Yen-Hsiang Wang, and Mau-Chung Frank Chang

***Abstract*—A 7-bit, 2.2-GS/s time-interleaved subranging CMOS analog-to-digital converter (ADC) for low-power gigabit wireless communication system-on-a-chip (SoC) is presented. A time-splitting subranging architecture is invented to significantly boost the speed of individual ADC channels. In addition, a low-power and fast-settling distributed resistor array for reference voltages is proposed to mitigate gain mismatches within channels. Moreover, the channel offset mismatches are calibrated through the digital- controlled corrective current sources embedded in the track-and-hold amplifiers of each sub-ADC. The prototype is implemented in 65 nm CMOS, occupying only 0.3 mm^2 chip area and consuming 40 mW at 2.2 GS/s from a 1 V supply. Measured signal-to-noise and distortion ratio (SNDR) and spurious-free dynamic range (SFDR) are 38 dB and 46 dB, respectively, with a 1.08 GHz input at 2.2 GS/s sampling rate. The effective number of bits (ENOB) is 6.0 bits at Nyquist rate, and the figure-of-merit (F.O.M.) is 0.28 pJ/conv.-step. This prototype has also been integrated into a gigabit self-healing wireless transceiver SoC.**

***Index Terms*—Analog-to-digital conversion, CMOS analog integrated circuits, subranging A/D converters, switched capacitor circuits, time-interleaved ADC (TI-ADC).**

I. Introduction

THE ubiquitous access and usage of digital information content has inevitably increased the communication data rate requirement for a variety of applications. Also, wireless has become the most popular communication medium due to its user-friendly and hassle-free operation with mobility support. To support the demands of high data rate wireless applications, the 7 GHz unlicensed millimeter wave (mm-Wave) band spanning from 57–64 GHz has been allocated by the FCC. It results in several standard developments, such as IEEE 802.15.3c, IEEE 802.11ad, WirelessHD, etc., dedicated to multi-gigabit wireless communication systems. One of their common and ultimate goals is to expedite the realization of widespread integrated circuits supporting large wireless data transfers.

To achieve gigabit wireless communication in the 7 GHz unlicensed 60 GHz band, a low order data modulation, such as BPSK or QPSK, is often adopted due to the wide applicable bandwidth and modest circuit implementation complexity. Therefore, medium-resolution (6–8 bits), high-speed (> 1 GS/s) CMOS ADCs are particularly critical to provide power-efficient, low-cost SoC solutions for such applications [1]–[6]. Though a single ADC running beyond GHz is feasible in the advanced CMOS nodes, a time-interleaved ADC is preferable due to its capability to achieve better power efficiency by combining multiple sub-ADCs operating at a lower sampling rate to deliver the required high sampling rate. The time-interleaved architecture, however, suffers from channel mismatches in timing, offset, and gain among individual sub-ADCs. Also, as the number of channels increases, the total area increases proportionally, which significantly complicates the associated routing of multiple phase clock signals and digital outputs. The long routing wires of the clocks and outputs unavoidably introduce excessive parasitic capacitance, which results in a significant power penalty compared to individual sub-ADC. To achieve high power efficiency and performance, a proper choice of sub-ADC architecture and an effective strategy of alleviating channel mismatches are crucial to the time-interleaved ADC design.

Recent publications have adopted successive-approximation-register ADCs (SAR-ADCs) [3], [7] and pipelined ADCs [4] as the sub-ADCs in a time-interleaved architecture. Despite its power efficiency, the sampling rate of the SAR ADC is still limited since a large number of comparisons, at least one for each bit, needs to happen in each sampling period. Therefore, a time-interleaved SAR ADC requires a large number of channels, which in turn increases the overall chip area and power consumption. On the other hand, pipelined ADCs can operate at higher speeds; however, it imposes a stringent gain-bandwidth requirement on the op-amps, which becomes more and more difficult to realize as scaled CMOS supply voltages continue to decrease. With regard to the methodologies to mitigate notorious channel mismatches of time-interleaved ADCs, research has been conducted to mitigate these through digital signal processing (DSP) approaches [8]–[12]. However, their intensive usage of digital function blocks, such as adaptive filter and FFT processor, may lead to significant chip area or power consumption overhead after implementation, making those DSP approaches unfavorable for a modest resolution, high speed, while low power and compact ADC.

In this work, a 7-bit, 2.2-GS/s CMOS ADC utilizing a number of analog-centric and light-weight digital design techniques to

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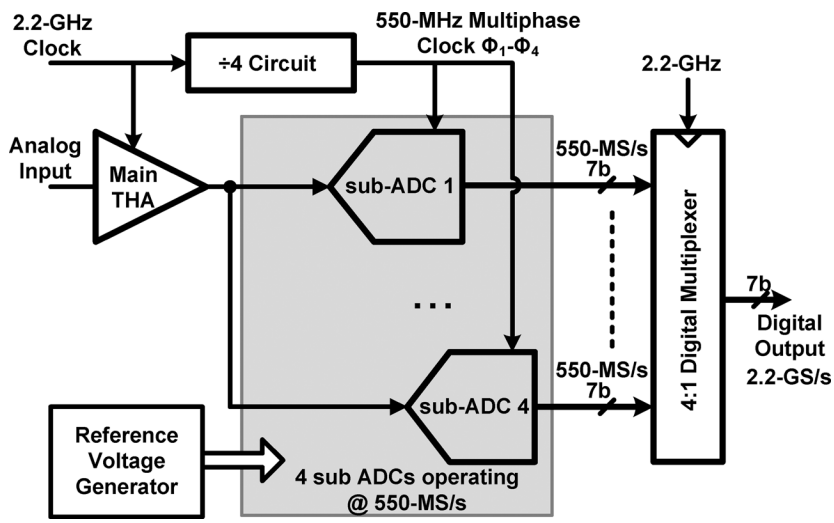

Fig. 1. Time-interleaved ADC architecture.

overcome the limitations of the time-interleaved architecture is described [13]. A time-splitting subranging ADC architecture that can offer significant higher sampling rate is invented, and is used as the sub-ADC in the interleaved ADC. This compact sub-ADC greatly reduces the required number of channels and thus the total chip area. To achieve high power efficiency, a distributed resistor array is further proposed to generate reference voltages for the time-interleaved ADC. It alleviates channel gain mismatches by exploiting better matching characteristics of poly resistors in the applied technology, while simultaneously maintains minimum power consumption overhead and fast settling response. Moreover, digitally controlled current sources embedded in each sub-ADC correct for dc offset mismatch between channels.

This paper is organized as follows. Section II introduces the architecture of the time-interleaved ADC, and Section III illustrates the proposed subranging ADC architecture. Two channel mismatch reduction techniques, distributed resistor array reference and digital offset calibration are presented in Section IV. Section V describes the circuit implementation of critical building blocks. Section VI presents the experimental results, and Section VII concludes the paper.

II. Time-Interleaved ADC Architecture

Fig. 1 shows the proposed time-interleaved ADC block diagram. A dedicated front-end track-and-hold amplifier (THA) samples the input signal at a full clock rate of 2.2 GHz. It removes the timing mismatches induced by unequal input delay and clock skew among interleaved channels. To achieve a compact and low-power realization in 65 nm CMOS, the number of ADC channels must be minimized. After eliminating SAR and pipelined architectures due to their low sampling rates and strict op-amp design requirements as mentioned above, the subranging and flash architectures are the remaining candidates to build the sub-ADCs. Subranging ADCs have a much smaller area and less power consumption than their flash counterparts though their conversion rate is lower. To compensate for this speed difference, a time-splitting high-speed 7-bit sub-ADC with $> 550\ \mathrm{MS/s}$ sample rate is invented, and adopted as the sub-ADC architecture. It reduces the required number of interleaved ADC channels down to four, and greatly simplifies the mismatch calibration and routing complexity. After sub-ADC quantization, the digital outputs from individual sub-ADCs are then multiplexed to constitute a full rate 2.2 GS/s digital output. The 550 MHz multiphase clocks for each sub-ADC are generated by a divide-by-four circuit, where the four-phase clock outputs are delayed by a 90° phase shift from each other. An on-chip reference generator distributes the reference voltages to the sub-ADCs, and provides current biases for each circuit block.

III. Time-Splitting Subranging ADC

Through two-step conversion, the subranging architecture avoids the exponential growth in power and area of the flash architecture, while maintaining fairly high speed operation. The conventional subranging architecture, however, hardly meets the design specification of 550 MS/s due to a tight timing budget. In order to boost the subranging ADC operating speed, the tight timing budget, which mandates a complete signal quantization within a clock period, must be broken. We, herein, proposed a time-splitting architecture to relax the timing budget by accomplishing the conversion of the subranging ADC in two clock phases instead of one through pipeline processing. Fig. 2 shows the architecture of the 7-bit subranging ADC. It consists of a sub-THA, a 4-bit coarse ADC (CADC) and a 4-bit fine ADC (FADC). The quantization procedure occurs in two phases. In phase 1, the sub-THA tracks the input signal and CADC is in reset mode, where it samples the reference voltage. In phase 2, the sub-THA output is connected to the CADC, where it is in amplification mode, while FADC samples the sub-THA held output voltage V_x. Then in the following phase (phase 1), the references is connected to the FADC, where it amplifies the difference between V_x and the corresponding reference voltage based on CADC digital output $D\langle 3:0\rangle$. As revealed by the timing diagram in Fig. 3(a), CADC must perform amplification, comparison and digital

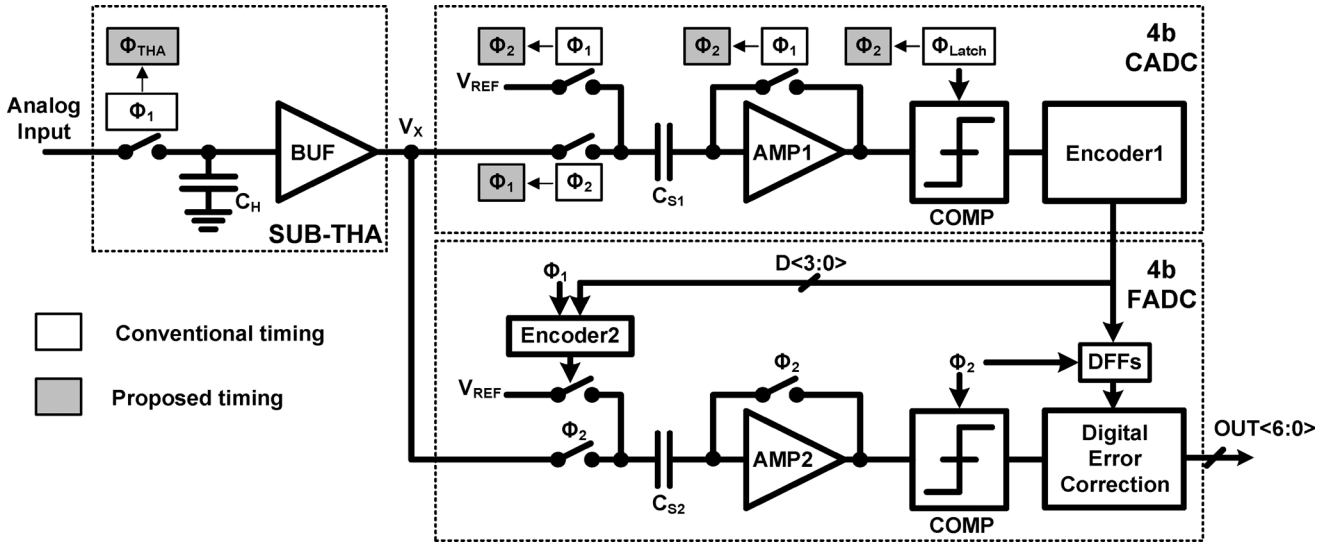

Fig. 2. Two-step subranging ADC architecture.

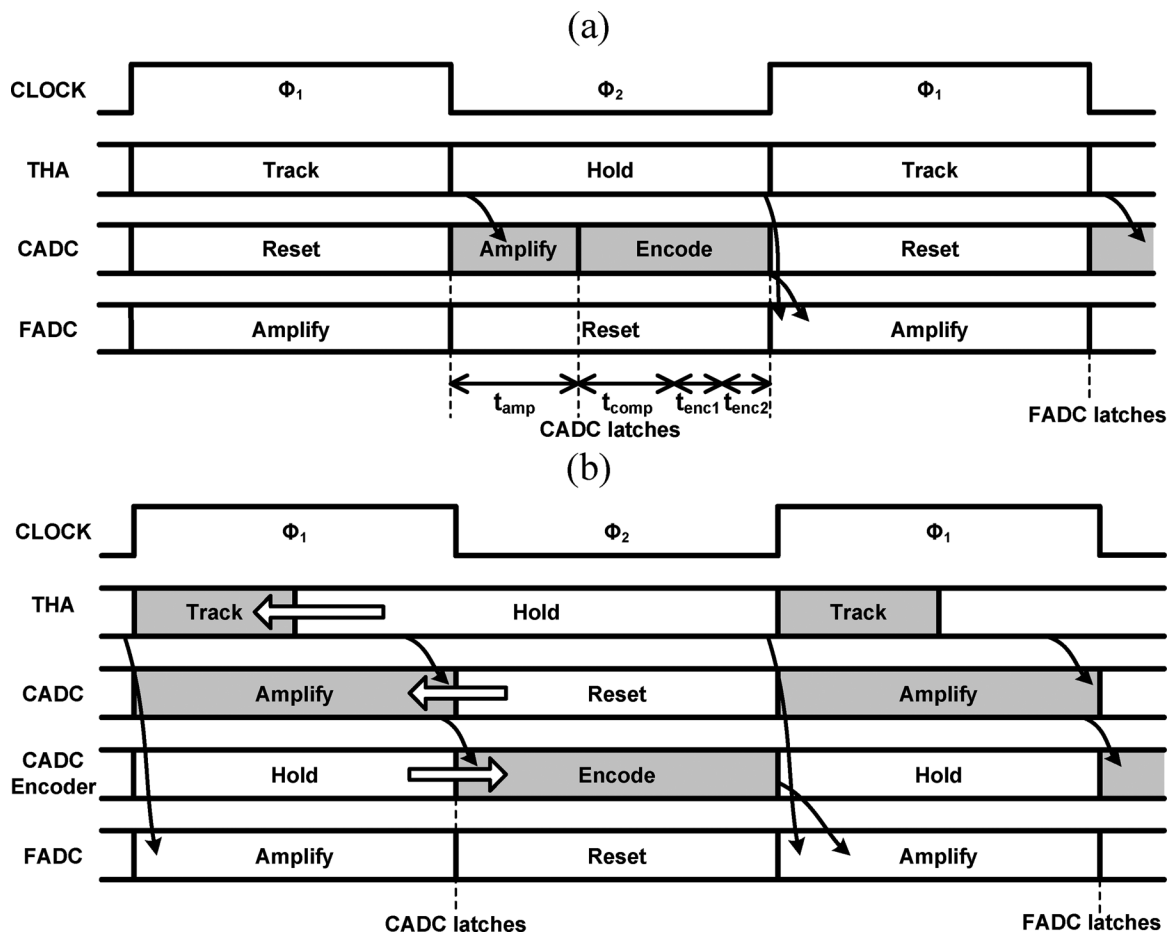

Fig. 3. (a) Conventional timing diagram. (b) Proposed time-splitting timing diagram.

encoding within half a clock cycle. The time allowed for amplification is expressed as

$$t_{amp} = \frac{T_S}{2} - (t_{\rm comp} + t_{\rm enc1} + t_{\rm enc2}) \quad (1)$$

where T_S is the sampling period, $t_{\rm comp}$ is the comparator regeneration time and $t_{\rm enc1}$ & $t_{\rm enc2}$ are the digital encoding time of the CADC and FADC, respectively. In the employed 65 nm CMOS technology, the typical comparator regeneration time and digital encoding time are around ~ 200 ps. These become worse over process corner and temperature variation, granting insufficient time for the CADC amplification, thereby limiting the sampling rate of a conventional subranging ADC. Either an extra sample-and-hold (S/H) for time-interleaving is

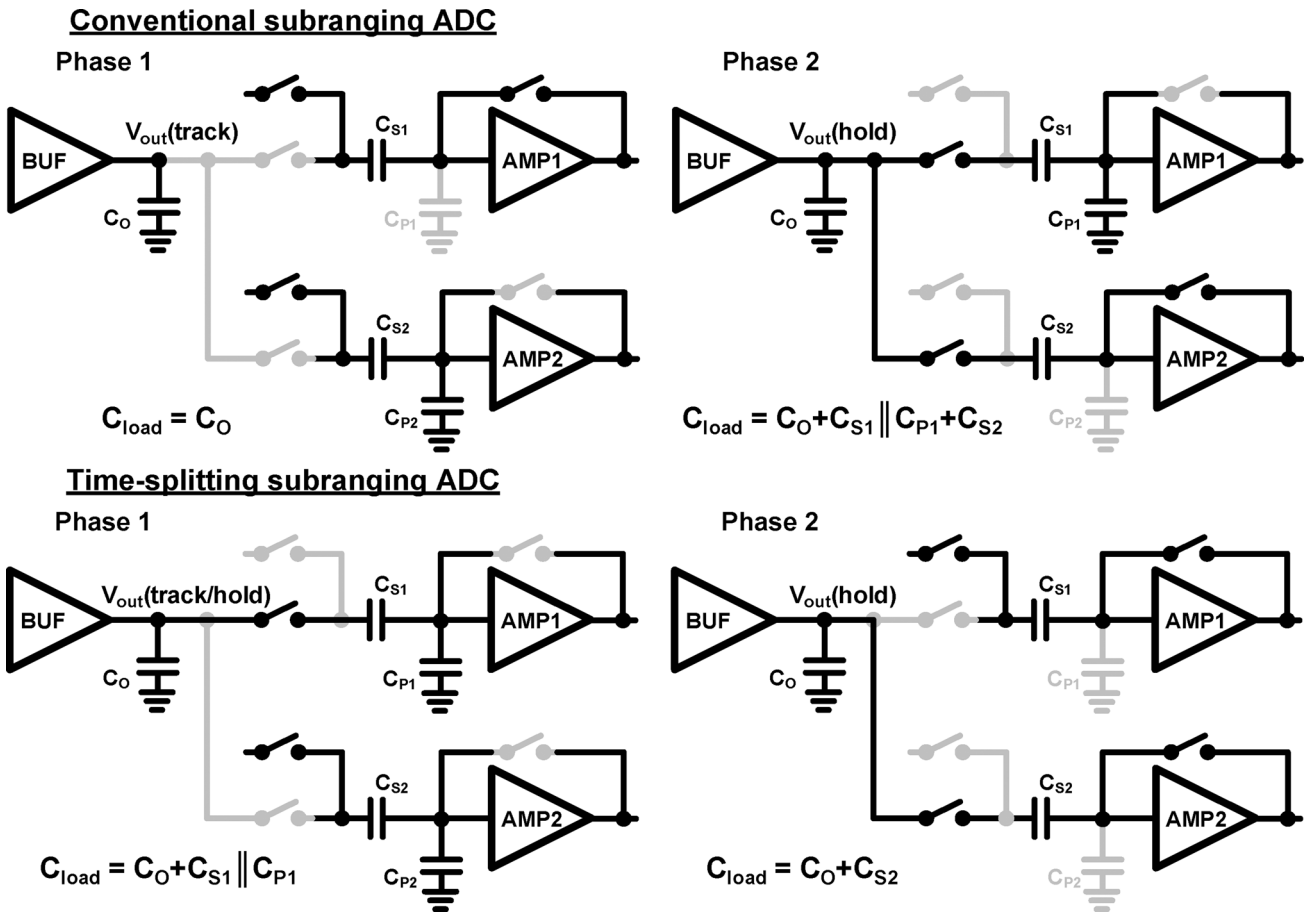

Fig. 4. Load reduction in sub-THA for conventional and proposed architecture.

required [14], which increases the total chip area, or extensive amount of power is consumed to boost up the subranging ADC speed [15].

To overcome this limitation and break the tight timing budget, a time-splitting subranging architecture is proposed. Its timing diagram is illustrated in Fig. 3(b). The track/hold time of the sub-THA is now shifted by ¼ clock cycle. Moreover, phase 1 and phase 2 are exchanged in the CADC. This phase-exchanging scheme leads to different sampling instances of CADC and FADC. In phase 1, the sub-THA tracks and amplifies the analog input signal, while CADC amplifies the sub-THA output V_x concurrently. In phase 2, CADC initializes the comparison and encodes the digital output $D\langle 3:0\rangle$ for the FADC, and then amplifies the signal in the subsequent phase. The proposed architecture has two main advantages: First, the CADC amplification and encoding time are now split into two phases instead of one. As shown in the timing diagram, the CADC amplification time is shifted to the left occupying the entire phase 1, where phase 2 is dedicated for CADC digital encoding. With a much more relaxed timing budget, the amplifier and comparator plus digital encoders now can operate separately within half a clock cycle. This empowers the subranging ADC to achieve a much higher conversion rate with lower power consumption. The second advantage is that this architecture distributes the loading to sub-THA in different phases by CADC and FADC. This is illustrated in Fig. 4. In the conventional subranging architecture, the sub-THA output capacitance loading is its intrinsic loading C_O in phase 1 and the combined input capacitance of CADC and FADC in phase 2. In the proposed architecture, the CADC and FADC capacitances are distributed to different phases, where it evens the loading imposed to the sub-THA in each phase. Since the required bandwidth for the sub-THA is proportional to the maximum loading across both phases, an evenly distributed loading can reduce the sub-THA bandwidth requirement leading to power saving, and result in further power reduction in the sub-THA buffer. The similar circumstance applies to the reference voltage buffer as well. The capacitive loading imposed to the reference voltage buffer is also distributed across both phases, thereby reducing its power consumption.

One issue associated with this architecture is the sub-THA incomplete settling in phase 1. As shown in Fig. 3(b), the sampled voltage across the CADC input capacitor may not settle within 7 bits accuracy at the end of phase 1 since only ¼ clock period is allocated for the sub-THA during CADC amplification. This incomplete settling, however, can be mitigated by using the digital error correction circuit. Similar to the early comparison scheme in pipelined ADC [17], as long as the error voltage is less than 4 LSBs (16 mV), it can be corrected with one bit redundancy in the CADC. Another drawback of this architecture is the reduced sub-THA tracking time. This can be compensated with a larger switch and a larger clock driver that slightly increase the dig-

ital power, which only constitutes a small portion of the overall power consumption. Simulation shows that the single-channel 7-bit subranging ADC running at 550 MS/s only consumes 7 mW, which is much smaller compared to subranging ADCs with similar specifications [15], [16] and validates the proposed architecture.

IV. Low-Power Channel Mismatch Reduction Techniques

To alleviate the effect of channel mismatch in time-interleaved ADCs, circuit techniques to improve matching between channels are required. Moreover, correction circuitries with minimum power and area overhead are essential, especially for high-speed, medium resolution ADCs. A pure digital solution is enticing due to its isolation from analog blocks that normally need to deliver speed and resolution. However, it may not be the most efficient because it does not correct the errors existing in each analog block. An alternative approach is to calibrate the error by using analog correction with fine digital controls, where the corrections are executed offline at a low speed. In this section, two low-power mismatch reduction techniques, distributed resistor array reference and digital offset calibration, are proposed to mitigate the non-idealities caused by gain mismatch and offset mismatch.

A. Distributed Resistor Array References

For sub-ADCs implemented in a flash-type architecture, the major source of gain mismatch is reference voltage mismatch. As shown in Fig. 5(a), a conventional time-interleaved ADC uses high-speed buffers to distribute reference voltages to each channel. This approach, however, has two serious drawbacks: first, the small buffer transistor, to ensure high-speed operation, generates reference voltage mismatches among interleaved channels, and therefore leads to large channel gain mismatch. Second, the high-speed buffer tends to consume large power, and a large number of high speed buffers further exacerbates the power consumption. To realize a low-power reference generator with small channel gain mismatch, a distributed resistor array as reference voltage generator is proposed, as shown in Fig. 5(b). Two low-speed buffers provide global voltages, V_{TOP} and V_{BOT}, to the four parallel resistor arrays in the sub-ADCs, where the reference voltages $\mathrm{V}_{\mathrm{REF,N}}$ are generated within each resistor arrays. With j resistors in each array, and a mismatch of $\Delta \mathrm{R}_{1\ldots j}$ for each resistor, the reference voltage $\mathrm{V}_{\mathrm{REF,N}}$ for the Nth-channel can be written as

$$
\begin{aligned}
&V_{\mathrm{REF,N}} \\
&= (V_{TOP} - V_{BOT}) \cdot \frac{R_2 + \cdots + R_{j-1}}{R_1 + \cdots R_j} \\
&= (V_{TOP} - V_{BOT}) \cdot \frac{(j-2)\,R \cdot \left(1 + \frac{\Delta R_2 + \cdots + \Delta R_{j-1}}{(j-2)R}\right)}{jR \cdot \left(1 + \frac{\Delta R_1 + \cdots + \Delta R_j}{jR}\right)} \\
&\approx \underbrace{(V_{TOP} - V_{BOT}) \cdot \frac{j-2}{j}}_{V_{\mathrm{REF}}} \\
&\quad \cdot \left(1 + \frac{\Delta R_2 + \cdots + \Delta R_{j-1}}{(j-2)\,R} - \frac{\Delta R_1 + \cdots + \Delta R_j}{jR}\right) \qquad (2)
\end{aligned}
$$

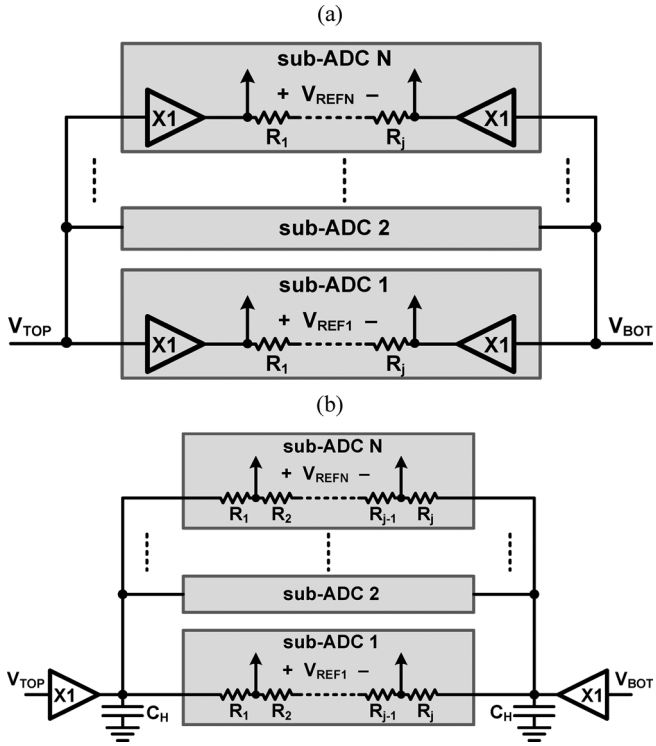

Fig. 5. (a) Conventional reference generator. (b) Proposed distributed resistor array as reference generator.

where $\mathrm{V}_{\mathrm{REF}}$ is the ideal reference voltage without resistor mismatch. The reference voltage mismatch then can be expressed as

$$
\frac{\Delta V_{\mathrm{REF}}}{V_{\mathrm{REF}}} \approx \left(\frac{4}{(j-2)\,j^2} + \frac{2}{j^2}\right)^{1/2} \cdot \left(\frac{\Delta R}{R}\right). \qquad (3)
$$

Given $\mathrm{j} = 18$ and poly resistor matching $\Delta \mathrm{R/R} = 0.85\%$ in the applied 65 nm CMOS, the reference voltage mismatch achieves an accuracy of 0.07%. Since the resistor array can be realized with small resistor value by increasing area and introducing minor speed penalty, a fast settling less than 1 ns can be expected. The two buffers only need to provide DC current to the resistor arrays instead of taking part in the high speed settling. With the same DC current, the proposed resistor array achieves a lower output impedance compared with that of the active CMOS devices in 65 nm CMOS. Consequently, a large amplifier gain-bandwidth is not necessary and the overall power consumption can be reduced noticeably. Two additional large capacitors are applied at the buffer output to further stabilize the reference voltages and reduce the kickback noise from the sub-ADCs. In summary, the proposed distributed resistor array can provide accurate multi-channel on-chip voltage references with much lower power consumption than conventional active CMOS buffer realization.

B. Channel Offset Calibration

Channel offset mismatch originates from the DC offset of sub-ADCs and contributes to noise tones at frequencies $\mathrm{f_s}/4$ and $\mathrm{f_s}/2$ [18], [19], where $\mathrm{f_s}$ is the sampling frequency. The conventional way of reducing mismatch is to increase transistor size, hence averaging out the random process variation. However, in

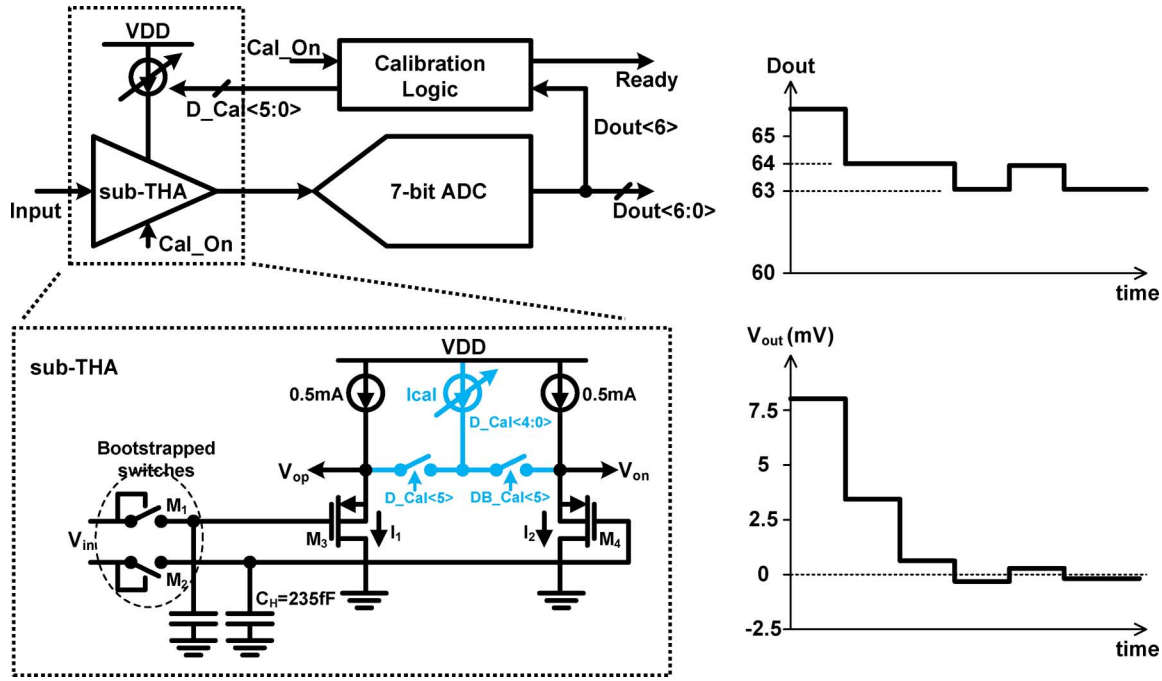

Fig. 6. Architecture of channel offset calibration circuit and its calibration procedure.

order to obtain an offset voltage less than 1/10 LSB, a large transistor dimension is required. This not only inevitably increases the total chip area, but also results in large sub-ADC input capacitance. To alleviate this tradeoff, transistors with minimum size are employed and the corresponding DC offsets of each channel are calibrated out digitally during start-up. Fig. 6 shows the architecture of the channel offset calibration circuit. For each individual channel, the input-referred offset is corrected by adjusting additional binary-weighted current sources inside the sub-THA buffers [20]. During calibration, the clock rate is lowered to 100 MHz due to the speed limitation of the synthesized calibration logic. The sub-ADC input terminals are connected together, and the digital outputs are read out to determine the offset voltage. Assume the source follower has unity gain, and let $\mathrm{I}_1 = \mathrm{I} + \Delta\mathrm{I}/2$ and $\mathrm{I}_2 = \mathrm{I} - \Delta\mathrm{I}/2$, the standard deviation of the offset voltage at the sub-ADC input can be expressed as

$$\begin{aligned} V_{os,\mathrm{in}} &= V_{os,\mathrm{sw}} + V_{os,\mathrm{subTHA}} + V_{os,ADC} \\ &\approx \underbrace{\frac{(WL)_{1,2} C_{ox} \Delta V_{th1,2}}{\sqrt{2}\cdot C_{\mathrm{H}}}}_{\text{switch charge injection}} \\ &\quad \underbrace{+\sqrt{2}\cdot \Delta V_{th3,4} + \sqrt{\frac{I}{2\mu_p C_{ox}(\frac{W}{L})_{3,4}}}\cdot\frac{\Delta I}{I}}_{\text{sub-THA offset}} + V_{os,ADC} \end{aligned} \tag{4}$$

where $\mathrm{V}_{os,\mathrm{sw}}$ is the charge injection mismatch of the sampling switch M_1&M_2, $\mathrm{V}_{os,\mathrm{subTHA}}$ is mismatch of input device M_3&M_4 and $\mathrm{V}_{os,ADC}$ is the mismatch of ADC itself. By adjusting the corrective current $\Delta\mathrm{I}$, it is able to correct the offset voltage, which is typically dominated by the threshold voltage mismatch of M_3&M_4. The calibration procedure is illustrated as follows (Fig. 6): In the first cycle, depending on the output code $\mathrm{D}_{\mathrm{out}}\langle 6\rangle$, the corrective current will switch in the direction of compensating the offset voltage. In the next few cycles, the corrective current $\Delta\mathrm{I}$ is then adjusted by switching on/off the binary-weighted current sources $\mathrm{I}_{\mathrm{cal}}$ in sequence to calibrate the offset voltage, as indicated in (4). As shown in Fig. 6, the digital output toggles between 63 and 64 at the end of calibration, and the offset voltage converges to a finite small value in six clock cycles. The calibration is able to correct a maximum offset voltage of 10 mV and an accuracy of more than 10 bits can be achieved. Since the calibration is executed offline, it consumes negligible power when the ADC is in normal operation. It is worth noting that the introduction of the calibration current cells in the sub-THA buffer only increases the power consumption negligibly to maintain an identical buffer gain-bandwidth due to their small capacitance load.

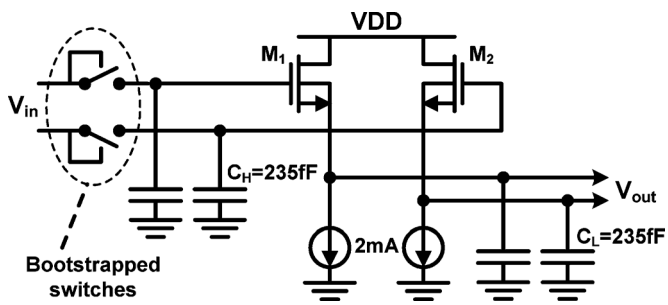

Fig. 7. Schematic of the main THA.

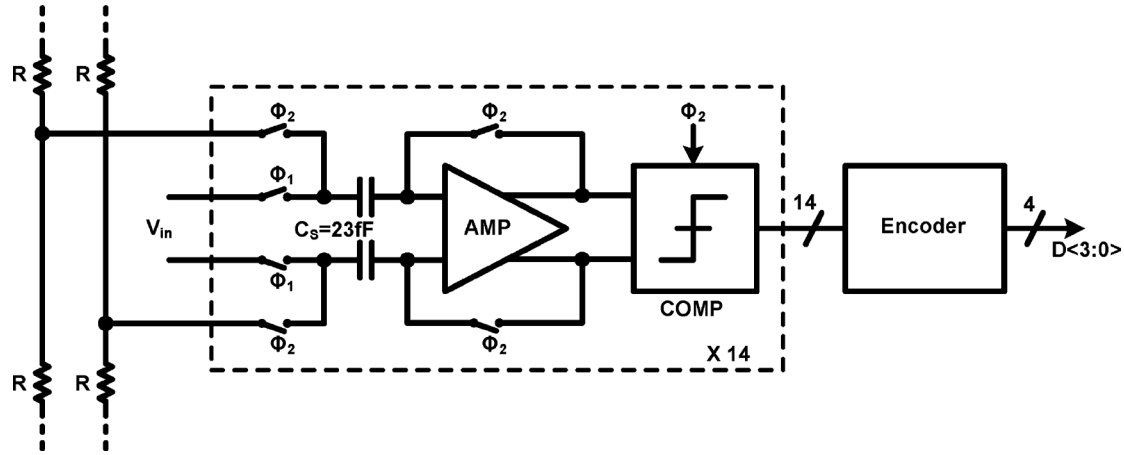

Fig. 8. 4-bit CADC block diagram.

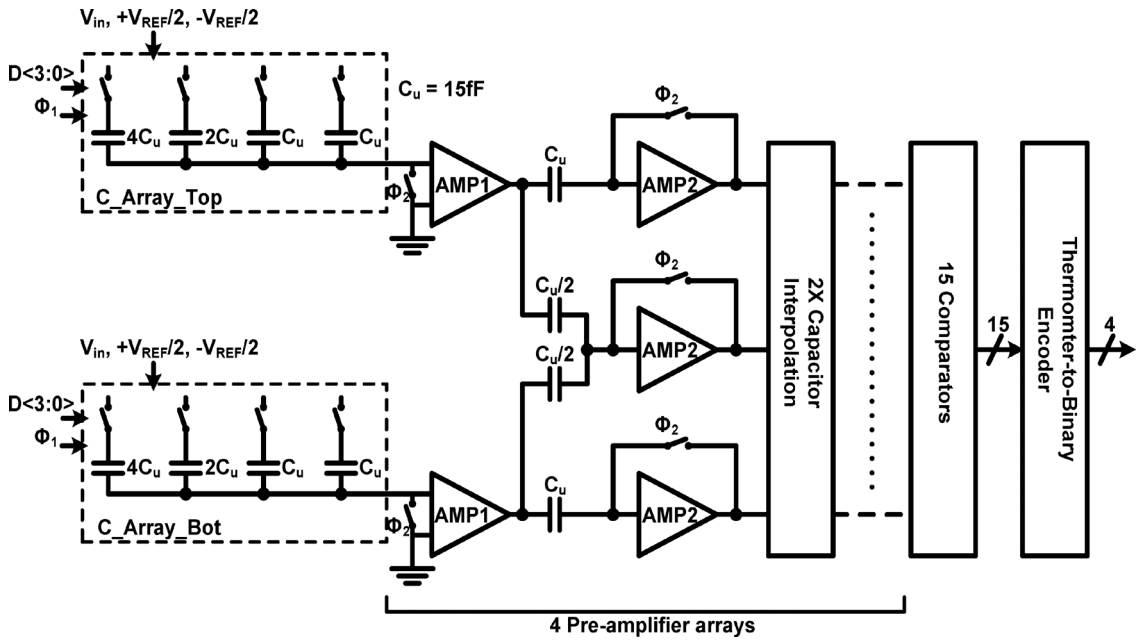

Fig. 9. 4-bit FADC block diagram.

V. Circuit Implementation

A. Main Track-and-Hold Amplifier

In this work, a main THA operating at full clock rate of 2.2 GS/s is designed to capture an input signal bandwidth $<$ 1 GHz and remove the timing mismatch for the following interleaved channels. As illustrated in Fig. 7, the main THA is implemented with an open-loop pseudo-differential architecture with bootstrapped switches used in [21]. An NMOS source follower is employed to operate at a high speed of 2.2 GHz. The sampling capacitors for both the main THA and sub-THA are $\mathrm{C_H} = \mathrm{C_L} = 235$ fF, which gives an input-referred noise of 440 μV. While threshold voltage variation due to body-effect can be avoided by tying the bulk of $\mathrm{M_{1,2}}$ to the source, nonlinearity caused by channel length modulation still remains. Nevertheless, this effect is tolerable for a 7-bit application and simulation demonstrates that the maximum harmonic is < -62 dBc in worst-case corner.

B. Coarse ADC

The 4-bit CADC block diagram is shown in Fig. 8. It consists of 14 unit arrays of pre-amplifier and comparator, and a resistor array that provides the coarse reference voltages. Since one redundant bit over-range is used for digital error correction, the noise and offset requirements of the CADC are greatly relaxed. A maximum error up to 16 mV (4 LSB) can be tolerated. Consequently, the associated transistor and capacitor sizes can be made small, resulting in more power and area saving.

C. Fine ADC

Since the FADC determines the overall linearity of the converter, it is required to obtain an accuracy of 7-bit resolution. Fig. 9 illustrates the block diagram of the 4-bit FADC. Two set of binary-weighted capacitor arrays determine the reference level for the FADC according to the CADC digital output $\mathrm{D}\langle 3:0\rangle$. To minimize the comparator offset, four cascaded pre-amplifier arrays preceding the comparator array are implemented. To

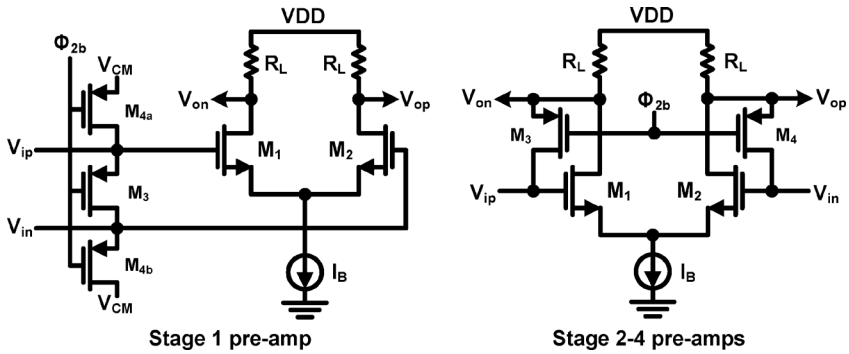

Fig. 10. FADC pre-amplifiers.

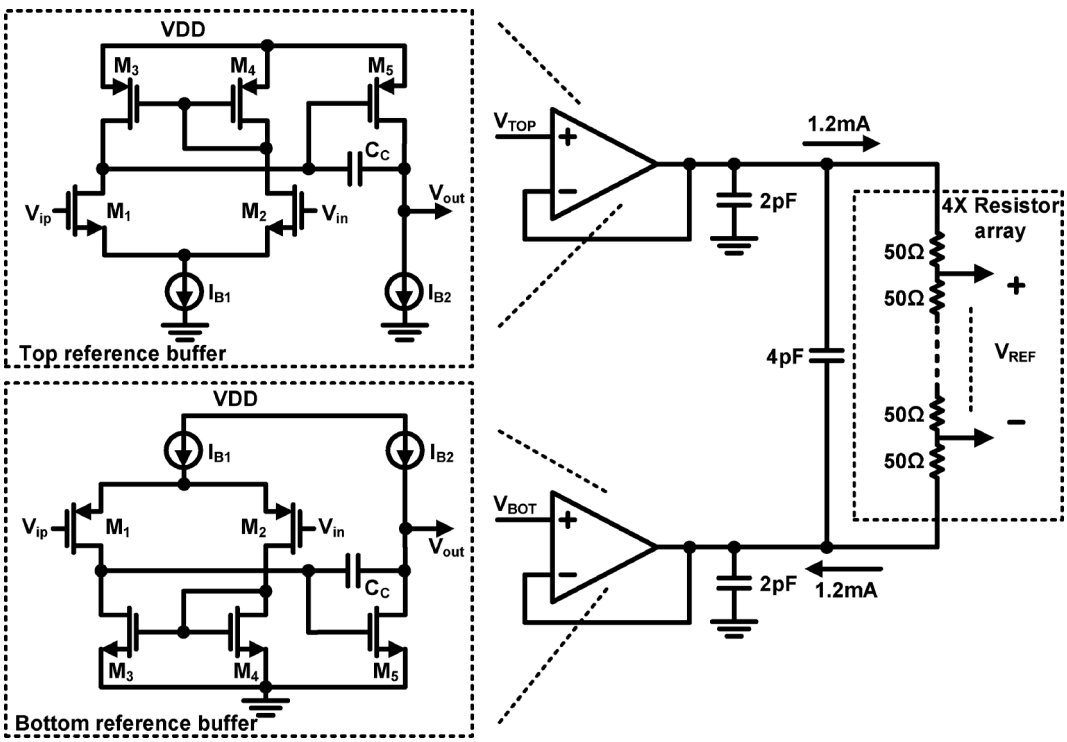

Fig. 11. Schematic of the reference voltage buffers.

satisfy a low kT/C noise requirement, a unit capacitor with a value of 15 fF is chosen, which gives a total capacitance of 16×15 fF $= 240$ fF differentially in each capacitor array. The large capacitance not only results in large area penalty, but also add excessive loading to the sub-THA. Therefore, two times interpolation is employed in each pre-amp stage so that only two sets of large sampling capacitor arrays are required, instead of fifteen sets of capacitor arrays. Capacitor interpolation [22] is used in this design for two reasons: First, it doesn't require extra dummies to overcome boundary effect [23] as in resistor interpolation. Second, DC offset cancellation is adopted in each stage pre-amps through switched-capacitor input/output offset storage [24]. Fig. 10 shows stage 1–4 pre-amps for the FADC. The first stage pre-amp uses output offset storage, where smaller sampling switches are utilized to reduce charge injection. Stage 2–4 pre-amps use input/output offset storage, which is more power efficient and offers faster reset speed. In order to reduce power consumption, a dynamic comparator [17] followed by SR latch is implemented in this design.

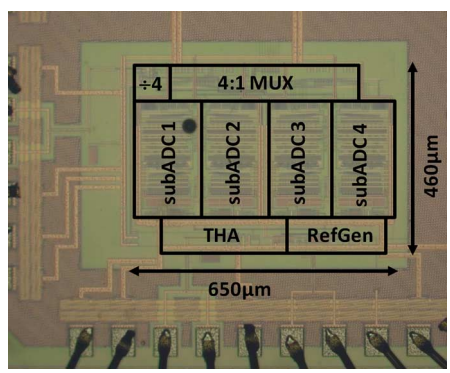

Fig. 12. Die micrograph.

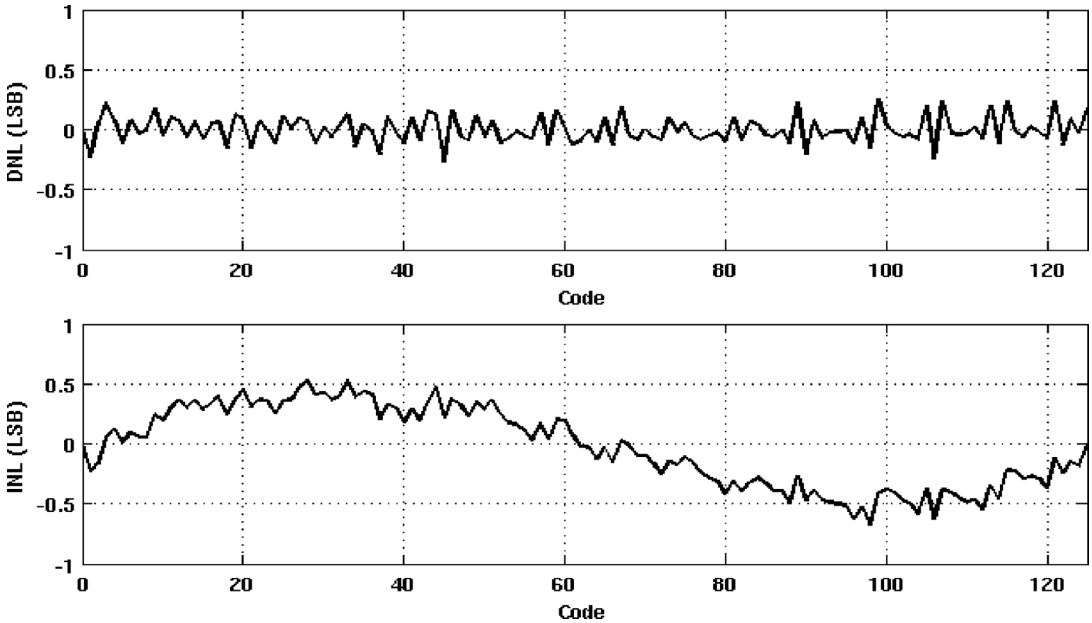

Fig. 13. Measured DNL and INL.

D. Reference Voltage Buffers

As mentioned in Section IV, two low-speed buffers are required to distribute the reference voltage to each interleaved channel. Since they only need to provide DC current for the four parallel resistor arrays, their power consumption can be small. As shown in Fig. 11, a two-stage amplifier with classical Miller compensation is employed as unity-gain reference buffer. For fast settling response, small unit resistor value of 50 Ω is selected for the resistor array and results in 1.2 mA reference ladder current. In addition to 2 pF decoupling capacitors to ground, a 4 pF capacitor is connected differentially at the buffer outputs to stabilize the differential reference voltage V_{REF}. From simulation, the total power consumption of the two reference buffers is only 2 mW. To guarantee the matching performance, symmetrical tree layout for reference voltage distribution is adopted to minimize the imbalance in metal routing wires. Moreover, all the resistor arrays are kept in the same orientation surrounded with small resistor dummies.

VI. Experimental Results

The prototype ADC has been fabricated in 65 nm GP CMOS, and occupies 0.3 mm^2 active area, as shown in the die micrograph of Fig. 12. At 2.2 GS/s, the ADC consumes 40 mW from a 1 V supply. To characterize the ADC, the digital outputs are sampled off-chip with a decimation factor of 15. Fig. 13 shows the measured DNL and INL of the ADC, which are $-0.27/0.26$ LSB and $-0.68/0.53$ LSB, respectively. Fig. 14 shows the measured FFT spectrum of the ADC with a 0.5 V_{pp}, 4 MHz & 1.08 GHz input signal at 2.2 GS/s. The measured SNDR and SFDR are 39 dB and 48 dB, respectively, for 4 MHz input frequency and 38 dB and 46 dB, respectively, for 1.08 GHz input frequency. According to the measured spectrum, the ADC performance is limited by the spurious tone caused by channel mismatch as well as the 3rd harmonic. The measured offset mismatch agrees well with designed offset calibration capability; however, the $f_s/4 \pm f_{in}$ and $f_s/2 \pm f_{in}$ spurs are larger than originally predicted. We suspect that this results from the gain and bandwidth mismatches among the sub-THAs [19]. Moreover, the extra current required for offset calibration further degrades the matching in the sub-THAs. The 3rd harmonic degradation is mainly due to the THA switch bandwidth limitation and the unwanted parasitic capacitance at the gate of the THA switch, which can be improved by increasing the supply voltage.

TABLE I
Power Dissipation Distribution of the ADC

Main THA	4mW
4 sub-ADCs	28mW
Reference Buffer	2mW
Clock Generator	4mW
4:1 Multiplexer	2mW
Total Power	40mW

Fig. 15 plots the SNDR and SFDR of the converter versus input signal frequency. At a fixed 2.2 GS/s sampling rate, the SNDR and SFDR are relatively constant and achieved an effective resolution bandwidth (ERBW) of 1.8 GHz. Fig. 16 plots the SNDR and SFDR of the converter versus sampling frequency with a fixed input frequency of 1 GHz. The ADC also demonstrates an ENOB > 5.5 bits at 2.6 GS/s. To quantify the effect of supply voltage on ADC performance, the SNDR and SFDR versus supply voltage is shown in Fig. 17. As shown in the figure, the ADC performance deteriorates with a lower supply, which is dominated by 3rd harmonic distortion and gain mismatch spurs. This implies a limited bandwidth of the main THA switch, and bandwidth mismatches among sub-THA switches, due to large tracking switch on-resistance. With a higher supply voltage, the effective V_{gs} of the bootstrapped

TABLE II
PERFORMANCE SUMMARY AND COMPARISON

	This Work	[3]	[4]	[5]	[6]
Process	65nm	45nm	90nm	65nm	65nm
Architecture	TI Subranging	TI SAR	TI Pipeline	Pipeline	Flash
Resolution (bit)	7	7	7	8	8
Sampling Rate (GS/s)	2.2	2.5	1.1	2.4	1.5
Supply (V)	1.0	1.1	1.3	1.0	1.0
ENOB @ Nyquist (bit)	6.0	5.4	5.7	4.9	5.7
Power (mW)	40	50	92	318	35
F.O.M. (pJ/conv.-step)	0.28	0.48	1.18	3.2	0.42
Active Area (mm^2)	0.3	1	0.37	0.042	0.5

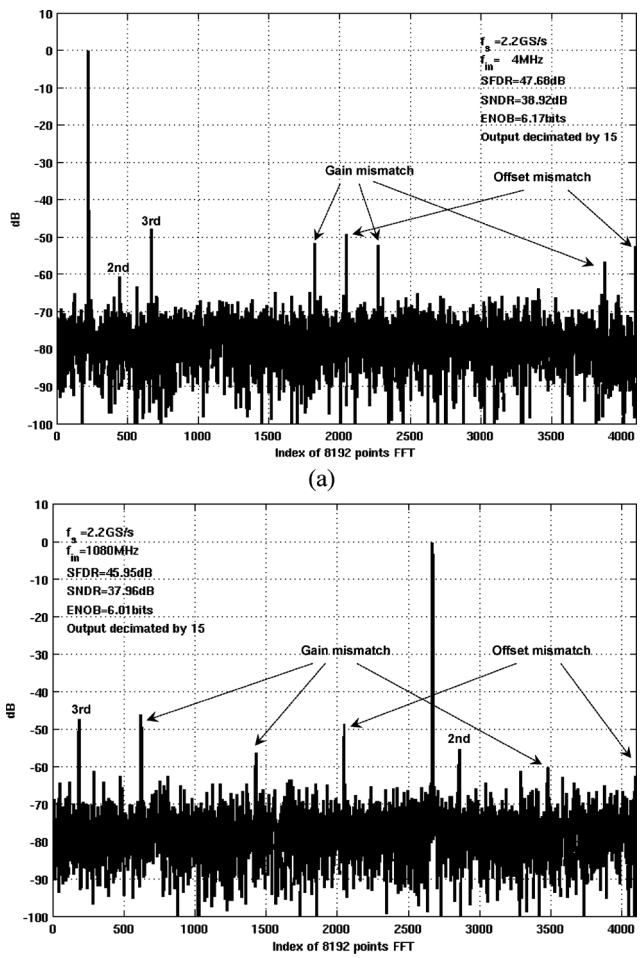

Fig. 14. Measured spectrum at 2.2 GS/s with (a) 4 MHz and (b) 1.08 GHz input frequency.

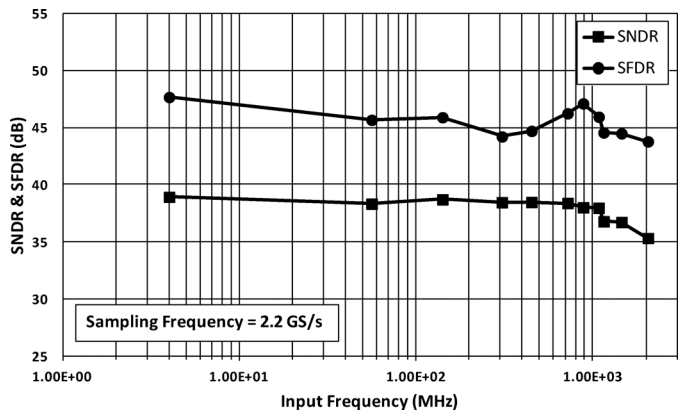

Fig. 15. Measured SNDR and SFDR vs. input frequency at $f_s = 2.2\ \mathrm{GS/s}$.

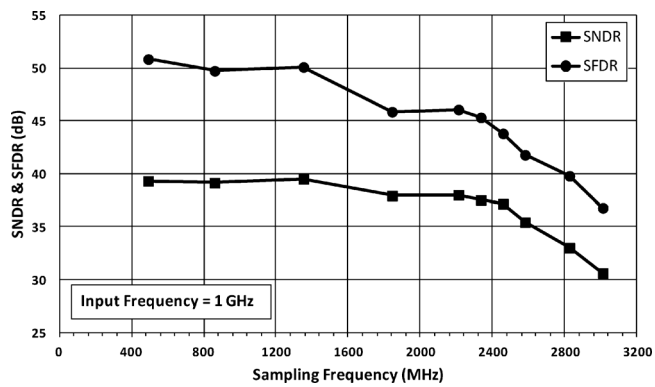

Fig. 16. Measured SNDR and SFDR vs. sampling frequency at $f_{in} = 1\ \mathrm{GHz}$.

switch increases, thus reducing the switch on-resistance. The prototype ADC achieves a figure of merit (FOM) of 0.28 pJ/conv.-step, which is defined as

$$\mathrm{FOM} = \frac{\mathrm{power}}{\min\left(f_s, 2\mathrm{ERBW}\right) \cdot 2^{\mathrm{ENOB},\min(f_s/2,\mathrm{ERBW})}}. \quad (5)$$

Table I shows the power dissipation distribution for this ADC. The performance summary and its comparison to state-of-the-art ADCs [3]–[6] with 7–8 bits resolution and $> 1\ \mathrm{GS/s}$ sampling rate is shown in Table II. To the authors' best knowledge, this ADC achieves the best F.O.M. and the second smallest active area in this category.

VII. CONCLUSION

A 7-bit, 2.2 GS/s time-interleaved subranging ADC for gigabit wireless communication systems has been described.

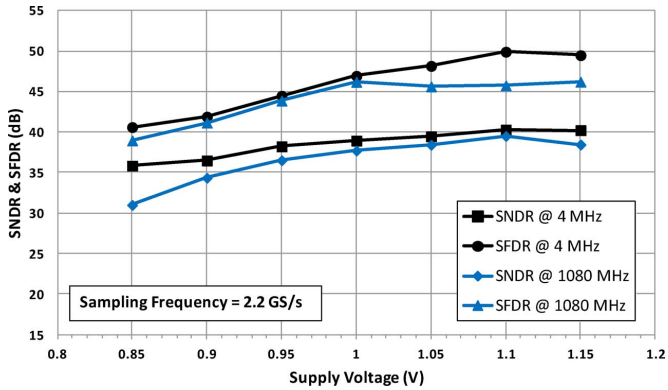

Fig. 17. Measured SNDR and SFDR vs. supply voltage at $f_s = 2.2\ \mathrm{GS/s}$.

The proposed time-splitting subranging architecture significantly increases the speed of individual ADC channels and reduces the total number of interleaved channels to only four. By employing a distributed resistor array to produce the voltage reference, channel gain mismatch is alleviated while maintaining low power consumption. Channel offset mismatch is calibrated through corrective current sources embedded in the sub-THAs with small area overhead and negligible power during normal operation. The ADC is implemented in a 65 nm CMOS process, occupying 0.3 mm^2 active area and consuming 40 mW. The measured ENOB is 6.0 bits at Nyquist rate with a F.O.M. of 0.28 pJ/conv.-step. This ADC has also been successfully integrated into a 60 GHz wireless transceiver for gigabit wireless applications.

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