A 6-Bit, 1.2-GS/s ADC with Wideband THA in 0.13-µm CMOS

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***Abstract*-This paper presents a 6-bit, 1.2-GSample/s flash ADC with new proposed wideband track-and-hold amplifier (THA) fabricated in TSMC 0.13-µm CMOS technology. The wideband THA employs a front-end super source follower (SSF), which has a very low input capacitance of only 0.2-pf, to boost analog bandwidth without any on-chip passive inductor. Moreover, the flatness of the data bandwidth of ADC will improve. The SSF can also relax the power consumption of the voltage buffer in the THA.**

I. Introduction

High speed (>1GHz) with medium to moderate (4-7 bits) resolution analog-to-digital converters (ADCs) are commonly used in read-write channel of a hard disk drive system, Gigabit Ethernet, wireless receivers and so forth. In general, ADCs are the dominant power hungry block for the whole analog front-end, thus reducing its power consumption is very important for many handheld wireless applications system. The proposed ADC is based on true single phase clock (TSPC) and designed with averaging [1] and interpolation techniques [2]-[5], so that the power consumption of digital circuits and preamplifiers, and the output loading of THA can be reduced.

Furthermore, the flatness of the data bandwidth (BW) of ADC is also an important specification for the wireless receivers, especially in ultra-wideband (UWB) communication system. In order to improve the flatness of ADC, we proposed a new wideband THA with front-end SSF. Using the dedicated wideband THA at front, it is not only used to eliminate skew among comparators in the ADC, but also it can boost analog BW without any on-chip passive inductor [6], so that the flatness of the data BW of ADC can be improved. At the same time, it also has a very low input capacitance around 0.2-pf, very suitable for RF interface. Moreover, based on the same BW requirement, the SSF can relax the power consumption of the voltage buffer in the THA, which is used to drive the first stage preamplifier capacitive load. According to experimental results, the flatness of ADC only decreases 1.2-dB from 1-MHz to 300-MHz input frequency at 1.2-GS/s.

II. ADC Architecture

The flash architecture shown in figure 1 consists of both analog and digital circuit blocks. The analog block includes a wideband THA, multistage preamplifier, an on-chip reference generator, bandgap reference (BGR) and biasing circuits. The wideband THA tracks and holds the input differential signals to provide a DC level for the first stage preamplifier. The multistage preamplifiers are necessary to provide enough gain for the least significant bit (LSB) overcoming the comparators static and dynamic offset. Using averaging technique can reduce the offset contributed by the preamplifiers, and along with interpolation technique, the total power consumption of the preamplifiers can be reduced. On-chip reference generator combined with BGR circuit provides all the reference voltage levels. Biasing circuits provide the mirrored tail current for the wideband THA, the preamplifiers and the reference generator.

The digital block consists of the clock buffer, the comparator latch array and the encoder. The clock buffer provides the timing for the digital and analog blocks. The comparator latch regenerates the amplified signal from the preamplifiers. The encoder uses logic circuits instead of ROM. It converts thermometer code to binary code, which also employs Gray code to perform bubble error correction.

The current mode logic (CML) output buffer is used to drive the off-chip loading and it also provides low swing differential output signals to reduce transient noise coupling to the ADC core.

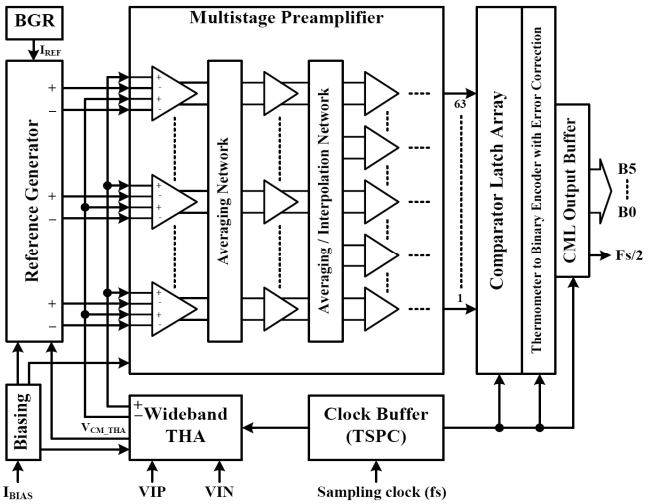


Fig. 1. Implemented ADC block diagram.

III. Implemented Design

A. Proposed Wideband THA

Figure 2 shows the proposed wideband THA schematic. It consists of a front-end SSF, a T/H circuit and a conventional source follower (CSF) voltage buffer. The T/H circuit is a NMOS switch M3, fabricated in deep n-well to remove body effect, combined with a holding capacitor, C_H, of 0.1-pF. After this T/H circuit, a CSF voltage buffer is used to drive the first stage preamplifier input capacitive load, C_{ADC}, and potentially its large self-load. The front-end SSF circuit is used to boost the analog BW without any on-chip passive inductor, as often required by other BW boost circuits, and to relax power consumption of the CSF voltage buffer. Specifically, this paper will focus more on the discussion of how front-end SSF can boost the BW of THA.

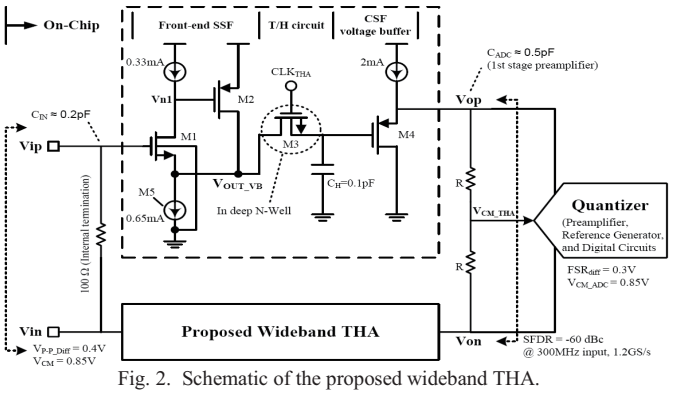


Fig. 2. Schematic of the proposed wideband THA.

Compared to some other high-speed ADCs, another CSF is used instead of front-end SSF to remove parasitic inductance effect and simplify input matching network. And that will result in dominated real poles which are contributed by C_H and C_{ADC}. When using front-end SSF, the transfer function for Vop(S)/Vip(S) will be very complicated in terms of AC, though its DC term is quite simple as shown in (1). With the help of in-house program, we can better analyze the AC results. The simplified AC transfer function of the V_{OUT_VB}(S)/Vip(S) and Vn1(S)/Vip(S) are shown in (2) and (3), respectively. Its related coefficients are shown in (4)-(6). Compared with SPICE simulation, the simplified functions are enough to reveal the BW boosting mechanism by SSF.

The pole-zero analysis based on SPICE simulation is shown in figure 3. When the input radian frequency (rad/s), ω, increases the Vn1/Vip would first encounter a real zero, Z1, at -335M (rad/s) before impacted by the second zero, Z2, and the first complex poles, P1 and P2. And then, the second complex poles, P3 and P4, create a peak in Bode diagram for Vn1/Vip shown in figure 4. Nonetheless, the pole-zero map of the V_{OUT_VB}/Vip, also shown in figure 3, shows a zero, Z3, is encountered after complex poles, P3 and P4. Still, it creates a peak in the Bode diagram for V_{OUT_VB}/Vip as shown in figure 4. Overall, the THA with front-end SSF has a BW boosting effect. The frequency response of THA with two different front-end voltage buffers, CSF and SSF, are shown in figure 5. The THA with front-end SSF has larger BW than the THA with front-end CSF at same DC gain through normalizations.

Another key design issue is that the gain boosted by Z1 will compress V_{DS} of the M1. When the input frequency goes up, the V_{DS} will get smaller compared with that at DC, so that the linearity would be degraded. Also by using standard small signal parasitic model, (2) and (3) seem to include several parasitic capacitance. But actually they all belong to device M2. M2 and C_H are the most critical devices for the BW optimization purpose.

$$T(S) \equiv \frac{Vop(S)}{Vip(S)} = T(S=0)\cdot T_{AC}(S)\Big|_{\frac{Vop}{Vip}} \approx \frac{g_{m,M1}}{g_{m,M1}+g_{mb,M1}}\cdot T_{AC}(S)\Big|_{\frac{Vop}{Vip}} \quad (1)$$

$$T_{AC}(S)\Big|_{\frac{V_{OUT\_VB}}{Vip}} \approx \frac{\frac{C_H\cdot C_{gs,M2}}{g_{m,M2}\cdot g_{ro,M3}}\cdot S^2 + \left(\frac{C_H}{g_{ro,M3}}+\frac{C_{gs,M2}}{g_{m,M2}}\right)\cdot S + 1}{a\cdot S^3 + b\cdot S^2 + c\cdot S + 1} \quad (2)$$

$$T_{AC}(S)\Big|_{\frac{Vn1}{Vip}} \approx -\frac{\frac{C_H\cdot C_{db,M2}}{g_{ro,M3}\cdot\left(g_{ro,M2}+g_{ro,M5}\right)}\cdot S^2 + \left(\frac{C_H+C_{db,M2}}{g_{ro,M2}+g_{ro,M5}}\right)\cdot S + 1}{a\cdot S^3 + b\cdot S^2 + c\cdot S + 1} \quad (3)$$

$$a \approx \frac{C_H\cdot\left(C_{gs,M2}\cdot C_{gd,M2}+C_{gs,M2}\cdot C_{db,M2}+C_{gd,M2}\cdot C_{db,M2}\right)}{g_{m,M2}\cdot g_{ro,M3}\cdot\left(g_{m,M1}+g_{mb,M1}\right)} \quad (4)$$

$$b \approx \frac{C_H\cdot\left(C_{gs,M2}+C_{gd,M2}\right)+C_{gs,M2}\cdot\left(C_{gd,M2}+C_{db,M2}\right)+C_{gd,M2}\cdot C_{db,M2}}{g_{m,M2}\cdot\left(g_{m,M1}+g_{mb,M1}\right)} \quad (5)$$

$$c \approx \left(\frac{C_H}{g_{ro,M3}}+\frac{C_{gs,M2}}{g_{m,M2}}+\frac{C_{ds,M2}}{g_{m,M1}+g_{mb,M1}}\right) \quad (6)$$

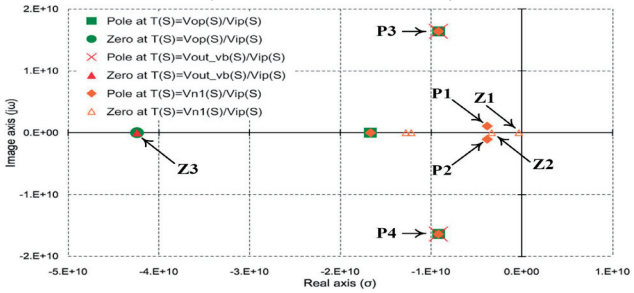


Fig. 3. Pole-zero map of different nodes versus node Vip.

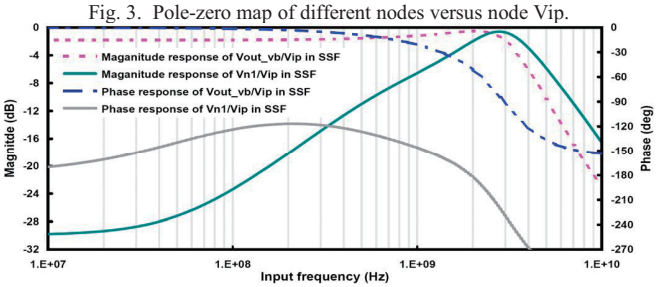


Fig. 4. Bode diagram of different nodes versus node Vip in SSF.

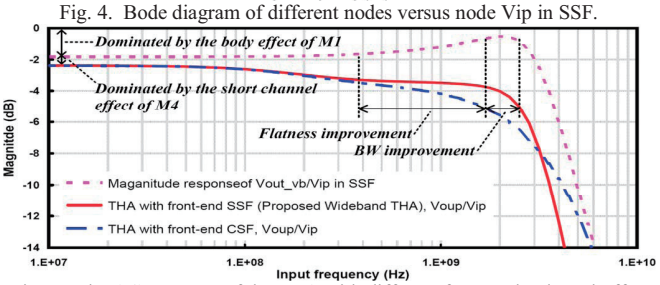


Fig. 5. The AC response of the THA with different front-end voltage buffer.

Due to the supply voltage is only 1.2-V, the input signal swing cannot be too high to insure decent linearity in the THA. In our design, we used differential input range of 0.4-V, while the input common mode is 0.85-V. According to post-layout simulation result, the THA with front-end SSF consumes about 5.3-mA. Compared to the THA with front-end CSF, the BW improved above 35%.

B. Reference Generator and BGR circuit

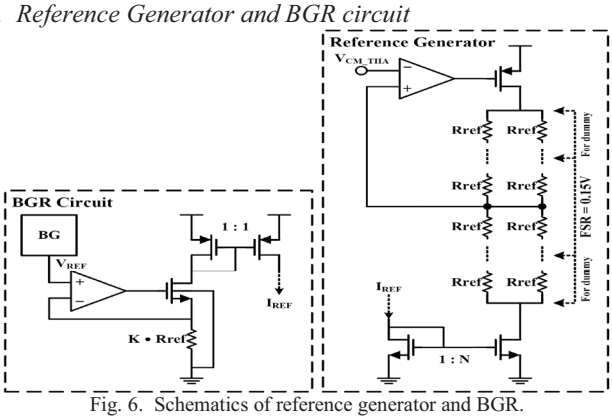


Fig. 6. Schematics of reference generator and BGR.

Figure 6 shows the schematics of on-chip reference generation and BGR circuit. The reference generator consists of a two-stage OTA, two column resistor ladders and a current mirror source, which is biased by BGR circuit to insure constant full scale range. Two inputs of the OTA are connected to the center taps of the two column resistor ladders and the output common mode of the wideband THA respectively. It can track the common mode voltage, which reduces the offset caused by process, temperature and voltage supply variations. Moreover, the two column resistor ladders are designed for better symmetrical routing on layout phase, which is important for dynamic performance in high speed ADC.

C. Multistage Preamplifier

A conventional flash ADC consists of a resistor ladder followed by 63 comparators. With 0.3-V differential input full scale range (FSR), combined with 6-bit resolution it will require for σ_{offset} smaller than a few millivolts for the comparators. This will result in a large and slow design. Therefore, the ADC applies amplification, averaging, and interpolation to relieve comparators offset requirements.

The schematic of the multistage preamplifier is shown in figure 7. It is implemented in four stages, which are designed under the UWB constraints of BW, gain and power consumption. The resistor averaging technique, which is interpolation for free, is used to reduce the offset contributed by preamplifiers. Also the dummy preamplifiers have to be deployed to remove the boundary effect. The numbers of dummy preamplifiers are optimized using the spatial filter theory developed in [1]. Using interpolation technique, it can reduce the number of preamplifiers and the output loading of the THA, thus reduce the analog power consumption. To have the best speed to power ratio, total interpolation by 8 with each stage by 2, except for the first stage, is chosen.

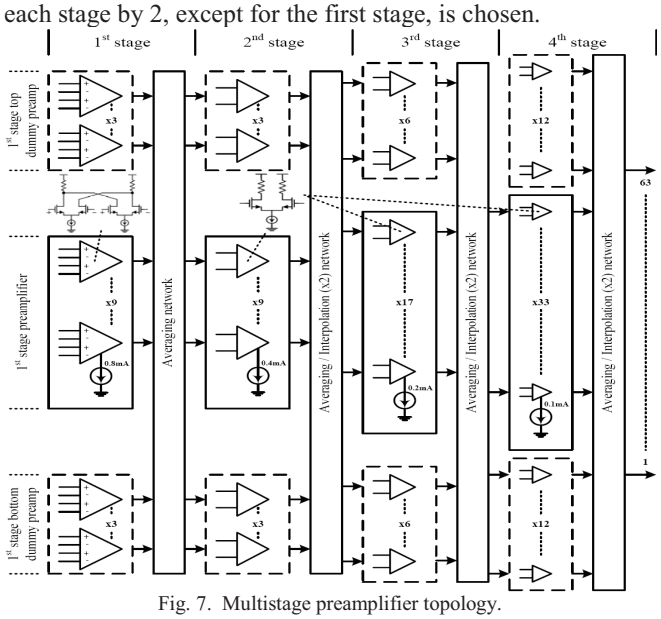


Fig. 7. Multistage preamplifier topology.

D. Digital Circuits

In general, comparator latch is a power hungry block in flash ADC. Therefore, the comparator latch in the ADC is implemented in dynamic logic structure, which has no static current, so that the power consumption of the ADC can be reduced. The schematic of the comparator latch based on TSPC [7] is shown in figure 8.

The overall ADC timing diagram and digital circuits are shown in figure 9, respectively. The THA clock, CLK_{THA}, is a delay signal of the comparator latch and the DFF clock, CLK_{CMP}. Noticed that the comparator latch is triggered near at the end of the THA on holding phase to ensure the differential input signal has being settled. Because of the ADC is based on TSPC, the schematic of the clock buffer is very simple. Moreover, the D flip-flop (DFF) is also implemented in TSPC.

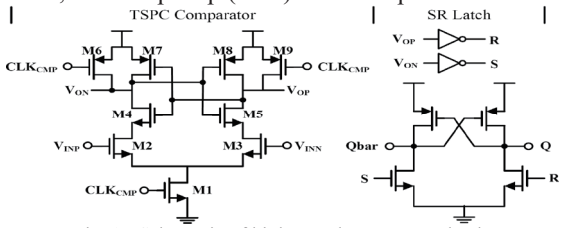


Fig. 8. Schematic of high-speed comparator latch.

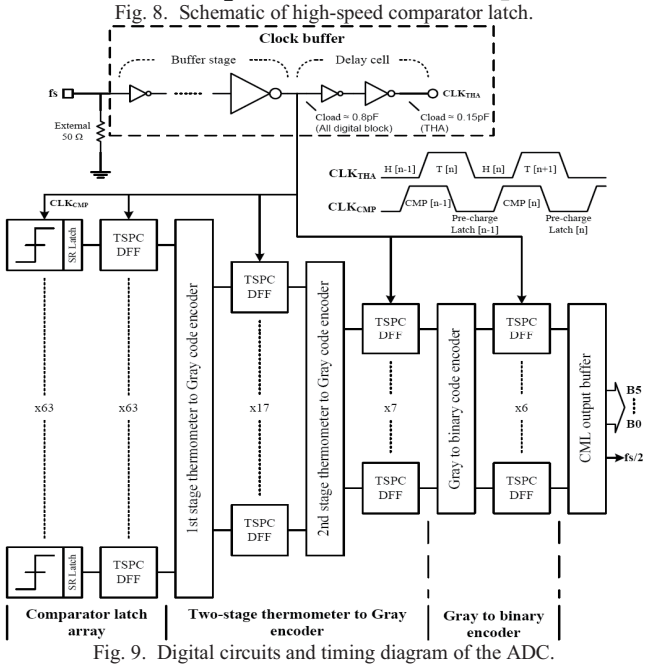


Fig. 9. Digital circuits and timing diagram of the ADC.

IV. Experimental Results

The maximum value of the DNL and INL, shown in figure 10, are within 0.33-LSB and 0.55-LSB, respectively. The dynamic performance is shown in figure 11 and figure 12, respectively. Operating at 1.2-GS/s, the ADC achieves an effective resolution bandwidth (ERBW) of 600-MHz, and 5.12 effective bits at 500-MHz input frequency. At 1.6-GS/s it achieves 5.05 effective bits for 300-MHz input frequency. Figure 13 is the output spectrum of an input signal of 500-MHz, with 1024-point FFT at 1.2-GS/s, indicating SFDR of 43.49-dBc, which is dominated by 2nd order harmonic. The chip microphotograph is shown in figure 14. All the ADC performances are summarized in table I. The ADC excluding CML output buffer consumes only 75-mW with internal references at 1.2-V supply and occupies 0.43-mm^2 active area.

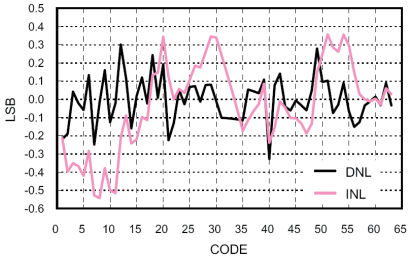


Fig. 10. Measured DNL/INL at 1.2-GS/s and 1-MHz input frequency.

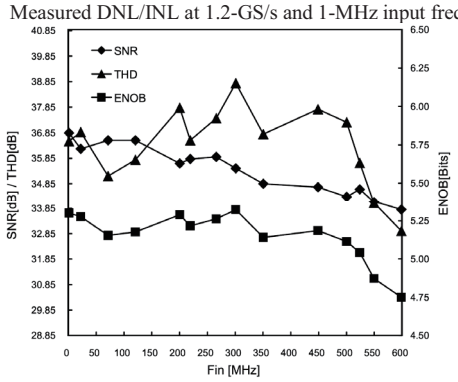


Fig. 11. Measured dynamic performance versus input frequency at 1.2-GS/s.

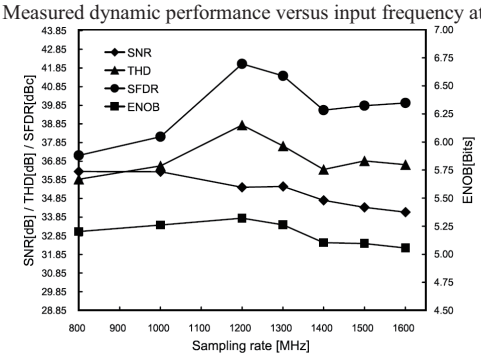


Fig. 12. Measured dynamic performance versus fs at Fin=300-MHz.

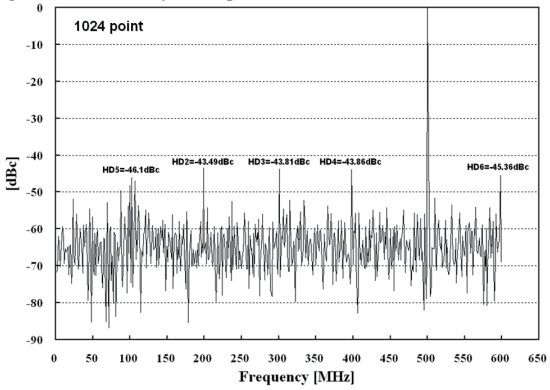


Fig. 13. Measured ADC spectrum normalized at 1.2-GS/s, Fin=500-MHz.

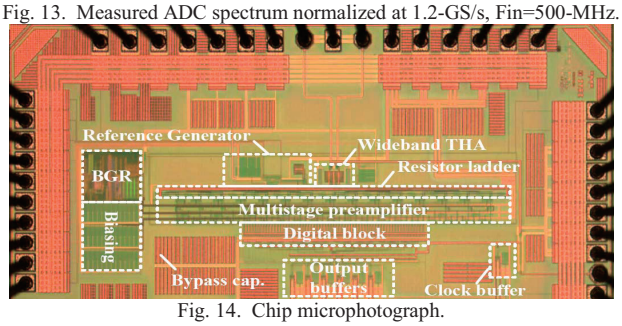
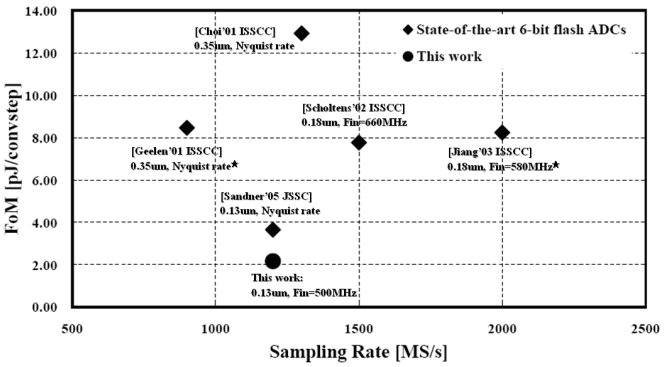


Fig. 14. Chip microphotograph.

Table I
ADC performance summary

Technology	**TSMC 0.13 µm CMOS**
Resolution	**6 bit**
Sampling Rate	**1.2 GS/s**
Input Range (Differential)	**0.4 Vp-p**
Input Common Mode	**0.85 V**
Input Capacitance	**0.2 pF**
DNL / INL @ 1.2GS/s	**0.33 LSB / 0.54 LSB**
ENOB @ Fin=300MHz	**5.32 bit @ 1.2 GS/s** **5.05 bit @ 1.6 GS/s**
@ Fin=500MHz	**5.12 bit @ 1.2 GS/s**
ERBW @ 1.2GS/s	**600 MHz**
Supply Voltage	**1.2 V**
Power Consumption (65% due to analog circuits)	**75 mW**
Active area	**0.43 mm^2**
Figure of Merit (FoM) ★	**2.17 pJ/convstep**

★ **FoM=Power/(2^{ENOB} · 2 · Fin)**
Where input frequency (Fin) is defined when ENOB ≧ 5 bit.



★ Estimated values from publications

Fig. 15. Comparison to state-of-the-art 6-bit flash ADCs with resistor averaging and/or interpolation techniques.

V. Conclusion

The proposed 6-bit, 1.2-GS/s ADC with wideband THA is demonstrated in 0.13-µm CMOS process which meets the MB-OFDM UWB communication system requirements. According to the experimental results, the figure-of-merit (FoM) of the proposed ADC is 2.17-pJ/convstep. As show in figure 15, our ADC has the best FoM for recently 6-bit flash ADCs with resistor averaging and/or interpolation techniques ever published [1]-[5].

References

[1] Michael Choi and A. A. Abidi, "A 6b 1.3GSample/s A/D Converter in 0.35-µm CMOS," IEEE ISSCC, pp. 126-127, Feb. 2001.

[2] G. Geelen, "A 6b 1.1GSample/s CMOS A/D Converter," IEEE ISSCC, pp. 128-129, Feb. 2001.

[3] P. Scholtens and M. Vertregt, "A 6b 1.6GSample/s Flash ADC in 0.18-µm CMOS using Averaging Termination," IEEE ISSCC, pp. 128-129, Feb. 2002.

[4] X. Jiang and M.-C. F. Chang, "A-1GHz Signal bandwidth 6-Bit CMOS ADC with power-efficient averaging," IEEE JSSC, vol. 40, no. 2, pp. 532-535, Feb. 2005.

[5] C. Sandner, M. Clara, A. Santner, T. Hartig, and F. Kuttnert, "A 6-Bit 1.2-GS/s Low-Power Flash-ADC in 0.13-µm Digital CMOS," IEEE JSSC, vol. 40, no. 7, pp. 1499-1505, Jul. 2005.

[6] Y.-Z. Lin, Y.-T. Liu and S.-J. Chang, "A 5-Bit 4.2GS/s Flash ADC in 0.13-µm CMOS," IEEE CICC, pp. 213-216, Sept. 2007.

[7] T. Kobayashi, K. Nogami, T. Shirotori, and Y. Fujimoto, "A Current-Controlled Latch Sense Amplifier and a Static Power Saving Input Buffer for Low-Power Architecture," IEEE JSSC, vol. 28, no. 4, pp. 523-527, Apr. 1993.