A 2-GS/s 6-bit Flash ADC with Offset Calibration

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***Abstract*-A 6-bit flash analog-to-digital converter (ADC) with a digital offset calibration scheme is fabricated in a 0.13-μm CMOS process. Adjusting the programmable loading devices of the preamplifiers enhances the linearity of the proposed ADC. To reduce power consumption, the utilized current-mode flip-flops change their operation mode depending on the sampling rate. A simple detector composed of an inverter and a diode-connected transistor senses the clock rate. This ADC consumes 170 mW from a 1.2-V supply in high-speed mode. The maximum operation speed of this ADC achieves 3.4 GS/s when the input frequency is low. When operating at 2 GS/s, its ENOB is 5.11 bit and ERBW is 650 MHz. The proposed ADC achieves an FOM of 3.79 pJ/conversion-step at 2 GS/s.**

I. Introduction

Owing to the progress of CMOS technology, increased cut-off frequency enables higher operation speed of flash ADCs. However, mismatches between paired devices result in random offsets which limit the accuracy of differential circuits. Conventionally, enlarging device sizes or using resistive averaging network reduces the random offsets. Nonetheless, increasing device size degrades operation speed and causes higher power consumption. Resistive averaging network has been proven a useful technique and extensively utilized in 6-bit flash ADCs [1-4]. Calibration techniques provide alternative solutions for accuracy enhancement [5-8]. In a 4-bit 4-GS/s flash ADC, digital-to-analog converters (DACs) trim the output voltages of the comparators [5]. In [6], a 4-bit 1.25-GS/s flash ADC uses programmable capacitor arrays to perform offset calibration. In [7], a 5-bit 3.5-GS/s flash ADC directly trims its reference voltages to cancel the offsets induced by comparators. A background offset calibration scheme is proposed in a 6-bit 1-GS/s two-step ADC [8]. An auxiliary differential pair is used to reduce the offset of the main differential pair.

In this paper, the proposed foreground digital calibration scheme employs resistive programmable devices instead of capacitive ones. Adjusting the programmable loading devices of the preamplifiers greatly reduces the random offsets. The proposed calibration circuits produces little capacitive loading to the preamplifiers. Therefore, the operation speed of the proposed ADC is not influenced.

At low operation speed, reducing the power dissipation of amplifiers avoids wasting power consumption and makes the overall circuit more power efficient. In [9], a switched capacitor bias current generator scales the bias currents automatically with the conversion rate, which gives scaleable power consumption of the ADC. In this work, a simple continuous-time detector senses the clock rate. The current-mode flip-flops automatically change their operation mode according to the decision of the detector.

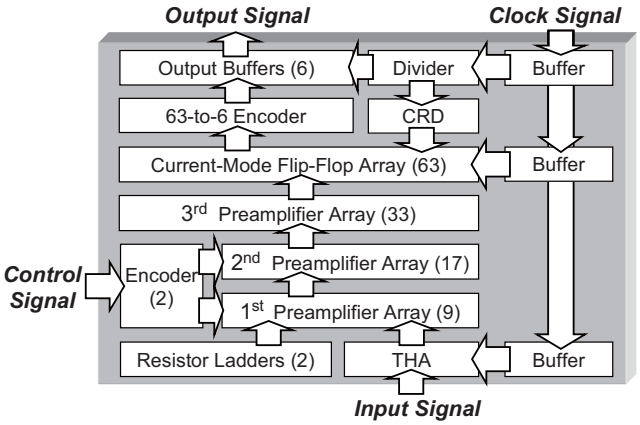


Fig. 1. Block diagram of the proposed ADC.

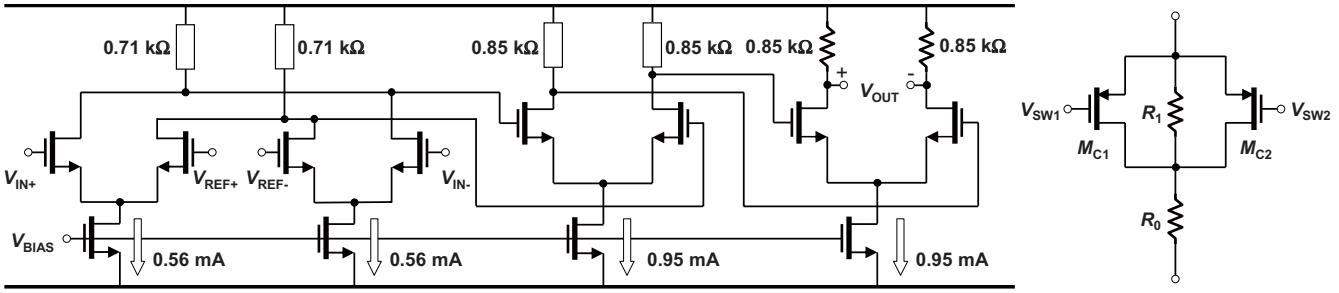
The remainder of the paper is organized as follows: Section II discusses the architecture of the ADC and implementation of building blocks. The calibration scheme is also described in this section. Section III presents the measurement results of the proposed ADC. Finally, Section IV is the conclusion.

II. ADC Architecture and Building Blocks

A. ADC Architecture

Fig. 1 shows the simplified block diagram of the proposed ADC. The ADC core consists of a track-and-hold amplifier (THA), two reference ladders, three preamplifier arrays, one current-mode flip-flop array, a 63-to-6 current-mode logic-based encoder and calibration circuits. The loading devices of the preamplifiers in the first two preamplifier arrays are modified to calibrate random offsets induced by process variations. For input matching, a 100-Ω resistor connects to the differential input ports to make the amplitude of input signals stable in the desired frequency range. For measurement, the output data are synchronized by flip-flops clocked at 1/64 sampling frequency. A frequency divider composed of six current-mode flip-flops generates the divided clock which is also applied to a clock rate detector (CRD). The employed current-mode flip-flops change their operation mode depends on the decision of the CRD.

B. Preamplifiers with Adjustable Loading Devices



(a) (b)

Fig. 2. (a) The employed preamplifiers. (b) The loading device of the 1st-stage and 2nd -stage preamplifier.

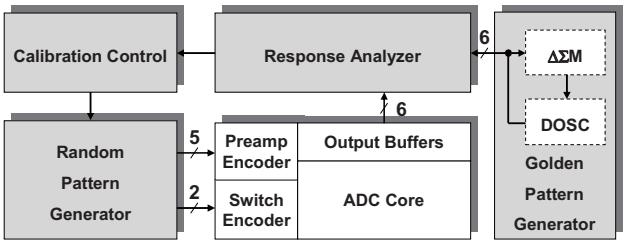
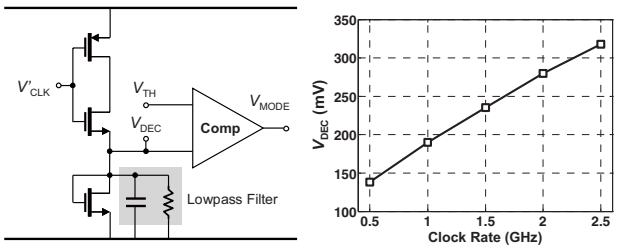


Fig. 3. The proposed calibration scheme.



(a) (b)

Fig. 5. (a) The clock rate detector. (b) Measured V_{DEC} versus clock rate.

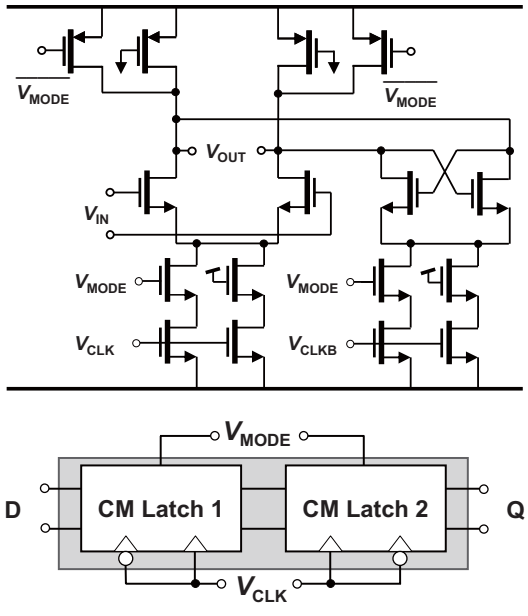


Fig. 4. The proposed current-mode latch (upper) and flip-flop (lower).

Fig. 2(a) shows the schematic of the three preamplifiers. Each loading device of the 1st-stage and 2nd-stage preamplifiers is comprised of a main resistor R_0, a calibration resistor R_1 and two p-type calibration transistors $M_{c1\text{-}2}$ as depicted in Fig. 2(b). In this design, the calibration resistors of the 1st-stage and 2nd-stage preamplifiers are 150 and 200 Ω, respectively. The on-resistance of a calibration transistor is about 800 Ω. Turning on the calibration transistors changes the total resistance of a loading device. The switching of calibration transistors generates a difference of the output voltages which can compensate random offsets induced by component mismatches. The gain of the 1st-stage preamplifier is 1.6 V/V and that of the 2nd-stage is 2.8 V/V. The input-referred voltage change caused by a calibration transistor in the 1st-stage preamplifier is around 8 mV, and that caused by a 2nd-stgae one is 4 mV. Because one LSB of this ADC is 9.5 mV, the maximum calibration ranges of the 1st-stage and 2nd-stage preamplifiers are ±1.7 and ±0.85 LSB, respectively. The 1st-stage preamplifiers perform the coarse calibration while the 2nd-stage ones do the fine adjustment. Calibrating the preamplifiers properly enhances the linearity of the proposed ADC.

To preserve the calibration information, there is a static latch connected to each calibration transistor. All the latches are controlled by a 5-to-26 preamp encoder and a 2-to-4 switch encoder. The overall calibration mechanism is depicted in Fig. 3 where an off-chip processor performs the functions of the gray blocks. Before the calibration process starts, the value of each calibration transistor is reset to VDD (off). Then a pattern generator randomly assigns the calibration transistors to GND (on). After the assignment completes, the output codes of the calibrated ADC are fed to the response analyzer. A digital oscillator (DOSC) and a ΔΣ modulator produce a golden reference histogram [10]. The response analyzer compares the output codes with the golden patterns and then evaluates the peak DNL and INL. Repeating these calibration procedures, the best combination of the assigned values is obtained.

The bandwidth of a preamplifier depends on its RC time constant. The output capacitive loading influences the operation speed of a comparator. Calibration circuits such as DACs or capacitor arrays induce extra capacitive loading and limit the bandwidth and operation speed. To augment the bias

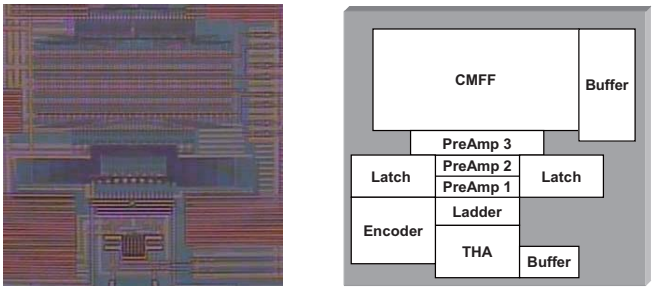


Fig. 6. Chip photograph and floorplan of the major part.

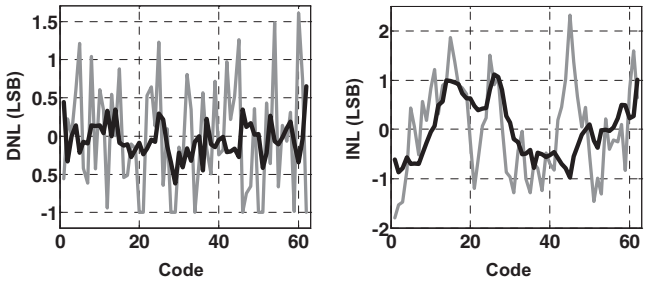


Fig. 7. DNL and INL with (black) and without (gray) calibration.

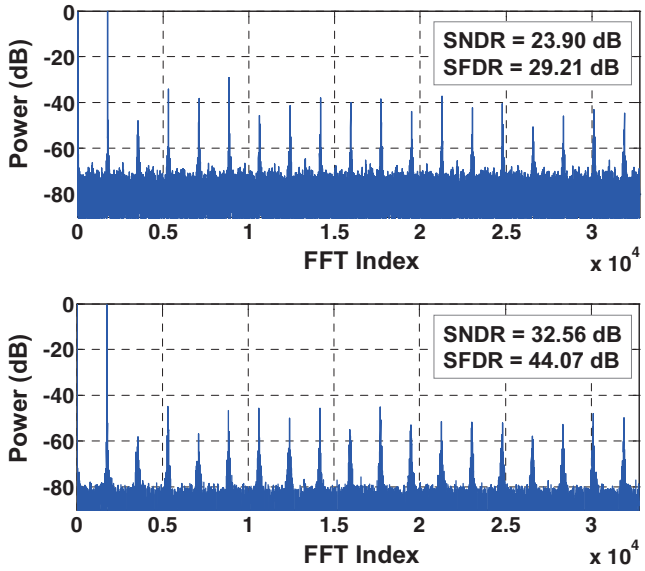


Fig. 8. Measured FFT results without (upper) and with (lower) calibration at 1 MHz (0.9 full-scale sine) input and 2.4 GS/s.

current is a general solution to compensate the loss of bandwidth and speed. In this work, the output resistance becomes smaller when calibration transistors turn on, and the proposed calibration circuits add very little capacitive loading to the preamplifiers. Therefore, the bandwidth of the preamplifier does not deteriorate because of the calibration circuits.

C. *Current-Mode Flip-Flop and Clock Rate Detector*

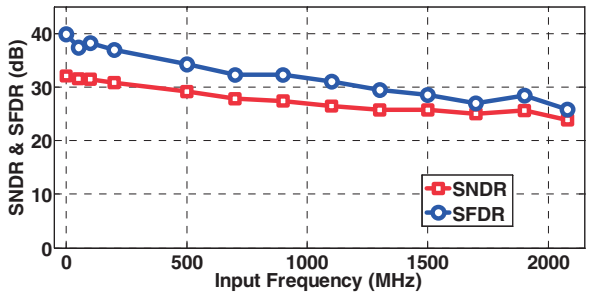


Fig. 9. Measured SNDR and SFDR versus f_{in} at 2 GS/s.

TABLE I
SPECIFICATION SUMMARY

Specification (Unit)	Experimental Result
Supply Voltage (V)	1.2
Input Range (V_{pp})	0.6
Active Area (mm^2)	0.2
Peak DNL / INL (LSB)	1.61 (**U**) 0.65 (**C**) / 2.32 (**U**) 1.1 (**C**)
Power (mW)	140 (**L**) / 170 (**H**)
SNDR (dB)	31.18 @ 1 MHz 3.4GS/s (**HC**) 28.29 @ 200 MHz 1.2GS/s (**LC**) 28.32 @ 200 MHz 1.2GS/s (**HC**) 8.06 @ 200 MHz 2.4GS/s (**LC**) 28.85 @ 200 MHz 2.4GS/s (**HC**)
ENOB (bit)	5.11 @ 2GS/s
ERBW (MHz)	650 @ 2GS/s
FOM (pJ/conv.-step)	3.79 @ 2GS/s

H: high-speed mode **L**: low-power mode **C**: calibrated **U**: uncalibrated

In this ADC, the current-mode flip-flop performs the functions of a comparator: high-speed sampling and digitalization. The employed flip-flop is composed of two current-mode latches as depicted in Fig. 4. When V_{MODE} is low, there is only one current path in each differential pair. For higher speed operation, V_{MODE} is set to V_{DD} to turn on the other path. To keep the output common-mode voltage the same, auxiliary p-type transistors turn on in the high-speed mode. Switching between the low-power and high-speed modes is automatically controlled by a clock rate detector (CRD). Fig. 5(a) illustrates the detector where V_{CLK} is the divided system clock. The diode-connected n-type transistor forms a discharging path from the inverter to ground. When the clock rate grows higher, the discharging time of V_{DEC} becomes shorter and therefore a higher average voltage value is detected. After first-order voltage regulation, V_{DEC} is compared to a predefined threshold voltage (V_{TH} = 0.25 V) and then the comparator determines the value of V_{MODE}. Fig. 5(b) shows the measured V_{DEC} versus the clock rate, where V_{DEC} increases smoothly with the increase of the clock rate.

III. EXPERIMENTAL RESULTS

The proposed work is fabricated in a 0.13-μm CMOS process. In the high-speed mode, the total power consumption excluding the output buffers is 170 mW, and the dissipation is 140 mW in the low-power mode. The occupied active area of

TABLE II
COMPARISON OF STATE-OF-THE-ART 6-BIT FLASH ADCS

	Choi'01 [1]	Scholtens'02 [2]	Uyttenhove'03 [11]	Sandner'05 [12]	Hung'06 [3]	Deguchi'07 [4]	This work
Sampling Rate (GS/s)	1.3	1.5	1.3	1.2	1.6	3.5	2.0
Supply (V)	3.3	1.95	1.8	1.5	1.8	0.9	1.2
ENOB (bit)	5.52	5.70	5.22	5.7	5.66	5.35	5.11
ERBW (MHz)	650	600	600	700	300	1650	650
Power (mW)	395	328	600	160	350	98	170
FOM (pJ/conv.-step)	6.7	5.26	13.4	2.2	11.56	0.95	3.79
Technique	Averaging	Averaging	N/A	Capacitive interpolation	Averaging	Averaging	Calibration
Technology (μm)	0.35	0.18	0.25	0.13	0.18	0.09	0.13

this ADC is 0.2 mm^2. Fig. 6 shows the photograph and floorplan of the major part. For measurement, output data are sampled by flip-flops clocked at 1/64 sampling frequency. Fig. 7 shows the peak DNL values before and after calibration are 1.61 and 0.65 LSB, respectively. The peak INL values before and after calibration are 2.32 and 1.1 LSB, respectively. The data shows the offset calibration greatly reduces the DNL errors of this ADC. However, the peak INL after calibration is somewhat large due to the non-linearity of the THA. Fig. 8 shows the FFT results with and without calibration. Fig. 9 shows the measured SNDR and SFDR versus the input frequency at 2 GS/s. To evaluate the overall performance of the ADC, we use an FOM equation defined as

$$FOM = \frac{Power}{2 \times 2^{ENOB} \times \min(ERBW, f_s/2)} \quad (1)$$

where f_s is the sampling frequency, *ERBW* is the effective resolution bandwidth and *ENOB* is the effective number of bits at low input frequencies. The ADC achieves an ENOB of 5.11 bit and ERBW of 650 MHz at 2 GS/s. The resultant FOM is 3.79 pJ/convsersion-step.

Table I summarizes the experimental results. At low input frequencies, the operation speed of the proposed ADC achieves 3.4 GS/s. At a low sampling speed, the ADC has similar performance in both power modes and is more power-efficient in the low-power mode. The table also shows the high-speed mode is the only choice when the sampling rate is high. Table II shows the comparison of recent GS/s 6-bit CMOS flash ADCs. The proposed ADC achieves comparable FOMs with the other state-of-the-art works. Most of these works use resistive averaging network to enhance the performance. This work provides an alternative approach.

IV. CONCLUSION

This paper presents the design and implementation of a 6-bit 2.4-GS/s flash ADC with digital offset calibration. With this technique, the preamplifiers can use small size transistors. As a result, the speed of this ADC is enhanced and the power consumption is greatly reduced. The fabricated ADC demonstrates the effectiveness of the clock rate detection, power mode switching and calibration technique.

ACKNOWLEDGMENT

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