Invited Paper

A 10GS/s Single-Core 8-bit ADC with an ENOB above 7.0 up to 4.2GHz

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***Abstract*—An 8b folding and interpolating ADC designed in a 180GHz SiGe BiCMOS process operates at 10GS/s without resorting to interleaving. It achieves an ENOB of 7.44 at 40kHz and 6.95 at 4.995GHz for a power dissipation of 9.1W, which corresponds to an energy per conversion step of 7.4pJ. Data output occurs in real time over ten 10Gb/s serial lanes using a proprietary protocol.**

I. Introduction

In digital storage oscilloscopes with bandwidths of several gigahertz, analog-to-digital converters (ADC) are typically built by time-interleaving multiple quantizer cores—possibly integrated on a same chip—operating at a fraction of the overall sampling rate. Time-interleaving introduces specific error sources degrading the signal-to-noise-and-distortion ratio (SNDR)—or equivalently, the effective number of bits (ENOB)—of the overall ADC. These error sources include sampling time skew, gain and offset mismatch, frequency response mismatch and quantization threshold mismatches between the quantizer cores. Compensating for such errors by calibration involves substantial overhead at high interleaving factors. A single-core ADC has the potential of achieving a higher ENOB than multiple time-interleaved cores while needing only straightforward calibration if at all. The key challenge in building such an ADC running at gigasamples per second is the design of a quantizer capable of settling within less than a sampling period. The present paper describes an 8-bit ADC chip based on a single quantizer core operating at the rate of 10GS/s, integrated in a 0.25µm SiGe BiCMOS technology with a peak transition frequency (f_T) of 180GHz. The 5mm by 5mm die (Fig. 1) is mounted into a 156-ball EBGA package and dissipates 9.1W overall.

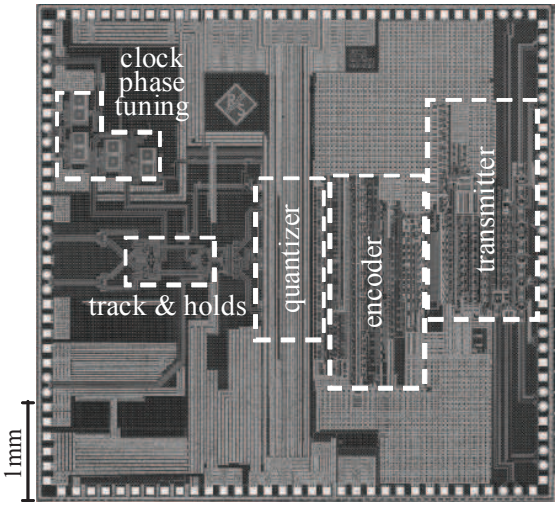

Figure 1. Chip photograph

II. Architecture

The architecture of the chip is shown in Fig. 2. A 10GHz sinusoidal clock signal is provided externally. The phase of the input clock can be rotated over 360° with 10b resolution in order to align the sampling times of multiple oscilloscope channels. The analog input signal is sampled by two time-interleaved track-and-hold (T&H) units operating at 5GS/s each. Each T&H unit tracks the input for 100ps, then holds a voltage sample for another 100ps, whereby most of the 100ps clock period is available for the quantizer to settle. An analog multiplexer selects the output of whichever T&H is in the hold state at any particular time. The 8-bit quantizer (Fig. 3) has a 3-layer folding and interpolating architecture [1] with an overall folding factor of 9 and interpolation factor of 4. An 8-level coarse flash quantizer (Fig. 3) eliminates coding ambiguities inherent to folding converters [1]. The 32 fine and 8 coarse output signals are digitized by a set of 40 current-mode logic (CML) flip-flops clocked at 10GHz. An encoder (Fig. 2) maps the resulting 40-bit pattern onto a 9-bit word including a parity bit. A transmitter sends the data in real-time to an external host through 10 high-speed serial lanes operating at 10Gb/s each, using a proprietary protocol based on techniques otherwise found in 10Gb/s Ethernet networks. Both the encoder and the transmitter are implemented as pipelined CML logic operating on the same 10GHz clock as the front-end of the chip.

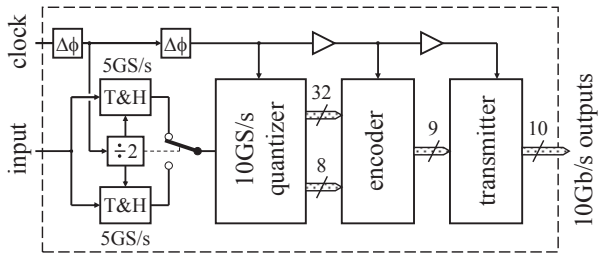

Figure 2. Architecture of the ADC chip

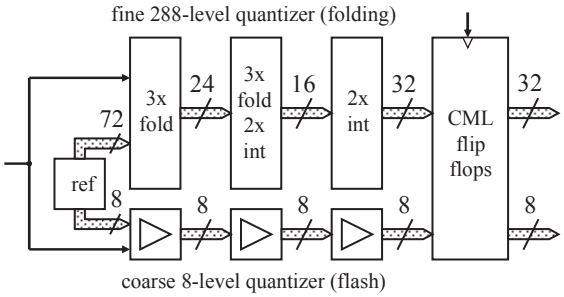

Figure 3. Architecture of the folding quantizer

III. Implementation Details

A. Track-and-hold amplifier

Each T&H unit is implemented by switched emitter followers [2] as shown in Fig. 4. In track mode (Vclkn>Vclkp), transistors Qfp and Qfn operate as emitter followers applying the differential input voltage Vinp–Vinn to two hold capacitors. In hold mode (Vclkn<Vclkp), the bias currents of Qfp and Qfn are turned off while their base voltages are lowered, whereby Qfp and Qfn remain turned off no matter how the input voltage may vary during the hold time. The output voltage is buffered by a pair of emitter followers.

B. Folding amplifiers

Each 3x folding amplifier is implemented by summing the output currents of three differential pairs (Fig. 5). The current sum is converted back to a voltage by a transimpedance amplifier (TIA). Due to its low input and output impedances, parasitic wiring capacitances are charged faster by the TIA than by equivalent passive load resistors, hence reducing settling time. For implementing 2x interpolation between consecutive folding amplifiers, two additional half-size differential pairs are connected in parallel to each differential pair shown in Fig. 5. The half-weight output currents of any two consecutive differential pairs are connected together, adding up to the average between the two related full-weight output currents (Fig. 6). The interpolated output current is converted back to a voltage by a TIA, identical in design to the TIA found at the primary output of each folding amplifier. Compared to the traditional voltage-mode interpolation by lateral resistive interconnections, this approach offers better delay matching between the primary and the interpolated outputs because both types of signal paths operate at the same impedance level.

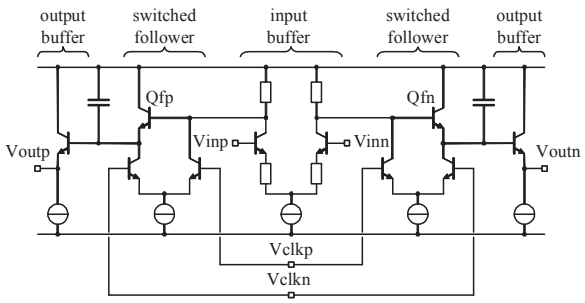

Figure 4. Circuit diagram of a switched-emitter-follower T&H

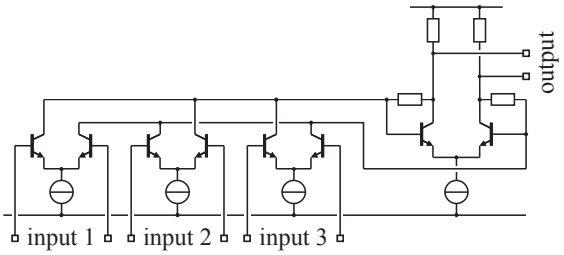

Figure 5. Simplified circuit diagram of a 3x folding amplifier

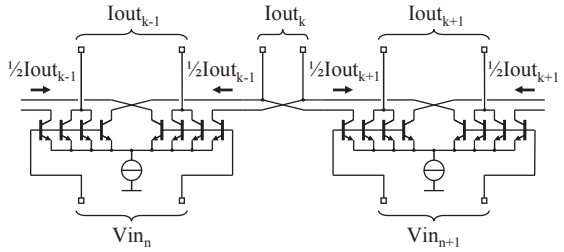

Figure 6. Interpolation by a factor of two in the current domain

C. Transmitter

The transmitter block structures the data into 32-sample frames and transmits them over a set of high-speed serial lanes running at 10Gb/s each. Each frame consists of a 2-bit synchronization header followed by 30 scrambled data bits. Scrambling enables AC-coupling to the receiver chip and data recovery by readily available 10Gb/s clock-and-data-recovery (CDR) circuits. The synchronization headers support alignment across lanes in the receiver, as well as synchronization between scrambler and descrambler in each lane. Together with parity bits, they enable a quick and reliable detection of error conditions in the data transmission path.

The overall capacity of the output data interface must be at least 96Gb/s in order to transmit 10GS/s with 9 bits per sample—8 data bits plus a parity bit—as well as the synchronization overhead. The output interface consists of ten 10Gb/s lanes, so that the entire transmitter can operate at exactly the same clock rate as the remainder of the ADC chip, which eliminates the possibility of generating spurs in case of cross-talk from the transmitter clock to the ADC input. The circuit shown in Fig. 7 maps the raw data to be transmitted onto these ten output lanes and inserts synchronization headers [3]. During the first two clock cycles of a frame, incoming 9-bit words are loaded in parallel into a shift register

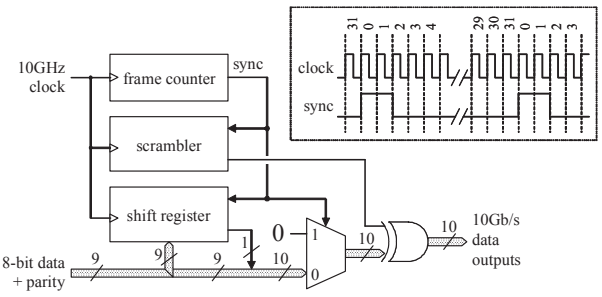

Figure 7. Block diagram of the transmitter

while a 2-bit synchronization header is output to all 10 lanes. The header consists either of the pattern 01 or the pattern 10 depending on the state of a scrambling sequence generator at the beginning of the frame. For the remaining 30 clock cycles of the frame, incoming 9-bit words are scrambled and transmitted without further processing through 9 of the output lanes, while the two samples stored in the shift register are transmitted serially onto the 10th lane.

D. Calibration

The chip includes a set of digital-to-analog converters (DAC) for aligning the gain, offset and timing of the two T&H units. In addition, a set of DAC is provided for trimming the static linearity of the quantizer. The calibration procedure runs on an external host processor.

IV. Results

The ADC chip was characterized after calibration using a 10GHz sinusoidal clock source (Rohde & Schwarz SMF100A) with an RMS jitter of about 100fs and a signal amplitude matching the ADC full-scale to within 0.1dB. The measured effective number of bits (ENOB) is 7.44 at 40kHz. The effective resolution bandwidth (ERBW)—i.e., the bandwidth over which the ENOB remains within 0.5b of its low-frequency value—is 4.995GHz, that is the Nyquist frequency minus 5MHz (Fig. 8). In a narrow frequency range around Nyquist, the ENOB dips slightly to 6.75, presumably because of distortion originating in device self-heating. The energy per conversion step, defined as $P/(2^{ENOB} \cdot 2ERBW)$ [4], is 7.4pJ. The spurs-free dynamic range (SFDR) remains above 52dB up to the ERBW. The signal-to-noise ratio is 46.4dB at 40kHz and gradually decreases to 44.7dB at the ERBW. The measured differential nonlinearity (DNL) is 0.38LSB whereas the integral nonlinearity is 0.44LSB.

To the best of the authors' knowledge, the 10GS/s converter described herein is the fastest 8-bit single-core ADC—i.e., ADC not resorting to time-interleaving—ever publicly reported. The next-fastest published ADC core known to the authors operates at 3GS/s, albeit with a nominal resolution of 10b [5]. Single-chip 8-bit converters have been reported in [6] and [7], which resort to massive interleaving to achieve an overall sampling rate higher than the chip described herein. A comparative plot of effective resolutions (Fig. 8) reveals that the present chip brings an improvement of more than 0.7b around DC and 1.1b at 5GHz over the best massively interleaved ADC.

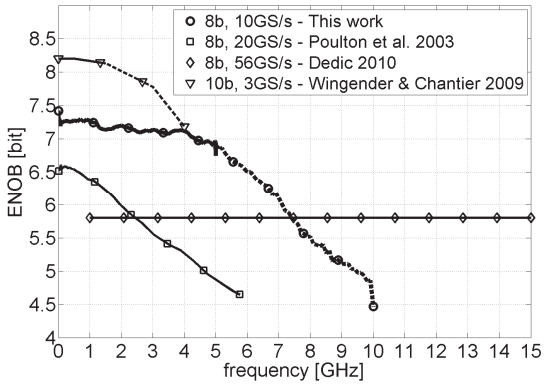

Figure 8. Measured ENOB compared to other ≥ 8b single-chip converters with a bandwidth of 5GHz or more (solid lines below Nyquist, dashed lines above Nyquist)

Acknowledgment

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