3 GS/s S-Band 10 Bit ADC and 12 Bit DAC on SiGeC Technology

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Abstract—

In advanced applications such as digital radar, Ultra Wide Bandwidth communications and software defined radio, the need for instantaneous bandwidth often drives system design decisions. Access to high speed data converters enabling up and down conversion directly in the L Band and S Band removes the limit imposed by bandwidth scarcity and allows the design of flexible and simplified system architectures. Broadband ADC's (Analogue to Digital Converters) and DAC's (Digital to Analogue Converters) are key enabling components which open up new design opportunities for digital transceiver systems, including digital down and up-conversion closer to the antenna.
In this regard, this paper describes new 10bit 3GS/s ADC and 12 Bit 3GS/s DAC, based on a 200 GHz SiGeC bipolar Technology, which enables direct digitizing or synthesing of 1GHz arbitrary broadband waveforms directly in the high IF region closer to the Antenna.

Keywords-components: Development of next-generation broadband flexible radar systems; Increased sampling rates, bandwidth and resolution; Expanded output frequency spectra and update rates; Broadband instantaneous frequency capture or generation; Direct sampling and/or Digital synthesis of arbitrary UWB signals in L_Band or S_Band;

I. INTRODUCTION

High speed ADCs and DACs featuring a good linearity over a wide range of frequency inputs are key components for new generations of broadband RF Radar transceivers.
In this regard, a new generation of low latency Ultra Wide Band ADC and DAC circuitries based on a 200 GHz SiGeC (SiGe Carbon) fully bipolar Technology has been designed to serve next-generation broadband flexible radar and countermeasure systems.

II. 10 BIT 3 GS/S ADC AND 12 BIT 3GS/S DAC

A. 10 Bit 3 GS/s ADC and 12 Bit 3 GS/s DAC based on 200 GHz SiGeC (SiGe Carbon) Technology

The 10-Bit ADC operates at 3 GS/s (Giga Samples per second) and features 5 GHz full power input bandwidth which allows operation in either L-Band or S-Band.

The ADC is packaged in a Multi-Chip-Module (MCM) EBGA317 (Enhanced Ball Grid Array) with a 1:4 DMUX companion chip, with selectable output demultiplexing ratio.
The ADC is based on a single core architecture, and do not rely on internal interleaved core ADCs to achieve 3GS/s. Hence, the ADC does not require any calibration before or during operation over temperature as sometimes required with interleaved multi-cores architectures.
The ADC embeds multiple 8 Bit Control DAC's, which are monitored through a 3 Wire Serial Interface (3WSI), for remote fine tuning of the ADC sampling delay, gain and offset, for easy interleaving of multiple ADCs.
The 12-Bit 3GS/s DAC is based on the same SiGeC Technology as the ADC. The MuxDac features a Return To Zero (RTZ) mode for operation in the 2nd and 3rd Nyquist zones, enabling direct digital synthesis of UWB arbitrary waveforms in the high IF region (S_Band).
The DAC power dissipation is only 1.3 Watt, including the power of the 4:1 embedded MUX, and is packaged in a small fPBGA196 plastic package.

B. Performance enabling SiGeC Technology

The ADC and DAC performance is enabled by a 200 GHz SiGeC bipolar Technology together with innovative architecture concepts. The technology features deep trench vertical isolated bipolar NPN transistors, with 4 levels of Copper metal for very low interconnect parasitics, enabling peak cutoff frequency (fT) of 230 GHz for low current densities. The 10 Bit ADC and 12 Bit DAC prototypes reported in this paper are both based on this technology.

III. 10 BIT 3 GS/S ADC +1:4 DMUX

A. Receiver System Architecture improvements

Innovative architecture concepts together with the high cut-off frequencies of the SiGeC Technology allows for enhanced linearity and noise performance for the ADC with 5 GHz full power input bandwidth, and update rates of 3 GS/s together with multi Nyquist operation.
Direct under sampling of Ultra Wide Band (UWB) signals of up to 1GHz instantaneous bandwidth in either L_Band or S_Band can be envisioned.
The following figure depicts the architecture improvement in terms of size, power, complexity and cost of a typical receiver system based on a performing UWB ADC.

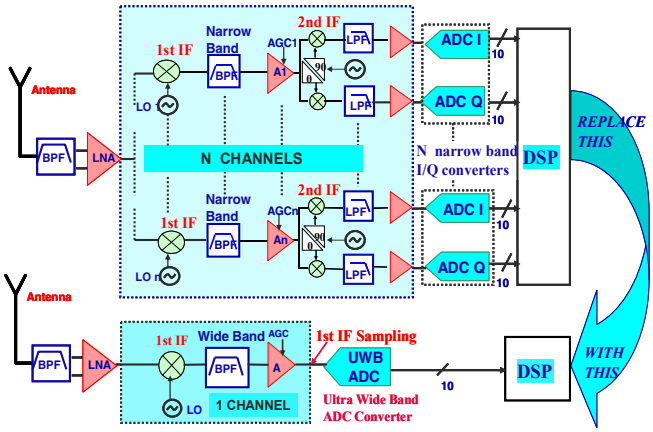

Figure 1. Example of Receiver System Improvement with UWB ADC

B. 10 Bit 3 GS/s ADC Chip Description

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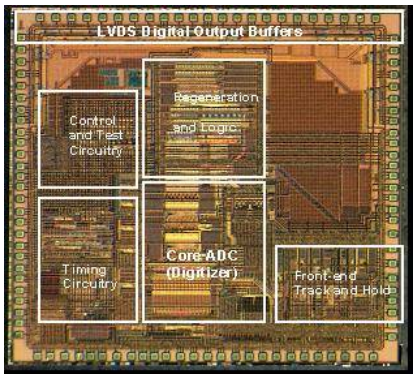

Figure 2. 10 Bit 3 GS/s ADC Microphotograph and MCM Package

The ADC is based on 100 % fully bipolar vertically isolated NPN transistors. Component count is 6500 SiGeC transistors and 8000 oxide isolated resistors. Accurate thin film TaN resistors are used for on-chip 50 Ω embedded terminations.
The interconnections are based on four levels of Copper for low RC parasitics. The ADC architecture is fully differential from Analog input and Clock input up to the LVDS compatible Digital Outputs. The ADC maximum Power Consumption is 3.9 Watt at Tj = 125°C junction temperature. Power supplies are +5.2V and +3.3V for the Analog section, and + 2.5V for the digital output buffers. The 1:4 DMUX companion chip is designed on a 45 GHz fuly bipolar SiGe technology, and operates up to 4 GS/s for a power dissipation of 2.2 Watt.

C. 10 Bit 3 GS/s ADC Architecture general Description

Broadband ADC Architectures are generally based on fast and accurate front-end Track and Holds (T/H), driving fast settling fast settling Core ADCs, which performs analogue quantification. The T/H is a bipolar version of the differential switched follower structure described in [1].The T/H shall feature enhanced track mode large signal linearity performance, together with fast hold to track acquisition times, in order to recapture the analogue input after hold mode in less than ¼ of the clock period, i.e. in less than 80 ps at 3 GS/s.

The core analogue quantifier is based on fast settling cascaded folding and interpolation structures [3], designed to feature very low throughput propagation delay, in order to settle within the very short hold mode time width available at 3 GS/s. This structure also provides very low input loading capacitance for the T/H.

D. ADC Characterization Results

1) ADC Single Tone FFT Computation at 3 GS/s in 1st, 2nd and 3rd Nyquist zones

At 3 GS/s in the 1st Nyquist (Fin=1495MHz, -1dBFS), an ENOB of 8.1 Bit and an SFDR of 59 dBc is achieved (Fig. 3).
In the 2nd Nyquist (Fin=2995MHz, -3 dBFS), an ENOB of 8.0 Bit is still achieved, with an SFDR performance of 58 dBc (Fig. 4). With Fin=3995MHz (-3 dBFS), corresponding to the S_Band upper limit, the ENOB is still 7.7 Bit, with an SFDR of 55 dBc, and the SNR is 49.5 dBFS. The SNR roll off versus input frequency is related to the voltage noise induced by the 120 fs rms internal sampling clock jitter of the ADC. The large linearity roll off over frequency is related to the large signal dynamics of the front-end Track and Hold, which improves for smaller signals.
The 0dBFS ADC Full Scale reference voltage span is 500 mV, and Full Scale input power is -2dBm if single-ended driven in 50 Ω and -5 dBm if differentially driven in 100 Ω termination. At 3 GS/s and Fin = 3 GHz, an SNR of 51 dB is achieved, leading to an FFT noise floor of: SNR + 10log(N/2) = 51dB+10log(16384)=93dB per 32K FFT bin width.
The normalized noise floor in dBc/Hz at Fs=3 GS/s is 51 dB + 10log(Fs/2)=142.7dBc/Hz. Since ADC Full Scale differential input power is -5dBm, the normalized (per/Herz) Noise floor is -5dBm-143dB = -148 dBm/Herz. The ADC total noise power includes the input referred thermal noise and the voltage noise induced by time jitter. Therefore the contribution of the ADC to overall system noise figure can be calculated.

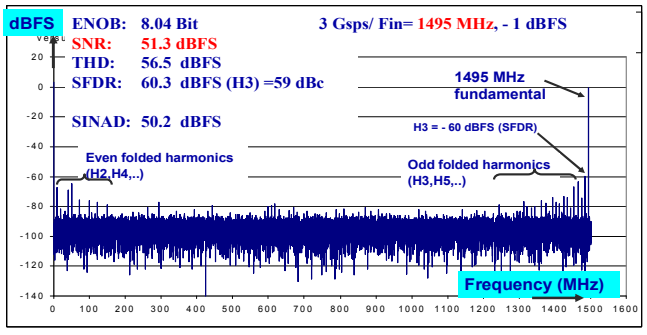

Figure 3. FFT Computation at 3 GS/s 1st Nyquist Fin= 1495 MHz , - 1dBFS

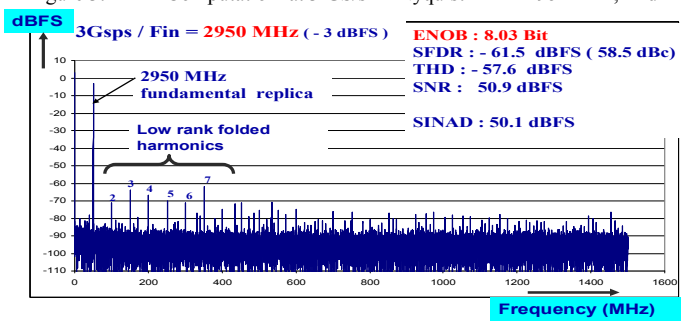

Figure 4. FFT Computation at 3 GS/s 2nd Nyquist,Fin= 2950 MHz , - 3dBFS

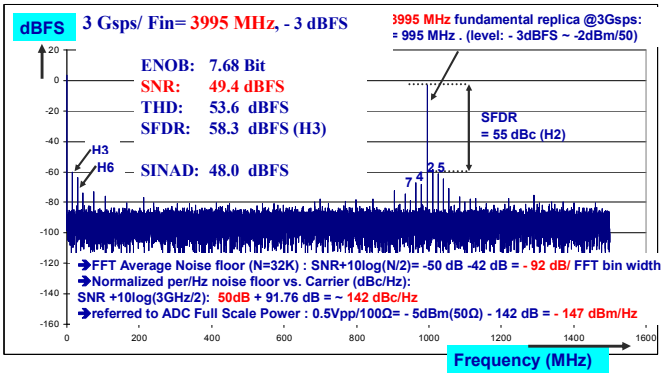

Figure 5. FFT Computation at 3 GS/s 3rd Nyquist, Fin=3995 MHz , - 3dBFS

2) ENOB, SNR and SFDR rolloff characteristics at 3 GS/s over 3 Nyquist Zones and vs. Input level

The following Figures (6,7,8) depict the ENOB, SNR and SFDR characteristics versus analogue input frequency measured at 3GS/s over 3 successive Nyquist zones (DC up to Fin = 4 GHz), covering the L_Band and S_Band regions. The Signal levels are ranging from -1 dBFS to -18 dBFS, to illustrate large signal versus small signal performance.

The ENOB roll-off characteristics depicted in (Fig.6) results from the contribution of SNR (Noise) and THD (Linearity) components which are RSS summed.

The ADC features more than 8 Bit ENOB at 3 GS/s in the 1st Nyquist zone for signals close to ADC Full Scale. In the 2nd Nyquist, an ENOB of 8 Bit is still achieved for slightly lower input levels (-3 dBFS). In the 3rd Nyquist with Fin=4GHz, the 8 Bit ENOB performance is achieved with -6 dBFS input levels. At -1 dBFS and Fin=4GHz, the ENOB rolls off to 7.2 Bit is due to large signal non linearity effects and time jitter effects which are analog input slew-rate dependent.

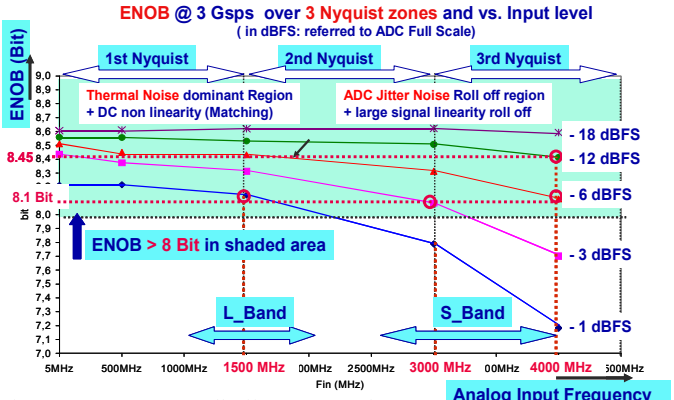

Figure 6. ADC ENOB roll off over 3 Nyquist zones at 3 GS/s vs. input level

The SNR Characteristic in (Fig. 7) is mainly related to two noise components:

- The ADC input referred thermal noise, related to front-end T/H thermal noise spectral density integrated over ADC input Bandwidth. Since the thermal noise power features much higher weighting than quantification noise power, it clips the SNR to 54 dB, instead of 62 dB if only ideal 10bit quantification noise is considered.
- The voltage noise induced by sampling clock time jitter: The ADC internal jitter is 120 fs rms, causing the SNR to roll off for fast slewing analogue inputs (e.g.: SNR=54dB for low input frequencies and SNR=50 dB at Fin=3GHz, -1 dBFS).

Phase Noise floor requirements for clock source shall be better than 155 dBc/Hz: for a 5.5 GHz integration bandwidth, the integrated Single Side Band (SSB) phase noise floor 10log (Rad^2 /Hz) expressed in dBc/Hz is given by: -155+10log($5{,}5.10^{09}$) = -57.6 dB. The total integrated phase noise power is SQRT($2.10^{-57{,}6/10}$) = $1{,}86.10^{-03}$ radians (rms). With a 3 GHz sinewave clock source, the corresponding rms time domain jitter is $1{,}86.10^{-03}$ radians (rms) / 2.Π.3GHz = 98 fs rms. An SSB phase noise floor of 160 dBc/Hz will only contribute for 55 fs rms time jitter. Total sampling clock jitter will be: SQRT(120^2 +$50^{2)}$ =130 fs rms. Therefore any clock source phase noise floor in the range of 160 dBc/Hz will have negligible contribution to total sampling jitter.

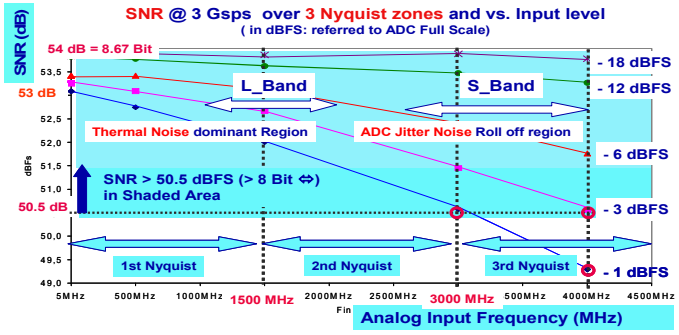

Figure 7. ADC SNR roll off over 3 Nyquist Zones at 3 GS/s & vs. Input level

The Spurious Free Dynamic Range (SFDR) roll off characteristic is shown in (Fig.8) over three Nyquist zones. The large signal distortion effect over frequency and versus signal level is clearly shown. The - 60 dBFS spurious level is achieved in the 1st Nyquist with - 1 dBFS level, - 3 dBFS in the 2nd Nyquist, and - 6 dBFS in the 3rd Nyquist region.

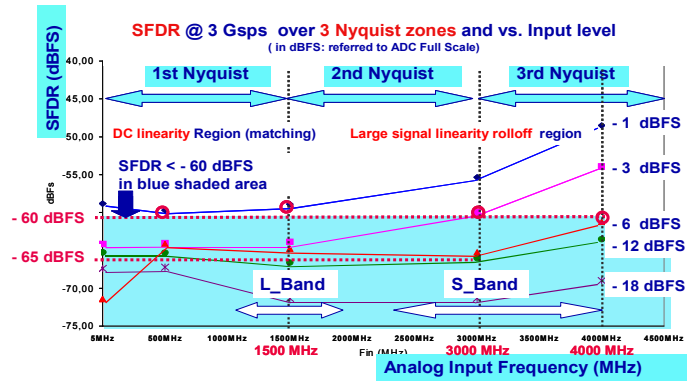

Figure 8. ADC SFDR roll off over 3 Nyquist Zones at 3 GS/s vs. input level

3) Dual tone FFT computations at 3 GS/s and IMD3 performance in 1st Nyquist and 2nd Nyquist.

Dual tone FFT computations were carried out at 3 GS/s with -7 dBFS tones places at respectively (790MHz, 800MHz) and (2951MHz,2961MHz), showing the different intermodulations products. The IMD3 performance is given by the (2F1-F2, 2F1-F2) non filterable product terms close to the carriers. The IMD3 performance is 58 dBc at either 1st or 2nd Nyquist region (Figures 9 and 10) and is mainly dictated by DC linearity characteristics of the ADC, which needs to be improved. Complement of investigation needs also to be carried out at higher input frequencies (3rd Nyquist) and for lower input levels to check small signal IMD.

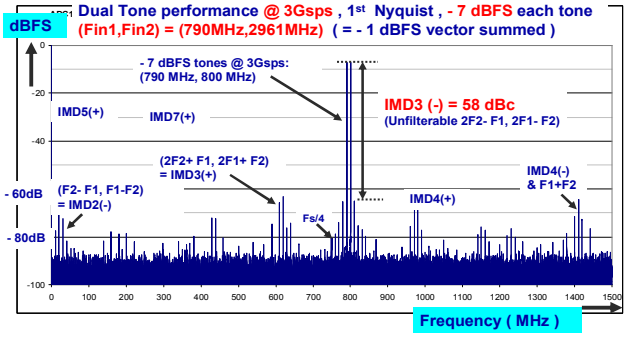

Figure 9. Dual Tone FFT computation at 3 GS/s (790MHz, 800 MHz)

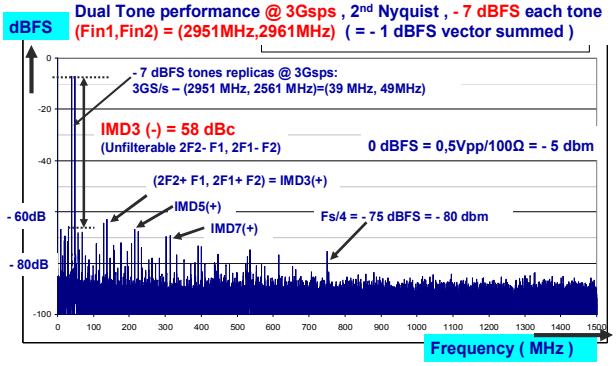

Figure 10. Dual Tone FFT computation at 3 GS/s (2951MHz, 2961 MHz)

IV. 12 BIT 3 GS/S 4:1 MUXDAC

A. *Transmitter Systems Architecture improvements*

Direct Digital Synthesis (DDS) becomes a requirement for arbitrary waveforms generators, with instantaneous bandwidths generation capability of up to 1 GHz in the high IF region. DDS allows easier discrimination of targets and increased number of waveforms. Benefits of the DDS as compared to Phase Locked Loop based synthesizers include instant frequency hopping, continuous phase and flexibility provided by Digital Signal Processing (DSP). Therefore, the demand for an Ultra Wide Band (UWB) high dynamic range DAC is increasing, especially for digital beam forming or multicarrier radar applications. A key component in a DDS System is a high performance DAC, which is often the performance limiting element. Direct IF Synthesis allows I-Q modulated signals to be digitally constructed into a single modulated IF output. This avoids the potentially damaging distortion that external analog vector modulators can introduce. Digitally Summing I and Q channels gives excellent I-Q phase and amplitude matching along with ideal symbol timing. Direct RF generation eliminates the need for external components for up converting the IF signal to an RF frequency. Therefore direct UWB synthesis in the high IF region (L_Band or S_Band) offers more flexibility together with the decrease in size and cost of the transmitter system, provided a high performance DAC is available.

B. *12 Bit 3 GS/s 4:1 MuxDAC Chip Description*

The chip Layout of the 12 Bit DAC is shown in figure 10, showing the four 12 Bit digital LVDS input ports of the 4:1 MUX embedded, with selectable multiplexing ratio.
The device is pad limited due to high pad count requested by the 4x12 differential digital inputs. The DAC is designed on the same 200 GHz SiGeC Technology as the ADC device, and is based on fully bipolar NPN transistors. Thin film TaN resistors are used for embedded 100Ω terminations and Analog output sourcing. The digital input buffers are LVDS compatible, allowing up to 4 x 12 Bit data exchange with standard FPGAs. The DAC maximum Power Consumption is 1.3 Watt at Tj = 125°C junction temperature, including the 4:1 MUX. The device is packaged in a fPBGA196 plastic Package. The DAC is supplied with +5V for the Analog Output section, and + 3.3V for the digital and logic Sections.

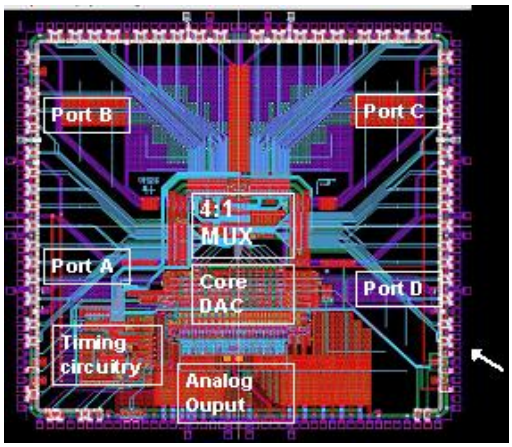

Figure 11. 12 Bit 3 GS/s 4:1 MuxDAC Chip Layout

C. *12 Bit 3 GS/s DAC Architecture general Description.*

Broadband DACs are based on fast current steering architectures ([4],[5],[6],[7],[8]). The spectral purity of the DAC relies heavily on the current switch design, inducing data-dependent switching noise to the Analog output. The use of a re-sampling RTZ feature improves the spectral purity and noise performance of the DAC, and also enables the expansion the sin(x)/x roll off curve, allowing operation in the 2nd and 3rd Nyquist. Enhanced HF isolation is also necessary for optimum rejection of the clock related spurs and images induced by the switching Mux, especially if the 4:1 MUX ratio is requested,

for optimum spurious free dynamic range in the center regions of Nyquist zones.

1) Return to Zero versus Non Return to Zero feature:.

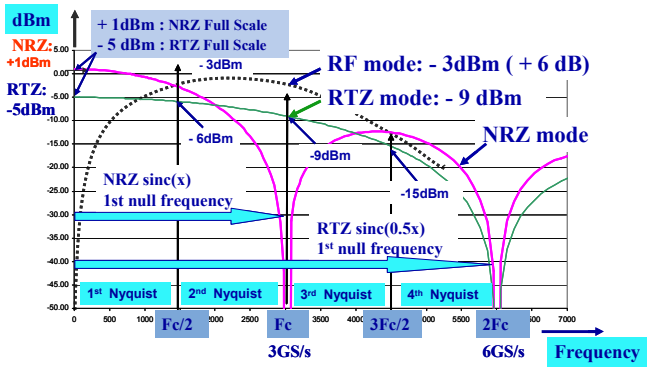

Figure 12. NRZ (sinc(x) and RTZ sinc(0.5x) nulling frequencies and rolloff

With a 50% resampling clock pulse width in RTZ mode, the zero order hold time window is ½ the clock period and allows the expansion of the DAC sinc function by a factor 2. This enables operation in the 2nd and 3rd Nyquist regions. However, the RTZ mode induces a 6 dB loss in carrier power, which directly impacts the SFDR level in dBc. Therefore, an alternate mode called "RF" or "mixed" mode would be more convenient for operation in the 2nd and 3rd Nyquist region without decreasing the carrier power by 6 dB. Although the "RF" mode does not allow operation in the 1st Nyquist because of null frequency in DC, a future improved version of the DAC including the RF feature can be envisioned.

D. 12 Bit 3 GS/s 4:1 MuxDAC Characterization Results

The measured SFDR performance vs. Nyquist frequency remains nearly flat up to 3.5 GS/s, featuring an SFDR of 67 dBc measured @3.5GS/s with Fout = 1750 MHz, - 3dBFS.

The characterization results demonstrate the capability to design a low power DAC on 200 GHz SiGeC technology capable of operation beyond 3 GS/s over the three first Nyquist zones, covering L_Band and S_Band regions, with cutting-edge ENOB and linearity performance.

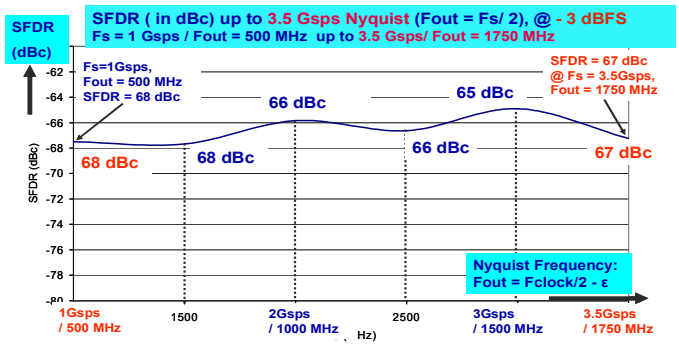

Figure 13. SFDR in dBc versus Nyquist frequency up to 3.5GS/s, - 3dBFS

1) DAC SFDR rolloff at 3 GS/s vs. Input Frequency (RTZ mode) over 3 Nyquist Zones

The following plots summarizes the SFDR roll-off in dBc and dBFS versus output frequency in RTZ mode, from DC up to Fout = 4500 MHz. The SFDR in dBFS remains flat, close to - 80 dBFS, which demonstrates that the SFDR in dBc is mainly dictated by the output carrier level roll off over frequency and not by the spurs level. The optimum SFDR performance in dBc at 3GS/s is achieved at -3 dBFS, featuring 65 dBc at 1.5GHz, 54 dBc at 3GHz, and 50 dBc at Fout = 4.5 GHz. It is clearly shown that an "RF" mode feature would be of interest to further improve the dBc spurious performance of the DAC.

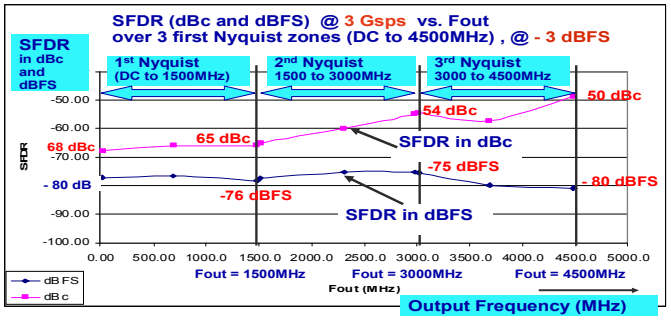

Figure 14. SFDR in dBFS and in dBc over 3 first Nyquist zones @ 3GS/s

2) DAC Single Tone FFT Computation at 3 GS/s in 1st, 2nd and 3rd Nyquist

The following single tone spectrum plots (Figures 15,16) are carried out at 3 GS/s in respectively 1st and 3rd Nyquist, to illustrate the spurious distribution up to Fout = 4500MHz. It is shown that the SFDR is dictated by signal harmonics in the range of - 77dBm to - 80 dBm. The Fc/4 clock related spur and images are rejected below -80dBm. However this may not be enough for certain Radar applications requiring a better rejection of clock spurs and images, and better HF isolation between digital and analog section needs is requested in a future version of the DAC. Up to 2GS/s ratings, the 2:1 MUX ratio can be selected to improved spurious performance.

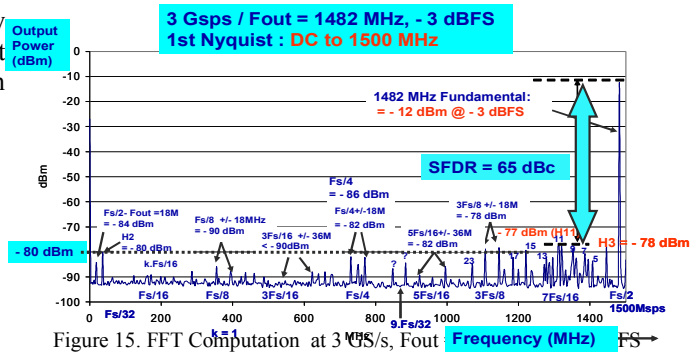

Figure 15. FFT Computation at 3 GS/s, Fout = Fs/2

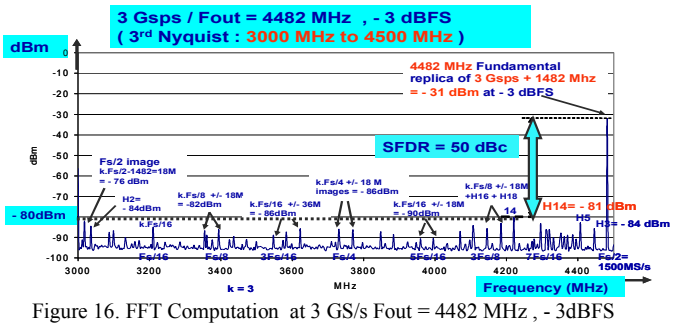

Figure 16. FFT Computation at 3 GS/s Fout = 4482 MHz , - 3dBFS

3) DAC Noise Power Ratio Measurement@ 3GS/s in 1st, 2nd and 3rd Nyquist (NRZ vs. RTZ mode)

The spectrum of a 1 GHz UWB pattern synthesized at 3 GS/s and replicated over 1st , 2nd and 3rd Nyquist zones is shown in Figures 17 and 18, in respectively NRZ and RTZ mode. The output pattern noise power is at - 14 dBFS which is the optimum loading factor for a 12 Bit DAC for optimum weightings of saturation noise versus quantification noise.

A 50 MHz notch is centered within the 1 GHz pattern, to measure the NPR of the DAC. With an ideal DAC, the notch is filled with quantification noise only. For a real DAC, the notch is filled with additional thermal noise, voltage noise induced by time jitter, and intermodulation products from all the surrounding carriers placed within the pattern. The NPR is representative of the actual DAC performance in the situation of synthesizing 1 GHz UWB patterns.

At 3 GS/s in the 1st Nyquist, an NPR of 53 dB is achieved in NRZ mode, which is 10.17 Bit ENOB equivalent, and 50 dB in RTZ mode, corresponding to 9.7 Bit ENOB. In RTZ mode, an NPR of 45 dB is still achieved in the 2nd Nyquist, which corresponds to an ENOB of 8.85 Bit, and 40 dB in the 3rd Nyquist corresponding to 8.0 Bit ENOB in the S_Band region (3000 to 4000MHz).

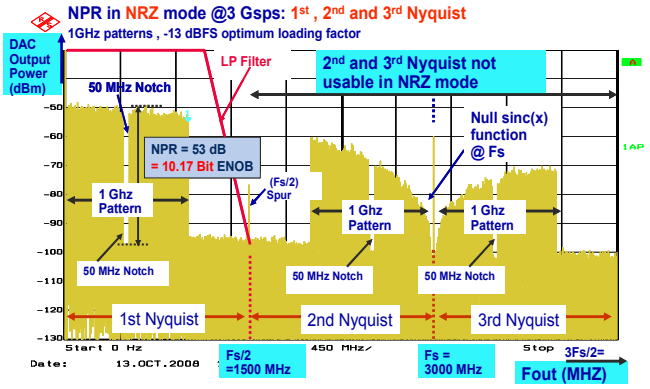

Figure 17. NPR in NRZ mode over 3 Nyquist Zones (DC to 4500MHz)

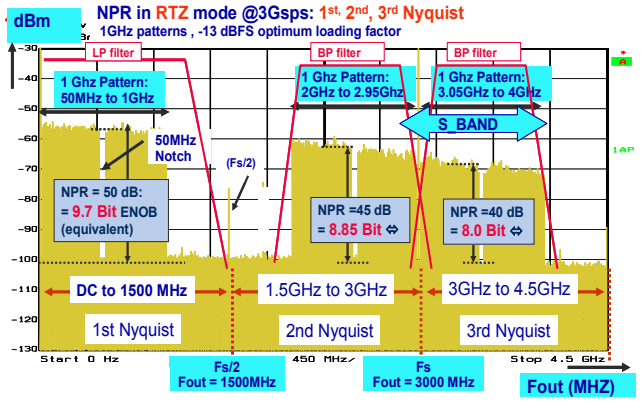

Figure 18. NPR in RTZ mode over 3 Nyquist zones (DC to 4500MHz)

V. PACKAGING AND TESTING ISSUES

The increased sampling rates also created new challenges in package HF modelling and industrial testing:

The ADC and DAC Packages have been developed with the help of HF Softwares for design and modelling.

The ADC and DAC parts are tested industrially and screened at full operating speed.

VI. SUMMARY

A 10 Bit 3 GS/s ADC featuring 5 GHz Full power bandwidth and a 12 Bit 3GS/s RTZ DAC capable of operation at multi Nyquist frequency with signals of up to 1 GHz instantaneous bandwidth have been designed, and fabricated with a 200 GHz SiGeC bipolar technology. The parts have been characterized at 3 GS/s over three Nyquist zones, showing cutting-edge performances which enables the direct under sampling and/or synthesizing of 1 GHz UWB signals directly in the L_Band or in the S_Band, simplifying the RF transceivers complexity, cost and size, with increased flexibility for Radar systems.

Based on the same SiGeC platform, further axis of improvements for the ADC and DAC which can be envisioned are twofold, depending on Radar needs: Either increasing the ADC Bandwidth and sampling speed to 4GS/s, to cover the entire S_Band in the 2nd Nyquist region, or increasing the resolution up to 10 Bit ENOB and 70 dBc SFDR by operating at lower rates (1GS/s to 1.5GS/s) to improve settling accuracy.

ACKNOWLEDGMENT

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