# A 2.4 GS/s, 4.9 ENOB at Nyquist, Single-channel Pipeline ADC in 65nm CMOS

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***Abstract*— This paper presents a high-speed single channel pipeline analog-to-digital converter sampling at 2.4 GS/s which, to the authors' best knowledge, is the fastest reported for pipeline converters. The use of a time-borrowing clocking scheme eliminates the comparator latency from the critical path and together with the use of fast open-loop current-mode amplifiers the high sample rate is achieved. Implemented in a 65nm general purpose CMOS technology the effective number of bits is above 4.7 in the Nyquist band, being 5.4 and 4.9 at DC and Nyquist respectively. This shows that very fast pipeline ADCs are possible to implement as key building blocks in interleaved structures.**

## I. INTRODUCTION

Analog-to-digital converters with sample rates of 10+ GS/s are implemented by the interleaving of typically either SAR or pipeline ADCs. These architectures both have the benefit that the input capacitance is bound by thermal noise constraints. The use of high-speed pipeline ADCs for interleaving results in a lower aggregate input capacitance and a reduced interleaving factor which offer benefits of reduced power dissipation and complexity of the interleaving process. This 2.4 GS/s single-channel pipeline ADC achieves an effective number of bits of at least 4.7 bits throughout the Nyquist band. With an input capacitance of 250 fF, this architecture is suitable for interleaving to facilitate the high sample rates needed in 40 and 100 Gb/s Ethernet standards.

The proposed ADC achieves a high sample rate through two improvements, a clocking scheme which eliminates the comparator latency from the critical path as well as a new fully differential, open-loop current-mode amplifier with common-mode balancing which allow fast settling times and easy integration of the DAC. The resulting sample-rate of 2.4 GS/s is, to the authors' best knowledge, significantly faster than any previously reported single-channel pipeline ADC [1][2][3].

In Section II, the ADC architecture is described together with the time-borrowing clocking scheme. Section III presents the important circuit implementations, which are the sample-and-hold (S/H) and MDAC stages. The error correction principle and measurement results are presented in Section IV and the paper is concluded in Section V.

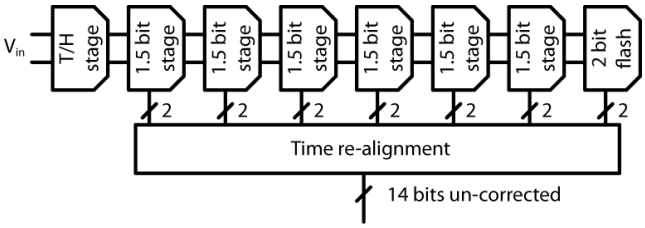


Figure 1. Architecture of the pipeline ADC.

## II. ADC ARCHITECTURE

The ADC, shown in Fig. 1, is comprised of a track-and-hold (T/H) stage, six pipeline stages and a flash converter with all stages being differential. The T/H stage keeps the input signal to the first pipeline stage constant during one clock cycle. Each pipeline stage, shown in Fig. 2, consists of a 1.5 bit sub-ADC (two comparators followed by latches), two interleaved S/H stages and one differential MDAC. The interleaved S/H samples the input signal once per clock cycle while simultaneously holding the previously sampled data constant at the output throughout the entire time period. The MDAC stage is a time-continuous, open-loop, current mode amplifier performing common-mode balancing, signal gain and subtraction of the DAC values. At the rising clock edge the S/H circuit samples its input and feeds it to the MDAC. In order to save time, the sub-ADC comparators latch earlier,

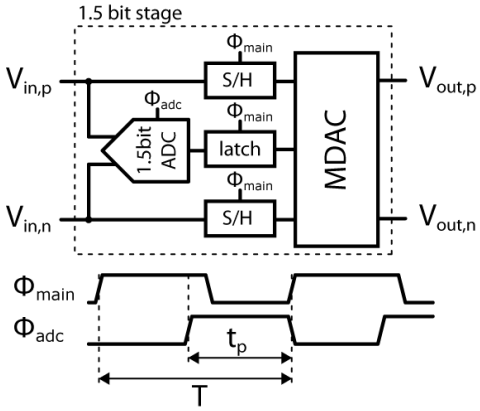


Figure 2. 1.5 bit pipeline stage with the associated timing diagram.

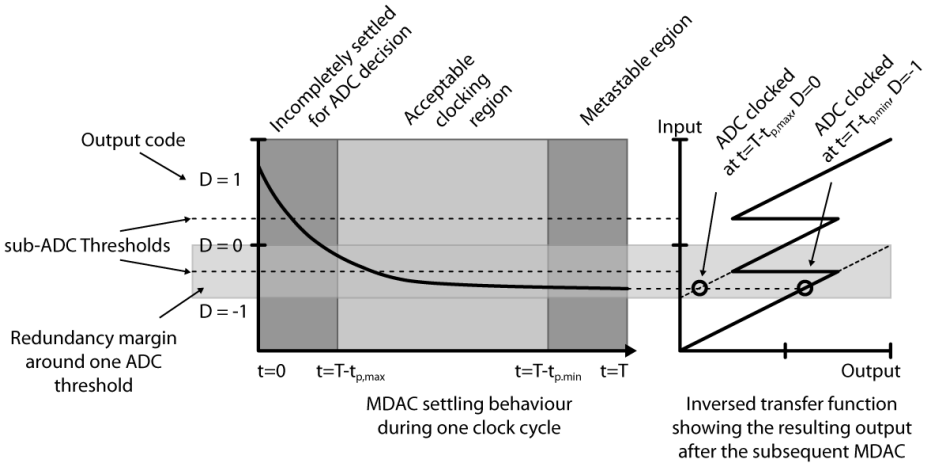


Figure 3. The effect of sub-ADC decision time on the MDAC output of the pipeline stage.

$t_p$ before the above-mentioned rising edge. At the rising edge the sub-ADC decisions are also latched making both the analog and digital inputs stable at this point in time. The MDAC then has the entire sample-period available for settling. After time T-$t_p$, the outputs have settled enough to be used by the sub-ADC in the following stage. Finally, at time T the output is latched by the following stage. The entire clock cycle is then used as follows. For the analog-to-digital path, it is used for limited MDAC settling plus comparator decision time. For the analog signal path, the full clock cycle is used for MDAC settling. The remaining sub-ADC time (T to T+$t_p$) is used for comparator reset.

Redundancy in pipeline ADCs allow for offset in the sub-ADC comparators without overdriving the MDAC output. In this design this redundancy is also used to allow the sub-ADC to take its decision on the incompletely settled MDAC outputs. If $V_{FS}/2$ is the single-ended peak amplitude of the input signal, then a sub-ADC comparator error of up to $V_{FS}/8$ is tolerable in 1.5bit pipeline architectures. If the error is larger than this the MDAC can overdrive the output range, which will result in missing codes. This allows the sub-ADC to be clocked at a time instant where the sum of comparator offset, noise and the decision settling error is less than the tolerable error. A time window now exists where the sub-ADC can be clocked. If it is clocked too early, the MDAC will not have settled completely and the resulting error will be larger than the redundancy tolerance. If the sub-ADC is clocked too late the comparator decision time will be too short which will result in a higher probability of metastable events with degradation in signal-to-noise ratio and bit error events. These timing constraints are illustrated in Fig. 3 with the left part showing the settling behavior of an MDAC. The output signal of the subsequent pipeline stage will depend on the sub-ADC decision with the different output possibilities being shown in the right part of Fig. 3.

## III. Circuit Implementation

With the sub-ADC of the first pipeline stage being located in front of the S/H, an additional input T/H stage that was shown in Fig. 1 is needed in order not to have the input signal vary from the time instant of the sub-ADC decision to the time the pipeline stage S/H samples the data. The T/H amplifiers are implemented using pMOS source followers.

### A. Sample-and-hold

Each pipeline stage should process a data sample each clock cycle. Because the entire clock period is dedicated to the MDAC settling time, interleaved sampling is used as shown in Fig. 4. The S/H stage includes four nMOS switches and two current-mode buffer stages. These buffers serve two purposes. The first is to prevent harmful charge sharing between the sampling capacitance and the input capacitance of the MDAC while the second is to convert an nMOS signal level, at the input, to a pMOS signal level, at the output. If the output pMOS is driving another pMOS with the same size, the gain is nominally one, as the currents in the two cases are the same. In order to control the common-mode level caused by clock feed-through and channel charge injection of the switch transistors, dummy transistors clocked with the opposite phase are used. The switches are controlled by non-overlapping clock signals.

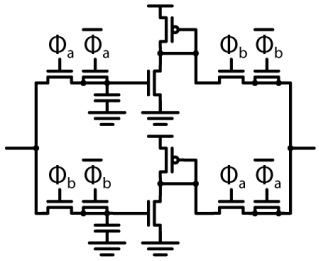


Figure 4. Interleaved sample-and-hold circuit.

### B. MDAC

The differential MDAC is shown in Fig. 5. Here we use a differential input signal ($V_{in,p} = V_{CM}+\Delta V$, $V_{in,n} = V_{CM}-\Delta V$) at pMOS levels, driving a p-to-n-stage, where the pMOS levels are converted to nMOS levels, making both available. In the following stage, $M_{3p}$ adds a current from $V_{in,p}$ to the output node and $M_{5p}$ subtracts a current from $V_{in,n}$ from the same node. Therefore we create $V_{in,p}$-$V_{in,n} = 2\Delta V$, the input signal doubled with common-mode removed. Furthermore, $M_{4p}$ and $M_{6p}$ (controlled by the sub-ADC) act as DAC and can add or subtract an appropriate current to the output node. The use of both nMOS and pMOS DAC transistors allows a differential voltage to be both added and subtracted to the output while

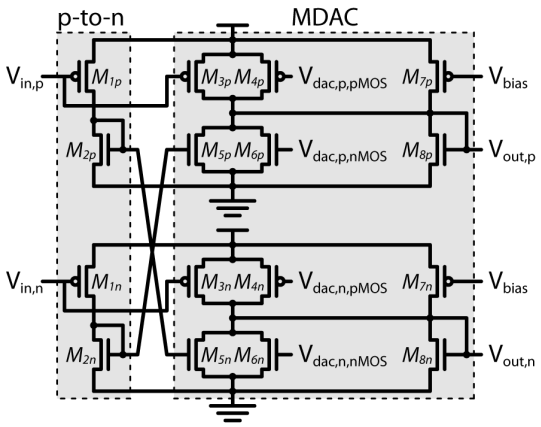


Figure 5. Differential MDAC implementation.

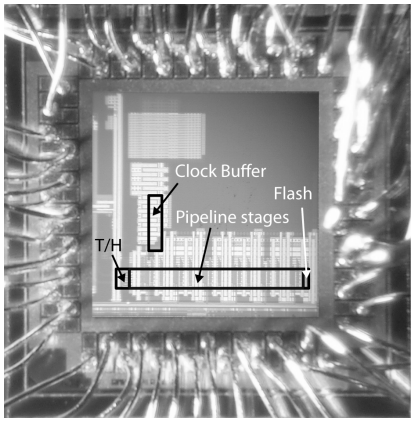


Figure 6. Chip micrograph.

leaving the common-mode level unchanged. $M_{7p}$ is used to set the output common-mode level while $M_{8p}$ finally constitutes the load of this stage, creating an output voltage with nMOS levels. In practice, the gain of the different stages differs from their nominal value due to nonzero output conductance of the transistors ($g_{d0}\neq 0$). Therefore all gains are adjusted by varying the transistor widths.

### C. *Voltage swing*

The voltage swing in this design is limited by the fact that we need to bias the transistors above a minimum gate voltage ($V_G>V_M$) and also to keep them in saturation. Consider for example the low input voltage, $V_L$, to the nMOS $M_{5p}$. Its gate voltage thus needs to exceed $V_M$, given by the minimum required $f_T$ of the transistor. For the high input voltage, $V_H$, symmetry and having an identical input range for all stages, will cause the output voltage over the MDAC load to be equal to the low voltage $V_L$. The transistor terminal voltages must be such that the transistor still remains in saturation. Simulations indicate that an nMOS DC level of 350 mV with a single-ended swing of 240 mV provides reasonable performance while not dissipating an excess of static power.

### D. *Noise analysis*

Following the studies in [4], the sampling capacitor is dimensioned according to the thermal noise requirements. The first sampling capacitor, in the T/H stage, is driven by 2 transistors, each with transconductance $g_{mTH}$ and an output impedance of $1/g_{mTH}$. The noise current squared into the load is $2\cdot 4\gamma kTg_{mTH}B$, where $\gamma$ is the transistor noise factor (assumed 1.5) and B is the noise bandwidth. With $B=g_{mTH}/4C_s$ this leads to a noise voltage squared at the output of $2\gamma kT/C_s$, which can be seen as an equivalent input referred noise voltage as the gain of this stage is 1. The next sampling capacitor (in S/H of the first pipeline stage) is driven by the output buffer of the T/H circuit, leading to another equivalent input referred noise voltage squared of $2\gamma kT/C_s$. The third sampling capacitor (in the second stage S/H) is controlled by the MDAC output, which is driven by the S/H buffer. This means that we have 8 transistors generating noise current to this capacitor (assuming both DAC transistors off). Assuming that they have about the same $g_m$, they will give rise to a noise current squared of $8\gamma kTg_mB$. With a load impedance of $1/g_m$ (MOS diode $M_{8p}$) and noise bandwidth of $g_m/4C_s$ the noise voltage squared is $8\gamma kT/C_s$. Note that there is a gain of 2 in this stage, so the equivalent input referred noise voltage squared is $2\gamma kT/C_s$. For the further stages in the chain, the equivalent input referred noise voltage is reduced by 4x due to their gain, making their importance small. Totally we estimate the equivalent input referred noise voltage squared to $6\gamma kT/C_s$. With a voltage swing of $V_{FS}$=240mV (single ended) we have a quantization noise voltage squared of $v_q^2=V_{FS}^2 2^{-2n}/12$. Equalizing the quantization noise and the estimated thermal noise for n=8b gives $C_s$=510fF for the single ended case. For the differential case noise squared is doubled and $V_{FS}^2$ is quadrupled, making $C_s$ half of the above value, 255fF. We have chosen to implement Cs≈250fF (including parasitics).

## IV. Evaluation and Measurement Results

The prototype pipeline ADC has been designed and fabricated in a general purpose 65nm CMOS process and the die photo is shown in Fig. 6. The active area of the ADC core occupies 0.6 x 0.07 $mm^2$. As the gain of the pipeline stages are hard to control and will vary from process variations and mismatch, error correction is performed. For this prototype ADC, it is not performed on-chip but implemented offline. The error correction principle is shown in Fig. 7 and follows a concept similar to [5]. The error correction works by correcting for gain errors in the pipeline stages as well as non-linear distortion in the input T/H stage. Each pipeline stage is modeled by two parameters, one gain estimation in the region where the DAC is inactive and another gain when the DAC is on, either adding or subtracting current. In the input stage, the non-linear distortion is modeled using two parameters, compensating for the 3rd and 5th order distortions. Working backwards, the digital output of the flash stage, $D_7$, is multiplied by the two gain parameters, corresponding to the reciprocal of the gains from stage 6. Depending on whether the DAC was active, one of the two outputs is chosen by a multiplexer and the digital output from stage 6 is added. This continues to the input stage, where the partial result, taken to

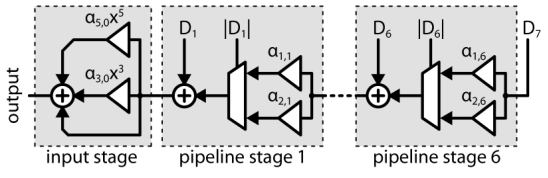


Figure 7. Error correction principle.

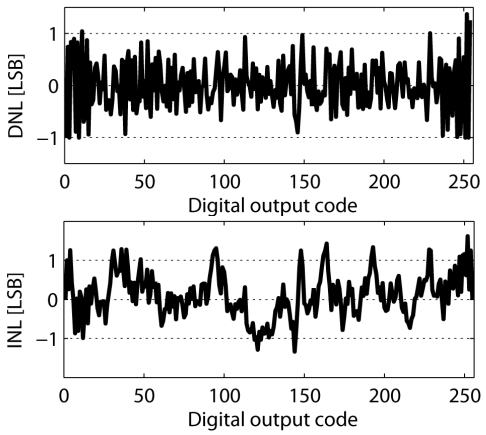


Figure 8. DNL and INL.

the power of 3 and 5, are multiplied with their respective coefficient and summed with the original output from stage 1 to generate the final output.

For the measurement, the chip was bare bonded on to the PCB and the digital output signals are downsampled by a factor of 32 for increased signal integrity. This downsampling factor is programmable between 1 and 32. First, the value of the error correction parameters are estimated using a low frequency input signal, based on maximizing the SNDR of the measured output data. The resulting DNL and INL after calibration are shown in Fig. 8. Using these parameters Fig. 9 shows the SNDR versus input frequencies for sample rates up to 2.4 GS/s while operating at a supply voltage of 1.0 V.

At 2.4 GS/s, the SNDR at DC is 34.1 dB, corresponding to an effective number of bits of 5.4. The effective resolution stays above 4.7 throughout the Nyquist band and is 4.9 at the Nyquist frequency. The higher resolution at DC can be explained by the fact that this is the frequency at which the error correction calibration was performed. The power dissipation of the entire ADC including output buffers is 318 mW and is measured for a Nyquist rate input signal.

The thermal noise level is estimated by measuring the SNDR versus input amplitude, and comes out to be below 8 bits, corresponding well to the theoretical level discussed in section II. Simulations indicate that the performance is limited by coupling through the substrate and supplies, generating noise, signal dependent distortion and inter-sample interference.

The measurement results are summarized in Table I together with state-of-the-art pipeline ADCs with high channel rates. It can be seen that this ADC achieves a sample rate almost twice that of all previously reported single-channel pipeline ADCs while still achieving a competitive figure-of-merit, which here is defined as $FoM=P/(2^{ENOB@DC}\cdot f_S)$.

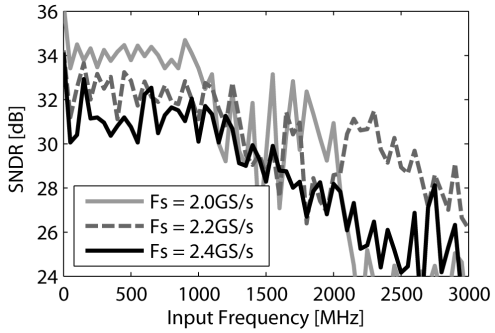


Figure 9. SNDR vs. input frequency for sample rates up to 2.4 GS/s.

## V. Conclusion

A prototype single-channel pipeline ADC with a sample rate of 2.4 GS/s has been presented. This is enabled by a new clocking technique which eliminates the comparator latency from the critical path as well as a fast, differential, current-mode MDAC with common-mode cancellation. The sampling rate of the proposed pipeline ADC is, to the authors' best knowledge, faster than any other reported CMOS pipeline ADC.

## References

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TABLE I. ADC Performance Summary and Comparison

| Author/ year | Architecture | CMOS Process | Sample Rate (GS/s) | Channel rate (GS/s) | SNDR @ DC | $SNDR_{min}$ DC-Nyquist | Power Dissipation (mW) | FoM (pJ/conv-step) |
|---|---|---|---|---|---|---|---|---|
| Shen [1] JSSCC-07 | Pipeline | 0.18µm | 0.8 | 0.8 | 33.7 | 31.5 | 105 | 3.3 |
| Varzaghani [2] JSSCC-09 | Interleaved Pipeline | 0.13µm | 4.8 | 1.2 | 30.4 | 30.0 | 300 | 2.3 |
| Nazemi [3] VLSI-08 | Interleaved Pipeline | 90nm | 10.3 | 1.3 | 36.6 | 32.4 | 1600 | 2.8 |
| **This Work** | **Pipeline** | **65nm** | **2.0**<br>**2.2**<br>**2.4** | **2.0**<br>**2.2**<br>**2.4** | **36.4**<br>**34.2**<br>**34.1** | **33.4**<br>**31.1**<br>**30.1** | **294**<br>**310**<br>**318** | **2.7**<br>**3.4**<br>**3.2** |