A 1.8 V 1.0 GS/s 10b Self-Calibrating Unified-Folding-Interpolating ADC With 9.1 ENOB at Nyquist Frequency

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***Abstract*—An advance in folding-interpolating analog-to-digital converters (ADCs) is demonstrated which simplifies their extension to higher resolution by building the converter out of identical but scaled pipelined cascaded folding stages. In this unified folding architecture the parallel coarse channel has been eliminated by recursively using the previous folding stage as the coarse channel for each following cascaded stage. This new architecture is demonstrated in a 10-bit ADC using six cascaded folding-by-3 stages with a total folding order of 729. At 1.0 GS/s, this interleave-by-2 ADC achieves $< \pm 0.2$ LSB DNL, $\leq \pm 0.5$ LSB INL, 9.2 ENOB at 100 MHz input, 9.1 ENOB at Nyquist, and 8.8 ENOB at 1 GHz input. The value at $F_{\rm IN} = 1$ GHz is 1 ENOB higher than any value published to date. The power consumption from a single 1.8 V supply is 1.2 W/channel which includes the LVDS drivers for this dual-channel (I and Q each running at 1 GS/s) ADC.**

***Index Terms*—Analog-to-digital conversion, calibration, CMOS analog integrated circuits, folding, high-speed techniques, interpolation, pipelined, Nyquist converter.**

I. Introduction

ANALOG-TO-DIGITAL converters (ADCs) have been relentlessly improved in the thirty-one years since the first monolithic device was commercially demonstrated [1]. Especially in CMOS technologies, the highest-resolution Nyquist ADCs have favored the residue-based pipeline architecture, often with a dedicated Track & Hold driving a 2–3 bit resolution first stage followed by scaled stages each resolving 1.5 bits. The flash architecture, by contrast, dominated for maximum single-channel conversion rate, but was limited in resolution to usually $M = 6$ or 8 bits, due to the area and power penalty of processing 2^M parallel analog paths.

The folding architecture [2]–[4] has potentially nearly the same conversion speed as flash, without the same restriction on resolution because the folded transfer curve results in much fewer parallel analog paths. The drawback of folding is the larger susceptibility to device mismatch especially when implemented in CMOS technologies, since MOS devices lead to larger offsets than bipolar devices. We recently showed that this disadvantage could be mitigated by an automatic user-transparent power-on calibration sequence, demonstrated in a 1.6-GS/s 8-bit ADC with 7.26 Effective Number of Bits (ENOB) at Nyquist [5].

With broad-market demand, especially in communications, justifying the extension of monolithic Giga-Hertz ADCs to resolutions above 8 bits, we faced a limitation of the classical folding architecture in high-resolution designs. As the resolution becomes higher, so does the required folding order. However, it becomes increasingly difficult for the parallel "coarse channel" to resolve in which of the folds the input signal lies. This paper presents this problem in more detail, our proposed solution which completely eliminates the need for a separate parallel coarse channel, and a demonstration of the resulting unified architecture in a 1.8 V 1.0 GS/s 10-bit ADC with 9.1 ENOB at Nyquist Frequency.

II. Folding-Interpolating ADC

Folding ADCs are well suited for high-speed conversion rates, due to the large parallel analog processing in the flash-like front-end stage. Fig. 1 shows such a flash stage which creates 27 parallel output signals from a single differential input voltage. For simplicity, this and later figures show this $V_{\rm IN}$ input voltage and the reference ladder as single-ended, although best practice for high-performance ADCs and all of the work presented here uses differential signals. A further simplification used through this paper is to represent the many parallel output signals from a flash stage by a single quantity $V_{\rm AMPx0,STAGE}$ defined for a flash/folding amplifier stage as the amplifier pair corresponding to the zero-crossing. Thus, the input varying between $V_{R,0}$ and $V_{R,26}$ which moves the stage 0 zero-crossing from amp 0 to amp 26 can be equivalently represented as $V_{\rm AMPx0,0}$ varying between 0 and 26. The utility of this description is that the output is now a single value $V_{\rm AMPx0,1}$, referenced to the zero crossings of the following cascaded stage (in this case stage 1), whose value also varies linearly between 0 and 26. Note that the "units" of "Amp 0" through "Amp 26" on the X axis refer to stage 0, and those on the Y axis refer to stage 1. This is equivalent to having the units "0 V" through "3 V" on both the X and Y axis of a unity-gain amplifier.

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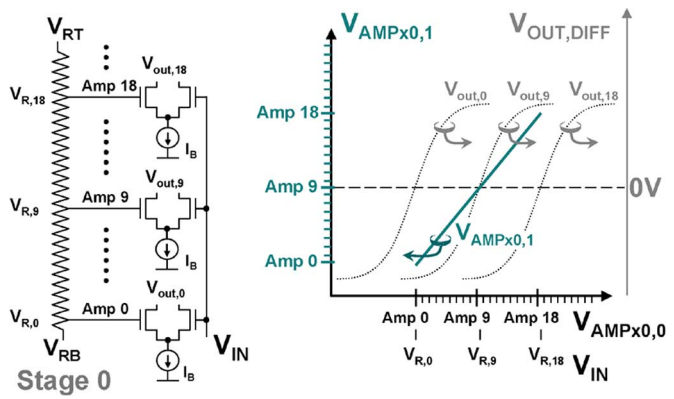

Fig. 1. Flash ADC stage with reference ladder. The set of differential output voltages can be replaced by a single quantity $V_{\mathrm{AMPx0,1}}$.

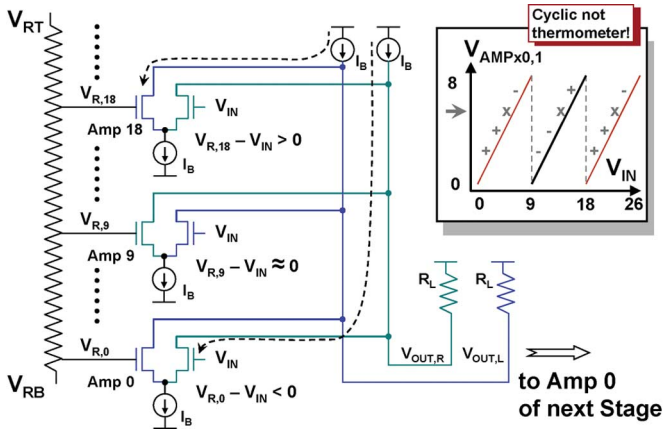

Fig. 2. Example of folding the outputs of an array of flash pre-amplifiers by 3 with graphically represented transfer curve. If V_{IN} is near $V_{R,9}$, amps 0 and 18 are fully saturated, and they do not affect the output voltage.

The pre-amplifier stage 0 of Fig. 1 which creates 27 zero-crossings is identical to that used in the ADC presented in the later sections, with the additional required zero-crossings for a 10-bit converter created by resistive interpolation [6]. To ensure good interpolation linearity, we only interpolated by-3, but multiple times in cascaded pre-amplifier stages 1 through N. Folding [2]–[4] prevents this interpolation from creating too many parallel analog paths, otherwise 2^M comparators are required for an M-bit converter. In this technique, the input range is divided (or folded) into multiple regions, each region sharing a smaller number of comparators to digitize the input. To accomplish this, the outputs of k widely spaced amplifiers that are part of a flash-array are tied together with alternately opposing polarities, as shown in Fig. 2 for $k = 3$. The amplifier whose reference voltage is close to the input voltage is "active", while the two amplifiers not close to a zero-crossing are saturated, and do not influence the comparator decision: Three detectable zero-crossings are at the desired values of $V_{R,0}$, $V_{R,9}$, and $V_{R,18}$. Therefore, the number of parallel analog channels (and therefore required comparators) has been reduced by the folding order, $k = 3$. In the case that 27 zero-crossings were provided by the reference ladder directly, or in practice by the preceding flash stage 0, nine groups of folded-by-3 are formed. Since the output is referenced to the zero-crossings of the next cascaded pre-amplifier stage, the output range is now only nine, 0 through 8. The resulting waveform is shown as an insert of Fig. 2, clearly showing the three regions the input transfer function has been folded into, reducing the number of parallel analog paths. However, the information of which fold corresponds to the input signal, V_{IN}, is lost. To date this information was obtained by parallel coarse channels, which in addition to adding power and loading required careful alignment between the coarse and the folded "fine" channel.

Note, in many of the publications on folding to date, the output is usually shown as a group of curves which are triangular in shape. By plotting the scalar value $V_{\mathrm{AMPx0,Stage}}$, a single saw-tooth output waveform results. A saw-tooth transfer curve appears to us conceptually more correct for describing folding, especially when it comes to designing the encoder, since the comparators/diff-pairs which go through zero-crossings are 0, 1, . . . 7, 8, and then again 0, 1, . . . 7, 8, (not 0, 1, . . . 7, 8, 7, . . . 1, 0, 1 . . . as the representation of a triangular waveform might lead one to erroneously believe).

By using the $V_{\mathrm{AMPx0,STAGE}}$ definition, we clearly see in Fig. 2 that the folding output contains extra information which reduces by 2X the problem of locating which fold corresponds to the input. If the comparators digitizing the folded signal resolve not just the location of the zero-crossing, but also its polarity (i.e., are the differential voltages below the zero crossing positive or negative), then this cyclic encoding will not only resolve the input voltage, but also whether the input lies in an even or odd fold. Although not explicitly published, this information has been used in the encoder to elegantly align the "fine" folding channel to the parallel coarse channel in many commercially produced folding ADCs.

III. Proposed Advance in Folding ADC

To fully exploit the folding technique for high-resolution converters requires a high folding order. A high folding order cannot be achieved in a single pre-amplifier stage, since the parallel signals which are folded need to be sufficiently spaced to ensure saturation of the inactive differential pairs. In addition, a single-stage high folding order would be slow due to the loading by these inactive differential pairs. For the parallel folding topology of Fig. 2, an odd number of folds is most power efficient, therefore we used the popular cascaded folding-by-3. In addition, to systematize the design, the converter was built out of identical but scaled cascaded folding-interpolating stages. Therefore, the interpolation order of each stage had to match the folding order, so that the input signal bus width matched the output signal bus width $(= 27)$. Following flash stage 0, there are six stages of folding & inter-polating-by-3, as shown in Fig. 3, which for clarity is drawn with a reduced signal bus width of only 9. Compared to previous work (including our own 8 bit folding ADC with folding order $k = 9$ [5]) the order of folding is extremely high $(k = 3^6 = 729)$.

A. Elimination of Coarse Channel

The primary problem with the high folding order, $k = 729$, is the difficultly in localizing in which fold V_{IN} lies. The coarse channel would need to be a 10-bit converter in itself, with the

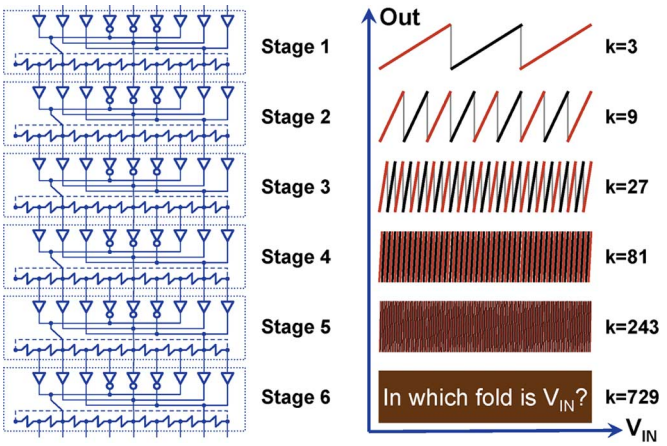

Fig. 3. Schematic and graphical representation of cascading folding-by-3 six times to achieve a folding order 729. The classical approach of using a separate coarse channel to determine in which of the final folds the input signal lies is prohibitive due to their close spacing and large number.

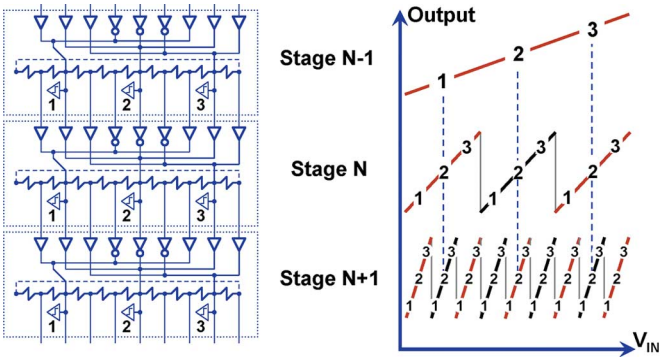

Fig. 4. Proposed approach to allow an arbitrary high order of folding: Each folding-by-3 stage contains 3 comparators, enabling it to act as the coarse channel for the following cascaded stage.

impossible task of aligning to the folding ADC of Fig. 3, due to both static and dynamic mismatches. However, a parallel coarse channel can be completely eliminated by using the previous stage to obtain the "coarse" information of which fold $V_{\rm IN}$ lies in for the following cascaded stage, as shown in Fig. 4, which is a simplified schematic of 3 of the 6 scaled pre-amplifier stages used in this design. It is because the coarse channel functionality is integrated into the "fine" channel containing the folding stages that we refer to this architecture as unified-folding.

B. Distributed Comparators

The three comparators of Fig. 4 are equally spaced inside each amplifier stage on existing/propagated signals, such that their crossing points are folded into the complete analog channel transfer curve as shown. By knowing the exact position of $V_{\rm IN}$ in Stage N-1, the particular fold for Stage N is localized. The position of $V_{\rm IN}$ in Stage N-1 is in turn iteratively determined by the previous stages. This extends the work of [7] where a coarse channel existed but was distributed. Distributing the comparators also reduces their total number. In our previous 8-bit folding ADC [5], there were 43 comparators; for the 10-bit design presented following, there are only 20 comparators (3 for each folding stage, plus 2 at stage 0, the non-folded first flash stage).

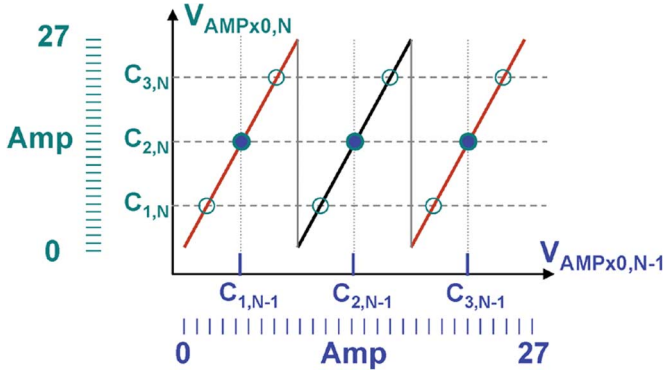

Fig. 5. The three evenly-spaced comparators of stage N-1 map directly onto comparator C_2 of stage N, allowing the more highly gained stage N to correct the comparator offset errors of stage N-1.

C. Recursive Error Correction

By using an identical folding order, interpolation factor, and comparator number for each stage, comparator 2 of each stage is actually redundant with comparator 1, 2, or 3 of the previous stage. Fig. 5 shows how the zero-crossings detected by comparators of stage N-1 ($C_{1,N-1}$, $C_{2,N-1}$, and $C_{3,N-1}$) map directly onto the zero-crossing detected by midcomparator of the stage N ($C_{2,N}$). Thus, there are two recursive information transfers down the length of the cascaded ADC pre-amplifier stages. In the forward direction, stage N-1 recursively localizes the fold for stage N; in the reverse direction the output of each comparator 2 from the more highly gained stage N corrects the decision of all comparators of stage N-1. Intuitively, it may seem that the two simultaneous information paths cannot co-exist without contradicting one another. However, this is not the case, since the comparator correction in the reverse direction can not change the value of the fold in the forward direction: The encoder which computes the correction and fold assignment uses the polarity information of the zero-crossings as described previously. This results in excellent differential linearity and complete sparkle suppression while requiring only relaxed comparator accuracy, since the Referred-To-Input (RTI) gain at the final comparators exceeds 5000. The encoder complexity is high due to the error correction which can ripple from the last stage back to the first. In addition, the analog processing is implemented fully in power-of-3, so the encoder requires a base-3 to base-2 conversion. Fortunately, modern IC processes are well suited for such digital synthesis.

IV. Implementation of Proposed Architecture

Figs. 1–5 exactly represent in simplified form the ADC used to demonstrate the proposed architecture, with the exception that Figs. 3 and 4 only show an analog bus width of 9 instead of 27. With 3 comparators even in the final pre-amplifier stage 6, there are three times as many final zero-crossings as folds, or $3\times3^6 = 2187$ levels, sufficient for 11 bits. For this ADC, the encoder output is truncated to 1025 levels, resulting in a 10 bit converter with over-range.

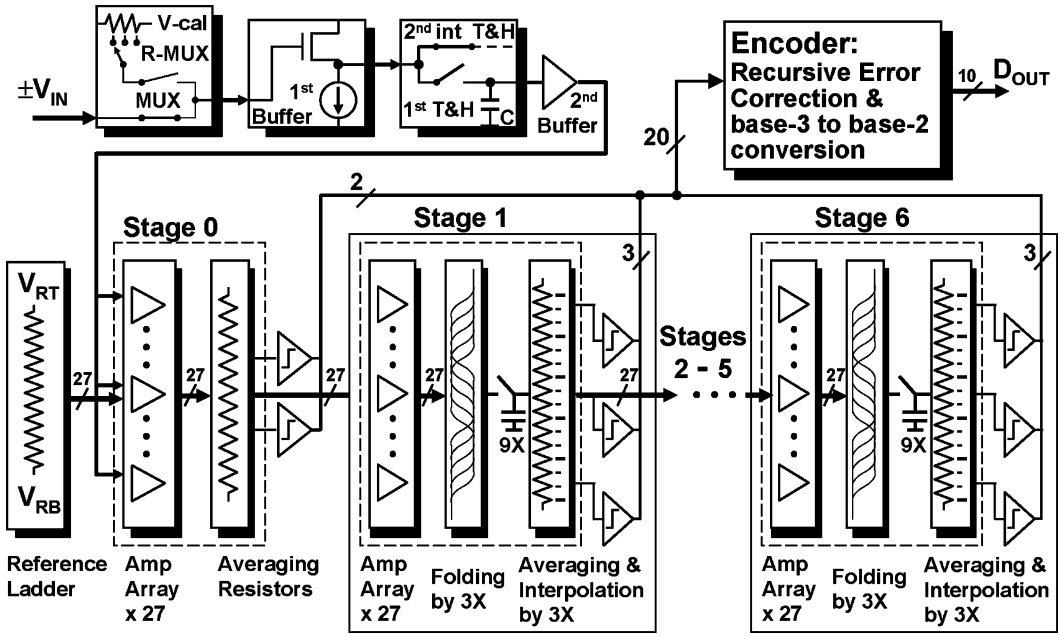

Fig. 6. Block diagram of the realized self-calibrating unified-folding-Interpolating ADC, showing only the first interleaved channel.

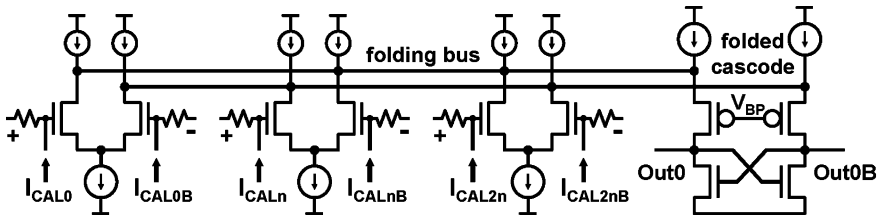

Fig. 7. One of nine triplet folding-sections of the folding-interpolating stage with calibration adjust resistors used at stages 1, 2, and 3.

A. ADC Implementation

Fig. 6 shows only one channel of the by-2 interleaved unified-folding-interpolating ADC. During normal operation, the input signal is routed by a MUX to the Track & Hold, whose differential output signal is combined with the differential flash reference ladder in stage 0 to create an analog bus of 27 differential signals. This bus width of 27 is maintained through the cascaded folding-interpolating stages 1–6, to allow the same pre-amplifier block to be optimized once, and then be repeatedly reused for each stage in a down-scaled form as previously mentioned. The 20 comparator outputs are gathered by the encoder which performs the recursive error correction, fold determination, and base-3 to base-2 conversion as a single combinatorial logic function. The CMOS level outputs are converted to LVDS before being driven off-chip, to minimize the noise fed back to the sensitive analog input stage.

B. Pipelining

The previous discussion on the cascaded folding-interpolating stages implicitly assumed some form of alignment between the distributed comparators and the analog signal propagating as a 27-wide differential analog bus from stage 0 to stage 6. The simplest and most exacting alignment between comparator strobing and propagating analog signal is to use pipelining, so that the comparators from stage N-1 and next stage N can sample the same settled signal. Pipelining has the additional advantage of substantially extending the allowed settling time of each pre-amplifier stage as first demonstrated in folding ADCs in [8], since one clock period does not need to be divided among all stages' settling. The pipelining is implemented by using the MOS gate capacitance present in the amplifier arrays as the storage element, which becomes the held voltage node after completion of the tracking or acquisition phase. To minimize the number of signals which need to be held, pipelining is performed after folding but before interpolation, so that only 9 signals need to be held as indicated.

C. Offset Calibration

The input MUX prior to the input buffer allows the automatic application of on-chip generated reference voltages during the user-transparent self-calibration of the amplifier offsets at power-up, especially important in this CMOS design. The technique used is similar to our previous work on an 8-bit ADC [5], but in this case the foreground offset calibration has been expanded to include stages 2 and 3. The application of the offset correction is through digitally controlled DACs for each of the 27 parallel diff-pairs for these stages, as shown in Fig. 7. Stages 4, 5, and 6 do not require offset calibration for this 10-bit design despite their larger offsets resulting from their down-scaled device size. The gain of stages 0 through 3 is sufficiently large to make the RTI effect of these offsets negligible.

Although schematically represented as a resistor, the calibration reference voltages are generated on-chip using a segmented DAC, which achieves a 14-bit integral linearity of 0.8 LSB by using layout randomization of its current sources to cancel first and second order gradient effects [9]. The reference voltages are selected to force a zero-crossing for each of the 27 diff-pairs for stages 1, 2, and 3. The offsets and non-linearity of the input buffer, Track & Hold, its output buffer, and stage 0 are all mapped to stage 1 and corrected concurrently during its calibration.

D. Track & Hold and Clocking

Because the conversion speed of the ADC described in this paper is high for a CMOS technology, the open-loop topology from our earlier work [5] was reused for the Track & Hold. A pseudo-differential architecture which uses two separate but identical circuits for the positive and negative part of the differential input signal simplifies implementing the constant $-V_{GS}$ switch, required to retain low distortion at high input frequencies. The input buffer and sampling switch were increased to minimize third harmonic distortion, with both limiting the performance in equal measure. The power and distortion of the input buffer were again deemed necessary, since this buffer provides isolation between the noisy capacitive sampling, and the external amplifier driving the ADC whose settling performance is further degraded by the inductance of the bond wires to the ADC's input pads. Furthermore, the displacement current of an unbuffered switch-capacitor input would add nonlinearity to the reference DAC voltages.

A total sampling jitter target of 100–200 fs-rms required greater immunity to power-supply noise than achievable with CMOS logic. Even in the presence of perfect external supplies, there is sufficient noise generated by the ADC itself, from its encoders, output drivers and clock switching to strongly degrade clock purity which does not have a high PSRR, especially given the epi-based technology used. As a result, the clock path was designed in differential CML logic as much as practical, despite of the resulting area and power penalty. The CML clock path could not run right up to the Track & Hold given that a large CMOS level swing was necessary for the constant $-V_{GS}$ sampling switch.

E. Interleaving-by-2

As seen in Fig. 6, interleaving-by-2 is used, so that at 1 GS/s each interleaved ADC is running at 500 MS/s. A master sampling clock as in [10] minimized the timing offset between the two channels. Because the two interleaved ADCs are calibrated by the same reference DAC, the offset and gain mismatches between the two channels is automatically also calibrated. Note that the presented ADC has two inputs, I and Q, and that each of these uses an interleaved ADC. Thus, there are actually four 500 MS/s cores on one die.

V. Comparison to Residue Pipelined ADC

Due to the similarities between the proposed architecture and the "classical" pipelined ADC [11], we will briefly compare them. The classical pipeline architecture is residue based (which is how we will refer to it for distinction), where at each stage the signal is applied both to multiple comparators and amplified for presentation to the next cascaded stage. However, in the unified-folding ADC the analog amplification is done fully open loop, unaffected by the comparators' results; any interaction between the stages beyond signal propagation is strictly in the digital domain of the encoder. In the residue-based pipelined ADC, amplification of the residue must await the comparator decision at that stage, so that the MDAC can be set correctly to shift the amplified signal to fit the range of the next cascaded stage. This waiting time for the comparator result is one of the factors limiting the maximum conversion rates of residue-based pipelined ADCs. A more complete comparison between these two architectures is given in Fig. 8. V_{REF} is the single-ended reference voltage and V_{AMP} is the single-ended output swing of the differential amplifiers. The main disadvantage of the unified-folding architecture is that amplifier offset affects INL, due to the parallel analog paths. The main advantage is no need for a linear DAC, since the residue is not explicitly calculated, and no need for a high gain-bandwidth amplifier in comparison to the classical residue-based pipelined ADC.

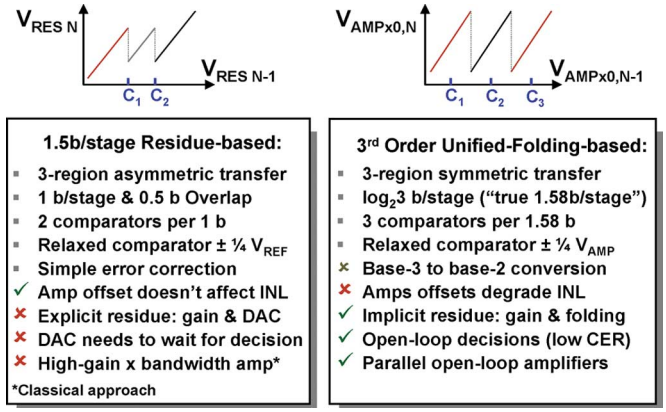

Fig. 8. Residue versus unified-folding pipelined ADCs.

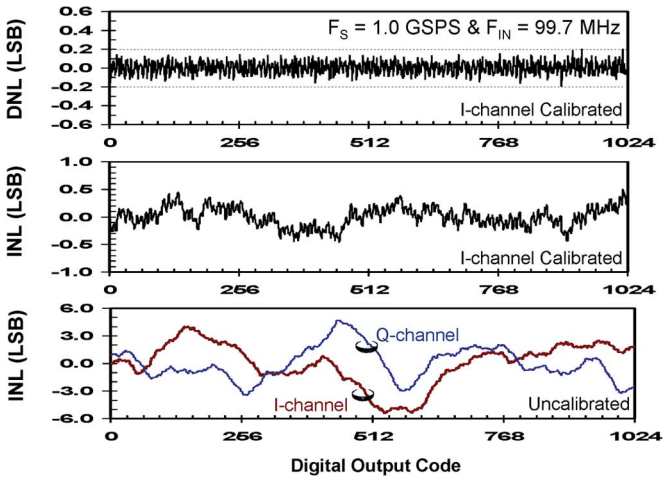

Fig. 9. Measured 4M-point DNL and INL at 1.0 GS/s.

VI. Experimental Results

Fig. 9 shows the DNL ($< \pm 0.2$ LSB) and INL ($\leq \pm 0.5$ LSB) at 1.0 GS/s for just the I-channel with a 97.77 MHz sine-wave input extracted with a least-squared fit. In addition, INL is plotted for both the I and Q channel with calibration disabled. The uncalibrated INL curve is typically $< \pm 6$ LSB. The use

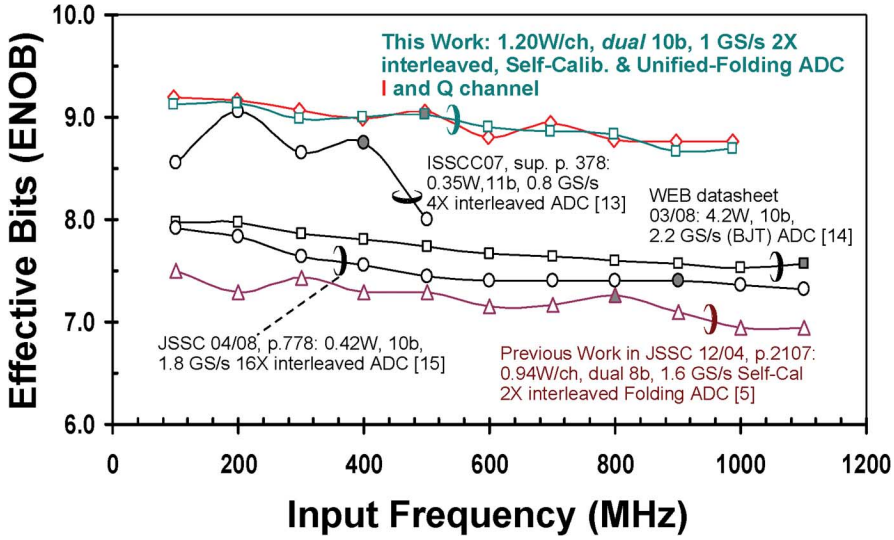

Fig. 10. Measured ENOB versus $F_{\rm IN}$ for this and comparative work. Filled symbols show the Nyquist Frequency.

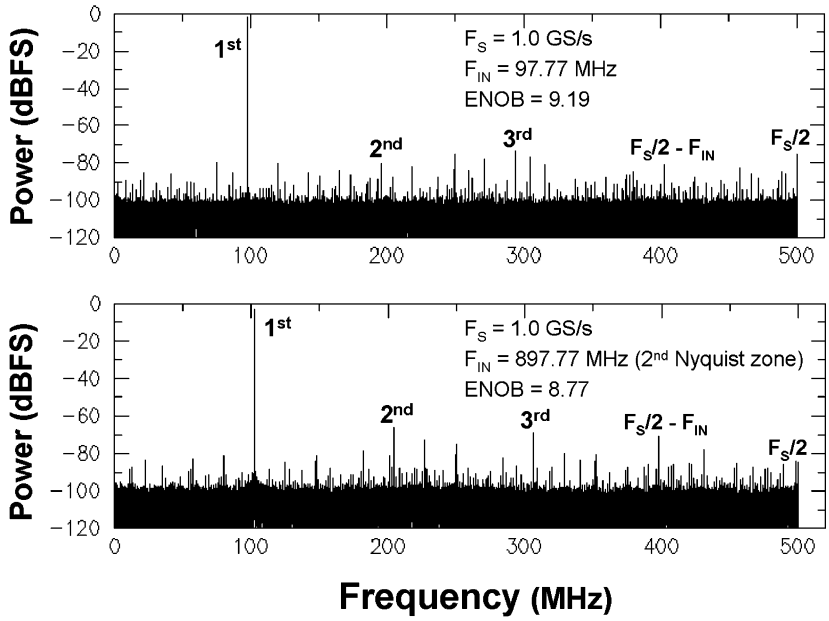

Fig. 11. Measured 128K-point FFT Spectrums at 1.0 GS/s for $F_{\rm IN} = 97.77$ MHz and 897.77 MHz.

of best design practices (such as averaging the output of the pre-amplifier arrays [12]) to optimize the ADC linearity prior to introducing calibration resulted in this small required calibration range, simplifying the calibrator circuitry and resulting in stable continuous performance over time without recalibration.

Fig. 10 plots ENOB versus input frequency for both the I and Q channels, starting at 9.2 ENOB, achieving nearly 9.1 ENOB simultaneously at Nyquist, and maintaining nearly 8.8 ENOB up to 1.0 GHz input. The remarkably small SNR roll-off versus input frequency (from 57.4 dBc @ 100 MHz to 55.5 dBc @ 1 GHz) results from the extremely low clock jitter which we estimated as $<$ 180 fs-rms for the combined contributions of the clock and input sources and ADC itself, using the equation

$$\text{SNR\_MAX}(dB) = -20\log_{10}(2\pi F_{\rm IN} t_{j,RMS})$$

and attributing all of the SNR degradation at $F_{\rm IN} = 1$ GHz to the effect of the rms aperture jitter, $t_{J,RMS}$. For this same figure we have also plotted the most recent $\geq 8b$ ADCs in the GS/s range. At 1.0 GHz input this 10b ADC's performance is more than one ENOB above prior art [13]–[15]. The spectrum of just the I-channel FFT is shown for 100 MHz and 900 MHz input in Fig. 11.

A 1.0 GHz beat-frequency test is shown in Fig. 12, in which the input and sampling frequencies are almost identical, resulting in a low frequency output signal corresponding to the difference or "beat" between F_{CLK} and $F_{\rm IN}$. In this case, the sampling period is slightly longer than the period of the input signal, resulting in an time resolution given by $T_{CLK} - T_{VIN} =$ 100 fs. The output toggling at the peak of the sine-wave between two codes separated by one LSB is consistent with a RTI device noise simulation of the ADC of between 1/4 and

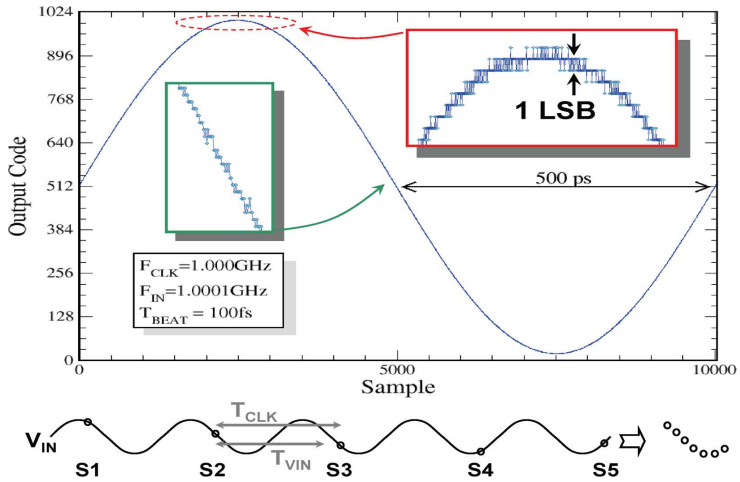

Fig. 12. Measured 1.0 GHz beat-frequency response, which increases the time resolution 10,000 X by repetitive sampling. The principle of the test is indicated below.

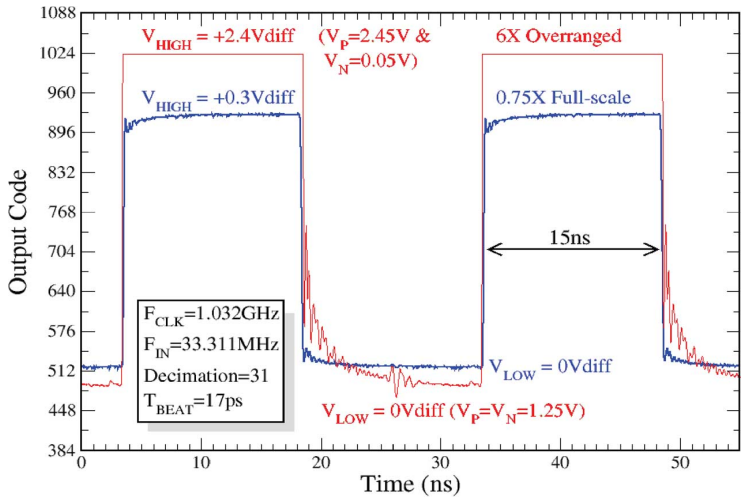

Fig. 13. Measured 6X over-range pulse response. The time resolution has been again increased by repetitive sampling, this time with decimation due to the lower $F_{\rm IN}$.

1/3 LSB-rms. Note that the errors at the center of the sine-wave increase beyond 1 LSB as jitter/timing errors become significant at the maximum slew. A graphical representation of the test principle is indicated in the lower part of the figure, where the input sine-wave is drawn as a solid line, and the sampling positions indicated as small circles.

Fig. 13 shows that graphical decimation can be used to create a beat-frequency test even when the input frequency is substantially smaller than the sampling frequency, in this case to quantify the over-range recovery of the ADC. Instantaneous over-range recovery is desired not only in test and measurement applications and telemetry (where the receive path may be partially exposed to the large transmit path signal), but also broadband communication systems where maximizing the bandwidth will result in the peak signal levels exceeding the input range of the converter. For all measurements presented to this point, the input of the ADC was ac-coupled. In this and the subsequent pulse measurement, the output of a differential digital pulse generator was directly dc-coupled to the input of the ADC. The over-range exceeded not only the $\pm$410 mV differential input range by 6 times, but as a result also the 1.8 V power-supply rail by 650 mV. As a result, it was not immediately clear if the settling tail seen was due to the ADC or measurement setup including the pulse generator. However, this was resolved by zooming into this settling tail, plotting it divided-by-8 so that it could be overlaid on the non-over-ranged +0.3 V pulse; see Fig. 14. Since these two waveforms exactly overlay, the response is linear, and there is no over-range induced nonlinearity. The settling tail and disturbance seen at 26 ns is the result of the measurement setup, most likely a combination of imperfect impedance matching, cable propagation times, and settling of the pulse generator.

One final measurement, a single-shot pulse response, is presented in Fig. 15. The extremely flat long-term settling is important for test and measurement applications, where the accuracy of frequency content near dc is critical. This is completely flat to 1 LSB also beyond the 0.5 μs shown in the insert, top right. The immediate transient response,

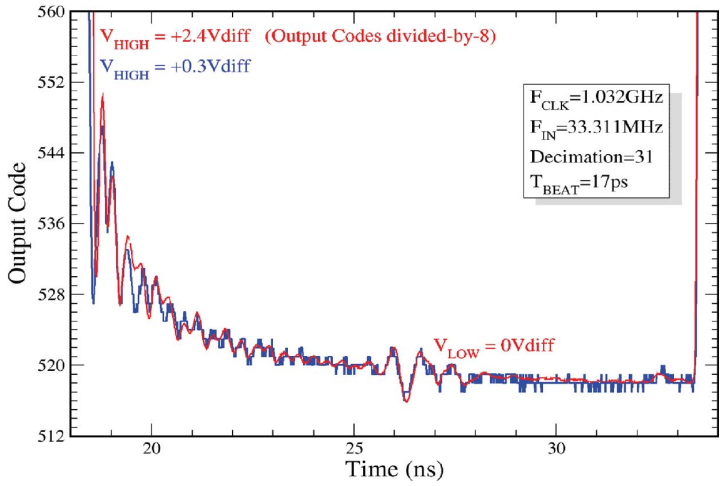

Fig. 14. Zoom-in of over-ranged output plotted divided-by-8, which perfectly overlays eight-times smaller 0.3 V pulse.

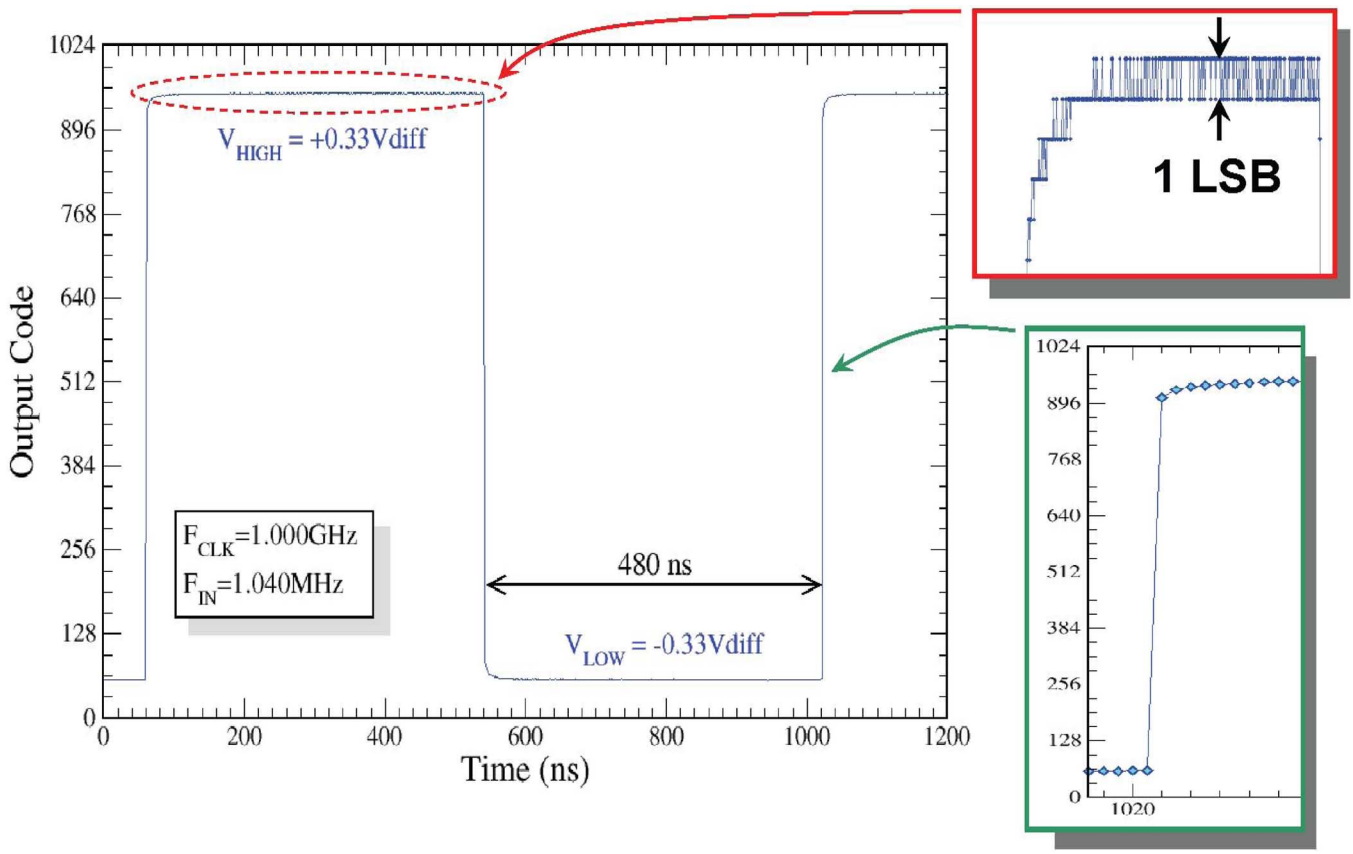

Fig. 15. Measured DC-coupled pulse response showing no long-term settling or "thermal tails". The output is not repetitively sampled in this plot.

bottom right is limited by the input bandwidth of the ADC.

Table I shows a performance summary at 1.0 GS/s and 1.8 V. We wish to stress that all of the data presented here was taken for a packaged & socketed part with both channels powered up and the I & Q data taken simultaneously including both I and Q LVDS 10-bit wide busses running at 1 Gbps for each bit. The total power with an active input is 1.26 W/channel and with a dc input is 1.20 W/channel, which includes the LVDS drivers. Data was captured at full speed (i.e., with no on-chip decimation) without any post processing or off-chip correction. All spectral specifications are with respect to the carrier, not full scale, and measured at -0.3 dBFS. For the plot of Fig. 10, comparative data was converted to the standard ENOB definition in the event that the ENOB was full-scale referenced.

A die photo of the pad-limited ADC is shown in Fig. 16. Because top metal obscures most structures, the circuit blocks are indicated. The Track & Hold and clocking are on the left followed by the calibration adjust DACs which surround the I and Q ADCs, each of which is interleaved by 2X. The output of

TABLE I
ADC PERFORMANCE SUMMARY FOR I AND Q CHANNELS SIMULTANEOUSLY CAPTURED DATA

	I-Channel	Q-channel
Sample Rate, F_S	1.0 GSample/s	
Resolution	10 bits	
Max DNL	+0.19 / -0.19 LSB	+0.18 / -0.20 LSB
Max INL	+0.50 / -0.46 LSB	+0.42 / -0.72 LSB
SNR @ F_{IN} = 497.77 MHz	56.9 dB	56.5 dB
SFDR @ F_{IN} = 497.77 MHz	66.3 dB (H3)	68.6 dB (H3)
THD @ F_{IN} = 497.77 MHz	- 65.4 dB	- 67.6 dB
ENOB @ F_{IN} = 497.77 MHz	9.06	9.04
Jitter @ F_{IN} = 997.77 MHz	< 180 fs-rms	< 170 fs-rms
ENOB @ F_{IN} = 497.77 MHz	9.09 for I-channel with Q-input = DC	
I/Q X-talk @ $F_{IN} \leq$ 900 MHz	≤ - 70 dB	
Input –3 dB Bandwidth	> 3 GHz	
Over-range Recovery	Instantaneous (< 17ps)	
Input Range	±410 mV differential	
Input Capacitance	~ 2 pF	
Input Termination	50 Ω (100 Ω differential)	
Single Supply	1.8 V	
Power @ F_{IN} = 97.77 MHz	1.26 W / channel including full-speed LVDS outputs	
Power @ F_{IN} = DC	1.20 W / channel including full-speed LVDS outputs	
ADC die area	49 mm^2 (for dual ADC, pad limited)	
Package	292-pin BGA	
Technology	0.18 μm Triple-well CMOS (1-poly, 6-metal) No capacitor module nor dual-gate process	

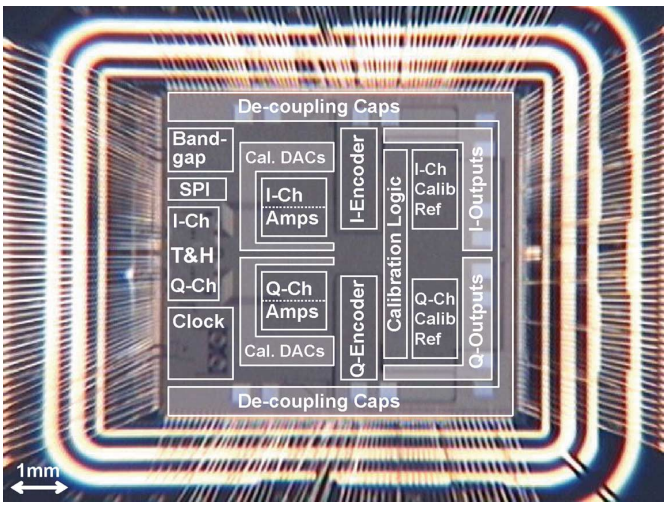

Fig. 16. Die photo of dual (I and Q both operating at 1 GS/s) 10-bit ADC in 292 pin BGA.

the CMOS-level encoders drives directly to the LVDS output drivers which form the perimeter of most of the chip. Their large number results from the ADCs optionally providing the data in 1:2 deMUX format for slower (but therefore wider) data-capture. The reference DACs used for calibration are located beyond the encoders and digital calibration logic on the right.

VII. CONCLUSION

We have presented an advance in folding-interpolating ADCs in which the parallel coarse channel has been eliminated by recursively using the previous folding stage as the coarse channel for each following cascaded stage. Alignment between the comparator values for a signal propagating through the cascaded pre-amplifier stages is simplified by using pipelining. In addition, this pipelining extends the allowed settling time for each pre-amplifier stage. An additional design methodology was to build the converter out of identical but scaled pipelined cascaded folding stages. By using an identical folding order, interpolation factor, and comparator number for each stage, comparator overlap allows error correction. Thus, there are two recursive information transfers down the length of the cascaded ADC pre-amplifier stages. In the forward direction, stage N-1 recursively localizes the fold for stage N; in the reverse direction each comparator 2's output of the more highly gained stage N corrects the decision of all comparators of stage N-1.

This new architecture is demonstrated in a 10-bit ADC, using six cascaded folding-by-3 stages with a total folding order of 729. An on-chip user-transparent foreground calibration was used to correct for the amplifier offsets at power-up, improving linearity approximately 10X. At 1.0 GS/s, the ADC achieves $< \pm 0.2$ LSB DNL, $\leq \pm 0.5$ LSB INL, 9.2 ENOB at 100 MHz input, 9.1 ENOB at Nyquist, and 8.8 ENOB at 1 GHz input. The value at $F_{\mathrm{IN}} = 1$ GHz is 1 ENOB higher than any value published to date. The power consumption from a single 1.8 V supply is 1.2 W/channel which includes the LVDS drivers for this dual-channel (I and Q each running at 1 GS/s) ADC.

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