A Single Channel 2GS/s 6-bit ADC with Cascade Resistive Averaging

Youtao Zhang * , Xiaopeng Li, Ao Liu, Ming Zhang and Feng Qian

Abstract —*A single channel 2GS/s 6-bit ADC with cascade resistive averaging is demonstrated in 0.18μm CMOS. The proposed power efficient crossing connection method of averaging resistors has less reference voltage consumed than convention with excellent offset averaging. The peak DNL and INL are measured as 0.26 LSB and 0.21 LSB, respectively. The SNDR and SFDR have achieved 34.2 and 37.5dB, respectively, with 1.22 MHz input signal and 2GS/s. The SNDR and SFDR maintain above 30 and 35dB, respectively, up to1000MHz input signal and 900MS/s. The proposed ADC, including on-chip track-and-hold amplifiers and clock buffers, consumes 570 mW from a single 1.8V supply while operating at 2GS/s*[1].

Index Terms —Analog-to-digital conversion, offset averaging, flash, interpolation.

I. INTRODUCTION

Monolithic high-speed Analog to Digital Converter (ADC) is a key component in modern high performance digital signal processing systems such as software defined radio, disk drive read channel, digital oscillograph et al. For the resolution of 6bit, flash architecture is the most general choice for GS/s converters. However, the conventional flash architecture needs 2^{N-1} preamplifiers and comparators, which lead to a big challenge of ADC linearity, die area and power consumption. So, many mixed architectures and new technology are developed for decreasing power dissipation and improve performance [1]-[7].

This paper describes the realization of a single channel 2GS/s 6-bit ADC with on-chip track-and-hold amplifier (THA). The chip use interpolation and cascade resistive averaging to achieve good static linearity and dynamic performance, without self-calibration or autozero..

II. ADC ARCHITECTURE

The detail block diagram of the proposed ADC is shown in Fig.1, including wideband THA, the first pre-amplifiers, the second cascade amplifiers with 2 times interpolation, comparator stage, digital encoding with error correction and output stage. In the cascade amplifiers, continual resistor averaging is used to decrease mismatch between amplifier arrays, which also relieve the strict requirements of comparators offset and obtain lower power consumption.

[1] Youtao Zhang is with the National Key Laboratory of Monolithic Integrated Circuits and Modules, Nanjing Electronic Devices Institute, NanJing, China(e-mail: zhangyt@nedc-ic.com).

Xiaopeng Li is with the Integrated Circuit Laboratory, Nanjing Electronic Devices Institute, NanJing, China(e-mail: lixp@nedc-ic.com).

Ao Liu is with the Integrated Circuit Laboratory, Nanjing Electronic Devices Institute, NanJing, China (e-mail:liua@nedc-ic.com)..

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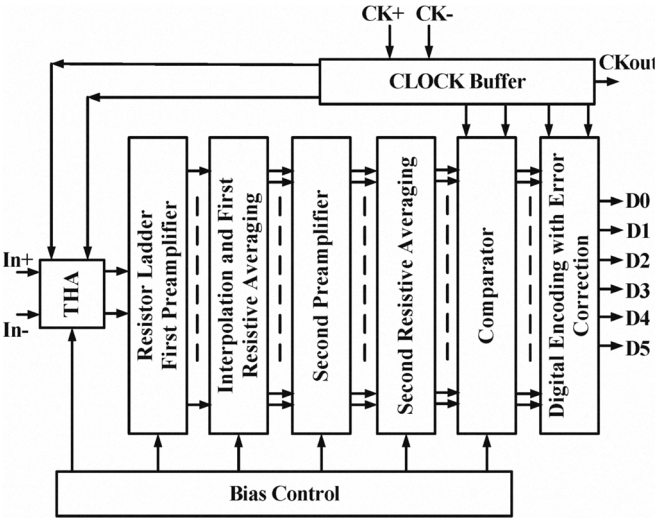

Fig. 1. Block Diagram of the proposed ADC

A. Wideband THA

Because a front-end THA will relax the requirement of preamplifier bandwidth, the THA is extremely important for the GS/s ADC dynamic performance, especially for effective resolution bandwidth (ERBW). An on-chip open-loop pseudo-differential THA is shown in Fig.2 [8], [9].

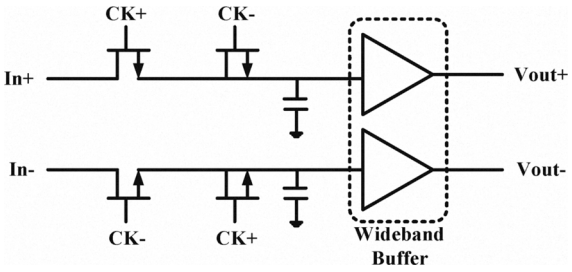

Fig.2. On-chip wideband THA

In each channel THA, a passive FET switch connected to the hold capacitance is used to achieve broadband and high dynamic distortion. To overcome the charge injection, which is signal-dependent and drastically deteriorates THA distortion, a dummy switch driven by the complement of its corresponding sampled switch clock is used. The dummy switch should be sized up to share the dumped charge suitably and lower the common-mode jump. The low input common-mode voltage and appropriate switch size are also critical to get a good switch on-resistance. Simulations show that the distortion between the two differential nodes of the hold capacitance could be lower than -60dBc, when quantizing a 244MHz full scale sine wave at 2GS/s.

B. Cascade amplifiers with resistor averaging and interpolation

The preamplifiers should be wideband and provide sufficient gain to overcome comparator offsets. In this design, the needed gain is equally distributed in two cascaded preamplifiers to obtain the maximum signal bandwidth which is important for quantizing high frequency signal. However, the offset errors of amplifiers are the main drawback to limit the ADC resolution. It is more obviously in multistage amplifiers. Resistor averaging is used to effectively reduce the offset voltages of the preamplifiers and enhance ADC static performance, which allows to use minimum-sized transistors in preamplifiers and further lowering the input capacitance of the ADC [3],[7]-[9]. The proposed resistor average could correct the boundary bending problem with low penalty of area and power consumption, which is shown in Fig.3.

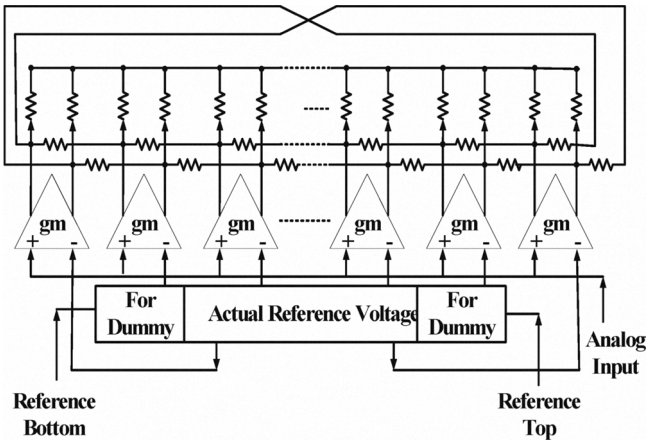

Fig.3. Proposed averaging resistor termination

Only two dummy amplifiers which waste the useful reference voltage are inserted at the bottom and top level of the amplifier array. The input of another two boundary dummy amplifiers are all from inner reference and input signal. This topology maintains the averaging effect with minimally decreasing the useful reference voltage and lower power consumption of dummy amplifiers. For the condition of 6mv quantizing step and 20mv Gauss-distributed offset (1 σ), 100 times Monte-Carlo simulations illustrate the proposed resistive averaging effect. Fig 4(a) shows the zero-crossing linearity of the first preamplifiers array using proposed resistive averaging, which indicates its mean DNL<0.35LSB and INL<0.83LSB. Fig 4(b) shows the corresponding results without proposed averaging, which indicates the mean DNL<3.68LSB and INL<2.67LSB. So, the proposed resistive averaging could get 10.5/3.2 times improvement for DNL/INL even under huge offset.

The second preamplifiers array uses the same averaging technology. As a result, the cascade amplifiers and averaging could get both needed gain and good linearity before comparator stage to obtain excellent total linearity of ADC.

In order to decrease the number of the first preamplifiers and input capacitance, the uniform resistive interpolation is

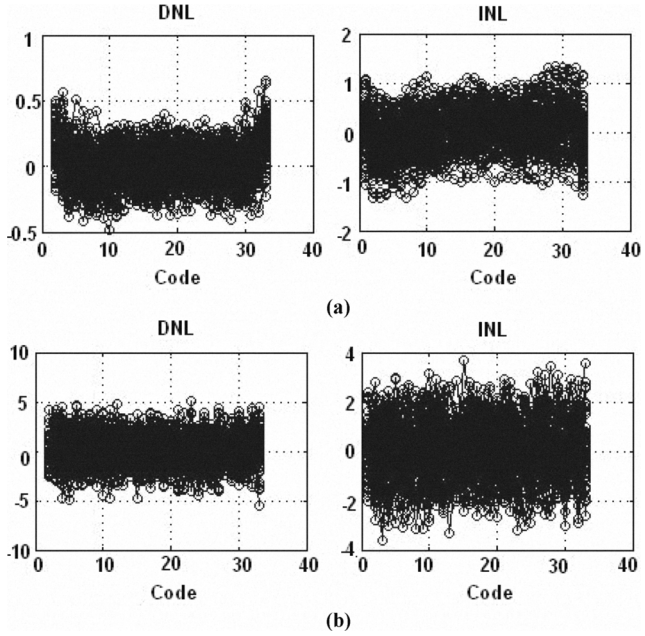

Fig.4. Linearity performance comparison between using (a) and not using (b) proposed resistive averaging

chosen, as shown in Fig.5. By a resistor voltage divider, the extra output signals are generated without adding anymore power consumption. At the same time, offset averaging is done.

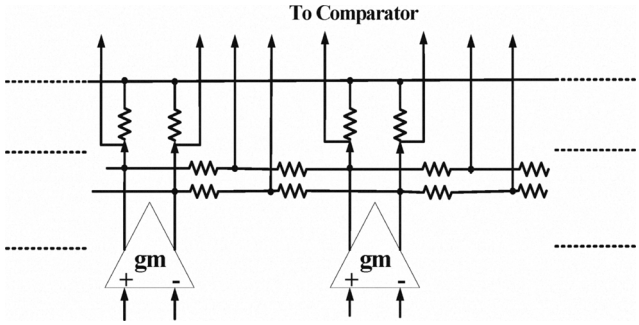

Fig.5. Uniform resistive interpolation

C. Comparator

The proposed comparators include regenerative comparator and RS Latch. Fig.6 shows the topology of the regenerative comparator.

A reset switch is added to solve the overdrive recovery which limits the comparator speed [9]. In track phase, the comparators vary with input differential voltage through M1/M2/M3. At the same time, the reset switch M7 shorts the differential output nodes to quickly eliminate the memory of the previous decision state. In latch phase, the reset switch is open and the comparators are configured into a positive-feedback with M4/M5/M6 so that the comparators output decision state. The gain during regenerative latch should be large to overcome dynamic offset and comparator metstability. A RS latch following the CML comparators to improve the metstability and bit error rate further.

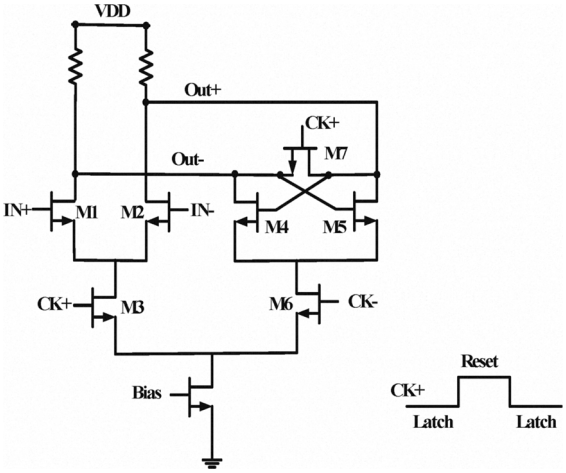

Fig.6. Regenerative comparator with reset switch

D. Digital Encoding with Error Correction

A ROM-based encoder after comparators stage maps the thermometer code to 1-of-n code. 3-input nand and quasi-Gray encoding are used to overcome bubbles and spikes [9]. Only one stage xor gates are needed to convert quasi-Gray to binary code without pipelined delay of conventional Gray encoding. Flip flops are inserted to guarantee the high-speed timing. 6 channels 1:2 DMUX are used to slow down the output data rate for feasible using. Otherwise, in this design 16 times decimation is optional for testing and debugging. The output buffer could driver the load of 50ohm with CML logic level.

III. EXPERIMENTAL RESULTS

The ADC is implemented in 0.18μm CMOS technology. The die size restricted by many extra pads is 3.1mm × 1.7mm, as shown in Fig.7. Many decoupled capacitances are placed on the empty areas of the die.

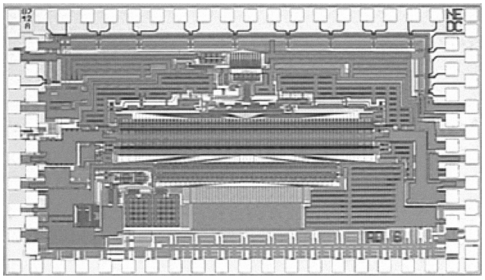

Fig.7. Chip photograph

The ADC is mounted in a100-pin CQFP for all tests. Excluding output buffers and including THA and clock buffer, it consumes about 480mW from a single 1.8V at 1GS/s, and 570mW at 2GS/s. The peak DNL and INL are recorded in Fig.8 as 0.26 LSB and 0.21 LSB, respectively. Fig. 9 shows that the SNDR and SFDR reach 34.2dB and 37.5dB, respectively, at 1.22MHz input frequency with 2GHz clock. They maintain above 30dB and 35dB, respectively, for input signal frequency up to 1000MHz with 900 MHz clock, as shown in Fig.10. The Figure-of-Merit for this ADC, defined as Power/(2^ENOB*2*ERBW), is 6.5 pJ per conversion step. Table I shows a performance summary of the proposed ADC.

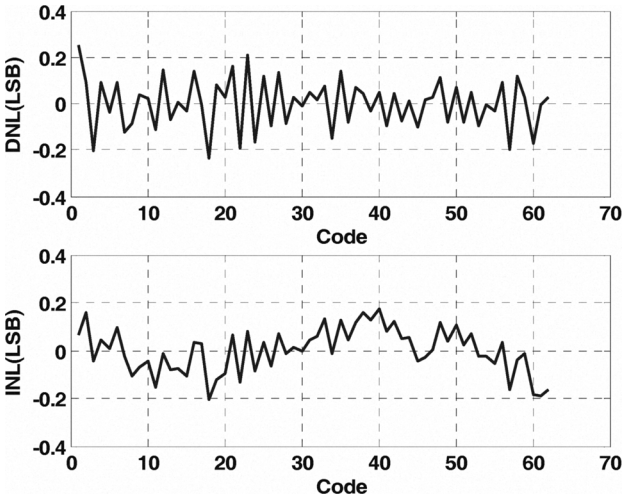

Fig.8. DNL and INL of the ADC

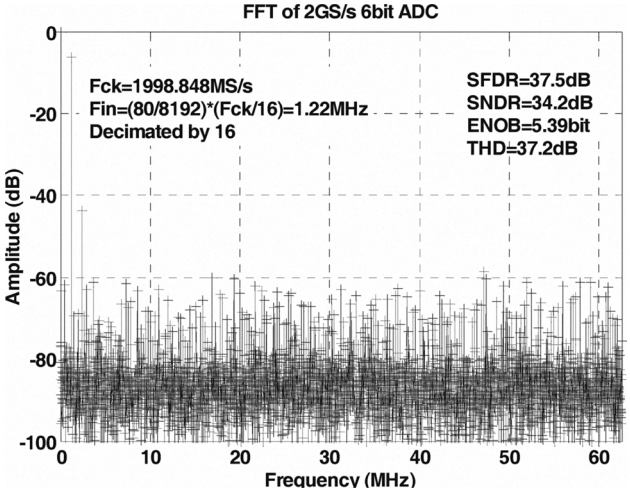

Fig.9. FFT of the proposed ADC

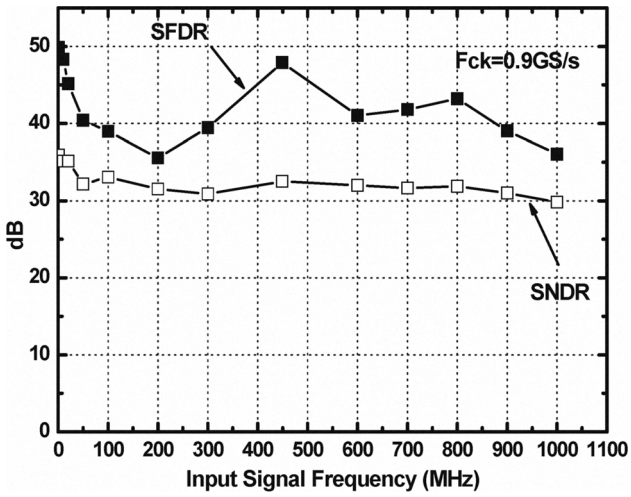

Fig.10. SFDR and SNDR as a function of input frequency

TABLE I
ADC PERFORMANCE SUMMARY

Item	Value
Resolution	6bit
Supply voltage	1.8V
Input range	800mvpp, diff
ENOB	5.39bit @2GS/s
DNL/INL	0.26/0.21
Power consumption	570mw@2GS/s
Die area	3.1mm × 1.7mm

IV. CONCLUSION

A single channel 2-GS/s 6-bit ADC is implemented in a 0.18μm CMOS technology. The architecture of the proposed ADC is based on a flash type with interpolation and cascade resistive averaging. A proposed termination method has excellent offset averaging effect with less reference voltage consumed. Broadband on-chip THA and cascade resistive averaging ensure the dynamic performance of ADC. The peak DNL and INL are 0.26 LSB and 0.21 LSB, respectively. The SNDR and SFDR reach 34.2dB and 37.5dB at 2GS/s with 570mW power consumption.

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