A 3 bit 20 GS/s Flash ADC in 65 nm Low Power CMOS Technology

Damir Ferenci, Markus Grözing, Felix Lang, Manfred Berroth

Institute of Electrical and Optical Communications Engineering, University of Stuttgart
Pfaffenwaldring 47, 70569 Stuttgart, Germany

damir.ferenci@int.uni-stuttgart.de

***Abstract*— A 20 GS/s 3 bit flash ADC with a wide analog bandwidth is realized in a 65 nm CMOS technology. By employing a fourfold parallelization a high sampling rate is achieved, while a large input bandwidth is maintained. The measured effective resolution is between 2 bit and 2.5 bit at a sampling rate of 12.8 GS/s and between 2 bit and 2.3 bit at a sampling rate of 18 GS/s. The power consumption of the ADC core is 2 W, the core area is 0.16 mm².**

I. Introduction

Fiber dispersion limits the maximum transmission distance in 10 to 40 Gbit/s fiber-optic systems. A solution is the implementation of an electronic equalization e.g. by a Viterbi equalizer with preceding analog-to-digital conversion. This equalization method requires a relatively low resolution of about 3 bit [1], [2].

Recent advances in CMOS technology allow the design of analog circuits in the range of multiple Gigahertz, which was traditionally dominated by bipolar technologies. Relatively expensive multi-chip solutions can be replaced by cost-efficient single-chip solutions [3]. This is the motivation for the development of high-speed ADCs in CMOS technology.

The fastest published CMOS analog-to-digital converter (ADC) with a sampling rate of 24 GS/s achieves an effective resolution of 4.2 bit at 8 GHz input signal frequency and 3.5 bit at 12 GHz input signal frequency. With a 160-fold parallelization the core area of the chip is 16 mm² [4].

In [5] we presented the simulation results of the ADC, whereas in this work we present the measurement results at 12.8 GS/s and 18 GS/s. With a core area of only 0.16 mm², this ADC is the smallest compared to any state of the art ADCs with sampling rates in this range. This allows for a cost-effective integration of multiple converters on a single chip. In the above described application of a 40 Gbit/s equalizer, we can integrate two ADCs followed by a Viterbi equalizer on a single chip in a state of the art CMOS technology [6].

II. ADC Architecture

The basic concept of the ADC is a fourfold parallelized flash ADC which is clocked by a four phase clock divider (Fig. 1). The analog input is demultiplexed by the sample and hold circuit. Following the sample and hold circuit a quantizer and decider is performing the quantization of the sampled input signal. Subsequently the thermometer code is encoded into the binary code. Finally all four channels are synchronized by a three step synchronizer to allow for a synchronous data output of all four channels.

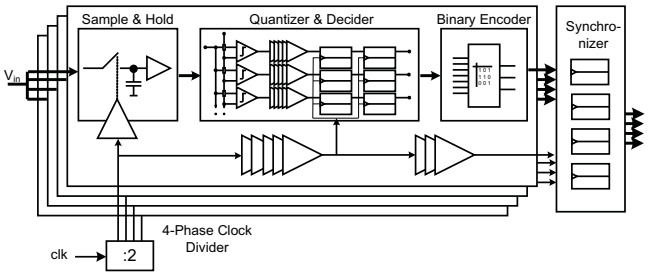

Fig. 1. Block diagram of the 3 bit ADC.

A. Sample and hold circuit

The sample and hold circuit in Figure 2 contains a track and hold circuit, followed by a linear open loop amplifier and a second track and hold circuit. The track and hold circuits are compensated by n-channel transfer transistors for clock feedthrough. The first track and hold circuit is compensated at the output side, while the second track and hold circuit is compensated at the input and the output side. The hold capacitances of the track and hold circuits are composed of the parasitic capacitances of the connected transistors and the wiring capacitances. The amplifier is used to drive the second track and hold circuit and the comparator stage. The linearity and the gain of the amplifier are optimized for a differential input voltage range of +/-400 mV and a common mode voltage of 900 mV [7].

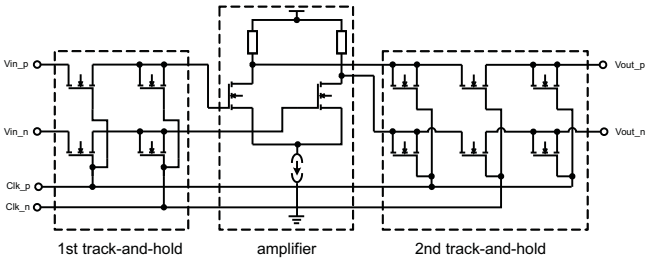

Fig. 2. Sample and hold circuit.

The clock signals for the sample and hold circuits are generated by the four phase clock divider. The clock divider is realized as a cross coupled static flip-flop. A fine tuning circuit for the duty cycle correction is added at the output of the clock divider for compensation of process variations and mismatch effects. A CML-to-CMOS converter is used to generate the CMOS voltage levels which are driving the sample and hold circuits clock drivers.

B. Analog Input Demultiplexer

The block diagram of the analog input demultiplexer is depicted in Fig. 3. It is build up of four sample and hold circuits, CMOS clock drivers and two bootstrap circuits. The CMOS clock drivers are used to obtain a high voltage swing, the bootstrap circuit is used to pull up the voltage levels by the value of the lowest input voltage. Due to the high voltage swing of the CMOS clock drivers and the implemented bootstrap circuit the on-resistance of the transfer gates is very low.

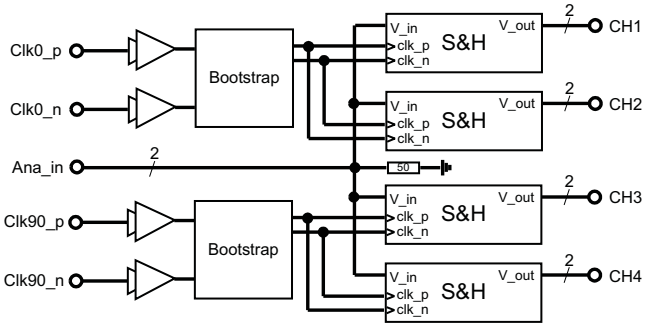

Fig. 3. Analog demultiplexer input stage of the ADC.

C. Quantization Circuit

The quantization circuit is depicted in Figure 4. It is realized by seven comparators followed by five CML stages and two flip-flop stages.

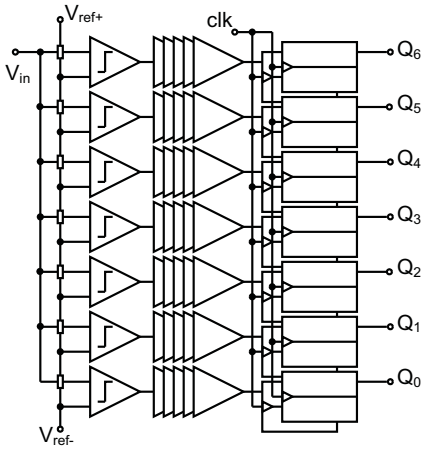

Fig. 4. Quantizer and decider circuit.

Each comparator compares the input signal with a constant reference voltage generated by a resistive reference ladder. The comparator has a gain of about one. Thus comparator input voltages near a reference voltage level lead to a very low comparator output voltage. The subsequent five CML stages amplify the signal by a factor of about eight. As the logic level swing is 300 mV, this gain is not sufficient to reach a defined logic level. To solve this problem the two stage flip-flops are connected to the output of the CML stages. As a flip-flop is composed of two latches and a latch has infinite gain while it is in the hold mode, undefined voltage levels at the input of the flip-flop stage are amplified to either logic level.

D. Thermometer-to-Binary Encoder

After the quantization stage a ROM-based thermometer-to-binary encoder is generating the three bit binary code (Fig. 5). A priority encoder, implemented by XOR-gates, generates seven select signals, which are directly encoded by OR-gates into the 3 bit binary code. The regular and symmetric structure of the circuit ensures equal delays for all paths which is necessary at the high clock rate of the circuit.

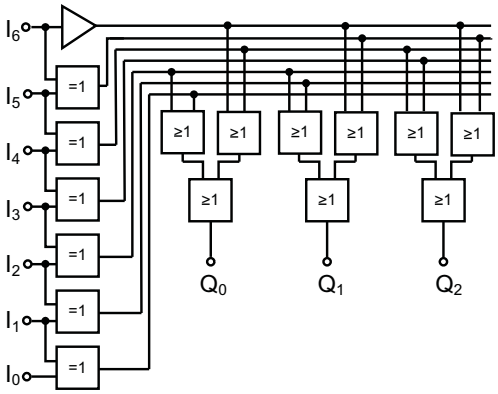

Fig. 5. Thermometer-to-binary encoder.

E. Synchronization Circuit

To simplify the interface to subsequent circuits a synchronization circuit was added to the outputs of the four channels (Fig. 6). The phase difference between channel one and four is 270 degrees, flip-flop stages are shifting the data 90 degree-wise closer to each other, resulting in a synchronization of the two channels after three stages. Channels two and three are shifted once and twice, respectively. Data synchronous flip-flop stages are added to channels two and three after data shifting to maintain all four channels synchronous.

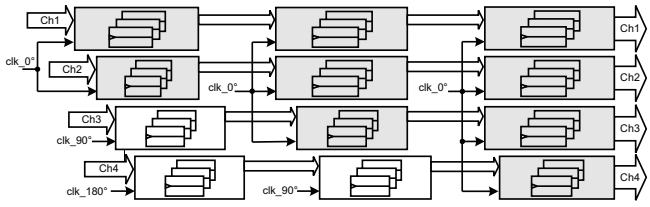

Fig. 6. Digital output synchronization.

III. Layout

The chip is fabricated in a 65 nm LP process, the chip size is 2.3 x 2.3 mm². The layout of the ADC and the ADC core is shown in Fig. 7. In the figure a part of the chip is hidden by the enlarged ADC core, this part contains blocking capacitors and the same output drivers as on the right hand side of the chip.

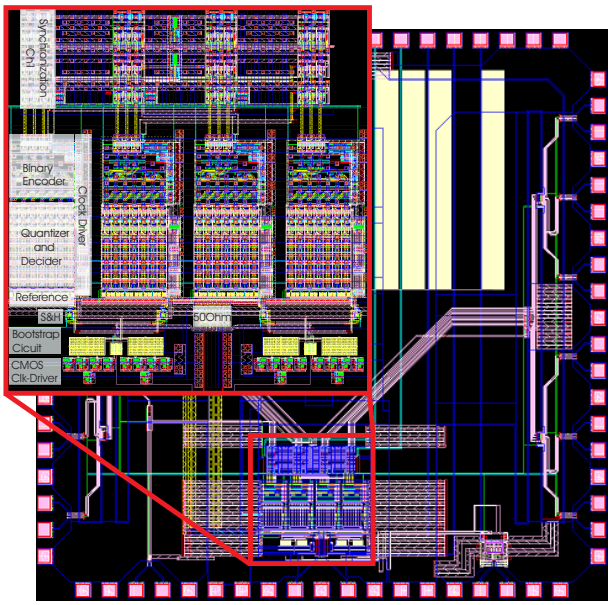

Fig. 7. Layout of the ADC chip.

The analog input is routed to the center of the ADC core and terminated by a 50 Ohm resistance to ground. A T-line structure connects the inputs of the sample and hold circuits to the 50 Ohm termination resistor. The sample and hold circuits are located directly in front of the corresponding comparator stage. The large sampling switch clock drivers are placed together with the bootstrap circuit below the sample and hold circuits, to minimize parasitic effects on the clock lines. Above the sample and hold circuit the comparators are placed together with the resistive reference ladder. Following the comparators the five CML stages, the decision flip-flop stages and the thermometer-to-binary encoder form an ADC channel. All clock drivers are placed directly to the right hand side of each stage. The clock drivers are optimized to exhibit the same delay as the signal path. This ensures a maximum setup time for the flip-flop stages. All four ADC channels are placed very close to each other and form together with the synchronization circuit the ADC core.

The digital outputs are on the left and the right hand side. The analog input, the clock input and the clock output are on the bottom side. An additional half rate clock output and control signals are on the top side. The ADC core is placed close to the analog input. The output of the synchronization circuit is connected to two intermediate synchronization and amplification stages, to compensate for internal losses.

IV. Measurement Results

The ADC is mounted on Taconic RF-60A substrate. The chip is placed in the center of the substrate and bonded to RF transmission lines, which are routed in a star-like layout. The analog input signal is generated by a sinusoid generator and balanced with a 180 °-hybrid. The amplitude is kept constant at the maximum input voltage range over the measured frequency range, by compensating the losses of the input transmission lines up to the bond wire of the chip. The real-time output data from the ADC is stored into the embedded RAM of a Virtex4 FPGA. The used FPGA is equipped with gigabit interfaces, which operate up to a speed of 6.5 Gbit/s. The measurement data is transferred offline to a PC where a discrete Fourier transform (DFT) is computed in MATLAB to calculate the signal-to-noise-and-distortion-ratio (SNDR) and the effective resolution. Fig. 8 shows an example of a measured time domain signal and the corresponding frequency spectrum. The example measurement shows the results of a single ADC channel operating at a quarter of 17.92 GS/s, resulting in a single channel sampling rate of 4.48 GS/s. The input frequency is 4.935 GHz, the number of samples is 128.

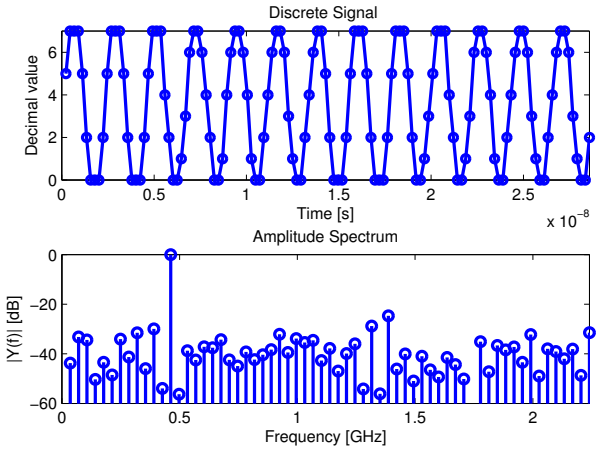

Fig. 8. Single channel measurement result: Sampled signal and frequency spectrum of a sinusoidal input signal with a frequency of 4.935 GHz at a sampling rate of 4.48 GS/s.

In Fig. 9 the single channel measurement results for a combined sampling rate of 12.8 GS/s are depicted. Due to mismatch the results of the individual channels differ by up to 0.5 bit, the best channel has an effective resolution above 2.5 bit up to 7 GHz input signal frequency. Figure 10 shows the single channel measurement results for a sampling rate of 17.92 GS/s. The effective resolution of the best channel is above 2.3 bit up to 10 GHz input signal frequency. The difference between the channels shows the necessity of a calibration circuit. The calibration circuit can be added to the resistive reference ladder without affecting the input bandwidth as in [8]. After multiplexing all four channels to a single 17.92 GS/s channel an effective resolution above 2 bit is achieved (cf. Fig. 11). Table I summarizes the chip performance and Figure 12 depicts the micrograph of the ADC chip.

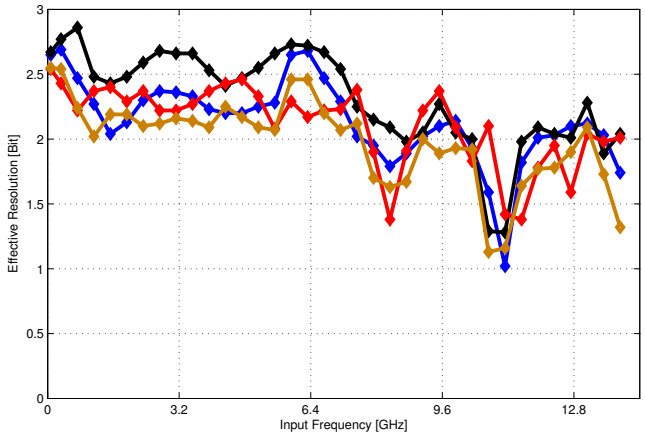

Fig. 9. Effective resolution versus the input signal frequency of the four ADC channels, each channel is operating at 3.2 GS/s.

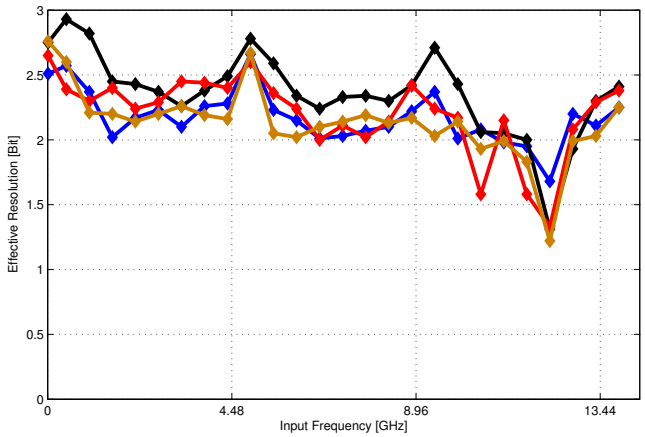

Fig. 10. Effective resolution versus the input signal frequency of the four ADC channels, each channel is operating at 4.48 GS/s.

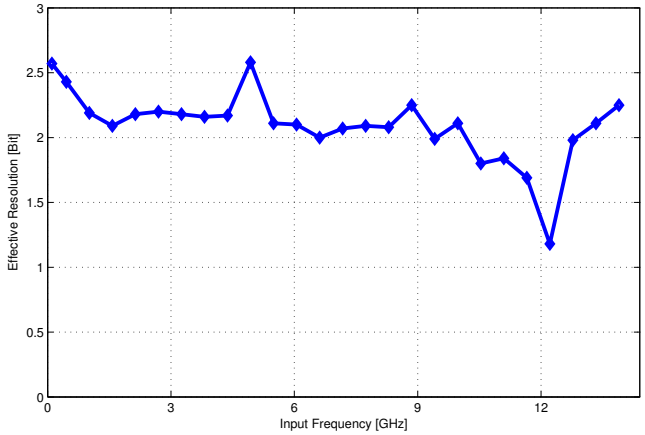

Fig. 11. Effective resolution versus the input signal frequency of the ADC at 17.96 GS/s.

TABLE I
ADC PERFORMANCE

Nominal resolution	3 bit
ENOB @ 10 GHz	2 bit
Conversion rate	2-20 GS/s
Input voltage range	0.8 $V_{pp\text{-}diff}$
Supply voltage	1.5 V
Core power consumption	2 W
Chip power consumption	3.1 W
ADC core size	0.16 mm^2
ADC chip size	5.2 mm^2

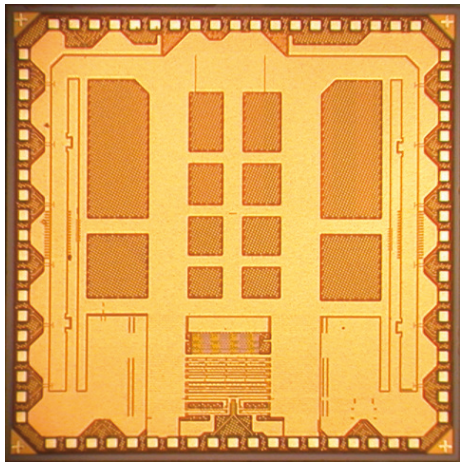

Fig. 12. Micrograph of the ADC.

V. CONCLUSION

The presented 3 bit 20 GS/s CMOS ADC achieves an effective resolution above 2 bit, while occupying a very small core area of 0.16 mm^2. This is the smallest chip area ever reported for an ADC with a sampling rate above 20 GS/s, and a hundred times smaller than the currently fastest CMOS ADC [4]. This allows for the cost-effective integration with a Viterbi equalizer for high speed fiber-optic systems on a single CMOS chip [6].

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