A 40 GS/s SiGe Track-and-Hold Amplifier

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ABSTRACT— **An ultra-high-speed SiGe track-and-hold amplifier (THA) using a switched-emitter-follower (SEF) configuration is presented. Operating off a +5.5 V power supply, this THA exhibits -32.4 dBc of total harmonic distortion (THD) when sampling a 10 GHz input signal at the rate of 40 GS/s, and reaches -50.5 dBc of THD when sampling a 2 GHz input at 12 GS/s. Compared to the THAs published in the literature with an operational range from 10 GS/s to 20 GS/s, the present THA demonstrates a THD comparable to the best one achieved to date to our knowledge for Si technology, with much improved high-frequency characteristics. On the other hand, in the operational range of 30 GS/s and above, the present SiGe THA still exhibits robust characteristics compared to the fastest THAs in terms of linearity, power consumption, and sampling rate.**

Keywords: ADC, SiGe HBT, Silicon-Germanium (SiGe), Track-and-Hold Amplifier (THA)

I. Introduction

With the rapid evolution of digital CMOS technology, the processing power of modern digital signal processors has greatly improved over time, requiring a large increase in analog-to-digital conversion rates to improve the overall system performance. Therefore, high-speed analog-to-digital converters (ADC) have emerged as a performance-limiting factor in many wireless and wireline systems, and are therefore receiving significant attention. With the increased performance requirements on power, accuracy, and bandwidth, especially from telecommunications and measurement instrumentation systems, the design of ultra-high-speed ADCs represent a serious challenge. Among all of the ADC building blocks, the track-and-hold amplifier (THA), located at the ADC's frond end, is a critical one, since it will in large measure determine the ADC's overall performance. Several high-speed THAs with a different operational ranges and linearity performance have been reported recently. For instance, a SiGe THA with an improved version of pseudo-differential structure, inspired by the design in [1], was reported in [2]. It achieves -52.4 dBc of total harmonic distortion (THD) at the sampling rate of 12.1 GS/s, and is the fastest 8-bit Si-based THA achieved to date. A 40 GS/s SiGe THA with a switched-emitter-follower (SEF) configuration and a low-noise input preamplifier was reported in [3], and [4] employed a 3-stage SEF architecture to realize a distributed SiGe THA that achieves the fastest sampling rate demonstrated to date, 50 GS/s.

In the present paper, an ultra-high-speed SiGe THA operating at a sampling rate of up to 40 GS/s is presented. Realized with a SEF structure and a fully-differential configuration, this THA employs the feedthrough attenuation network originally proposed in [5] to suppress the signal-dependent non-linear feedthrough interference. A modified version of the SEF design in [6] is used here to alleviate the interference affecting the input buffer's operation. A current-compensation circuit is also used in the THA's output buffer to mitigate the current leakage and improve the droop rate. This THA was fabricated in 130 nm, 200 GHz silicon-germanium (SiGe) heterojunction bipolar transistor (HBT) BiCMOS technology, as discussed in Section II. Section III describes the design of this SiGe THA, and measurement results of the THA are presented in Section III, followed by a summary.

TABLE I
Summary of the SiGe HBT Parameters.

$W_{E,eff}$	130 nm
Peak β	400
Peak f_T	200 GHz
Peak f_{max}	280 GHz
BV_{CEO}	1.7 V
BV_{CBO}	5.9 V

II. SiGe Technology

The SiGe HBT technology used for the present THA is a commercially-available 130 nm BiCMOS process [7], and features high-performance *npn* SiGe HBTs with a peak f_T / f_{MAX} of 200/280 GHz [7], ASIC compatible 1.3 V Si CMOS, and a full suite of passive elements, including metal-insulator-metal (MIM) capacitors and thin-film resistors. Five levels of full copper interconnects are available, along with two thick top layer aluminum metalization layers to enable high-Q inductors and robust transmission line designs. Typical SiGe HBT parameters are summarized in Table I.

III. THA Design

The traditional THA with a SEF configuration [8] has some drawbacks that affect the operation of the THA and degrade performance. One major limitation is the hold-mode feedthrough interference that causes large pedestal error in the voltages on the hold capacitors. This problem comes from the signal coupling from the input amplifier through the non-linear emitter-base junction capacitance of the bipolar transistor in the SEF. To suppress this

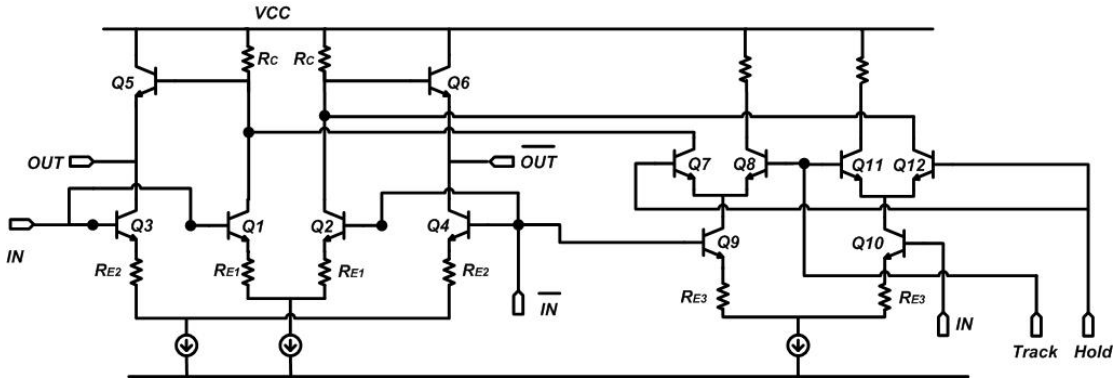

Fig. 2. Simplified schematic of the input buffer and feedthrough attenuation network.

feedthrough interference, a feedthrough attenuation network is introduced in the present THA, and the block diagram is shown in Figure 1. In track mode, the feedthrough

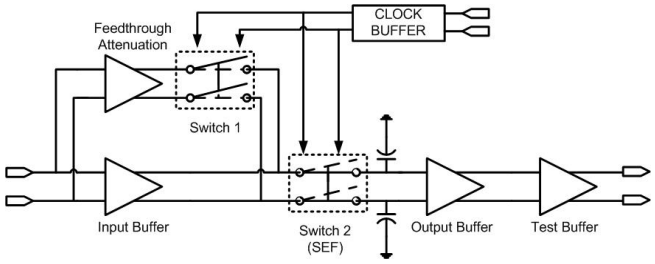

Fig. 1. The SiGe THA block diagram.

attenuation network doesn't function, as switch 1 is open. In the hold mode, however, switch 1 is closed and the output of the feedthrough attenuation network will be approximately out of phase with respect to that of the input buffer. As a result, the combined signal will be largely attenuated during the hold mode. The whole system employs a fully-differential configuration to mitigate common-mode noise and suppress even-order harmonics.

The simplified schematic of the input buffer and feedthrough attenuation network is shown in Figure 2. To achieve high linearity in the input buffer, emitter-degenerated differential pairs are used in the design of input buffer, with two transistors ($Q5$ and $Q6$) added to suppress the non-linearity caused by V_{BE} modulation.

The schematic of the SEF is shown in Figure 3. Compared with the conventional SEF design presented in [8], a resistor R_h and a transistor $Q14$ are added in the present SEF. By introducing an additional emitter-follower stage, the base voltage of $Q13$ will be clamped at a certain range instead of experiencing large voltage variations during the track and hold transition period, which can push the input buffer's differential pair into saturation during hold mode. The base voltage of $Q14$, acting as the main switch, will be decreased by a value of $-I_h{*}R_h$ in the track to hold-mode transition, and turning $Q14$ off.

The design of the output and test buffer is shown in Figure 4. Current compensation is provided to reduce the current leakage from the hold capacitors and hence decrease the droop rate.

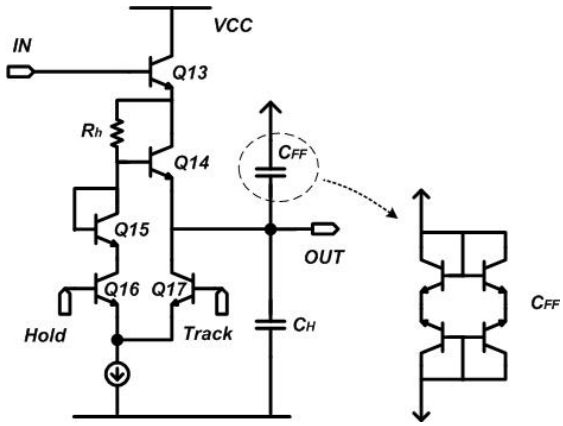

Fig. 3. Schematic of the THA's SEF.

IV. Measurement Results

The layout of the SiGe THA is strictly symmetrical to fully leverage the differential configuration. The THA chip has a die size of 1.8 × 1.0 mm^2 including bondpads and is shown in Figure 5. On-wafer measurements of the THA were performed using 40 GHz probes and cables. Hybrids were used to split the single-ended input signals into differential signals. A wideband oscilloscope, a spectrum analyzer, a PNA network analyzer, and two 50-GHz signal generators were used in the measurements.

Figure 6 shows the measured differential output waveform of the THA operating at the sampling rate of 40 GS/s, with a 6 GHz input frequency. The output spectrum with a sampling rate of 40 GS/s and a 10 GHz input frequency is shown in Figure 7. It can be seen from this figure that the second-order harmonic distortion is suppressed, which is a direct consequence of the fully differential design and symmetrical layout employed in the design. The measured THD is -32.4 dBc under these measurement conditions. The THD im-

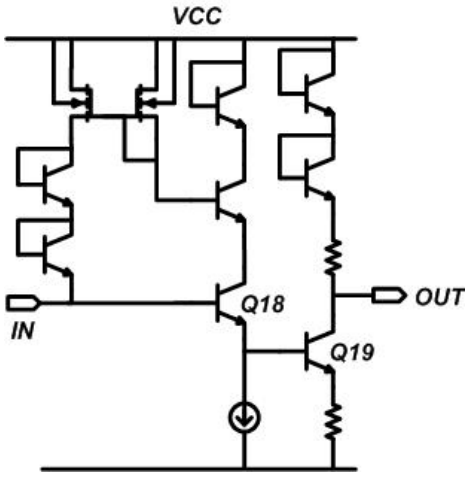

Fig. 4. Schematic of THA's output and test buffer.

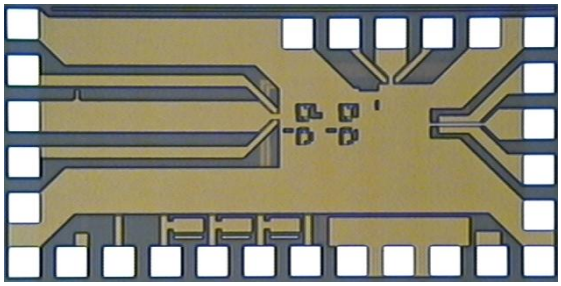

Fig. 5. Photo-micrograph of the SiGe THA.

proves to -44.2 dBc when the sampling rate is 18 GS/s and the input signal frequency is 3 GHz, and to -50.5 dBc under the condition of 12 GS/s and 2 GHz input signal. Figure 8 shows the THA's measured S11 and S21 in the track mode with the measurement performed in a single-ended configuration. The S21 is around -9 dB in the passband, including the signal loss from the single-ended measurements. The 3-dB bandwidth is tested to be around 16 GHz in the track mode. A two-tone test result is also shown in Figure 9, with an input power set to -4 dBm. The difference between the third-order intermodulation interference and fundamental signal is around 39.2 dB. We calculated the third-order input intercept point (IIP3) for these test results to be 15.6 dBm.

The measured results of this SiGe THA are summarized in Table II. A comparison has also been made between this SiGe THA and other THAs that can be found in the literature. The results are summarized in Table III. It can be seen that the present SiGe THA has a wide operational range, with comparable characteristics to other THAs operating in different conditions. Compared to the THAs published in the literature with the operational range from 10 GS/s to 20 GS/s, the present THA demonstrates a THD comparable to the best one achieved to date in Si technology, reported in [2], with much improved high-frequency characteristics. On the other hand, in the operational range of 30 GS/s and above, the present SiGe THA still exhibits robust characteristics compared to the fastest reported THAs in terms of linearity, power consumption, and sampling rate.

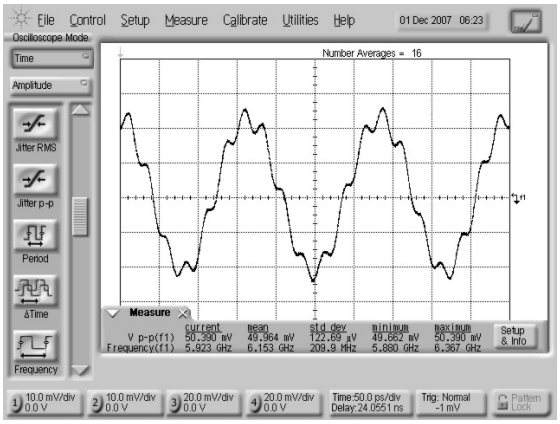

Fig. 6. Measured differential output with a 40 GS/s sampling rate and a 6 GHz 1.0 Vpp input.

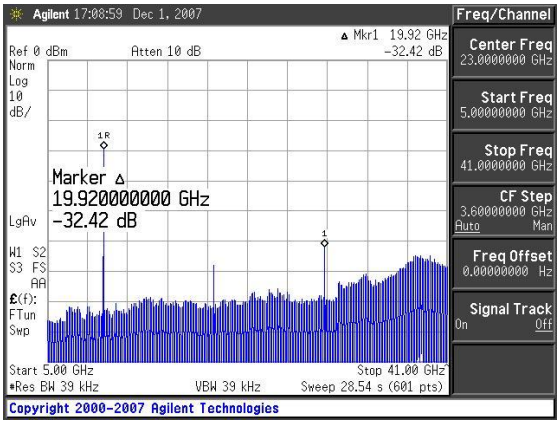

Fig. 7. Measured output spectrum with a sampling rate of 40 GS/s and a 10 GHz 1.0 Vpp input.

V. Summary

An ultra-high-speed SiGe THA with a fully differential configuration is reported. This SiGe THA can operate at a 40 GS/s sampling rate with -32.4 dBc of THD, and consumes 560 mW of power with a core area of 0.83 × 0.22 mm^2.

VI. Acknowledgment

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TABLE III
PERFORMANCE COMPARISON TO STATE-OF-THE-ART THAS OPERATING IN A SIMILAR FREQUENCY RANGE

Reference	Max. f_{sample} [GS/sec]	THD@f_{in}/f_{sample} [dBc @ GHz / GS/s]	Bandwidth [GHz]	Input	Power Supply [V]	P_{diss} [mW]	Process/f_T [–/GHz]
This work	40	-32.4 @ 10/40 -44.2 @ 3/18 -50.5 @ 2/12	16	1.0 Vpp	+5.5	560	SiGe/200
[2]	12.5	-52.4 @ 1.5/12.1 -49.5 @ 3.0/12.5	5.5	1.0 Vpp	+3.5	700	SiGe/200
[3]	40	-29 @ 10/40 -27 @ 19/40	43	-	+3.6	540	SiGe/160
[4]	50	-35 @ 40.001/40[1]	42	0 dBm	+4, +3	640	0.18-μm SiGe BiCMOS
[9]	12.001	-23.3 @ 12.001/12[1]	> 14	1.0 Vpp	-5.2	390	InP/120
[10]	30	-29 @ 7/30	7	-12 dBm	+1.8	270	0.13-μm CMOS
[11]	18	-32.3@ 2/18	7	1.0 Vpp	+3.5	128	SiGe/120
[12]	4	-30 @ 8/4	10	0.6 Vpp	+5.2	550	SiGe/45

[1]Measured results from the beat frequency test.

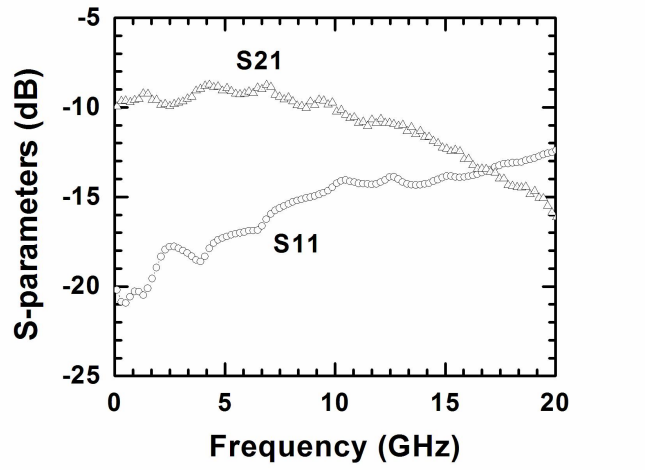

Fig. 8. Measured THA's S11 and S21 in the track mode.

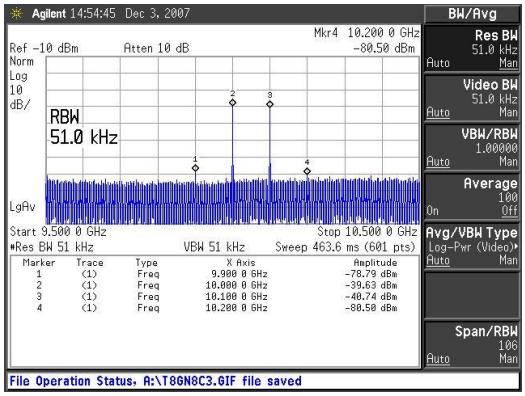

Fig. 9. Two-tone test at 10 GHz, with an input power of -4 dBm.

TABLE II
SUMMARY OF THE SIGE THA'S MEASURED PERFORMANCE.

Power Supply	+5.5 V
Power Consumption (Clock Excluded)	560 mW
Input Peak-to-Peak Voltage	1.0 V
Bandwidth in Track Mode	16 GHz
Differential Droop Rate	< 10 mV/nsec
THD@40 GS/sec f_{sample}, 10 GHz f_{in}	-32.4 dBc
@18 GS/sec f_{sample}, 3 GHz f_{in}	-44.2 dBc
@12 GS/sec f_{sample}, 2 GHz f_{in}	-50.5 dBc
Max. Sampling Rate	40 GS/sec

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