15th International Conference
MIXDES 2008
Poznań, POLAND
19 - 21 June 2008

A 9-BIT 1GS/S CMOS FOLDING ADC IMPLEMENTATION USING TIQ BASED FLASH ADC CORES

O. AYTAR[1], A. TANGEL[1], G. DUNDAR[2]
[1]KOCAELI UNIVERSITY, TURKEY
[2]BOGAZICI UNIVERSITY, TURKEY

KEYWORDS: CMOS flash ADC, Folding ADC, Threshold inverter quantizer

ABSTRACT: The purpose of this work is to employ the so-called Threshold Inverter Quantization (TIQ) technique in traditional CMOS folding ADC architectures. It also has a novel approach when multiplexing the appropriate folded signals into the fine flash part of the converter. The simulation results include 1MHz analogue input bandwidth, 1 Gs/s sampling rate using AMS-HIT KIT design library for 0.35µ H35B4 CMOS process model parameters. The analogue range is 1.7V, power supply is 3.3V, and maximum power consumption is 375mW. This paper also focuses on practical design considerations of the analogue pre-processing unit in folding ADCs.

INTRODUCTION

A/D converters are the basic components that translate the analog signals to the form that digital systems can understand. Most of the digital applications need these components.There are primarily four different high speed ADC architectures in the literature; the full-flash, the semi-flash, the pipeline, and the folding and interpolating ADCs. The fastest A/D converter type known in the literature is the Full-Flash architecture. However it is limited to lower resolution levels due to a large number of comparators (requiring 2n-1 comparators for an n-bit ADC). On the other hand, in a typical folding ADC architecture the number of comparators needed is reduced a lot when comparing with full-flash case without loosing the fully parallel nature [1].

In the literature, one can find an alternative way of analog part implementation to solve some of the flash ADC problems. This idea is called Threshold Inverter Quantization (TIQ) approach [2], [3], [4], [5], [6]. The main purpose of this study is to investigate whether or not possible to apply TIQ technique to a traditional folding scheme without using traditional resistive interpolation techniques. The AMS- HIT-Kit v3.72 for Cadence 5.1.41 design tool is used during design and simulation steps of this work.

IMPLEMENTATION OF THE TIQ BASED FLASH A/D CONVERTER

The idea behind the so called TIQ technique is to use the digital CMOS inverter as an internally-set analog voltage comparator. This eliminates the need for high-gain differential input voltage comparators that are inherently more complex and slower than the digital inverters [3]. As shown in fig. 1 where a specific TIQ sub-unit is magnified, replacing the analog part of the traditional flash architecture with TIQ block eliminates the need of reference voltages requiring a resistor ladder circuit as in traditional Flash ADC designs. Moreover, it allows a complete high-speed ADC to be implemented using the standard CMOS logic technology, making the featured ADC ideal for SoC implementations.

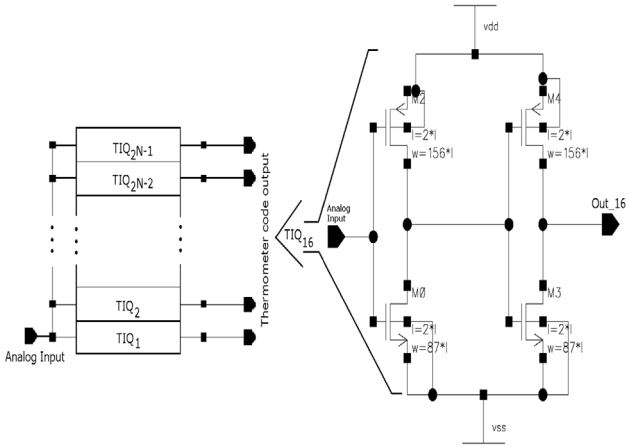

Fig. 1. TIQ Schematic

The large signal behaviour of the CMOS inverter must be investigated to understand the TIQ technique. The examination of fig. 2 at the Vin=Vout point can give a brief idea about the TIQ approach.

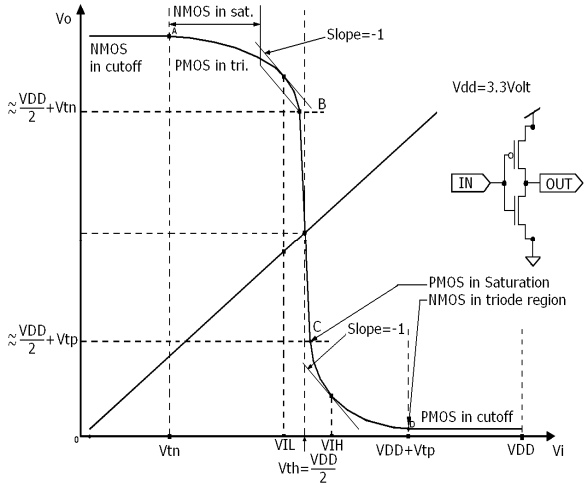

Fig. 2. Voltage transfer curve of a CMOS inverter

Two equations for a transistor in this figure can be written. One of the equations is for saturation region and the other one is for linear region operation of a transistor in the inverter. The mathematical expression of the threshold point of any quantizer sub-unit can be derived approximately as follows [7]:

For NMOS,

$$i_{DN} = k_n^{'}\left(\frac{W}{L}\right)\left[\left(v_I - V_{tm}\right)v_O - \frac{1}{2}v_O^2\right] \Rightarrow v_O \le v_I - V_{tm}$$

$$i_{DN} = \frac{1}{2}k_n^{'}\left(\frac{W}{L}\right)\left(v_I - V_{tm}\right)^2 \Rightarrow v_O \ge v_I - V_{tm}$$

For PMOS,

$$i_{DP} = k_p^{'}\left(\frac{W}{L}\right)\left[\left(V_{DD} - v_I - \left|V_{tp}\right|\right)\left(V_{DD} - v_O\right) - \frac{1}{2}\left(V_{DD} - v_O\right)^2\right] \Rightarrow v_O \ge v_I - V_{tp}$$

$$i_{DP} = \frac{1}{2}k_p^{'}\left(\frac{W}{L}\right)\left(V_{DD} - v_I - \left|V_{tp}\right|\right)^2 \Rightarrow v_O \le v_I - V_{tp}$$

For $i_{DN} = i_{DP}$,

$$\frac{1}{2}k_n^{'}\left(\frac{W}{L}\right)\left(v_I - V_{tm}\right)^2 = \frac{1}{2}k_p^{'}\left(\frac{W}{L}\right)\left(V_{DD} - v_I - \left|V_{tp}\right|\right)^2$$

$$Vth - Vtn = \left(\frac{\left(k_p^{'}\frac{W}{L}\right)_p}{\left(k_n^{'}\frac{W}{L}\right)_n}\right)^{1/2}\left(V_{DD} - Vth - \left|Vtp\right|\right)$$

$$\left(Vth - Vtn\right)\sqrt{\left(\frac{k_n^{'}}{2}\frac{W}{L}\right)_n} = \left(V_{DD} - Vth - \left|Vtp\right|\right)\sqrt{\left(\frac{k_p^{'}}{2}\frac{W}{L}\right)_p} \quad (1)$$

Let,
$$\left(\frac{\left(k_p^{'}\frac{W}{L}\right)_p}{\left(k_n^{'}\frac{W}{L}\right)_n}\right)^{1/2} = r \quad (2)$$

Substituting (1) in (2) above yields:

$$Vth\left(1 + r\right) = r\left(V_{DD} - \left|Vtp\right|\right) + Vtn$$

Finally,

$$Vth = \frac{r\left(V_{DD} - \left|Vtp\right|\right) + Vtn}{1 + r} \quad (3)$$

The final equation above shows the non-linear relationship between transistor aspect ratios and threshold voltage value of a CMOS inverter. In fact, The Cadence Analog Design Environment has been used for obtaining more accurate thresholding points using the BSIM3 transistor model parameters during the design process. As a result, a 4-bit and 5-bit TIQ based flash ADCs have been designed to use as the coarse flash part and the fine flash part of the 9-bit folding ADC, in this study. The flash core ADCs consist of a TIQ quantizer unit, a dynamic latch unit, a 1-of-N coder unit, and a PLA binary encoder unit as shown in fig. 3 for 4-bit case only.

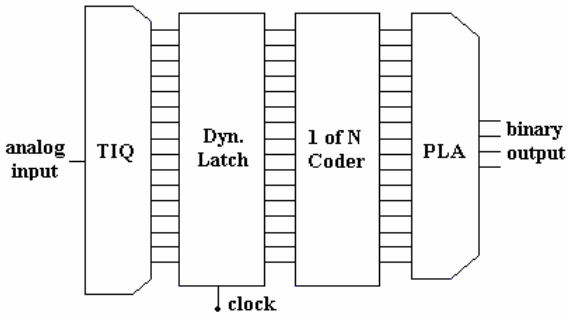

Fig. 3. TIQ based 4 bit flash ADC block diagram

FOLDING ADC IMPLEMENTATION

Today, the folding and interpolating technique is well established for use in high-speed ADC implementations. The advantage of a folding A/D converter is the reduced number of comparators compared to a full-flash converter. The result is a high speed, low power A/D with small die area [1]. A more detailed discussion of the folding and interpolating principle can be found in the literature [1], [8].

The proposed folding ADC consists of an analog pre-processing unit, a 4-bit TIQ based flash coarse ADC, a folder selector unit, which consists of the so-called OR-block and the SWITCH-block units, and a 5-bit TIQ based fine flash ADC unit as shown in fig. 4.

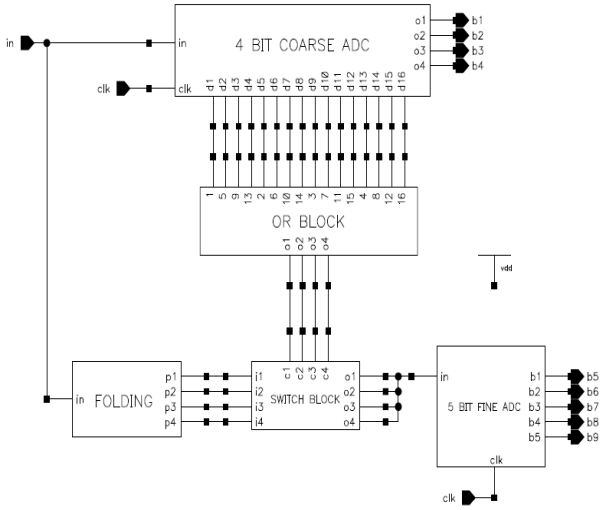

Fig 4. Block diagram of the folding ADC

The Analogue Pre-processing Unit

As shown in fig. 5, the analog pre-processing unit includes four folding unit to overcome the rounding problem of the folded analog input signals in the case of one folded signal is used for fine conversion. The so called double folding technique was one of the earlier methods of solving this problem addressed in the literature [1], [8].

Multiple folded signals are also common; therefore, in this study, folded signals are obtained by shifting the reference voltage levels from one folding circuit to another precisely. Hence, only the linear transition parts of the each folded signals are chosen and then multiplexed by the so called folder-selector circuit to the analog input of the fine ADC. Therefore, a more linear conversion can be obtained.

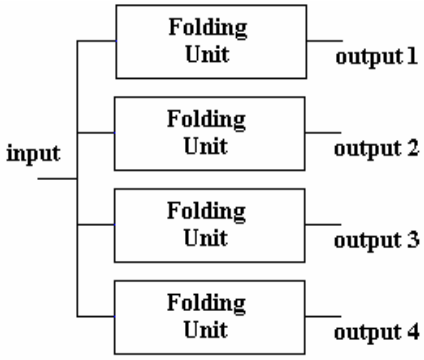

Fig 5. Block diagram of the analog preprocessing unit

Fig 6. Folding unit block diagram

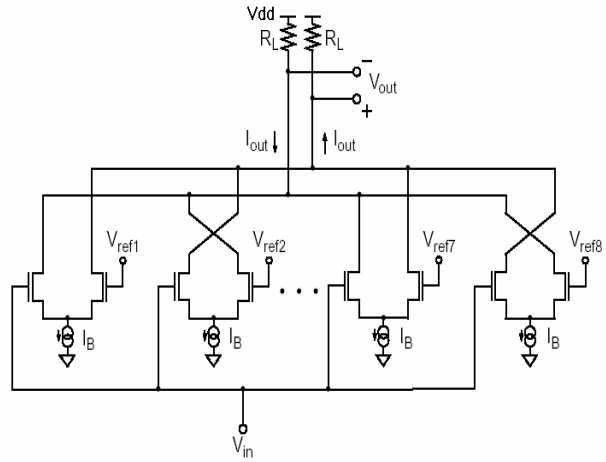

Fig 7. Folding Circuit

The folding unit consists of a CMOS folding circuit, a trans-resistance amplifier and differential amplifier stages for signal conditioning purpose as shown in fig. 6. Fig. 7 shows a CMOS folding circuit used in fig. 6 [1], [8]. Due to capacitive effects on the output nodes of the folding circuit, a dc level shifting is observed during transient analysis at high frequencies. To overcome this problem, a trans-resistance amplifier followed by a buffer is connected to the outputs of the each folding circuit as an interfacing buffer as was proposed in [1]. Hence, more suitable folded signals are obtained to be multiplexed in to the fine flash ADC input. The folding circuit output and the differential amplifier output signals are shown in fig. 8 and fig. 9, respectively. The corresponding trans-resistance amplifier circuit is shown in fig. 10

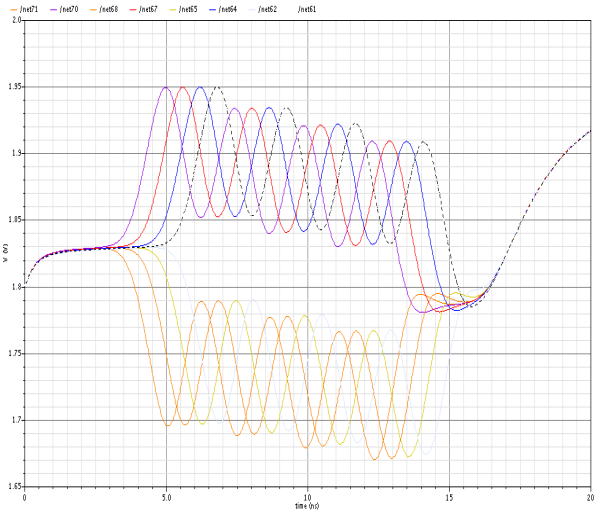

Fig 8. Folding circuit output for 50 MHz analogue input signal

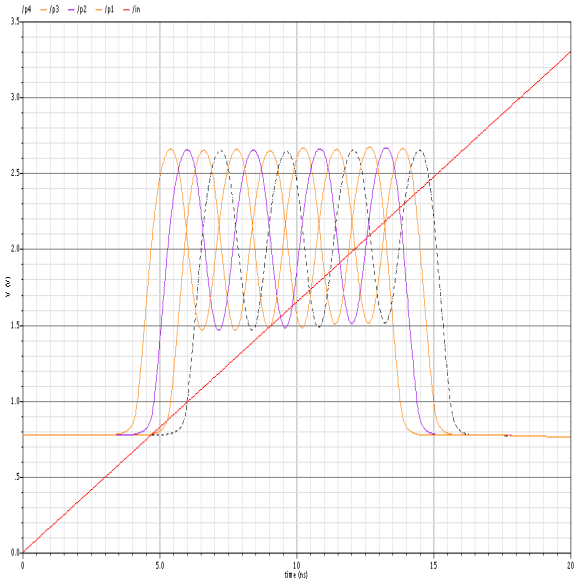

Fig 9. The conditioned signal after trans-resistance and differential amplifier circuitry

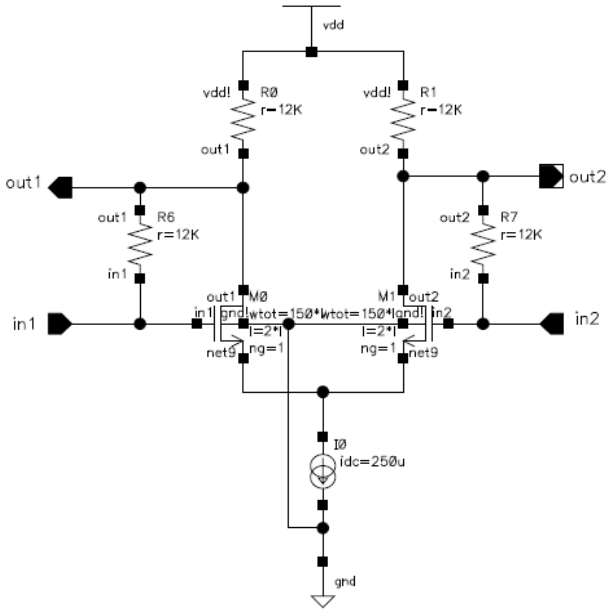

Fig 10. Trans-resistance amplifier

Folder Selector Unit

It consists of an OR-block, which is controlled by the selected TIQ outputs of the coarse ADC for timing the multiplexing operation of the folded signals, and a SWITCH-block to multiplex the selected linear parts of the each folded signal to the fine part of the ADC as depicted in fig. 11. This approach can also be considered as a novel approach in this study, although it has currently some delay problems, and bandwidth limit.

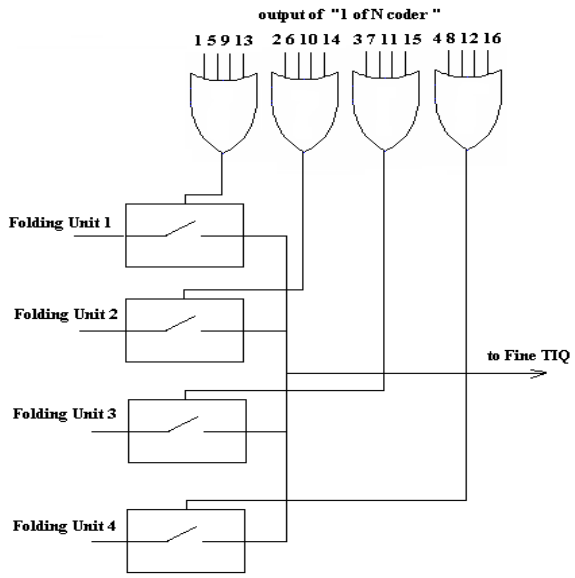

Fig 11. The schematic of the folder selector unit

Here, the OR block inputs are the selected output control signals of the 1-of-N coder. The transfer characteristics of the four folding units shown in fig. 9 are multiplexed to the fine ADC input by using analog switches, which are controlled by the OR-block outputs. Therefore, an appropriate zig-zag shape folded analog signal is obtained as shown in fig. 12.

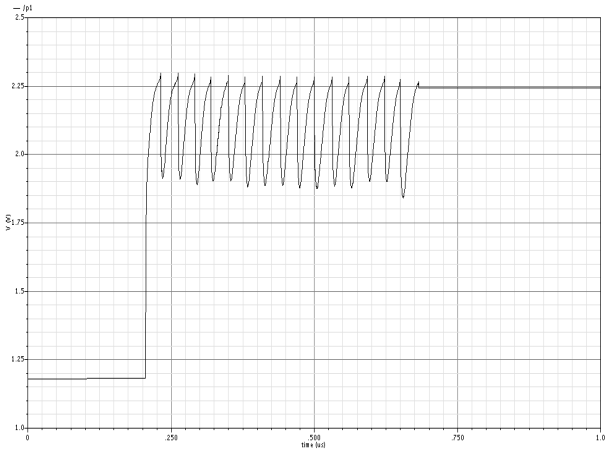

Fig 12. The obtained folded analog signal after conditioning and switching processes

Switch Circuit Performance

Especially, folding input-output characteristic implies that bandwidth of the signal at the output of folding circuit will be larger than that of the input. It can be shown that for an input frequency, the maximum instantaneous frequency at the output is

$$f_{out} = \sqrt{2}.F_f.f_{in} \quad (4)$$

where F_f is the folding factor[9].
The equation above shows for a folding factor of F_f=8, f_{in}=1MHz, output frequency approximately is 11.3MHz. Like any analog circuit designs, transistor sizing of switch circuit is very important. Therefore, Bandwidth-limit of the system is calculated and plotted by using Elmore-delay formula and Matlab. Fig 13 shows simple R-C model to get information about fine adc input signal's maximum frequency value.

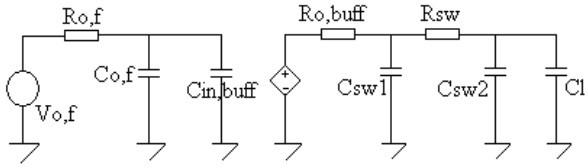

Fig 13. R-C model diagram

As shown in Fig 13, the R-C model consist of 4 stages. The first stage is folding circuit R-C model. Second stage is traditional CMOS unity gain buffer R-C model. The unity gain voltage buffer in the system has very low output resistance [10], [11]. Third stage is switch circuit R-C model and then the final stage is input capacitor of fine ADC.
$R_{o,f}$,output resistance of folding circuit. $C_{o,f}$, output capacitor of folding circuit. $C_{in,buff}$, input capacitor of voltage buffer. $R_{o,buff}$, output resistance of voltage buffer. C_{sw1}, input of switch circuit. C_{sw2}, output of switch circuit. R_{sw}, resistance of switch circuit.
According to fig 13, The mathematical expression of time constants are calculated by using Elmore-Delay formula [12] as follows:

$$\tau 1 = R_{o,f}(C_{o,f} + C_{in,buff})$$

$$\tau 2 = R_{o,buff}(C_{sw1} + C_{sw2} + C_1) + R_{sw}(C_{sw2} + C_1)$$

Resistance and capacitor value of the switch circuit is obtained by 0.35µ H35B4 CMOS process model parameters. The equations above are applied to MATLAB programs. Fig 14 shows system frequency with respect to variations of W/L for the switch circuit.

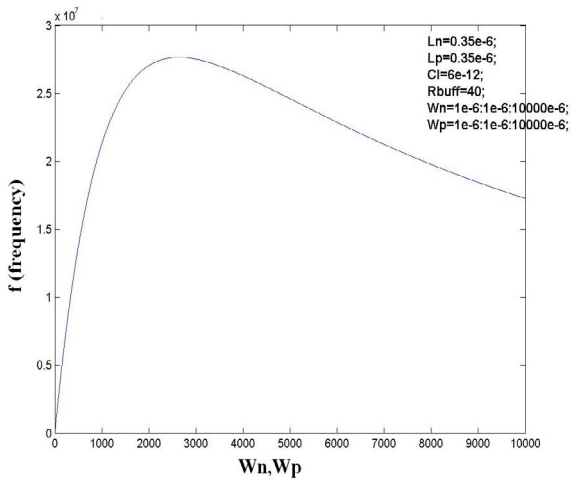

Fig 14. Frequency plot with respect to transistor sizes

As shown in fig 14, maximum system frequency is approximately 27 MHz so that maximum input frequency is 2.4 MHz. Fig. 14, clearly illustrate the system bandwidth limitation.

RESULTS AND FUTURE WORKS

A 9-bit folding ADC was realized in this study. TIQ based flash ADCs were used as the flash cores in implementation of the folding ADC, which was the improved version of [13]. Sampling rate was observed at 1 Gs/s with some missing codes on folder transition regions. Maximum analog input bandwidth is currently 2.4 MHz, but results are measured for 1 MHz. The AMS-HIT kit 0.35 micron CMOS process model parameters were used during the design and the simulations. Fig. 15 shows the 9-bit binary outputs for a ramp input signal in DC analysis. And fig 16 shows transient analysis for 1 MHz, 1 Gs/s Although, there are a few missing codes observed on AC simulation results given on Fig. 15, transient results, however, have shown some burst error codes on the fine ADC part on the locations where the folder transitions take place due to switching delays. It is concluded that the maximum input signal bandwidth attainable for this the system is 2 MHz although analog signal pre-processing unit works well up to 50 MHz level.

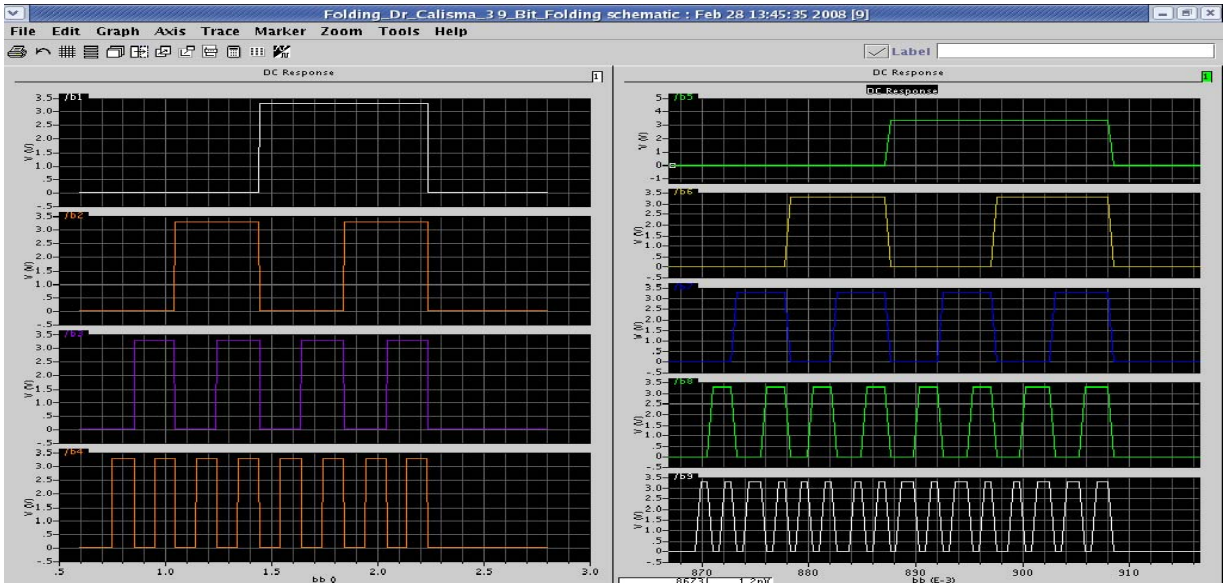

Fig 15. The TIQ based folding A/D converter binary outputs for a DC ramp input

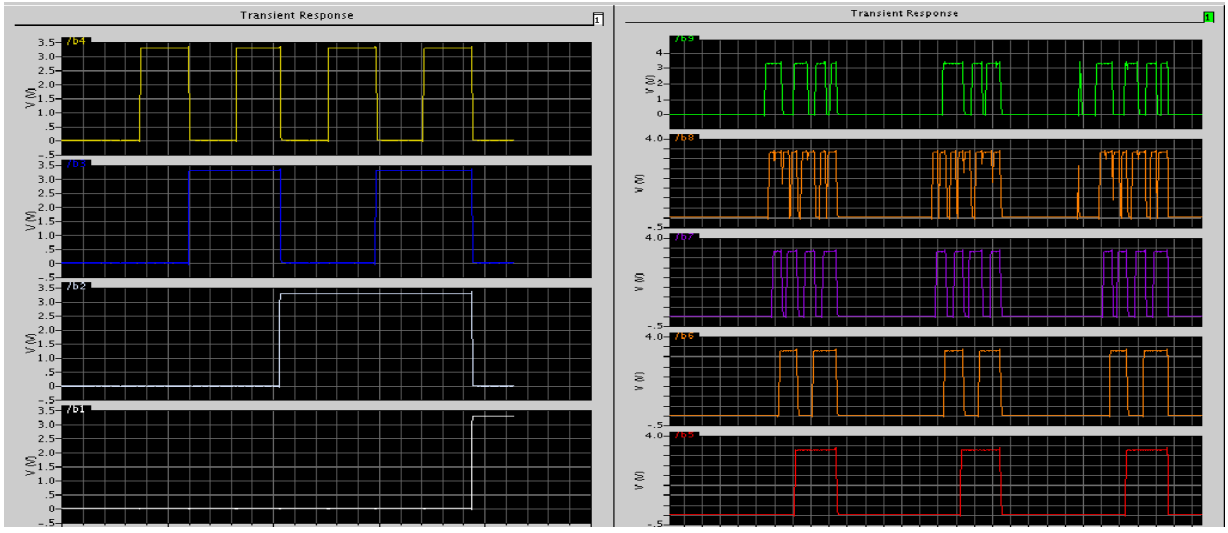

Fig 16. The TIQ based folding A/D converter binary outputs for 1 MHz, 1 Gs/s

THE AUTHORS

Oktay Aytar and Dr. Ali Tangel are with the Department of Electronics & Communication Engineering, Kocaeli University, Turkey. E-mail: oktay@kou.edu.tr
Gunhan Dundar is with the Department of Electrical and Electronics Engineering, Bogazici University, Istanbul, Turkey.

ACKNOWLEDGEMENTS

This work is financially supported by The Scientific Research and Grant Council of Kocaeli University under the contract number of BAP: 2007/42.

REFERENCES

[1] B. Nauta, A. G. W. Venes, " A 70 MS/s 100-mW 8-b CMOS Folding and Interpolating A/D converter" *IEEE Journal of Solid-State Circuits*, Vol. 30, pp. 1302-1308, Dec. 1995.

[2] A. Tangel, K. Choi, "The CMOS Inverter as a Comparator in ADC Designs", *Analog Integrated Circuits and Signal Processing*, Vol. 24,pp.147-155, May 2004.

[3] J. Yoo, K. Choi, and D. Lee, "Comparator Generation Selection for Highly Linear CMOS Flash Analog to Digital Converter", *Analog Integrated Circuits and Signal Processing*, Vol 35, pp. 179-187, 2003.

[4] J. Yoo, K. Choi, and A. Tangel, " 1-GSPS CMOS Flash Analog-to-Digital Converter for System-on-Chip Applications", *Proc. IEEE Computer Society Workshop on VLSI*, , pp.135-139, April 2001.

[5] J. Yoo, D. Lee, K. Choi and, A. Tangel, "Future Ready Ultrafast 8-bit CMOS ADC for System-on-Chip Applications" *14th Annual IEEE International ASIC/SOC Conference*, pp. 789-793, Sept. 2001.

[6] O. Aytar, A. Celebi, A. Tangel, and F. Tekin, "8-Bit 1Gs/s Flash ADC Based on Threshold Inverter Quantization Technique" *11th International Conference Mixed Design of Integrated Circuits and Systems*, pp. 121-124, June 2004.

[7] A. S. Sedra,, K. C. Smith, .Microelectronics Circuits. Oxford University Press, New York, 1998.

[8] M. P. Flynn, D. J. Allstot, "CMOS Folding A/D converters with current-mode interpolation", IEEE J. Solid-State Circuits,Vol. 31, pp. 1248-1256, 1996.

[9] S. Limotyrakis, K. Y. Nam and B. A. Wooley, "Analysis and Simulation of Distortion in Folding and Interpolation A/D Converters", IEEE Trans. on Circuits and Systems-II:Analog and Digital Signal Processing, Vol.39, No.3. pp. 161-169 March 2002.

[10] A.Torralba, R. G. Carvajal, M. Jimenez, F. Munoz, J. Ramirez-Angula, " New Low Voltage Class-AB CMOS Unity Gain Buffer and Current Mirror", XIX Conference on Design of Circuits and Integrated Systems, pp. 853-857, November, 2004.

[11] D.M.Monticelli, "A quad CMOS Single-Supply Opamp with Rail-to-Rail Output Stage", IEEE J.Solid-State Circuits, Vol.SC-21, pp.1026-1034, December 1986.

[12] J.P. Uyemura, " CMOS Logic Circuit Design", Kluwer Academic Publishers, 2001.

[13] M. F. Tekin, A. Tangel, O. Aytar, and A. Celebi," An 8-Bit CMOS Folding ADC Implementation Using TIQ Based ADC Core", MIXDES 2005, pp. 43-45, June 2005.