

A 10.3GS/s 6bit (5.1 ENOB at Nyquist) Time-Interleaved/Pipelined ADC Using Open-Loop Amplifiers and Digital Calibration in 90nm CMOS

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Abstract

A 10.3GS/s ADC with 5GHz input BW and 6 bit resolution in 90nm CMOS is presented. The architecture is based on an 8 way interleaved/ pipelined ADC using open-loop amplifiers and digital calibration. The measured performance is 5.8 ENOB (36.6dB SNDR) for a 100MHz input signal and 5.1 ENOB (32.4dB SNDR) for a 5GHz input (Nyquist) with phase offset correction across the interleaved array.

Introduction

10Gb/s transceivers for copper and optical fibers are experiencing a transition from analog to DSP based implementations [3] [4]. As an important example, Ethernet transceivers that incorporate electronic dispersion compensation (EDC) and operate over multimode fiber (MMF) links at 10.3Gb/s are moving to optimal maximum-likelihood sequence detection (MLSD) implementations. Because of the large amount of ISI introduced by modal dispersion, these transceivers require ADCs with ≥ 6 bit resolution.

Architecture

Fig. 1 shows the block diagram of the ADC. To increase resolution with moderate power dissipation, the circuit uses a pipelined architecture (1bit per stage) with open-loop amplifiers and digital calibration [1] [2]. Various trimming circuits are used to enhance yield over process. To achieve a BER $< 10^{-12}$ required by the application, each comparator requires a probability of a meta-stable event significantly lower than 10^{-12} , necessitating a comparator maximum clock rate of 1.5GHz. An 8 way interleaved ADC design is therefore used, comprising 8 channels clocked at 1.3GHz. Within each channel, the ADC circuit is replicated allowing continuous background calibration. Simulations show that, as a result of the variability of the MDAC gain, 10 pipelined stages are required to achieve 6 ENOB after calibration.

Circuit Implementation

Both the front-end T/H and the MDAC in each stage use open-loop amplifiers (see Fig. 3). The open-loop configuration trades stable gain and higher linearity for a higher BW at a given power consumption. Furthermore the short channel effect in the 90nm devices allows a relatively high linearity for open-loop amplifiers where the differential pair input is submitted to the full scale amplitude of the signal. In order to obtain sufficient settling speed for each MDAC, the BW of the open-loop amplifier is around 3GHz. The BW of each front-end T/H is higher than 5GHz to ensure that overall BW of the ADC is at least 5GHz. The main disadvantage of the open-loop amplifier is

the large gain variation over process and temperature. To alleviate this issue, a resistor trimming circuit controls the resistor absolute value accuracy within $\pm 3\%$.

The comparator is shown in Fig. 4. It includes a PMOS fully differential input pair and a cross-coupled NMOS pair to obtain the lowest regeneration time constant. Because of the high number of comparators used in each ADC channel, the device sizes have been scaled down to minimize power consumption, resulting in $< 1\text{mW}$ power dissipation per comparator. The resulting increase in input referred offset is corrected by an offset trimming circuit for each comparator. This circuit consists of a 4bit DAC controlled by a state machine as shown in Fig. 4. During the trimming phase, the inputs of the comparator are shorted. The state machine sweeps the DAC through the digital codes adding additional offset until the nominal offset of the comparator is cancelled.

The calibration is based on a reference provided by a 10bit DAC (Fig. 1). The DAC is clocked at 10MHz. The calibration results are stored in a lookup table. To obtain 6bit resolution on the calibrated result, a 10bit un-calibrated ADC output is required resulting in a 10-stage pipelined ADC design. Compensation of the DC offset and sampling phase and gain mismatch across the interleaved array are realized in the DSP using MIMO equalization techniques [4].

Measurement Results

The ADC is fabricated as part of a single-chip DSP based transceiver (Fig. 6). Fig. 5 shows the measured performance of the ADC from DC to 6.5GHz. For a 100MHz (DC) input signal the SNDR is 36.6dB which corresponds to an ENOB of 5.8. The SNDR at the Nyquist frequency of 5GHz is 25.3dB or 3.9 ENOB without phase offset correction and increases to 32.4dB or 5.1 ENOB with phase offset correction. The degradation at high frequency is essentially due to the aperture jitter of the T/H. The transceiver BER is below 10^{-12} which indicates a probability of meta-stable event in the comparators below 10^{-12} . The overall power consumption of the ADC including the digital calibration is about 1.6W. The feasibility of 10GS/s high resolution ADCs will enable widespread use of DSP based CMOS transceivers for very high speed applications such as optical communications [5] [6] [7].

References

- [1] D. Chang, G. Ahn and U. Moon, "Sub 1-V Design Techniques for High-Linearity Multistage/Pipelined Analog-to-Digital Converters," IEEE Transactions on Circuits and Systems, vol. 52, pp. 1-12, Jan., 2005.

- [2]C. Grace, P. J. Hurst, S. H. Lewis, "A 12b 80MS/s Pipelined ADC with Bootstrapped Digital Calibration," ISSCC Dig. Tech. Papers, pp. 460-461, Feb., 2004.
- [3]H. Bae, et al., "An MLSE Receiver for Electronic Dispersion Compensation of OC-192 Fiber Links," ISSCC Dig. Tech. Papers, pp. 234-235, Feb., 2006.
- [4]O. Agazzi, et al., "A 90nm CMOS DSP Maximum-Likelihood Sequence Detection Transceiver with Integrated AFE for Electronic Dispersion Compensation of Multimode Optical Fibers at 10Gb/s", to be presented in ISSCC 2008.
- [5]C. Paulus et al., "A 4GS/s 6b Flash ADC in 0.13 μ m CMOS," in Dig. Symp. VLSI Circuits, pp. 420-423, June, 2004.
- [6]K. Deguchi et al., "A 6-bit 3.5-GS/s 0.9-V 98mW Flash ADC in 90nm CMOS," in Dig. Symp. VLSI Circuits, pp. 64-65, June, 2007.
- [7]K. Poulton, et al., "A 20GS/s 8b ADC with a 1MB Memory in 0.18 μ m CMOS," ISSCC Dig. Tech. Papers, pp. 318-319, Feb., 2003.

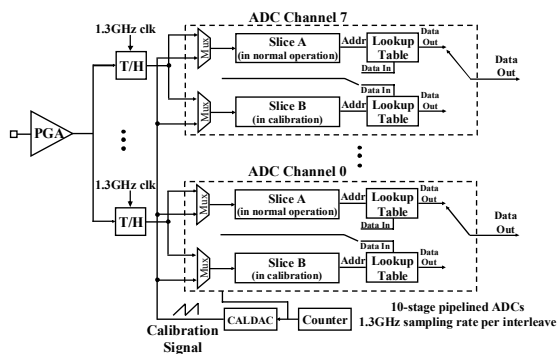


Fig. 1 Block diagram of the time-interleaved 10.3GS/s ADC with calibration DAC.

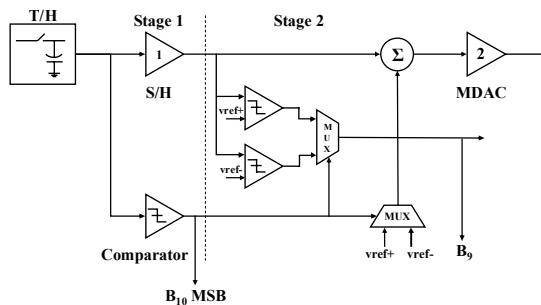


Fig. 2 Block diagram of the one bit look-ahead scheme.

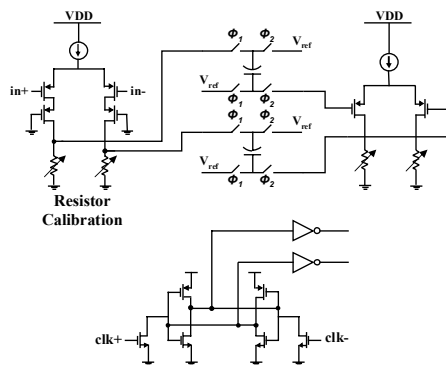


Fig. 3 Open-loop T/H-MDAC and non-overlapping clock generation circuits.

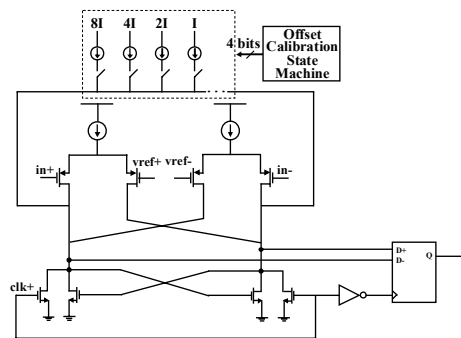


Fig. 4 Comparator schematic with digital offset calibration.

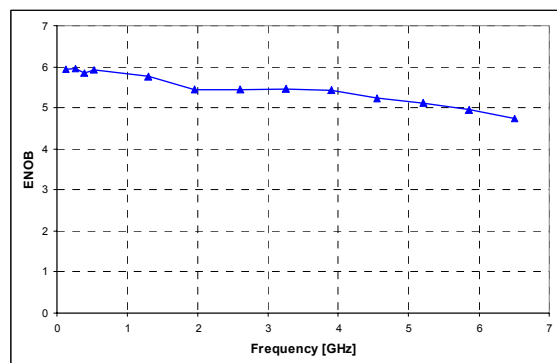


Fig. 5 Measured ENOB vs. frequency with phase offset and gain mismatch corrections.

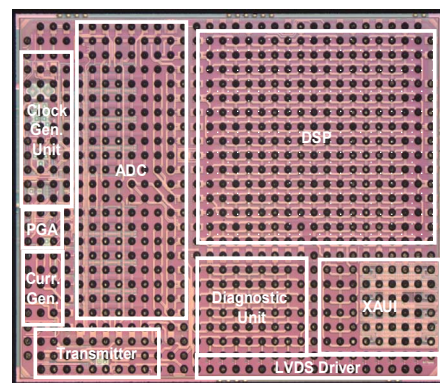


Fig. 6 Chip micrograph.

TABLE I: Performance Summary

Process	90nm CMOS
Sample Rate	Nominal: 10.3GS/s Maximum: 10.7GS/s
SNDR @ low frequency (100MHz)	36.6dB (5.8 ENOB)
SNDR @ Nyquist (5GHz) With P.O.C. (phase offset correction)	32.4dB (5.1 ENOB)
Prob. of meta-stable event	$< 10^{-12}$
INL/DNL (LSB)	0.27/0.21 (6bit)
Power	1.6W