Bulk Voltage Trimming Offset Calibration for High-Speed Flash ADCs

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***Abstract*—A bulk voltage trimming offset calibration technique is presented for flash analog-to-digital converters (ADCs). Offset calibration is achieved by digitally adjusting the bulk voltages of the preamplifier input devices. Without introducing additional capacitive loading in the analog path, this technique improves the accuracy of flash ADCs while not impairing their high-speed performance. A 4-bit ADC in 90-nm CMOS with the proposed technique achieves 3.71 effective number of bits (ENOB) at 5-GS/s sampling rate with 2.5-GHz effective resolution bandwidth (ERBW). The calibration generally improves ENOB by approximately 0.5 bit after calibration. The ADC consumes 86 mW at 5 GS/s with a 2.5-GHz input achieving a 1.32-pJ/convstep figure of merit. The ADC occupies 0.135-mm^2 chip area.**

***Index Terms*—Flash analog-to-digital converter (ADC), high-speed integrated circuits, offset calibration.**

I. Introduction

FLASH analog-to-digital converters (ADCs) offer the highest sampling rate without time interleaving compared with other architectures and have widely been used in applications requiring a high sampling rate, such as radio astronomy, optical communication, magnetic and optical read channels, and ultra-wideband wireless receivers. The performance of a flash ADC in CMOS is dominated by random offsets of comparators due to device mismatches [1], [2]. Various offset cancellation techniques were developed, for example, device sizing, offset averaging, autozeroing, calibrated redundancy, and comparator random chopping calibration. In recent years, digitally controlled trimming techniques have been developed [3]–[9]. In [3] and [4], a feedback loop detects the offset and then digitally adjusts the biasing current of each ADC comparator to cancel the offset. In [5], instead of applying a static correction using current sources, a dynamic correction with capacitors was used. In [6], a pair of calibration transistors in shunt with the comparator input transistors were used to adjust the comparator offset. The above methods can effectively compensate for large offsets of ADC comparators due to device mismatches; as a result, small and fast devices can be used in the comparator to save power and improve speed. However, those calibration devices can introduce additional capacitive loading to the high-speed analog signal path and degrade the high-speed performance for multi-gigasample-per-second flash ADCs [7], [8]. In [7]–[9], instead of trimming the comparator offset, the reference voltage was adjusted to compensate for the comparator offset. In [7] and [9], more resistors were used in the reference ladder to provide much finer resolution and a suitable reference level was then chosen for each comparator. In [8], a voltage-trimmable offset-canceling buffer is placed between each comparator and each resistor ladder reference to provide adjustable reference voltages.

In this brief, a new digitally controlled trimming offset calibration technique by modifying the bulk voltages of input differential pairs in preamplifiers is proposed to calibrate preamplifier and comparator offsets. In this technique, no additional transistor is added to the preamplifier and the comparator; the trim voltages are directly connected to the bulks of the transistors. Therefore, this technique does not introduce any additional capacitive loading in the analog signal path. In addition, the technique works with a standard resistor ladder. A 4-bit flash ADC with this technique was fabricated in 90-nm CMOS. The prototype achieves 3.71 effective number of bits (ENOB) at 5-GS/s sampling rate with 2.5-GHz effective resolution bandwidth (ERBW) after calibration, and the calculated figure of merit (FOM) is 1.32 pJ/convstep. Section II describes the ADC design with the proposed bulk voltage trimming offset calibration technique. Section III presents measurement results, followed by conclusion in Section IV.

II. Bulk Voltage Trimming Offset Calibration

To verify the proposed bulk voltage trimming offset calibration scheme, a 4-bit ADC is designed, as shown in Fig. 1. A preamplifier (A) and a three-stage comparator (C1, C2, and C3) are used for each path to reduce the probability of metastability. The outputs of SR latches are thermometer codes, which are converted to binary codes by a thermometer–gray-binary encoder. The encoder outputs are then decimated by a factor of 64 to facilitate the testing of the prototype. An offset calibration circuit (OSCAL) for each preamplifier detects and compensates offsets of the preamplifier and the comparator.

Fig. 2 shows the schematic of the preamplifier and the proposed offset calibration scheme. The preamplifier consists of two PMOS differential pairs with resistive loads. Since the threshold voltage V_t changes with the source bulk voltage $V_{\rm SB}$ and the drain current I_D changes with V_t, offset calibration is accomplished by modifying the bulk voltages of the input devices: LT for M1 and M2 and RT for M3 and M4. Using

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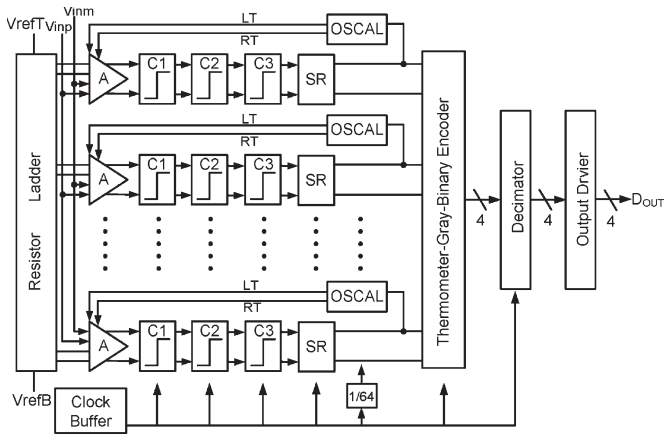

Fig. 1. Architecture of the ADC.

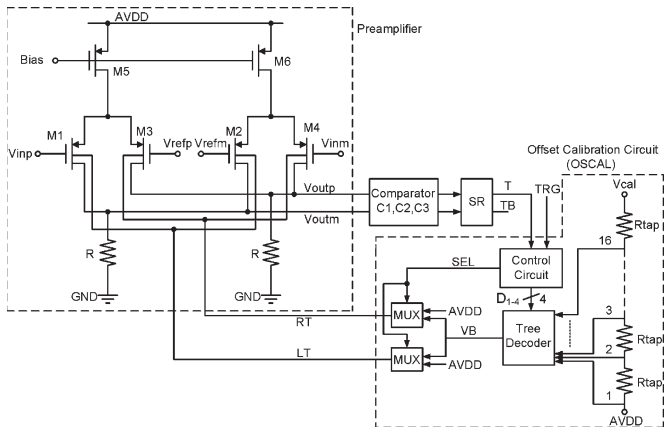

Fig. 2. Schematic of the preamplifier and the proposed bulk voltage trimming offset calibration scheme.

PMOS devices make it possible for M1 (M2) and M3 (M4) to be placed in different n-wells for adjusting their bulk voltages individually. To ensure the reverse-biasing condition in the source–bulk junctions, one of the bulk voltages will be fixed at AVDD, and the other will be raised above AVDD to increase the absolute threshold. A voltage higher than AVDD can generally be accommodated in current CMOS processes, in which multiple voltage supply levels are generally available. If NMOS devices are to be used, p-wells (or, equivalently, deep n-wells) are needed, as well as negative bulk voltages to ensure that the source bulk junctions are reversely biased. Since the offset is calibrated by adjusting the bulk voltages, there is no additional capacitive loading in the analog signal path. Therefore, the ADC high-speed performance is intact.

An OSCAL consists of a control circuit, a 4-bit resistor string digital-to analog converter (DAC) with a tree decoder, and multiplexers (MUXs). While each OSCAL has its own tree decoder, the resistor string is shared by all 15 OSCALs to minimize the die size. The power supply for most circuits is 1.2 V (AVDD), except for parts of the OSCAL circuits to provide voltages higher than AVDD for the bulk. Specifically, a 2.5-V supply is used for the tree decoder, MUXs, and digital output buffers for the signals SEL, and D_{1-4} and 2.5-V MOSFETs are used in these blocks.

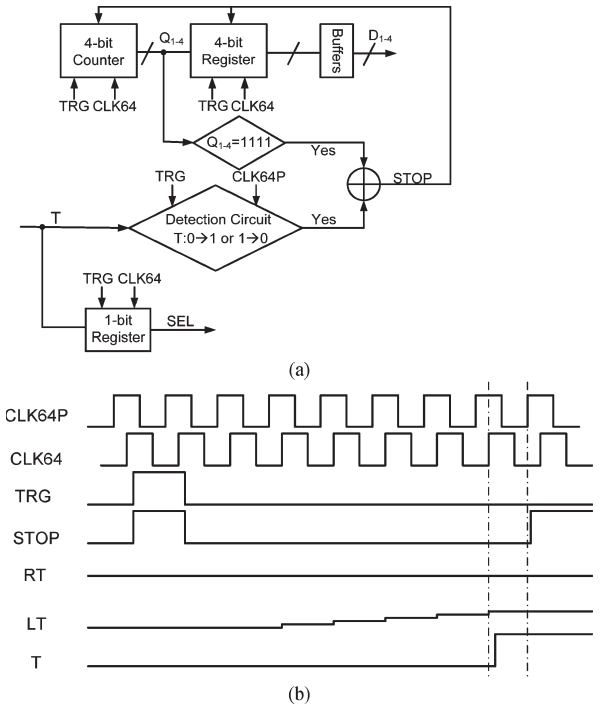

Fig. 3. (a) Control scheme. (b) Typical calibration timing diagram.

During calibration, all the inputs, i.e., Vinp, Vinm, Vrefp, and Vrefm, are fixed at the common-mode voltage level. As a result, the digital output of the SR latch after the comparator, i.e., T is determined only by the preamplifier and comparator offsets in each of the 15 paths. When $\mathrm{T} = 0$, left devices M1 and M2 need a higher absolute threshold voltage; thus, LT should be set to a higher voltage, i.e., VB, and RT should be set to the minimum bulk voltage, i.e., AVDD. For $\mathrm{T} = 1$, the situation is reversed. Based on the T value, the control circuit generates an SEL signal to control the MUXs to implement this logic. The higher bulk voltage VB is determined from a 4-bit digital code D_{1-4} controlling the DAC. The value of D_{1-4} is generated by the control circuit.

Fig. 3(a) shows the control scheme of the control circuit. The main blocks of the control circuit are a detection circuit, a 4-bit up counter, a 4-bit register, a 1-bit register, and digital output buffers. The control circuit uses a counter to generate D_{1-4}. When a trigger signal, i.e., TRG, is applied to the control circuit to initiate the calibration process, the counter starts to count up from 0, and the VB value increases from AVDD to modify the corresponding bulk voltage. The sampling rate of comparators is 6 GS/s, and OSCALs are clocked by CLK64 and CLK64P at 1/64 of the sampling frequency during calibration. Here, CLK64P leads CLK64 by 1/4 clock cycle. CLK64 is applied to the 1-bit register, the 4-bit counter, and the 4-bit register; CLK64P is applied to the detection circuit to detect the first occurring of $0 \rightarrow 1$ or $1 \rightarrow 0$ of the digital output T. When the T value flips from its initial value or when the counter has counted to 1111, the counter will stop, and its value is stored in the 4-bit register of the control circuit.

After the calibration initiates, the value of T is stored in the 1-bit register, and SEL is set to the stored value of T. For zero offset, because the digital output T dithers between 0 and

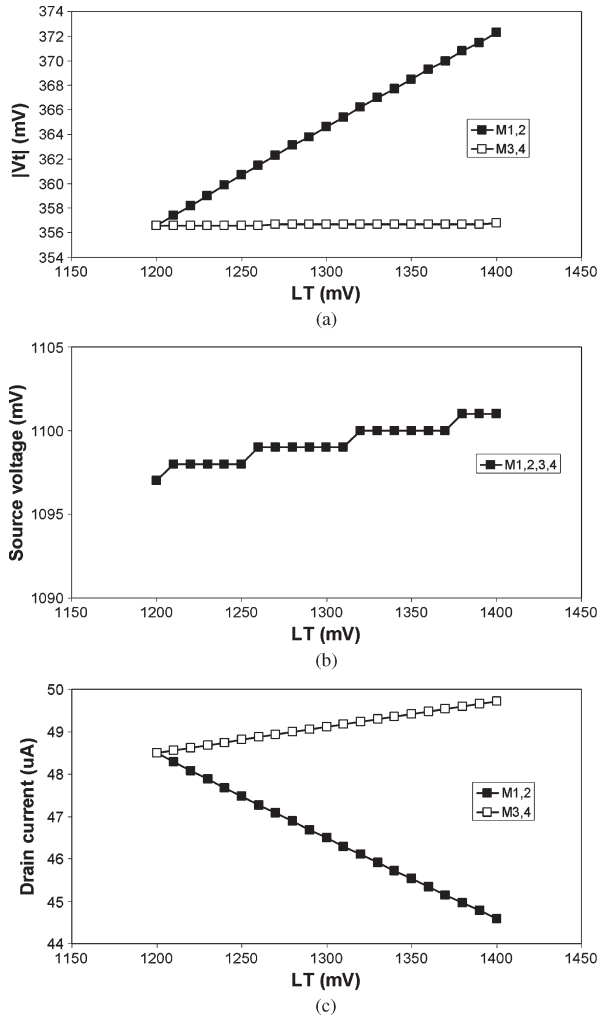

Fig. 4. Simulated (a) threshold voltage, (b) source voltage, and (c) drain current variations of the preamplifier input devices as a function of the bulk voltage LT.

1, a 0 or 1 is stored, and SEL can be 0 or 1. The detection circuit detects the first occurring of $0 \rightarrow 1$ or $1 \rightarrow 0$ when T is dithering between 0 and 1. Since the detection circuit is controlled by CLK64P, the counter is controlled by CLK64, and CLK64P leads CLK64, a STOP signal is generated to stop the counter before the counter counts up, and VB is not increased and stays at AVDD. Fig. 3(b) shows the timing diagram of CLK64P, CLK64, TRG, STOP, RT, LT, and T when LT should be set to a higher voltage. In this case, RT = AVDD, and LT = VB.

Fig. 4 illustrates how the threshold voltages, the source voltage, and the drain currents of the preamplifier input devices vary as a function of the bulk voltage LT, when all inputs are fixed at the common mode level and RT = AVDD. These are simulated results with no device mismatches in the preamplifier. The threshold voltage of a PMOS $|V_{t,p}|$ can be expressed as follows:

$$|V_{t,p}| = |V_{t0,p}| + |\gamma| \left(\sqrt{2\phi_f + |V_{\rm SB}|} - \sqrt{2\phi_f} \right) \qquad (1)$$

where $|V_{\rm SB}|$ is the bulk bias voltage applied between the source and the bulk, $|V_{t0,p}|$ is the threshold voltage with $|V_{\rm SB}| = 0$, ϕ_f is the Fermi level, and γ is the body-effect coefficient. Therefore, the threshold voltage of M1 and M2 increases with the bulk voltage LT, as shown in Fig. 4(a). Though the source voltage increases a little bit, i.e., about 4 mV, as shown in Fig. 4(b), as LT increases from 1.2 to 1.4 V, it is not as significant as the bulk voltage. As a result, the threshold voltage of M3 and M4 remains almost unchanged. The drain current of a PMOS in saturation can be expressed as follows:

$$I_{D,p} = \frac{1}{2}\mu_p C_{\rm ox} \frac{W}{L} \left(V_{\rm SG} - |V_{t,p}| \right)^2 \qquad (2)$$

where μ_p is the mobility of hole, $C_{\rm ox}$ is the gate oxide capacitance per unit area, W and L are the channel width and the length of the transistor, and $V_{\rm SG}$ is the source–gate voltage. For M1 and M2, the increment of $V_{\rm SG}$ is very small compared with that of $|V_{t,p}|$; as a result, the drain current of M1 and M2 mainly decreases with $|V_{t,p}|$. For M3 and M4, the $|V_{t,p}|$ term remains almost constant. However, the increment in $V_{\rm SG}$ due to the increment of the source voltage causes the drain current of M3 and M4 to increase. Since the source voltage does not increase as much as the threshold voltage of M1 and M2, the increment amount in the drain current of M3 and M4 is smaller than the decrement amount in the drain current of M1 and M2, as shown in Fig. 4(c). The dc output voltage $Voutm$ has the same tendency as the drain currents of M1 and M2, and the dc output voltage $Voutp$ has the same tendency as the drain currents of M3 and M4. The output offset of the preamplifier is $V_{\rm os,out} = Voutp - Voutm$. The input referred offset of the following comparator will be added to the output offset of the preamplifier. Therefore, the offset of the comparator is compensated at the output of the preamplifier by changing dc output voltages of the preamplifier through changing bulk voltages of input devices.

The drain current is not a linear function of the source–bulk voltage from (1) and (2). There are square-root terms of $|V_{\rm SB}|$ when (1) is put into (2). As a result, the dc output voltage of the preamplifier is not a linear function of the source bulk voltage. In addition, the DAC can experience nonlinearity due to random resistor mismatches of the resistor string. Therefore, the nonlinearity of the offset compensation is the combination of system nonlinearity of the bulk voltage trimming and nonlinearity of the DAC due to random mismatch. Since the offset compensation is nonlinear, the concept of offset calibration accuracy in terms of ADC LSB is, in fact, average accuracy. Therefore, Monte Carlo simulations are used to find the LSB size of the DAC in order to determine the offset calibration accuracy and range. To balance the tradeoff between circuit complexity and the offset calibration result, a 4-bit resolution is used in this design. If a large offset calibration range and high calibration accuracy are desired, a DAC with higher resolution can be used with increased circuit complexity. For a DAC of given resolution, a large size of LSB covers a large offset calibration range, while the calibration accuracy is low. A small size of LSB covers a small offset calibration range, while the calibration accuracy is high. Figs. 5 and 6 show Monte Carlo simulation results to find an optimum value for the DAC LSB size. Specifically, Fig. 5 shows the reduction of offset standard deviation after calibration, and Fig. 6 shows the ADC yield

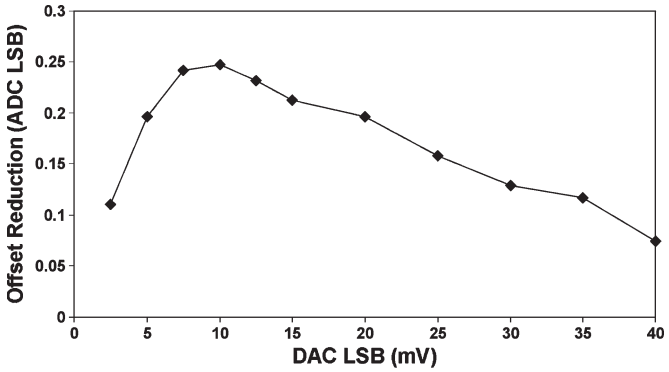

Fig. 5. Reduction of offset standard deviation after calibration as a function of the DAC LSB size.

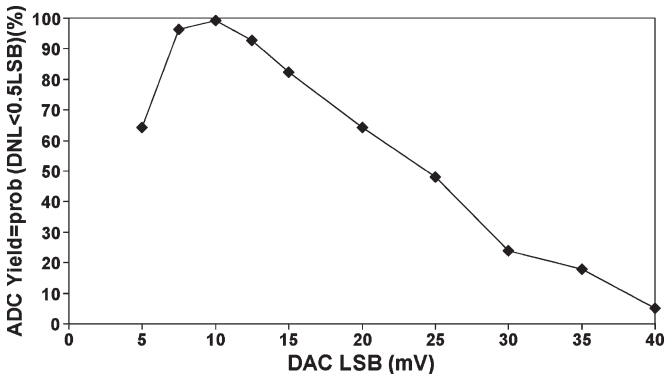

Fig. 6. ADC yield after calibration versus DAC LSB for the proposed scheme.

defined as DNL < 0.5 LSB as functions of the DAC LSB size. The simulations were run in the typical corner with mismatch analysis, and the number of runs is 50 for each DAC LSB size. The optimum calibration result is achieved when the DAC LSB is 10 mV, as used in this design. The total offset calibration range with four digital control bits is ± 0.67 LSB of the ADC. The corresponding offset calibration accuracy is 0.045 LSB of the ADC.

III. Measurement Results

The ADC is fabricated in 90-nm CMOS and packaged in a QFN56 plastic package. Fig. 7 shows the die micrograph. The active area of the ADC is 0.135 mm^2 including the resistor string and excluding output drivers. Fig. 8 shows the measured differential nonlinearity (DNL) and integral nonlinearity (INL) of the ADC for a 4-MHz input at 5-GS/s sampling rate. The measured DNL range was reduced from $-0.98 \sim 0.97$ LSB before calibration to $-0.33 \sim 0.43$ LSB after calibration. The measured INL range was reduced from $-0.87 \sim 0.71$ LSB before calibration to $-0.37 \sim 0.32$ LSB after calibration. This is over 0.5-bit improvement. Fig. 9 shows the measured signal-to-noise-plus-distortion ratio (SNDR) versus the sampling rate for an input signal of 100 MHz before and after calibration. The SNDR was about 21 dB before calibration and was above 24 dB after calibration. Therefore, there was approximately 3-dB improvement in SNDR or 0.5-bit improvement in ENOB after calibration.

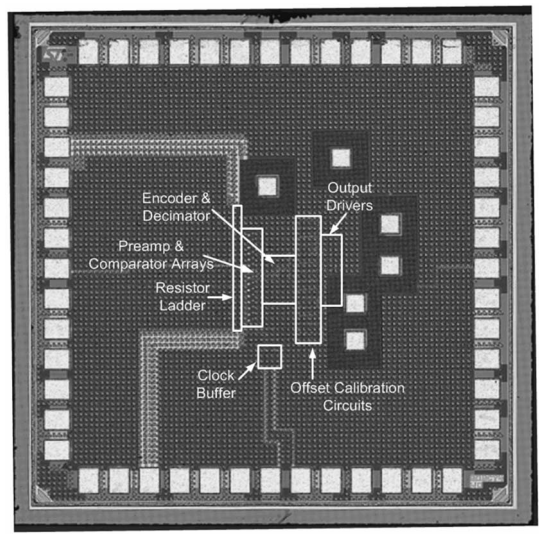

Fig. 7. Chip micrograph.

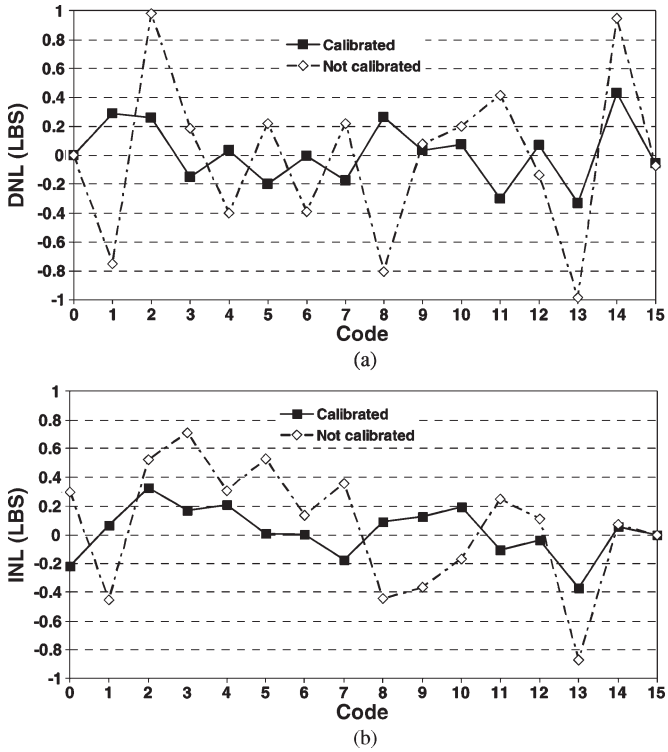

Fig. 8. Measured (a) DNL and (b) INL at 5 GS/s.

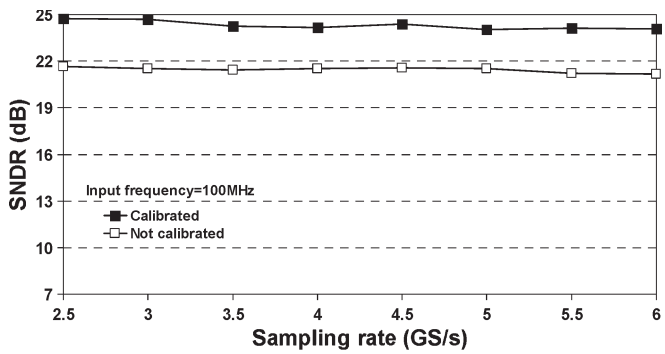

Fig. 9. Measured SNDR versus sampling rate for a 100-MHz input signal.

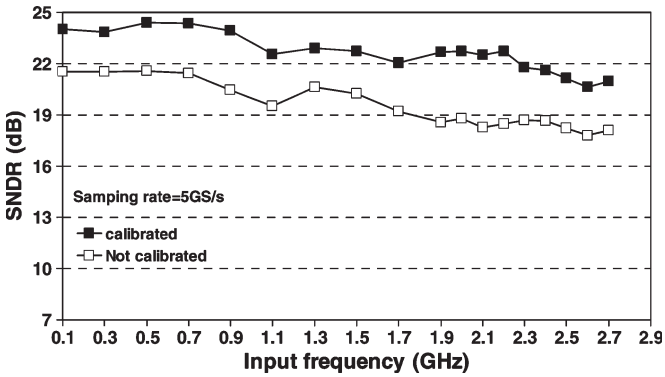

Fig. 10. Measured SNDR versus input signal frequency at 5 GS/s.

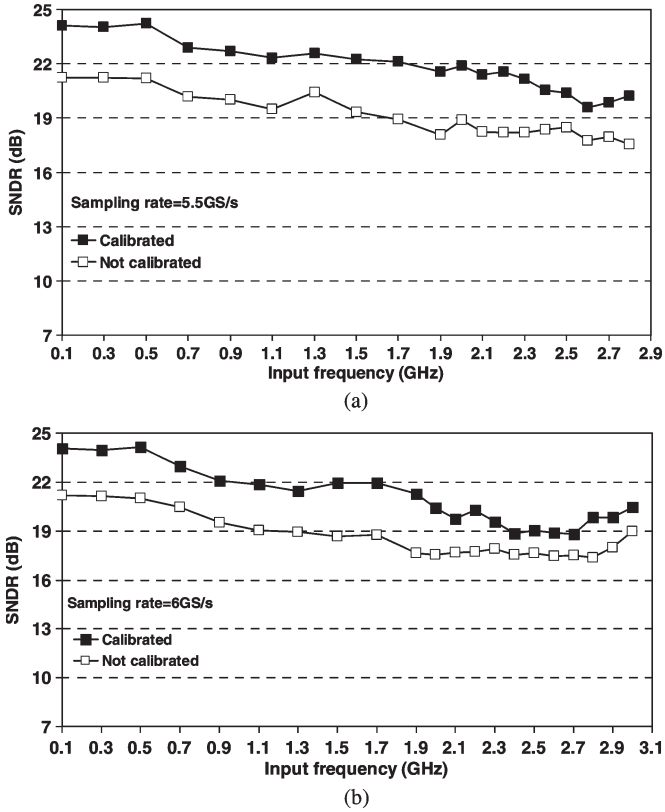

Fig. 11. Measured SNDR versus input signal frequency at (a) 5.5-GS/s and (b) 6-GS/s sampling rates.

Fig. 10 shows the measured SNDR versus the input signal frequency at 5-GS/s sampling rate before and after calibration. At 5 GS/s, the ENOB is 3.71 at low-frequency inputs and 3.22 ENOB at 2.5 GHz after calibration, i.e., the ERBW is above the Nyquist frequency. There is approximately a 3-dB or 0.5-bit improvement after calibration from low frequencies to the Nyquist frequency. Fig. 11 shows the measured SNDR versus the input signal frequency as the sampling rate is increased to 5.5 and 6 GS/s. The calibration is effective for these higher sampling frequencies. The power consumption is 86 mW at 5 GS/s, and the calculated FOM is 1.32 pJ/convstep. Table I summarizes the performance of the ADC at 5 GS/s and at higher sampling frequencies.

TABLE I
PERFORMANCE SUMMARY

Technology	90 nm CMOS
Resolution	4 bits
Sampling Rate	5 GS/s
Supply	1.2 V, 2.5 V (parts of the OSCAL)
Power	86 mW@f_s=5 GS/s, f_{in}=2.5 GHz
Input Range	0.4 $V_{pp\text{-}diff}$
DNL	-0.33~0.43 LSB (after calibration) -0.98~0.97 LSB (before calibration) @ f_s=5 GS/s, f_{in}=4MHz
INL	-0.37~0.32 LSB (after calibration) -0.87~0.71 LSB (before calibration) @ f_s=5 GS/s, f_{in}=4MHz
ENOB	3.71@f_s=5 GS/s, f_{in}=4 MHz 3.22@f_s=5 GS/s, f_{in}=2.5 GHz 3.71@f_s=5.5 GS/s, f_{in}=4 MHz 3.22@f_s=5.5 GS/s, f_{in}=2.3 GHz 3.75@f_s=6 GS/s, f_{in}=4 MHz 3.24@f_s=6 GS/s, f_{in}=1.9 GHz
FOM	1.32 pJ/convstep@5 GS/s 1.48 pJ/convstep@5.5 GS/s 1.77 pJ/convstep@6 GS/s
Active Area	0.135 mm^2 (260 µm×520 µm) (incl. res. ladder)
Input Capacitance	360 fF
Package	QFN56

IV. CONCLUSION

This brief has presented a digitally controlled bulk voltage trimming offset calibration technique for compensating preamplifier and comparator offsets in flash ADCs. It calibrates offset by adjusting bulk voltages of the ADC preamplifier input pair and avoids introducing additional capacitive loading by calibration devices to improve ADC speed. A 4-bit flash ADC in 90-nm CMOS with this calibration technique has achieved 3.71 ENOB at 5-GS/s sampling rate with 2.5-GHz ERBW and a 1.32-pJ/convstep FOM. The offset calibration improves the DNL, INL, and ENOB (SNDR) of the ADC by approximately 0.5 bit after calibration.

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