A 2.6 mW 6 bit 2.2 GS/s Fully Dynamic Pipeline ADC in 40 nm Digital CMOS

Bob Verbruggen, *Member, IEEE*, Jan Craninckx, *Member, IEEE*, Maarten Kuijk, *Member, IEEE*, Piet Wambacq, *Member, IEEE*, and Geert Van der Plas, *Member, IEEE*

***Abstract*—A 2.2 GS/s 4×-interleaved 6b ADC in 40 nm digital CMOS is presented. Each ADC slice consists of a 1b folding stage followed by a pipelined binary-search sub-ADC using dynamic nonlinear amplifiers for low power consumption and high speed. The folding stage samples the input, removes its common-mode component and rectifies the differential voltage. The pipelined binary-search sub-ADC leverages threshold calibration to correct for amplifier and comparator imperfections, which allows the use of inherently nonlinear dynamic amplifiers. The prototype achieves 31.6 dB SNDR at 2.2 GS/s with a 2 GHz ERBW for 2.6 mW power consumption in an area of 0.03 mm^2.**

***Index Terms*—Analog-digital conversion, calibration, CMOS analog integrated circuits.**

I. Introduction

COMMUNICATION in the unlicensed frequency band around 60 GHz requires a very fast ADC with low resolution. Pipeline converters have not been used often at these low resolutions and high speeds, because of the power required for processing the signals with sufficient speed. At these low resolutions simpler architectures such as flash or SAR are dominant because the speed advantage of pipeline over SAR converters is small, while the power advantage over flash converters is small or non-existent. Pipelined converters are used most often when high performance is required. They can attain resolutions well over 10 bits at speeds of a few hundred megasamples per second [1]–[3].

The speed of pipeline converters is typically limited by the OPAMPs used to generate and amplify the residues. The required amount of OPAMP settling depends on the desired SNDR, but fast settling OPAMPs often consume significant power. In [4], reference voltage calibration and look-ahead pipelined stages are used to deal with incomplete OPAMP settling which enables a resolution of 5 bits at a speed of 1200 MS/s for approximately 75 mW in 0.13 μm CMOS. In [5] a conversion speed of 500 MS/s with 9 ENOB is attained for 55 mW in a 90 nm CMOS technology by using a high speed OPAMP and correcting its non-idealities digitally after calibration. In addition to limiting the speed, the OPAMPs typically dominate the power consumption. Research efforts have been made to remove OPAMPs from pipelined converters, mostly motivated by degraded OPAMP performance in scaled technologies or their high power consumption. In [6] a charge-domain pipeline converter is proposed, in [7] OPAMPs are replaced by dynamic source follower-based amplifiers while in [8] comparator-based instead of OPAMP-based switched capacitor circuits are used. In all these approaches, the goal is still to provide linear residue generation and amplification throughout the pipeline; none of them are particularly well-suited for high speed converters.

Another interesting research topic is the use of calibration in pipelined converters [5], [7], [9], [10]. In most cases the pipeline stages bit outputs are digitally corrected, in some cases however, the analog operation is adapted to correct for errors: in [11] the gain of an amplifier is adjusted. Threshold calibration, where each ADC threshold is adjusted to its desired value, is typically avoided because the exponential dependence of calibration effort on resolution.

In this work both of these research topics are explored and a calibrated high speed, low resolution pipeline converter without OPAMPs is proposed. A prototype ADC which leverages this architecture will be described in Section II. Section III describes its charge-sharing folding front-end which removes the common-mode input component. In Section IV, the design of the pipelined binary search (PLBS) sub-converter and its flash back-end will be explained. Section V describes the implementation of low timing skew interleaved sampling while Section VI details the procedure used to calibrate the prototype. In Section VII the measurement results are shown. Finally, conclusions are drawn.

II. Architecture

The proposed ADC architecture consists of four identical interleaved channels. Each channel uses a 1-bit charge-sharing folding front-end, 3 bits of PLBS conversion and a 2-bit flash back-end, as shown in Fig. 1. The folding stage samples the input voltage, removes its common-mode component and rectifies the differential signal while determining the MSB of the converter. The magnitude of the rectified signal is the input of three stages of PLBS conversion which provide 3-bit quantization and generate a residue on one of four outputs. This residue is then further quantized by one of eight 2-bit flash converters, only one of which is activated each cycle, depending on the digital outputs of the PLBS stages. This results in a nominal 6-bit resolution. Clocking and the combination of the different channel

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B. Verbruggen is with SSET/WL IMEC, B-3001 Leuven, Belgium. He is also with the Vrije Universiteit Brussel, Department ETRO, Belgium (e-mail: vbruggen@imec.be).

J. Craninckx, P. Wambacq, and G. Van der Plas are with IMEC, B-3001 Leuven, Belgium.

M. Kuijk is with the Vrije Universiteit Brussel, Department ETRO, Belgium.

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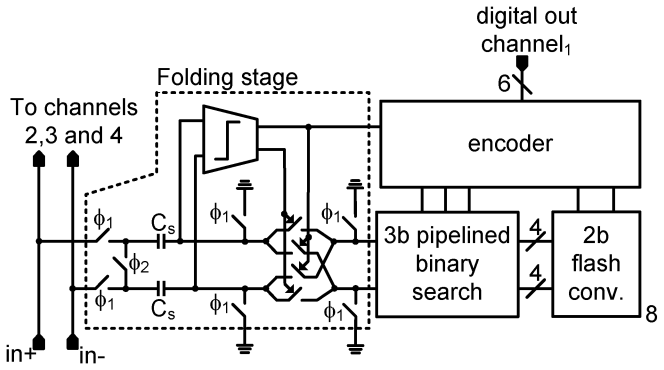

Fig. 1. Architecture of one channel of the four-way interleaved ADC.

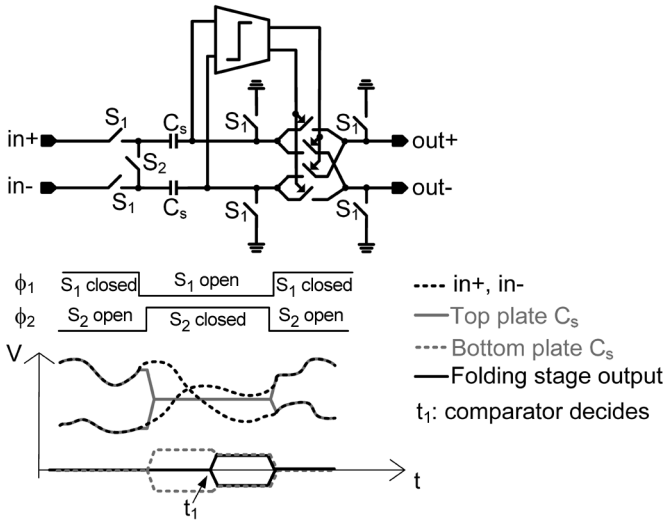

Fig. 2. Common-mode insensitive folding stage (top) and its waveforms (bottom). Common-mode charge injection not shown.

outputs are not shown in Fig. 1 for simplicity, but also implemented. As timing skew between the four channels is reduced to acceptable levels by design, no front-end sample-and-hold or timing calibration is required.

At the core of this design is the PLBS sub-converter. It enables low power quantization at high speed with low input capacitance. This architecture was inspired by the comparator-based asynchronous binary search (CABS) converter of [12]. In [12] an efficient 6-bit ADC is realized that has 63 dynamic comparators with different thresholds but clocks only six of them. The conversion speed is limited as the six comparisons occur successively in the same clock phase. In the technique proposed here, pipelining is used to increase the speed but of course amplifiers are required. Instead of spending power to ensure the linearity of these amplifiers, linearity requirements are avoided by activating a different dynamic comparator for each ADC threshold and calibrating the corresponding comparator threshold to a desired input-referred value, canceling errors both from nonlinear signal processing and offsets in the comparators. As in [12], only a subset of the comparator tree is activated, based on the decisions of previous pipeline stages. However, as each ADC threshold is calibrated, the calibration effort exponentially increases with resolution. This is not an issue if the resolution is kept fairly low. The folding front-end halves the required calibration effort and reduces the influence of the common-mode input voltage on this calibration. In the following sections, the building blocks of this architecture are discussed in greater detail.

III. Common-Mode Insensitive Charge-Sharing Folding Stage

Fig. 2 shows a simplified schematic of the folding front-end and its waveforms. This is a modified version of the charge-sharing folding front-end used in [13]: in addition to sampling and rectifying the input signal it also removes its common-mode component as in [14]. When the S1 switches are closed the input voltages are tracked across C_s. At a falling φ_1 edge the charges on C_s are fixed. Their bottom plates are at ground and the top plates at their sampled input voltage, neglecting charge injection. Closing S2 shorts the top plates and generates the differential voltage at the bottom plates with some loss due to stray capacitance. The folding stage comparator is then activated, and based on its decision closes one set of switches in the chopper (at t_1), sharing the charge on the bottom plates with the next stage, with some more signal loss due to stray and load capacitance. Due to the closing of the appropriate set of chopper switches, the differential output voltage always has the same sign.

In the implemented circuit, common-mode charge Q_{CM} is added to the C_s bottom plates through charge redistribution. This ensures that the bottom plate voltages do not go below the ground potential, and is not shown in Fig. 2. The common-mode output is therefore independent of the common-mode input which fixes the common-mode voltage for the ADC back-end and significantly improves the common-mode input range. Moreover, the applied common-mode voltage may differ in calibration and normal operation.

The charge-sharing folding operation causes small-signal loss which must be limited to ensure sufficient SNR. Indeed, given top and bottom plate parasitics of C_t and C_b respectively, and an output load of C_L the small-signal gain corresponds to $C_S/(C_S + C_b + C_L)$. The sampling capacitance must therefore be sufficiently large compared to the bottom plate parasitics and the load capacitance to ensure the small-signal loss is limited. The low input capacitance of the PLBS sub-converter allows the use of a sampling capacitance of only 40 fF while achieving an acceptable folding gain of approximately 0.6. Due to parasitics of roughly 10 fF at the top plates of C_s the total input capacitance is 50 fF per channel.

For the folding stage to function correctly, equal magnitude but opposite sign input signals must generate the same output. Any asymmetry cannot be corrected by calibration and is therefore to be avoided. We will show that this imposes some requirements for the matching of C_b and C_t but mismatch of C_L is not an issue. To this end we will consider the question of what will happen to the folding stage output when the polarity of its input voltage is reversed. Since in practical cases C_s is the largest capacitance in this circuit, it is assumed that the C_s capacitances match sufficiently. The mismatch spread of the implemented C_s capacitances is well below the roughly 1% error allowed in this 6-bit design.

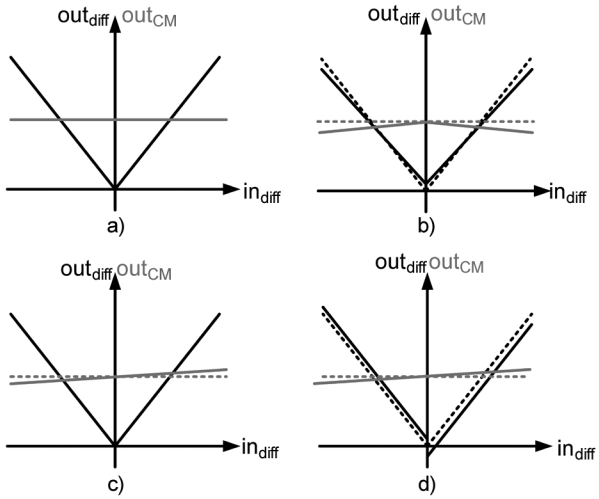

Fig. 3. Simplified input-output characteristics for the folding stage in the ideal case (a), with load mismatch (b), top plate mismatch (c) and bottom plate mismatch (d). Ideal curves shown in dashed lines.

We will first show that load capacitance mismatch does not introduce asymmetry in the input-output characteristic. Let us assume that due to mismatch the load capacitance on the positive output of the folding stage is too large and a positive input voltage is applied. Due to a positive sign comparator decision, the bottom plate of the lower sampling capacitance in Fig. 2 is connected to the positive output. Since the folding stage processes charge, this would lead to a reduced voltage on the positive output node when compared to a nominal case without mismatch. However, when the input voltage polarity is reversed and a negative voltage is applied, the sign comparator decision changes and a different set of folding switches closes. This new set of folding switches now connects the bottom plate of the top sampling capacitance of Fig. 2 to the positive folding stage output. Again, due to charge-domain processing, the voltage on the positive output node is reduced with respect to the nominal case. Consequently, for both the positive and negative inputs, the load capacitance mismatch leads to the same deviation from the nominal case and introduces no asymmetry, as shown in Fig. 3(b).

We will now discuss the effect of top plate capacitance mismatch, as shown in Fig. 3(c). When the positive top plate stray capacitance is larger than the negative one, there will be more charge on the positive input than the negative one. When the two top plates are shorted the voltage of the positive top plate will change less and that of the negative top plate will change more. The final voltage at the shorted top plates is consequently dependent on the input voltage, and as a result, the common-mode voltage at the bottom plates is similarly affected. However, if the bottom plates are matched, the final differential voltage at the bottom plates is not affected by top plate capacitance mismatch since the sum of the voltage changes of the positive and negative top plates still equals exactly the input voltage, reduced by the small-signal gain. An acceptable common-mode asymmetry of 6 mV is obtained for 2 fF top plate parasitic mismatch, which can be ensured by design.

Finally, we will discuss the effect of bottom plate capacitance mismatch, as shown in Fig. 3(d). The charge added to both bottom plates shifts their common-mode voltage up, but if there is mismatch on the bottom plate capacitance, it will also generate a differential error voltage on these bottom plates. This differential error voltage is independent of the applied input voltage but the polarity with which it is passed to the output depends on the sign of the input voltage. The error on the output differential voltage therefore changes sign when the input does, and leads to differential asymmetry, which cannot be corrected using threshold calibration of the sub-converter. Bottom plate mismatch also results in asymmetric small signal gains. It can be intuitively seen that this is negligible by looking at the expression of the small signal gain, $\mathrm{C_S}/(\mathrm{C_S}+\mathrm{C_b}+\mathrm{C_L})$: small errors in $\mathrm{C_b}$ are lumped into the sum with $\mathrm{C_s}$ and $\mathrm{C_L}$, and therefore only have a negligible effect on the gain. The same unequal gain results in a negligible quantity of common-mode asymmetry. The main cause of asymmetry is due to the charge redistribution which sets the output common-mode and is an offset rather than a gain error.

To reduce this asymmetry error below 0.5 LSB would require a matching error of less than 0.3 fF, which would be extremely challenging to achieve by design. Instead of attempting this, the bottom plate capacitance is calibrated. By placing finely tunable capacitance on both bottom plate nodes the bottom plate mismatch is simply reduced to acceptable levels during start-up calibration, which is described in Section V. Conveniently, this calibration also corrects for any mismatch in the charge injection of the bottom plate S1 switches.

IV. The PLBS Sub-Converter

A block diagram of the implemented pipelined binary search (PLBS) converter is shown in Fig. 4, with grayed-out units inactive for an example conversion. The lack of linearity requirements allows the use of a novel dynamic amplifier which is merged with a comparator. Instead of a residue, the input minus a value determined by the previous stage decision is amplified, as in [10]. Consequently, each stage output contains no information about the digital decision of that stage. Instead, the digital decision determines which of two units of the next stage is activated. This significantly increases the maximum speed, as each stage can generate its output without waiting for its comparator decision.

In the example of Fig. 4, the first stage comparator output is positive, so the top unit of the second stage is activated. Due to a negative second stage decision the second third stage unit is activated and generates the input for a pair of 2-bit flash converters while stage one is reset. Because of a positive third stage decision the third of eight 2-bit flash sub-converters is activated while stage two is reset.

A block diagram of the dynamic amplifiers and comparators is shown at the top of Fig. 5, circuit schematics are shown at the bottom. Switches resetting the drains of P2, P3, and P4 to ground are not shown for simplicity. The dynamic amplifier uses internal comparator nodes $\mathrm{D+}$ and $\mathrm{D-}$ to generate its differential output (through P1) while the comparator input voltages are used for common-mode feed-forward (through P2). The comparator is a modified version of [15] calibrated using digitally controllable capacitors [16] instead of a shunt input pair and will

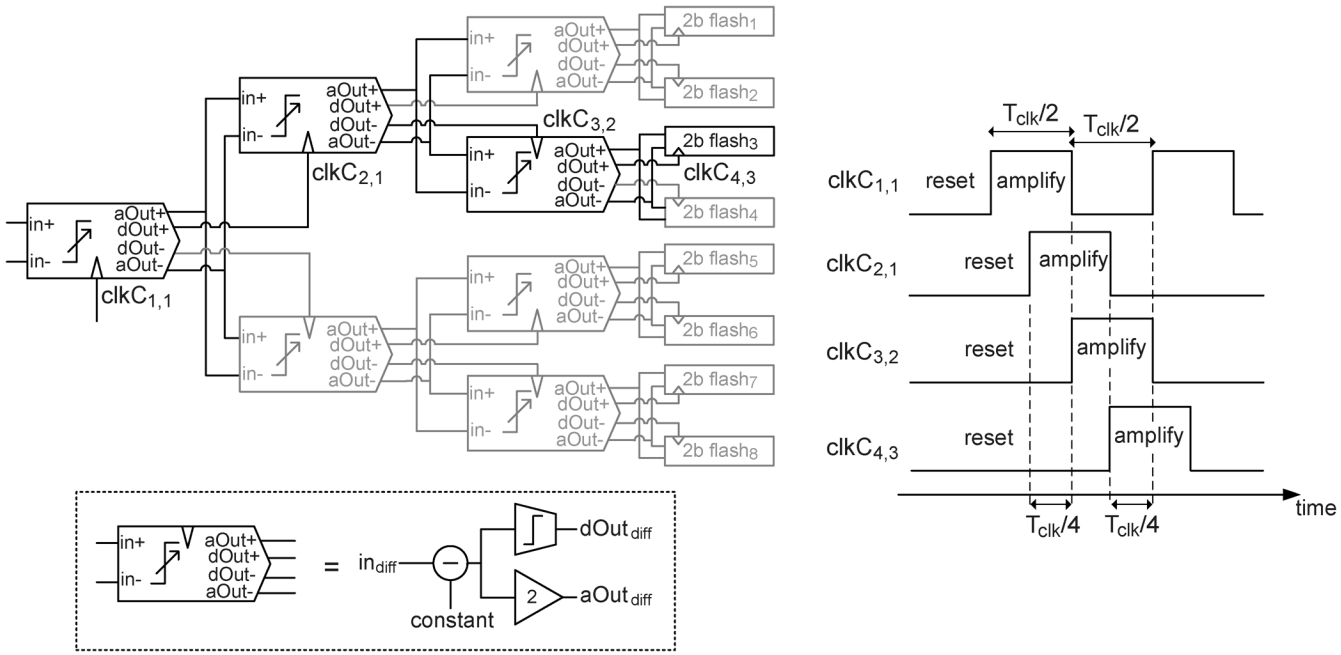

Fig. 4. Block diagram of the PLBS sub-converter. Grayed out parts are inactive for an example conversion.

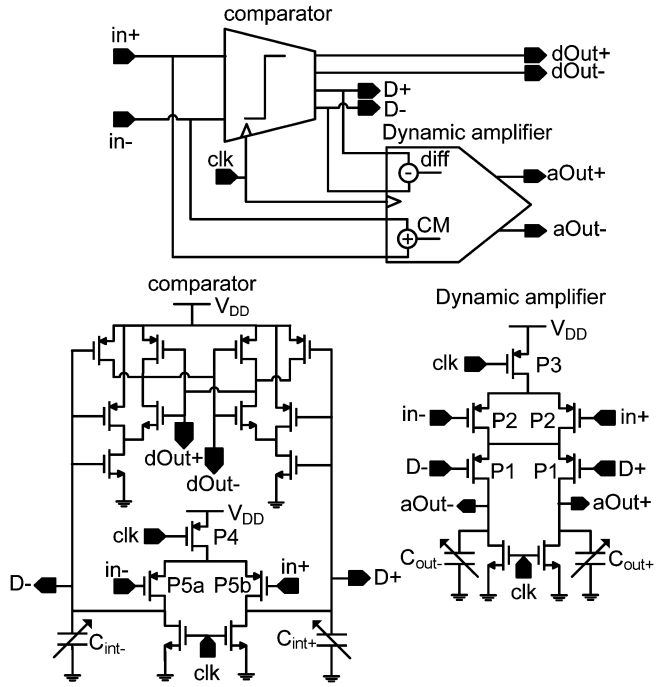

Fig. 5. Block diagram (top) and schematics (bottom) of the comparator and dynamic amplifier used in the PLBS sub-converter.

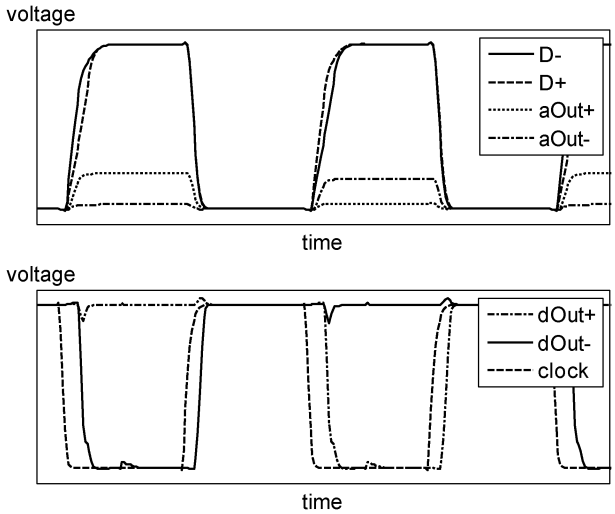

Fig. 6. Simulated waveforms of the dynamic amplifier and comparator.

not be discussed further here. The common-mode feed-forward (P2) is ignored for now.

Fig. 6 shows simulated waveforms of the dynamic amplifier. When the clock is high the circuit is reset: nodes $\mathrm{D}+$, $\mathrm{D}-$, $\mathrm{aOut}+$ and $\mathrm{aOut}-$ are pulled to ground and there is no static current. At a falling clock edge, $\mathrm{D}+$ and $\mathrm{D}-$ charge up to $\mathrm{V_{DD}}$ with a speed depending on the input voltage. Transistors P1 briefly carry current until the voltages on $\mathrm{D}+$ and $\mathrm{D}-$ are high enough to turn them off. At this moment, the voltages on $\mathrm{aOut}+$ and $\mathrm{aOut}-$ are fixed and correspond to the amount of charge put in $\mathrm{C_{out}}$ by P1. This charge depends on the slope of $\mathrm{D}+$ or $\mathrm{D}-$ and hence the input voltage, resulting in a monotonic (but not linear) input-output characteristic. The circuit thus implements an extremely low-power amplifier that consumes no static current. The amplifier settling time corresponds to the time it takes for nodes $\mathrm{D}+$ and $\mathrm{D}-$ to turn off P1, roughly 250 ps in simulation, which is less than the required comparator regeneration time. The amplifier nonlinearity is compensated by the individual threshold calibration in the PLBS architecture.

The amplifier output voltage depends on the slew rates of $\mathrm{D}+$, $\mathrm{D}-$, $\mathrm{aOut}+$ and $\mathrm{aOut}-$, and hence on the values of $\mathrm{C_{int}}$ and $\mathrm{C_{out}}$ and the drive currents of the input pair and P1 transistors. The $\mathrm{C_{int}}$ and $\mathrm{C_{out}}$ capacitances are implemented using an array of nMOS transistors with digitally controllable gates and their

sources and drains connected to the D and aOut nodes respectively. All of these arrays have a fixed width and binary scaled lengths. By digitally changing the gate voltages the gain and offset of the amplifier are tuned, according to the procedure described in Section V. The values of C_{int} are also used to calibrate the comparator threshold, which will be taken into account in this calibration procedure. Six elements are used for each C_{int} and four for each C_{out} yielding a total of 20 bits controlling each dynamic amplifier and comparator.

The common-mode output level of this dynamic amplifier is not exactly known at design time. This is a potential issue because common-mode gain could cause the common-mode to diverge: higher common-mode input decreases the slew rate of the $D+$ and $D-$, resulting in more charge put into capacitors C_{out}, and hence higher common-mode output level still. Transistors P2 decrease the common-mode gain of the dynamic amplifier by decreasing the drive current of P1 when the common-mode input level increases. As a result, the output common-mode level is nearly independent of the common-mode input.

Analytical noise calculations for the dynamic amplifier require stochastic differential equations [17] and are outside the scope of this work. However, for a given speed the input-referred noise can be decreased by increasing the power consumption quadratically. The linearity of the PLBS sub-converter is in theory limited only by the calibration step. In practice however, the complexity of the calibration and thermal noise will restrict the applicability of this PLBS technique at higher resolutions. As the amplifier settling is faster than comparator regeneration it does not limit the speed of the PLBS sub-converter. Rather, this speed is limited by the time required for a comparator to regenerate, the aperture time of the next comparator, and the time required to reset the first comparator. The speed could thus be improved by decreasing the comparator regeneration time, for example by increasing the overdrive of the input pair. However, as shown in [17], this would increase the input-referred noise for a given power consumption and thus impose a power consumption penalty.

Because of the folding front-end, the input range of the PLBS sub-converter should not be centered around zero. Instead, it should span from 0 mV to approximately 200 mV differential, with the threshold determining the MSB of the sub-converter, implemented by the first stage comparator of Fig. 4, at approximately 100 mV. This threshold corresponds to a threshold at positive or negative 160 mV at the ADC input.

To accommodate this, intentional offset is added to both the comparator and the amplifier by using different widths for P5a and P5b which changes the slew rates of the $D+$ and $D-$ nodes. In first order, the threshold of the imbalanced comparator is the input voltage for which the two nodes have equal rise-time. When these rise-times are equal, equal charge is put into both C_{out} capacitances, and the differential output voltage is zero. This imbalance therefore implements a subtraction of 100 mV before comparison and amplification. If a gain of two is implemented by the dynamic amplifier, the output swing of the first stage therefore spans from -200 mV to 200 mV. The individual amplifiers in the second stage then process inputs ranging from -200 mV to 0 and 0 to 200 mV, respectively. This implies that the circuit from the first stage can be reused in the second stage, with differential inputs swapped when appropriate. Similarly, the third stage also only contains this identical circuit block. It is interesting to note that in the second and third stage the subtraction due to the imbalance corresponds to the generation of the residue of the first and second stages, respectively. The circuit in Fig. 5 therefore replaces the comparator, amplifier, and DAC of a conventional pipeline stage.

As a result of using the same size dynamic amplifier and comparator in the first three stages, these stages generate equal noise. However, due to the small-signal gain in the pipeline stages, the input-referred noise contribution of comparators and amplifiers in the second and third stages is smaller than that of the first stage. It would be possible to decrease the power consumption and in turn increase the noise of the second and third stages of the PLBS without significantly impacting the performance. This is not done in this prototype to minimize the design effort. The first stage dynamic amplifier and comparator are sized such that its noise limits the performance of the overall ADC, to maximize the power efficiency.

The nominal thresholds of the flash back-ends should be at ± 50 mV, ± 100 mV, and ± 150 mV. The comparator topology from the PLBS stages is reused, with intentional offset implemented by an imbalanced input pair which results in three different comparator sizings for the different nominal offsets. These comparators are implemented with roughly 40% reduced power consumption and consequently almost threefold increased noise with respect to the pipeline stage comparators. In addition, the calibration step used for the comparator offset is increased, using only 4 bits per C_{int} array. Due to the nominal gain of 4 in the pipeline, the noise and calibration step referred to the PLBS sub-converter input are still smaller than those of the first stage comparator.

V. Low Timing Skew Interleaved Sampling

Interleaved converters are subject to many kinds of errors such as gain error, offset error, bandwidth mismatch and timing skew. In this design gain error and offset error are reduced to acceptable levels through threshold calibration, bandwidth mismatch is reduced by ensuring the bandwidth spread of the sampling network is sufficiently small and the nominal bandwidth sufficiently large. Timing skew requires highly accurate clock signals and accurately matched sampling switches. In this section it is explained how the low timing skew spread required for uncalibrated interleaved sampling is achieved. The effect of timing skew spread is analyzed using high-level Monte Carlo simulations, as shown in Fig. 7. The top plot of Fig. 7 shows the distribution of the ENOB at 1.7 GHz of 5000 instances of an otherwise ideal four-channel 6-bit converter with different levels of timing skew spread. The yield, defined as the percentage of these converters attaining 5.5 ENOB at 1.7 GHz, is shown in the bottom plot.

The sampling instant of each channel is defined by the opening of the bottom plate switches in its folding stage. The signals controlling these switches are obviously unique to each converter channel, and their falling edges of these signals must occur precisely one period of the master clock apart. The obvious approach to generating the required signals would be to divide the master clock signal by four and use the four phases

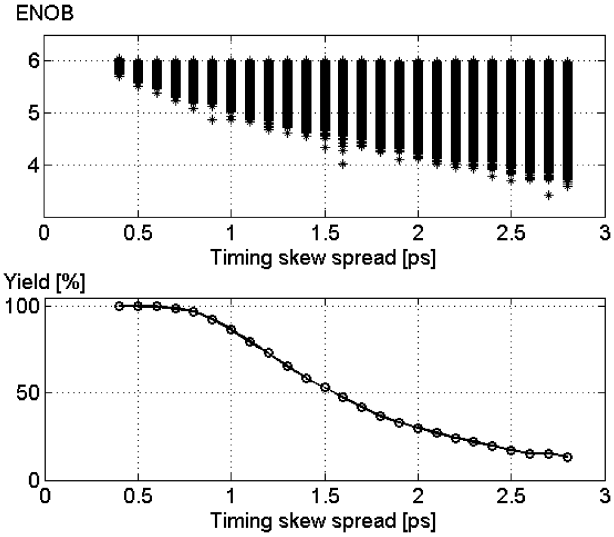

Fig. 7. Distribution of ENOB at 1.7 GHz for 5000 four-channel 6-bit converters with different levels of timing skew spread (top) and yield for 5.5 ENOB at 1.7 GHz (bottom).

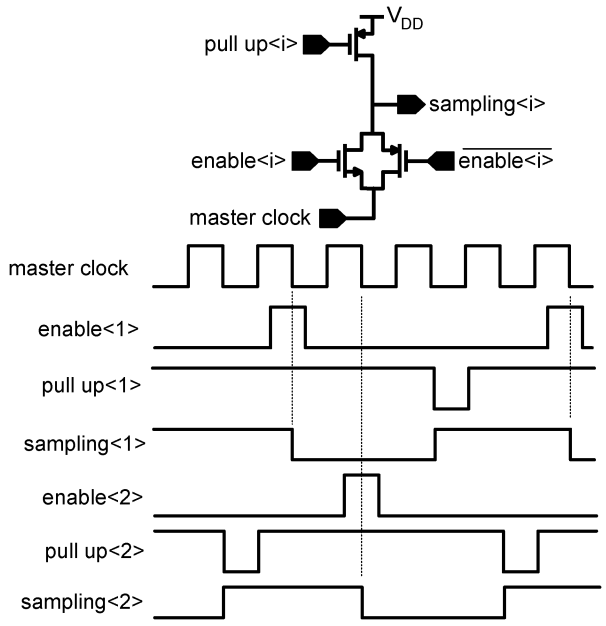

Fig. 8. Circuit used to generate sampling signals (top) and waveforms illustrating its timing (bottom).

of the divided signal to clock the different channels. However, the delays between the common clock edges and the edges of the sampling signals must match precisely. Due to local process variability, each transistor in the clock path between the common master clock signal and the bottom plate switches adds delay spread inversely proportional to its area. Consequently for these transistors a minimum area is imposed, which also fixes the minimum power consumption to switch the required size transistor. In this design the number of transistors in this path is aggressively minimized, thereby limiting the number of contributions to spread in the aforementioned delay. As the allowed total delay spread is unchanged, the reduced number of transistors can each contribute a larger portion to this total spread which implies the remaining transistors have relaxed matching requirements. Consequently, the power consumption is reduced both due to a reduced number of transistors to switch as due to the lower area required for each transistor.

In this design, only a pass-gate separates the falling edge of the sampling signal and that of the common master clock signal, as shown at the top of Fig. 8, with the timing of the timing of these signals for the first two channels shown at the bottom of this figure. The sampling signals generated in this way directly control the bottom plate switches. The $\overline{enable}$ signals close the switches of Fig. 8 slightly before the falling edge of the common clock signal, and open again before its rising edge thereby passing the falling edges of the common clock to the sampling switches. As the start of the tracking phase is not critical, the rising edges of the sampling signal are generated using a pMOS transistor controlled by a non-critical signal. The timing of the top plate sampling switches is less critical and signals controlling these switches are generated from the bottom plate signal using two cascaded inverters.

Because the signals generated as in Fig. 8 are floating for most of the conversion time, there is a potential issue of charge injection changing the voltage from the desired level. To avoid this some care is taken during layout to avoid parasitic coupling capacitance into these nodes. Harmful coupling through C_{gs} and C_{gd} is also avoided: the sensitive signals are only applied to the bottom plate switches, the source and drain of which remains at ground potential during tracking. While these sources and drains do change during the hold phase, the differential changes on the positive and negative side cancel, and the common mode change is too small to cause any adverse effect on the operation.

The critical sampling instants are thus controlled by falling edges of a common clock, and all other signals are robust to significant amounts of mismatch. This reduces the power consumption required for the generation of the closely matched interleaved sampling clocks. In this configuration, the timing skew on the falling edges of the sampling signals is determined only by the spread in the on-resistance of the pass-gates of Fig. 8. The simulated spread on this falling edge is reduced to 500 fs using 2 μm devices for both nMOS and pMOS in the pass-gate. This enables very low power consumption in the critical timing path. While using larger devices still for these pass-gates would reduce the spread of its on-resistance, the higher parasitic switch capacitance can decrease the slew-rate on these nodes and thus increase the timing spread unless the drive strength of the common clock is suitably adjusted.

The sampling switches themselves also contribute to timing skew. If the average threshold voltage of the sampling switches in one of the four channels is too high, the sampling instant of this channel will be too early because the gate voltage of the sampling switches has a finite slew rate. Since the sampling switches have a threshold voltage spread of 15 mV and a simulated slew rate of 32 V/ns at their gates, this yields a timing spread contribution of roughly 500 fs.

Since the two contributions the timing spread are assumed independent, their powers must be summed yielding a total timing skew spread of roughly 700 fs. In an otherwise ideal four-way interleaved ADC, this results in an ENOB greater than 5.5 at

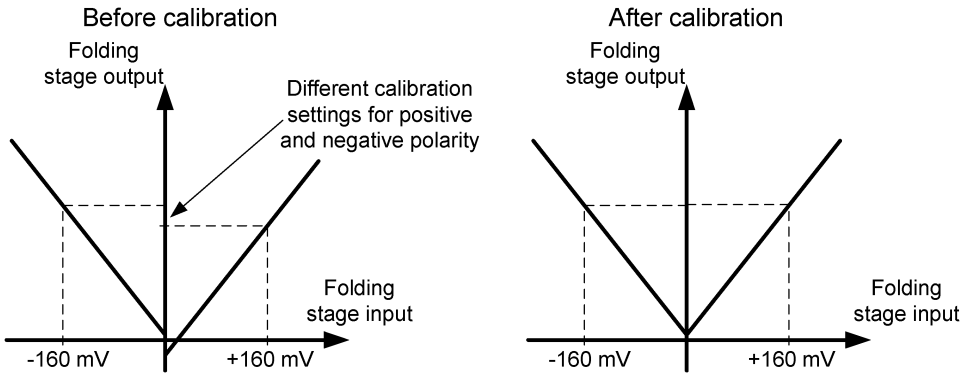

Fig. 9. Bottom plate calibration in the folding stage improves the folding symmetry.

1.7 GHz in over 99% of samples. Since the timing skew is limited to an acceptable value by design, the four ADC channels can be simply put in parallel and clocked at appropriate times, without front-end sample and hold or timing calibration.

VI. Calibration

In this section we will describe the calibration procedure used for this design. The four channels are calibrated one at a time in no particular order and their outputs are isolated by outputting all zeros for the other three channels. Each comparator threshold is calibrated by applying the desired threshold at the ADC input (for example with a low-speed DAC) and changing $\mathrm{C_{int}}$ in a binary search. Each step of the binary search uses 1736 samples to average the effect of noise as described in [18]. In addition to the comparator thresholds, the tunable capacitance on the bottom plates of the sampling capacitances and the values of $\mathrm{C_{out+}}$ and $\mathrm{C_{out-}}$ must be calibrated.

The folding stage comparator is calibrated first. The implementation of this comparator is identical to the comparators in the PLBS sub-converter, except no intentional offset is added. Since $\mathrm{C_{int+}}$ and $\mathrm{C_{int-}}$ are controlled by 6 bits each, this process comprises seven steps in a binary search algorithm.

Next, the bottom plate calibration capacitances are tuned to improve the folding symmetry. To this end the two thresholds implemented by the first stage comparator threshold of the PLBS sub-converter are made as symmetrical as possible, as shown in Fig. 9. This comparator is calibrated for both of the ADC thresholds it implements: $+160$ mV and -160 mV. As shown in the left side of Fig. 9, this will yield different calibration settings if there is significant asymmetry in the folding stage. By comparing the obtained calibration settings for both polarities, the bottom plate calibration capacitances can be adapted to reduce this difference. As there are 3 bits of tuning for each bottom plate capacitance, this process is repeated four times. Each of these iterations comprises seven steps each to calibrate the positive and negative polarity threshold, for a total of 56 steps to calibrate the folding symmetry.

Next, the PLBS sub-converter is calibrated. The PLBS stages are calibrated from the first stage to the last. In each PLBS sub-circuit, the comparator threshold is calibrated first with $\mathrm{C_{int}}$, which requires seven steps. Next, the $\mathrm{C_{out}}$ capacitances are used to set the amplifier output close to the uncalibrated comparator thresholds of the next stage when their corresponding ADC thresholds are applied, as described below.

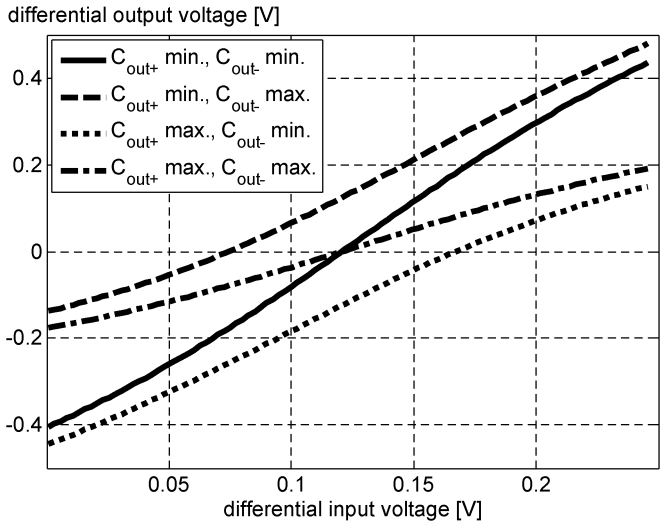

Fig. 10. Simulated input-output characteristic of the dynamic amplifier for different values of $\mathrm{C_{out+}}$ and $\mathrm{C_{out-}}$.

Fig. 10 shows the simulated input-output characteristic for maximum and minimum values of the $\mathrm{C_{out}}$ capacitances. At high input voltages, the output voltage is much more sensitive to $\mathrm{C_{out+}}$ than to $\mathrm{C_{out-}}$, whereas the inverse is true at low input voltages. This matches intuition: when the positive output voltage is high, a lot of charge has been dumped into this node and a change in its capacitance value leads to high voltage change. This input-dependent sensitivity is exploited in the proposed calibration procedure, as explained below.

The calibration of the $\mathrm{C_{out}}$ capacitances is done in two steps, as shown in Fig. 11. In the first step, the top threshold $(\mathrm{th_{top}})$ of the next stage is applied, and $\mathrm{C_{out+}}$ is changed to bring the amplifier output in the calibration range of the comparator which implements this threshold. Next, the bottom threshold $(\mathrm{th_{bottom}})$ of the next stage is applied and $\mathrm{C_{out-}}$ is similarly changed. The next PLBS stage can then be calibrated using the same process: calibrating the comparator threshold first and the $\mathrm{C_{out}}$ capacitances next.

However, the value of $\mathrm{V_{diff}}(\mathrm{th_{top}})$ changes during the calibration of $\mathrm{C_{out-}}$, as shown in Fig. 12. This change is undesired but due to the input-dependent sensitivity described above,

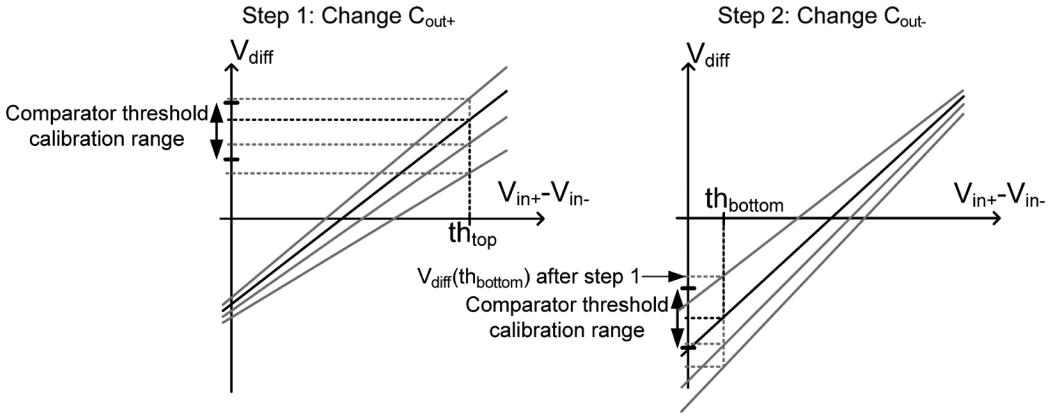

Fig. 11. The two calibration steps used to calibrate $\mathrm{C_{out+}}$ and $\mathrm{C_{out-}}$.

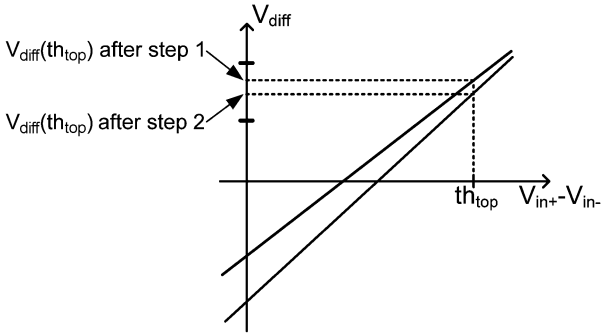

Fig. 12. The unintended change of $\mathrm{V_{diff}(th_{top})}$ during $\mathrm{C_{out-}}$ calibration, which must be accommodated by the calibration range marked on the vertical axis.

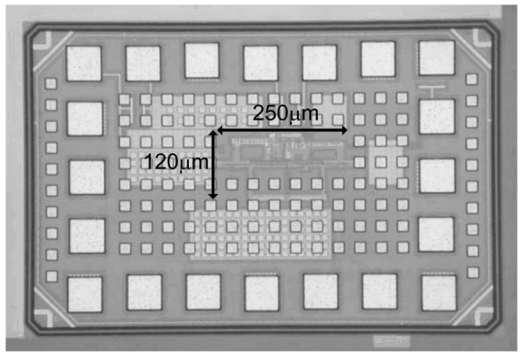

Fig. 13. Chip microphotograph with core area indicated.

$\mathrm{V_{diff}(th_{top})}$ is fairly insensitive to $\mathrm{C_{out-}}$ and will change only slightly during $\mathrm{C_{out-}}$ calibration. This change can easily be compensated for by slightly increasing the calibration range of the comparator thresholds so that no iteration on $\mathrm{C_{out+}}$ is required. Since $\mathrm{C_{out+}}$ and $\mathrm{C_{out-}}$ are controlled by 4 bits each, calibrating both requires a total of eight steps. Combined with the seven steps used to calibrate the comparator threshold, the calibration of a complete PLBS sub-circuit therefore requires 15 steps, for a total of 105 steps for all seven sub-circuits.

After all PLBS stages are calibrated, the 24 comparators comprising the eight flash converters are calibrated. Each of these comparator thresholds requires five steps to calibrate, yielding a total of 120 calibration steps. The complete calibration of a channel therefore requires 288 steps, using 1736 ADC samples each, for a total of roughly half a million samples per channel.

Implementing this calibration on-chip would require a low-frequency DAC to generate reference levels and a calibration controller to control both the DAC and the calibration settings of the ADC. As the DAC levels are used as a reference to steer the ADC levels, their accuracy must be better than the desired ADC accuracy: using a 7-bit linear DAC is sufficient to achieve a 5 ENOB ADC. The calibration controller can easily be implemented in VHDL, and consumes negligible energy compared to the energy required for obtaining the ADC outputs. A final consideration is that the calibration is sensitive to both supply voltage and temperature, and must therefore be repeated when these change. If continuous operation is required, a fifth, redundant channel could be implemented: in this configuration one channel can always be calibrated while the five channels rotate between normal operation and calibration.

In this prototype, neither the reference DAC nor the controller is implemented on-chip: they are replaced by GPIB-controlled voltage sources and a PC running Matlab respectively. The bits controlling the calibration are stored in an on-chip shift-register and programmed using a serial interface.

VII. Measurements

The ADC prototype has been manufactured in a one-poly-seven-metal (1P7M) 40 nm low-power CMOS process with a core chip area of 0.03 $\mathrm{mm^2}$ as shown in Fig. 13. The folding front-ends are located close together, near the central clock generation to improve the matching and reduce the routing required for the sampling clock signals. As a result, the routing connecting the folding front-end output to the inputs of the pipeline stages is longer and does not match for the four channels. This is not an issue since any variation is corrected by threshold calibration.

All data is brought off-chip at full speed by three 2-bit, 50 Ω output DACs for measurement with a four-channel oscilloscope. The power required for buffering the bit streams to these DACs and the DACs themselves is drawn from a separate supply and not included in the reported power consumption.

The ADC is calibrated at low speed for a 10 mV LSB using 300 mV of common-mode input voltage and a 1.1 V supply. The calibrated static performance is then measured at 2.2 GS/s

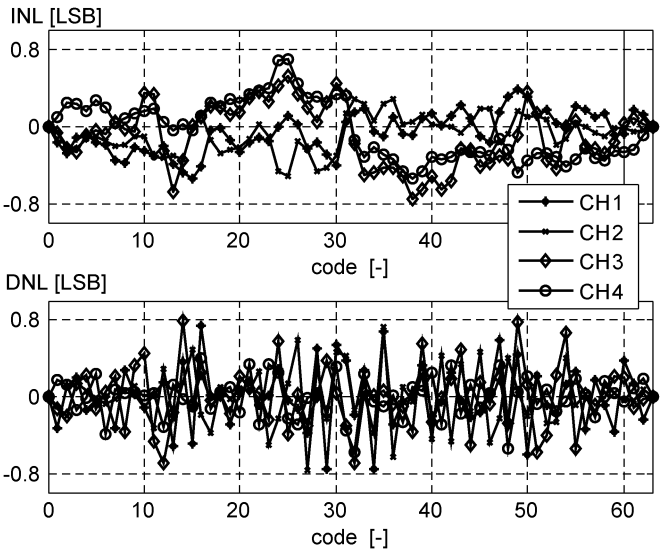

Fig. 14. Calibrated INL and DNL of each ADC channel.

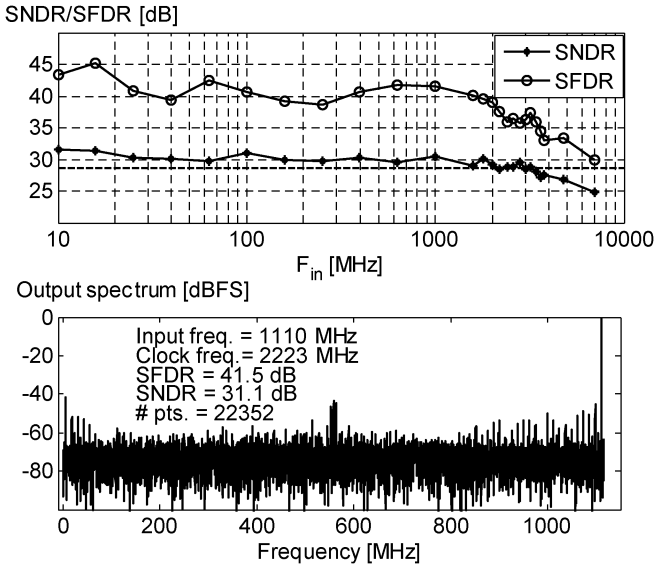

Fig. 15. Measured SNDR and SFDR versus input frequency at 2.2 GS/s sampling frequency (top) and output spectrum (bottom).

using a slow ramp input. The INL and DNL for each channel are below 0.8 LSB as shown in Fig. 14. The INL and DNL of the overall converter are within 0.5 LSB due to averaging of the different channels. Decreasing the calibration step would benefit the linearity somewhat at the cost of increased calibration effort.

In channels 2 and 4 there is an unintended parasitic coupling between the folding stage outputs and the digital output of the folding stage comparators. This coupling results in errors when the MSB of the ADC channel changes. In channel 2, for example, the bit-line couples to the negative folding stage output. When the MSB changes from zero to one, the bit-line injects charge into the negative folding stage output and shifts its voltage up. As a result, the differential voltage at the pipeline input is decreased, leading to decreased output codes. When the MSB changes from one to zero, the voltage on the negative folding stage output is lowered, hence increasing the differential voltage at pipeline input. Due to the folding action, this again results in a decrease of the digital output. In channel 4, the coupling acts on the positive folding stage output, with the inverse effect. The coupling can easily be removed without performance penalty in a redesign. In this design, the errors are reduced digitally by applying the following algorithm to the ADC outputs:

$$corrected = out(n) + X \cdot [out_{\mathrm{MSB}}(n) \oplus out_{\mathrm{MSB}}(n-4)]$$

$$X = \begin{cases} 1, & for\ channel\ 2 \\ -1, & for\ channel\ 4 \\ 0, & for\ channels\ 1\ and\ 3. \end{cases}$$

For the remainder of the measurements, this correction algorithm is applied to the output data.

The top plot of Fig. 15 shows SNDR and SFDR versus input frequency at 2.2 GS/s, the low-frequency SNDR is 31.6 dB, limited by thermal noise, and the ERBW is 2 GHz. The bottom plot in Fig. 15 shows the spectrum with a 1.1 GHz input at 2.2 GS/s. As can be seen near 550 MHz in this plot, all interleaving related spurs are below -40 dBFS.

The variation of the low-frequency ENOB as a function of the common-mode and supply voltage is shown in Fig. 16. Unless a new calibration is done, 50 mV change of the supply

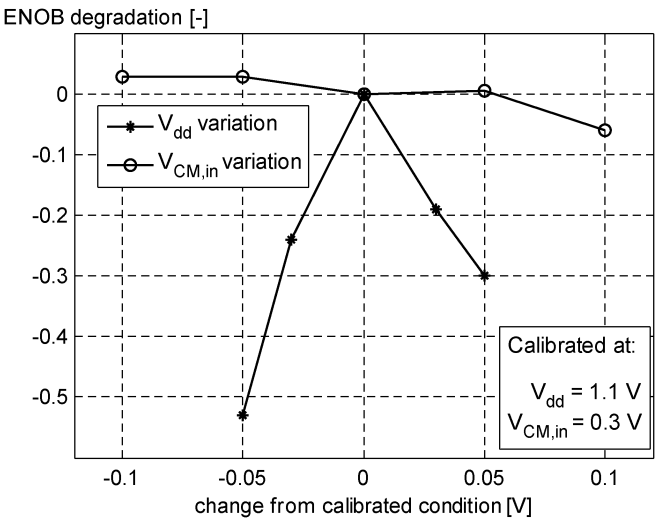

Fig. 16. Measured degradation of the low frequency ENOB as a function of the supply voltage and common-mode input voltage.

voltage degrades the low frequency ENOB by 0.5. From simulations, a temperature increase of 20 degrees has roughly the same effect as 25 mV increase of the supply voltage. Due to the common-mode suppression in the sampling stage, the ENOB is nearly independent of the common-mode input voltage. The ENOB only decreases slightly towards higher common-mode inputs, which can be explained by the reduced top plate switch overdrive. Up to 400 mV common-mode input, the low-frequency ENOB degrades by less than 0.1.

The SNDR and SFDR for different clock frequencies with a near-Nyquist input are shown in the top plot of Fig. 17. The SNDR starts dropping around 2.2 GS/s, to 26.2 dB at 3.5 GS/s. Since the ADC consumes no static power and the dynamic power is 1.15 pJ/conversion, the energy per conversion step is 40 fJ up to 2.2 GS/s as shown in the bottom plot of Fig. 17.

The performance of the ADC can be increased by increasing the input range of the ADC. Recalibrating the circuit with a

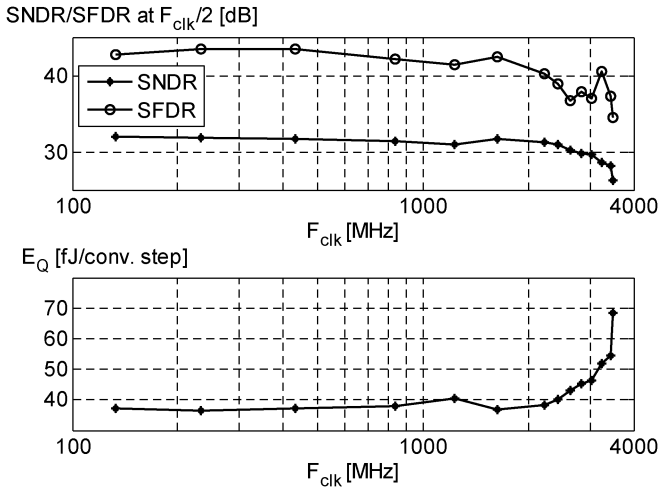

Fig. 17. Measured SNDR and SFDR near Nyquist input frequency (top) and energy per conversion step (bottom) versus clock frequency.

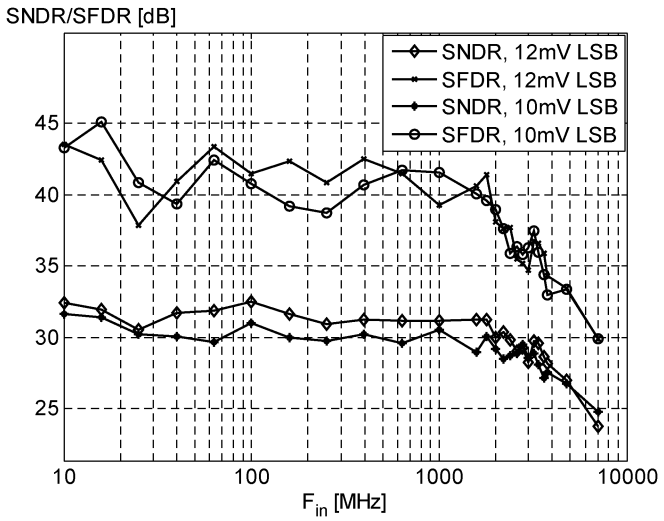

Fig. 18. Measured SNDR and SFDR at 2.2 GS/s for 10 mV and 12 mV LSB sizes.

12 mV LSB yields the SNDR and SFDR shown in Fig. 18. The SFDR is nearly unchanged, but the SNDR increases by an average of 1.2 dB in the 2 GHz effective resolution bandwidth before the SFDR starts decreasing. This increase is largely due to the decreased impact of thermal noise and in part due to a relative decrease of the threshold calibration step. With the increased input range, the energy per conversion step decreases to 35 fJ, but the input energy per conversion step defined as

$$E_{Q,in} = \frac{C_{\text{in}} \cdot (\text{input range})^2}{2^{3 \cdot \text{ENOB}}}$$

increases from 2.7 aJ to 3 aJ. The performance of this prototype is summarized in Fig. 19.

VIII. Conclusion

We have presented a 2.2 GS/s 6-bit fully dynamic folding/PLBS/flash ADC. The converter consists of four identical channels in parallel each of which consists of a 1-bit folding stage and a pipelined binary search sub-converter. Due to low timing skew interleaved sampling, no front-end sample and hold is required.

Technology	**1.1V 40nm LP CMOS**
Area	**0.03 mm^2**
Speed	**2.2 GS/s**
INL	**< 0.8 LSB**
DNL	**< 0.8 LSB**
SNDR$_{max}$	**31.6 dB**
SNDR$_{min.}$ (in Nyquist bandwidth)	**29.6 dB**
ERBW	**2 GHz**
Power consumption	**1.15 μW/MHz**
Input range	**640 mV$_{pp,diff}$**
Input capacitance (single-ended)	**200 fF**

Fig. 19. Performance summary.

The folding stage samples the input signal, removes its common-mode and rectifies the differential signal through passive charge sharing. The sensitivity of the implemented folding stage to mismatch in parasitic capacitance and load capacitance has been discussed, and it has been shown that only the bottom plate parasitic capacitances present a serious problem, which is tackled using calibration in this prototype.

The pipelined binary search sub-converter provides low power quantization with a low input capacitance. The absence of linearity requirements in this architecture is leveraged to introduce a novel dynamic amplifier which allows high speed settling at low power consumption.

It has been explained how the low timing skew interleaved sampling is achieved. This timing skew spread is reduced to just 700 fs by passing the falling edges of a common master clock signal to individual channels with pass-gates. The four channels can thus be simply put in parallel without front-end sample and hold or timing calibration.

The procedure used to calibrate the thresholds of this ADC has been described. For each ADC threshold, digitally controllable capacitance at the amplifier outputs is used to coarsely tune the preceding amplifier characteristics. Next, capacitance on internal comparator nodes is used for fine tuning of the input-referred comparator threshold.

The prototype converter consumes no static power, and dynamic power of 1.15 pJ/conversion from a 1.1 V supply. At 2.2 GS/s, the low frequency SNDR is 31.6 dB with an ERBW of 2 GHz. This yields an energy per conversion step of only 40 fJ with an input capacitance of only 200 fF and an LSB of 10 mV LSB. Increasing the size of the input range by 20% increases the SNDR by roughly 1.2 dB and lowers the energy per conversion step to 35 fJ.

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Bob Verbruggen (S'07–M'09) received the M.S. and Ph.D. degrees in electrical engineering from the Vrije Universiteit Brussel, Belgium, in 2005 and 2010, respectively. During his Ph.D. he worked on high-speed calibrated analog-to-digital converters at the Smart Systems and Energy Technology group of IMEC.

In 2010 he joined IMEC as a researcher working on analog-to-digital converters for software-defined radio systems.

Jan Craninckx (M'98–SM'07) received the M.S. and Ph.D. degrees in microelectronics *summa cum laude* from the ESAT-MICAS Laboratories of the Katholieke Universiteit Leuven, Belgium, in 1992 and 1997, respectively. His Ph.D. work was on the design of low-phase-noise CMOS integrated VCOs and synthesizers.

From 1997 to 2002, he worked with Alcatel Microelectronics (later part of STMicroelectronics) as a senior RF engineer on the integration of RF transceivers for GSM, DECT, Bluetooth, and WLAN. In 2002, he joined IMEC, Leuven, Belgium, where he currently is the senior principal scientist of the analog wireless research group. His research focuses on the design of RF transceiver front-ends for software-defined radio (SDR) systems, covering all aspects of RF, analog, and data converter design. He has authored or coauthored more than 100 papers and several book chapters, and has published one book in the field of analog and RF IC design. He is the inventor of 10 patents.

Dr. Craninckx is the chair of the SSCS Benelux chapter, a member of the Technical Program Committee for the ISSCC and ESSCIRC conferences, and an associate editor of the JSSC.

Maarten Kuijk (M'95) was born in Canada in 1965. He received the Ph.D. degree in electrical engineering from the Vrije Universiteit Brussels (VUB), Belgium, in 1993 on the subject of optoelectronic thyristor devices in III–V semiconductors.

In 1994, he became Assistant Professor at the VUB in the field of integrated electronics and optoelectronics and was additionally appointed as Research Associate for the fund for scientific research Flanders (FWO-V) in 1997. In 2000, he became a Professor in electrical engineering at the ETRO department of the VUB. His current research topics include electrical and optical interconnects devices and building blocks, optical components and sensors, CMOS and SiGe-BICMOS circuits. He has authored or coauthored more than 70 international refereed publications, and holds 19 international patents with eight patents pending. He cofounded the VUB spin-off EqcoLogic which sells equalizer circuits in CMOS for a number of leading electrical communication standards. He cofounded the VUB spin-off Optrima which sells CMOS APS sensors for time-of-flight imaging.

Piet Wambacq (M'91) received the M.Sc. degree in electrical engineering and the Ph.D. degree from the Katholieke Universiteit Leuven, Belgium, in 1986 and 1996, respectively.

Since 1996, he has been with IMEC, Heverlee, Belgium, working as a principal scientist in the wireless research group. He is also a Professor at the University of Brussels (Vrije Universiteit Brussel). He has authored or coauthored two books and more than 200 papers in edited books, international journals, and conference proceedings. His research interests are in the field of circuit design in advanced CMOS for RF and millimeter-wave applications.

Dr. Wambacq was an associate editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS from 2002 to 2004. He was a corecipient of the Best Paper Awards at the Design, Automation and Test Conference (DATE) in 2002 and 2005. He is a member of the ESSCIRC Program Committee.

Geert Van der Plas (S'90–M'03) received the M.Sc. and Ph.D. degrees from the Katholieke Universiteit Leuven, Belgium, in 1992 and 2001, respectively.

From 1992 to 2002, he was a Research Assistant with the ESAT-MICAS Laboratory of the Katholieke Universiteit Leuven. Since 2003, he has been with IMEC (SSET), Belgium, where he is a Principal Scientist and has been working on energy-efficient data converters, low-power scalable radios, signal integrity and design technology for 3-D integration. He has authored or coauthored over 100 papers in journals and conference proceedings and serves as a member of the technical program committee of the Symposium on VLSI Circuits.