A 1-GS/s 6-Bit Two-Channel Two-Step ADC in 0.13-μm CMOS

Hung-Wei Chen, *Student Member, IEEE*, I-Ching Chen, Huan-Chieh Tseng, and Hsin-Shu Chen, *Member, IEEE*

***Abstract*—In this paper, a 6-bit 1-GS/s 49 mW two-channel two-step analog-to-digital converter (ADC) without calibration is implemented in 0.13-μm CMOS process. The proposed multiplying digital-to-analog converter (MDAC) processes the analog signal with two clock periods for one conversion: half for sampling, half for Coarse ADC (CADC) resolving, and one for residue amplification. A self-timing technique is used to prevent disturbance at the beginning of the residue amplification. The reduction of the MDAC output swing by enhancing the accuracy of CADC increases the output devices' over-drive voltage and decreases output loading. The proposed design methods allow closed-loop MDAC to operate at high speed while maintaining low power consumption. The measured SFDR, SNR, and SNDR are 40.7 dB, 33.8 dB, and 33.7 dB, respectively, at the Nyquist rate input. The ADC power dissipation is 49 mW and corresponds to a figure-of-merit (FoM) of 1.24 pJ/conv.-step. The active area occupies 0.16 mm^2.**

***Index Terms*—Analog-to-digital converter, high speed, low power, power efficiency, time-interleaved, two-step.**

I. Introduction

FAST data rate transmission and huge capacity data storage are two essential requirements for high-definition multimedia systems. Ultra-wideband (UWB), Serial ATA (SATA), Blu-ray Disc, and magnetic recording systems, which are widely used in multimedia products, require a 6-bit resolution and Gigasamples per second (GS/s) range ADC to perform high data rate operation. The core competencies for these consumer electronics are low cost and low power; hence, the trend is to realize ADC designs in these systems in a highly integrable low cost CMOS process with minimum area and power. Among the Nyquist ADC topologies, flash architecture can perform at maximum speed because its analog signal level is compared with entire quantization levels in parallel. However, its power, area, and design complexity increase exponentially as the number of bits increases. The comparator offset always limits the accuracy of flash ADC. To meet 6-bit accuracy, the preamplifier and the averaging network are added to reduce the impact of offset voltages by about 3$\times$ [1], [2], but extra power dissipation and silicon area are required.

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The authors are with the Department of Electrical Engineering and Graduate Institute of Electronics Engineering, National Taiwan University, Taipei 10617, Taiwan (e-mail: hschen@cc.ee.ntu.edu.tw).

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The multi-stage architectures, such as two-step, pipeline, or subranging, break the bit resolving into a number of low-resolution ADC stages to reduce the number of comparators. Digital error correction reduces the accuracy requirement for CADCs, but Fine ADC (FADC) still requires high precision. The two-step [3] and pipeline [4] architectures amplify the residue voltage back to full input range to relax the FADC accuracy requirement. However, they are restricted by demanding a high-gain and high-bandwidth operational amplifier (OPAMP) for inter-stage residue amplification. The subranging architecture without residue amplification typically implements auto-zero technique [5] or offset calibration circuit [6], [7] to ensure the FADC accuracy. The calibration circuit is required for each comparator to reach 6-bit accuracy in the FADC. It also needs time for calibration before the output codes become valid. These works [6], [7] demonstrate the DNL/INL improvement by approximately 4$\times$ after calibration.

Recently, low power ADC designs in GS/s range have also been realized by successive approximation (SA) architectures [8]–[10]. As the SA ADC only resolves one bit per cycle, it needs to interleave the greatest number of channels to achieve GS/s. However, timing skew, channel offset, and gain mismatch among the channels demean the performance of time-interleaved ADC [11]. Channel mismatches cause pattern noise that degrades the signal-to-noise ratio (SNR) and the effective bit resolution of ADC. Therefore, it is difficult to achieve high resolution with multiple time-interleaved channels. Calibration circuit is usually needed to achieve high-accuracy time-interleaved ADC.

This work employs two-step two-channel architecture to achieve GS/s. Without any calibration, the residue amplification with gain of 4 is used to alleviate the FADC input-referred offset requirement. The time-interleaved two channels are used to increase conversion rate with minimized degradation caused by channel mismatch. The prototype design achieves 5.3 ENOB at sampling rate 1 GS/s with the Nyquist rate input. In Section II, the architecture is introduced. Then, a rearranged timing scheme and a MADC transfer function are discussed. The key circuit implementations to enhance the ADC speed are highlighted in Section III. In Section IV, the experimental results are presented. Finally, the summary of the paper is given in Section V.

II. Proposed Architecture Overview

A. Converter Architecture

In two-step and pipeline architectures, the residue amplification is used to reduce FADC input-referred offset problems, but it consumes lots of power and time. Pipeline architectures with a

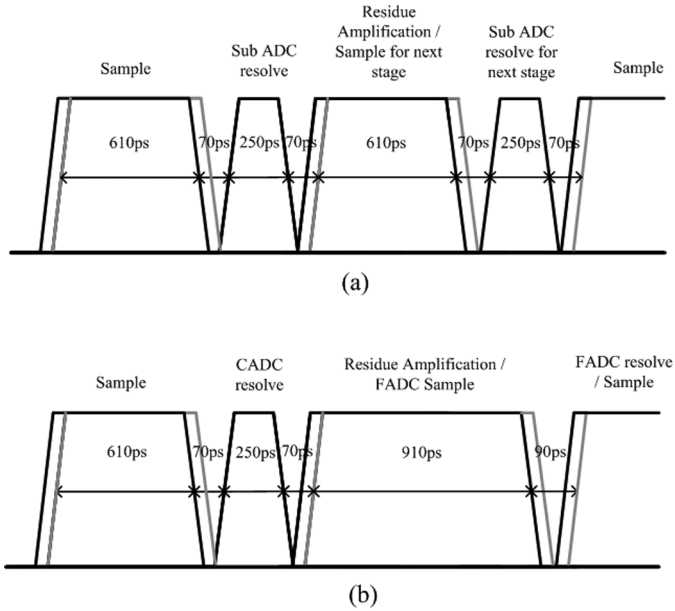

Fig. 1. MDAC timing waveforms for (a) pipeline and (b) two-step.

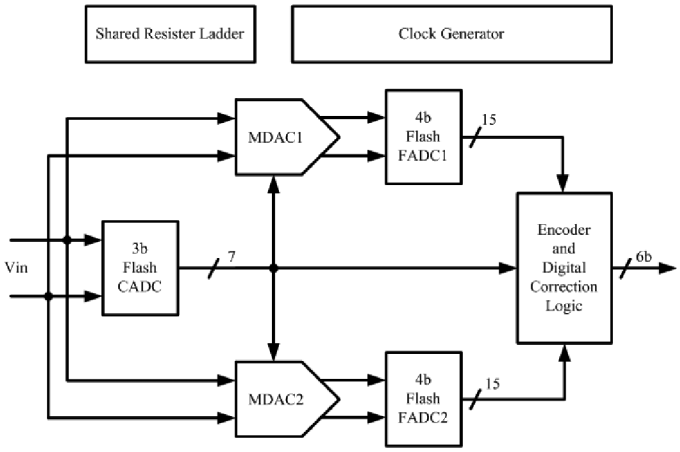

Fig. 2. Block diagram of the proposed ADC.

1.5-bit per stage realize the fastest residue amplification because their feedback factor for the closed-loop MDAC is the highest. However, to obtain the residue amplification with gain of 4 from 1.5-bit per stage pipeline, two MDAC stages are needed. A conventional timing arrangement example for pipeline ADC operating at 500-MS/s is shown in Fig. 1(a). The sub-ADC bit resolving is typically arranged between the sample and the residue amplification phases. Using 0.13-μm technology, this example needs 250 ps for comparator resolving, 20 ps delay for clock bottom-plate sampling, and 50 ps for clock rising and falling edges. The available time for either sample or residue amplification is only 610 ps. On the other hand, because the two-step architecture has only one MDAC, the FADC results do not need to be used for residue amplification. The beginnings of the FADC resolving and the sample phase can be aligned as illustrated in Fig. 1(b). The usable time for residue amplification can now be prolonged to 910 ps. Compared to the 1.5-bit per stage pipeline, the time for residue amplification is 49% longer in this example. The two-step architecture is therefore adopted in this work.

The system block diagram of this work, shown in Fig. 2, consists of a 3-bit flash CADC, two MDACs, two 4-bit flash FADCs, a shared resister ladder, a clock generator, and a digital error correction circuit. The 3-bit CADC converts the input, and its output is selected by the two MDACs alternatively. The MDACs also sample the input and amplify the residue voltages, and the outputs are passed on the corresponding FADCs. The quantization levels for the sub-ADCs are given by the same resister ladder to save power and minimize area. Finally, the results of the sub-ADCs are encoded and reassembled in the digital circuit to construct 6-bit outputs.

B. Timing

In the two-step architecture, the MDAC performs three operations for one conversion: sample, bit-resolve, and residue amplification. In conventional designs, the time of the bit-resolve operation is the shortest compared to that of the other two operations. The bit-resolve operation is arranged between nonoverlapping clock phases. However, the weight of bit-resolve time increases in high-speed designs due to short conversion time, and is no longer negligible. In this work, two clock periods are used for one conversion and half-clock period is dedicated for CADC resolving. The time after CADC resolving in this half-clock period can be utilized for self-timing reference voltage connection, which will be discussed later in detail. The proposed MDAC and the system timing schemes are illustrated in Fig. 3(a) and (b), respectively. An analog signal consumes two clock periods to transform into digital format. The half-clock period is used by the CADC and the MDAC to track the analog signal. Another half is for the CADC bit-resolve and the MDAC reference voltage connection. The other clock period for residue amplification helps reduce the closed-loop bandwidth constraint. The time-interleaved conversion sequence starts with $\phi 1$. V[n] is sampled by CADC and MDAC1 simultaneously. In $\phi 2$, the CADC converts V[n] to a 7b thermometer code; then, a self-timing circuit makes reference voltage connections to the capacitor array of MDAC1 before $\phi 2$ ends. In $\phi 3$ and $\phi 4$, MDAC1 amplifies residue voltage of V[n], and FADC1 samples the output of MDAC1. Concurrently, CADC and MDAC2 begin to process $V[n+1]$ in $\phi 3$. Then, FADC1 quantizes the MDAC1 output in the next $\phi 1$ and $\phi 2$. The output of FADC1 would be encoded into binary code and then combined with the delayed output of CADC by the digital error correction circuit.

C. MDAC Transfer Function

Larger transconductance provided by advanced process devices can enable OPAMPs to reach higher unit gain bandwidth. However, the output resistance of the devices is also reduced because the channel-length modulation effect worsens as channel length is scaled down. The conventional design technique to preserve output resistance is to increase channel length of the device. However, to maintain transconductance of the device with fixed bias current, channel width needs to be increased. As a result, parasitic capacitance of the device becomes larger and the OPAMP bandwidth is decreased. The transconductance of

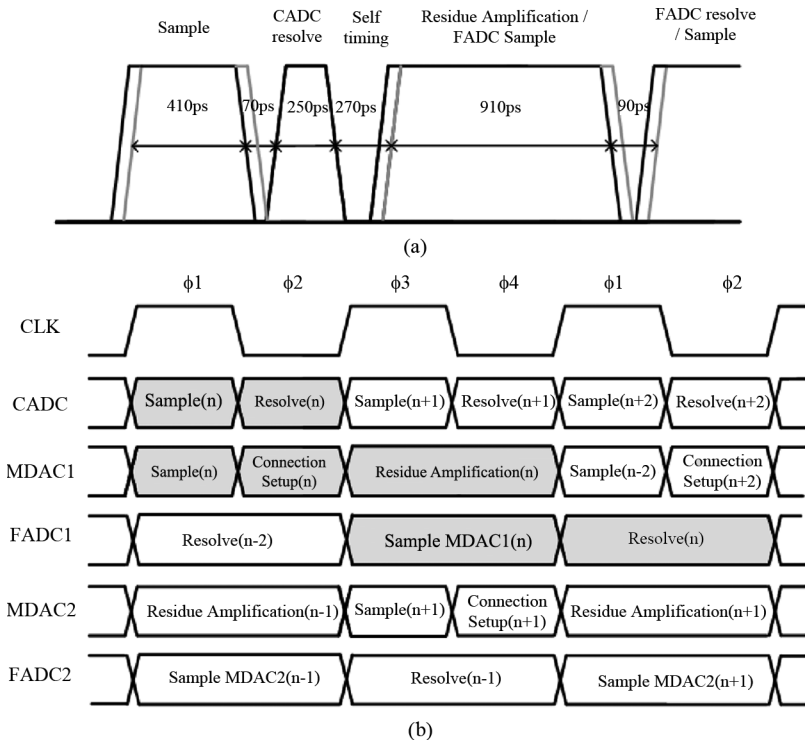

Fig. 3. Proposed timing diagrams for (a) MDAC and (b) ADC system.

active load does not affect the gain or bandwidth of OPAMP. Therefore, the active load should be designed so as to have large enough output resistance with low parasitic capacitance. To provide the fixed bias current with small channel width, the device needs to enlarge the gate-source voltage. To ensure that the active load device is operated in the saturation mode, the drain-source voltage has to be increased, resulting in the reduction of the OPAMP output swing. In this work, the output swing of the OPAMP is relaxed by increasing the accuracy of CADC. The 8-level input-output transfer function utilized in this design is illustrated in Fig. 4. The two-step ADC overlaps the residue voltage range for the second stage to relieve the requirements of the CADC accuracy to 3-bit. When the CADC is more accurate, the OPAMP output swing requirement can be reduced. If the CADC is ideal, the MDAC output can be bounded within only $\pm 1/2V_{\rm ref}$. For example, when the CADC has 4-bit accuracy, the MDAC output would be bounded to $\pm 3/4V_{\rm ref}$. In this work, both the CADC and FADC are designed to be of 4-bit accuracy, and the MDAC output swing can be reduced 25% to $\pm 3/4V_{\rm ref}$. Besides the channel width of the active load can be reduced for less parasitic capacitance, the reduction of the MDAC output swing can also decrease the slew time of OPAMP.

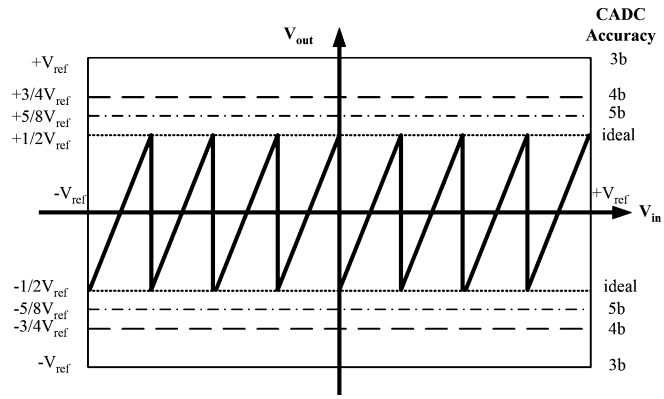

Fig. 4. MDAC transfer function and output swing versus CADC accuracy.

III. Circuit Implementation

A. Charge Injection Disturbance in MDAC

In switched-capacitor MDACs, switches could create disturbances, which are caused by charge injection and clock feedthrough. Because they only consume a small portion of conversion time, they are usually ignored in traditional designs. For high conversion rate designs, this problem worsens because the conversion time is very short. Moreover, larger switches used for smaller turned-on resistance introduce larger disturbance. A typical switched-capacitor MDAC circuit is illustrated in Fig. 5. Here C_s, C_{ov1}, C_{ov2}, and C_a are the sampling capacitor, the overlap capacitors of M_1, M_2, and the parasitic capacitor of $node_1$, respectively. During the sample phase, the transistors M_1–M_3 are turned on. The voltages of $node_2$ and $node_1$ are equal to input voltage, $V_{\rm in}$, and input common-mode voltage, V_{cmi}, respectively as shown in Fig. 5. After sampling the input voltage, by using the bottom-plate sampling technique, M_3 turns off first and then the other switches. The charge injection of M_3 is insignificant. The total charge at $node_1$ and $node_2$ are expressed as Q_1 and Q_2:

$$\begin{aligned} Q_1 &= C_a(V_{cmi} - V_g) + C_s(V_{cmi} - V_{\rm in}) \\ &= C_a(V_{x1} - V_g) + C_s(V_{x1} - V_{x2}) \end{aligned} \quad (1)$$

$$\begin{aligned} Q_2 &= C_{ov1}(V_{\rm in} - VSS) + C_{ov2}(V_{\rm in} - VDD) \\ &\quad + C_s(V_{\rm in} - V_{cmi}) \\ &\quad + \frac{1}{2}C_{ox}W_1L_1\,(VSS + V_{\rm in} - |V_{thp}|) \\ &\quad - \frac{1}{2}C_{ox}W_2L_2\,(VDD - V_{\rm in} - V_{thn}) \\ &= C_{ov1}(V_{x2} - VDD) + C_{ov2}(V_{x2} - VSS) \\ &\quad + C_s(V_{x2} - V_{x1}) \end{aligned} \tag{2}$$

where $C_{ox}W_1L_1$ and $C_{ox}W_2L_2$ are the capacitances between the channel and the gate of M_1 and M_2. The charge injection of M_1 and M_2 to $node_2$ is estimated to be half by assuming that the impedances at the source and the drain are the same, and the rising edge is sharp in this work. To simplify the equation, the absolute value of V_{thp} is assumed to be equal to V_{thn}. As $node_1$ and $node_2$ are high impedance right after the sample phase is finished, the charge injection of M_1 and M_2 induces a drift voltage, $V_{\rm drift}$, at $node_1$.

$$V_{\rm drift} = \frac{(C_{ox}W_2L_2 + C_{ox}W_1L_1)C_s}{2(C_s(C_{ov1}+C_{ov2})+C_aC_s+(C_{ov1}+C_{ov2})C_a)}V_{\rm in}. \tag{3}$$

Eq. (3) shows that $V_{\rm drift}$ is proportional to $V_{\rm in}$, but it does not affect the MDAC transfer function as it disappears after $node_2$ is connected to a reference voltage. However, in conventional designs, the MDAC waits for the CADC output to connect $node_2$ to the corresponding reference voltage at the beginning of the residue amplification phase. If the polarity of $V_{\rm drift}$ is opposite to that of the settled residue input voltage, it originates the OPAMP output by amplifying to the reverse direction. Therefore, it requires additional time to recover. The settling behavior of the OPAMP input and output at the beginning of the residue amplification phase in the traditional MDAC design is shown in Fig. 6. T_{rec_in} is the time for OPAMP input voltage to recover from the effect of $V_{\rm drift}$. The OPAMP output voltage recovery time, T_{rec_out}, is longer than T_{rec_in} due to the delay of OPAMP. T_{rec_in} is dependent on switch turned-on resistance, sample capacitance, reference voltage buffer bandwidth, and the OPAMP closed-loop bandwidth. Because the OPAMP is used in the closed-loop MDAC to accomplish negative feedback, the residue voltage at the OPAMP input has opposite polarity to that at the OPAMP output. When $V_{\rm in}$ equals maximum reference voltage, $V_{\rm drift}$ is maximum and the residue voltage at the OPAMP input is minimum. On the other hand, when $V_{\rm in}$ equals minimum reference voltage, $V_{\rm drift}$ is minimum and the residue voltage at the OPAMP input is maximum. These two cases are the worst-case scenarios, and the OPAMP requires the longest time to recover. The worst-case simulation results based on an ideal reference voltage indicate that T_{rec_in} and T_{rec_out} occupy 10% and 35% of the residue amplification time. In the measurement setup, the finite-bandwidth reference voltage would result in even longer recovery time. Therefore, it is advantageous to avoid the $V_{\rm drift}$ recovery time in the high-speed MDAC design.

As illustrated in Fig. 7(a), because the conventional design synchronizes the reference voltage switches with the residue amplification phase, the OPAMP output needs additional time

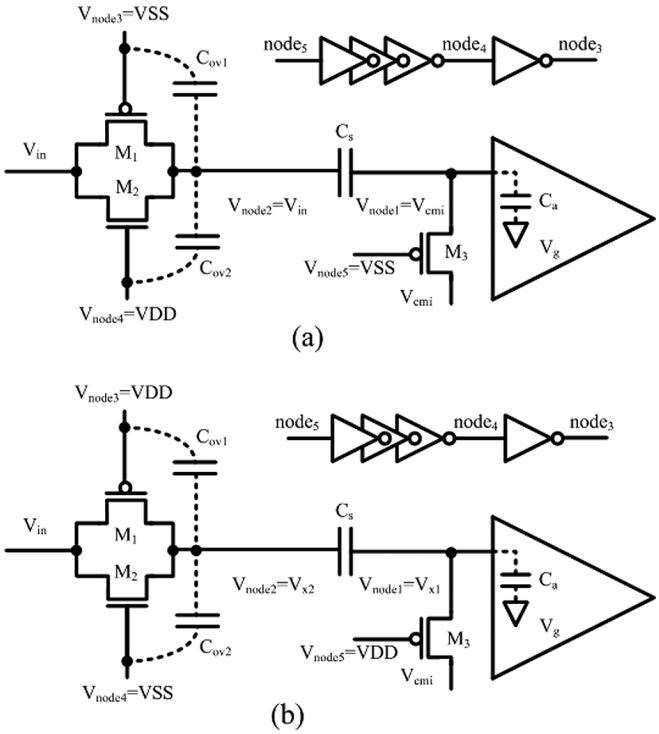

Fig. 5. Sampling switch operation (a) at the sample phase and (b) right after the sample phase.

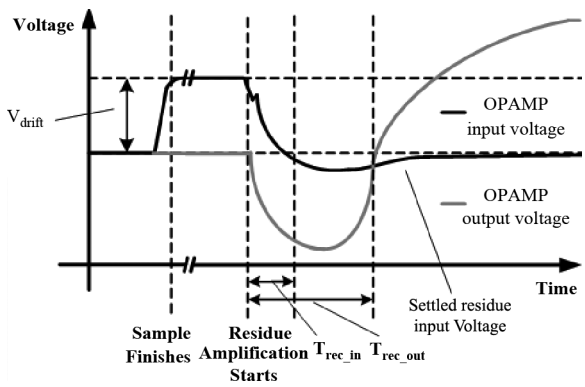

Fig. 6. Settling behavior of MDAC OPAMP input and output in conventional designs.

to overcome the disturbance. To reduce the effect of $V_{\rm drift}$, the proposed MDAC in Fig. 7(b) uses a self-timing switch to turn the reference voltage switches on earlier. Here, seven C_Ss and one C_R in the MDAC track input voltage at the sample phase. Afterward, the C_Ss are connected to the reference voltages, and the C_R input is flipped around to the OPAMP output. In this work, the C_F is used to reduce the residue amplifier gain for CADC error overlapping. The transfer function of this MDAC configuration is given as follows:

$$V_{\rm out} = \frac{C_R + 7C_S}{C_R + C_F} \times V_{\rm in} - \frac{C_S}{C_R + C_F} \times D \times V_{\rm ref}. \tag{4}$$

Here, D is the output code of CADC. The capacitance values of C_S, C_R, and C_F are all 50 fF.

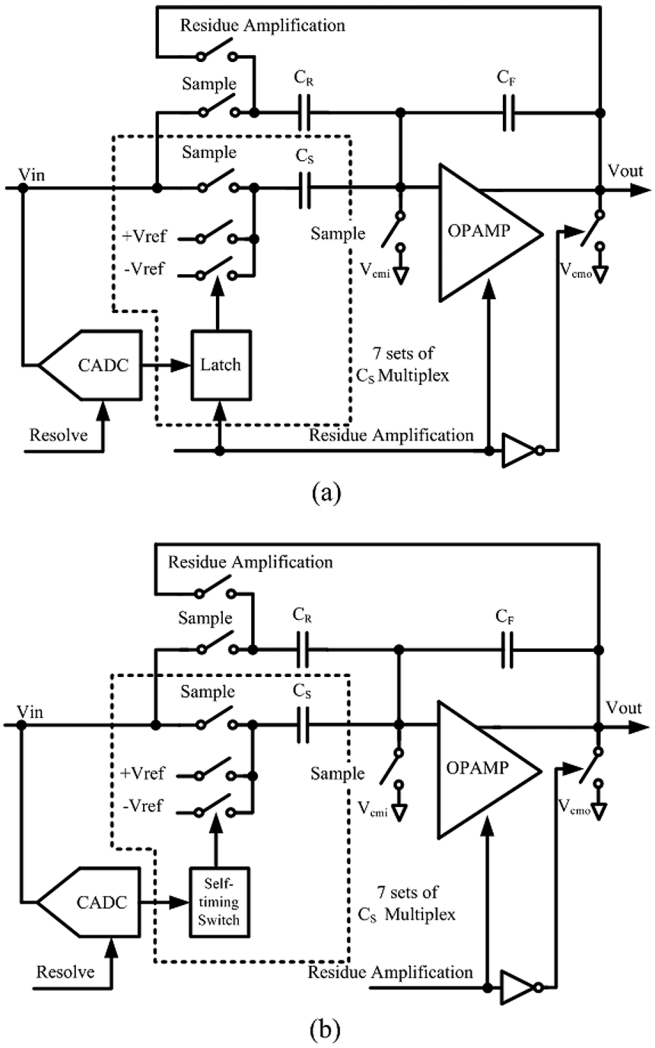

Fig. 7. (a) Conventional MDAC design and (b) proposed MDAC design.

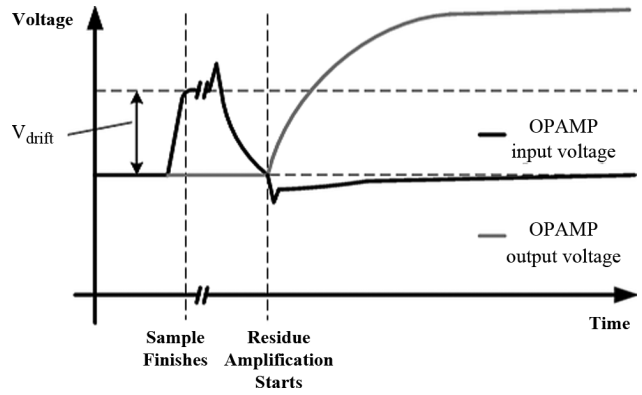

Fig. 8. Settling behavior of MDAC OPAMP input and output with self-timing switch circuit.

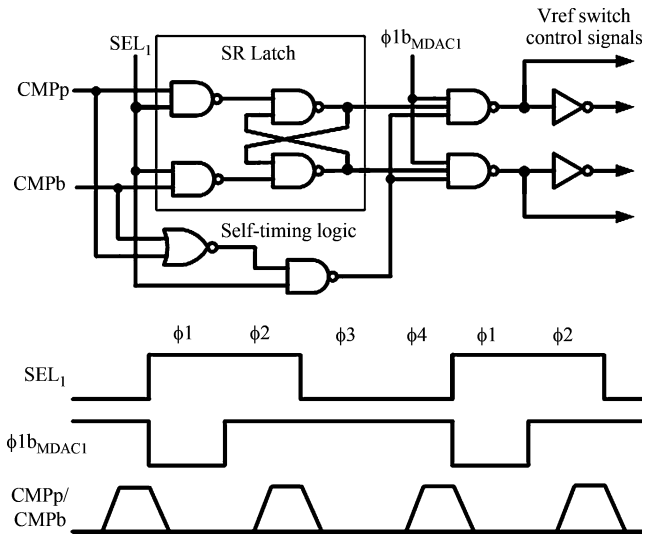

Fig. 9. Self-timing switch circuit.

The CADC is designed to resolve the signal within a half-clock period. Each C_S switch array is controlled by a corresponding CADC comparator. Each comparator in the CADC has two outputs, and they are both reset to the same state before bit resolving. After the comparator resolves the signal, only one of the two outputs would change state. By adding a self-timing circuit, the present work can connect C_Ss to the reference voltages before the amplification phase begins. The effect of $V_{\rm drift}$ can then be eliminated. Even if all seven C_Ss are connected to the corresponding reference voltages 100 ps earlier than the start of the amplification phase, the effect of $V_{\rm drift}$ could be effectively removed during the residue amplification phase. Hence, the MDAC can settle faster, as illustrated in Fig. 8.

B. Self-Timing Switch

The proposed self-timing switch circuit allows the reference voltage switches to remain turned-off before the input voltage is resolved by the CADC. Once the comparator result is made, the self-timing turns on one of the two reference voltage switches before the amplification phase begins. The circuit is utilized in both MDAC channels. An example connection for the MDAC1 channel is presented in Fig. 9. The SEL_1 is high during the sample and bit-resolve phases, which enables the SR latch to update the output code. During the residue amplification phase, it ensures the reference switch is turned-on. The comparator outputs, $CMPp$ and $CMPb$, are reset to low in the sample phase. Because only one of the two outputs rises to high after the comparator decision is made, the NOR gate can be adopted to detect when the bit resolving is finished. The reference switch is turned on after the NOR gate output becomes high. The $\phi 1b_{\rm MDAC1}$ signal is used to make sure reference switches are turned-off in the sample phase. The propagation time of NOR and NAND gates is designed to be a bit longer than that of the SR-latch to prevent glitches in the reference switch control signals. In the metastability situation, when comparator inputs are closed, the result may not be resolved before the amplification phase begins. The SEL_1 signal forces the switches on and then stops the SR-latch to update the comparator output. The reference connection remains as the previous comparator result. The error from metastability can be recovered by digital error correction.

C. OPAMP

The design bottlenecks of high-speed closed-loop MDAC are the bandwidth and slew rate of OPAMP. To improve

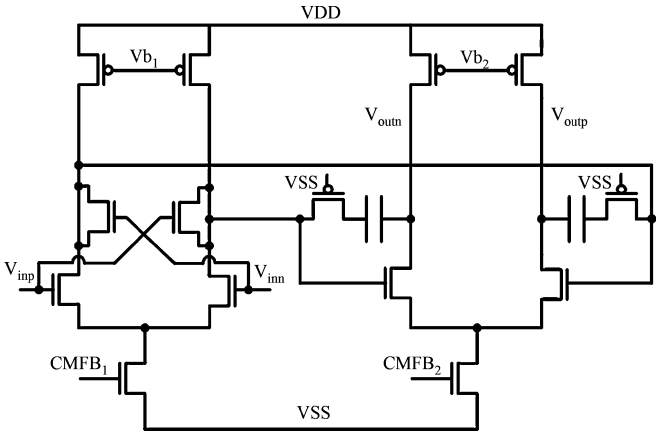

Fig. 10. OPAMP schematic.

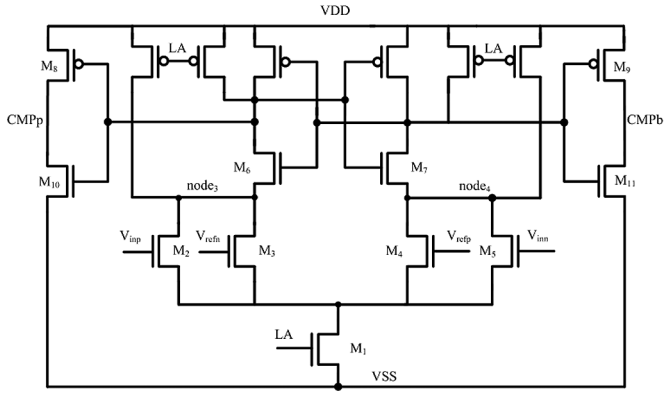

Fig. 11. Dynamic comparator schematic.

these, parasitic capacitance should be as small as possible, and short-channel MOSFET should be used to provide a high current driving ability. The input parasitic capacitance of OPAMP significantly affects MDAC bandwidth because it reduces the closed-loop feedback factor. Two-stage Miller-compensated OPAMP is utilized in this work as shown in Fig. 10. The input common-mode voltage, V_{cmi}, is designed to be 0.9 V, and nMOS is used for the OPAMP input differential pair to allow smaller device sizes. The high value of V_{cmi} gives pMOS large gate-source voltage. Consequently, the sample switches have low turned-on resistance without large device size. In addition, the capacitive neutralization technique is used to reduce the OPAMP input parasitic capacitance [12]; therefore, it further increases closed-loop bandwidth. According to the simulation result, the DC gain is over 46 dB for whole output range. The closed-loop bandwidth and the phase margin are 1.1 GHz and 67 degrees, respectively. The OPAMP consumes a DC power of around 10 mW.

D. Comparator Latch

A 4-input dynamic latch-comparator [13] used in this work is illustrated in Fig. 11. When the clock signal, *LA*, is low, $node_3$ and $node_4$ are reset to high. Then, the comparator outputs, $CMPp$ and $CMPb$, are reset to low. The bit-resolve starts when *LA* is set to high. The transistors, M_2–M_5, are in the saturation mode and M_6, M_7 are in the linear region. Hence, the input-referred offset voltage is mainly contributed from the mismatch of input devices M_2–M_5. When the input signal is resolved, either $CMPp$ or $CMPb$ changes from low to high. The channel width and length of M_2–M_5 are 9.5 μm and 0.18 μm, respectively. The Monte Carlo simulation result shows that the static offset voltage of this comparator is about 30 mV for three sigma variation. The bit-resolving time takes around 250 ps for 30 mV input. The CADC and FADC can achieve 4-bit accuracy without any pre-amplifier or calibration circuit.

IV. Experimental Results

The prototype ADC is fabricated in 0.13-μm CMOS process. The chip area and the active area are 0.97 mm $\times$ 0.94 mm and 0.45 mm $\times$ 0.36 mm, respectively. The chip micrograph is shown in Fig. 12. Care should be taken to ensure a symmetric layout due to the two-channel time-interleaved architecture. The active area floor plan of this work is presented in Fig. 13. Identical symmetry to the center is kept for the two MDAC layouts. The CADC and the resister-ladder reference are placed between the two MDACs. Moreover, the input signal path is placed at the center of two channels from the top to the sampling capacitor arrays and the CADC. Input signals are commonly shielded with ground to prevent clock signal disturbance. However, the shielding technique might increase the parasitic capacitor loading to both input and clock signals. Therefore, this technique is not employed in our design. Instead, to prevent the clock signal from disturbing the input signal, the clock signal is intentionally placed as far from the input signal as possible. The clock signal path into the digital circuit is placed at the opposite direction of the input. The clock signals for MDACs are placed at the two sides.

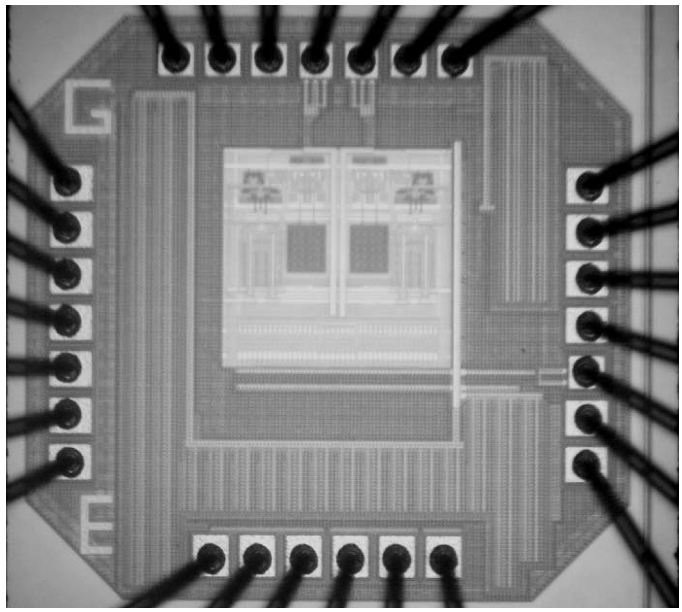

Fig. 12. Die micrograph.

The static performance is measured with 66.7 MHz sinusoidal input signal at a conversion rate of 1 GS/s. Fig. 14 shows the

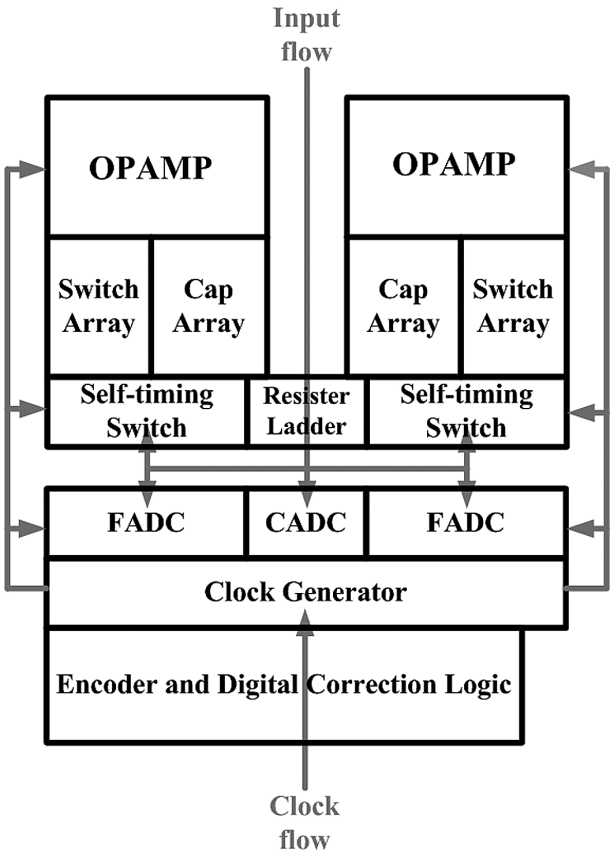

Fig. 13. Floor plan.

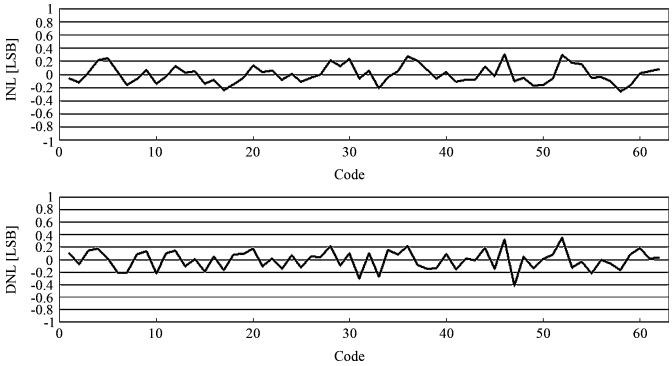

Fig. 14. Measured INL and DNL.

measured differential nonlinearity (DNL) and integral nonlinearity (INL) to be $+0.25/-0.28$LSB and $+0.28/-0.30$LSB, respectively. The dynamic performances of varying input frequencies from 100 MHz to 1067 MHz at sampling rate of 1 GS/s are presented in Fig. 15. The peak SNDR is 34.5 dB at input frequency of 300 MHz, and the SNDR remains above 30.9 dB up to 1 GHz. At the Nyquist rate input frequencies, the SFDR, SNR, and SNDR are 40.7 dB, 33.8 dB, and 33.7 dB, respectively. The FFT spectrum is presented in Fig. 16. The dynamic performance is limited by the skew mismatch between two channels, and the largest spur tone is -40.7 dB at $1/2Fin - Fs$. The tone of $Fs/2$, caused by offset mismatch between the two channels, is -72.4 dB. The second and the third harmonics are

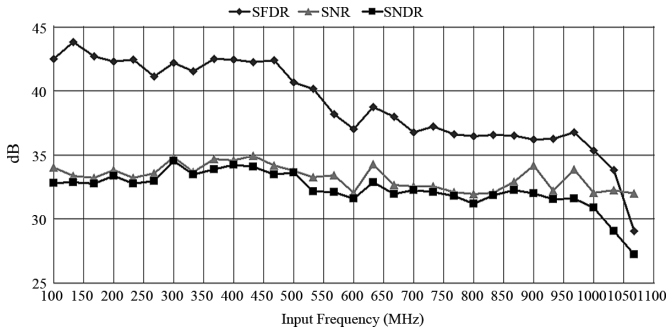

Fig. 15. Dynamic performance versus input frequency at sampling rate 1 GS/s.

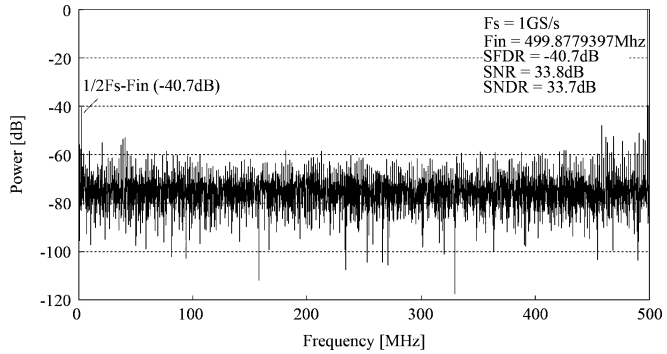

Fig. 16. Nyquist rate input FFT plot at sampling rate 1 GS/s.

TABLE I
MEASURED PERFORMANCE SUMMARY

Technology	0.13-μm CMOS
Resolution	6-bit
Active area	0.16mm^2
Full-scale analog input	1Vpp
DNL	+0.25/-0.28LSB
INL	+0.28/-0.30LSB
Sample rate	1-GS/s
Power supply voltage	1.2V
Power dissipation	49mW
SFDR (Fin = 500MHz)	40.7dB
SNR (Fin = 500MHz)	33.8dB
SNDR (Fin = 500MHz)	33.7dB
FoM	1.24pJ/conv.-step

-59.0 dB and -53.6 dB, respectively. The power dissipations of analog circuit, clock generator, and digital circuit with a 1.2 V power supply are 27 mW, 18 mW, and 4 mW, respectively. The reference buffers are provided externally and their power is excluded. The FoM, defined as $\mathrm{Power}/(2^{\mathrm{ENOB}} \times Fs)$, is 1.24 pJ/conv.-step at 500 MHz input frequency. The highest operating conversion rate of this work is 1.2 GS/s at 1.4 V voltage supply. With the Nyquist rate input at 1.2 GS/s, the SNDR, SNR, and SFDR are 31.4 dB, 33.0 dB, and 39.6 dB, respectively. A summary of the measured performance is given in Table I. A comparison table of the low-power GS/s range ADCs in recent years is presented in Table II.

V. CONCLUSION

Due to the limitations of closed-loop MDAC bandwidth, it is challenging to design a high-speed two-step ADC. With

TABLE II
COMPARISON LOW POWER GS/S RANGE ADCS

Author/year	Core Architecture	number of channels	Tech. (μm)	Fs (GS/s)	DNL/INL (LSB)	SNDR (dB) F_{IN}@ Fs/2	Power (mW)	FoM (pJ/C.S.)	Calibration
Figueiredo'06[6]	Subranging	2	0.09	1	0.22/0.28	33.8	55	1.37	Yes
Lien'08 [7]	Subranging	1	0.09	1	0.35/0.61	33.2	30	0.80	Yes
Cao'08[9]	SAR	2	0.13	1.25	-	32.0 (450Mhz)	32	0.79	Yes
Gupta'06[14]	Pipeline	8	0.13	1	0.7/2.0	52.0 (400Mhz)	250	0.77	Yes
Hsu'07[15]	Pipeline	4	0.09	1.1	0.36/0.46	36.1 (400Mhz)	92	1.60	No
Verbruggen'08 [16]	Folding	1	0.09	1.75	0.29/0.28	27.6	2.2	0.064	Yes
Deguchi' 08 [17]	Flash	1	0.09	3.5	0.50/0.96	31.0	98	0.95	No
This Work	Two-Step	2	0.13	1	0.28/0.30	33.7	49	1.24	No

time-interleaving, timing rearrangement, self-timing, and reduced OPAMP swing and loading parasitic capacitance, this work demonstrates that it is possible to operate the closed-loop two-step architecture at gigahertz range. The 6-bit 1-GS/s ADC without calibration is realized in 0.13-μm CMOS process and only occupied 0.16 mm^2. The power consumption is 49 mW while operating at 1 GS/s. Compared to other types of ADCs, the proposed ADC is an attractive architecture for low power and high data rate systems.

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Hung-Wei Chen (S'07) was born in Taipei, Taiwan, in 1978. He received the B.A.Sc. degree from the University of Toronto, Canada, in 2001, and the M.S. degree from National Taiwan University in 2006. He is currently pursuing the Ph.D. degree in the Graduate Institute of Electronics Engineering, National Taiwan University.

He is a co-founder of Hycon Technology Inc., Taipei County, Taiwan. His research interests are low-power ADCs, and mixed-signal integrated circuits.

I-Ching Chen was born in Taiwan in January 1982. He received the B.S.E.E. degree from National Tsing Hua University, Taiwan, in 2004, and the M.S. degree in electrical engineering from National Taiwan University, Taipei, Taiwan, in 2007.

Since 2008, he has been with Mstar Semiconductor, Inc, Taiwan, where he is involved in the CMOS mixed-signal circuit design for data conversion and signal processing. His research interests are high-speed and low-power ADCs.

Huan-Chieh Tseng received the B.S. degrees in electrical engineering from National Central University, Taoyuan, Taiwan, in 2005, and the M.S. degree in graduate institute of electronics engineering from National Taiwan University, Taipei, Taiwan, in 2008.

He is currently a design engineer with Mobile Devices, Inc., Hsinchu, Taiwan. His current research interest focuses on analog-to-digital converter design.

Hsin-Shu Chen (S'94–M'01) received B.S. degree in electrical engineering from National Taiwan University, Taiwan, in 1989, and the M.S. degree from the University of California at Los Angeles in 1992. He received the Ph.D. degree from the University of Illinois at Urbana-Champaign (UIUC) in 2001.

He was a full-time teaching assistant with the Department of Electrical Engineering at National Taiwan University from 1989 to 1990. From 1992 to 1993 he was with LinCom Corporation, Los Angeles, CA, where he was involved in satellite communication system design and firmware design for spread spectrum cordless phone. From 1994 to 1996, he was a graduate research assistant in the Coordinated Science Laboratory of the Department of Electrical and Computer Engineering at the University of Illinois at Urbana-Champaign, concentrating on the design of analog-to-digital converters. From 1996 to 2002, he was with Intersil Corporation, Melbourne, FL, as a data converter design engineer. From 2002 to 2003, he was with Maxim Integrated Products Inc. Melbourne Design Center as a mixed-signal circuit designer. Since 2003, he has been an Assistant Professor in the Department of Electrical Engineering, National Taiwan University, Taipei, Taiwan. His current research interests are low-power, high-speed mixed-signal integrated circuits.

Dr. Chen has served as an Associate Editor of IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II: EXPRESS BRIEFS since 2008.