4.3 A 1.8V 1.0GS/s 10b Self-Calibrating Unified-Folding-Interpolating ADC with 9.1 ENOB at Nyquist Frequency

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An advance in folding-interpolating ADCs is presented that simplifies their extension to higher resolution by building the converter out of identical but scaled pipelined cascaded folding stages. The limitation of the classical folding architecture [1] is the separate coarse channel to determine which fold an input signal is in. Higher-resolution ADCs benefit from a higher order of folding, which results in more closely spaced folds and makes the alignment between this "fine" channel and the "coarse" channel increasingly difficult due to offset and settling mismatch. In this paper we eliminate this separate coarse channel using instead a single "unified" set of cascaded folding stages, in which each folding stage acts as the coarse channel for the following folding stage. This extends the work of [2] where the coarse channel is distributed and [3] where the cascaded folding stages are pipelined. Our approach is demonstrated in a dual 1.8V 1.0GS/s 10b ADC that achieves ±0.2 LSB DNL and 9.1 ENOB at Nyquist while consuming 1.2W/channel.

Folding-interpolating ADCs are well suited for high-speed conversion rates, due to their flash-like front-end architecture and low number of comparators that results from folding the transfer curve such that one comparator can be used to detect multiple levels. However, the information of which fold corresponds to the input signal V_{IN}, is lost. To date this information has been obtained by parallel coarse channels, which in addition to adding power and loading, require careful alignment between the coarse and fine channels.

Figure 4.3.1 shows only one channel of the interleaved-by-2 unified-folding-interpolating ADC. The input MUX prior to the input buffer allows the automatic application of on-chip generated reference voltages during the self-calibration of the amplifier offsets, especially important in this CMOS design. The technique is similar to our previous work on an 8b ADC [4], but in this case the offset calibration is expanded to include up to amp 3 in Fig. 4.3.1. After the open-loop track-and-hold, the cascaded amps 0 through 6 have embedded comparators that are decoded and combined with the other interleaved channel to send the LVDS output at clock speed, running at 1 Gb/s for each bit.

The main focus of this work is the analog channel. Compared to previous work (including our 8b folding ADC with folding-order k=9 in [4]) the order of folding is extremely high ($k=3^6=729$). Therefore, pipelining is added in the folding stages to allow more time for the amplifier signals to settle [3]. The need for distinct coarse channels is eliminated by embedding comparators at each of the 6 folding-interpolating stages, as shown in Fig. 4.3.2, which is a simplified schematic of 3 of the 6 identical (but scaled) differential cascaded amplifier stages used in this design. Each stage folds by-3 using cross-connected differential pairs, which is followed by interpolation-by-3, so that the number of input and output signals, 27, remains constant.

Three comparators are equally spaced inside each amplifier stage on existing/propagated signals, such that their crossing points are folded into the complete analog channel transfer curve as shown. By knowing the exact position of V_{IN} in stage N-1, the particular fold for stage N is localized without a separate coarse ADC. This is extremely important for the later stages, where the high folding order makes the absolute position of V_{IN} relative to the many folds very difficult to determine. The position of V_{IN} in stage N-1 is in turn iteratively determined by the previous stages. Furthermore, comparator 2 of each stage is actually redundant with comparator 1, 2, or 3 of the previous stage. Thus, while stage N-1 localizes the fold for stage N, error-correction logic in the encoder uses comparator 2's output of the more highly gained stage N to correct stage N-1's decision, resulting in excellent differential linearity and complete sparkle suppression while requiring only relaxed comparator accuracy, since the RTI gain at the final comparators exceeds 5000.

Embedding comparators also reduces their total number. In our previous 8b ADC, there are 43 comparators; for this 10b design there are only 20 comparators (3 for each folding stage, plus 2 at stage 0, the non-folded first flash stage). This cascaded architecture is most efficient for folding-by-3, producing a base-3 result. The encoder complexity is high due to the error correction, which can ripple from the last stage back to the first, and the required base-3-to-base-2 conversion.

Figure 4.3.3 shows the DNL (<±0.2 LSB) and INL (≤±0.5 LSB) at 1.0GS/s for just the I-channel with a 97.77MHz sine-wave input extracted with a least-squares fit. In addition, INL is plotted for both the I and Q channel with calibration disabled. The uncalibrated INL curve is typically <±6 LSB.

Figure 4.3.4 plots ENOB versus input frequency for both the I and Q channels, starting at 9.2 ENOB, achieving nearly 9.1 ENOB simultaneously at Nyquist, and maintaining nearly 8.8 ENOB up to a 1.0GHz input. The remarkably small SNR roll-off versus input frequency (from 57.4dBc @ 100MHz to 55.5dBc @ 1GHz) results from the extremely low clock jitter, which we estimate as $<180fs_{rms}$ for the combined contributions of the clock and input sources and ADC itself, using the equation:

$$SNR\_MAX\ (dB) = -20\ \log_{10}(2\pi\ f_{IN}\ t_{J,RMS}),$$

and attributing all of the SNR degradation at f_{IN} = 1GHz to the effect of the rms aperture jitter, $t_{J,RMS}$. Compared to earlier 8b work [4], the clock path is fully redesigned in CML to improve the PSRR, since even dedicated supplies are rarely truly clean. For this same figure we plot the most recent ≥8b ADCs in the GS/s range. At 1.0GHz input this 10b ADC's performance is more than one ENOB above prior art. The spectrum of just the I-channel FFT is shown for 100MHz and 900MHz input in Fig. 4.3.5.

Figure 4.3.6 shows a performance summary at 1.0GS/s and 1.8V. The data presented here is taken from a packaged-and-socketed part with both channels powered-up and I&Q data taken simultaneously. Data is captured at full speed (no decimation), without any post-processing or off-chip correction. All spectral specifications are taken with respect to the carrier, not full scale, and measured at -0.3dBFS. The total power with an active input, including the LVDS drivers, is 1.26W/channel and with a DC input it is 1.20 W/channel. A die micrograph of the ADC is shown in Fig. 4.3.7. Because top metal obscures most structures, the circuit blocks are indicated.

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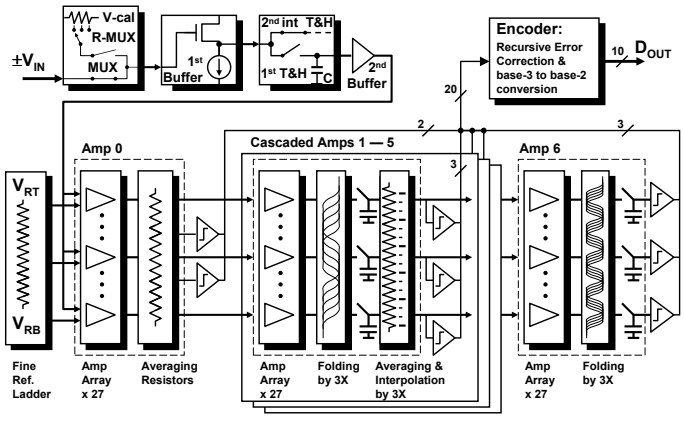

Figure 4.3.1: Block diagram of the self-calibrating Unified-Folding-Interpolating ADC showing only 1st interleaved channel.

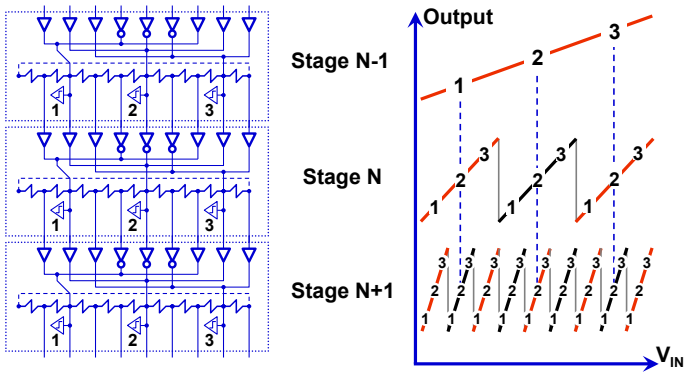

Figure 4.3.2: The order of folding at each stage (N) of this ADC is k = 3^N (N=1 to 6).

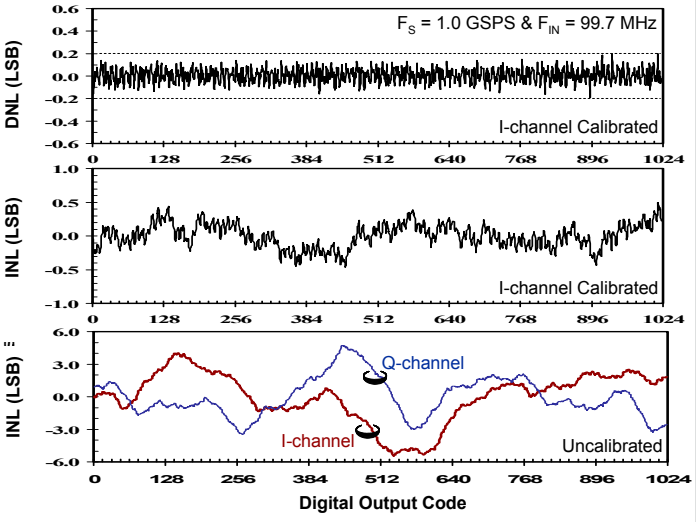

Figure 4.3.3: Measured 4M-point DNL and INL curves at 1.0GS/s.

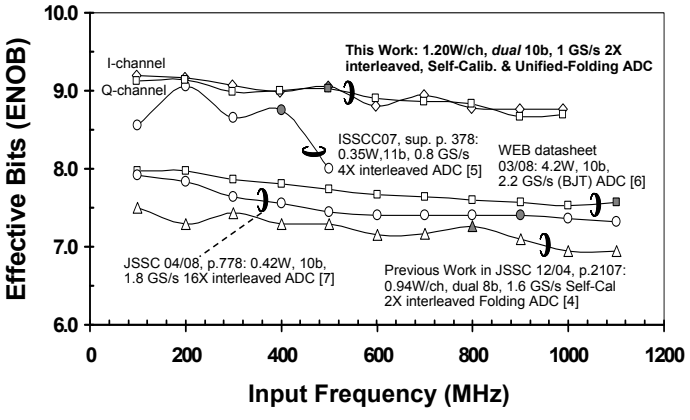

Figure 4.3.4: Measured ENOB versus f_{IN} for this and comparative work. Filled symbol shows the Nyquist frequency.

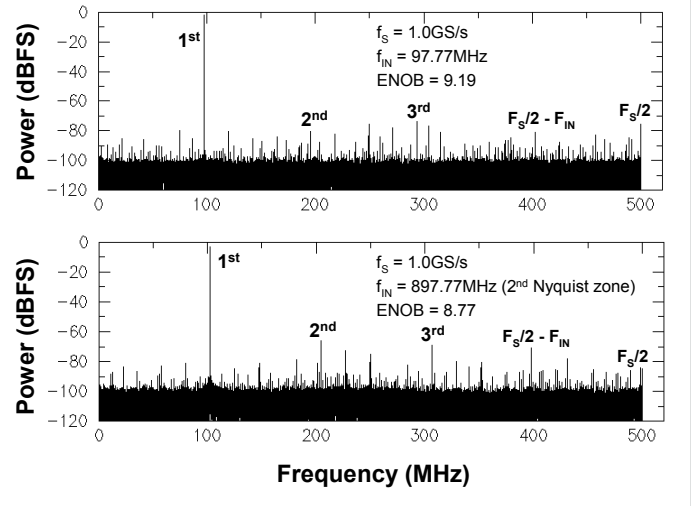

Figure 4.3.5: Measured 128K-point FFT spectra at 1.0GS/s for f_{IN} = 97.77MHz and 897.77MHz.

	I-Channel	Q-channel
Sample Rate f_S	1.0GS/s	
Resolution	10b	
Max DNL	+0.19 / -0.19 LSB	+0.18 / -0.20 LSB
Max INL	+0.50 / -0.46 LSB	+0.42 / -0.72 LSB
SNR @ f_{IN} = 497.77MHz	56.9dB	56.5dB
SFDR @ f_{IN} = 497.77MHz	66.3dB (H3)	68.6dB (H3)
THD @ f_{IN} = 497.77MHz	- 65.4dB	- 67.6dB
ENOB @ f_{IN} = 497.77MHz	9.06	9.04
Jitter @ f_{IN} = 997.77MHz	<180fs$_{rms}$	<170fs$_{rms}$
ENOB @ f_{IN} = 497.77MHz	9.09 for I-channel with Q-input = DC	
I/Q X-talk @ f_{IN} ≤ 900MHz	≤ -70dB	
Input –3dB Bandwidth	3GHz	
Input Range	±410mV differential	
Input Capacitance	~2pF	
Input Termination	50Ω (100Ω differential)	
Single Supply	1.8V	
Power @ f_{IN} = 97.77MHz	1.26W/channel	
Power @ f_{IN} = DC	1.20W/channel	
ADC die area	49mm^2 (for dual ADC, pad-limited)	
Package	292-pin BGA	
Technology	0.18µm Triple-well 1P6M CMOS No capacitor module nor dual-gate process	

Figure 4.3.6: ADC performance summary for simultaneously captured data.

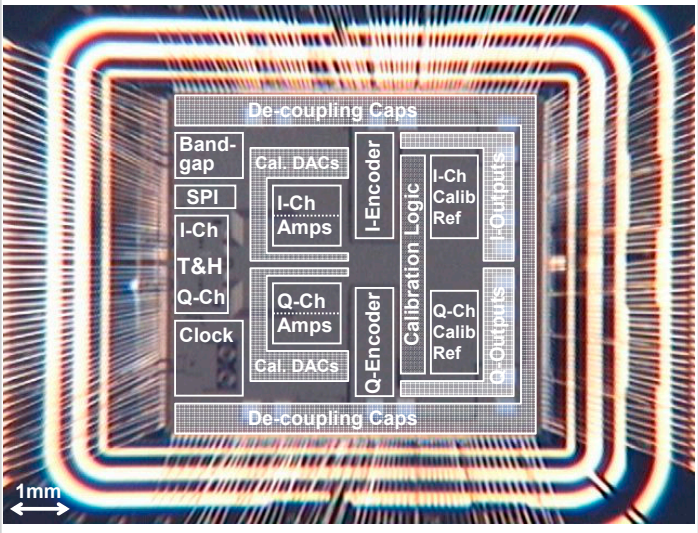

Figure 4.3.7: Die micrograph of dual 10b 1GS/s ADC in 292-pin BGA.

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