Cascaded voting process for flash ADC with interpolating scheme

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A 3-stage cascaded voting process is proposed for flash analogue-to-digital converters (ADCs) with an interpolation factor of 4 to eliminate the consecutive bubbles at the output nodes of the comparator array. Compared to the conventional 3-input voting process, the proposed process completely eliminates up to seven consecutive bubbles without hardware overhead, if the preamplifier output is assumed to have a single bubble at most. The proposed voting process is evaluated by 7-bit 1 GS/s CMOS flash ADCs with an interpolation factor of 4 which is designed by a 0.13 μm CMOS process with 1.2 V supply.

Introduction: For high speed analogue-to-digital converters (ADCs), a flash ADC architecture using the interpolation scheme is widely used to reduce the hardware and the input capacitance. To implement this architecture, two approaches have been studied. The resistor averaging scheme [1] is applied to output nodes of preamplifiers for the input stage of ADCs, and the gate-width-weighted transistors [2] are utilised at an input transistor of comparators to reduce the power consumption. Also, a digital encoder block in the flash ADC includes a voter block to suppress bubble errors caused by input offset voltage and meta-stability of preamplifiers and comparators in the thermometer code corresponding to the output of comparators [1]. To increase further the sampling rate and input bandwidth of flash ADCs, the preamplifier requires small input transistors for lower input and junction capacitance. However, this approach may lead to the large offset error which is not removed by the resistor average scheme since the input random offset voltage is inversely proportional to the square root of the transistor gate area [1]. Furthermore, the interpolation scheme without the resistor averaging scheme [2] is greatly affected by the offset error of preamplifiers. Actually, when the interpolation scheme with a factor of two or above is used at the preamplifier output, it may generate consecutive bubbles at the interpolated output even though only a single bubble at the preamplifier output exists. While the conventional 3-input majority voter in the digital encoder block can remove an isolated bubble, it cannot remove consecutive bubbles. Although the 5-input majority voter can completely eliminate up to 2 consecutive bubbles, it requires the twice gate count of the 3-input majority voter.

In this Letter, a 3-stage cascaded voting scheme is proposed to completely eliminate up to seven consecutive bubbles without any hardware overhead, when the preamplifier output has a single bubble at most.

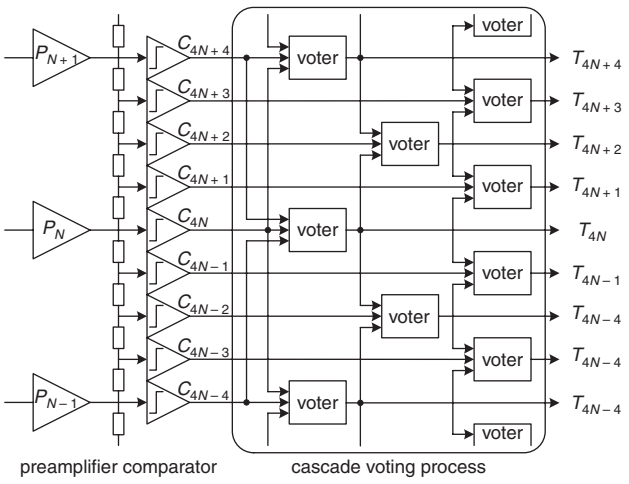

Fig. 1 *3-stage cascaded voting process*

Circuit description: Fig. 1 shows the circuits performing the proposed 3-stage cascaded voting process in the flash ADC with the resistor averaging scheme for an interpolation factor of 4. The voting process is performed in three stages by using the conventional 3-input majority voters implemented with static logic gates. The partial thermometer codes ($\cdots$, C_{4N+4}, C_{4N}, C_{4N-4}, $\cdots$) are the comparator output codes corresponding to the direct outputs from the preamplifier. It is assumed that there is only a single bubble at most in these partial codes ($\cdots$, C_{4N+4}, C_{4N}, C_{4N-4}, $\cdots$). Among the entire thermometer codes ($\cdots$, C_{4N+4}, C_{4N+3}, C_{4N+2}, C_{4N+1}, C_{4N}, C_{4N-1}, C_{4N-2}, C_{4N-3}, C_{4N-4}, $\cdots$), the above-mentioned partial thermometer codes have the largest probability of bubble errors due to the use of interpolation. So, the codes, $\cdots$, C_{4N+4}, C_{4N}, C_{4N-4}, $\cdots$ are voted first at the first stage. This generates the bubble-free codes, $\cdots$, T_{4N+4}, T_{4N}, T_{4N-4}, $\cdots$. After the first stage voting, the second stage voting was performed for the corrected codes ($\cdots$, T_{4N+4}, T_{4N}, T_{4N-4}, $\cdots$) and the interpolated codes ($\cdots$, C_{4N+2}, C_{4N-2}, $\cdots$) from the mid-point of the interpolation resistor string. This second stage voting generates the bubble-free codes, $\cdots$, T_{4N+2}, T_{4N-2}, $\cdots$, since two out of three inputs of all the second stage voters are bubble-free. Similarly, the third stage voting generates the bubble-free codes, $\cdots$, T_{4N+3}, T_{4N+1}, T_{4N-1}, T_{4N-3}, $\cdots$. Therefore, this 3-stage cascaded voting process completely eliminates all the bubbles in the resultant codes, as long as there are no consecutive bubbles in the original partial codes ($\cdots$, C_{4N+4}, C_{4N}, C_{4N-4}, $\cdots$).

When only a single bubble in the partial codes ($\cdots$, C_{4N+4}, C_{4N}, C_{4N-4}, $\cdots$) of the flash ADC with an interpolation factor of 4 as shown in Fig. 1 exists, the maximum number of consecutive bubbles caused by the offset voltage of preamplifiers and comparators in the entire code is seven. Figs 2*a* and *b* show the examples of removing these bubbles by the proposed cascaded voting process when the number of consecutive bubbles is four and seven, respectively. The proposed 3-stage cascaded voting process eliminates the bubbles completely. Since only a single 3-input voter is assigned to each comparator output in the proposed voting scheme, this scheme does not cause any hardware increase in comparison with the conventional 3-input voting scheme.

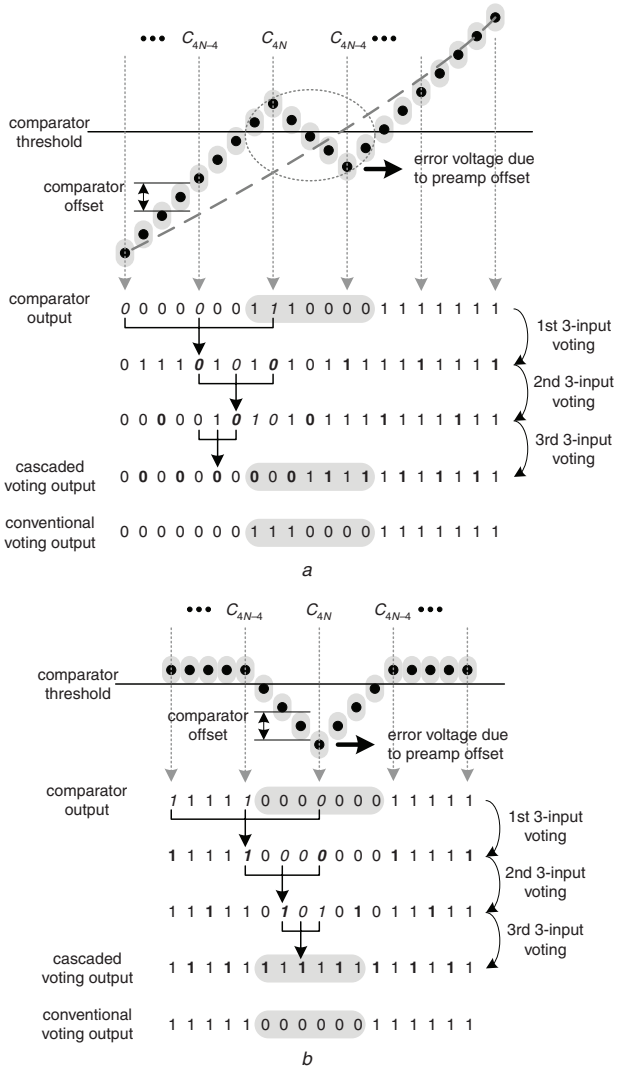

Fig. 2 *Examples of cascade voting process*

a Voting process for bubbles in transition region
b Voting process for maximum votable consecutive bubbles

If two bubbles in the input codes ($\cdots$, C_{4N+4}, C_{4N}, C_{4N-4}, $\cdots$) for the first voting stage in the flash ADC with an interpolation factor of 4 exist, the 5-input majority voters for only the first stage voter can be utilised. In this case, the maximum number of removable consecutive bubbles is eleven. However, the proposed voting process can result in increased latency by using the pipeline scheme in a digital encoder block as the sampling rate of ADCs increases.

Simulation results: To verify the effect of the proposed 3-stage cascaded voting process, two 1.2 V 7-bit 1 GS/s CMOS flash ADCs with an interpolation factor of 4 were designed by using a 0.13 μm CMOS process. The first designed ADC used the resistor averaging scheme [1] and the second ADC was designed by using gate-width-weighted transistors [2] for comparator input. These ADCs have the input range of 400 mV and the input voltage resolution of 12.5 mV because of 32 preamplifiers. According to a dynamic Monte-Carlo simulation of input-referred random offset, the offset voltages of the preamplifier and the comparator are 20 mV and 27 mV, respectively. Fig. 3 shows the simulated SNDR (signal-to-noise and distortion ratio) against the analogue input frequency at the sampling rate of 1 GS/s, where the SNDR of the first and second ADC with the proposed voting process increased by 1.36 and 1.95 dB, respectively, at the input frequency of 305 MHz

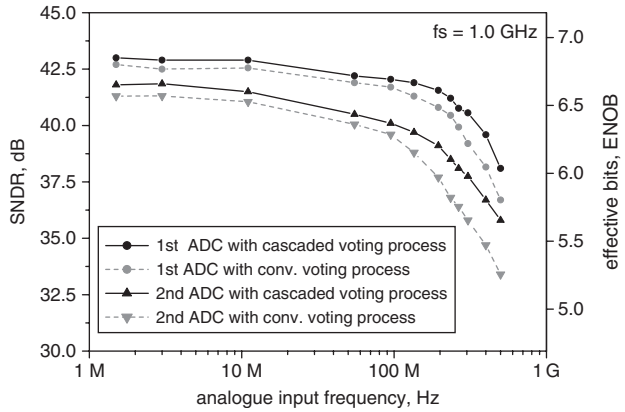

Fig. 3 *SNDR against input frequency at 1 GS/s*

Conclusion: A 3-stage cascaded voting process was proposed for flash ADCs with an interpolation factor of 4 to eliminate up to seven consecutive bubbles subject to, at most, a single bubble at the preamplifier output. The circuit for this voting process consists of the conventional 3-input majority voters without a hardware increase compared to the conventional 3-input voting process. The proposed voting process improved the dynamic performance of two 1.2 V 7-bit 1 GS/s CMOS flash ADCs designed using a 0.13 μm CMOS process.

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