A 5GS/s Voltage-to-Time Converter in 90nm CMOS

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***Abstract*— A voltage-to-time converter (VTC) is presented for use in a time-based analog-to-digital converter (ADC). The converter runs with a 5 GHz input clock to provide a maximum conversion rate of 5 GS/s. A novel architecture enables the VTC to provide an adjustable linear delay versus input voltage characteristic. The circuit is realized in a 90nm CMOS process. After calibration, the converter achieves better than 3.7 effective bits for input frequencies up to 1.75 GHz, making it suitable for use in a time-based ADC with up to 4-bit resolution.**

I. Introduction

High speed, low power analog-to-digital converters (ADCs) are an important area of research with applications in many areas including data storage and wireless receivers. In particular, the prospect of direct sampling receivers for GHz frequency communications systems such as ultra-wideband (UWB) is attractive [1]. At sampling rates above 1 GS/s, the flash ADC architecture is normally used for low power, moderate resolution applications [2].

A promising alternative to the traditional flash architecture is a time-based architecture that exploits digital CMOS technology to reduce power consumption and chip area [3]. In the time-based architecture, the conversion from an analog signal to a digital representation consists of two stages. The first stage, known as a voltage-to-time converter (VTC), produces a series of delayed pulses. The delay on each pulse is proportional to the analog input at the moment the pulse was created. A VTC can also be referred to as either a pulse position modulator (PPM) or pulse width modulator (PWM), depending on whether the delay is applied to one or both edges of the input clock pulses. The second stage, called a time-to-digital converter (TDC), measures the delays and produces a digital output corresponding to each pulse [3], [4]. The result is a time-based ADC, as illustrated in Fig. 1.

As CMOS feature size continues to decrease, traditional ADC architectures experience SNR degradation due to supply voltage reduction. Time-based signals, however, show an improvement in SNR due to higher switching speeds [1]. Although VTC performance is still limited by reductions in supply voltage due to the necessity of processing an input voltage signal, the TDC is not affected by this issue and can be designed to take full advantage of CMOS switching speed.

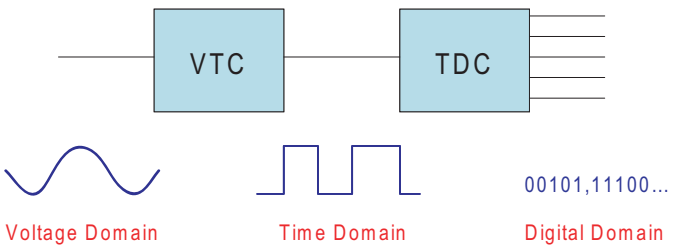

Fig. 1. Time-based ADC

Thus one of the key challenges in time-based ADC design is to produce a low power VTC with good linearity characteristics. Performance must be consistent across process and temperature variations. This paper describes a VTC designed for a 5 GS/s 3-bit ADC. The VTC takes in a single-ended analog input and produces a linear delay characteristic ranging from 0-50ps. The VTC was designed alongside a corresponding TDC, which will be the subject of a future publication.

Previously published VTCs typically operate at sampling rates far below 1 GS/s. For speeds in the MS/s range and below, VTCs based on linear voltage ramps and comparators can achieve high accuracy [5]. VTCs based on current-starved inverters have been reported operating from the low MS/s up to as high as 500 MS/s [6], [7]. The VTC in this work uses a variation of the starved inverter architecture to reach 5 GS/s.

II. Circuit Details

A. VTC Architecture

Figure 2 shows the block-level architecture for the VTC. The system is made up of two time-interleaved VTC channels. Each channel takes in the same analog input but is clocked independently with a 25% duty cycle clock, as shown. Each channel is therefore responsible for delaying every second clock pulse of the full 5 GHz input clock. The outputs of the channels are combined using OR gates to produce the desired 5 GHz output clock and data signals. All clocks and reset signals for both channels (including the sampling clock) are generated internally from a single input clock. Each channel requires DC bias voltages for calibration over process, voltage and temperature variations. These calibration voltages can be supplied by a set of 5-bit programmable digital-to-analog converters (DACs).

A more detailed view of channel A is shown in Fig. 3. Each channel produces two outputs: an output signal consisting of pulses delayed proportionally to the input, and an output clock with a fixed delay independent of the input. The time delay between corresponding pulses on the output signal and output clock ranges from 0-50ps over the full range of analog inputs (100mV span). This delay represents a sampled value of the

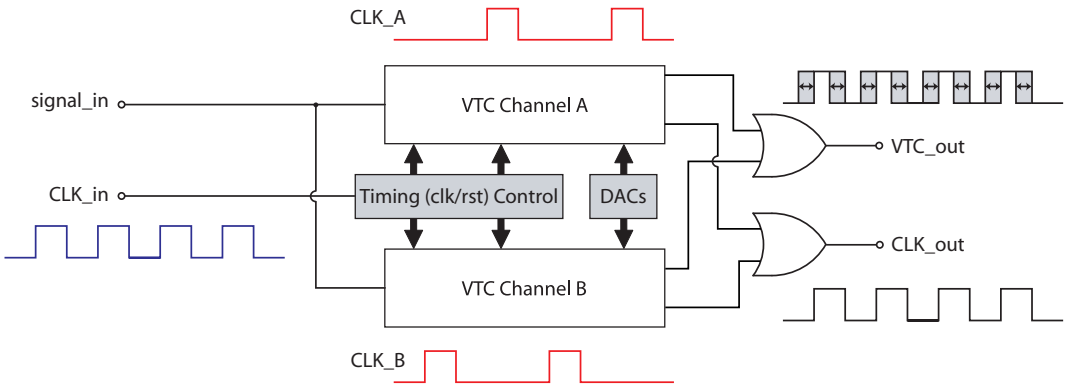

Fig. 2. Top-level VTC block diagram

input signal in the time domain, and is converted to a digital value in the following stage (the TDC).

Both the output signal and output clock are produced by an identical set of two VTC cores in series. Each VTC core produces a delay of 0-25 ps so it is necessary to cascade two to provide the full output range. For the output signal path, the same sampled signal is provided to both VTC cores by a track & hold circuit. The simple passive track & hold circuit is shown in Fig. 4. It consists of an NMOS switch followed by a hold capacitor, with a dummy NMOS device to balance charge injection.

The input to the VTC cores in the constant delay path is a fixed DC value that can be provided by programmable DACs to ensure that the clock and data pulses are aligned correctly.

B. VTC Core

The circuit for the VTC core is shown in Fig. 5. The circuit consists of 6 CMOS inverters, two of which are current starved to control the delay. The current-starved inverters have starving devices between the NMOS transistor and ground in order to delay the falling output edge without impacting the rising output edge. Since the inputs to the two current-starved inverters are separated by three inversions, they act on opposite edges of the signal and thus do not have an additive effect. Delaying both edges is necessary so that the pulse width of the output remains constant as the delay varies. In the figure, the non-starved inverters are represented by simple digital symbols to reduce clutter. Focusing on the first current-starved inverter in the figure, it can be seen that M1 and M2 make up a standard CMOS inverter, and M3 is an NMOS starving device controlled by the input. The bias voltage for the gate of M3 (and all the starving devices in the VTC) is a DC level which can be provided by a programmable DAC.

Unique to this design is NMOS device M4, which is connected as a CMOS capacitor. The capacitance of M4 can be tuned via the DC signal V_{cap}, which can also be provided by a programmable DAC. The motivation for including this tunable capacitance is that the total capacitance at the source terminal of M4 was found to be the key determinant of switching delay characteristics. Adjusting this capacitance effectively changes the gain of the VTC (gain in this case is defined as the output delay added per unit of input voltage). The delay is adjusted so that each starved inverter provides 0-25ps over the input range of 100mV.

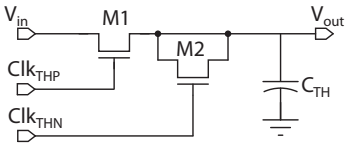

Fig. 4. Passive track & hold circuit

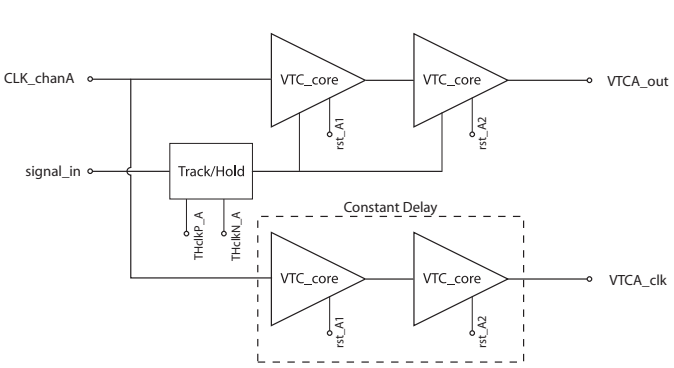

Fig. 3. Block diagram of a single VTC channel

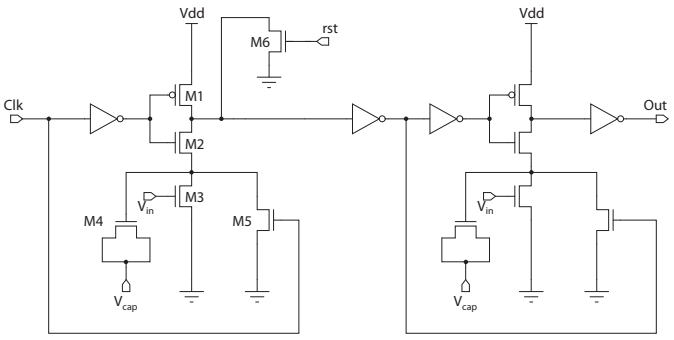

Fig. 5. VTC core schematic

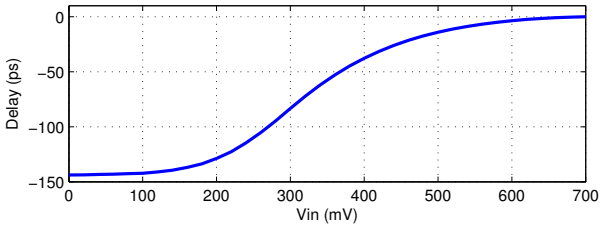

Fig. 6. Simulated VTC delay over a wide DC input bias range

Finally, devices M5 and M6 are very weak NMOS switches which are toggled every clock cycle to ensure that the nodes to which they are connected fully discharge after each conversion. This minimizes memory effects in the converter.

III. Simulated Results

A. Calibration and Linearity

Unlike previous linear VTC's [6] in which the biasing had to be manually adjusted to approximate a linear 'delay versus input' characteristic, the VTC in this work is designed to be inherently linear. The idea for accomplishing this was to create a circuit with high gain and restrict the input to a small range, similar to a small signal approximation often used in circuit analysis. The biasing is then used to adjust the gain to the correct value.

To provide further insight into the effect of biasing for this circuit, Fig. 6 shows the delay variation over a large DC input range. The DC input corresponds to the bias voltage on the gates of the starving devices in Fig. 5, with no AC input. It should be noted that the input variation shown in this graph is much larger than the specified input range of 100mV.

The appearance of the curve can be explained as follows: For low input levels, M3 in the VTC core is not providing any meaningful current, and the switching is accomplished by way of stored charge on the gate of the CMOS capacitor, with assistance from the weak M5 switch. As a result, the delay is relatively large and the voltage on the gate of M3 has little effect. Conversely, for very high input levels M3 provides a low resistance path, allowing the inverter to draw as much current as it needs to switch at the maximum rate. Between these two plateaus is the desired high gain region. During calibration, the DC bias voltage is chosen so that the input will swing around the center of this region, providing maximum gain and therefore maximum linearity.

The V_{cap} bias voltage is then set to adjust the gain to achieve the desired delay range. The third and final calibration value is the input to the constant-delay VTC blocks for the output clock path. This value is chosen to ensure that the delay between the clock and data outputs is zero for the maximum input voltage.

The circuit was simulated over process and temperature. The calibration procedure was performed manually for each condition. After calibration, the circuit was confirmed to operate with the correct range for all process corners and for temperatures between $0 - 75\,^{\circ}\mathrm{C}$.

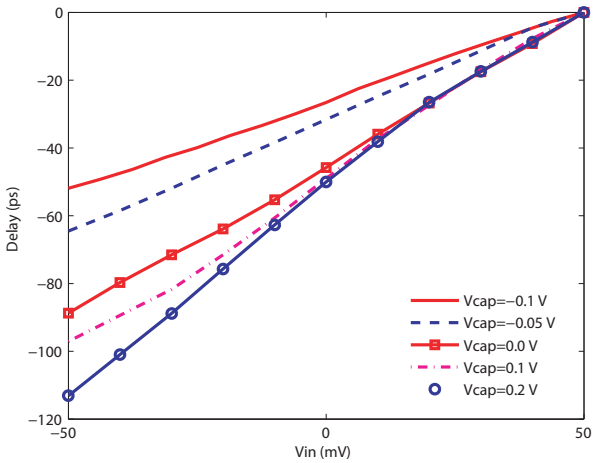

Fig. 7. Measured delay curves for different V_{cap} tuning voltages

IV. Measurements

The circuit was fabricated in an STMicroelectronics 90nm CMOS process. For this proof-of-concept run, the programmable DAC's were not included, so the DC bias voltages were provided from off-chip through bond pads. The fabricated IC is shown in Fig. 10. The IC contains a full ADC consisting of a VTC and TDC in series, as well as standalone versions of the VTC and TDC that are testable individually. The test results presented here are taken from the standalone VTC. The design is pad-limited, with an active area of 0.0068 mm^2. It was not possible to measure the power consumption of the VTC on its own, but extracted simulations predict a maximum current draw over all corners of 3.6 mA with the track & hold enabled, or 2.7 mA without it. The supply voltage is 1V.

The delay versus input voltage plot for the measured VTC, with a 5GHz clock and DC inputs, is shown in Fig. 7. Optimal bias conditions were selected using a manual calibration procedure. To illustrate the effect of biasing, delay curves are shown for various V_{cap} voltages. With optimal biasing the curve exhibits a total range of 53.3ps which is well within the adjustable range of the TDC, specified as 40-65ps. Fig. 8 shows the waveforms measured at the VTC output. An automated calibration routine making use of a microcontroller to set bias voltages using DACs is planned for a subsequent version of the chip.

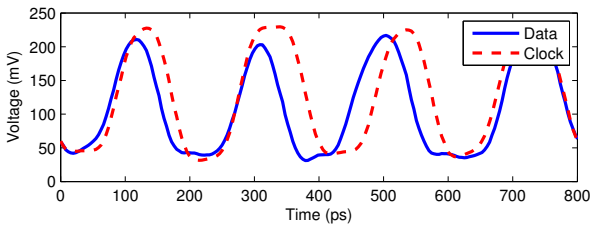

Fig. 8. Clock and data output waveforms with a 1.25GHz sinusoidal input, captured with an HP 54750A digitizing oscilloscope

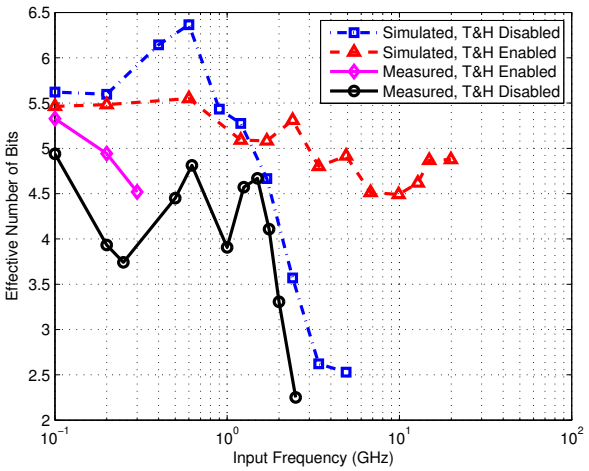

Fig. 9. Measured and simulated ENOB at 5 GS/s, with and without track & hold

In order to quantify the performance of the VTC, the effective number of bits (ENOB) was measured. The ENOB reflects the amount of noise and distortion introduced into the signal by the circuit. The standard method for computing the ENOB for an ADC is to excite the input, record a large number of data samples, and then calculate the signal-to-noise-and-distortion-ratio (SNDR) in the frequency domain. The ENOB is then found using the formula

$$ENOB = \frac{SNDR(dB) - 1.76}{6.02}. \quad (1)$$

To estimate the ENOB for the VTC, the following modified procedure was used due to the high clock rate and the time-based nature of the signal. After exciting the input, the output waveforms were captured using an HP 54750A digital sampling oscilloscope with 50GHz bandwidth. This instrument builds the waveform by taking samples across multiple clock periods, so it can only image waveforms that repeat periodically. It is therefore not possible to image a single output pulse from the VTC; rather the test must be set up so that the input sinusoid is synchronized with the clock, causing the output to repeat at regular intervals (every 4 pulses, every 25 pulses, etc). The implication is that since the delay is calculated based on multiple waveforms, dynamic noise and jitter will tend to average out of the measurement. The results should therefore be considered as a signal-to-distortion ratio (SDR), rather than the usual SNDR. Although the ENOB calculated from the SDR does not include information about the noise performance, it is still an important measure to characterize the VTC linearity. Full characterization will be possible when the full ADC (VTC and TDC) is tested.

Fig. 9 shows the ENOB measured as described above. With the track & hold disabled, the circuit achieves the equivalent of 4.9 bits for frequencies of 100 MHz and below, and remains above 3.7 bits up to 1.75 GHz. The sharp dropoff at higher frequencies occurs because the input is changing significantly during the conversion. With the track & hold enabled the circuit fails with inputs above 300 MHz due to a layout error.

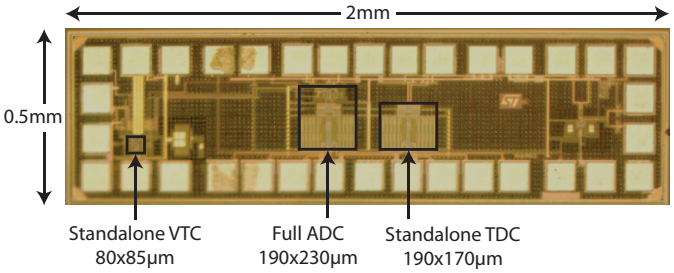

Fig. 10. IC photograph

The simulated data is also shown in Fig. 9, with and without the track & hold. It can be seen that enabling the track & hold prevents the ENOB from dropping off, and in fact allows the circuit to remain accurate well above the Nyquist frequency, up to 10 GHz.

V. Conclusion

A linear VTC was designed, fabricated and tested with an operating frequency of 5 GS/s. The linearity was found to exceed 3.7 effective bits with input frequencies up to 1.75 GHz, reaching 4.9 effective bits at low input frequencies. The estimated power consumption during these tests was 3.6 mW. The VTC is intended for use with a TDC as part of a time-based ADC.

Acknowledgment

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