A 3-Bit 2.2V 3.08pJ/Conversion-Step 11GS/s Flash ADC in A 0.12μm SiGe BiCMOS Technology

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***Abstract* — A 3-bit ADC for X-band applications that can work at a sampling rate of 11 GS/s is presented in this paper. Current comparators are used to achieve the high sampling rate of 11 GHz at X-band. A 3-bit current-steering DAC is also designed for testing the high-speed ADC. The ADC-DAC RFIC is implemented in a 0.12 μm SiGe technology and occupies a core area of 1.0 x 0.8 mm^2. The ADC can operate with a FOM of 3.08 pJ/conversion-step, consuming 0.22 W power with a 2.2 V power supply. It demonstrates a good performance at X-band sampling rate with the lowest power supply voltage, lowest power consumption, smallest core area and best FOM reported so far. The ADC-DAC RFIC is tested in a 44-pin CLLC package and achieves a peak SFDR of 28 dBc and a peak ENOB of 2.7 bits at 11 GS/s sampling rate.**

***Index Terms* — flash, analog-to-digital converter (ADC), digital-to-analog converter (DAC), low power, low voltage, X-band, current comparator, SiGe, BiCMOS.**

I. Introduction

Analog-to-digital converters (ADC) with X-band frequency sampling rates are critical components for applications such as digital oscilloscopes, waveform recorders and radar signal capture, etc [1]. Meanwhile, the development of modern communication and wireless applications necessitate the next generation receivers to have higher data transmission rates and lower power consumption. By moving the ADC closer to the system front-end, the majority of the processing can be performed in the digital domain [2]. To take advantage of the increasing speed and complication of digital signal processing, ADCs in the above applications are required to be implemented with small area and low power as well as fast sampling rates. Although a 10~20 GS/s 3~4-bit ADC in InP technology [3] and a 40 GS/s 3-bit ADC in SiGe technology [4] have been reported to demonstrate the capability of over 10 GHz sampling speed, their several-watt-order of power consumption, high supply voltage and large die area significantly prevent them from being integrated in a single fully-integrated transceiver chip for X-band frequency applications. In this paper, a 3-bit Flash ADC is presented to demonstrate a good X-band sampling rate performance with the lowest power supply voltage, lowest power consumption, smallest core area and best figure of merit (FOM) in reported X-band ADC designs so far.

The 0.12 μm SiGe HBT technology used for this design is featured with f_t/f_{max} of 210/310 GHz. The flash ADC architecture was chosen to achieve the maximum sampling frequency for the ADC design. The current mode logic (CML) circuits are adopted for digital logic implementations to provide fast switching speed. Finally, low voltage power supply is used to minimize total power consumption and avoid breakdown issues in HBTs and FETs in the technology.

The organization of this paper is as follows: in Section II, the 3-bit ADC architecture and circuit design are discussed. The discussion mainly includes circuit and layout design considerations and trade-offs for ultra-high speed, static and dynamic accuracy, and power consumption. A 3-bit current-steering high speed DAC is also designed for built-in-self-test (BIST) of the ADC function. In Section III, the measurement results of the ADC-DAC chip are be given. Conclusion is drawn in Section IV.

II. Flash ADC Architecture

As shown in Fig. 1, the proposed 3-bit ADC-DAC RFIC is composed of a 3-bit flash ADC and a 3-bit DAC for ADC testing. The ADC contains a 7-level current comparator, thermometer-to-gray decoder and D-flip-flops (DFFs) for retiming and buffering. A current-steering type DAC is used to obtain maximum sampling rate. During operation, the input analog signal is compared with 7 current-mode comparators which are set using 7 successive offset currents representing the 7 quantization threshold levels. Digital outputs can be obtained after thermometer-to-gray decoder and DFFs. The reconstructed analog signal by 3-bit DAC can be directly measured from the using a digital oscilloscope or a spectrum analyzer.

With a 2.2 V low voltage power supply, the CML circuit can only realize two level logic which will prolong the critical signal path and consequently increase inter-stage delay. Gray code is applied to mitigate the low power supply effect and obtain best speed performance by simplifying the decoder logic circuits [5]. With a two level

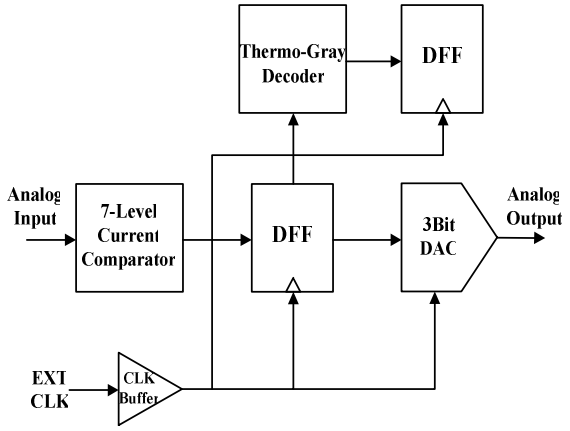

Fig. 1 Simplified block diagram for proposed 3-bit high-speed flash ADC and BIST DAC.

logic CML circuit, the gray decoder can cut the original three-stage logic (counting one gate and one emitter follower as one stage) to two-stage in the longest LSB signal path, compared to the traditional binary decoder. By saving one stage, the compensation circuits for balancing the propagation delay in other signal paths can also be removed so that lower power consumption and higher speed can be simultaneously achieved. Due to the limitation of 2.2 V power supply voltage, the head room for the bottom current source transistor is only about 300 mV. Because of the small amount of headroom, a BJT is not used for the bottom current source. Despite a smaller transconductance compared with the BJT, a FET with large enough width should be used to ensure that it operates in saturation region. Decoupling capacitors are also needed on the gates of some critical current source FETs such as comparators and the DAC output stage.

In flash type ADCs, current comparators convert the received analog input signal to digital outputs by setting different quantization threshold levels [4]. The accuracy and speed of the conversion directly affects almost all of its static and dynamic performance, such as differential nonlinearity (DNL), integral nonlinearity (INL), signal-to-noise (SNR), spurious free dynamic range (SFDR) and effective number of bits (ENOB). Unlike the resistor network used to set up voltage thresholds for conventional ADCs, current-mode comparators using active unit current sources can reduce parasitic RC effects in the crucial signal path during the conversion. As shown in Fig. 2, the current offsets set up by different current sources play the same role as the voltage thresholds in a voltage-mode comparator for quantizing the input signal. Large bias current and emitter degeneration resistors should be used to increase the linearity range [6]. For X-band application, the current comparator circuit needs to be redesigned post layout to take into consideration the parasitic RC effects.

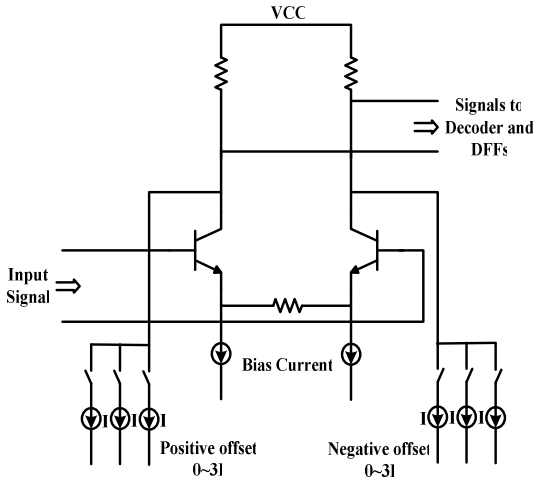

Fig. 2 Current comparator with quantization threshold levels set by the offset current.

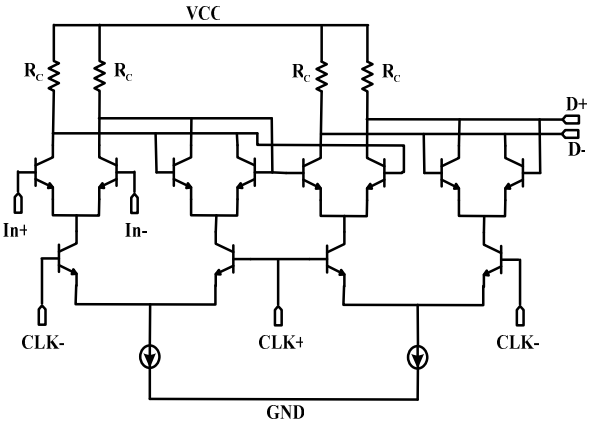

Fig. 3 Schematic for DFF used in this high-speed ADC.

Figure 3 show the topology of the DFF used in this design. Due to the low-voltage design with a 2.2 V power supply, although emitter followers between two-stage D latches are often used to suppress the kickback noise and isolate the unbalanced interference from the succeeding stages [2], they must be removed to provide enough headroom for the following clock input stage to make sure

correct operation of the D latch. In the DFF design, larger bias current and larger HBT devices are used in the second D latch in order to offer better driving strength for the following stages, which also improves the capacitance loading effect at outputs nodes, leading to an increased DFF speed.

III. Implementation and Experimental Results

The 11GS/s 3-bit ADC is implemented in a 0.12 µm SiGe BiCMOS technology, as shown in the chip micrograph in Fig. 4. For an integrated radar application, the ADC chip was embedded in a radar receiver MMIC that includes a 16 GHz RF front-end with an LNA and a mixer. The ADC circuit occupies 0.7 x 0.6 mm^2 die area and the 3-bit DAC takes an area of 0.3 x 0.6 mm^2. Operating at an 11 GS/s sampling rate with a single 2.2 V power supply, the power consumption of the ADC is only 0.22 W. This ADC realizes the lowest power supply voltage, lowest power consumption and smallest core area in all reported X-band ADC designs.

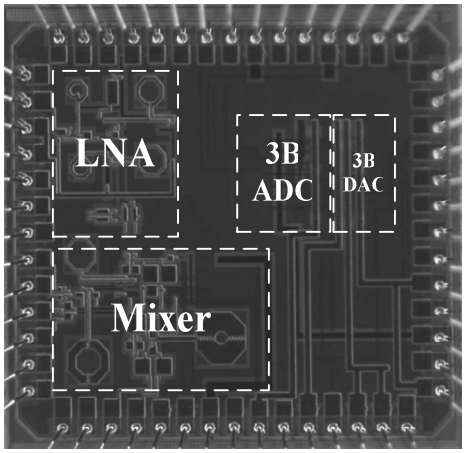

Fig. 4 Microphotograph of the 3-bit 11GS/s flash ADC-DAC RFIC chip.

For X-band testing, a Rogers RO4003 laminate PCB with a loss tangent of less than 0.003 is developed to provide good high frequency performance and temperature stability. At the DAC differential outputs, a 180 degree 3 dB hybrid coupler is used to provide differential-to-single-ended conversion for a spectrum analyzer to test the spectral performance of the overall ADC-DAC RFIC. During the measurement, the SINC roll-off from the DAC reconstruction must be considered to give the accurate results. All measurements were done using CLLC packaged prototypes, while other reported high-speed ADCs [3][4][7] were all tested on wafer, which has less problems associated with the package heat dissipation and bonding wire parasitic effect.

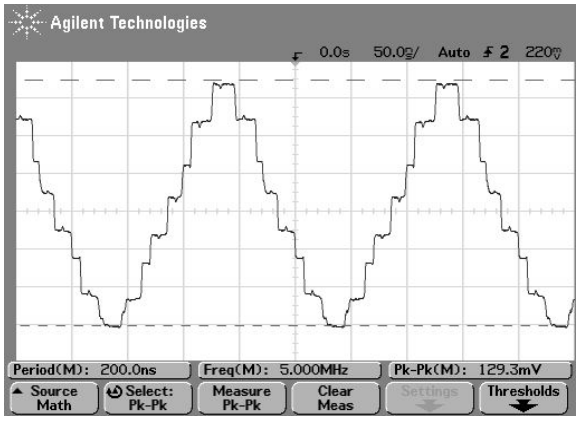

Fig. 5 Measured ADC/DAC output waveform with 8 quantization steps at an 11GS/s sampling rate.

The measured ADC output waveform reconstructed by the on-chip DAC given in Figure 5 clearly demonstrates the 8 quantization steps with an 11 GS/s sampling rate. Figure 6 gives the measured DAC output spectrum for a 1.102 GHz ADC input signal at 11GS/s sampling rate. The measured SFDR, SNDR and ENOB under this condition are 26.5 dBc, 17.8 dBc and 2.7 bits, respectively. It demonstrates a good dynamic performance for the 3-bit ADC-DAC RFIC.

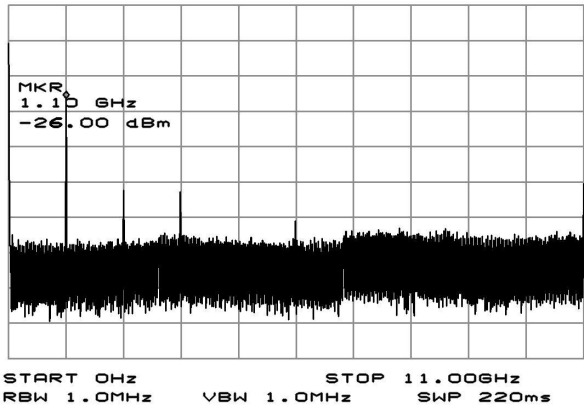

Fig. 6 Measured output spectrum of the ADC-DAC pair for a 1.102 GHz input signal with the sampling rate of 11 GS/s.

The measured SFDR for different ADC input frequencies at the maximum sampling rate of 11GS/s is given in Fig. 7. The maximum dynamic range of the implemented ADC-DAC is measured as 28 dBc with a 1.5 GHz ADC input. For larger than 20 dBc SFDR, the ADC achieves an input bandwidth larger than 3.5 GHz. The

ADC dynamic performance will be improved once a track-and-hold amplifier is applied at the input stage of the ADC with additional power consumption. The performance comparison of the 3-bit flash ADCs operating at above 10 GS/s sampling rate is given in Table I. The presented ADC realizes the best FOM of 3.08 pJ/conversion-step with a 2.2 V power supply and 0.22 W power consumption implemented in a 1.0 x 0.8 mm^2 core chip area. In addition, this ADC was the only one measured using packaged parts, while all other mm-wave ADCs were measured using wafer-probe.

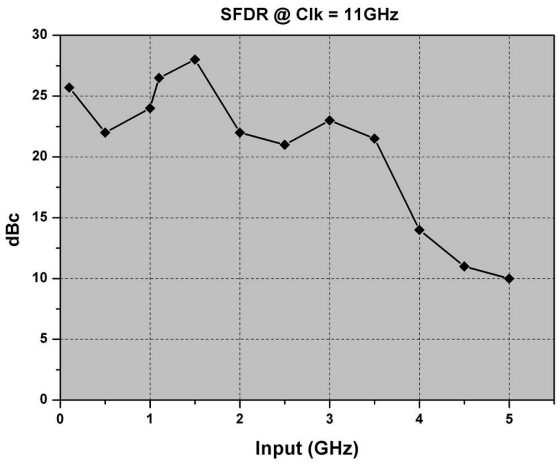

Fig. 7 Measured SFDR for 3-bit ADC-DAC pair as a function of input frequency at the sampling rate of 11GS/s.

TABLE. I PERFORMANCE COMPARISON OF MM-WAVE ADCS.

	[3]	[4]	[7]	This work
Sample Rate (GS/s)	10	40	24	**11**
SFDR / Input (dBc / GHz)	30.1/6	33/9	25/6	**28/1.5**
ENOB / Input (bits / GHz)	2.8/1	2.8/0.05	2.3/10	**2.7/1.102**
Power Supply (V)	4	--	-4	**2.2**
Power (W)	4.25	3.8	3.84	**0.22**
Technology (- / f_T in GHz)	InP/80	SiGe/210	InP/150	**SiGe/210**
Die Area (mm^2)	--	2.2 x 1.8	3 x 3	**1.0 x 0.8**
FOM($Pw/2^{ENOB}*f_s$) (pJ/step)	61.0	16.0	32.4	**3.08**
Test Prototypes	Wafer	Wafer	Wafer	**Packaged**

IV. CONCLUSION

A 3-bit 2.2V 3.08pJ/conversion-step 11GS/s flash ADC for X-band applications has been implemented in a 0.12 µm SiGe technology. At the maximum sampling rate of 11 GS/s, the packaged ADC-DAC RFIC is measured with a peak SFDR of 28 dBc at 1.5 GHz ADC input and a peak ENOB of 2.7 bits at 1.102 GHz ADC input. The ADC-DAC RFIC achieves the best FOM of 3.08 pJ/conversion-step, consumes 0.22 W power with a 2.2 V supply and occupies a core area of 1.0 x 0.8 mm^2. This ADC demonstrates a good X-band sampling performance with the lowest power supply voltage, lowest power consumption, smallest core area and best FOM comparing to prior art mm-wave ADC designs.

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