A Compact Integrated 100 GS/s Sampling Module for UWB See Through Wall Radar with Fast Refresh Rate for Dynamic Real Time Imaging

Quanhua Liu, Yazhou Wang, and Aly E. Fathy

Department of EECS, University of Tennessee, Knoxville, TN 37996, USA

***Abstract* — This paper presents the development of a compact integrated sampling module for Ultra Wideband (UWB) see through wall radar. The development of this radar is geared towards see through wall imaging and micro-Doppler detection of any human motions. The radar transmits a UWB impulse signal for high rang resolution and utilizes 8 Vivaldi antenna array as receive array to achieve fine azimuth resolution. UWB data acquisition and high system data rate are two of the main challenges in designing UWB radar. By using equivalent time sampling method, a data acquisition solution is proposed and a compact module is implemented upon integrating a dual channel ADC chip and a Xilinx FPGA in one circuit board. See through wall experiments in a real scenario have been carried out to demonstrate the performance of this compact sampling module. The module supports two equivalent time sampling channels with maximal 100GS/s sample rate. It meets system update data rate requirement for Doppler processing, meanwhile it still can scan 8 receiver antennas and gives out 2D image of targets behind the wall.**

***Index Terms* — Ultra wideband radar, Radar remote sensing, Data acquisition, Field programmable gate arrays (FPGA), Motion detection.**

I. Introduction

Ultra Wideband (UWB) see through wall radar provides unique capability for non-contact inspection of human targets hidden behind barriers. It can be used for diverse purposes like in rescue missions, urban warfare, counter terrorism and law enforcement scenarios [1]. The advantages of the UWB radar are system simplicity and the potential of extremely high range resolution. However, design of an UWB system has its own challenges, i.e. UWB data acquisition. For example, a 1ns width short pulse requires several Giga-Hz sampling for fine resolution. The best commercial ADC chips, such as EV10AQ190 from e2V company, can reach 5 giga-samples per second (GS/S). But its ideal resolution is only 10 bits which limits signal-noise-ratio (SNR) and dynamic range to no more than 60dB. Additionally, these relatively high gigahertz sampling rate ADC chips are quite expensive and consume high power.

Luckily, there is another sampling method called equivalent time sampling that can be used [2]. For years, oscilloscope manufacturers have used this method to capture extremely fast repetitive waveforms. Equivalent time sampling constructs the entire input waveform by accumulating samples captured by phase shifting sample clock over many signal cycles. Therefore this method strictly requires that the input waveform be repetitive throughout the whole sampling cycle. In a typical see through wall scenario, the radar echoes can be considered quasi-static and periodic because of human relative slow movement, which makes it feasible to apply equivalent time sampling method.

Previously, our group developed a real-time see though wall system and utilized commercial ADCs and FPGA boards to realize equivalent time sampling module [3]. The used commercial firmware is made up of one Avnet Xilinx Virtex-4 FPGA evaluation board and two Maxim MAX108 ADC evaluation boards. Such an approach significantly speeds up the system design. But it also has some limitations. The clock feeding ADC chips, for example, came from FPGA pins due to the firmware architecture. It decreased the system performance caused by jitter of the TTL clock signal. Additionally, the 9-bit ADC providing a 54 dB dynamic range is not so attractive now. And twisted-pair wires were used to connect differential ADC output data to the FPGA boards. These connections are not convenient and lack maintainability. Aiming at improving the system maintainability, extendibility and reusability, we completely redesigned the original sampling system and have integrated its different modules. The newly designed compact general-purpose digitizing module can achieve 100 GS/S capture rate using equivalent time sampling mode and will be reported here.

This paper is arranged as follows: Section II is a brief overview of UWB though wall radar microwave front end. Section III discusses hardware design of the compact sampling module. Section IV presents the experimental results of see though wall imaging and human vital signs detection. Section V concludes the paper.

II. Overview of the Radar Front End

The detailed specifications of our current see through wall radar system are summarized in Table I. Block

diagram of the microwave front end is demonstrated in Fig.1 [3], [4].

Table I:
SPECIFICATIONS OF THE UWB RADAR SYSTEM

Specifications	Values
Operation Frequency Range	1.5 – 4.5 GHz
Carrier Frequency	3 GHz
Peak Transmitting Power	25 dBm
Pulse Repetition Frequency (PRF)	10 MHz
Pulse Repetition Interval (PRI)	100 ns
Pulse Shape	Gaussian Pulse
Pulse Width	0.7 ns
Receiver	I & Q Demodulation
Transmit Antenna	Horn Antenna
Receive Antenna	Linear Vivaldi Array

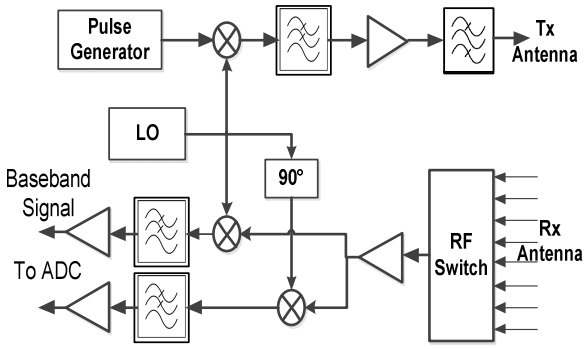


Fig. 1. Block diagram of UWB radar front end

The 1×8 Vivaldi antenna array has a spacing of 6.0 cm to achieve a high azimuth resolution. For low cost consideration, there is only one receiver implemented in the radar system. For a SAR operation, a single-pole 8-throw (SP8T) switch is utilized to sequentially select one linear array. One of the main applications for this radar system is Doppler-based human motion detection. Human motion such as walking, arm swing, breathing will induce micro-Doppler effects on radar echo that can be observed using time–frequency transforms [5]. The slow time domain sample rate should satisfy Nyquist theorem and that means the system update data rate should be higher than the maximum Doppler frequency shift. The average human walking speed is less than 2m/s in building and arm swing speed is less than 5m/s. Thus the Doppler frequency shift at 3GHz is no more than:

$$f_d = \frac{2v}{\lambda} = \frac{2\times 5\text{m/s}}{10\text{cm}} = 100\text{Hz} \qquad (1)$$

Given that the value of the drift frequency f_d determines the requirement of system update data rate, then the scanning rate of receive antenna needs to achieve 200Hz.

III. HARDWARE DESIGN OF SAMPLING MODULE

The method of equivalent time sampling is well-documented [2], [6]. This technique requires a high precision programmable time delay circuit. Our compact sampling module uses commercial ICs to provide a low cost, lightweight digitizer with effective sampling rate of 100GHz. It employs a National Semiconductor dual channel 16-bit 160MHz ADC chip ADC16DV160, ON Semiconductor delay line chip MC100E196 and Xilinx Virtex5 FPGA.

The clock distribution network is the key part of the whole digitizer design. Its principal block diagram is presented in Fig. 2.

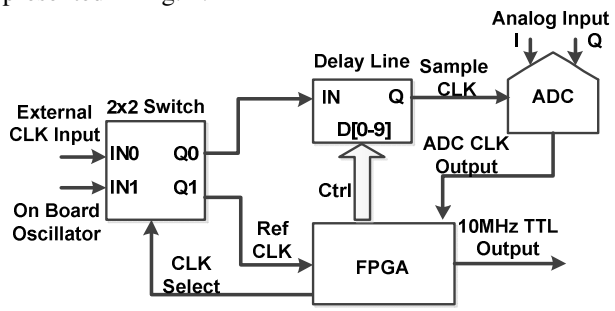


Fig. 2. Block diagram of clock distribution network

A 2x2 cross-point switch is used to select internal or external clock source. External clock input is useful when there is a need for changing sample frequency or for multi-board synchronous application. One switch output feeds FPGA as reference clock which is without phase shifting and it is used to generate a timing logic, and a 10MHz TTL output connected to the UWB pulse generator. The other switch output is sent to the delay line chip MC100E196 aimed at producing equivalent time sampling clock. MC100E196 provides a minimum 10ps delay step size with maximum 10ns delay range. The delay size can be programmed with a 10-bit digital control bus connected to the FPGA. The 10ps delay resolution gives us a sample rate of 100GS/s. FPGA uses ADC output clock to synchronize the ADC data.

The picture of the compact sampling module is shown in Fig.3. It is a 4-layer PCB board and the substrate is FR4. The 16-bit ADC chip has dual channel and the digital data is provided via Dual Data Rate (DDR) outputs and the logic standard is Low-Voltage Differential Signaling (LVDS). Thus there are only 16 different pair LVDS signals. Termination of LVDS is not necessary at the

FPGA input because we use the Xilinx Digitally Controlled Impedance (DCI) resistors inside the FPGA. All these features greatly minimize PCB routing area. Xilinx Virtex5 FPGA has input DDR modules to get the ADC data. The sample data is transferred to a personal computer via USB interface. The board employs a Cypress USB microcontroller CY7C68013 which is an integrated USB 2.0 transceiver. The throughput rate is about 26MB/s based on our test results. Our previously developed data acquisition module can be found in [4], which uses individual ADC and FPGA evaluation boards, and power supply circuits. Obviously, new compact module is more convenient to use due to small size and integration.

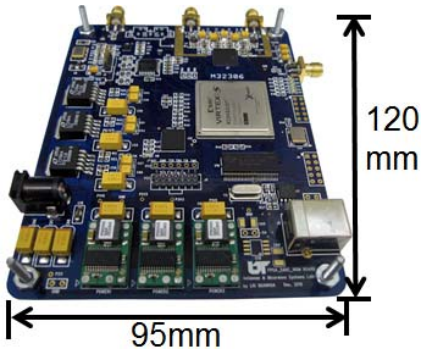
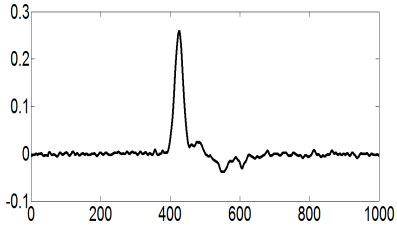


Fig.3. Compact sampling module

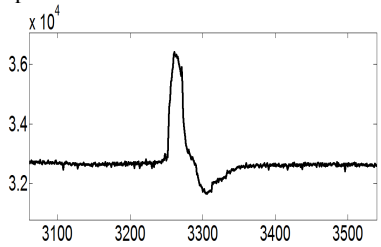
Another improvement of our new module is the clock jitter. As we mentioned above, the old system employed FPGA output to clock ADC chips. The jitter of the TTL clock signal is approximately 300ps and it degrades ADC performance. As shown in Fig.2, we can deduce total jitters in new module. The crosspoint switch produces maximum random clock jitter 0.5ps and deterministic jitter 10ps. The amount of delay line chip generated jitter is 0.2ps. The aperture jitter of ADC chip itself is only 0.08ps. The crystal oscillator on board is a Voltage Control Crystal Oscillator (VCXO) with 30ps jitters. Except for clock network selection, the careful board layout will also yield high level SNR.

IV. Experiment Results

In this section, we show some results from see through wall experiments using the compact sampling module. Figs.4 (a) and (b) show the pulse signals measured with real time oscilloscope and with our compact module, respectively. Good agreement has been achieved to validate the excellent performance of the developed sampling module. We also carried out an experiment in the corridor of engineering building at University of Tennessee, to investigate the performance of UWB radar when imaging multiple targets, as shown in Fig. 5. Fig. 5(a)

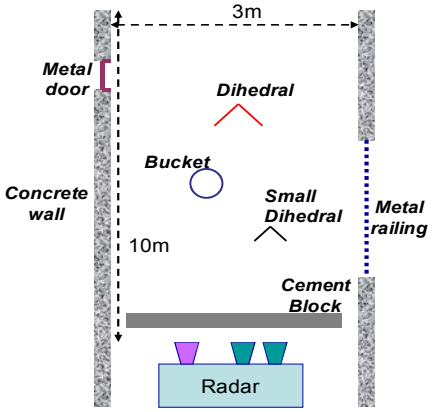


(a) A pulse measured with real time oscilloscope

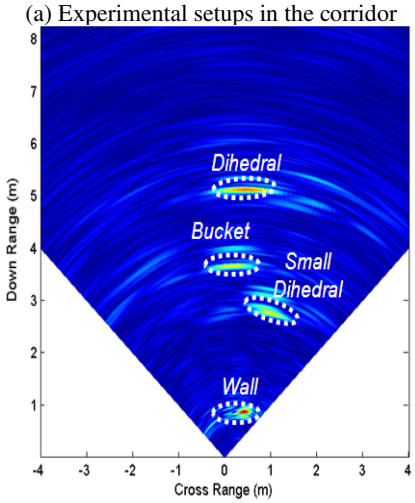


(b) A pulse measured with our compact module

Fig.4 Raw data records



(a) Experimental setups in the corridor



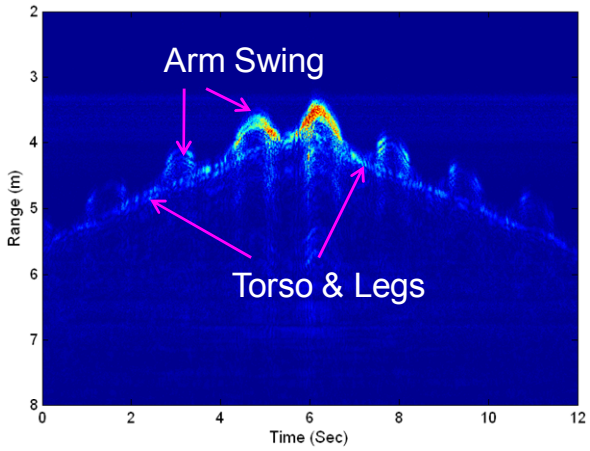
(b) Experimental imaging of multiple targets

Fig.5 UWB radar for see through wall imaging experiment

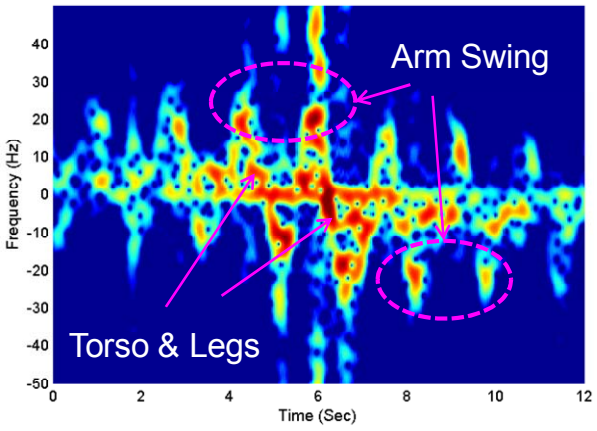
shows the layout plan of the experimental setup, where two dihedrals and a bucket are used as the detection

targets behind a cement block. The imaging result, as shown in Fig. 5(b), has accurately indicated the locations of the three targets, as well as the wall.

Experiments have also been performed to acquire the micro-Doppler signatures from human motions. A human is walking toward/away the UWB Doppler radar, with one-arm swing. The range-time plot in Fig. 6(a) indicates the walking trace of the human object clearly, with many humps on it that are due to the arm swing. The Doppler spectrogram in Fig. 6(b) presents the Doppler frequencies due to both walking and arm swinging. Comparing the two plots, the movements of torso and legs generate a positive Doppler frequency at time range 0 to 6s when human target is walking toward the radar and a negative Doppler at 6s to 12s when walking backward. The walking velocity is estimated to be 0.3 m/s using the range-time characteristics, which also agrees well with the calculation using the Doppler due to torso and legs motions. The periodic positive/negative Doppler frequencies in the spectrogram are generated by the arm movement, as marked in Fig. 6(b).



(a) Distance change with time of a walking human



(b) Doppler spectrum

Fig.6 UWB radar for Doppler detection of a walking human

V. Conclusion

This paper presents a new compact sampling solution for UWB impulse acquisition. The compact integrated module realizes two sampling channels with a maximum sample rate of 100GS/s. It achieves 220Hz system update rate at 30ps sample interval when scanning 8 receive antennas and meets the requirement for Doppler processing of any human motions. A faster system update data rate can be achieved if using a larger sample interval. The experimental results demonstrate the performance of this sampling module and show that the UWB radar is capable of imaging multiple targets and detecting Doppler signatures of human motions through the wall. The sampling module can be successfully applied in any case whenever we need high speed, accurate acquisition in UWB impulse systems. The current system update data rate is mainly limited by USB transfer speed. A Gigabit Ethernet transceiver can further increase the system update data rate and will be used to replace USB in future work.

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