30.3 A 24GS/s 6b ADC in 90nm CMOS

Peter Schvan[1], Jerome Bach[2], Chris Falt[1], Philip Flemke[1], Robert Gibbins[1], Yuriy Greshishchev[1], Naim Ben-Hamida[1], Daniel Pollex[1], John Sitch[1], Shing-Chi Wang[1], John Wolczanski[1]

[1]Nortel, Ottawa, Canada
[2]STMicroelectronics, Crolles, France

New receivers for 10-to-40Gb/s optical communications rely on DSP-based equalization to correct for fiber impairments and enhance channel spectral efficiency [1-3]. This requires a 6b ADC with sampling rate that is twice the data rate and low ENOB degradation up to the Nyquist frequency. Previously a 24GS/s ADC was designed in InP technology [3] with only 3b resolution and a 5b 22GS/s BiCMOS ADC reported in our earlier work [4] required 3W and was not suitable for integration with DSP core in an advanced CMOS technology. A 20GS/s 8b ADC implemented in 0.18µm CMOS [5] achieved 4.6b at 6GHz input, but consumed 9W. Lower sampling rate converters include a 10GS/s 5b ADC in SiGe BiCMOS [2] and a 12.5GS/s 4.5b ADC in 65nm CMOS [6]. This paper presents a 24GS/s 6b ADC in 90nm CMOS with the highest ENOB up to 12GHz input frequency and lowest power consumption of 1.2W compared to ADCs with similar performance. It uses an interleaved architecture of SAR type self-calibrating converters operating from 1V supply combined with an array of 2.5V T/Hs with delay, gain and offset-calibration capability.

For a CMOS ADC with sampling rates above 10GHz, the time-interleaved architecture is an effective approach exploiting the superior performance of CMOS switched-capacitor circuits. The ADC presented in this paper, (see Fig. 30.3.1) uses 16 interleaved 25mW 1.5GS/s 6b sub-ADCs preceded by T/H circuits. To reduce bandwidth degradation at the 50Ω differential input, the T/H circuits are split into 2 arrays of 8, driven through a 6dB power splitter. Digitally controlled calibration circuits are used to correct for offset, gain mismatch and timing skew between the 16 channels. The outputs of the sub-ADCs are fed into an array of 16 6b-wide 1:8 DEMUXes to produce time-aligned data at $F_s/64$ rate for writing into the memory. The on-chip 128K memory along with on-board SFI-4 PC interface is used for further data processing and ADC characterization.

The T/H circuit (Fig. 30.3.2) is implemented with 2.5V MOS devices using well-known switch topology [7]; additional transistors M7-M8 are introduced for feedthrough compensation. Unity-gain buffers drive approximately 0.5pF load at the sub-ADC input. An essential part of T/H is the 1V CML to 2.5V CMOS clock converter. Two differential amplifiers (M11-M18) convert 0.4V CML differential signal into two 2.5V CMOS signals. Pull-up current sources M9-M10 provide optimum biasing conditions for the differential amplifiers and decrease sensitivity to noise on 1V supply. Resistors R1, R2 improve frequency response and symmetry of the rise /fall time of the amplifiers. The T/Hs are sampled at 1.5GHz with 25% duty-cycle clocks to allow longer settling time.

The multi-phase 1.5GHz sampling clocks are generated (see Fig. 30.3.3) by clocking two sets of shift registers with both edges of the $F_s/4$=6GHz I,Q quadrature clocks. The delay of each sampling clock is fine tuned in 0.4ps steps using a phase interpolator. The sampling time of the sub-ADC is also adjustable to maximize the available settling time.

The 25mW sub-ADC is a 6b 1.5GS/s interleaved ADC composed of 10 elementary SAR converters running in parallel at full clock rate as shown in Fig. 30.3.4. Each single SAR converter is using charge-redistribution principle [8] and requires 10 clock cycles to generate the 6b binary output data, 2 for the self-calibration, 1 for input-signal sampling, 6 for the 6b successive-approximation binary-search process and 1 for data output delivery. With this architecture, the overall output data rate equals the clock rate.

The comparator of the single SAR is composed of 2 cascaded g_mR-gain stages with 24dB gain and 1.7GHz bandwidth. Measured INL and DNL are below 0.1LSB and the sub-ADC area is 0.09mm^2. The sub-ADC achieves 5.6 ENOB at F_s=1.5GS/s and F_{in}=750MHz leading to a FOM of 0.34pJ/conversion-step that compares favorably with other reported result for the same type of ADC [9].

The ADC is packaged in CBGA and mounted on a circuit board together with a PC-interface FPGA. The input signals are applied through microwave-type connectors, therefore, reported performance includes slight signal degradation in the short PCB traces and in the package. The ADC is tested at 24GS/s sampling rate with sine-wave inputs with nominal power supplies. The INL and DNL, measured at 2GHz input signal using standard code density method, are below 0.5 LSB. Output spectrum before calibration (Fig. 30.3.5) typically shows largest spurs related to the input frequency mixed with harmonics of 1/16th and 1/4th of the sampling clock frequency. After the calibration, maximum harmonic power (SFDR) is < -35dBc up to F_{in}=12GHz or about -50dBc for F_{in}=3.28GHz (bottom of Fig. 30.3.5). The timing, gain and offset-calibration settings are determined by processing 64-sample FFT for each sub-ADC. The T/H sampling times are adjusted to minimize the phase errors between the fundamental harmonics. No compensation is performed to reduce non-linearity.

ENOB frequency characteristics are measured for two methods of calibration (see Fig. 30.3.6). For curve (a) averaged calibration settings are obtained after performing several calibrations at different input frequencies and averaging the coefficients. The input amplitude is set to 95% of full scale at 100MHz. For curve (b) calibration is re-done at each frequency and input amplitude is adjusted to maintain 95% ADC fill. In case (b) reduction of ENOB at higher frequency is primarily due to clock jitter, uncompensated timing skew and T/H non-linearity.

ENOB remains above 4.1 up to 8GHz and above 3.5 up to 12GHz input frequency. The periodic variation of ENOB curve (a) can be explained by the phase-mismatch variation between T/Hs with input frequency. When calibration is performed at every frequency this variation is significantly reduced. Standard method for estimating the sampling jitter from ENOB variation at high frequency after removing all harmonics yields close to 0.4ps$_{rms}$ jitter generated by clock circuitry and external signal sources (estimated to be below 0.1ps$_{rms}$).

The ADC is fabricated in a 90nm CMOS process. Figure 30.3.7 shows the die micrograph of the ADC and the summary of the ADC packaged performance. The ADC core occupies 4×4mm^2 with the sub-ADCs arranged in a U-shape around the T/H circuits. To minimize supply noise, metal-to-metal and MOS decoupling capacitors are used extensively and analog and digital parts of the circuit are powered separately. Power dissipation is 1.2W operating from 1V and 2.5V supplies resulting in a FOM of <5pJ/conversion-step that is better than those reported previously for high-speed converters [3-5].

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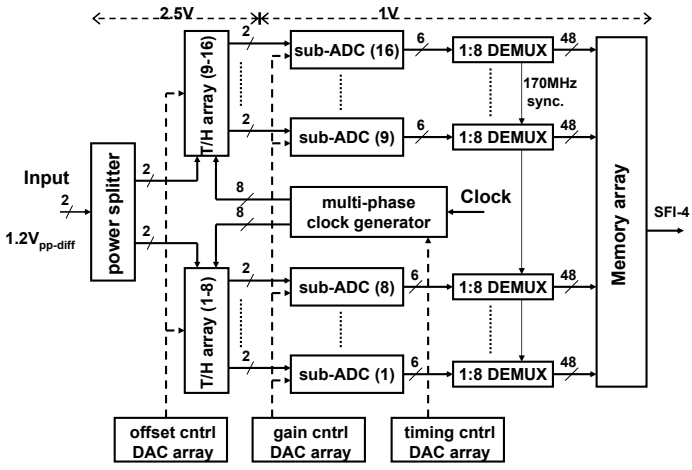

Figure 30.3.1: ADC architecture including on-chip memory for testing.

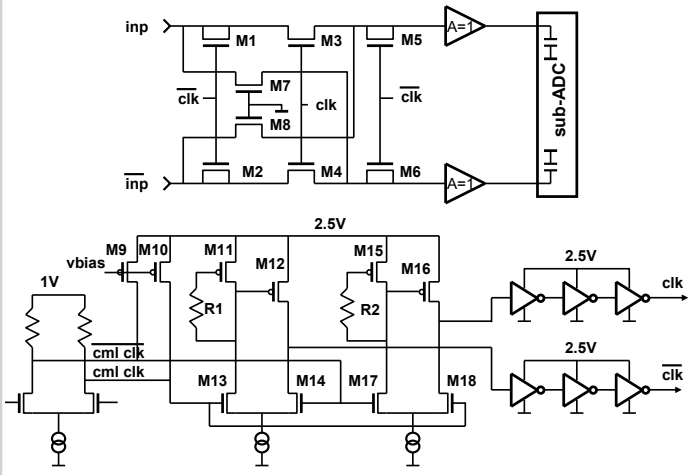

Figure 30.3.2: Schematic of the T/H and CML to CMOS converter.

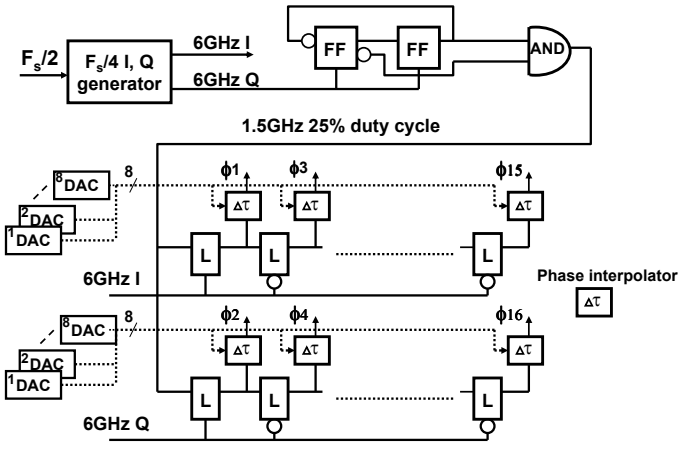

Figure 30.3.3: Multi-phase clock generator.

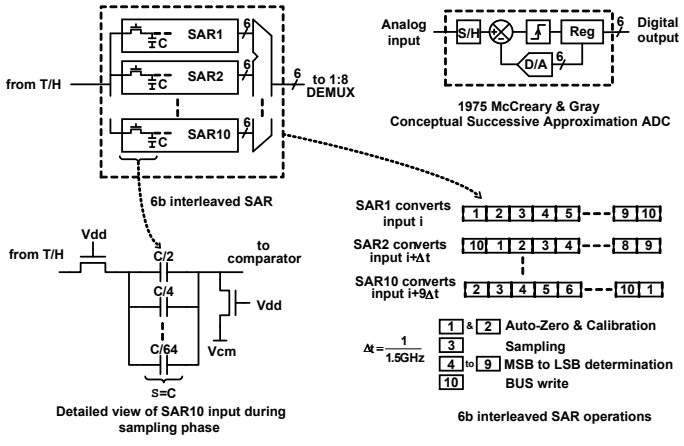

Figure 30.3.4: Interleaved SAR ADC.

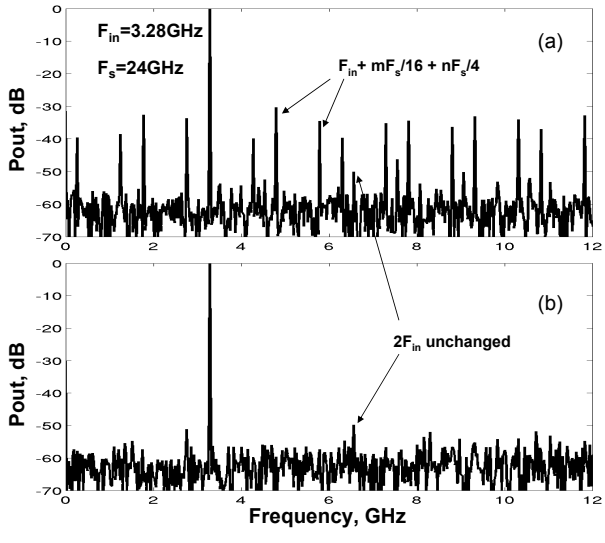

Figure 30.3.5: ADC output spectrum (a) before and (b) after calibration.

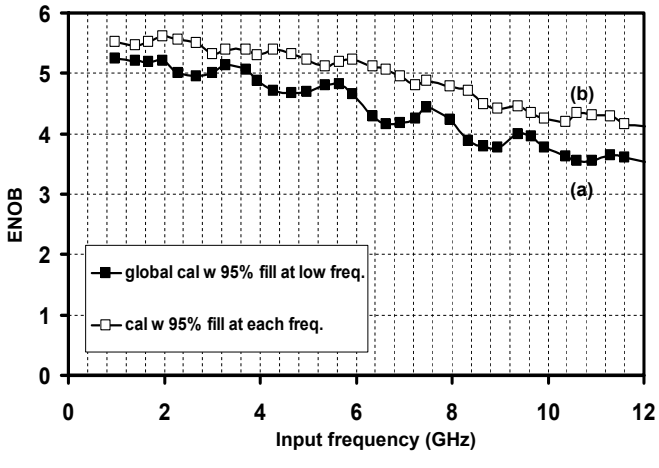

Figure 30.3.6: ENOB vs. input frequency at F_s=24GS/s.

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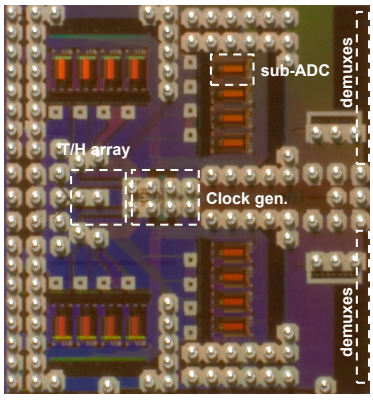

Packaged ADC performance

Resolution	6b
Conversion rate	0.1 - 24GS/s
Input range	$1.2V_{pp\text{-}diff}$
ENOB average cal / cal each freq	 4.2/4.8, F_{in}= 8GHz 3.5/4.1, F_{in}= 12GHz
SFDR	40dB @ 8GHz 35dB @ 12GHz
Power	1.2W @ 1V and 2.5V
ADC core	4 x 4 mm^2
Process	90nm CMOS

Figure 30.3.7: ADC die micrograph w/o memory and performance summary.

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