Fully Integrated and Reconfigurable Architecture for Coherent Self-Testing of IQ ADCs

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***Abstract*—In this paper we present a reconfigurable architecture for coherent built-in self-testing (BIST) of high speed IQ ADCs with moderate resolutions. The proposed system can be fully integrated with the ADC and, besides a low-jitter clock reference, no other external high quality generators are required. A locked system comprising a first phase-locked loop (PLL) with two IQ linear outputs and a second PLL with a squared output signal are proposed as well as the dedicated voltage-controlled oscillator (VCO) circuits. To illustrate the simplicity of the proposed solution, the system is designed, parameterized and simulated targeting the BIST of a 6-bit 1 GS/s ADC.**

I. INTRODUCTION

Modern CMOS technologies allow the design of very high speed analog-to-digital converters (ADCs) with moderate resolutions (6 to 10 bits). Currently, a strong effort has been done to develop new circuits and new techniques to reach such high conversion rates, without investing a similar effort in the implementation of new and efficient testing methodologies.

Testing during mass-production is very time consuming and represents a very significant percentage of the total cost of an ADC. With sampling frequencies increasing towards the GS/s range, this cost will be critical in the near future. In conventional dynamic testing of ADCs we must provide, off-chip, an input test stimulus (usually a sine wave) and a clock signal [1]. External signal generators with the required accuracy and bandwidth, which must exceed the device under test specifications, are very expensive. Transformers for single-ended to differential conversion are difficult to implement and have limited frequency range. The printed-circuit board layout must be done with special care to avoid mismatches in path length and associated parasitics.

Fully integrated built-in self-testing (BIST) methods are the answer to these challenges. Owing to the low cost and reliability of CMOS integration, it is possible to integrate on-chip efficient and cost-effective circuits specifically intended for testing. This paper is emphasized on a fully integrated architecture for dynamic BIST of high speed in-phase and quadrature-phase (IQ) ADCs.

Recently, several integrated schemes have been proposed for ADC static and dynamic BIST. An accurate on-chip sine wave generator accompanied by a digital signal processor (DSP) for frequency-domain test of delta-sigma converters is proposed in [2], but this is not suitable for high frequency testing and leads to a large area overhead. In [3], an on-chip read-only memory is used to store the input samples and a digital-to-analog converter followed by an amplifier and a filter converts the digital bit-stream into the analog sine wave; however, there is a large area overhead, the dynamic range is low, and the amplifier has a large input capacitance. In static testing, several techniques have been proposed to generate on-chip a linear ramp to perform monotonicity and histogram test of ADCs [4], [5], but the results depend largely on the accuracy of the additional components in the test circuitry. Linearity characterization of an ADC excited by noise is obtained through spectral analysis in [6], but this can not be used for ADC dynamic testing.

This paper presents a fully integrated, reconfigurable, and low-cost architecture for coherent self-testing of IQ ADCs with resolution ranging from 6 to 10 bits and conversion rates from 80 MHz to 1 GHz. The architecture is based on two PLLs to generate coherent sampling and requires only a stable external reference signal. The implementation of the critical blocks, namely the VCOs, is described in detail, and a filtering scheme is proposed to improve the output harmonic distortion of one of them.

II. PROPOSED ARQUITECTURE

To evaluate the dynamic performance, e.g., signal-to-noise ratio (SNR), total harmonic distortion (THD), effective number-of-bits (ENOB), etc. of an ADC, it is traditionally stimulated by a sine wave and the converted samples set is translated to the frequency-domain by means of a DSP performing the Fourier transform. By analyzing the resulting spectral content the dynamic parameters are obtained.

The Fourier transform assumes that the waveform is continuous from -∞ to +∞, and an incorrect result arises if the waveform is not sampled over an integer number of periods. To solve this problem, either windowing or coherent sampling can be used. Windowing originates spectral spreading (the energy of the main frequency component spreads to adjacent bins) and requires additional mathematical processing to derive the spectral content. When possible, it is preferable to avoid windowing by employing a sampling technique known as coherent sampling, which is achieved by having [1]:

$$f_{in}/f_s = N_p/N_s \tag{1}$$

where f_{in} is the sine wave input frequency, f_s is the sampling frequency, N_p is the integer number of periods from which we take samples, and N_s is the total number of samples taken. The best results are obtained if N_p is integer (so that the waveform

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continuity is guaranteed) and N_s is a power of 2 to allow the use of the efficient fast Fourier transform (FFT) algorithm. For efficiency and to reduce test time, the ratio N_p/N_s must be irreducible so that no redundant information is collected [1]. The length of the samples set that result in a representative spectral content for an N bit ADC is

$$N_s > \pi \cdot 2^N \approx 2^{N+2}. \tag{2}$$

Analyzing (1) we can see coherent sampling relies on two frequency multiplications (or divisions), which have a well-defined relationship. Frequency multiplication can be realized by either a PLL or a delay-locked loop (DLL), in which a low frequency is multiplied by a factor to result in a higher frequency. The main advantage of a DLL is that no jitter accumulates at the output over multiple operation cycles [7]. However, the frequency multiplication circuitry is difficulty to implement and large multiplication factors are not possible. Hence, to obtain coherent self-testing of ADCs we propose a fully integrated architecture based on PLLs.

The proposed architecture, depicted in Fig. 1, is composed of two PLLs (PLL_1 and PLL_2) that share the same external reference signal to ensure coherent sampling. Each PLL is built with a phase/frequency detector (PFD), a charge pump (CP), a loop filter (LF), a VCO and a frequency divider. PLL_1 generates IQ sine wave signals and PLL_2 generates a square wave clock signal, which are used to test the IQ ADCs. The converted N_s samples (for each ADC) are processed by a DSP to calculate the dynamic performance parameters of the ADCs. The results are then compared with different resolution thresholds (for example, 6, 7, and 8 bits) up to the maximum resolution allowed by the self-testing system and, for each comparison, a pass or fail indication is shown. With this, ADCs having different resolutions are separated and also it is possible to check the performance degradation during the ADCs life time.

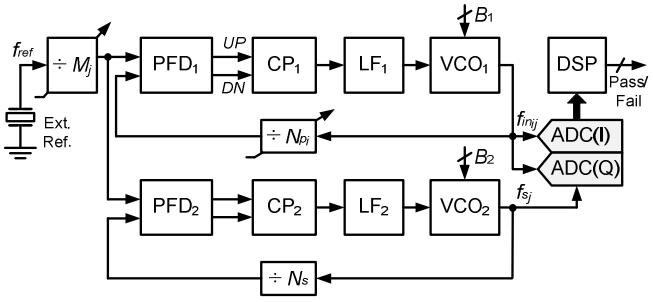

Fig. 1. Proposed architecture for coherent self-testing of IQ ADCs.

When the two PLLs are in lock, the input and sampling frequencies of the ADCs are

$$f_{in_{ij}} = N_{p_i} \cdot f_{ref} / M_j \tag{3}$$

$$f_{s_j} = N_s \cdot f_{ref} / M_j \tag{4}$$

where, f_{ref} is a stable external reference frequency (e.g., produced by a crystal oscillator) and M_j and N_{p_i} $(i, j = 1, 2, 3)$ are programmable frequency divider values, which enable different frequencies for the input and sampling signals. From (3) and (4) we obtain (1), i.e., coherent sampling is performed.

The architecture parameters N_s, N_{p_i}, and M_j should be selected according to the resolution of the ADCs under test, the external reference frequency, the desired sampling frequencies ($\hat{f}_{s_j}$) and the desired normalized input frequencies ($\hat{f}_{in_i} / f_s$). N_s is a power of 2, given by (2). N_{p_i} (i = 1, 2, 3) is given by

$$N_{p_i} = \left\{ \left(\hat{f}_{in_i} / f_s \right) \cdot N_s \right\} \tag{5}$$

where $\{x\}$ means the nearest odd integer value of x. Note that odd integer values for N_{p_i} ensure irreducibility with respect to N_s. M_j (j = 1, 2, 3) is given by (6), where $\langle x \rangle$ is nearest integer value of x.

$$M_j = \left\langle f_{ref} \cdot N_s / \hat{f}_{s_j} \right\rangle \tag{6}$$

TABLE I gives the architecture parameters and the resulting frequency map for 6 bits ADCs with f_{ref} = 10 MHz, $\hat{f}_{s_j}$ = 250, 500, and 1000 MHz, and $\hat{f}_{in_i} / f_s$ = 1/2, 1/4, and 1/8. We can see that the actual input and sampling frequencies are slightly different from the desired ones. In TABLE II, the values are obtained for 10 bits ADCs with $\hat{f}_{s_j}$ = 80, 120, and 160 MHz, and the same reference frequency and normalized input frequencies considered in TABLE I.

TABLE I. PROGRAMMABLE PARAMETERS AND FREQUENCY MAP FOR 6 BITS ADCS (ALL FREQUENCIES ARE IN MHZ)

$f_{ref} \equiv 10$ MHz		$\hat{f}_{s_1} \equiv 250$	$\hat{f}_{s_2} \equiv 500$	$\hat{f}_{s_3} \equiv 1000$
$N \equiv 6$ bits	$N_s = 256$	$M_1 = 10$	$M_2 = 5$	$M_3 = 3$
		$f_{s_1} = 256$	$f_{s_2} = 512$	$f_{s_3} = 853.3$
$\hat{f}_{in_1} / f_s \equiv 1/2$	$N_{p_1} = 129$	$f_{in_{11}} = 129$	$f_{in_{12}} = 258$	$f_{in_{13}} = 429.9$
$\hat{f}_{in_2} / f_s \equiv 1/4$	$N_{p_2} = 65$	$f_{in_{21}} = 65$	$f_{in_{22}} = 130$	$f_{in_{23}} = 216.6$
$\hat{f}_{in_3} / f_s \equiv 1/8$	$N_{p_3} = 33$	$f_{in_{31}} = 33$	$f_{in_{32}} = 66$	$f_{in_{33}} = 109.9$

TABLE II. PROGRAMMABLE PARAMETERS AND FREQUENCY MAP FOR 10 BITS ADCS (ALL FREQUENCIES ARE IN MHZ)

$f_{ref} \equiv 10$ MHz		$\hat{f}_{s_1} \equiv 80$	$\hat{f}_{s_2} \equiv 120$	$\hat{f}_{s_3} \equiv 160$
$N \equiv 10$ bits	$N_s = 4096$	$M_1 = 512$	$M_2 = 341$	$M_3 = 256$
		$f_{s_1} = 80$	$f_{s_2} = 120.1$	$f_{s_3} = 160$
$\hat{f}_{in_1} / f_s \equiv 1/2$	$N_{p_1} = 2049$	$f_{in_{11}} = 40$	$f_{in_{12}} = 60.1$	$f_{in_{13}} = 80$
$\hat{f}_{in_2} / f_s \equiv 1/4$	$N_{p_2} = 1025$	$f_{in_{21}} = 20$	$f_{in_{22}} = 30.1$	$f_{in_{23}} = 40$
$\hat{f}_{in_3} / f_s \equiv 1/8$	$N_{p_3} = 513$	$f_{in_{31}} = 10$	$f_{in_{32}} = 15$	$f_{in_{33}} = 20$

III. VOLTAGE-CONTROLLED OSCILLATORS

The test system requires an oscillator to generate IQ sine waves and another to generate a square wave.

A. *Two-Integrator Oscillator* (VCO_1)

PLL_1 produces IQ sine wave signals. Thus, VCO_1 must generate sine waves in quadrature with high spectral purity. One possibility would be to use two cross-coupled LC oscillators. However, the inductors area is large and to improve the quality factors a CMOS process with special RF options (several metal layers with a thick top metal) would be required. A more attractive solution is depicted in Fig. 2. This

oscillator has two-integrators in a feedback structure, it is an inductorless circuit, and can operate in a quasi-linear regime. Additionally, it has a wide tuning range [8].

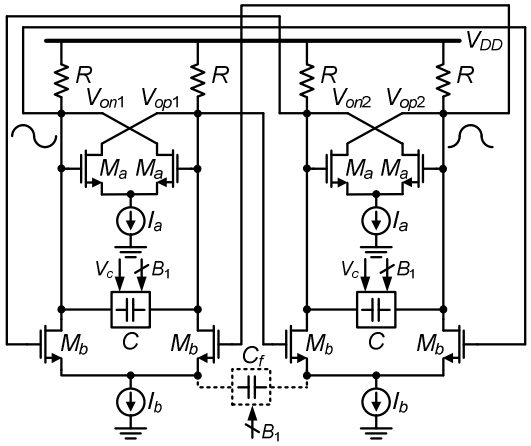

Fig. 2. Two-integrator oscillator (VCO_1).

Each integrator is realized by a differential pair (transistors M_b) and a capacitor (C). An additional differential pair (transistors M_a), with the output cross-coupled to the inputs, implements a negative resistance to compensate the losses due to resistors (R); it makes oscillation possible, and helps to stabilize the output amplitude.

In quasi-linear operation the differential outputs ($V_{od1} = V_{op1} - V_{on1}$ and $V_{od2} = V_{op2} - V_{on2}$) are in quadrature, and the oscillation frequency is [8]:

$$f_{osc} \approx g_{m_b} / (2\pi \cdot C). \tag{7}$$

Frequency tuning can be done by changing C or g_{m_b} (i.e., changing the current I_b). Since the last option also influences the output amplitude, it is preferable to use a varactor for tuning. We combine discrete and continuous tuning to lower frequency modulation sensitivity and widen the tuning range [9]. A switched-capacitor array controlled by B_1 bits defines the oscillator center frequency, and a small-size MOS varactor controlled by V_c is responsible for continuous variations around this frequency.

For accurate measurements, this VCO must have a THD at least 10 dB lower than the expected THD for the ADCs under test. We propose a filtering scheme based on a switched-capacitor array (C_f) to filter out the third harmonics, which are the dominant ones. This filtering technique is somewhat related to the technique proposed in [10], which was intended for phase noise reduction rather than for THD improvement. We have verified that, when a capacitance is placed between the current sources I_b, some harmonics are significantly attenuated, and that the maximum attenuation for a given harmonic can be controlled by the capacitance value.

B. *Relaxation Oscillator* (VCO_2)

To generate a square wave to clock the ADCs we need an oscillator with low power, small area and a reasonable phase noise. LC oscillators with high quality factor have the better phase noise. However, they require large silicon area. A superior monolithic solution is to use a RC oscillator, where both ring oscillators and relaxation oscillators are candidates. Although practical ring oscillators are slightly better than practical relaxation oscillators [11], we implemented VCO_2 as a relaxation oscillator, shown in Fig. 3. This choice is justified by: 1) relaxation oscillators have a constant frequency tuning gain; 2) in addition to the square wave, these oscillators also generate a triangular wave which can be used to calibrate timing errors in a time-interleaved ADC (this is out of the scope of this paper and is currently being investigated).

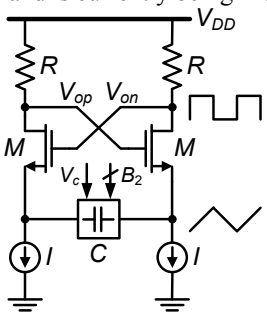

Fig. 3. Relaxation oscillator (VCO_2).

The relaxation oscillator (Fig. 3) is composed of an integrator implemented simply by a capacitor (C) and a Schmitt-trigger formed by two current sources (I), a cross-coupled pair of transistors (M) and two resistors (R) [8]. The oscillation frequency is approximately given by

$$f_{osc} \approx 1/(8RC). \tag{8}$$

This oscillator can be tuned by changing C, and, for the same reasons pointed out above, we chose a varactor combining both discrete and continuous tuning.

IV. Simulation Results

To simulate the whole system only the oscillators were implemented at transistor level using a 130 nm CMOS process. All the remaining circuits were modeled in Verilog-AMS. The two third order type-II PLLs were modeled with a three-state phase/frequency detector, a charge pump, a $C\|(R+C)$ passive loop filter and a frequency divider.

The simulations were performed for the highest frequencies shown in TABLE I (at lower frequencies the system specifications are more relaxed). In this case the architecture parameters are set to N_s = 256, N_{p1} = 129, and M_3 = 3. The reference frequency is 10 MHz, which results in sampling and input frequencies of 853.3 MHz and 429.9 MHz, respectively. VCO_1 has R = 240 Ω, M_a with 14 µm/0.36 µm, I_a = 1.45 mA, M_b with 18 µm/0.36 µm, I_b = 1.55 mA, C = 0.61 pF, C_f = 0.96 pF, and dissipates 7.2 mW from a 1.2 V supply. VCO_2 has R = 200 Ω, M with 189 µm/0.12 µm, C = 1.26 pF, I = 1.5 mA, and it consumes 3.6 mW. Fig. 4 (a) and (b) show the simulated phase noise of VCO_1 and VCO_2, respectively. Also shown in this figure is the phase noise when these VCOs are inserted in PLLs with a loop bandwidth of 400 kHz. The resulting rms jitter integrated above 3 MHz (set by the max. observation time) is about 1.5 ps for the clock signal (VCO_2), which is sufficient to accurately test 6-bit ADCs with input frequencies below 430 MHz. The simulations were performed with Cadence SpectreRF simulator.

The spectrum at the output of an ideal 6-bit ADC when the two PLLs are in lock state is shown in Fig. 5. This spectral profile was obtained by applying FFT over 256 digitized samples. The resulting THD is -50.0 dB, which is sufficient to test an ADC with 6 bits. This spectrum clearly shows that it resulted from coherent sampling, which validates the proposed approach.

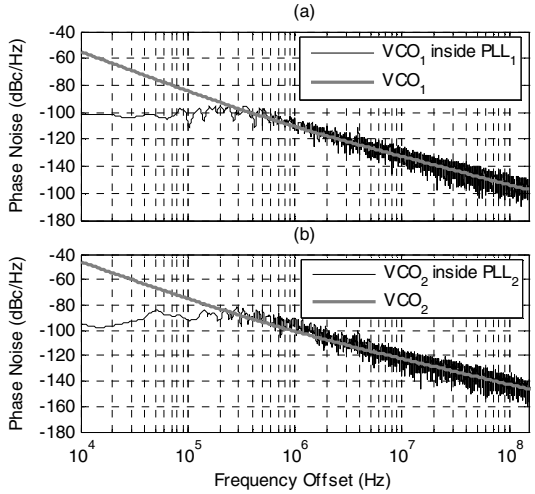

Fig. 4. Phase noise of (a) VCO_1 and PLL_1, and (b) VCO_2 and PLL_2.

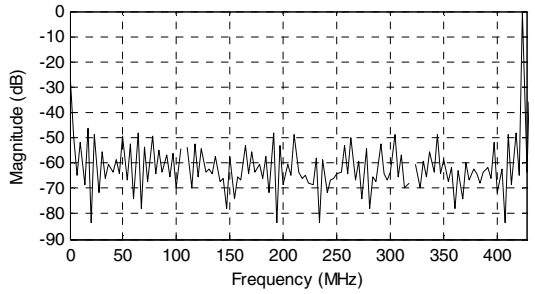

Fig. 5. Spectrum of the output of an ideal 6 bits 1GS/s ADC when the whole system is in lock (256 points FFT).

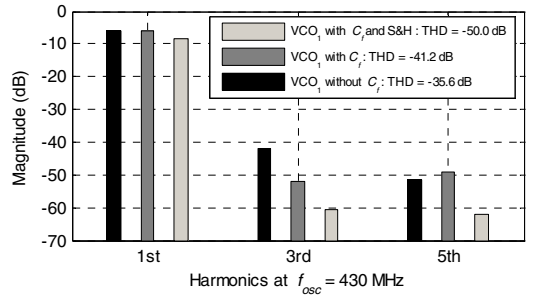

Fig. 6. HDs at the output of VCO_1 for three distinct cases: VCO_1 without C_f, VCO_1 with C_f, and VCO_1 with C_f and a S&H circuit with a BW of 500 MHz.

The dominant harmonic magnitudes (HDs) at the output of VCO_1 for three distinct cases are illustrated in Fig. 6. Firstly, the harmonics are measured when no filtering technique is applied to the VCO_1. In this case the resulting THD is -35.6 dB. When the capacitor array C_f is inserted we are able to notice a significant reduction on the third harmonic, which results in a THD improvement of about 5.6 dB. Finally, considering the case of an ADC having a finite sample-and-hold (S&H) bandwidth of 500 MHz, the actual signal that is supplied to the ADC has a THD of -50.0 dB because of the first order low-pass characteristic of the S&H. It is important to mention that, for the other $f_{in_{ij}}$ frequencies shown in TABLE I, the THD at the output of VCO_1 is always better than -48 dB even without any S&H, since the proposed filtering technique is more effective at lower frequencies.

V. Conclusions

We presented a fully integrated, low cost, reconfigurable architecture for coherent self-testing of high frequency and moderate resolutions IQ ADCs. Two PLLs, one for ADC input signal and the other for the clock signal, are used. We presented an example of a test system for 6-bit 1 GS/s ADCs and give a detailed description of the VCOs, which are the critical blocks. There is a stringent specification for the THD, for which we present a solution: a filtering technique that requires only one extra capacitor is applied to the VCO.

Acknowledgment

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