
STM32
CubeMX

1. Description

1.1. Project

Project Name	DSPBoardH7
Board Name	custom
Generated with:	STM32CubeMX 6.2.1
Date	05/18/2021

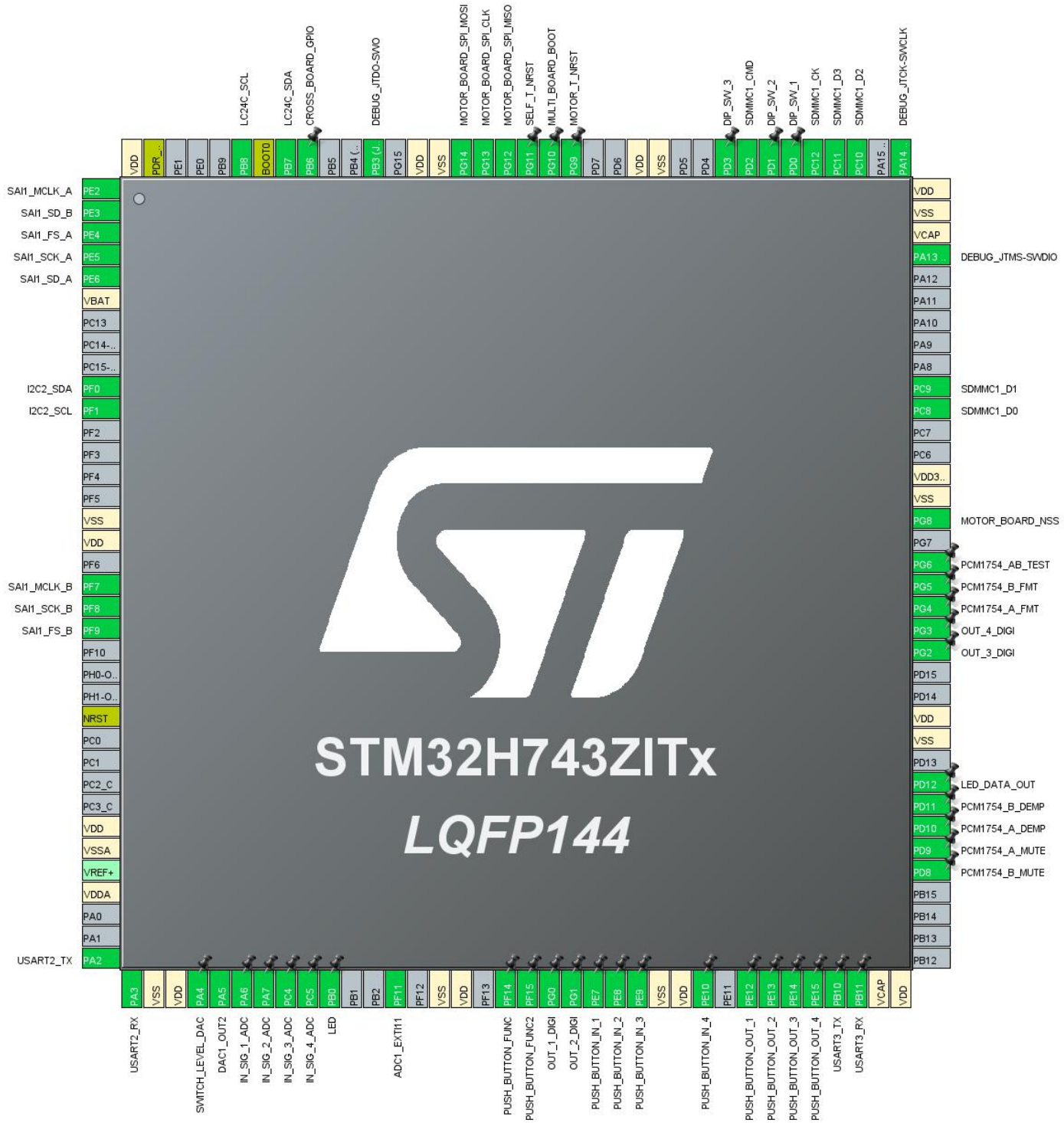
1.2. MCU

MCU Series	STM32H7
MCU Line	STM32H743/753
MCU name	STM32H743ZITx
MCU Package	LQFP144
MCU Pin number	144

1.3. Core(s) information

Core(s)	ARM Cortex-M7

2. Pinout Configuration



3. Pins Configuration

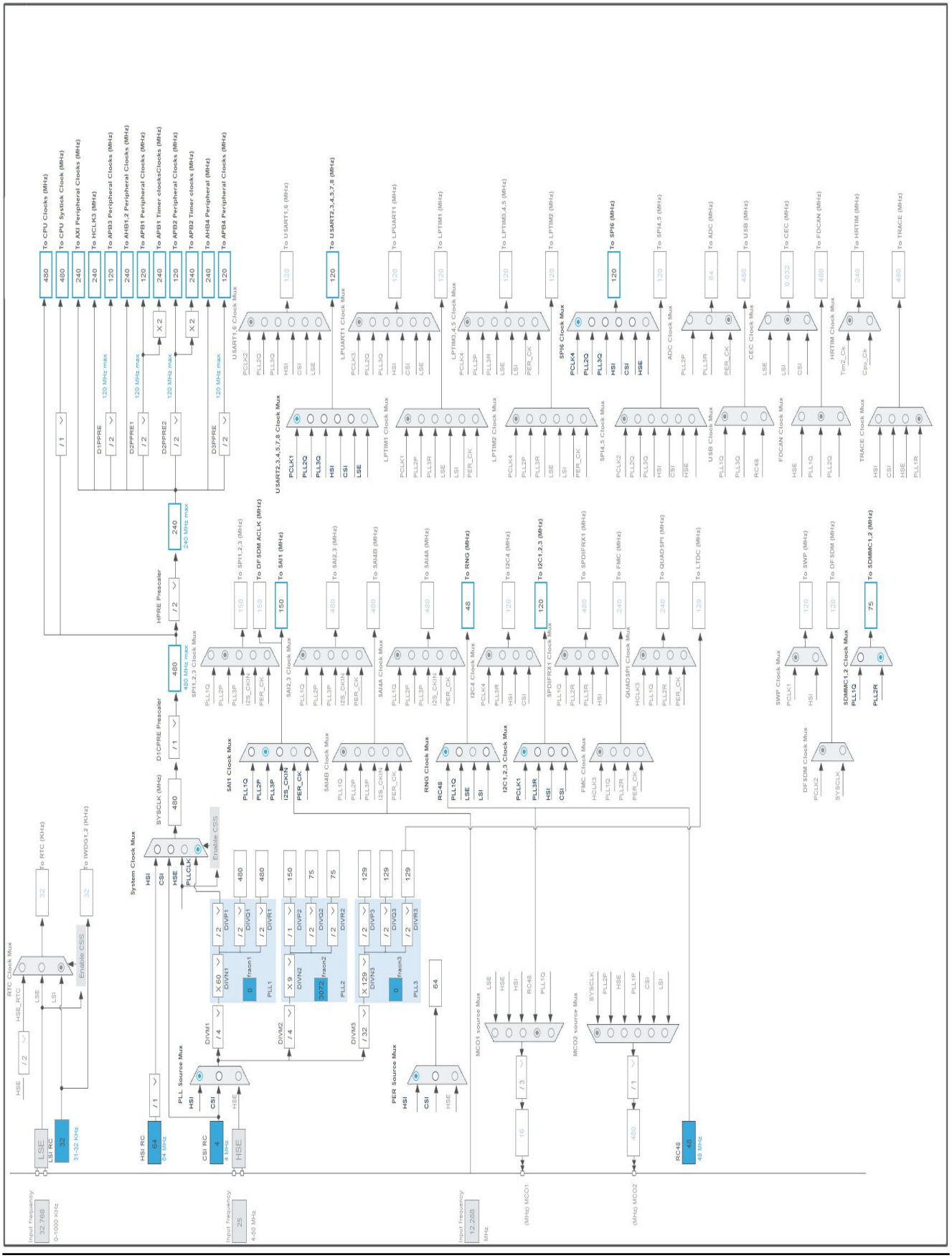
Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	PE2	I/O	SAI1_MCLK_A	
2	PE3	I/O	SAI1_SD_B	
3	PE4	I/O	SAI1_FS_A	
4	PE5	I/O	SAI1_SCK_A	
5	PE6	I/O	SAI1_SD_A	
6	VBAT	Power		
10	PF0	I/O	I2C2_SDA	
11	PF1	I/O	I2C2_SCL	
16	VSS	Power		
17	VDD	Power		
19	PF7	I/O	SAI1_MCLK_B	
20	PF8	I/O	SAI1_SCK_B	
21	PF9	I/O	SAI1_FS_B	
25	NRST	Reset		
30	VDD	Power		
31	VSSA	Power		
33	VDDA	Power		
36	PA2	I/O	USART2_TX	
37	PA3	I/O	USART2_RX	
38	VSS	Power		
39	VDD	Power		
40	PA4	I/O	DAC1_OUT1	SWITCH_LEVEL_DAC
41	PA5	I/O	DAC1_OUT2	
42	PA6	I/O	ADC1_INP3	IN_SIG_1_ADC
43	PA7	I/O	ADC1_INN3, ADC1_INP7	IN_SIG_2_ADC
44	PC4	I/O	ADC1_INP4	IN_SIG_3_ADC
45	PC5	I/O	ADC1_INN4, ADC1_INP8	IN_SIG_4_ADC
46	PB0 *	I/O	GPIO_Output	LED
49	PF11	I/O	ADC1_EXTI11	
51	VSS	Power		
52	VDD	Power		
54	PF14 *	I/O	GPIO_Input	PUSH_BUTTON_FUNC
55	PF15 *	I/O	GPIO_Input	PUSH_BUTTON_FUNC2
56	PG0 *	I/O	GPIO_Output	OUT_1_DIGI
57	PG1 *	I/O	GPIO_Output	OUT_2_DIGI
58	PE7 *	I/O	GPIO_Input	PUSH_BUTTON_IN_1

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
59	PE8 *	I/O	GPIO_Input	PUSH_BUTTON_IN_2
60	PE9 *	I/O	GPIO_Input	PUSH_BUTTON_IN_3
61	VSS	Power		
62	VDD	Power		
63	PE10 *	I/O	GPIO_Input	PUSH_BUTTON_IN_4
65	PE12 *	I/O	GPIO_Input	PUSH_BUTTON_OUT_1
66	PE13 *	I/O	GPIO_Input	PUSH_BUTTON_OUT_2
67	PE14 *	I/O	GPIO_Input	PUSH_BUTTON_OUT_3
68	PE15 *	I/O	GPIO_Input	PUSH_BUTTON_OUT_4
69	PB10	I/O	USART3_TX	
70	PB11	I/O	USART3_RX	
71	VCAP	Power		
72	VDD	Power		
77	PD8 *	I/O	GPIO_Output	PCM1754_B_MUTE
78	PD9 *	I/O	GPIO_Output	PCM1754_A_MUTE
79	PD10 *	I/O	GPIO_Output	PCM1754_A_DEMP
80	PD11 *	I/O	GPIO_Output	PCM1754_B_DEMP
81	PD12	I/O	TIM4_CH1	LED_DATA_OUT
83	VSS	Power		
84	VDD	Power		
87	PG2 *	I/O	GPIO_Output	OUT_3_DIGI
88	PG3 *	I/O	GPIO_Output	OUT_4_DIGI
89	PG4 *	I/O	GPIO_Output	PCM1754_A_FMT
90	PG5 *	I/O	GPIO_Output	PCM1754_B_FMT
91	PG6 *	I/O	GPIO_Output	PCM1754_AB_TEST
93	PG8	I/O	SPI6_NSS	MOTOR_BOARD_NSS
94	VSS	Power		
95	VDD33_USB	Power		
98	PC8	I/O	SDMMC1_D0	
99	PC9	I/O	SDMMC1_D1	
105	PA13 (JTMS/SWDIO)	I/O	DEBUG_JTMS-SWDIO	
106	VCAP	Power		
107	VSS	Power		
108	VDD	Power		
109	PA14 (JTCK/SWCLK)	I/O	DEBUG_JTCK-SWCLK	
111	PC10	I/O	SDMMC1_D2	
112	PC11	I/O	SDMMC1_D3	
113	PC12	I/O	SDMMC1_CK	
114	PD0 *	I/O	GPIO_Input	DIP_SW_1

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
115	PD1 *	I/O	GPIO_Input	DIP_SW_2
116	PD2	I/O	SDMMC1_CMD	
117	PD3 *	I/O	GPIO_Input	DIP_SW_3
120	VSS	Power		
121	VDD	Power		
124	PG9 *	I/O	GPIO_Input	MOTOR_T_NRST
125	PG10 *	I/O	GPIO_Output	MULTI_BOARD_BOOT
126	PG11 *	I/O	GPIO_Input	SELF_T_NRST
127	PG12	I/O	SPI6_MISO	MOTOR_BOARD_SPI_MISO
128	PG13	I/O	SPI6_SCK	MOTOR_BOARD_SPI_CLK
129	PG14	I/O	SPI6_MOSI	MOTOR_BOARD_SPI_MOSI
130	VSS	Power		
131	VDD	Power		
133	PB3 (JTDO/TRACESWO)	I/O	DEBUG_JTDO-SWO	
136	PB6 *	I/O	GPIO_Input	CROSS_BOARD_GPIO
137	PB7	I/O	I2C1_SDA	LC24C_SDA
138	BOOT0	Boot		
139	PB8	I/O	I2C1_SCL	LC24C_SCL
143	PDR_ON	Reset		
144	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	DSPBoardH7
Project Folder	C:\Users\casht\repos\eurorack-beettweek\stcubeideworkspace\DSPBoardH7
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_H7 V1.9.0
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	Yes
Enable Full Assert	Yes

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	MX_GPIO_Init	GPIO
2	MX_DMA_Init	DMA
3	SystemClock_Config	RCC
4	MX_ADC1_Init	ADC1
5	MX_DAC1_Init	DAC1
6	MX_TIM4_Init	TIM4
7	MX_USART3_UART_Init	USART3
8	MX_TIM2_Init	TIM2
9	MX_RNG_Init	RNG
10	MX_I2C1_Init	I2C1
11	MX_TIM5_Init	TIM5

Rank	Function Name	Peripheral Instance Name
12	MX_SAI1_Init	SAI1
13	MX_SDMMC1_SD_Init	SDMMC1
14	MX_SPI6_Init	SPI6
15	MX_I2C2_Init	I2C2
16	MX_USART2_UART_Init	USART2

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32H7
Line	STM32H743/753
MCU	STM32H743ZITx
Datasheet	DS12110_Rev5

6.2. Parameter Selection

Temperature	25
Vdd	3.0

6.3. Battery Selection

Battery	Alkaline(9V)
Capacity	625.0 mAh
Self Discharge	0.3 %/month
Nominal Voltage	9.0 V
Max Cont Current	200.0 mA
Max Pulse Current	0.0 mA
Cells in series	1
Cells in parallel	1

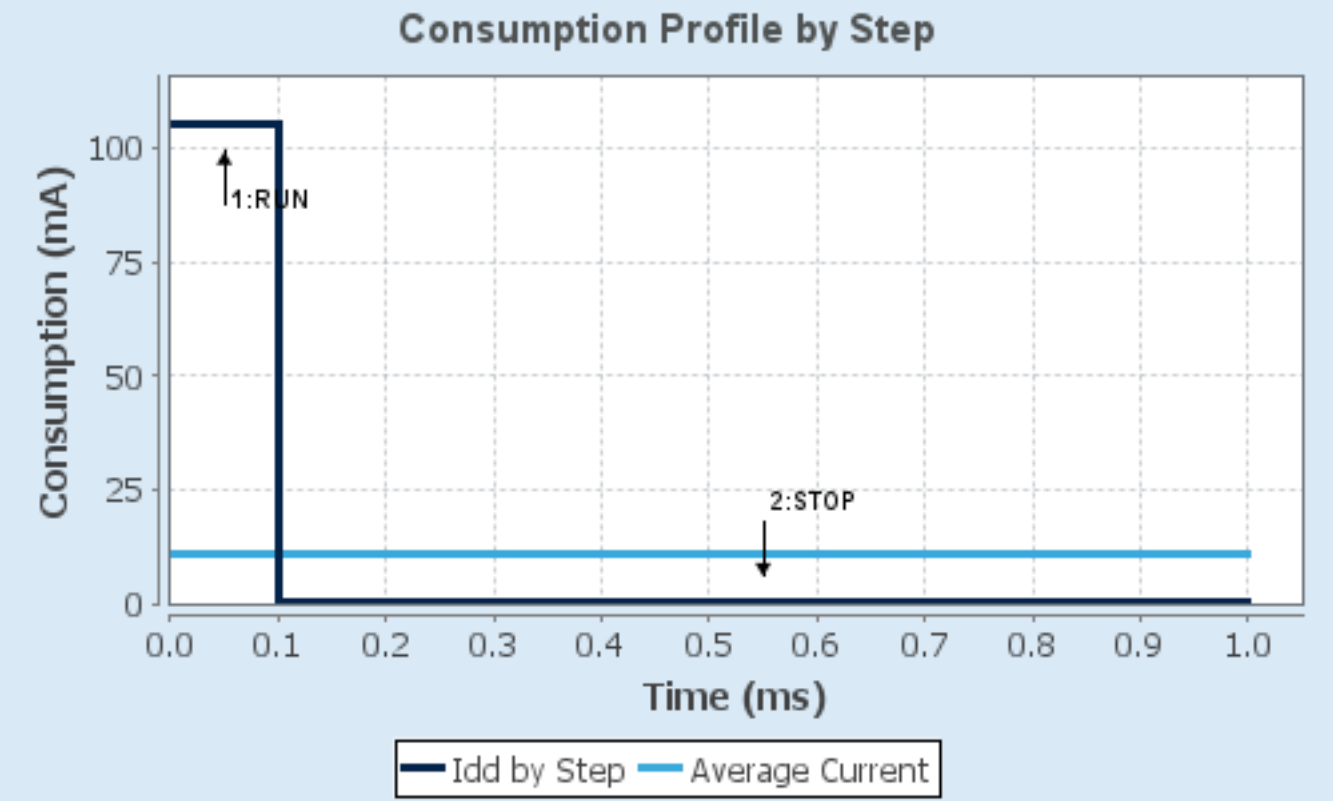
6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP
Vdd	3.0	3.0
Voltage Source	Battery	Battery
Range	VOS1: Scale1-High	SVOS5: System-Scale5
D1 Mode	DRUN/CRUN	DSTANDBY
D2 Mode	DSTANDBY	DSTANDBY
D3 Mode	DRUN	DSTOP
Fetch Type	FLASH_A	NA
CPU Frequency	400 MHz	0 Hz
Clock Configuration	HSE BYP PLL Flash-ON Cache-ON	Flash-LP
Clock Source Frequency	25 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	105 mA	170 µA
Duration	0.1 ms	0.9 ms
DMIPS	856.0	0.0
Ta Max	111.14	124.98
Category	In DS Table	In DS Table

6.5. Results

Sequence Time	1 ms	Average Current	10.65 mA
Battery Life	2 days, 10 hours	Average DMIPS	856.00006 DMIPS

6.6. Chart


Consumption Profile by Step
Consumption (mA)
100
75
50
25
0
1:RUN
2:STOP
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
Time (ms)
Idd by Step
Average Current

7. Peripherals and Middlewares Configuration

7.1. ADC1

IN3: IN3 Single-ended

IN4: IN4 Single-ended

mode: IN7

mode: IN8

EXTI Conversion Trigger: Regular Conversion Trigger

7.1.1. Parameter Settings:

ADCs_Common_Settings:	
Mode	Independent mode
ADC_Settings:	
Clock Prescaler	**Synchronous clock mode divided by 4 ***
Resolution	ADC 16-bit resolution
Scan Conversion Mode	Enabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
End Of Conversion Selection	**End of sequence of conversion ***
Overrun behaviour	**Overrun data overwritten ***
Left Bit Shift	No bit shift
Conversion Data Management Mode	**DMA Circular Mode ***
Low Power Auto Wait	Disabled
ADC_Regular_ConversionMode:	
Enable Regular Conversions	Enable
Enable Regular Oversampling	Disable
Number Of Conversion	**4 ***
External Trigger Conversion Source	EXTI Line11
External Trigger Conversion Edge	**Trigger detection on the rising and falling edges ***
Rank	1
Channel	Channel 3
Sampling Time	**32.5 Cycles ***
Offset Number	No offset
Offset Signed Saturation	Disable
Rank	**2 ***
Channel	**Channel 7 ***
Sampling Time	**32.5 Cycles ***
Offset Number	No offset
Offset Signed Saturation	Disable

Rank	**3 ***
Channel	**Channel 4 ***
Sampling Time	**32.5 Cycles ***
Offset Number	No offset
Offset Signed Saturation	Disable
Rank	**4 ***
Channel	**Channel 8 ***
Sampling Time	**32.5 Cycles ***
Offset Number	No offset
Offset Signed Saturation	Disable

ADC_Injected_ConversionMode:

Enable Injected Conversions	Disable

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

7.2. DAC1

OUT1 connected to: only to external pin

OUT2 connected to: only to external pin

7.2.1. Parameter Settings:

DAC Out1 Settings:

Mode selected	Normal Mode
Output Buffer	Enable
Trigger	None
User Trimming	Factory trimming

DAC Out2 Settings:

Mode selected	Normal Mode
Output Buffer	Enable
Trigger	None
User Trimming	Factory trimming

7.3. DEBUG

Debug: Trace Asynchronous Sw

7.4. I2C1

I2C: I2C

7.4.1. Parameter Settings:

Timing configuration:

Custom Timing	Disabled
I2C Speed Mode	**Fast Mode ***
I2C Speed Frequency (KHz)	400
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	**0x00B03FDB ***

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

7.5. I2C2

I2C: I2C

7.5.1. Parameter Settings:

Timing configuration:

Custom Timing	Disabled
I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	**0x307075B1 ***

Slave Features:

Clock No Stretch Mode	Disabled

General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

7.6. RCC

7.6.1. Parameter Settings:

Power Parameters:

SupplySource	PWR_LDO_SUPPLY
Power Regulator Voltage Scale	Power Regulator Voltage Scale 0

RCC Parameters:

TIM Prescaler Selection	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000
CSI Calibration Value	16
HSI Calibration Value	32

System Parameters:

VDD voltage (V)	3.3
Flash Latency(WS)	4 WS (5 CPU cycle)
Product revision	rev.Y

PLL range Parameters:

PLL1 clock Input range	Between 8 and 16 MHz
PLL2 input frequency range	Between 8 and 16 MHz
PLL1 clock Output range	Wide VCO range
PLL2 clock Output range	MEDIUM VCO range

7.7. RNG

mode: Activated

7.7.1. Parameter Settings:

Clock Error Detection	Enable

7.8. SAI1

Mode: Master with Master Clock Out

mode: I2S/PCM Protocol

Mode: Master with Master Clock Out

mode: I2S/PCM Protocol

7.8.1. Parameter Settings:

SAI A:

Synchronization Inputs	Asynchronous
Audio Mode	Master Transmit
Output Mode	Stereo
Companding Mode	No companding mode
SAI SD Line Output Mode	Driven
Protocol Parameters	
Protocol	**I2S Msb Justified ***
Data Size	**16 Bits Extended ***
Number of Slots (only Even Values)	2
Clock Source	SAI PLL Clock
Master Clock No Divider	Enabled
Audio Frequency	**96 KHz ***
Real Audio Frequency	**97.656 KHz ***
Error between Selected	**1.72 % ***
Fifo Threshold	Empty
Output Drive	**Enabled ***

SAI B:

Synchronization Inputs	Asynchronous
Audio Mode	Master Transmit
Output Mode	Stereo
Companding Mode	No companding mode
SAI SD Line Output Mode	Driven
Protocol Parameters	
Protocol	**I2S Msb Justified ***
Data Size	**16 Bits Extended ***
Number of Slots (only Even Values)	2
Clock Source	SAI PLL Clock
Master Clock No Divider	Enabled
Audio Frequency	**96 KHz ***
Real Audio Frequency	**97.656 KHz ***
Error between Selected	**1.72 % ***
Fifo Threshold	Empty
Output Drive	**Enabled ***

7.9. SDMMC1

Mode: SD 4 bits Wide bus

7.9.1. Parameter Settings:

SDMMC parameters:

Clock transition on which the bit capture is made	Rising transition
SDMMC Clock output enable when the bus is idle	Disable the power save for the clock
SDMMC hardware flow control	The hardware control flow is disabled
SDMMC clock divide factor	0
Is external transceiver present ?	no

7.10. SPI6

Mode: Full-Duplex Master

Hardware NSS Signal: Hardware NSS Output Signal

7.10.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	**16 Bits ***
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	**16 ***
Baud Rate	**7.5 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Output Hardware
Fifo Threshold	Fifo Threshold 01 Data
Tx Crc Initialization Pattern	All Zero Pattern
Rx Crc Initialization Pattern	All Zero Pattern
Nss Polarity	Nss Polarity Low
Master Ss Idleness	00 Cycle
Master Inter Data Idleness	00 Cycle
Master Receiver Auto Susp	Disable

Master Keep Io State	Master Keep Io State Disable
IO Swap	Disabled

7.11. SYS

Timebase Source: SysTick

7.12. TIM2

Clock Source : Internal Clock

7.12.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**16 ***
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	**1024 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

7.13. TIM4

Clock Source : Internal Clock

Channel1: PWM Generation CH1

7.13.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**350 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

Clear Input:

Clear Input Source	Disable

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	**60 ***
Output compare preload	Enable
Fast Mode	**Enable ***
CH Polarity	High

7.14. TIM5

Clock Source : Internal Clock

7.14.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	4294967295
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

7.15. USART2

Mode: Asynchronous

7.15.1. Parameter Settings:

Basic Parameters:

Baud Rate	**31250 ***
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	1
Fifo Mode	Disable
Txfifo Threshold	1 eighth full configuration

Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.16. USART3

Mode: Asynchronous

7.16.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	1
Fifo Mode	Disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA6	ADC1_INP3	Analog mode	No pull-up and no pull-down	n/a	IN_SIG_1_ADC
	PA7	ADC1_INN3	Analog mode	No pull-up and no pull-down	n/a	IN_SIG_2_ADC
	PC4	ADC1_INP4	Analog mode	No pull-up and no pull-down	n/a	IN_SIG_3_ADC
	PC5	ADC1_INN4	Analog mode	No pull-up and no pull-down	n/a	IN_SIG_4_ADC
	PF11	ADC1_EXTI11	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	
DAC1	PA4	DAC1_OUT1	Analog mode	No pull-up and no pull-down	n/a	SWITCH_LEVEL_DAC
	PA5	DAC1_OUT2	Analog mode	No pull-up and no pull-down	n/a	
DEBUG	PA13 (JTMS/SWDIO)	DEBUG_JTMS-SWDIO	n/a	n/a	n/a	
	PA14 (JTCK/SWCLK)	DEBUG_JTCK-SWCLK	n/a	n/a	n/a	
	PB3 (JTDO/TRACESWO)	DEBUG_JTDO-SWO	n/a	n/a	n/a	
I2C1	PB7	I2C1_SDA	Alternate Function Open Drain	No pull-up and no pull-down	Low	LC24C_SDA
	PB8	I2C1_SCL	Alternate Function Open Drain	No pull-up and no pull-down	Low	LC24C_SCL
I2C2	PF0	I2C2_SDA	Alternate Function Open Drain	No pull-up and no pull-down	Low	
	PF1	I2C2_SCL	Alternate Function Open Drain	No pull-up and no pull-down	Low	
SAI1	PE2	SAI1_MCLK_A	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PE3	SAI1_SD_B	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE4	SAI1_FS_A	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE5	SAI1_SCK_A	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE6	SAI1_SD_A	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PF7	SAI1_MCLK_B	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PF8	SAI1_SCK_B	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PF9	SAI1_FS_B	Alternate Function Push Pull	No pull-up and no pull-down	Low	
SDMMC1	PC8	SDMMC1_D0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC9	SDMMC1_D1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC10	SDMMC1_D2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PC11	SDMMC1_D3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC12	SDMMC1_CK	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD2	SDMMC1_CMD	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
SPI6	PG8	SPI6_NSS	Alternate Function Push Pull	No pull-up and no pull-down	Low	MOTOR_BOARD_NSS
	PG12	SPI6_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Low	MOTOR_BOARD_SPI_MISO
	PG13	SPI6_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Low	MOTOR_BOARD_SPI_CLK
	PG14	SPI6_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Low	MOTOR_BOARD_SPI_MOSI
TIM4	PD12	TIM4_CH1	Alternate Function Push Pull	**Pull-down ***	Low	LED_DATA_OUT
USART2	PA2	USART2_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA3	USART2_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USART3	PB10	USART3_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB11	USART3_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
GPIO	PB0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED
	PF14	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	PUSH_BUTTON_FUNC
	PF15	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	PUSH_BUTTON_FUNC2
	PG0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	OUT_1_DIGI
	PG1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	OUT_2_DIGI
	PE7	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	PUSH_BUTTON_IN_1
	PE8	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	PUSH_BUTTON_IN_2
	PE9	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	PUSH_BUTTON_IN_3
	PE10	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	PUSH_BUTTON_IN_4
	PE12	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	PUSH_BUTTON_OUT_1
	PE13	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	PUSH_BUTTON_OUT_2
	PE14	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	PUSH_BUTTON_OUT_3
	PE15	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	PUSH_BUTTON_OUT_4
	PD8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	PCM1754_B_MUTE
	PD9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	PCM1754_A_MUTE
	PD10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	PCM1754_A_DEMP
	PD11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	PCM1754_B_DEMP
	PG2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	OUT_3_DIGI
	PG3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	OUT_4_DIGI
	PG4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	PCM1754_A_FMT
	PG5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	PCM1754_B_FMT
	PG6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	PCM1754_AB_TEST
	PD0	GPIO_Input	Input mode	**Pull-up ***	n/a	DIP_SW_1
	PD1	GPIO_Input	Input mode	**Pull-up ***	n/a	DIP_SW_2
	PD3	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	DIP_SW_3

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PG9	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	MOTOR_T_NRST
	PG10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MULTI_BOARD_BOOT
	PG11	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	SELF_T_NRST
	PB6	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	CROSS_BOARD_GPIO

8.2. DMA configuration

DMA request	Stream	Direction	Priority
TIM4_CH1	DMA2_Stream0	Memory To Peripheral	**High ***
MEMTOMEM	DMA2_Stream1	Memory To Memory	Low
SAI1_A	DMA1_Stream0	Memory To Peripheral	Low
ADC1	DMA1_Stream1	Peripheral To Memory	Low
SAI1_B	DMA1_Stream2	Memory To Peripheral	Low

TIM4_CH1: DMA2_Stream0 DMA request Settings:

Mode:	**Circular ***
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

MEMTOMEM: DMA2_Stream1 DMA request Settings:

Mode:	Normal
Use fifo:	**Enable ***
FIFO Threshold:	Full
Src Memory Increment:	**Enable ***
Dst Memormy Increment:	**Enable ***
Src Memory Data Width:	**Half Word ***
Dst Memormy Data Width:	**Half Word ***
Src Memory Burst Size:	Single
Dst Memormy Burst Size:	Single

SAI1_A: DMA1_Stream0 DMA request Settings:

Mode:	**Circular ***
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	**Half Word ***
Memory Data Width:	**Half Word ***

ADC1: DMA1_Stream1 DMA request Settings:

Mode:	**Circular ***
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

SAI1_B: DMA1_Stream2 DMA request Settings:

Mode:	**Circular ***
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	**Half Word ***
Memory Data Width:	**Half Word ***

8.3. BDMA configuration

nothing configured in DMA service

8.4. MDMA configuration

nothing configured in DMA service

8.5. NVIC configuration

8.5.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
DMA1 stream0 global interrupt	true	0	0
DMA1 stream1 global interrupt	true	0	0
DMA1 stream2 global interrupt	true	0	0
USART3 global interrupt	true	0	0
DMA2 stream0 global interrupt	true	0	0
SPI6 global interrupt	true	0	0
SAI1 global interrupt	true	0	0
DMAMUX1 overrun interrupt	true	0	0
PVD and AVD interrupts through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1 and ADC2 global interrupts	unused		
TIM2 global interrupt	unused		
TIM4 global interrupt	unused		
I2C1 event interrupt	unused		
I2C1 error interrupt	unused		
I2C2 event interrupt	unused		
I2C2 error interrupt	unused		
USART2 global interrupt	unused		
EXTI line[15:10] interrupts	unused		
SDMMC1 global interrupt	unused		
TIM5 global interrupt	unused		
TIM6 global interrupt, DAC1_CH1 and DAC1_CH2 underrun error interrupts	unused		
DMA2 stream1 global interrupt	unused		
HASH and RNG global interrupts	unused		
FPU global interrupt	unused		
HSEM1 global interrupt	unused		

8.5.2. NVIC Code generation

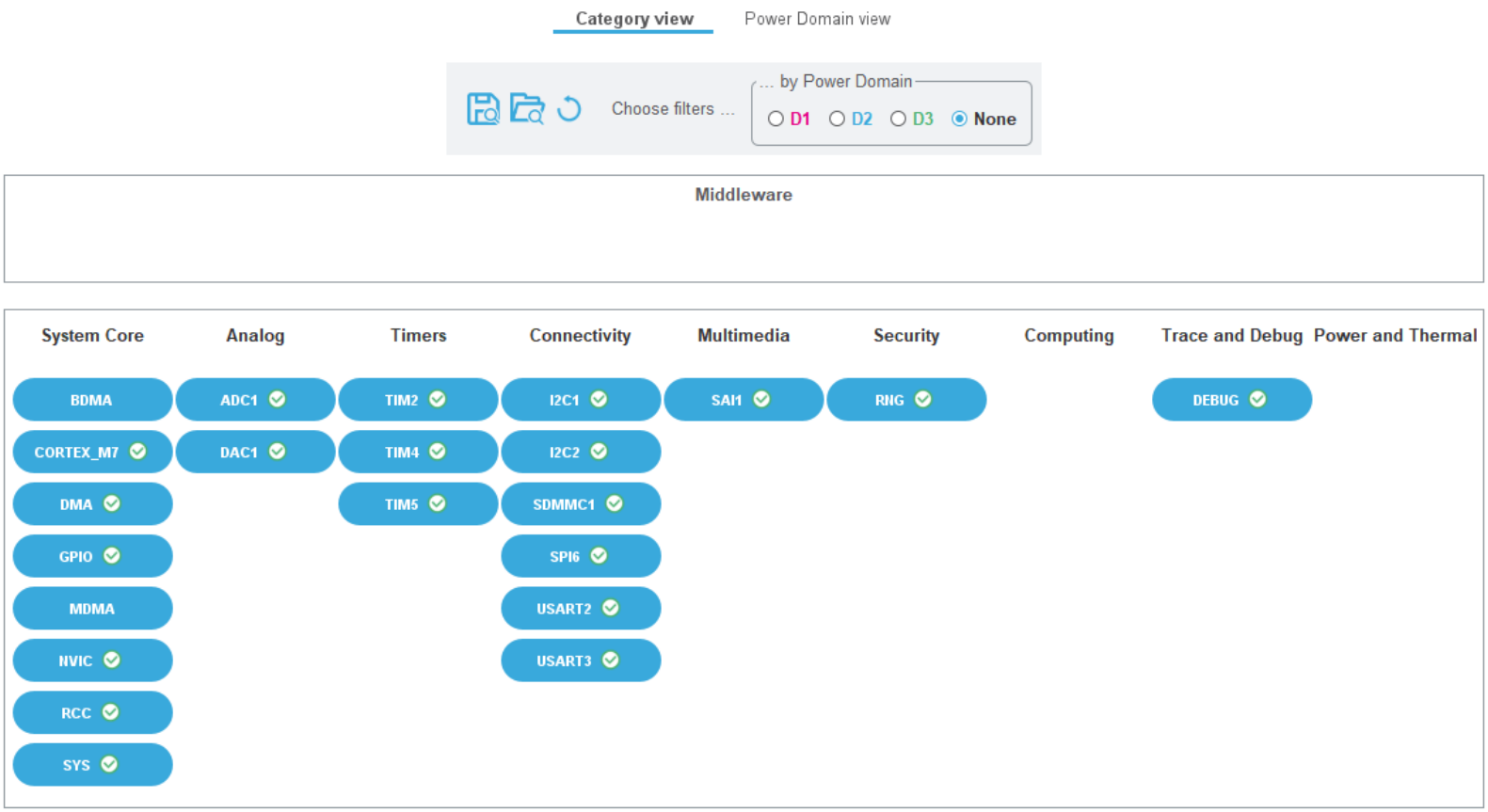
Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	false
DMA1 stream0 global interrupt	false	true	true
DMA1 stream1 global interrupt	false	true	true
DMA1 stream2 global interrupt	false	true	true
USART3 global interrupt	false	true	true
DMA2 stream0 global interrupt	false	true	true
SPI6 global interrupt	false	true	true
SAI1 global interrupt	false	true	true
DMAMUX1 overrun interrupt	false	true	true

*** User modified value**

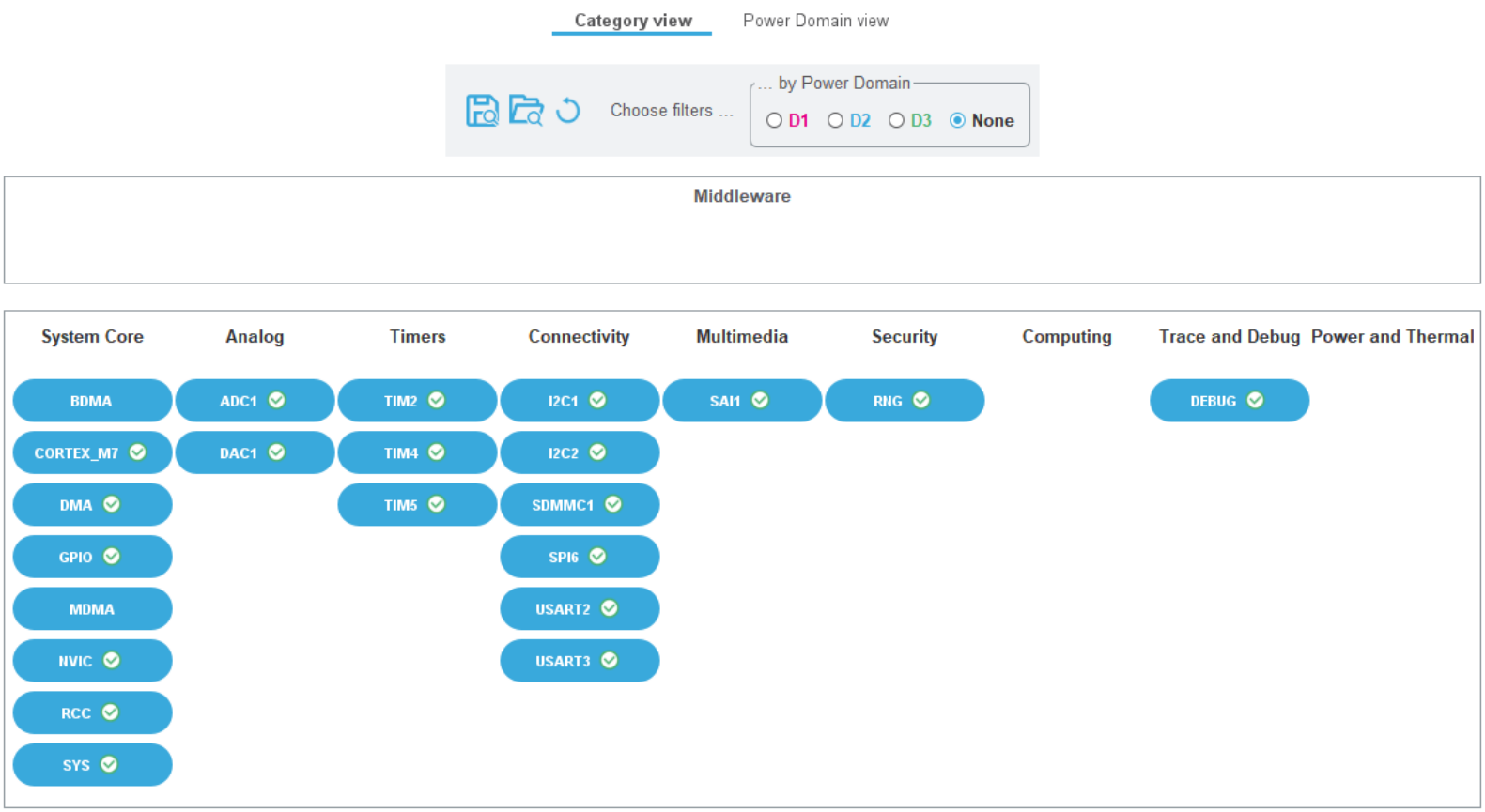
9. System Views

9.1. Category view

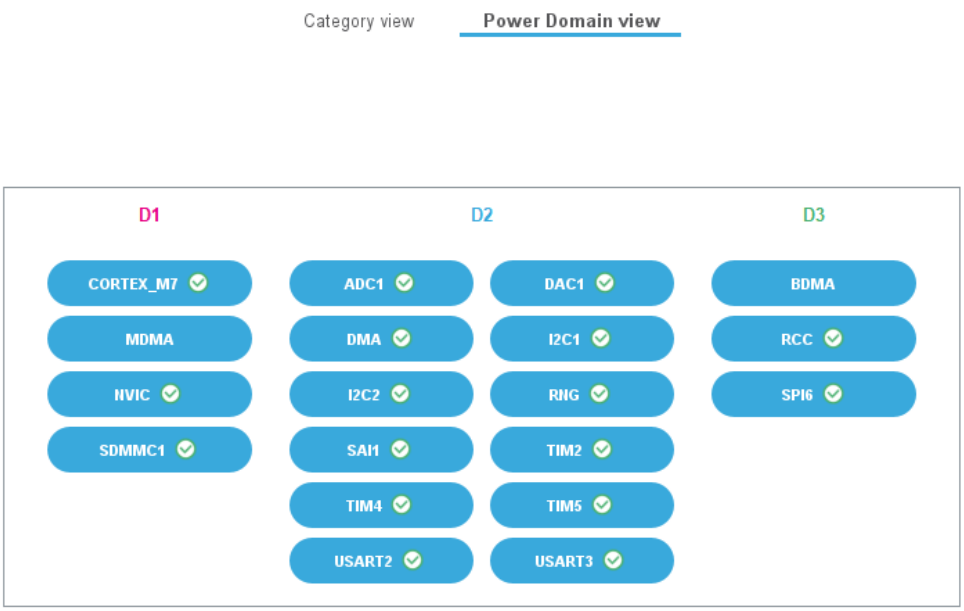
9.1.1. Current



9.1.2. Without filters



9.2. Power Domain view



10. Docs & Resources

Type	Link
Datasheet	http://www.st.com/resource/en/datasheet/DM00387108.pdf
Reference manual	http://www.st.com/resource/en/reference_manual/DM00314099.pdf
Programming manual	http://www.st.com/resource/en/programming_manual/DM00237416.pdf
Errata sheet	http://www.st.com/resource/en/errata_sheet/DM00368411.pdf
Application note	http://www.st.com/resource/en/application_note/CD00167594.pdf
Application note	http://www.st.com/resource/en/application_note/CD00211314.pdf
Application note	http://www.st.com/resource/en/application_note/CD00259245.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264342.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264379.pdf
Application note	http://www.st.com/resource/en/application_note/DM00042534.pdf
Application note	http://www.st.com/resource/en/application_note/DM00072315.pdf
Application note	http://www.st.com/resource/en/application_note/DM00073742.pdf
Application note	http://www.st.com/resource/en/application_note/DM00073853.pdf
Application note	http://www.st.com/resource/en/application_note/DM00081379.pdf
Application note	http://www.st.com/resource/en/application_note/DM00121475.pdf
Application note	http://www.st.com/resource/en/application_note/DM00129215.pdf
Application note	http://www.st.com/resource/en/application_note/DM00151811.pdf
Application note	http://www.st.com/resource/en/application_note/DM00160482.pdf
Application note	http://www.st.com/resource/en/application_note/DM00220769.pdf
Application note	http://www.st.com/resource/en/application_note/DM00227538.pdf
Application note	http://www.st.com/resource/en/application_note/DM00257177.pdf
Application note	http://www.st.com/resource/en/application_note/DM00272912.pdf
Application note	http://www.st.com/resource/en/application_note/DM00272913.pdf
Application note	http://www.st.com/resource/en/application_note/DM00226326.pdf
Application note	http://www.st.com/resource/en/application_note/DM00236305.pdf

Application note	http://www.st.com/resource/en/application_note/DM00296349.pdf
Application note	http://www.st.com/resource/en/application_note/DM00327191.pdf
Application note	http://www.st.com/resource/en/application_note/DM00287603.pdf
Application note	http://www.st.com/resource/en/application_note/DM00337702.pdf
Application note	http://www.st.com/resource/en/application_note/DM00393275.pdf
Application note	http://www.st.com/resource/en/application_note/DM00337873.pdf
Application note	http://www.st.com/resource/en/application_note/DM00354244.pdf
Application note	http://www.st.com/resource/en/application_note/DM00373474.pdf
Application note	http://www.st.com/resource/en/application_note/DM00315319.pdf
Application note	http://www.st.com/resource/en/application_note/DM00356635.pdf
Application note	http://www.st.com/resource/en/application_note/DM00380469.pdf
Application note	http://www.st.com/resource/en/application_note/DM00354333.pdf
Application note	http://www.st.com/resource/en/application_note/DM00395696.pdf
Application note	http://www.st.com/resource/en/application_note/DM00431633.pdf
Application note	http://www.st.com/resource/en/application_note/DM00493651.pdf
Application note	http://www.st.com/resource/en/application_note/DM00535045.pdf
Application note	http://www.st.com/resource/en/application_note/DM00525510.pdf
Application note	http://www.st.com/resource/en/application_note/DM00536349.pdf
Application note	http://www.st.com/resource/en/application_note/DM00609692.pdf
Application note	http://www.st.com/resource/en/application_note/DM00622045.pdf
Application note	http://www.st.com/resource/en/application_note/DM00623136.pdf
Application note	http://www.st.com/resource/en/application_note/DM00625700.pdf
Application note	http://www.st.com/resource/en/application_note/DM00660346.pdf
Application note	http://www.st.com/resource/en/application_note/DM00600614.pdf
Application note	http://www.st.com/resource/en/application_note/DM00628458.pdf
Application note	http://www.st.com/resource/en/application_note/DM00725181.pdf