M.KUMARASAMY
COLLEGE OF ENGINEERING
NAAC Accredited Autonomous Institution
Approved by AICTE & Affiliated to Anna University
ISO 9001:2015 & ISO 14001:2015 Certified Institution
Thalavapalayam, Karur – 639 113.

# A CIRCUIT TECHNIQUE FOR LEAKAGE POWER REDUCTION IN CMOS VLSI CIRCUITS

## A MINOR PROJECT - I REPORT


***Submitted By***

**YUVAPRABHA B** **(927621BEC247)**

**SUBASHINI M** **(927621BEC216)**

**VAISHALI K** **(927621BEC232)**

**SWATHIKA P B** **(927621BEC225)**


**BACHELOR OF ENGINEERING**

in

**DEPARTMENTOF ELECTRONICS AND COMMUNICATION ENGINEERING**

**M.KUMARASAMY COLLEGE OF ENGINEERING**

(Autonomous)

**KARUR – 639 113**

**DECEMBER 2022**

# M.KUMARASAMY COLLEGE OF ENGINEERING, KARUR

## BONAFIDE CERTIFICATE

Certified that this 18ECP103L- Minor Project 1 report "**A CIRCUIT TECHNIQUE FOR LEAKAGE POWER REDUCTION IN CMOS VLSI CIRCUITS**" the bonafide work of "**Yuvaprabha B (927621BEC247),Subashini M (927621BEC216), Vaishali K (92721BEC232),Swathika P B (927621BEC225)**"who carried out the project work under my supervision in the academic year 2022-2023.

**SIGNATURE**
Dr.S.PALANIVELRAJAN, M.E., Ph.D.,
**HEAD OF THE DEPARTMENT,**
Professor,
Department of Electronics and Communication Engineering,
M.Kumarasamy College of Engineering
Thalavapalayam,
Karur-639113.

**SIGNATURE**
Mr.K.SUDHAKAR,M.E.,
**SUPERVISOR**
Assistant Professor,
Department of Electronics and Communication Engineering,
M.Kumarasamy College of Engineering,
Thalavapalayam,
Karur-639113.

This project report has been submitted for the **18ECP103L-Minor Project 1** Viva Voce Examination held at M.Kumarasamy College of Engineering, Karur on _____.

**PROJECT COORDINATOR**

## Vision of the Institution

To emerge as a leader among the top institutions in the field of technical education.

## Mission of the Institution

**M1:** Produce smart technocrats with empirical knowledge who can surmount the global challenges.

**M2:** Create a diverse, fully-engaged, learner-centric campus environment to provide quality education to the students.

**M3:** Maintain mutually beneficial partnerships with our alumni, industry and professional associations.

## Vision of the Department

To empower the Electronics and Communication Engineering students with Emerging Technologies, Professionalism, Innovative Research and Social Responsibility.

## Mission of the Department

**M1:** Attain the academic excellence through innovative teaching teaching learning process, research areas & laboratories and Consultancy projects.

**M2:** Inculcate the students in problem solving and lifelong learning ability.

**M3:** Provide entrepreneurial skills and leadership qualities.

**M4:** Render the technical knowledge and industrial skills of faculties.

## Program Educational Objectives (PEOs):

**PEO1: Core Competence:** Graduates will have a successful career in academia or industry associated with Electronics and Communication Engineering.

**PEO2: Professionalism:** Graduates will provide feasible solutions for the challenging problems through comprehensive research and innovation in the allied areas of Electronics and Communication Engineering.

**PEO3: Lifelong Learning:** Graduates will contribute to the social needs through lifelong learning, practicing professional ethics and leadership quality

## Program Outcomes (POs):

**PO 1: Engineering knowledge:** Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.

**PO 2: Problem analysis:** Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.

**PO 3: Design/development of solutions:** Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

**PO 4: Conduct investigations of complex problems:** Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

**PO 5: Modern tool usage:** Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.

**PO 6: The engineer and society:** Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues, and the consequent responsibilities relevant to the professional engineering practice.

**PO7: Environment and sustainability:**Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development

**PO8: Ethics :**Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice

**PO9: Individual and team work:** Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings

**PO10: Communication:** Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions

**PO11: Project management and finance:** Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments

**PO12: Life-long learning:** Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

## PROGRAM SPECIFIC OUTCOMES(PSO'S)

**PSO1**: Applying knowledge in various areas, like Electronics, Communications, Signal processing, VLSI, Embedded systems etc., in the design and implementation of Engineering application.

**PSO2**: Able to solve complex problems in Electronics and Communication Engineering with analytical and managerial skills either independently or in team using latest hardware and software tools to fulfil the industrialexpectations.

## MAPPING OF PROJET WITH POs AND PSO

| Abstract | Matching with POs , PSOs |
|---|---|
| CMOS,PMOS,NMOS,<br>VLSI,MICMOS,GIDL,<br>PDP | PO1,PO2,PO3,PO4,PO5,PO6,PO7,PO8,PO9<br>PO10,PO11,PO12,PSO1,PSO2 |

# ABSTRACT

Scaling of CMOS technology improved the speed nevertheless the leakage currents are leftover as an adverse effect. The problem has taken a serious turn as the scaling extends into ultra-deep-submicron (UDSM) region. These unsolicited leakage currents should be minimized for the smooth functioning of the circuit. Designing of such leakage free nanoscale CMOS circuits turns to be a challenging task. In this work, we address the issue of leakage power that arises with the device channel length scaling to sub-100nm. We present a circuit technique to mitigate the leakage currents of MOSFET through controlling the voltage at the source terminal of the MOSFET. CMOS inverter designed using the proposed technique results in 98% and 30% improvement in static and total power dissipation respectively compared with its conventional design. The simulation results of NAND and NOR gates designed using the same technique indicates 15.89% and 18.83% improvement in the total power compared with their corresponding conventional designs. 11-stage CMOS ring oscillator designed using the proposed technique is analyzed, and corresponding simulation results are reported. Comparison of the proposed circuits in terms of power dissipation and delay with two existing techniques is presented. The circuits designed using the proposed technique results in good Power-Delay Product (PDP).

# TABLE OF CONTENTS

## LIST OF FIGURES

# LIST OF TABLES

# ACRONYMS/LIST OF ABBREVIATIONS

**CMOS** - Complementary Metal Oxide Semiconductor

**MTCMOS** - Multi threshold CMOS

**VLSI** - Very Large Scale Integration

**MOSFET** - Metal Oxide Semiconductor Field Effect Transistor.

**GIDL** - Gate Induced Drain Leakage

**PDP** - Power-Delay-Product

**VTC** - Voltage transfer characteristic

# CHAPTER 1

# INTRODUCTION

With the rapid technological growth in the semiconductor industry, the high computational and even complex applications are being implemented in a small size VLSI chip with the use of Complementary Metal Oxide Semiconductor (CMOS) technology. Fortunately, the growth in the semiconductor technology is capable of providing required feature size. With the utilization of each new technology node, the speed of the Integrated Circuit (IC) has increased by 30% roughly . The Requirement of high density chips and high speed systems made MOS devices to scale to smaller dimensions that increased the current drive (gm) capability. These smaller transistors and shorter interconnects results in less capacitance and altogether increased the speed of the integrated circuit . Nonetheless, the extent of scaling is constrained by physical limitations such as short-channel effects. The main consequences are the leakage currents contributing to massive static power dissipation. The leakage current increases with the scaling of device channel length. With the overall effect, power dissipation has become the critical issue in the design of microelectronic circuits. Enormous efforts have been paid and need to do more to mitigate these leakage currents. Few of the efforts for reducing leakage currents include techniques, MTCMOS Power Gating, Super Cutoff CMOS Circuit, Forced Transistor Stacking and Sleepy Stack. Multi threshold CMOS (MTCMOS) inserts extra

(s) either PMOS/NOMS or both called sleep transistor(s) into the design. During the normal mode of operation, these transistors set to “on” state without disturbing the functionality of the circuit. During the standby mode, these transistors switched to “off” state to isolate the power supply from the circuit. The isolated supply voltage causes the leakage currents to minimize . Nevertheless, this technique increases the dynamic power dissipation of the circuit. Super Cutoff CMOS, an alternate to MTCMOS uses low threshold voltage sleep transistors instead of high threshold voltage transistors. It turns off sleep transistors with a small negative voltage to reduce the subthreshold leakage current leaving a difficulty of designing of the controller circuit to generate negative gate voltage for the sleep transistors . Stacking is another technique that uses series connected transistors to reduce subthreshold leakage currents. If the natural stacking of transistors does not exist in the circuit, then one can achieve stacking effect by replacing a single transistor with two transistors in the design called forced stacking . This technique works efficiently when more than one transistor in the stack of series connected transistors are in “off” state . Due to extra transistors, this technique results in delay penalty. Sleepy stack is another method that can reduce this delay by adding additional transistor in parallel to the additional stack transistor. However, sleepy stack approach results in higher dynamic power consumption, and it needs an extra complex sleep signal circuitry . LECTOR is a circuit technique for achieving low power dissipation. It inserts two extra transistors in the circuit circuits by using two extra transistors.

## 1.1 OBJECTIVE

The development of digital integrated circuits is challenged by higher power consumption. The combination of higher clock speeds, greater functional integration, and smaller process geometries has contributed to significant growth in power density. Scaling improves transistor density and functionality on a chip. Scaling helps to increase speed and frequency of operation and hence higher performance. As voltages scale downward with the geometries, threshold voltages must also decrease to gain the performance advantages of the new technology, but leakage current increases exponentially. Thinner gate oxides have led to an increase in gate leakage current. Today leakage power has become an increasingly important issue in processor hardware and software design. With the main component of leakage, the sub-threshold current, exponentially increasing with decreasing device dimensions, leakage commands an ever increasing share in the processor power consumption. In 65 nm and below technologies, leakage accounts for 30-40% of processor power. According to the International Technology Roadmap for Semiconductors (ITRS), leakage power dissipation may eventually dominate total power consumption as technology feature sizes shrink. While there are several process technology and circuit-level solutions to reduce leakage in processors, in this paper several novel approaches for reducing both leakage and dynamic power with minimum possible area and delay trade off are proposed.

## 1.2 POWER CONSUMPTION

Power consumed by the CMOS circuit can be devided into three different components.They are:

**1)Dynamic (switching)power consumption**

**2)Short circuit power consumption**

**3)Static (Leakage) power consumption**

### 1)Dynamic (switching) power dissipation

As the name indicates it occurs when signals which goes through the CMOS circuits change their logic state. At this moment energy is drawn from the power supply to charge up the output node capacitance.Charging up of the output capacitnce causes transition from 0V to Vdd.Considering an inverter exaple power drawn from the power supply is dissipated as heat in pMOS transitor.
On the other hand charge down process causes NMOS transistor to dissipate heat.

Output capacitance of the CMOS logic gate consists of below components:

**1)Output node capacitance of the logic gate:** This is due to the drain diffusion region.

**2)Total interconnect capacitance:** This has higher effect as technology node shrinks.

**3)Input node capacitance of the driven gate:** This is due to the gate oxide capacitance.

**2)Short circuit power consumption**

The switching power dissipation is due purely to the energy required to charge and discharge the load capacitance and independent of the rise and fall time of the driving waveform. However, in a CMOS circuit if the rise and fall time have finite rise and fall time value, then for a particular time period during switching both nMOS and pMOS transistors will conduct simultaneously and provide a direct path between VDD and the ground-rail resulting in short circuit power dissipation. The current component that passes through both the nMOS and pMOS transistor during switching does not contribute to the charging of the capacitance in the circuit, and hence, it is called short circuit current.

When the input voltage is below the threshold voltage Vt, only the pMOS transistor is in the active region and the nMOS transistor is completely off. As the rise time of the waveform attains

the value equal to or greater than Vt, the nMOS transistor also starts conducting due to the short circuit current flowing between VDD and GND resulting in short circuit power dissipation.

Pshort = VDD*Ishort

**3)Static (Leakage) power consumption**

Static power is the power consumed when there is no circuit activity or you can say, when the circuit is in quiescent mode. In the presence of a supply voltage, even if we withdraw the clocks and don't change the inputs to the circuit, the circuit will still consume some power, called the static power consumption.

It is mainly due to the leakage currents that flows, when the transistor is in off-state. There are many types of leakage currents, however in the diagram below I have shown only two common leakage currents.

Reverse bias leakage current flows when the junction diodes within the transistors are reverse biased. Similarly sub-threshold leakage current flows from drain to source through the channel, when $V_{GS} \lesssim V_{th}$ [$V_{th}$ is the threshold voltage of the transistor]. Typically the leakage power dissipation in a transistor is inversely proportional to its threshold voltage .

# CHAPTER 2

# LITERATURE REVIEW

## Existing Method

Leakage or static power dissipation occurs due to the presence of various leakage currents such as subthreshold leakage, reverse-bias source/drain junction leakages, gate oxide tunneling leakage, Gate Induced Drain Leakage (GIDL) . Subthreshold leakage current is the dominant leakage current in sub-100nm circuits . Even when the gate voltage is less than the threshold voltage of the device, the current flows between the drain and source due to the diffusion of minority carriers. The subthreshold leakage current, Isub can be expressed as

$$I_{sub} = I_{D0} \times e^{\frac{V_G}{mV_T}} \times (e^{-\frac{V_S}{V_T}} - e^{-\frac{V_D}{V_T}})$$

Subthreshold leakage current is due to the diffusion of minority carriers in the channel of MOS transistor . This current depends on temperature, size of the device, supply voltage and process parameters. For the desired speed of operation, the supply voltage and threshold voltage should be minimized as the CMOS technology subjected to scales down. However, subthreshold current increases exponentially with the decrease in the threshold voltage. The power dissipation of Intel process technologies are shown in Fig1. In 1µm technology the leakage power is only about 0.01% of the active power.

But as the technology scales down to 100 nm, the leakage power contribution raised and became 10 % of the active power dissipation. It means that leakage currents are increasing with the scaling of channel length. This has motivated many researchers to work on it, and many innovations have been proposed to circumvent the leakage power problem.

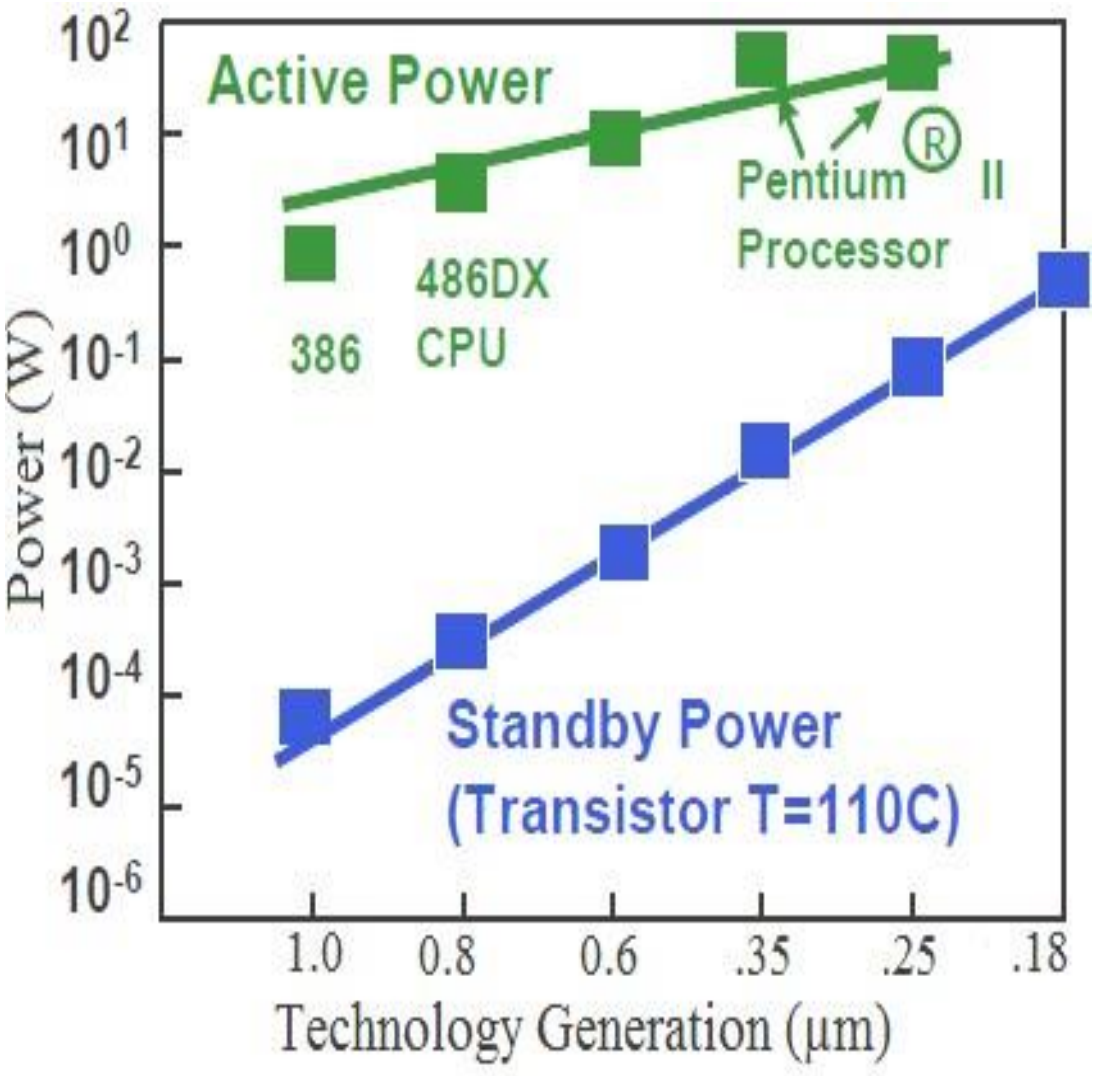



Fig. 1.Power consumption of Intel technologies [8].

# CHAPTER 3

# FEASIBILITY REVIEW

## 3.1 Proposed Method

The basic idea behind our proposed approach is to raise the voltage at the source terminal of the MOS transistor to reduce the leakage currents so as to minimize the static power dissipation. It is known that the subthreshold current increases exponentially with the decrease in the threshold voltage. And it is observed that the threshold voltage of a short channel MOSFET reduces with increase in the drain to source voltage (VDS) . It implies more subthreshold current occurs at higher drain to source voltage. With reference to the subthreshold current equation (1), the subthreshold current can be minimized significantly by decreasing drain to source voltage (VDS). Considering these two facts, subthreshold current can be minimized by reducing the drain to source voltage. Drain to source voltage can be reduced by raising the voltage at the source terminal of the MOSFET called source biasing. For better understanding of the approach, we consider CMOS inverter circuit. The corresponding circuit designed using the proposed approach is shown in Fig. 2 along with the conventional circuit.

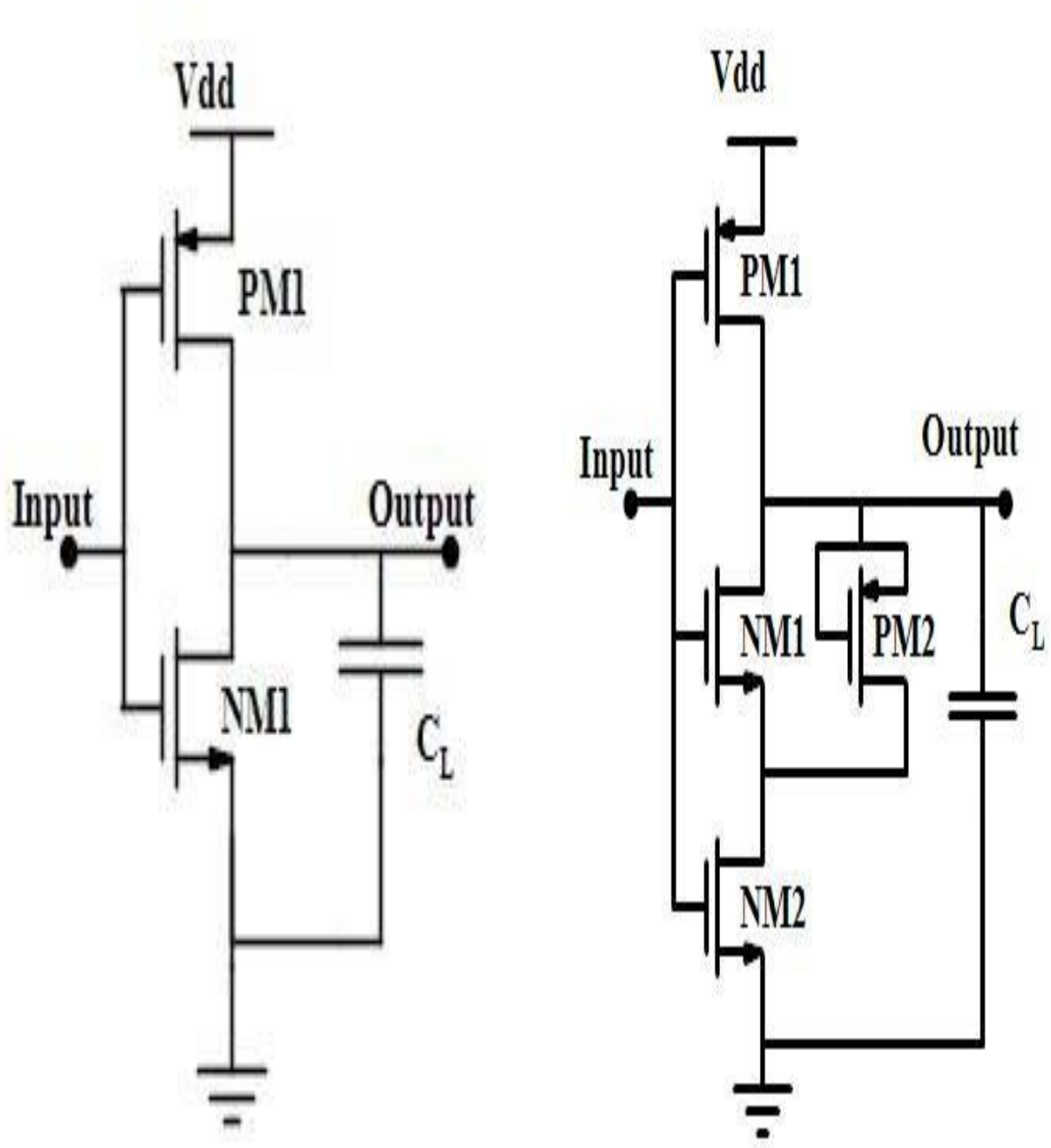



Fig. 2.Circuit schematic of CMOS inverter designed using: (a) Conventional technique, (b) proposed technique.

Here, we have used two extra transistors labeled PM2 (PMOS) and NM2 (NMOS) for the purpose of raising the voltage at the source terminal of the MOSFET. Transistor PM2 is configured to work in "*cut off"* mode (source and gate connected) while the transistor NM2 follows the circuit input conditions. The transistor PM2 is connected between the output node of the circuit and the source terminal of the transistor NM1. The purpose of the transistor PM2 is to supply the leakage currents to the source terminal of the upper NMOS transistor (NM1) to charge the node (source terminal of NM1). During the logic '0' condition at the input, the two NMOS transistors NM1 and NM2 turned *off* and a logic '1' appears at the output node. As the extra PMOS transistor PM2 set to "*cut off"* state, it supplies leakage currents and establishes a certain voltage at the source terminal of the upper NMOS transistor NM2 depending on the amount of leakage current provided by the transistor PM2. The increased source voltage (VS) of the upper NMOS transistor (NM1) reduces the drain-to-source voltage (VDS) of the transistor NM1 and then the subthreshold leakage current. The dependency of node voltage on the width of PMOS transistor PM2 is depicted in Fig. 3.

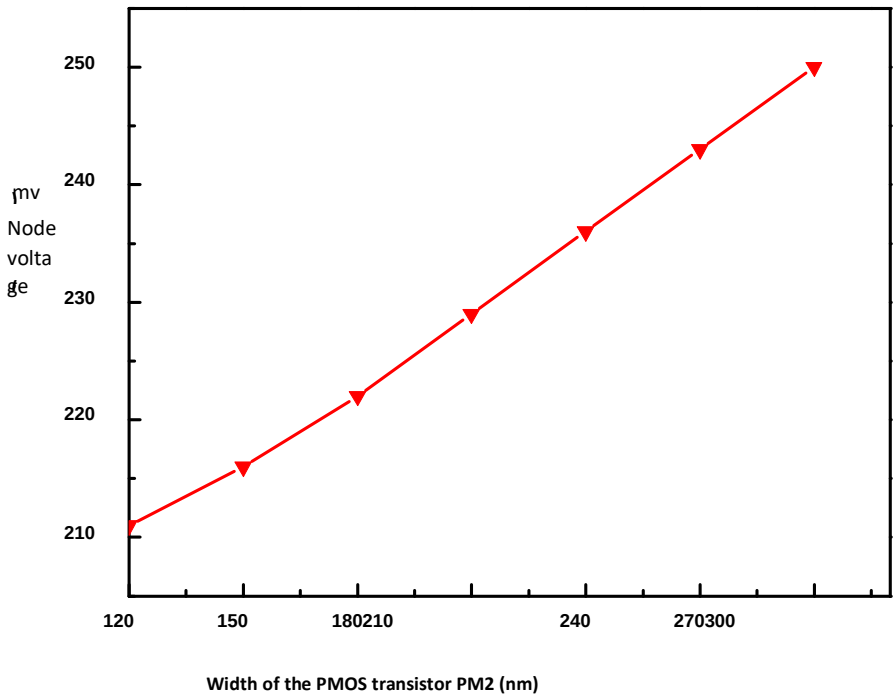



Fig. 3.Dependency of node voltage (source terminal of NM1) on the width of the transistor PM2

The source voltage of the transistor NM2 increases with the width of PM2 as the amount of leakage in PM2 increases with its width. Exclusive charging of source terminal of the lower NMOS transistor (NM1) in the proposed inverter circuit keeps VGS more negative. Voltage transfer characteristic (VTC) for proposed CMOS inverter circuit along with conventional circuits are shown in Fig. 4. The proposed CMOS inverter circuit exhibits good characteristic curve than the circuit designed using LECTOR technique, and it is comparable to the conventional circuit. We have designed NAND and NOR gates using the proposed approach. Using the proposed CMOS inverter, we have designed an 11-stage CMOS ring oscillator. Fig. 5 shows the circuit schematic of NAND gates designed using conventional,

LECTOR and proposed techniques. It also shows the schematic of CMOS inverter designed using LECTOR technique. We have discussed the results of all these circuits in the following section.

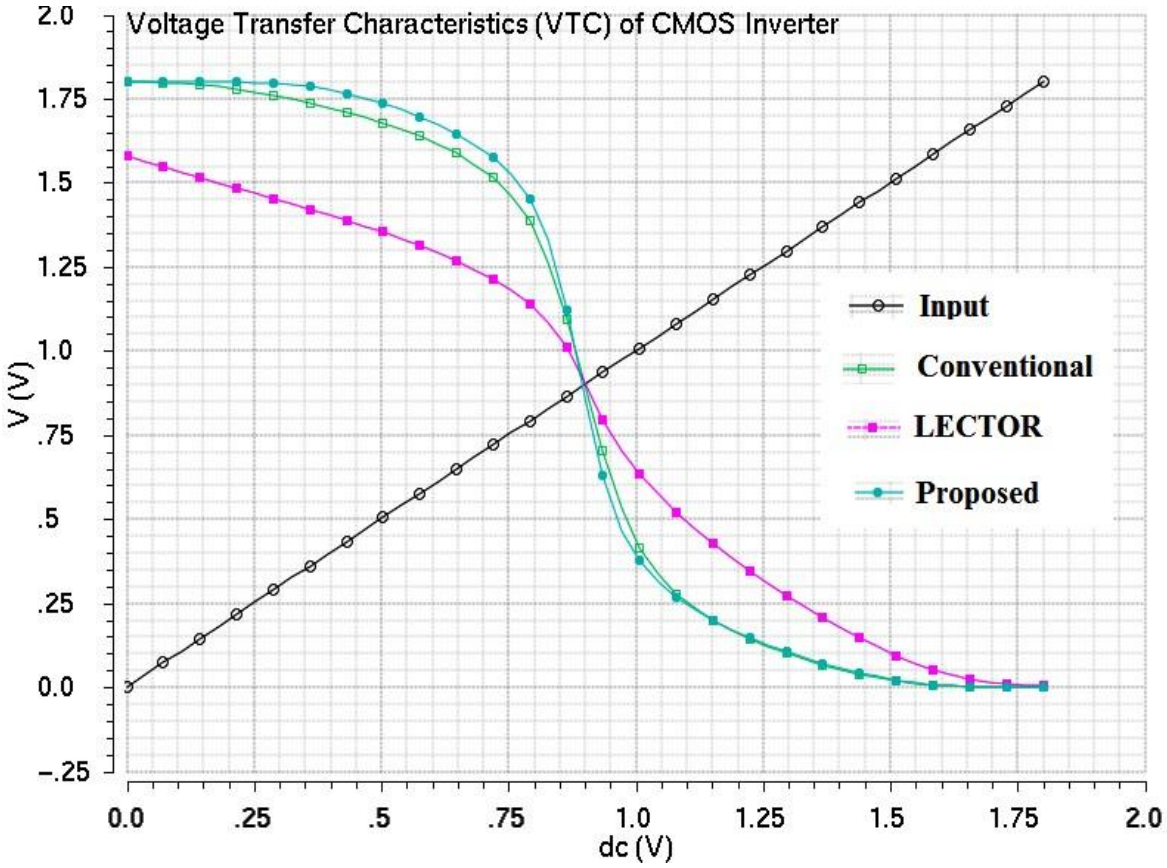
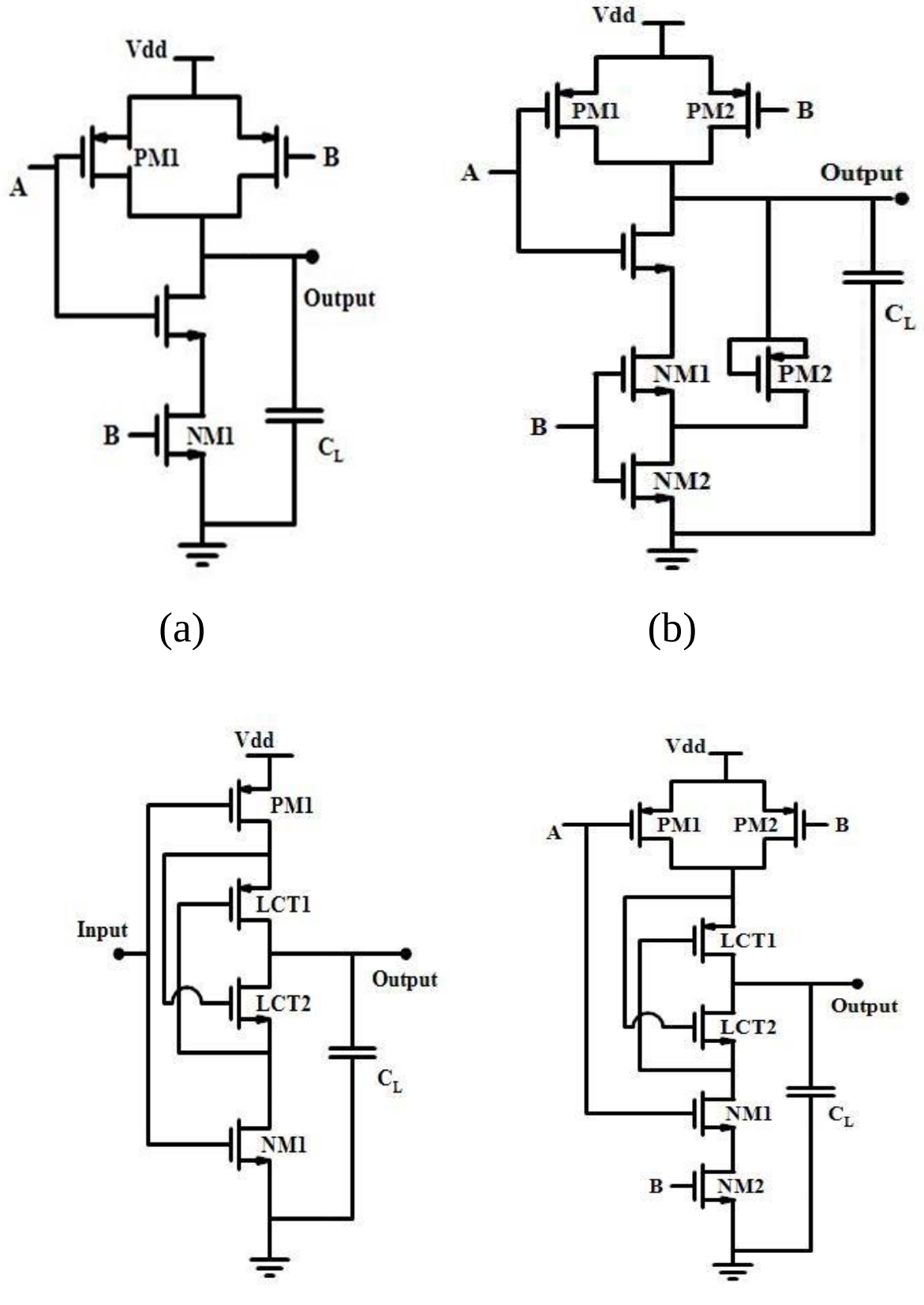



Fig. 4.Voltage Transfer characteristc (VTC) of CMOS Inverter circuit




(a) (b)

(c) (d)Fig. 5.Circuit schematic of: (a) conventional NAND gate, (b) proposed NAND gate, (c) LECTOR CMOS inverter, (d)LECTOR NAND gate.

# CHAPTER 4

## RESULTS AND DICUSSION

In this section, we have made an elaborate discussion on the simulation results of the proposed and conventional designs obtained using 90nm technology file. Simulations are carried out in Cadence Spectre simulation tool. Fig. 6 shows the output waveforms of CMOS inverter circuits designed using conventional, LECTOR and proposed techniques. It is well observed that our proposed circuit results in full swing output voltage similar to the case of conventional circuit.

But the output of the circuit designed using the LECTOR technique does not reach to full swing voltage. The reason could be as at least one among two extra transistors inserted for leakage control set to be “cut off” state at any time, the output voltage may not get full swing. Among two additional transistors, one is inserted in pull-up path and the other is in the pull-down path. In the case of the proposed design, the working mode of the extra transistor (NM2) inserted in the pull down path is similar to the transistor NM1. There is no additional transistor inserted in the pull up path of the proposed circuit. So the circuit can attain full value (logic “1”) at the output.

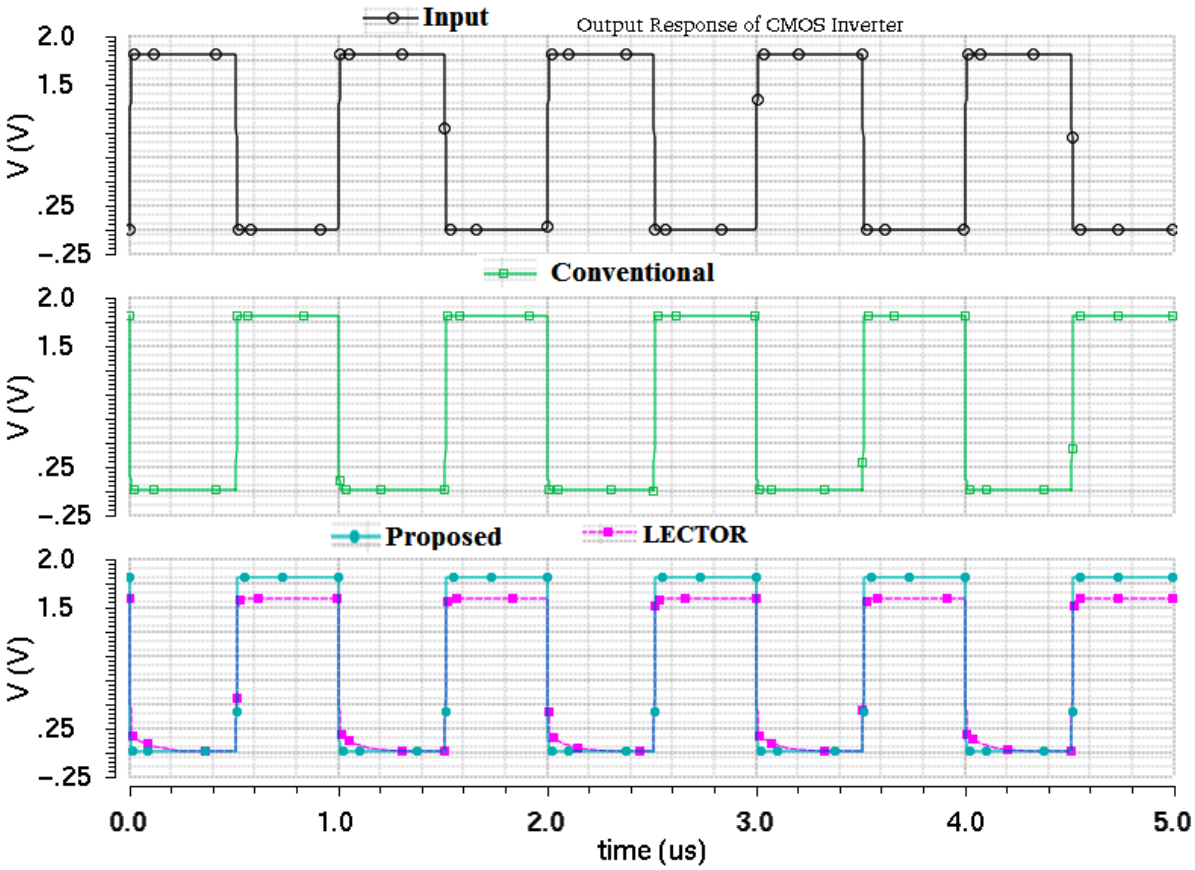



Fig. 6.Output waveforms of CMOS inverter circuit

Table I shows the static power consumption of the CMOS inverter circuit. Proposed CMOS inverter circuit dissipates less power compared to the other two circuits. The total power dissipated by CMOS inverter, 2- input NAND and NOR gates and 11-stage ring oscillator circuits is presented in Table II.

For a considered simulation setup, all the circuits dissipated less power compared to conventional circuits. CMOS inverter and 11-stag ring oscillator designed using proposed approach dissipate less power compared to the corresponding circuits designed using LECTOR technique. Static power consumed by NAND and NOR gates designed

using conventional, LECTOR and proposed circuit techniques is summarized in Table III.

We have listed the leakage power dissipated during each possible input vector. In the table, ‘A’ and ‘B’ represents the inputs to the gate. Power-Delay-Product (PDP) is the important parameter to assess the quality and performance of logic circuits. It represents the energy consumed for switching event. It is preferred to have the least value of PDP for the logic circuits. We measured PDP for the all three designs (conventional, LECTOR and proposed) and summarized in Table IV.

CMOS inverter circuit along with the two logic gates NAND and NOR designed with proposed technique results in less PDP compared with the conventional design. Proposed CMOS inverter exhibits less PDP compared to the CMOS inverter circuit designed through LECTOR approach. PDP plays a significant role in low power designs. On overall comparison, our proposed technique results in full swing operation along with good PDP. All the results of theproposed circuits are obtained by choosing the width of the extra PMOS transistor PM2 equal to 120nm. Extra PMOS transistor PM2 is the transistor connected between the output and the node.

TABLE I. STATIC POWER DISSIPATION OF CMOS INVERTER

| **Circuit/ Design** | **Conventional (w)** | **LECTOR (w)** | **Propos ed (w)** | **% Improvement comparison with** | |
|---|---|---|---|---|---|
| | | | | **Conventional** | **LECTOR** |
| CMOS Inverter | 489.2 $e^{-9}$ | 253.9 $e^{-9}$ | 8.9 $e^{-9}$ | 98.2 $e^{-9}$ | 96.5 $e^{-9}$ |

TABLE II. TOTAL POWER DISSIPATION

| **Circuit/Technique** | **Conventional (µw)** | **LECTOR (µw)** | **Propos ed (µw)** | **Improvement (%) Comparison with** | |
|---|---|---|---|---|---|
| | | | | **conventional** | **LECTOR** |
| Inverter | 1.35 | 0.96 | 0.94 | 30.7 | 2.81 |
| NAND | 0.89 | 0.66 | 0.75 | 15.9 | -13.1 |
| NOR | 1.13 | 0.76 | 0.92 | 18.8 | -20.3 |
| 11-stage RO | 296.67 | 318.9 | 285.1 | 3.9 | 10.6 |

TABLE III. STATIC POWER DISSIPATION OF NAND AND NOR GATES

| **Input vector** | | **Conventional (nw)** | | **LECTOR (nw)** | | **Proposed (nw)** | |
|---|---|---|---|---|---|---|---|
| **A** | **B** | **NAND** | **NOR** | **NAND** | **NOR** | **NAND** | **NOR** |
| 0 | 0 | 9.67 | 1008 | 9.53 | 508.47 | 9.69 | 528.89 |
| 0 | 1 | 569.6 | 47.5 | 285.69 | 35.82 | 572.77 | 47.49 |
| 1 | 0 | 336.3 | 16.12 | 278.21 | 14.31 | 7.97 | 16.12 |
| 1 | 1 | 9.96 | 0.07 | 6.08 | 0.07 | 9.96 | 0.07 |

## TABLE IV. POWER-DELAY PRODUCT(PDP)

| **Design** | **Conventional (J)** | **LECTOR (J)** | **Proposed (J)** |
|---|---|---|---|
| Inverter | 854.66 $e^{-18}$ | 707.31 $e^{-18}$ | 621.73 $e^{-18}$ |
| NAND | 537.84 $e^{-18}$ | 451.76 $e^{-18}$ | 447.97 $e^{-18}$ |
| NOR | 457.32 $e^{-18}$ | 358.48 $e^{-18}$ | 377.21 $e^{-18}$ |

# CHAPTER 5

# CONCLUSION

In this paper, a low leakage power circuit technique that controls the source voltage of the MOSFET through the leakage currents of another MOSFET is presented. Maximum improvement in the power dissipation depends upon the amount of leakage currents that are supplied to the source terminal of the subjected MOSFET. CMOS inverter circuit designed using the proposed technique results in full swing operation along with better power improvement. 11-stage ring oscillator designed using proposed technique attained 3.9 % and 10 % improvement in the total power consumption compared with the conventional and LECTOR techniques respectively. Power-delay product of the proposed circuits improved well compared with conventional designs. The proposed CMOS inverter can be used in the design of inverter based designs like SRAM, CMOS ring oscillator for low power operation.

# CHAPTER 6
# REFERENCES

[1] Chenming C. Hu, Modern Semiconductor Devices for Integrated Circuits, 1st ed. New Jersey: Prentice Hall, 2010.

[2] B.S. Deepaksubramanyan and Adrian Nunez, "Analysis of subthreshold leakage reduction in CMOS digital circuits," in Proc.13th NASA VLSI Symposium, POST FALLS, IDAHO, USA, June 2007, pp. 1-8.

[3] Kaushik Roy, Saibal Mukhopadhyay and Hamid Mahmoodi Meimand, "Leakage current mechanisms and leakage reduction techniques in deepsubmicrometer CMOS circuits," Proc. IEEE, vol. 91, no.2, pp. 305-327, February 2003.

[4] Ndubuisi Ekekwe and Ralph Etienne-Cummings, "Power dissipation sources and possible control techniques in ultra deep submicron CMOS technologies," Microelectronics Journal, vol. 37, pp.851-860, September 2006.

[5] Narender Hanchate, and Nagarajan Ranganathan, "LECTOR: a technique for leakage reduction in CMOS circuits," IEEE Trans. Very Large Scale Integration (VLSI) Systems, vol. 12, no. 2, pp. 196-205, February 2004.