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NMAM INSTITUTE OF TECHNOLOGY, NITTE

(An Autonomous Institution affiliated to VTU, Belagavi)

III Sem B.E. (CSE/ISE) Mid Semester Examinations - II, October 2016

15CS302/15IS302 – DIGITAL SYSTEMS DESIGN

on: 1 Hour Max. Marks: 20

*Note: Answer any **One** full question from **each Unit.***

		Marks	BTL*
	Unit – I		
a)	Explain in detail, the design of positive edge triggered RS flip flop along with its timing diagram	06	L*4
b)	Synthesize an SR flip flop using D flip flop	04	L5
a)	Obtain characteristic equation, finite state machine and excitation table for the following flip flop: i. RS flip flop ii. D flip flop iii. JK flip flop	06	L4
b)	With circuit diagram and truth table, explain the working of JK master slave flip flop	04	L2
	Unit – II		
a)	Explain in detail working of serial-in serial-out shift register.	05	L2
b)	Design and explain sequence generator and sequence detector circuit using shift register	05	L4
a)	List and explain different types of shift register along with block diagram	06	L1
b)	Along with state table, explain the design of switch tail counter.	04	L2

Bloom's Taxonomy, L* Level

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NMAM INSTITUTE OF TECHNOLOGY, NITTE

(An Autonomous Institution affiliated to VTU, Belagavi)

Third Semester B.E. (CSE) (Credit System) Degree Examinations

November - December 2019

18CS302 – DIGITAL SYSTEM DESIGN

ation: 3 Hours

Max. Marks: 100

ote: *Answer* ***Five full*** *questions choosing* ***Two full*** *questions from* ***Unit – I*** *and* ***Unit – II each*** *and* ***One full*** *question from* ***Unit – III.***

		Marks	BT*	CO*	PO*
	Unit – I				
a)	Define gate? Show universality of NAND and NOR gate.	6	L*1	2	1
b)	Develop an HDL using Verilog to implement the half adder and full adder circuit separately.	6	L3	2	1,2
c)	Illustrate different models for writing Verilog modules. Give an example for each.	8	L1	2	1,2
a)	Solve the expression $F(A,B,C,D)=\sum m(0,1,2,5,6,7,9,10,11,14)$ using Quine Mcklusky method to derive prime implicants and essential prime implicants.	10	L3	1	1
b)	Distinguish between Positive Logic and Negative Logic. Show that a positive AND gate is equivalent to negative OR gate.	5	L2	2	1
c)	Apply the Karnaugh map technique to simplify the function for the expression $F(W,X,Y,Z)= \sum m\ (0,1,2,4,5,12,14)+dc(8,10)$	5	L2	2	1,2
a)	Solve the expression $F(A,B,C,D)=\sum m(7,9,12,13,14,15)+d(4,11)$ using Quine Mcklusky method to derive prime implicants and essential prime implicants.	10	L3	1	1
b)	Apply the Karnaugh map technique to simplify the function in POS form for the expression $F(A,B,C,D)= \pi M\ (0,1,4,5,8,9,11)+d(2,10)$	5	L3	1	1,2
c)	Prove that $ABC + ABC' + AB'C + A'BC = AB + AC + BC$	5	L3	1	1
	Unit – II				
a)	Show the behavioral model in Verilog for 4:1 multiplexer.	5	L1	3	3
b)	Why Multiplexer can be called as Universal Logic Circuit? Explain nibble multiplexer with neat diagram.	5	L2	3	2
c)	Design and explain the role of X-OR gate in i. Parity checker and generator circuit ii. Adder/Subtractor circuit.	10	L2	3	1
a)	Construct 4:1 multiplexer using 2:1 multiplexer	5	L3	3	2
b)	Implement the following for Full Adder i. Truth table and circuit diagram using NAND ii. HDL code.	10	L3	3	1,2
c)	Develop 4:1 multiplexer using the function $F(A,B,C)=\sum m(0,1,2,7)$	5	L3	2	1
a)	What is Decoder? Develop a Full subtractor circuit using 3 to 8 Decoder circuit and multi-input OR gate.	6	L3	4	2
b)	Explain in detail 1-bit magnitude comparator.	4	L2	4	
c)	What do you mean by ripple adder? With the help of fast adder circuit measure the expression for 4 bit carry?	10	4	3	2

P.T.O.

a) Analyze edge triggered JK flip flop. Explain its operations with respect to logic diagram, logic symbol, truth table and timing diagram. 8 L4

b) Derive characteristic equation, state transition diagram, Excitation table of SR and T flip flop. 6 L4

c) Design a sequence detector using Moore model that receives Binary data stream at its input X, & signals when a combination '011' arrives at the input by making output Y high. 6 L4

Unit – IV

a) Design 4-bit serial input serial output shift register using D flip-flop. Draw the waveforms to shift the number 0100 into this shift register. Assume that it has 4 bit number QRST=1010 stored in it. List the sequence of events occurred. 6 L6

b) Design a modulo-4 irregular counter with following count sequence using D flip-flop.

c) Explain in detail applications of shift register. 8 L4

a) Design a 4-BIT switched tail counter with D flip-flop. Also explain its state table. 6 L2

b) Design a self correcting modulo-6 counter using JK flip flop in which all the unused states leads to state CBA=000. Design the circuit diagram for the mentioned counter. 6 L2

c) With a neat block diagram explain parallel in parallel out register. 8 L4

Unit – V

a) What is principle of working of counter method ADC? 6 L2

b) Explain D/A converter testing

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Third Semester B.E. (CSE/ISE) (Credit System) Degree Examinations

November - December 2016

15CS302/15IS302 – DIGITAL SYSTEMS DESIGN

ion: 3 Hours | Max. Marks: 100

*Note: Answer **Five full** questions choosing **One full** question from **each Unit.***

		Marks	BT*
	Unit – I		
a)	What is meant by don't care condition on Karnaugh Map? How can using don't care aid circuit simplification? Get the minimized sum of product expression for $f(a,b,c,d) = \sum m(1,4,8,9,13,14,15) + d(2,3,11,12)$	8	L*5
b)	Use boolean algebra to simplify the following expressions. I. ABC+ABC'+AB'C+A'BC II. A(A'+C)(A'B+C)(A'BC+C') Design the circuit for the simplified expressions.	6	L6
c)	Design the circuit for the expression y=AB+CD and implement the verilog HDL code for the same including test bench (Use any type of Verilog modeling Techniques).	6	L5
a)	What are universal gates? Realize the following function using universal gates only. F = ((A+B)'C)' D	6	L4
b)	Simplify the following expression using Quine Mc Clusky Method. $F = \sum m(1,2,8,9,12,13,14,15)$ Design the circuit for minimized expression using NAND gates only.	8	L6
c)	Minimize the following function using K-map method and express it in SOP form. Also realize logic circuits using NAND gates only. $f(a,b,c,d) = \sum m(7,9,10,11,12,13,14,15)$	6	L5
	Unit – II		
a)	What is decoder? Design a circuit that realizes following three functions using a decoder and OR gates. $F1=\sum m(1,4,6)$ F2=A'BC+A F3=A'B'+AC	6	L4
b)	Design half adder using only NAND gates.	2	L6
c)	Implement u=ad+bc'+bd using I. 8:1 Mux II. 4:1 Mux	12	L4
a)	Design full adder using PROM. Explain in detail how does PROM differs from PAL?	6	L6
b)	State and explain the applications of EXOR gate.	5	L2
c)	Implement 1-bit comparator using a 2:4 decoder.	7	L6
d)	Write Verilog HDL code for 2:1 multiplexer using condition statement.	2	L1
	Unit – III		
a)	What is switch contact bounce? Explain in detail how SR latch is used to eliminate Switch Contact Bounce. Also show the waveforms of switch bounce and debounce.	6	L4
b)	Design NOR gate latch and NAND gate latch. Also explain its truth table.	6	L6
c)	Implement SR flip flop using D flip flop. Write the Verilog HDL code for D flip flop.	8	L4

P.T.O.

5	a)	What is Multiplexer? Realize a 4:1 multiplexer using NAND gates only and briefly explain its working.	07	L3
	b)	Implement full subtractor using demultiplexer.	07	L4
	c)	Implement following Boolean function decoder. $F_1(a,b,c) = \sum m(0,1,3,5)$ $F_2(a,b,c) = \sum m(3,5,7)$	06	L4
6	a)	Realize full adder using minimum number of NAND gates and give the relevant expressions and truth table.	07	L4
	b)	What is magnitude comparator? Design two bit magnitude comparator using basic gates.	06	L2
	c)	Write a note on Parity Generator and Checkers.	07	L3

Unit – III

7.	a)	Give state transition diagram of SR, D, JK and T Flip – Flop.	08	L2
	b)	With a neat logic and timing diagram, explain the working of a 4 – bit SISO register.	08	L3
	c)	Differentiate synchronous and asynchronous counters.	04	L2
8.	a)	Design synchronous mod-5 up counter using JK Flip-Flop.	10	L6
	b)	With a neat block diagram, explain Mealy and Moore model.	10	L2

BT* Bloom's Taxonomy, L* Level

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NMAM INSTITUTE OF TECHNOLOGY, NITTE

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III Sem B.E. (CSE) Mid Semester Examinations - II, October 2019

Duration: 1 Hour

18CS302 – DIGITAL SYSTEMS DESIGN

Max. Marks: 20

*Note: Answer any **One** full question from **each Unit**.*

			Marks	BT*	CO*	PO*
		Unit – I				
1.	a)	Show the realization of given functions f1(a,b,c) = ∑ m(1,4,6,7) and f2(a,b,c) = ∑ m(2,3,5) using 3 – to – 8 line decoder.	2	L*1	3	1,12
	b)	Design and explain the role of X-OR gate in 8 bit Parity checker and even parity generator circuit.	4	L2	3	1,12
	c)	Explain the design and working of common anode type seven segment decoder driver in detail.	4	L2	3	1,12
2.	a)	Illustrate the design and working of Decimal to BCD encoder.	2	L3	3	1,12
	b)	Obtain two bit comparator equations by using the logic of one bit comparator truth table. Also design the circuit for one bit comparator.	4	L2	3	1,12
	c)	Construct a digital circuit for 2 bit fast adder showing the required logic.	4	L3	3	1,12
		Unit – II				
3.	a)	Explain the Construction and working of Negative edge Triggered RS Flip flop in detail.	4	L2	4	1,12
	b)	Explain the construction and working of 4 bit serial adder and subtractor circuit. With an example, show the addition and subtraction performed by the same.	4	L2	4	1,12
	c)	Compare and contrast Combinational circuit and Sequential circuit	2	L5	4	1,12
4.	a)	List out various representations of SR and JK flip-flop.	4	L1	4	1,12
	b)	With the help of timing diagram explain JK Master-Slave flip-flop	4	L2	4	1,12
	c)	Perform the following in 2's complement arithmetic operation: i. Add +25 and +75 ii. Subtract +25 from +75	2	L2	4	1,12

BT* Bloom's Taxonomy, L* Level; CO* Course Outcome; PO* Program Outcome

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NMAM INSTITUTE OF TECHNOLOGY, NITTE

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III Sem B.E. (CSE) Mid Semester Examinations - I, September 2019

18CS302 – DIGITAL SYSTEMS DESIGN

Duration: 1 Hour | Max. Marks: 20

*Note: Answer any **One** full question from **each Unit.***

			Marks	BT*	CO*	PO*
		Unit – I				
1.	a)	Define positive and negative logic. Prove that a positive NOR is equal to negative NAND.	3	L*1	1	1
	b)	Outline the Verilog code for the design of half adder.	2	L2	1	1
	c)	Apply Karnaugh Map technique to solve the given expression F(A,B,C,D) = ∑m(0,1,3,4,5,9,11,13,15).	3	L3	2	1
	d)	Illustrate the realization of the given expression using NAND gates only $Y = \overline{AB} + CD$.	2	L2	1	1
2.	a)	What are universal gates? Prove the universality of NAND gate.	3	L1	1	1
	b)	Show the realization of the following expression using only NOR gates $Y = (a + c).(\overline{b} + \overline{d}).(\overline{a} + \overline{b} + \overline{c})$	2	L2	1	1
	c)	Apply Karnaugh Map technique to simplify the given expression F(A,B,C,D) = ∑m(7,9,11,12,13,14) + d(3,5,6,15) to get the final expression in Product of Sum method.	3	L3	2	1
	d)	Outline the Verilog code for the given expression Y=(A+B).(C+D)	2	L2	1	1
		Unit – II				
3.	a)	Apply the QM method to simplify the given expression F(A,B,C,D)=∑m(0,2,3,4,8,10,12,13,14) to derive prime implicants and essential prime implicants.	7	L3	2	1
	b)	Show the implementation of the given function f(a,b,c,d) =∑m(0,1,5,6, 7, 9, 10, 15) using 4 to 1 Mux with a & b as control inputs.	3	L2	2	1
4.	a)	Apply the QM method to simplify the given expression F(A,B,C,D)=∑m(2,3,10,11,12,13,14,15) + d(0,1) to derive prime implicants and essential prime implicants.	8	L3	2	1
	b)	Explain the working of 8 to 1 multiplexer in detail.	2	L2	2	1

BT* Bloom's Taxonomy, L* Level; CO* Course Outcome; PO* Program Outcome

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NMAM INSTITUTE OF TECHNOLOGY, NITTE

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III Sem B.E. (CSE) Mid Semester Examinations - I, September 2016

15CS302 – DIGITAL SYSTEM DESIGN

Time: 1 Hour Max. Marks: 20

*Note: Answer any **One** full question from **each Unit.***

		Marks	BT*
	Unit – I		
a)	By applying Quine Mc Clusky method find the Prime implicants for the given expressions f(a,b,c,d)=∑m(0,2,3,5,8,10,11)	6	L*3
b)	Prove the following i. DeMorgan's 1st law ii. Universality of Nand gate	4	L4
a)	Compute the following Boolean Expression using K- Map. f(a,b,c,d)=∑m(0,2,5,7,8,10,13,15)+dc(1,4,11,14)	6	L5
b)	Construct verilog code and logic circuit for the expression y=(A+B). (C+D)	4	L6
	Unit – II		
a)	Construct 8:1 multiplexer using following expression f(a,b,c,d)=∑m(0,2,5,7,8,10,13,15)	6	L6
b)	Design Half Adder circuit using NAND gates only.	4	L6
a)	Implement the following function using 3 to 8 line decoder f1(A,B,C)=Σm(0,4,6,7) f2(A,B,C)=Σm(1,4,5)	4	L6
b)	Explain 4:1 multiplexer with Block diagram, truth table and circuit diagram.	6	L2

* Bloom's Taxonomy, L* Level

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17CS302 SEE – November – December 2018

Unit – III

a)	Develop and explain serial- in- parallel- out shift register.	5	L2	5	2
b)	How Shift registers can be used in the construction of Sequence detector and Serial adder.	10	L3	5	1
c)	Explain the working of a RS flip-flop with the help of Timing diagram.	5	L2	5	1
a)	Compare Moore and Mealy model.	5	L2	5	1
b)	Construct mod-6 up counter by state synthesis process.	8	L3	5	1
c)	With the help of timing diagram explain Ripple Counter.	7	L3	5	2

Bloom's Taxonomy, L* Level; CO* Course Outcome; PO* Program Outcome

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Third Semester B.E. (CSE) (Credit System) Degree Examinations

November - December 2018

17CS302 – DIGITAL SYSTEMS DESIGN

ration: 3 Hours

Max. Marks: 100

Note: Answer ***Five full*** *questions choosing* ***Two full*** *questions from* ***Unit – I*** *and* ***Unit – II each*** *and* ***One full*** *question from* ***Unit – III.***

		Marks	BT*	CO*	PO*
	Unit – I				
a)	How can you prove that a NOR gate is an universal gate.	5	L*1	1	1
b)	Explain positive and negative logic in detail.	4	L2	1	1
c)	Develop an HDL using verilog to implement the half adder and full adder circuit separately.	6	L3	2	1
d)	Design the circuit for an expression y = ((A+B)(A' + B')) using NAND gates only.	5	L3	2	1
a)	Find out the simplified expression for the function F(A,B,C,D) = ∑m (3,4,5,7,9,13,14,15) using karnaugh map technique.	5	L1	1	1
b)	Solve the expression F(A,B,C,D) = ∑m (1,3,6,7,9,10,12,13,14,15) using Quine Mcklusky method to derive prime implicants and essential prime implicants.	10	L3	1	1
c)	Explain the structure of verilog program in detail.	5	L2	2	1
a)	Outline the circuit for the expression Y=AB+C' using only NOR gates.	5	L2	2	1
b)	Solve the expression F(A,B,C,D) = ∑m (0,1,2,3,10,11,12,13,14,15) using Quine Mcklusky method to derive prime implicants and essential prime implicants.	10	L3	1	1
c)	How can you prove that a bubbled AND gate is equivalent to a NOR gate.	5	L1	1	1
	Unit – II				
a)	Find the Boolean expressions for the three outputs of 4-bit magnitude comparator circuit having X and Y as inputs.	4	L1	3	1
b)	Outline the truth table of half adder and full adder. Find the simplified expressions for the outputs of a full adder. Prepare the NAND-only circuit for half adder.	10	L2	4	1
c)	Solve for the difference for the following, using 2's complement method. 1) +83 and +16 2)-43 and -78	6	L3	4	1
a)	Show the implementation of 4:1 mux in Verilog using data flow modeling technique.	6	L1	3	2
b)	Build a digital circuit that performs both addition and subtraction on 4-bit binary data. Briefly interpret it's working. Identify its drawbacks.	8	L3	4	2
c)	List the building blocks of arithmetic circuits. Build and describe a circuit that generates the 1's complement of a 4-bit binary sequence using XOR gates.	6	L1	4	2
a)	Explain the logic circuit for 2-bit fast adder generating the equations for sum and carry.	10	L2	4	1
b)	Define an encoder with its block diagram. What is the drawback of a normal encoder? Design a truth table to overcome the same.	10	L1	3	1

P.T.O.

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Third Semester B.E. (CSE) (Credit System) Degree Examinations

November - December 2017

16CS302 – DIGITAL SYSTEMS DESIGN

ation: 3 Hours Max. Marks: 100

Note: Answer ***Five full*** *questions choosing* ***Two full*** *questions from* ***Unit-I, Unit – II*** *and* ***One full*** *question from* ***Unit –III.***

		Marks	BT*
	Unit – I		
a)	What are universal gates? Realize $((\overline{A+B}).C)$ using only NAND gates.	05	L*2
b)	Simplify the following Boolean expression using K-Map and implement the same using (i) only NAND gates (ii) using only NOR gates $F(A,B,C,D)=\sum m(0,1,2,4,5,12,14)+dc(8,10)$	08	L5
c)	Find the prime implicants and essential prime implicants for the following Boolean expression using Quine-McClusky method. $F(A,B,C,D)=\sum m(1,2,3,5,9,12,14,15)+\sum d(4,8,11)$	07	L5
a)	Write the truth table of the logic circuit having 3-inputs A, B, C and the output expressed as: Y= $\bar{A}B\bar{C}$ + $\bar{A}B\bar{C}$ +AB$\bar{C}$ also simplify the expression using Boolean algebra and implement the logic circuit using NAND gates.	06	L4
b)	What is Positive and Negative logic? Explain.	04	L2
c)	A digital system is to be designed in which the months of the year is given as input in four bit form. The month January is represented as "0000", February as "0001" and so on. The output of the system should be "1" corresponding to the input of the month containing 31days or otherwise it is "0". Consider the excess numbers in the input beyond "1011" as don't care conditions. For this system of four variables (A, B, C, D), find the following: i) Give the truth table and simplify by using K-Map ii) Boolean expression in SOP and POS form iii) Implement the simplifies equation using NAND-NAND gates and NOR-NOR gates	10	L6
a)	Explain different implementation models used in HDL.	08	L4
b)	What are the drawbacks of K-Map? Find the prime implicants and essential prime implicants for the following Boolean expression using Quine-McClusky method. $F(A,B,C,D)=\sum m(1,3,6,7,9,1012,13,14,15)$ Write the gate diagram for the simplified equation using NAND-NAND gates.	12	L5
	Unit – II		
a)	Implement the Boolean function expressed by SOP: $F(A,B,C,D)=\sum m(1,2,5,6,9,12)$ using 8-to-1 MUX.	05	L5
b)	Implement a full adder using a 3-to-8 decoder.	05	L4
c)	Design and explain 7 – segments decoder. .	06	L3
d)	Show the 8-bit addition of these decimal numbers in 2's complement representation (i) +28, -15 (ii) +45, +56	04	L4

P.T.O.

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III Sem B.E. (CSE) Mid Semester Examinations - II, October 2018

17CS302- DIGITAL SYSTEMS DESIGN

ation: 1 Hour | Max. Marks: 20

*Note: Answer any **One** full question from **each Unit.***

	Unit – I	Marks	BT*	CO*	PO*
a)	Explain the construction and working of 8 bit parity checker in detail	4	L*2	3	1
b)	Show the realization of given functions f1(a,b,c) = ∑ m(1,4,6,7) and f2 (a,b,c) = ∑ m(2,3,5) using 3 –to – 8 line decoder	2	L1	3	1
c)	Illustrate the design of 1 bit magnitude comparator. Show how can you derive the Boolean expressions for 3 bit magnitude comparator using 1 bit comparator logic	4	L3	3	1
a)	Explain the design and working of common anode type seven segment decoder driver in detail	3	L2	3	1
b)	Illustrate the design and working of Decimal to BCD encoder	3	L3	3	1
c)	Demonstrate the construction and working of 8 bit even parity generator	4	L2	3	1
	Unit - II				
a)	Solve the following using 2's complement arithmetic system: i. Add +125 and -68 ii. Add +37 and -115 iii. Subtract -27 from +68	3	L3	4	2
b)	Construct a digital circuit for 2 bit fast adder showing the required logic.	4	L3	4	1
c)	Explain the Construction and working of RS Flip flop in detail.	3	L2	4	1
a)	Build and explain 4 bit adder subtractor circuit that can perform both addition and subtraction. Also perform the arithmetic following operations using its logic: i. Add +3 and +2 ii. Subtract +2 from +3	4	L1	4	2
b)	Explain the construction and working of gated D flip flop	3	L2	4	1
c)	Develop a Verilog code for the design of 3 to 8 line decoder	3	L3	4	2

[* Bloom's Taxonomy, L* Level; CO* Course Outcome; PO* Program Outcome

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NMAM INSTITUTE OF TECHNOLOGY, NITTE

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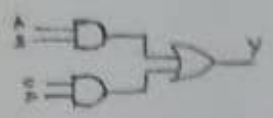
III Sem B.E. (CSE) Mid Semester Examinations - I, September 2017

16CS302 – DIGITAL SYSTEMS DESIGN

Duration: 1 Hour | Max. Marks: 20

*Note: Answer any **One** full question from **each Unit**.*

			Marks	BT*
		Unit – I		
1.	a)	Write the dual of an expression F(A,B,C)=A.B+B.C+C.A. Prove that the expression is also self-dual	2	L*2
	b)	Realize the expression Y=a'b + ac using only NOR gates	2	L3
	c)	Solve the following: i. Simplify the given expression f(a, b, c, d)= ∑m(0,2,5,7,8,10,13,15) + d(1,4,11,14) using Kamaugh map ii. Express the expression f(a, b, c, d)=πM(4,7,11,12) in Product Of Sum form	3 1	L3
	d)	Write the Verilog code to design the following circuit 	2	L1
2.	a)	Realize the expression Y=(a+c)(b'+d')(a'+b'+c') using only NAND gates	2	L3
	b)	Write a Verilog code to design a circuit that consist of a two input AND gate	2	L1
	c)	Solve the expression f(a, b, c, d) = πM(0,1,4,5,8,9,11) + d(2,10) using Kamaugh map to get the final expression in Product Of Sum form.	3	L3
	d)	Solve the following: i. Given a function f(a, b, c)=πM(0,3,5). Write its Sum Of Product Equation ii. Prove that (A+B)' = A'.B'	1 2	L2
		Unit – II		
3.	a)	Simplify the given expression F(A,B,C,D)=∑m(0,1,2,3,10,11,12,13,14,15) using QM method to derive the prime implicants and essential prime implicants	6	L3
	b)	Solve the following i. Implement f(a,b,c)=∑m(0,4,5,6) using 8-to-1 Multiplexer ii. implement f(a,b,c)=∑m(0,1,2,7) using 4-to-1 Multiplexer. Consider A & B as control inputs and C as data input	1 3	L4
4.	a)	Simplify f(a,b,c,d)=∑m(7,9,12,13,14,15) + d(4,11) using QM method to derive prime implicants and essential prime implicants	7	L3
	b)	Solve the following: i. Give the truth table and logical expression of 4-to-1 Multiplexer ii. Realize Y=A'B+B'C'+ABC using an 8-to-1 Multiplexer	3	L4

BT* Bloom's Taxonomy, L* Level

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NMAM INSTITUTE OF TECHNOLOGY, NITTE

(An Autonomous Institution affiliated to VTU, Belagavi)

III Sem B.E. (CSE) Mid Semester Examinations - I, September 2018

17CS302 - DIGITAL SYSTEM DESIGN

Duration: 1 Hour

Max. Marks: 20

*Note: Answer any **One** full question from **each Unit.***

			Marks	BT*	CO*	PO*
		Unit – I				
1.	a)	Show that a NAND gate is equivalent to bubbled or gate	2	L*1	1	1,12
	b)	Apply the realization using only NAND gates to realize the expression a'b + ab'	2	L3	1	1,12
	c)	Simplify f(A,B,C,D) = πM(0,1,2,3,4,7) using Karnaugh map technique to get the expression in SOP and POS form.	4	L3	1	1,12
	d)	Design a Verilog code to implement half adder circuit	2	L2	1	1,12
2.	a)	Solve the following functions using karnaugh map technique: 1. f(A,B,C,D) = ∑ m(3,4,5,6,7,9,13,14,15) 2. f(A,B,C,D) = ∑ m (7) + d(10, 11, 12, 13, 15)	4	L3	1	1,12
	b)	Apply the realization using only NOR gates to realize the expression Y= ((A+B)C)'D	3	L3	2	1,12
	c)	Define a positive and negative logic. Show that a positive AND is equal to negative OR	2	L1	2	1,12
	d)	Build the expression in SOP for f(a,b,c)= πM(0,3,5)	1	L3	2	1,12
		Unit – II				
3.	a)	Simplify F(A,B,C,D) =∑m(2,3,10,11,12,13,14,15) + d(0,1) using QM method to derive the prime implicants and essential prime implicants.	5	L3	1	1,12
	b)	Design function f(A,B,C)=∑m(1,4,5,7) using 4-to-1 Multiplexer. Consider A & B as control inputs and C as data input	3	L6	2	1,12
	c)	Illustrate the three modeling techniques used in verilog	2	L2	1	1,12
4.	a)	Explain the design of 8-to-1 multiplexer in detail	3	L2	2	1,12
	b)	Simplify F(a,b,c,d) = ∑m(0,1,2,5,10,11,14,15) using QM method to derive the prime implicants and essential prime implicants	5	L3	1	1,12
	c)	show how 4 to 1 multiplexer can be obtained from 2-to-1 multiplexer	2	L1	2	1,12

BT* Bloom's Taxonomy, L* Level; CO* Course Outcome; PO* Program Outcome

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NMAM INSTITUTE OF TECHNOLOGY, NITTE

(An Autonomous Institution affiliated to VTU, Belagavi)

III Sem B.E. (CSE) Mid Semester Examinations - II, October 2017

16CS302 – DIGITAL SYSTEMS DESIGN

uration: 1 Hour | Max. Marks: 20

*Note: Answer any **One** full question from **each Unit**.*

			Marks	BT*
		Unit – I		
I.	a)	How do you differentiate a demultiplexer from a decoder? Realize the following Boolean expression using 3-to-8 decoder and multi-input OR gates. $F1(A,B,C)=\sum m(1,2,3,5)$; $F2(A,B,C)=\sum m(1,7)$; $F3(A,B,C)=\sum m(0,5,6,7)$	2	L*1
	b)	Demonstrate the construction and working of 8 bit parity checker circuit in detail with an example.	3	L2
	c)	What is a magnitude comparator? Explain the design of 1 bit magnitude comparator in detail.	5	L2
2.	a)	Explain the design of common cathode type decoder in detail.	4	L2
	b)	Illustrate the working of odd parity generator circuit with an example.	3	L2
	c)	Construct and explain decimal-to-BCD encoder circuit.	3	L3
		Unit – II		
3.	a)	Solve the following binary arithmetic operations using 2's complement system i. add +43 and -19 ii. Subtract +25 from +77	4	L3
	b)	Explain the working of positive edge triggered D flip flop in detail along with the timing diagram.	4	L5
	c)	Explain the construction of a 4 bit controlled inverter along with an example.	2	L3
4.	a)	Explain the design of a 8 bit adder/subtractor. Analyze the total delay occurred for performing the 8 bit addition/subtraction. Perform the following operation using the concept of 8 bit adder/subtractor circuit I. Add +33 and +51 ii. Subtract +31 from +61	6	L4
	b)	With the help of truth table and timing diagram, explain the working of positive edge triggered RS flipflop.	4	L5

* Bloom's Taxonomy, L* Level

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18CS302 SEE – November – December 2019

Unit – III

a)	List and explain various characteristic equations of SR, D, JK and toggle flip-flop.	10	L2	5	1
b)	Develop and explain serial- in- parallel- out shift register.	5	L2	5	2
c)	Explain the working of a RS flip-flop with the help of Timing diagram.	5	L2	5	1
a)	Construct mod-6 up counter by state synthesis process.	8	L3	5	1
b)	Develop and Explain switch tail Counter with timing diagram.	6	L2	5	2
c)	Develop With the help of timing diagram explain Ripple Counter.	6	L3	5	2

* Bloom's Taxonomy, L* Level; CO* Course Outcome; PO* Program Outcome

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