```
===== QOR =====
============================================================
  Generated by:           Genus(TM) Synthesis Solution 21.14-s082_1
  Generated on:           Feb 27 2026  12:54:02 pm
  Module:                 RISC_V
  Operating conditions:   slow (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
============================================================

Timing
--------

Clock  Period
--------------
clk   10000.0


  Cost    Critical         Violating
 Group   Path Slack  TNS     Paths
-------------------------------------
clk          6803.8   0.0          0
default    No paths   0.0
-------------------------------------
Total                 0.0          0

Instance Count
--------------
Leaf Instance Count             122
Physical Instance count           0
Sequential Instance Count        30
Combinational Instance Count     92
Hierarchical Instance Count       0

Area
----
Cell Area                         0.000
Physical Cell Area                0.000
Total Cell Area (Cell+Physical)   0.000
Net Area                          0.000
Total Area (Cell+Physical+Net)    0.000

Max Fanout                        306 (debug_pc[1])
Min Fanout                        0 (n_141)
Average Fanout                    4.3
Terms to net ratio                3.1097
Terms to instance ratio           3.9508
Runtime                           80.256678 seconds
Elapsed Runtime                   3250 seconds
Genus peak memory usage           1817.04
Innovus peak memory usage         no_value
Hostname                          ic312.vit.ac.in

===== CLOCK =====
============================================================
  Generated by:           Genus(TM) Synthesis Solution 21.14-s082_1
  Generated on:           Feb 27 2026  12:54:02 pm
  Module:                 RISC_V
  Operating conditions:   slow (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
============================================================
```

Clock Description

Clock Name	Period	Rise	Fall	Clock Domain	Source Pin/Port	No of Registers
clk	10000.0	0.0	5000.0	domain_1	clk	30

Clock Network Latency / Setup Uncertainty

Clock	Network Latency Rise	Network Latency Fall	Source Latency Rise	Source Latency Fall	Setup Uncertainty Rise	Setup Uncertainty Fall
clk	0.0	0.0	0.0	0.0	0.0	0.0

Clock Relationship (with uncertainty & latency)

From	To	R->R	R->F	F->R	F->F
clk	clk	10000.0	5000.0	5000.0	10000.0

===== TIMING SUMMARY =====

===== TOP 10 PATHS =====

```
============================================================
  Generated by:           Genus(TM) Synthesis Solution 21.14-s082_1
  Generated on:           Feb 27 2026  12:54:02 pm
  Module:                 RISC_V
  Operating conditions:   slow (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
============================================================


Path 1: MET (6804 ps) Setup Check with Pin Program_Counter_pc_reg[31]/CK->D
          Group: clk
     Startpoint: (R) Program_Counter_pc_reg[2]/CK
          Clock: (R) clk
       Endpoint: (R) Program_Counter_pc_reg[31]/D
          Clock: (R) clk

                     Capture       Launch
        Clock Edge:+   10000            0
       Src Latency:+       0            0
       Net Latency:+       0 (I)        0 (I)
           Arrival:=   10000            0

             Setup:-     119
     Required Time:=    9881
      Launch Clock:-       0
         Data Path:-    3078
             Slack:=    6804

#-------------------------------------------------------------------------------
---------------
#        Timing Point          Flags    Arc   Edge   Cell     Fanout Load Trans Delay A
rrival Instance
#                                                                 (fF)   (ps)   (ps)
 (ps)  Location
```

```
#-------------------------------------------------------------------------------
---------------
  Program_Counter_pc_reg[2]/CK -       -      R     (arrival)     30    -     0     0
     0    (-,-)
  Program_Counter_pc_reg[2]/QN -       CK->QN F     DFFRX4         2  7.6    53   353
   353    (-,-)
  g118042__5107/Y              -       A->Y   R     NOR2X6         2  2.3    39    45
   398    (-,-)
  g118182/Y                    -       AN->Y  R     NOR2BX4        3  2.1    51   134
   533    (-,-)
  g118181/Y                    -       AN->Y  R     NOR2BX4        2  2.3    53   140
   673    (-,-)
  g118180/Y                    -       AN->Y  R     NOR2BX4        2  4.5    69   149
   821    (-,-)
  g118023/Y                    -       A->Y   F     INVX4          2  8.5    49    50
   872    (-,-)
  g118012__1881/Y              -       D->Y   R     NOR4X8         2  2.5   111    56
   928    (-,-)
  g118179/Y                    -       AN->Y  R     NOR4BX4        2  2.5   140   204
  1132    (-,-)
  g118176/Y                    -       AN->Y  R     NOR4BX4        2  2.5   140   215
  1346    (-,-)
  g118173/Y                    -       AN->Y  R     NOR4BX4        2  2.5   140   215
  1561    (-,-)
  g118170/Y                    -       AN->Y  R     NOR4BX4        2  2.5   140   215
  1776    (-,-)
  g118168/Y                    -       AN->Y  R     NOR4BX4        2  2.3   137   213
  1989    (-,-)
  g118167/Y                    -       AN->Y  R     NOR2BX4        2  2.3    53   172
  2162    (-,-)
  g118166/Y                    -       AN->Y  R     NOR2BX4        2  2.3    53   140
  2302    (-,-)
  g118165/Y                    -       AN->Y  R     NOR2BX4        2  2.3    53   140
  2442    (-,-)
  g118164/Y                    -       AN->Y  R     NOR2BX4        2  2.3    53   140
  2583    (-,-)
  g118163/Y                    -       AN->Y  R     NOR2BX4        2  2.3    53   140
  2723    (-,-)
  g118162/Y                    -       AN->Y  R     NOR2BX4        1  1.5    47   137
  2860    (-,-)
  g2/Y                         -       B->Y   F     XNOR2X4        1  0.9    58   172
  3033    (-,-)
  g117902__2398/Y              -       B->Y   R     NOR2X1         2  0.7    51    45
  3078    (-,-)
  Program_Counter_pc_reg[31]/D -       -      R     DFFRHQX4       2    -     -     0
  3078    (-,-)
#-------------------------------------------------------------------------------
---------------
```

```
Path 2: MET (7040 ps) Setup Check with Pin Program_Counter_pc_reg[30]/CK->D
          Group: clk
     Startpoint: (R) Program_Counter_pc_reg[2]/CK
          Clock: (R) clk
       Endpoint: (R) Program_Counter_pc_reg[30]/D
          Clock: (R) clk

                    Capture       Launch
        Clock Edge:+   10000            0
       Src Latency:+       0            0
       Net Latency:+       0 (I)        0 (I)
           Arrival:=   10000            0
```

```
             Setup:-     124
     Required Time:=    9876
      Launch Clock:-       0
         Data Path:-    2836
             Slack:=    7040

#-------------------------------------------------------------------------------
---------------
#        Timing Point          Flags    Arc   Edge   Cell     Fanout Load Trans Delay A
rrival Instance
#                                                                  (fF)   (ps)   (ps)
 (ps)  Location
#-------------------------------------------------------------------------------
---------------
  Program_Counter_pc_reg[2]/CK -       -      R     (arrival)     30    -     0     0
    0    (-,-)
  Program_Counter_pc_reg[2]/QN -       CK->QN F     DFFRX4         2  7.6    53   353
  353    (-,-)
  g118042__5107/Y              -       A->Y   R     NOR2X6         2  2.3    39    45
  398    (-,-)
  g118182/Y                    -       AN->Y  R     NOR2BX4        3  2.1    51   134
  533    (-,-)
  g118181/Y                    -       AN->Y  R     NOR2BX4        2  2.3    53   140
  673    (-,-)
  g118180/Y                    -       AN->Y  R     NOR2BX4        2  4.5    69   149
  821    (-,-)
  g118023/Y                    -       A->Y   F     INVX4          2  8.5    49    50
  872    (-,-)
  g118012__1881/Y              -       D->Y   R     NOR4X8         2  2.5   111    56
  928    (-,-)
  g118179/Y                    -       AN->Y  R     NOR4BX4        2  2.5   140   204
  1132    (-,-)
  g118176/Y                    -       AN->Y  R     NOR4BX4        2  2.5   140   215
  1346    (-,-)
  g118173/Y                    -       AN->Y  R     NOR4BX4        2  2.5   140   215
  1561    (-,-)
  g118170/Y                    -       AN->Y  R     NOR4BX4        2  2.5   140   215
  1776    (-,-)
  g118168/Y                    -       AN->Y  R     NOR4BX4        2  2.3   137   213
  1989    (-,-)
  g118167/Y                    -       AN->Y  R     NOR2BX4        2  2.3    53   172
  2162    (-,-)
  g118166/Y                    -       AN->Y  R     NOR2BX4        2  2.3    53   140
  2302    (-,-)
  g118165/Y                    -       AN->Y  R     NOR2BX4        2  2.3    53   140
  2442    (-,-)
  g118164/Y                    -       AN->Y  R     NOR2BX4        2  2.3    53   140
  2583    (-,-)
  g118163/Y                    -       AN->Y  R     NOR2BX4        2  2.3    53   140
  2723    (-,-)
  g117907__8428/Y              -       S0->Y  F     MXI2X1         1  0.9    81    61
  2784    (-,-)
  g117905__6260/Y              -       B->Y   R     NOR2X1         2  0.7    52    52
  2836    (-,-)
  Program_Counter_pc_reg[30]/D -       -      R     DFFRX4         2    -     -     0
  2836    (-,-)
#-------------------------------------------------------------------------------
---------------
```

Path 3: MET (7181 ps) Setup Check with Pin Program_Counter_pc_reg[29]/CK->D

```
         Group: clk
     Startpoint: (R) Program_Counter_pc_reg[2]/CK
          Clock: (R) clk
       Endpoint: (R) Program_Counter_pc_reg[29]/D
          Clock: (R) clk

                    Capture       Launch
        Clock Edge:+   10000            0
       Src Latency:+       0            0
       Net Latency:+       0 (I)        0 (I)
           Arrival:=   10000            0

             Setup:-     124
     Required Time:=    9876
      Launch Clock:-       0
         Data Path:-    2696
             Slack:=    7181

#-------------------------------------------------------------------------------------------
----------------
#        Timing Point          Flags    Arc   Edge   Cell     Fanout Load Trans Delay A
rrival Instance
#                                                                  (fF)   (ps)   (ps)
 (ps)  Location
#-------------------------------------------------------------------------------------------
----------------
  Program_Counter_pc_reg[2]/CK -       -      R     (arrival)     30    -     0     0
    0    (-,-)
  Program_Counter_pc_reg[2]/QN -       CK->QN F     DFFRX4         2  7.6    53   353
  353    (-,-)
  g118042__5107/Y              -       A->Y   R     NOR2X6         2  2.3    39    45
  398    (-,-)
  g118182/Y                    -       AN->Y  R     NOR2BX4        3  2.1    51   134
  533    (-,-)
  g118181/Y                    -       AN->Y  R     NOR2BX4        2  2.3    53   140
  673    (-,-)
  g118180/Y                    -       AN->Y  R     NOR2BX4        2  4.5    69   149
  821    (-,-)
  g118023/Y                    -       A->Y   F     INVX4          2  8.5    49    50
  872    (-,-)
  g118012__1881/Y              -       D->Y   R     NOR4X8         2  2.5   111    56
  928    (-,-)
  g118179/Y                    -       AN->Y  R     NOR4BX4        2  2.5   140   204
  1132    (-,-)
  g118176/Y                    -       AN->Y  R     NOR4BX4        2  2.5   140   215
  1346    (-,-)
  g118173/Y                    -       AN->Y  R     NOR4BX4        2  2.5   140   215
  1561    (-,-)
  g118170/Y                    -       AN->Y  R     NOR4BX4        2  2.5   140   215
  1776    (-,-)
  g118168/Y                    -       AN->Y  R     NOR4BX4        2  2.3   137   213
  1989    (-,-)
  g118167/Y                    -       AN->Y  R     NOR2BX4        2  2.3    53   172
  2162    (-,-)
  g118166/Y                    -       AN->Y  R     NOR2BX4        2  2.3    53   140
  2302    (-,-)
  g118165/Y                    -       AN->Y  R     NOR2BX4        2  2.3    53   140
  2442    (-,-)
  g118164/Y                    -       AN->Y  R     NOR2BX4        2  2.3    53   140
  2583    (-,-)
  g117912__6783/Y              -       S0->Y  F     MXI2X1         1  0.9    81    61
  2643    (-,-)
  g117908__5526/Y              -       B->Y   R     NOR2X1         2  0.7    52    52
```

```
  2696    (-,-)
  Program_Counter_pc_reg[29]/D -       -      R     DFFRX4          2    -     -     0
  2696    (-,-)
#-------------------------------------------------------------------------------------
---------------



Path 4: MET (7321 ps) Setup Check with Pin Program_Counter_pc_reg[28]/CK->D
         Group: clk
     Startpoint: (R) Program_Counter_pc_reg[2]/CK
         Clock: (R) clk
       Endpoint: (R) Program_Counter_pc_reg[28]/D
         Clock: (R) clk

                    Capture       Launch
       Clock Edge:+   10000            0
      Src Latency:+       0            0
      Net Latency:+       0 (I)        0 (I)
          Arrival:=   10000            0

            Setup:-     124
     Required Time:=    9876
      Launch Clock:-       0
         Data Path:-    2555
             Slack:=    7321

#-------------------------------------------------------------------------------------
---------------
#        Timing Point          Flags    Arc   Edge   Cell     Fanout Load Trans Delay A
rrival Instance
#                                                                 (fF)   (ps)   (ps)
 (ps)  Location
#-------------------------------------------------------------------------------------
---------------
  Program_Counter_pc_reg[2]/CK -       -      R     (arrival)     30    -     0     0
     0    (-,-)
  Program_Counter_pc_reg[2]/QN -       CK->QN F     DFFRX4         2  7.6    53   353
   353    (-,-)
  g118042__5107/Y              -       A->Y   R     NOR2X6         2  2.3    39    45
   398    (-,-)
  g118182/Y                    -       AN->Y  R     NOR2BX4        3  2.1    51   134
   533    (-,-)
  g118181/Y                    -       AN->Y  R     NOR2BX4        2  2.3    53   140
   673    (-,-)
  g118180/Y                    -       AN->Y  R     NOR2BX4        2  4.5    69   149
   821    (-,-)
  g118023/Y                    -       A->Y   F     INVX4          2  8.5    49    50
   872    (-,-)
  g118012__1881/Y              -       D->Y   R     NOR4X8         2  2.5   111    56
   928    (-,-)
  g118179/Y                    -       AN->Y  R     NOR4BX4        2  2.5   140   204
  1132    (-,-)
  g118176/Y                    -       AN->Y  R     NOR4BX4        2  2.5   140   215
  1346    (-,-)
  g118173/Y                    -       AN->Y  R     NOR4BX4        2  2.5   140   215
  1561    (-,-)
  g118170/Y                    -       AN->Y  R     NOR4BX4        2  2.5   140   215
  1776    (-,-)
  g118168/Y                    -       AN->Y  R     NOR4BX4        2  2.3   137   213
  1989    (-,-)
  g118167/Y                    -       AN->Y  R     NOR2BX4        2  2.3    53   172
  2162    (-,-)
```

```
  g118166/Y                     -       AN->Y  R     NOR2BX4        2  2.3    53   140
  2302    (-,-)
  g118165/Y                     -       AN->Y  R     NOR2BX4        2  2.3    53   140
  2442    (-,-)
  g117917__2802/Y               -       S0->Y  F     MXI2X1         1  0.9    81    61
  2503    (-,-)
  g117914__1617/Y               -       B->Y   R     NOR2X1         2  0.7    52    52
  2555    (-,-)
  Program_Counter_pc_reg[28]/D  -       -      R     DFFRX4         2    -     -     0
  2555    (-,-)
#-------------------------------------------------------------------------------------
----------------


Path 5: MET (7461 ps) Setup Check with Pin Program_Counter_pc_reg[27]/CK->D
          Group: clk
     Startpoint: (R) Program_Counter_pc_reg[2]/CK
          Clock: (R) clk
       Endpoint: (R) Program_Counter_pc_reg[27]/D
          Clock: (R) clk

                    Capture       Launch
        Clock Edge:+   10000            0
       Src Latency:+       0            0
       Net Latency:+       0 (I)        0 (I)
           Arrival:=   10000            0

             Setup:-     124
     Required Time:=    9876
      Launch Clock:-       0
         Data Path:-    2415
             Slack:=    7461

#-------------------------------------------------------------------------------------
----------------
#        Timing Point          Flags    Arc   Edge   Cell     Fanout Load Trans Delay A
rrival Instance
#                                                                 (fF)   (ps)   (ps)
 (ps)  Location
#-------------------------------------------------------------------------------------
----------------
  Program_Counter_pc_reg[2]/CK -       -      R     (arrival)     30    -     0     0
     0    (-,-)
  Program_Counter_pc_reg[2]/QN -       CK->QN F     DFFRX4         2  7.6    53   353
   353    (-,-)
  g118042__5107/Y               -       A->Y   R     NOR2X6         2  2.3    39    45
   398    (-,-)
  g118182/Y                     -       AN->Y  R     NOR2BX4        3  2.1    51   134
   533    (-,-)
  g118181/Y                     -       AN->Y  R     NOR2BX4        2  2.3    53   140
   673    (-,-)
  g118180/Y                     -       AN->Y  R     NOR2BX4        2  4.5    69   149
   821    (-,-)
  g118023/Y                     -       A->Y   F     INVX4          2  8.5    49    50
   872    (-,-)
  g118012__1881/Y               -       D->Y   R     NOR4X8         2  2.5   111    56
   928    (-,-)
  g118179/Y                     -       AN->Y  R     NOR4BX4        2  2.5   140   204
  1132    (-,-)
  g118176/Y                     -       AN->Y  R     NOR4BX4        2  2.5   140   215
  1346    (-,-)
  g118173/Y                     -       AN->Y  R     NOR4BX4        2  2.5   140   215
```

```
  1561    (-,-)
  g118170/Y                    -       AN->Y  R     NOR4BX4        2  2.5   140   215
  1776    (-,-)
  g118168/Y                    -       AN->Y  R     NOR4BX4        2  2.3   137   213
  1989    (-,-)
  g118167/Y                    -       AN->Y  R     NOR2BX4        2  2.3    53   172
  2162    (-,-)
  g118166/Y                    -       AN->Y  R     NOR2BX4        2  2.3    53   140
  2302    (-,-)
  g117922__8246/Y              -       S0->Y  F     MXI2X1         1  0.9    81    61
  2363    (-,-)
  g117919__5122/Y              -       B->Y   R     NOR2X1         2  0.7    52    52
  2415    (-,-)
  Program_Counter_pc_reg[27]/D -       -      R     DFFRX4         2    -     -     0
  2415    (-,-)
#-------------------------------------------------------------------------------------
----------------



Path 6: MET (7602 ps) Setup Check with Pin Program_Counter_pc_reg[26]/CK->D
          Group: clk
     Startpoint: (R) Program_Counter_pc_reg[2]/CK
          Clock: (R) clk
       Endpoint: (R) Program_Counter_pc_reg[26]/D
          Clock: (R) clk

                    Capture       Launch
       Clock Edge:+   10000            0
       Src Latency:+      0            0
       Net Latency:+      0 (I)        0 (I)
           Arrival:=  10000            0

             Setup:-    124
     Required Time:=   9876
      Launch Clock:-      0
         Data Path:-   2274
             Slack:=   7602

#-------------------------------------------------------------------------------------
----------------
#        Timing Point          Flags    Arc   Edge   Cell     Fanout Load Trans Delay A
rrival Instance
#                                                                 (fF)   (ps)   (ps)
 (ps)  Location
#-------------------------------------------------------------------------------------
----------------
  Program_Counter_pc_reg[2]/CK -       -      R     (arrival)     30    -     0     0
     0    (-,-)
  Program_Counter_pc_reg[2]/QN -       CK->QN F     DFFRX4         2  7.6    53   353
   353    (-,-)
  g118042__5107/Y              -       A->Y   R     NOR2X6         2  2.3    39    45
   398    (-,-)
  g118182/Y                    -       AN->Y  R     NOR2BX4        3  2.1    51   134
   533    (-,-)
  g118181/Y                    -       AN->Y  R     NOR2BX4        2  2.3    53   140
   673    (-,-)
  g118180/Y                    -       AN->Y  R     NOR2BX4        2  4.5    69   149
   821    (-,-)
  g118023/Y                    -       A->Y   F     INVX4          2  8.5    49    50
   872    (-,-)
  g118012__1881/Y              -       D->Y   R     NOR4X8         2  2.5   111    56
   928    (-,-)
```

```
  g118179/Y                     -       AN->Y  R     NOR4BX4        2  2.5   140   204
  1132    (-,-)
  g118176/Y                     -       AN->Y  R     NOR4BX4        2  2.5   140   215
  1346    (-,-)
  g118173/Y                     -       AN->Y  R     NOR4BX4        2  2.5   140   215
  1561    (-,-)
  g118170/Y                     -       AN->Y  R     NOR4BX4        2  2.5   140   215
  1776    (-,-)
  g118168/Y                     -       AN->Y  R     NOR4BX4        2  2.3   137   213
  1989    (-,-)
  g118167/Y                     -       AN->Y  R     NOR2BX4        2  2.3    53   172
  2162    (-,-)
  g117927__5115/Y               -       S0->Y  F     MXI2X1         1  0.9    81    61
  2222    (-,-)
  g117924__6131/Y               -       B->Y   R     NOR2X1         2  0.7    52    52
  2274    (-,-)
  Program_Counter_pc_reg[26]/D -        -      R     DFFRX4         2    -     -     0
  2274    (-,-)
#-------------------------------------------------------------------------------------
----------------



Path 7: MET (7746 ps) Setup Check with Pin Program_Counter_pc_reg[25]/CK->D
          Group: clk
     Startpoint: (R) Program_Counter_pc_reg[2]/CK
          Clock: (R) clk
       Endpoint: (R) Program_Counter_pc_reg[25]/D
          Clock: (R) clk

                    Capture       Launch
       Clock Edge:+   10000            0
       Src Latency:+      0            0
       Net Latency:+      0 (I)        0 (I)
           Arrival:=  10000            0

             Setup:-    124
     Required Time:=   9876
      Launch Clock:-      0
         Data Path:-   2130
             Slack:=   7746

#-------------------------------------------------------------------------------------
----------------
#        Timing Point          Flags    Arc   Edge   Cell     Fanout Load Trans Delay A
rrival Instance
#                                                                  (fF)   (ps)   (ps)
 (ps)  Location
#-------------------------------------------------------------------------------------
----------------
  Program_Counter_pc_reg[2]/CK -       -      R     (arrival)     30    -     0     0
     0    (-,-)
  Program_Counter_pc_reg[2]/QN -       CK->QN F     DFFRX4         2  7.6    53   353
   353    (-,-)
  g118042__5107/Y               -       A->Y   R     NOR2X6         2  2.3    39    45
   398    (-,-)
  g118182/Y                     -       AN->Y  R     NOR2BX4        3  2.1    51   134
   533    (-,-)
  g118181/Y                     -       AN->Y  R     NOR2BX4        2  2.3    53   140
   673    (-,-)
  g118180/Y                     -       AN->Y  R     NOR2BX4        2  4.5    69   149
   821    (-,-)
  g118023/Y                     -       A->Y   F     INVX4          2  8.5    49    50
```

```
   872    (-,-)
  g118012__1881/Y              -       D->Y   R     NOR4X8         2  2.5   111    56
   928    (-,-)
  g118179/Y                    -       AN->Y  R     NOR4BX4        2  2.5   140   204
  1132    (-,-)
  g118176/Y                    -       AN->Y  R     NOR4BX4        2  2.5   140   215
  1346    (-,-)
  g118173/Y                    -       AN->Y  R     NOR4BX4        2  2.5   140   215
  1561    (-,-)
  g118170/Y                    -       AN->Y  R     NOR4BX4        2  2.5   140   215
  1776    (-,-)
  g118168/Y                    -       AN->Y  R     NOR4BX4        2  2.3   137   213
  1989    (-,-)
  g117932__2883/Y              -       S0->Y  F     MXI2X1         1  0.9    81    88
  2078    (-,-)
  g117929__6161/Y              -       B->Y   R     NOR2X1         2  0.7    52    52
  2130    (-,-)
  Program_Counter_pc_reg[25]/D -       -      R     DFFRX4         2    -     -     0
  2130    (-,-)
#-------------------------------------------------------------------------------------
----------------



Path 8: MET (7767 ps) Setup Check with Pin Program_Counter_pc_reg[24]/CK->D
          Group: clk
     Startpoint: (R) Program_Counter_pc_reg[2]/CK
          Clock: (R) clk
       Endpoint: (R) Program_Counter_pc_reg[24]/D
          Clock: (R) clk

                    Capture       Launch
        Clock Edge:+   10000            0
       Src Latency:+       0            0
       Net Latency:+       0 (I)        0 (I)
           Arrival:=   10000            0

             Setup:-     124
     Required Time:=    9876
      Launch Clock:-       0
         Data Path:-    2109
             Slack:=    7767

#-------------------------------------------------------------------------------------
----------------
#        Timing Point          Flags    Arc   Edge   Cell     Fanout Load Trans Delay A
rrival Instance
#                                                                    (fF)   (ps)   (ps)
 (ps)  Location
#-------------------------------------------------------------------------------------
----------------
  Program_Counter_pc_reg[2]/CK -       -      R     (arrival)     30    -     0     0
    0    (-,-)
  Program_Counter_pc_reg[2]/QN -       CK->QN F     DFFRX4         2  7.6    53   353
   353    (-,-)
  g118042__5107/Y              -       A->Y   R     NOR2X6         2  2.3    39    45
   398    (-,-)
  g118182/Y                    -       AN->Y  R     NOR2BX4        3  2.1    51   134
   533    (-,-)
  g118181/Y                    -       AN->Y  R     NOR2BX4        2  2.3    53   140
   673    (-,-)
  g118180/Y                    -       AN->Y  R     NOR2BX4        2  4.5    69   149
   821    (-,-)
```

```
  g118023/Y                     -       A->Y   F     INVX4          2  8.5    49    50
   872    (-,-)
  g118022__7482/Y               -       B->Y   R     NOR2X4         2  4.5    61    48
   919    (-,-)
  g118018/Y                     -       A->Y   F     INVX4          2  8.5    48    48
   967    (-,-)
  g118017__7098/Y               -       B->Y   R     NOR2X4         2  2.5    47    40
  1007    (-,-)
  g118178/Y                     -       AN->Y  R     NOR4BX4        2  2.5   140   180
  1187    (-,-)
  g118175/Y                     -       AN->Y  R     NOR4BX4        2  2.5   140   215
  1402    (-,-)
  g118172/Y                     -       AN->Y  R     NOR4BX4        2  2.5   140   215
  1617    (-,-)
  g118169/Y                     -       AN->Y  R     NOR4BX4        2  3.2   151   220
  1837    (-,-)
  g117953/Y                     -       A->Y   F     INVX2          1  3.0    48    76
  1913    (-,-)
  g117943__7410/Y               -       D->Y   R     NOR4BBX4       1  1.7   123    60
  1974    (-,-)
  g117937__4733/Y               -       S0->Y  F     MXI2X1         1  0.9    81    84
  2057    (-,-)
  g117934__1881/Y               -       B->Y   R     NOR2X1         2  0.7    52    52
  2109    (-,-)
  Program_Counter_pc_reg[24]/D  -       -      R     DFFRX4         2    -     -     0
  2109    (-,-)
#-------------------------------------------------------------------------------------
----------------



Path 9: MET (7894 ps) Setup Check with Pin Program_Counter_pc_reg[21]/CK->D
          Group: clk
     Startpoint: (R) Program_Counter_pc_reg[2]/CK
          Clock: (R) clk
       Endpoint: (R) Program_Counter_pc_reg[21]/D
          Clock: (R) clk

                    Capture       Launch
       Clock Edge:+   10000            0
      Src Latency:+       0            0
      Net Latency:+       0 (I)        0 (I)
          Arrival:=   10000            0

            Setup:-     124
     Required Time:=    9876
      Launch Clock:-       0
         Data Path:-    1982
             Slack:=    7894

#-------------------------------------------------------------------------------------
----------------
#        Timing Point          Flags    Arc   Edge   Cell     Fanout Load Trans Delay A
rrival Instance
#                                                                 (fF)   (ps)   (ps)
 (ps)  Location
#-------------------------------------------------------------------------------------
----------------
  Program_Counter_pc_reg[2]/CK -       -      R     (arrival)     30    -     0     0
     0    (-,-)
  Program_Counter_pc_reg[2]/QN -       CK->QN F     DFFRX4         2  7.6    53   353
   353    (-,-)
  g118042__5107/Y               -       A->Y   R     NOR2X6         2  2.3    39    45
```

```
   398    (-,-)
  g118182/Y                    -       AN->Y  R     NOR2BX4        3  2.1    51   134
   533    (-,-)
  g118181/Y                    -       AN->Y  R     NOR2BX4        2  2.3    53   140
   673    (-,-)
  g118180/Y                    -       AN->Y  R     NOR2BX4        2  4.5    69   149
   821    (-,-)
  g118023/Y                    -       A->Y   F     INVX4          2  8.5    49    50
   872    (-,-)
  g118022__7482/Y              -       B->Y   R     NOR2X4         2  4.5    61    48
   919    (-,-)
  g118018/Y                    -       A->Y   F     INVX4          2  8.5    48    48
   967    (-,-)
  g118017__7098/Y              -       B->Y   R     NOR2X4         2  2.5    47    40
  1007    (-,-)
  g118178/Y                    -       AN->Y  R     NOR4BX4        2  2.5   140   180
  1187    (-,-)
  g118175/Y                    -       AN->Y  R     NOR4BX4        2  2.5   140   215
  1402    (-,-)
  g118172/Y                    -       AN->Y  R     NOR4BX4        2  2.5   140   215
  1617    (-,-)
  g118169/Y                    -       AN->Y  R     NOR4BX4        2  3.2   151   220
  1837    (-,-)
  g117950__5477/Y              -       S0->Y  F     MXI2X1         1  0.9    81    93
  1930    (-,-)
  g117946__9945/Y              -       B->Y   R     NOR2X1         2  0.7    52    52
  1982    (-,-)
  Program_Counter_pc_reg[21]/D -       -      R     DFFRX4         2    -     -     0
  1982    (-,-)
#-------------------------------------------------------------------------------------
----------------


Path 10: MET (7942 ps) Setup Check with Pin Program_Counter_pc_reg[23]/CK->D
          Group: clk
     Startpoint: (R) Program_Counter_pc_reg[2]/CK
          Clock: (R) clk
       Endpoint: (R) Program_Counter_pc_reg[23]/D
          Clock: (R) clk

                    Capture       Launch
        Clock Edge:+   10000            0
       Src Latency:+       0            0
       Net Latency:+       0 (I)        0 (I)
           Arrival:=   10000            0

             Setup:-     124
     Required Time:=    9876
      Launch Clock:-       0
         Data Path:-    1934
             Slack:=    7942

#-------------------------------------------------------------------------------------
----------------
#        Timing Point          Flags    Arc   Edge   Cell     Fanout Load Trans Delay A
rrival Instance
#                                                                 (fF)   (ps)   (ps)
 (ps)  Location
#-------------------------------------------------------------------------------------
----------------
  Program_Counter_pc_reg[2]/CK -       -      R     (arrival)     30    -     0     0
     0    (-,-)
```

```
  Program_Counter_pc_reg[2]/QN -       CK->QN F     DFFRX4         2  7.6    53   353
   353    (-,-)
  g118042__5107/Y              -       A->Y   R     NOR2X6         2  2.3    39    45
   398    (-,-)
  g118182/Y                    -       AN->Y  R     NOR2BX4        3  2.1    51   134
   533    (-,-)
  g118181/Y                    -       AN->Y  R     NOR2BX4        2  2.3    53   140
   673    (-,-)
  g118180/Y                    -       AN->Y  R     NOR2BX4        2  4.5    69   149
   821    (-,-)
  g118023/Y                    -       A->Y   F     INVX4          2  8.5    49    50
   872    (-,-)
  g118022__7482/Y              -       B->Y   R     NOR2X4         2  4.5    61    48
   919    (-,-)
  g118018/Y                    -       A->Y   F     INVX4          2  8.5    48    48
   967    (-,-)
  g118007__5122/Y              -       D->Y   R     NOR4X8         2  2.5   111    56
  1023    (-,-)
  g118177/Y                    -       AN->Y  R     NOR4BX4        2  2.5   140   204
  1227    (-,-)
  g118174/Y                    -       AN->Y  R     NOR4BX4        2  2.5   140   215
  1442    (-,-)
  g118171/Y                    -       AN->Y  R     NOR4BX4        2  3.2   150   220
  1662    (-,-)
  g117958/Y                    -       A->Y   F     INVX2          1  3.0    48    76
  1738    (-,-)
  g117947__4319/Y              -       D->Y   R     NOR4BBX4       1  1.7   123    60
  1798    (-,-)
  g117941__1666/Y              -       S0->Y  F     MXI2X1         1  0.9    81    84
  1882    (-,-)
  g117939__9315/Y              -       B->Y   R     NOR2X1         2  0.7    52    52
  1934    (-,-)
  Program_Counter_pc_reg[23]/D -       -      R     DFFRX4         2    -     -     0
  1934    (-,-)
#-------------------------------------------------------------------------------
---------------


===== AREA =====
================================================================
  Generated by:           Genus(TM) Synthesis Solution 21.14-s082_1
  Generated on:           Feb 27 2026  12:54:02 pm
  Module:                 RISC_V
  Operating conditions:   slow (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
================================================================

Instance Module  Cell Count  Cell Area  Net Area   Total Area   Wireload
-----------------------------------------------------------------------
RISC_V                 122      0.000     0.000        0.000 <none> (D)
  (D) = wireload is default in technology library

===== GATE COUNT =====
================================================================
  Generated by:           Genus(TM) Synthesis Solution 21.14-s082_1
  Generated on:           Feb 27 2026  12:54:02 pm
  Module:                 RISC_V
  Operating conditions:   slow (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
================================================================
```

Gate	Instances	Area	Library
AOI22X4	1	0.000	gpdk045bc
AOI2BB2X1	1	0.000	gpdk045bc
DFFRHQX4	1	0.000	gpdk045bc
DFFRX4	29	0.000	gpdk045bc
INVX2	2	0.000	gpdk045bc
INVX4	2	0.000	gpdk045bc
INVXL	1	0.000	gpdk045bc
MXI2X1	26	0.000	gpdk045bc
NOR2BX4	9	0.000	gpdk045bc
NOR2X1	28	0.000	gpdk045bc
NOR2X2	2	0.000	gpdk045bc
NOR2X4	2	0.000	gpdk045bc
NOR2X6	1	0.000	gpdk045bc
NOR4BBX4	2	0.000	gpdk045bc
NOR4BX4	12	0.000	gpdk045bc
NOR4X8	2	0.000	gpdk045bc
XNOR2X4	1	0.000	gpdk045bc
total	122	0.000	

Type	Instances	Area	Area %
sequential	30	0.000	0.0
inverter	5	0.000	0.0
logic	87	0.000	0.0
physical_cells	0	0.000	0.0
total	122	0.000	0.0

```
===== HIERARCHY =====
============================================================
  Generated by:           Genus(TM) Synthesis Solution 21.14-s082_1
  Generated on:           Feb 27 2026  12:54:35 pm
  Module:                 RISC_V
  Operating conditions:   slow (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
============================================================


  Hierarchy Report Format :

    level instance ( module ) <status>

    status :    preserve_<value> -- indicating preserve hierachy or inherited_preserve
value
           :    blackbox --  indicating  unresolved instance

================================================================

 0 RISC_V
```