Implementation of a CMOS 3-bit Wallace Tree Multiplier using 28nm PDK with Synopsys Custom Compiler

Subham Mohapatra
B.Tech Electrical and Electronics Engineering, National Institute of Technology Karnataka

***Abstract*— A Wallace multiplier is a hardware implementation of a binary multiplier, commonly used in digital computers. It is a digital circuit that multiplies two integers. It uses multiple AND gates, half and full adders to sum partial products in stages until two numbers are left.This is also called the Wallace tree or Wallace reduction. Wallace multipliers were devised by the Australian computer scientist Chris Wallace in 1964**

I. REFERENCE CIRCUIT DETAILS

The Wallace tree has three steps:

- Multiply each bit of one of the arguments, by each bit of the other.
- Reduce the number of partial products to two by layers of full and half adders.
- Group the wires in two numbers, and add them with a conventional adder.

First we need to multiply each bit of first factor(A) by each digit of the other factor(B). Each of this partial products will have weight equal to the product of its factors. The final product is calculated by the weighted sum of all these partial products. Next the resulting bits are reduced to two numbers, this is done by using a full adder to sum three components and half adder to sum two components. Finally the two resulting numbers are given as input to an adder and the final product is obtained.

II. REFERENCE CIRCUIT

Circuit diagram of the 3-bit Wallace Tree Multiplier is shown in Figure 1.

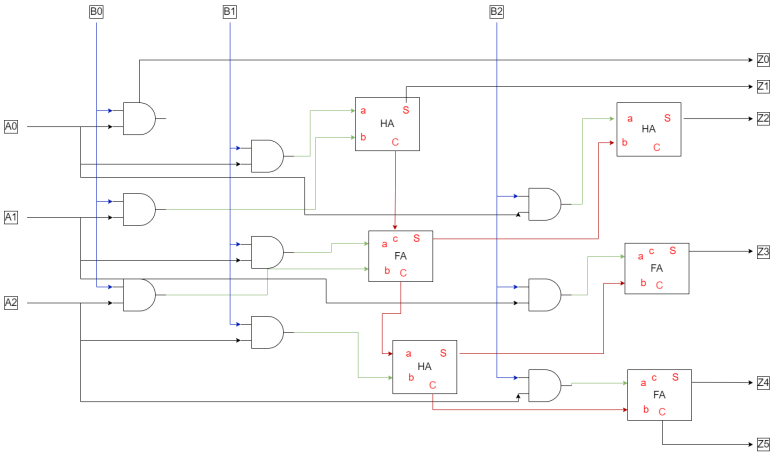

Fig. 1: 3-bit Wallace Tree Multiplier

III. REFERENCE CIRCUITS WAVEFORMS

Output Waveforms $(Z_5Z_4Z_3Z_2Z_1Z_0)$ of multiplying 3-bit input $A_2A_1A_0$ and $B_2B_1B_0$ is shown in figure 2.

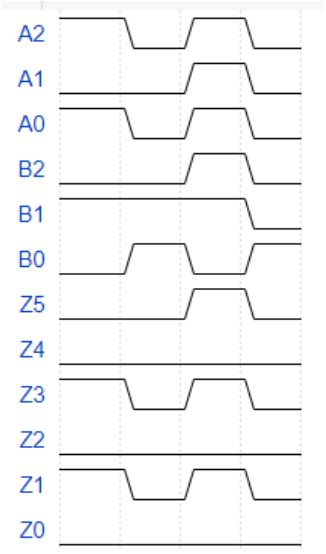

Fig. 2: Output Waveform

REFERENCES

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[2] N. Sureka, R. Porselvi and K. Kumuthapriya, "An efficient high speed Wallace tree multiplier," 2013 International Conference on Information Communication and Embedded Systems (ICICES), 2013, pp. 1023-1026, doi: 10.1109/ICICES.2013.6508192.