INDIAN INSTITUTE OF TECHNOLOGY PALAKKAD

CS5119- Advanced Computer Architecture Lab

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LAB 5

Problem 1: Generate the binaries of micro-benchmark suite for RISCV ISA using riscv-gnu-toolchain

problem 2: Run the applications (any 10) in gem5 in SE mode using out-of-order and in-order execution. Analyze and compare the results and discuss it in your report.

Solution:
in-order execution : It has four pipeline stages fetch1, fetch2, Decode, Execute. In in-order cpu or minor cpu , the program execute and fetch in in-order and it also execute in in-order.

Out of order execution : It has seven pipeline stages fetch, decode, Rename, issue, Execution, Write Back and Commit. Here the program fetch occurs in in-order and the execution occurs in out of order and the commit occur in-order. in all the seven stages in gem5 branch prediction are implemented in the decode stages.

For microbench CCm		
Parameter	In-order execution	Out of order execution
simSeconds	0.000006	0.0004553
simfreq	1000000000000	1000000000000
HostOprate	1063766	305980
CPU Cycles	701560	163460
Number of Idle cycles	0.002000	8465
Total dcache hit	66607	50809
Total dcache miss	49	169
Total Icache hit	273670	26649
Total Icache miss	136	223

For microbench CRf		
Parameter	In-order execution	Out of order execution
simSeconds	0.000584	0.000090
simfreq	1000000000000	1000000000000
HostOprate	1165081	351986
CPU Cycles	1168678	179773
Number of Idle cycles	0.002000	8300
Total dcache hit	133518	50809
Total dcache miss	50	169
Total Icache hit	63217	86107
Total Icache miss	218	201

For microbench MIP		
Parameter	In-order execution	Out of order execution
simSeconds	0.001023	0.000683
simfreq	1000000000000	1000000000000
HostOprate	776245	186002
CPU Cycles	2045128	1365209
Number of Idle cycles	0.002000	851255
Total dcache hit	88924	50090
Total dcache miss	49	172
Total Icache hit	267621	2391
Total Icache miss	10456	12025

For microbench $ML2_BW_ld$		
Parameter	In-order execution	Out of order execution
simSeconds	0.006752	0.003450
simfreq	1000000000000	1000000000000
HostOprate	900198	174704
CPU Cycles	13503858	6900927
Number of Idle cycles	0.002000	9484
Total dcache hit	600977	268575
Total dcache miss	55343	224389
Total Icache hit	2362183	99355
Total Icache miss	137	233

For microbench MM		
Parameter	In-order execution	Out of order execution
simSeconds	0.017995	0.009988
simfreq	1000000000000	1000000000000
HostOprate	745263	132328
CPU Cycles	35989136	19976096
Number of Idle cycles	0.002000	0
Total dcache hit	1772291	1524529
Total dcache miss	196803	230635
Total Icache hit	5157515	733730
Total Icache miss	138	223

For microbench MM st		
Parameter	In-order execution	Out of order execution
simSeconds	0.018095	0.006603
simfreq	1000000000000	1000000000000
HostOprate	734596	160809
CPU Cycles	36189700	13205130
Number of Idle cycles	0.002000	9090
Total dcache hit	1641215	1327882
Total dcache miss	196803	230620
Total Icache hit	4960898	800005
Total Icache miss	141	227

For microbench ML2 st		
Parameter	In-order execution	Out of order execution
simSeconds	0.010690	0.005993
simfreq	1000000000000	1000000000000
HostOprate	800962	158578
CPU Cycles	21379856	11986030
Number of Idle cycles	0.002000	10331
Total dcache hit	758810	139127
Total dcache miss	94107	255556
Total Icache hit	3214171	132034
Total Icache miss	138	225

For microbench ML2 bw idst		
Parameter	In-order execution	Out of order execution
simSeconds	0.007392	0.001585
simfreq	1000000000000	1000000000000
HostOprate	830516	253415
CPU Cycles	14783070	3169226
Number of Idle cycles	0.002000	10177
Total dcache hit	633977	139784
Total dcache miss	55111	255556
Total Icache hit	2952005	99177
Total Icache miss	139	230

For microbench ML2		
Parameter	In-order execution	Out of order execution
simSeconds	0.008841	0.005794
simfreq	1000000000000	1000000000000
HostOprate	891607	151050
CPU Cycles	17682488	11588243
Number of Idle cycles	0.002000	9662
Total dcache hit	577453	135335
Total dcache miss	78859	193726
Total Icache hit	2493221	132133
Total Icache miss	137	242

For microbench MIM		
Parameter	In-order execution	Out of order execution
simSeconds	0.001536	0.001033
simfreq	1000000000000	1000000000000
HostOprate	891607	151050
CPU Cycles	17682488	11588243
Number of Idle cycles	0.002000	9662
Total dcache hit	577453	135335
Total dcache miss	78859	193726
Total Icache hit	2493221	132133
Total Icache miss	137	242

Summary: based on the aforementioned status Since pipeling is used for the out of order execution, there will be stages into which the execution may be separated. As can be seen in all status files, the out of order execution requires less simulation time than the in-order. Additionally, host machine seconds are further out of sequence. Additionally, because the work is divided into stages, performing them out of sequence requires less cycles. And because there is more labour to be done when things are out of order, more energy is consumed.