Important Parameters

Sl No.	Impotant Parameter	Observation	Description
01	simSeconds	0.000493	The average time in seconds i.e, 0.000493 sec spent in processing one simulated event for 4 numbers of cores.
02	simTicks	493443000	Number of ticks simulated by the cpu
03	simInsts	6269	Number of instructions simulated by the cpu
04	system.clk_domain.clock	1000	Clock period in ticks
05	system.cpu.numCycles	493443	Number of cpu cycles simulated
06	system.cpu.exec_context.thread_0.numIntInsts	11142	Number of integer instructions Count
07	system.cpu.exec_context.thread_0.numFpInsts	0	Number of float instructions Count
08	system.cpu.exec_context.thread_0.numVecInsts	0	Number of vector instructions Count
09	system.cpu.exec_context.thread_0.numMemRefs	2076	Number of memory refs Count
10	system.cpu.exec_context.thread_0.numLoadInsts	1123	Number of load instructions
11	system.cpu.exec_context.thread_0.numStoreInsts	953	Number of store instructions
12	system.cpu.exec_context.thread_0.numIdleCycles	0.001000	Number of idle cycles
13	system.cpu.exec_context.thread_0.numBusyCycles	493442.999000	Number of busy cycles
14	system.cpu.mmu.dtb.rdAccesses	1123	TLB accesses on read requests
15	system.cpu.mmu.dtb.wrAccesses	953	TLB accesses on write requests
16	system.cpu.mmu.dtb.rdMisses	11	TLB misses on read requests
17	system.cpu.mmu.dtb.wrMisses	9	TLB misses on write requests
18	system.cpu.workload.numSyscalls	11	Number of system calls
19	system.mem_ctrl.totGap	493317000	Total gap between requests
20	system.mem_ctrl.avgGap	48988.78	Average gap between requests
21	system.mem_ctrl.dram.bytesInstRead::cpu.inst	63968	Number of instructions bytes read from this memory

22	system.mem_ctrl.dram.bytes Written::cpu.data	7240	Number of bytes written to this memory
23	system.mem_ctrl.dram.num Writes::cpu.data	951	Number of write requests responded to by this memory
24	system.mem_ctrl.dram.write Bursts	96	Number of DRAM write bursts
25	system.mem_ctrl.dram.avgBu sLat	5000.00	Average bus latency per DRAM burst
26	system.mem_ctrl.dram.avgM emAccLat	22248.07	Average memory access latency per
27	system.mem_ctrl.dram.bytes Read	572736	Total bytes read from the memory
28	system.mem_ctrl.dram.bytes Written	6144	Total bytes written on memory
29	system.mem_ctrl.dram.busUt ilRead	9.07	Data bus utilization in percentage for reads
30	system.mem_ctrl.dram.busUt ilWrite	0.10	Data bus utilization in percentage for writes

Summary: The above parameters and their values tells about the statistics of a 'Hello World' program which has been found in the ’/gem5/m5out’ folder as ’stats.txt’ . It takes about 0.000493 seconds for the simulation with a Clock Time period of 1000(ticks) and clock cycles of 493443.