CS5119: Advanced Computer Architecture Lab

Lab 7

Deadline:15th December 11:59 PM.

Problem 1: In continuation to previous lab 6, use 5 different micro-benchmarks and compare performance of RISC-V in-order CPU with L1 instruction and L1 data cache (same size) for different set associativity levels such as 2, 4, and 8. Discuss your conclusion in detail. Perform the experiments for Cache sizes as128 KB and 256 KB.