INDIAN INSTITUTE OF TECHNOLOGY PALAKKAD

CS5119- Advanced Computer Architecture Lab

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LAB 7

Problem 1: In continuation to previous lab 6, use 5 different micro-benchmarks and compare performance of RISC-V in-order CPU with L1 instruction and L1 data cache (same size) for different set associativity levels such as 2, 4, and 8. Discuss your conclusion in detail. Perform the experiments for Cache sizes as 128 KB and 256 KB.

Solution:
MissRate means the cache overall miss rate(system.cpu.dcache.overallMissRate ::total)

1. ML2_BW_ldst
   a) For 128 KB Cache

Parameter	set associative(**2**)	set associative(**4**)	set associative(**8**)
simSeconds	0.005017	0.005014	0.005011
MissRate	0.202299	0.202276	0.202226

   here, as we increase associativity simSeconds are decreased and the miss rate also decreases.

   b) For 256 KB Cache

Parameter	set associative(**2**)	set associative(**4**)	set associative(**8**)
simSeconds	0.004670	0.004672	0.004677
MissRate	0.185357	0.185380	0.185901

here we increase our cache size 128 KB to 256 KB, as we increase associativity simSeconds and miss rate both increase.

2. ML2_BW_st

   a) For 128 KB Cache

Parameter	set associative(**2**)	set associative(**4**)	set associative(**8**)
simSeconds	0.004240	0.004240	0.004237
MissRate	0.278922	0.279110	0.279140

   here, when we increase associativity from 2 to 4 simseconds remains the same but miss rate is increased but when we increase cache associativity to 8 then simSeconds is reduced but miss rate increases.

   b) For 256 KB Cache

Parameter	set associative(**2**)	set associative(**4**)	set associative(**8**)
simSeconds	0.003950	0.003953	0.003961
MissRate	0.258395	0.258717	0.259342

   here, as we increase associativity simSeconds are decreased and the miss rate also decreases.

3. MCS

   a) For 128 KB Cache

Parameter	set associative(**2**)	set associative(**4**)	set associative(**8**)
simSeconds	0.002657	0.002660	0.002513
MissRate	0.682438	0.682438	0.682438

   here, as we increase associativity from 2 to 4 simSeceonds and miss rate both are is increase but when we increase associativity to 8 then simSeceonds is decrease and miss rate is increase.

   b) For 256 KB Cache

Parameter	set associative(**2**)	set associative(**4**)	set associative(**8**)
simSeconds	0.001306	0.001680	0.002495
MissRate	0.257296	0.398906	0.682126

   here, as we increase associativity simSeconds and miss rate both increase.

4. MI

   a) For 128 KB Cache

Parameter	set associative(**2**)	set associative(**4**)	set associative(**8**)
simSeconds	0.000294	0.000294	0.000294
MissRate	0.002610	0.002610	0.002610

   as we increase associativity, simSeceonds and miss rate both remain the same.

   b) For 256 KB Cache

Parameter	set associative(**2**)	set associative(**4**)	set associative(**8**)
simSeconds	0.000294	0.000294	0.000294
MissRate	0.002610	0.002610	0.002610

   here, as we increase associativity, simSeconds and miss rate both remain the same, and increasing cache size from 128KB to 256KB does not change simSeconds and miss rate.

5. M_Dyn

   a) For 128 KB Cache

Parameter	set associative(**2**)	set associative(**4**)	set associative(**8**)
simSeconds	0.023462	0.023454	0.023433
MissRate	0.128108	0.127936	0.127484

   here, as we increase associativity both simSeconds and miss rate both are decrease.

   b) For 256 KB Cache

Parameter	set associative(**2**)	set associative(**4**)	set associative(**8**)
simSeconds	0.023448	0.023439	0.023419
MissRate	0.128108	0.127936	0.127484

   as we increase cache size from 128 KB to 256 KB and associativity both simSecond and miss rate decrease.

Conclusion:
By looking at the data above, we cannot come to the conclusion that increasing cache size or set associativity will improve speed because it all relies on the programme we are using and the environment in which it is being used. The ability to increase set associativity is constrained because doing so increases the time required to check the tag.