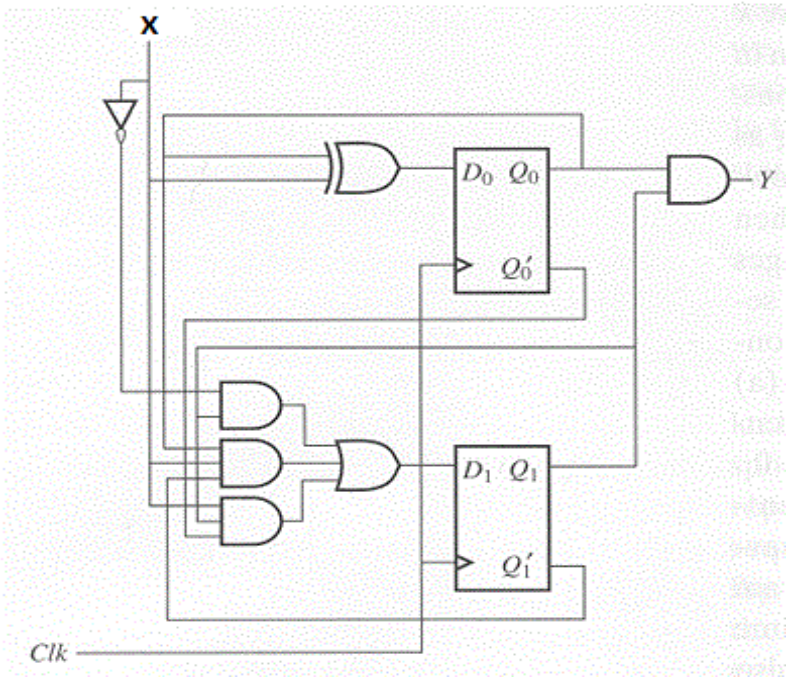
National University of Computer and Emerging Sciences, Lahore Campus

Course:	Digital Logic Design	Course Code:	EE227
Program:	BS(Computer Science)	Semester:	Fall 2018
Duration:	60 Minutes	Total Marks:	40
Paper Date:	15-Nov-18	Weight	15%
Section:	ALL	Page(s):	4
Exam:	Midterm-II	Roll No. Section:	

Instruction/Notes:
- *Attempt all the questions on this answer booklet. You can use extra sheets for your scratch work but **they will not be collected and marked**.*

Question 1[10 Marks]: Consider given diagram



i. Complete the truth table [5 marks, 1 mark for each column]

Present states		X (Input)	D_0	D_1	Next states		Y (Output)
$Q_0(t)$	$Q_1(t)$				$Q_0(t+1)$	$Q_1(t+1)$	
0	0	0					
0	0	1					
0	1	0					
0	1	1					
1	0	0					
1	0	1					
1	1	0					
1	1	1					

ii. Write next state equations [3]

Q_0 _____

Q_1_____

Y_____

iii. Draw state diagram [2]

Question 2 [10 Marks]: Design a 4-bit mini-Process Unit that works according to the given functionality:

M_1	M_0	$F(A,B) = S_3S_2S_1S_0$	Function Description
0	0	**A – 2*B**	Subtract 2 times B from A
0	1	**A + 4*B**	Add 4 times B and A
1	0	**A + B**	Add A and B
1	1	**A + 1**	Increment A

Where A and B are two 4-bit numbers. M inputs to your mini-processor are control inputs. Partial design of the mini-processor is given below. **Your task is to add required logic in the design given below in order to make mini-processor fully functional.**

Note: Assume that you already have Decoder(s), Encoder(s), MUX(s), DMUX(s) and Multiplier(s) blocks available. **Properly label all blocks and inputs/outputs to get credit.**

Question 3: Implement the function given below

$$F(A,B,C,D) = \Sigma m(0,2,4,5,6,12,14)$$

(a) **[10 Marks] Using a 4x1 MUX and external Gates only. Take C and D as Selection Inputs and A and B as Data Inputs**

(b) **[10 Marks] Using Decoder(s) and external NAND Gates only**

Note: Properly label inputs and outputs to get credit

Input				Output
A	**B**	**C**	**D**	**F**
0	0	0	0	
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

a)

b)