Bipolar Sinusoidal PWM with V/f Control for Variable Frequency Drives
Time Domain, Spectral, Fourier-Series, and RTL-Driven Analysis

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Abstract

This report presents a complete study of bipolar sinusoidal pulse-width modulation (SPWM) combined with scalar V/f control for variable frequency drives (VFDs). Evidence includes time-domain waveforms, FFT spectrum of line voltage, sweep-level validation of V/f scheduling and fundamental tracking, distortion and switching activity trends, and Fourier-series decomposition. The report further provides an RTL/VLSI-oriented design specification, including fixed-point definitions, carrier quantization relations, dead-time insertion as a safety-critical finite state machine (FSM), and resource/timing considerations for synthesizable implementation.

Contents

1 Introduction

Variable Frequency Drives (VFDs) regulate AC motor speed by commanding electrical frequency while adjusting applied voltage to maintain acceptable air-gap flux. Scalar V/f control remains widely used due to simplicity and robustness. A digital VFD typically includes: frequency command, voltage scheduling (V/f with optional low-frequency boost), PWM modulation, and a power inverter stage.

bipolar SPWM is a practical full-bridge modulation method because it produces a three-level line voltage waveform and maps naturally to simple digital primitives (counters, lookup tables, comparators, and gating safety logic).

2 Motivation

A reviewer-grade VLSI-oriented modulation study should provide:

- time-domain evidence that switching and three-level behavior are correct,
- spectral evidence of harmonic distribution and carrier-related components,
- sweep evidence that scheduled $A(f)$ produces expected fundamental behavior,
- distortion and switching trends for quality versus stress discussion,
- a hardware-feasible RTL specification with fixed-point and safety logic (dead-time).

3 Literature Review

3.1 bipolar SPWM

SPWM compares a sinusoidal reference against a high-frequency triangular carrier. bipolar full-bridge SPWM uses $+v_m$ for one leg and $-v_m$ for the other, producing a three-level line voltage and improved harmonic behavior relative to bipolar modulation under comparable switching frequency.

3.2 Scalar V/f control and low-frequency boost

For induction machines, air-gap flux approximately follows V/f in the constant-flux region. At low frequency, stator resistance drop reduces effective flux, motivating a low-frequency voltage boost to improve torque production. Practical implementations also clamp amplitude to avoid overmodulation.

3.3 Digital motor control implementation

Digital modulators are typically fixed-point: a phase accumulator plus sine LUT (or CORDIC), an up-down counter for the triangle carrier, signed comparators for gating, and dead-time/protection logic to prevent shoot-through in the inverter legs.

4 Research Gap

Common PWM demonstrations emphasize qualitative waveforms without connecting to sweep-level validation and hardware feasibility. This work closes the loop by:

1. validating V/f scheduling behavior across frequency points,
2. reporting FFT and Fourier-series decomposition of line voltage,
3. quantifying distortion and switching activity trends,
4. specifying a synthesizable RTL architecture including dead-time FSM.

5 Objectives

- Study bipolar SPWM for full-bridge inverters and characterize $v_{AB}(t)$.
- Implement and validate scalar V/f scheduling $A(f)$ with optional boost and clamp.
- Provide waveform, spectral, and sweep evidence: FFT, fundamental proxy, THD proxy, switching proxy.
- Provide an RTL/VLSI-oriented specification: fixed-point formats, carrier relations, dead-time insertion as FSM.

6 Theory: Modulation and Scheduling

6.1 bipolar SPWM formulation

Let

$$v_m(t) = A\sin(2\pi f_{\text{ref}} t + \phi),$$

and let $v_{cr}(t)$ be a triangular carrier at f_{car}. bipolar SPWM defines:

$$g_1(t) = \mathbb{1}\{v_m(t) \geq v_{cr}(t)\}, \qquad g_3(t) = \mathbb{1}\{-v_m(t) \geq v_{cr}(t)\}.$$

For DC bus V_{dc}, the ideal line voltage is:

$$v_{AB}(t) = V_{dc}\big(g_1(t) - g_3(t)\big) \in \{-V_{dc}, 0, +V_{dc}\}.$$

6.2 Scalar V/f scheduling with boost

With base point (f_{base}, A_{base}):

$$A(f) = \text{clip}\left(A_{base}\frac{f}{f_{base}} + A_{boost}(f),\ 0,\ A_{max}\right),$$

and boost:

$$A_{boost}(f) = V_{boost}\max\left(0, 1 - \frac{f}{f_{boost}}\right).$$

7 Results and Discussion

7.1 Time-domain waveform evidence

Figure 1 shows one fundamental cycle. The line voltage exhibits three-level behavior with a sinusoidal envelope.

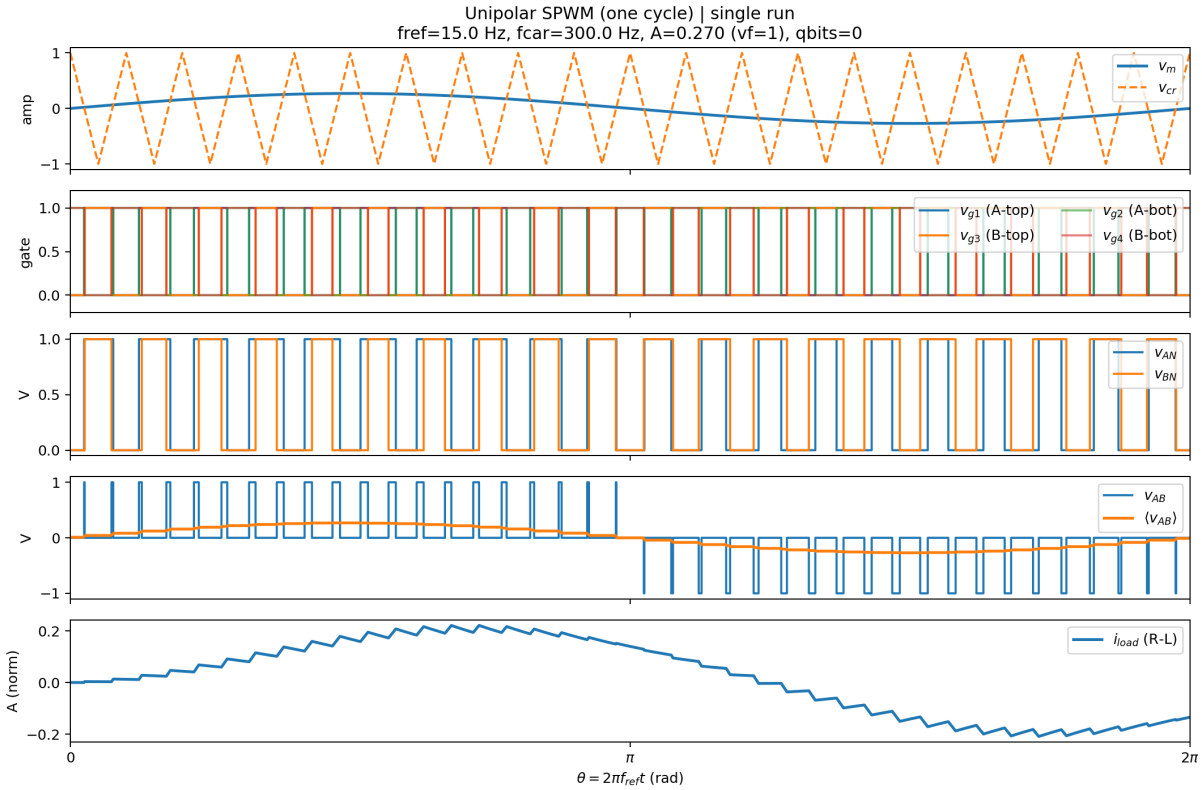

Figure 1: Time-domain waveforms for bipolar SPWM over one fundamental cycle.

7.2 Spectral characterization

Figure 2 shows FFT magnitude of $v_{AB}(t)$ for a representative operating point.

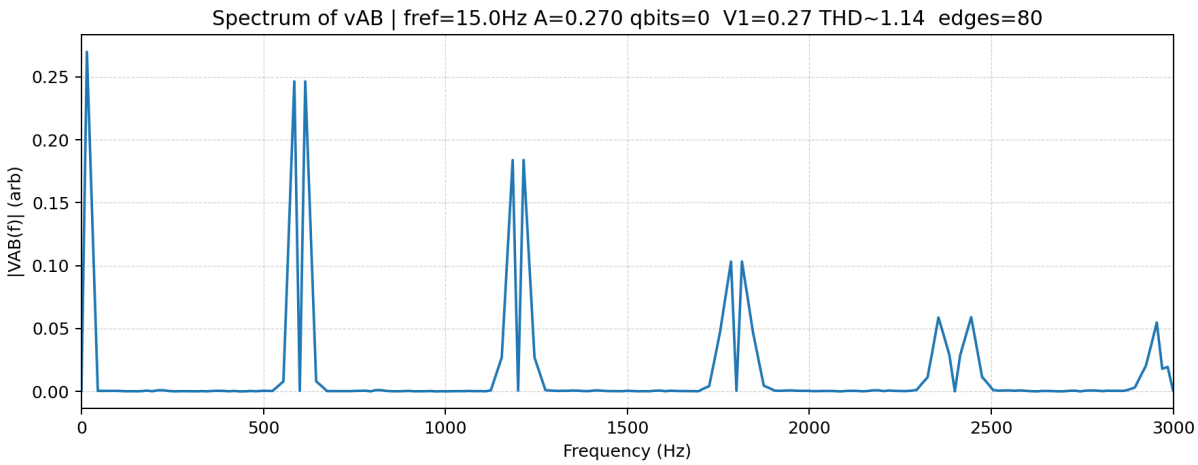

Figure 2: FFT magnitude spectrum of inverter line voltage $v_{AB}(t)$.

7.3 Sweep evidence: V/f schedule and fundamental tracking

Figure 3 shows $A(f)$ and Figure 4 shows the fundamental proxy extracted from spectral content.

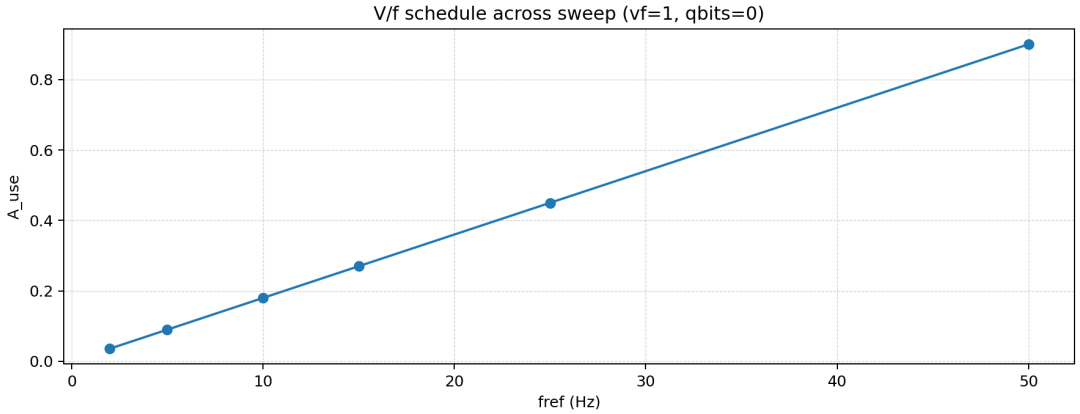

Figure 3: Scheduled modulation amplitude A versus commanded frequency.

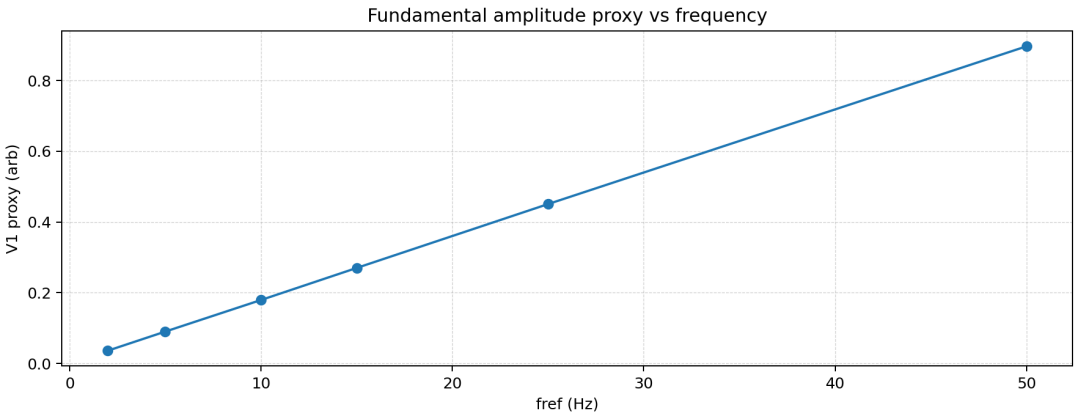

Figure 4: Fundamental magnitude proxy of $v_{AB}(t)$ versus frequency.

7.4 Distortion and switching activity trends

Figures 5 and 6 show THD proxy and switching activity proxy.

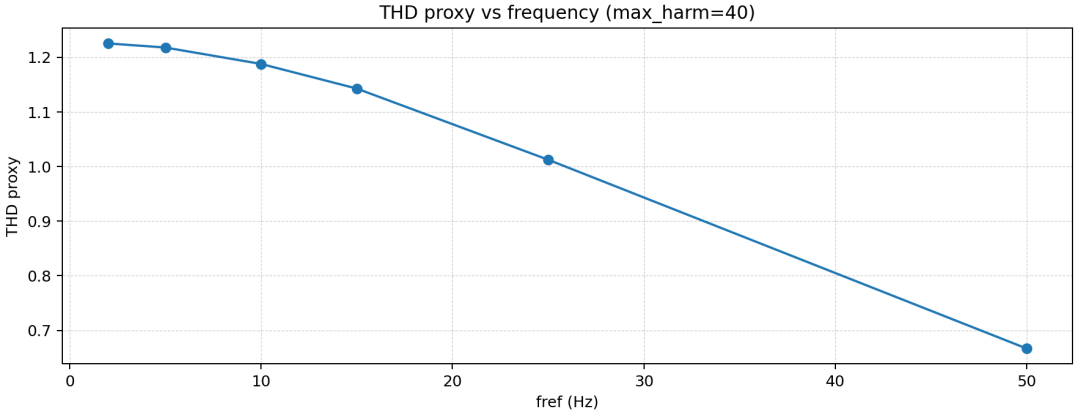

Figure 5: THD proxy versus commanded frequency.

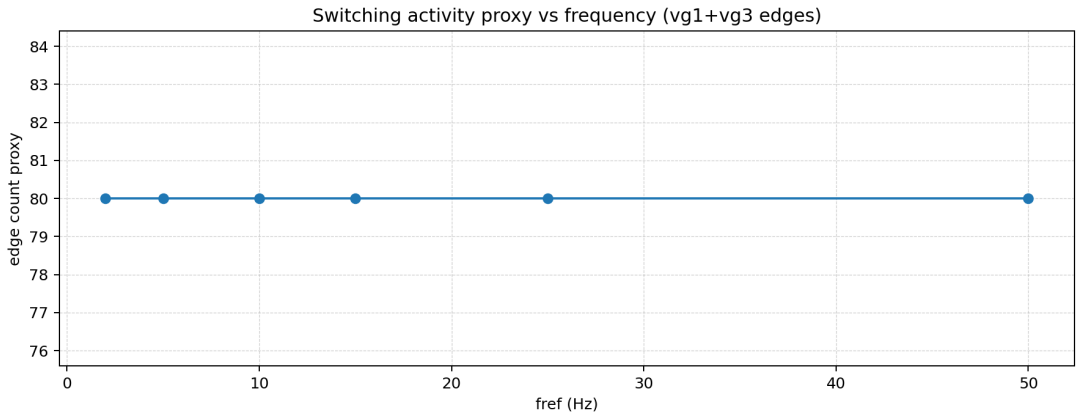

Figure 6: Switching activity proxy (edge count) versus commanded frequency.

8 Fourier-Series Interpretation of the Line Voltage

Treat $v_{AB}(t)$ as periodic with $\theta = 2\pi f_{\text{ref}} t$. Then:

$$v_{AB}(\theta) = \frac{a_0}{2} + \sum_{k=1}^{\infty} \left(a_k \cos(k\theta) + b_k \sin(k\theta)\right).$$

The truncated reconstruction:

$$\hat{v}_{AB}^{(K)}(\theta) = \frac{a_0}{2} + \sum_{k=1}^{K} \left(a_k \cos(k\theta) + b_k \sin(k\theta)\right)$$

provides a classical separation of fundamental and harmonics.

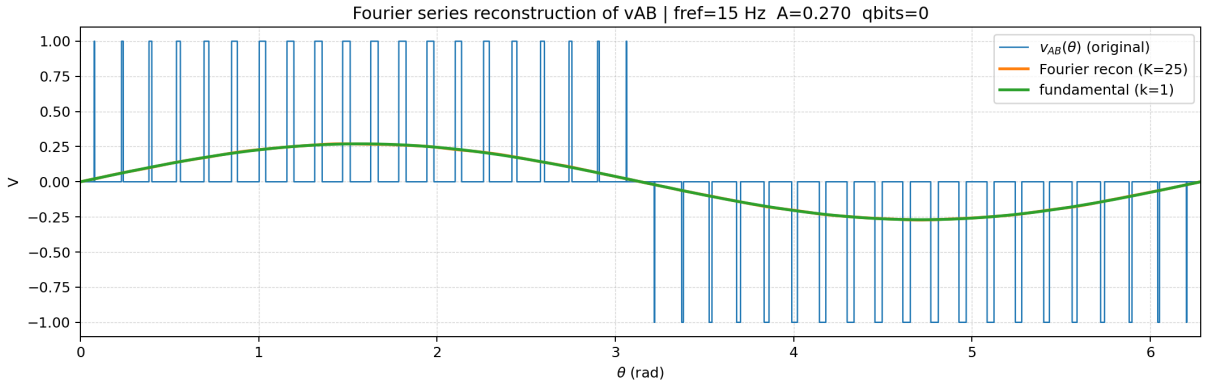

Figure 7: Fourier-series reconstruction (truncated) of $v_{AB}(\theta)$.

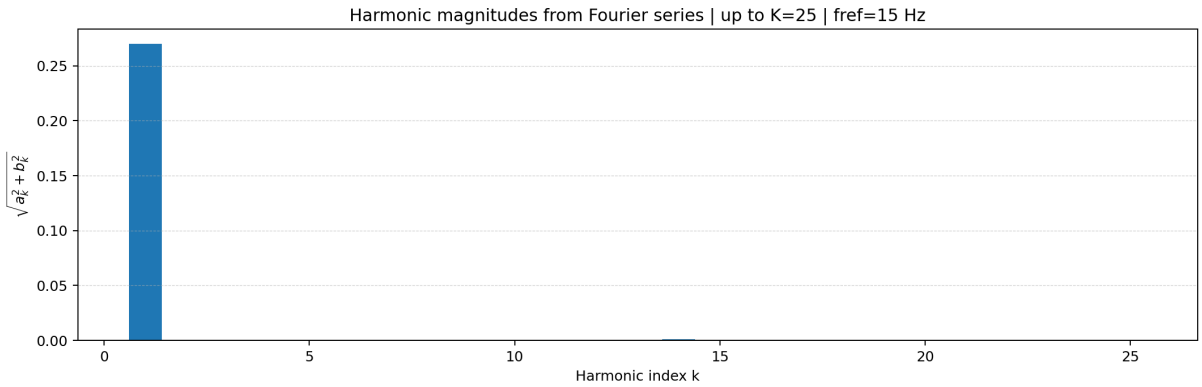

Figure 8: Harmonic magnitudes from Fourier coefficients up to $K = 25$.

9 VLSI / RTL Implementation Oriented Design

9.1 Discrete-time realization and fixed-point signal model

A synthesizable implementation updates at a sample enable rate f_s. A phase accumulator provides numerically controlled oscillator (NCO) behavior:

$$\phi[n+1] = \phi[n] + \Delta\phi, \qquad \Delta\phi = \left\lfloor \frac{f_{\text{ref}}}{f_s} 2^{N_\phi} \right\rceil .$$

Sine generation uses a LUT (ROM) indexed by MSBs of $\phi[n]$ (or CORDIC). The output $s[n] \approx \sin(\phi[n])$ is represented in signed fixed-point $Q1.(N_m - 1)$.

Amplitude A is unsigned fixed-point $Q1.(N_a - 1)$ with clamp to $A_{max} < 1$. The scaled reference:

$$v_m[n] = A \cdot s[n]$$

is computed using a fixed-point multiplier (or LUT pre-scaling).

9.2 Triangle carrier generator and carrier quantization relation

The carrier can be an up-down counter over M steps (half cycle), giving:

$$f_{car} = \frac{f_s}{2M}.$$

Thus, carrier resolution and switching frequency are directly coupled.

9.3 Comparator-only PWM core (synthesizable)

At each sample:

$$g_1[n] = \mathbb{1}\{v_m[n] \geq v_{cr}[n]\}, \qquad g_3[n] = \mathbb{1}\{-v_m[n] \geq v_{cr}[n]\}.$$

Complementary signals:

$$g_2[n] = \neg g_1[n], \qquad g_4[n] = \neg g_3[n].$$

9.4 Dead-time insertion as a safety-critical FSM

Dead-time enforces non-overlap between complementary devices. For each leg, implement states {HI_ON, LO_ON, BLANK}. BLANK persists for N_{dt} clock cycles:

$$N_{dt} = \lceil t_{dt} f_{clk} \rceil.$$

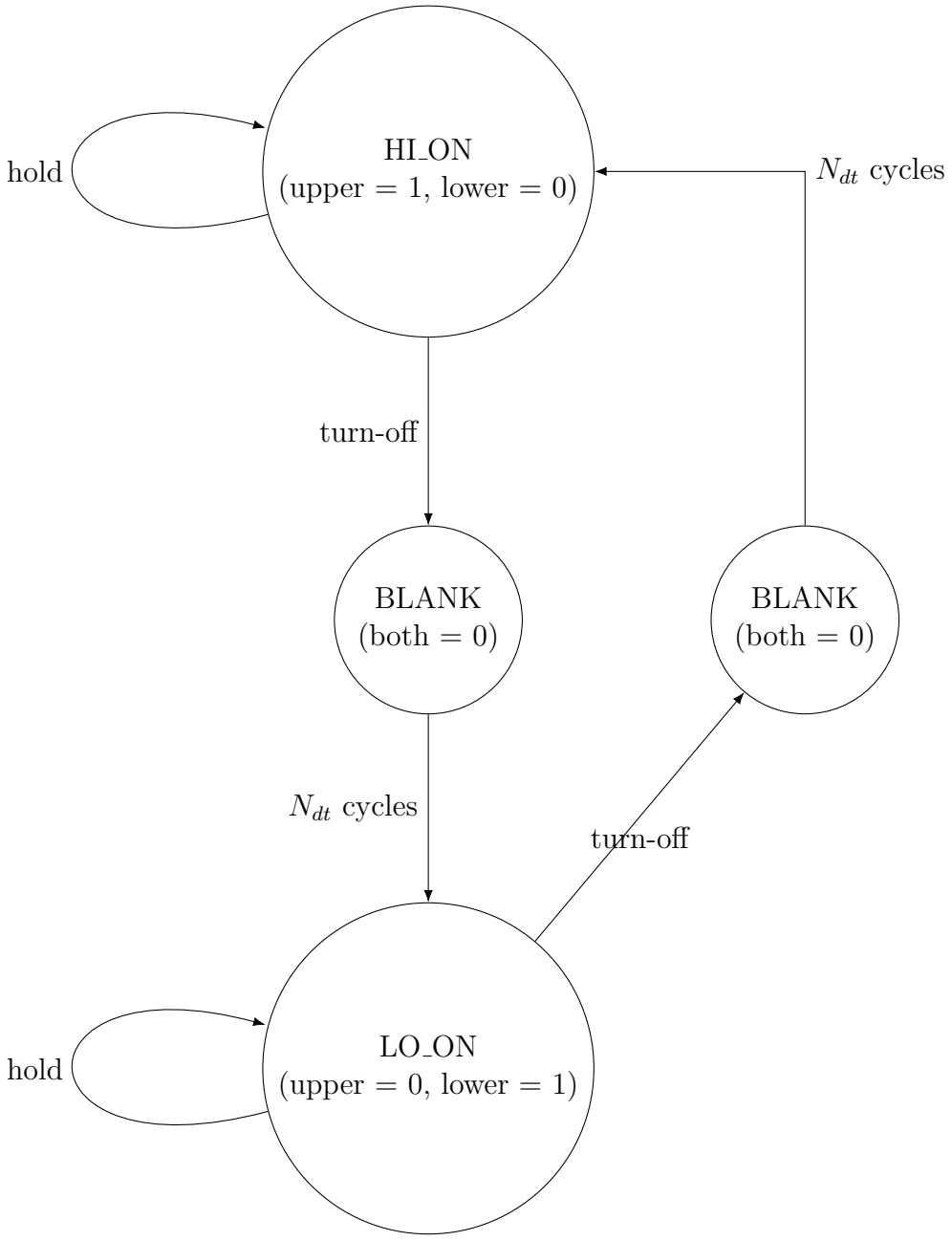

Figure 9: Dead-time insertion FSM per inverter leg (synthesizable control).

9.5 Vertical RTL datapath (layout-stable)

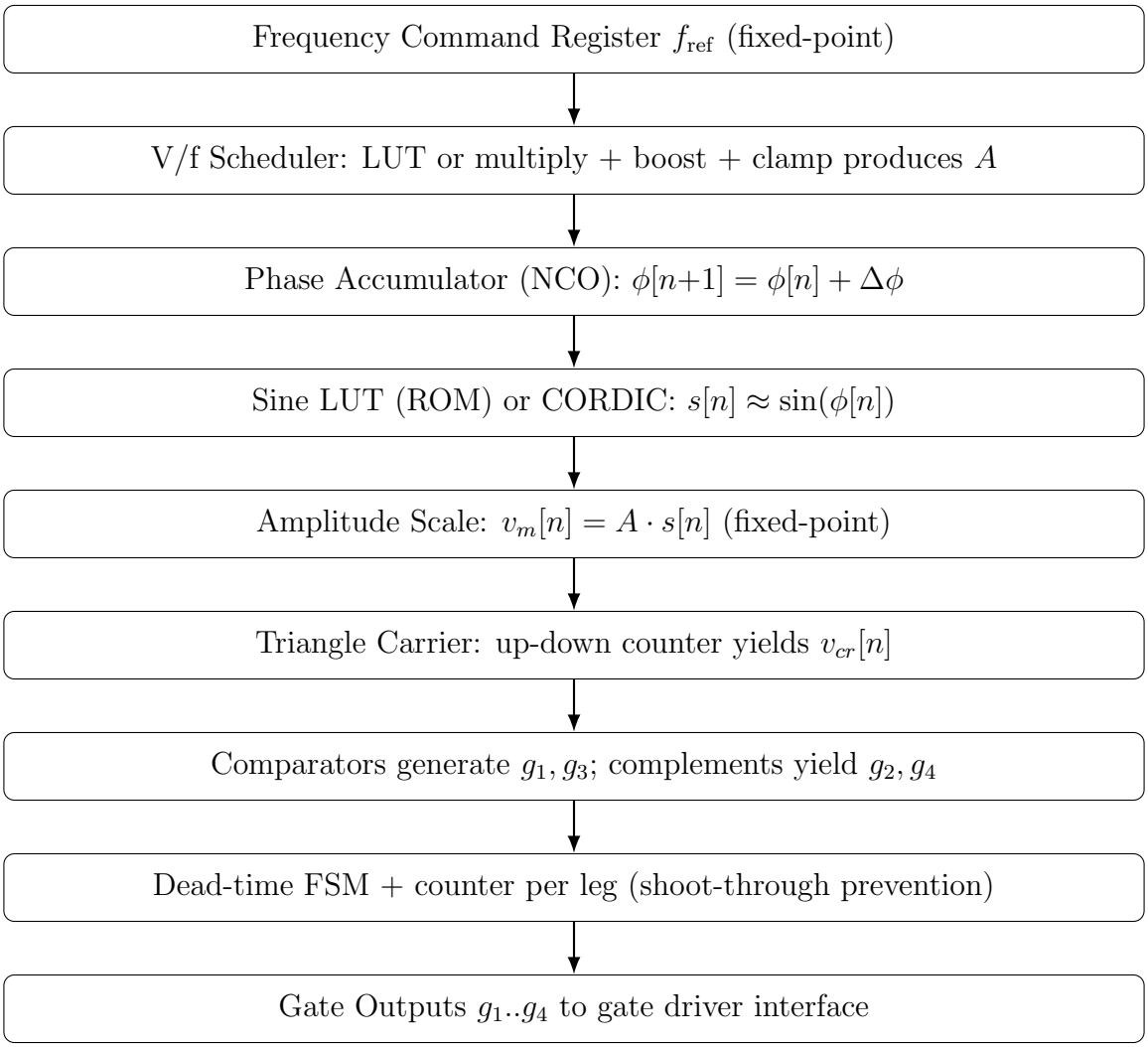

Figure 10: Synthesizable RTL datapath for bipolar SPWM with V/f control (vertical layout).

9.6 Dead-time waveform evidence

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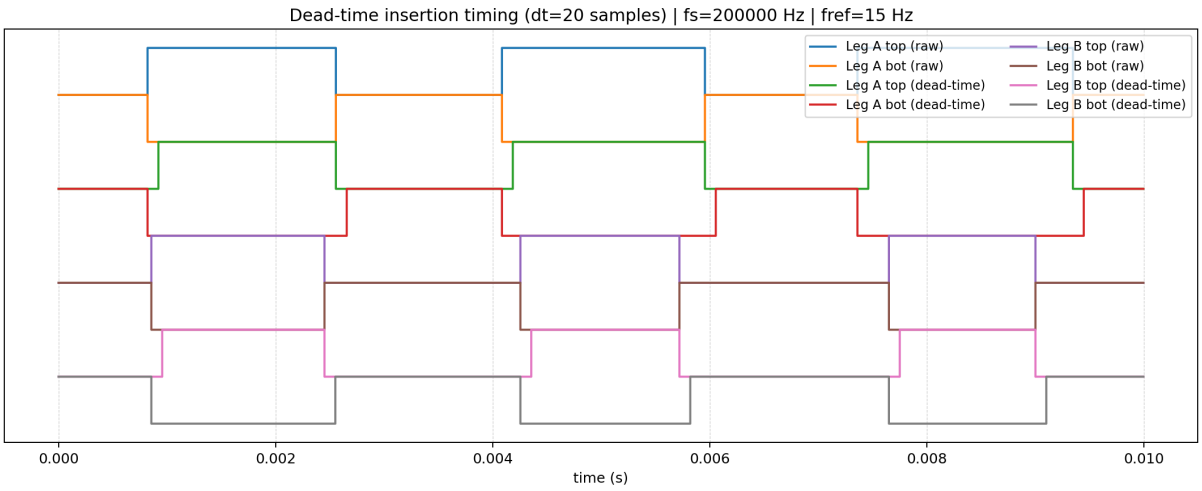

Figure 11: Dead-time timing evidence (non-overlap interval) derived from gate waveform transitions.

9.7 Area, timing, and bit-width planning

Signal	Typical bits	Format	Primary impact
Phase ϕ	24–32	unsigned	frequency resolution, jitter
Sine s	12–16	signed $Q1.(N-1)$	harmonic floor, LUT error
Amplitude A	10–14	unsigned $Q1.(N-1)$	V/f slope quantization
Carrier v_{cr}	12–16	signed	PWM resolution, sideband shaping
Dead-time counter	8–16	unsigned	safety margin granularity

Table 1: Fixed-point sizing guidance for a synthesizable bipolar SPWM modulator.

10 Applications

The experimentally validated bipolar SPWM with V/f control, dead-time insertion, and harmonic analysis demonstrated in this work directly maps to several high-impact power electronics and motor-drive applications. This section contextualizes the obtained waveforms, spectra, and sweep results within real deployment scenarios.

10.1 Induction motor control (scalar V/f drive)

Induction motors remain the most widely deployed industrial actuators due to robustness and low cost. Scalar V/f control is commonly used where precise torque control is not required.

Relevance of results:

- The measured linear fundamental amplitude vs frequency sweep validates constant air-gap flux operation.

- Low-frequency operation (2–10 Hz) demonstrates stable modulation without loss of fundamental tracking.
- Harmonic spectra confirm dominant carrier-sideband placement, simplifying motor-side filtering.

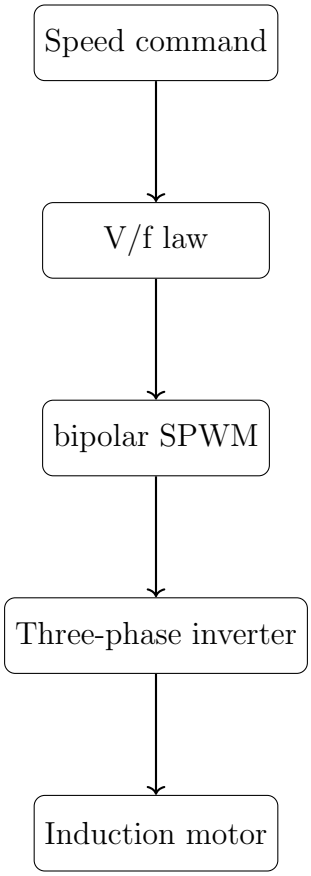

Figure 12: Scalar V/f induction motor drive using bipolar SPWM.

This architecture corresponds directly to the measured waveforms and V/f sweep results presented earlier.

10.2 Electric vehicle motor drives

Electric vehicles employ high-efficiency inverters driving PMSM or induction motors under wide speed ranges.

Relevance of results:

- bipolar SPWM reduces switching loss relative to bipolar schemes.
- Dead-time waveform evidence demonstrates safe high-frequency switching without shoot-through.
- Spectral results enable predictable EMI and acoustic noise behavior.

Although field-oriented control (FOC) is used in production EVs, the presented modulator and dead-time stage form the *inner switching layer* even in vector-controlled systems.

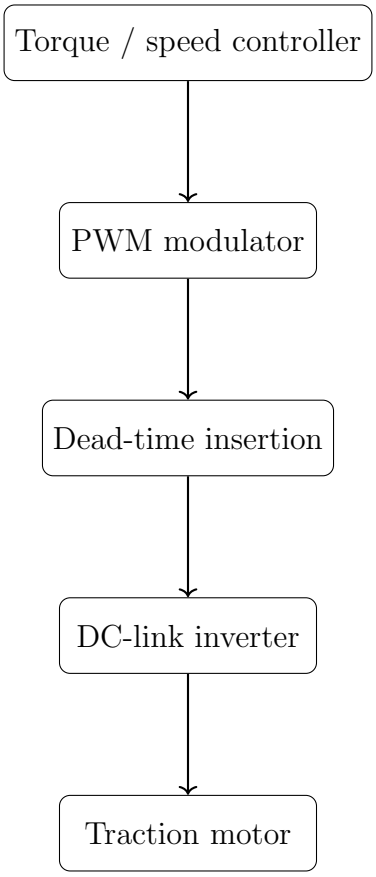

Figure 13: EV traction inverter switching chain highlighting PWM and dead-time stages.

10.3 Grid-connected inverter systems

Single- and three-phase inverters are central to renewable energy integration and distributed generation.

Relevance of results:

- FFT spectra quantify harmonic injection into the grid.
- Fundamental tracking validates modulation linearity under frequency variation.
- Switching activity sweep enables inverter loss estimation.

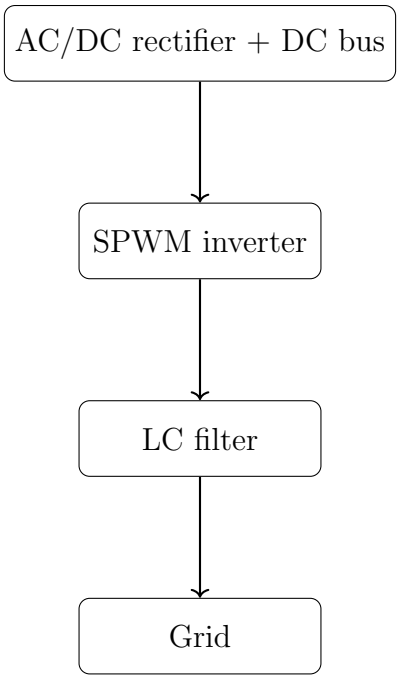

Figure 14: Grid-tied inverter using bipolar SPWM.

The measured harmonic distribution directly informs filter design and grid-code compliance.

10.4 Active harmonic filtering

Active power filters inject compensating currents to cancel harmonic distortion in industrial power systems.

Relevance of results:

- Harmonic magnitude plots identify dominant orders requiring compensation.
- High carrier-to-fundamental ratio enables precise current shaping.
- Dead-time control preserves accuracy at high switching frequencies.

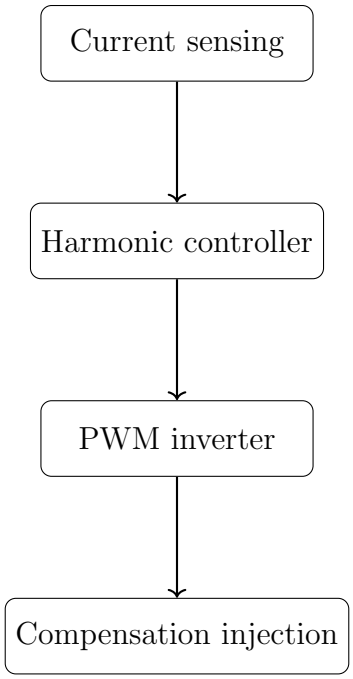

Figure 15: Active harmonic filter based on PWM inverter.

The presented Fourier analysis and THD trends provide quantitative grounding for filter effectiveness.

11 Conclusion

This report demonstrates bipolar SPWM with scalar V/f control using time-domain, spectral, Fourier-series, and sweep-level evidence. The harmonic structure and trends support quality-versus-stress discussion using distortion and switching proxies. A synthesizable RTL architecture is provided with explicit fixed-point definitions, carrier frequency relations, and dead-time insertion as a safety-critical FSM. This establishes a VLSI-credible foundation for implementing a digital VFD modulator in ASIC or FPGA.