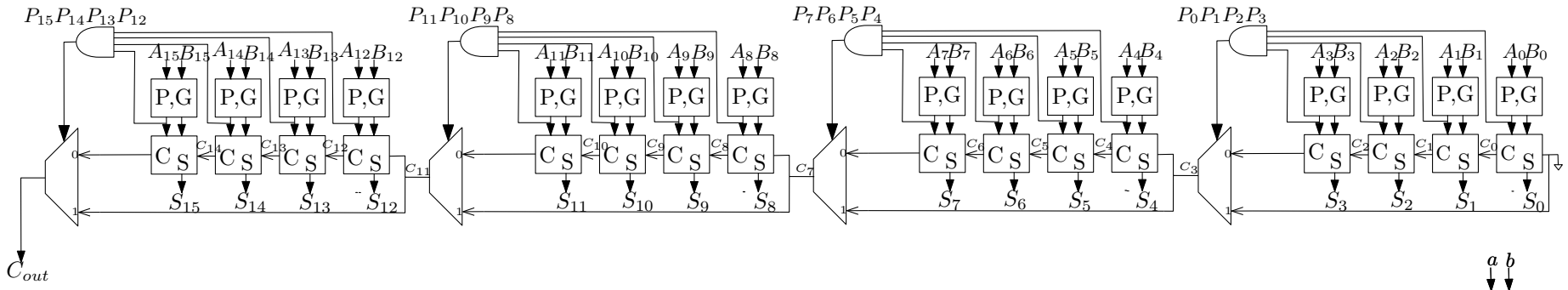
CARRY BYPASS ADDER ARCHITECTURE



$t_{sum} = 2 * t_{XOR-2}, t_{carry} = t_{OR-2} + t_{AND-2}$

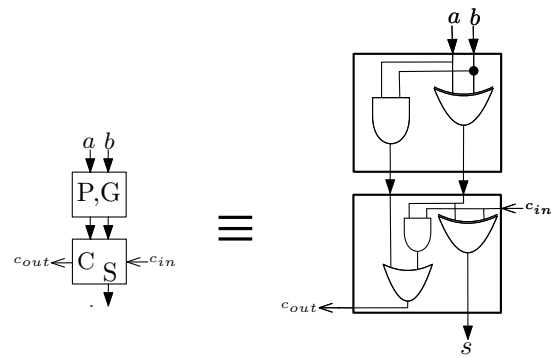
16-bit Carry By Pass Adder Delay (Block Size = 4):

For the worst case of ripple carry adder (A = 4'hFFFF, B = 4'h0001):

$\longrightarrow T_{SUM} = 4 * t_{carry} + 3 * T_{2:1-MUX} + 3 * t_{carry} + t_{sum}$

$\longrightarrow T_{SUM} = 7 * t_{carry} + 3 * T_{2:1-MUX} + t_{sum}$

$\longrightarrow T_{CARRY} = 8 * t_{carry} + 4 * T_{2:1-MUX}$



$C_0 = A_0B_0 + B_0C_{in} + C_{in}A_0 = A_0B_0 + (A_0 \oplus B_0)C_{in}$

$\longrightarrow C_o = G_0 + P_0C_{in} (G_0 = A_0B_0, P_0 = A_0 \oplus B_0)$

N-bit Carry By Pass Adder Delay With Block Size 'M':

For the worst case of ripple carry adder:

$$T_{SUM} = (2 * M - 1) * t_{carry} + (\frac{N}{M} - 1) * T_{2:1-MUX} + t_{sum}$$

$$T_{CARRY} = 2 * M * t_{carry} + (\frac{N}{M}) * T_{2:1-MUX}$$