A Study of prefetching methods (hardware and software) and their impact on performance

October 2, 2019

List of Group Members
1. Aanand Vishnu - 18114001
2. Ankita Dhiman - 18116010
3. Dileep Kushwaha - 18116027
4. Ravindra - 18114064
5. Sanchit Gupta - 18116068
6. Sanjeev Kumar Nirmal - 18116069
7. Subhash Suryawanshi - 18117076

1 Abstract

The purpose of this paper is to study different methods that classifies various design concerns in developing a prefetching strategy. We discuss various prefetching strategies and issues that have to be considered in designing a prefetching strategy for multi-core processors.
Data prefetching has been considered an effective way to mask data access latency caused by cache misses and to bridge the performance gap between processor and memory.
A good prediction method must not only be accurate, but prefetches must be initiated early enough to allow time for the instructions to return from main memory. Hybrid hardware/software controlled strategies are gaining popularity on processors with multi-thread support. To be effective, a prefetching strategy for multi-core processing environments has to be adaptive to choose among multiple methods to predict future data accesses.
In this paper, hardware prefetching methods like Stream Buffer, Stride, Next-Line (or Adjacent-Line) and Instruction Pointer as well as software based prefetching methods given by the complier and programmer are studied and analysed.