

## Laboratory 6

### Combinational Circuits-II Multiplexers and Demultiplexers

#### 1. Introduction and Purpose of Experiment

Students will learn to design, simulate and implement circuits using Multiplexers and Demultiplexers.

#### 2. Aim and Objectives

**Aim:** To verify functionality of Mux and Demux and use Multiplexer to implement Boolean functions

**Objectives:** At the end of this lab, the student will be able to

- Verify the functionality of Mux and Demux
- Use Multiplexers to implement given Boolean Functions

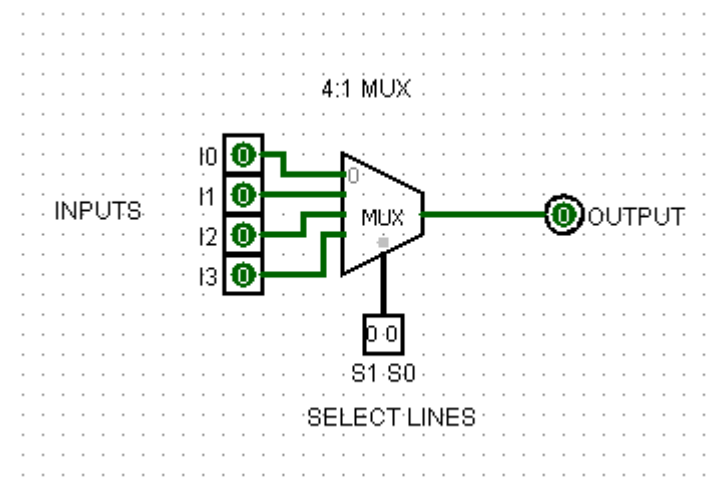
#### 3. Experimental Procedure

- Write truth tables and block diagrams for
  - 4 to 1 Multiplexer
  - 8 to 1 Multiplexer
  - 1 to 4 Demultiplexer
  - 1 to 8 Demultiplexer
- Construct the circuits for 3 (a) (I) to 3 (a) (IV) above using appropriate ICs. Verify the functionality and show the output to the course leader
- Use Logisim to simulate the circuits designed above.
- Using an example, show how any Boolean Expression in SoP form can be implemented using a Multiplexer. Simulate the same using Logisim.

Your document should include:

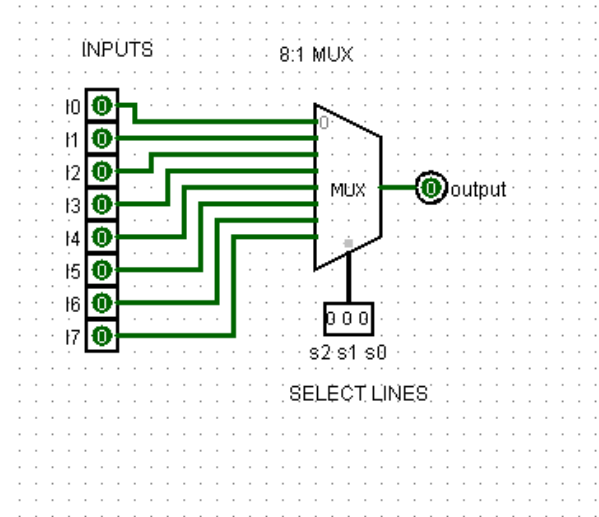
- Handwritten truth tables and block diagrams for the circuits in 3(a).
- Logisim screenshots of all the Multiplexers and Demultiplexers.
- Answer to 3(d)
- Logisim screenshots for 3(d)

4:1 Multiplexer circuit



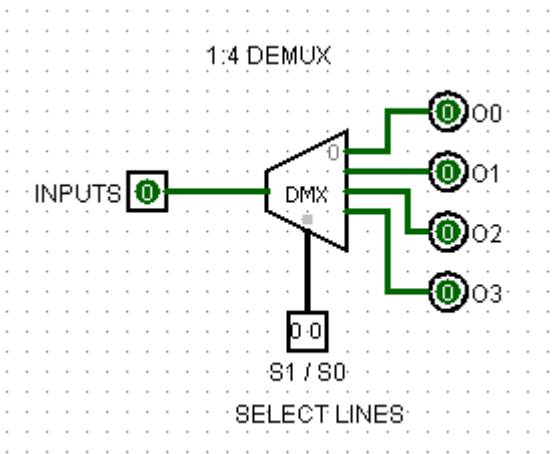
Select Data Inputs		Output
$S_1$	$S_0$	$Y$
0	0	$D_0$
0	1	$D_1$
1	0	$D_2$
1	1	$D_3$

8:1 Multiplexer



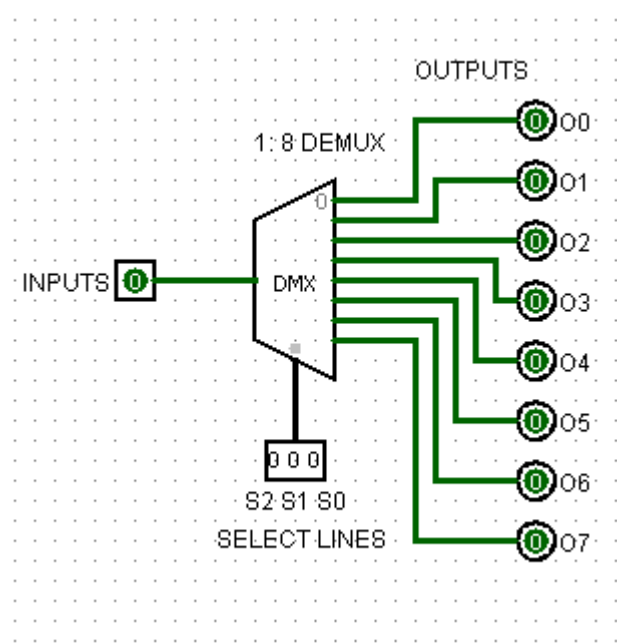
Select Data Inputs			Output
$S_2$	$S_1$	$S_0$	$Y$
0	0	0	$D_0$
0	0	1	$D_1$
0	1	0	$D_2$
0	1	1	$D_3$
1	0	0	$D_4$
1	0	1	$D_5$
1	1	0	$D_6$
1	1	1	$D_7$

1:4 DeMultiplexer



Data Input	Select Inputs		Outputs			
D	S <sub>1</sub>	S <sub>0</sub>	Y <sub>3</sub>	Y <sub>2</sub>	Y <sub>1</sub>	Y <sub>0</sub>
D	0	0	0	0	0	D
D	0	1	0	0	D	0
D	1	0	0	D	0	0
D	1	1	D	0	0	0

1:8 DeMultiplexer



Data Input	Select Inputs			Outputs							
D	S <sub>2</sub>	S <sub>1</sub>	S <sub>0</sub>	Y <sub>7</sub>	Y <sub>6</sub>	Y <sub>5</sub>	Y <sub>4</sub>	Y <sub>3</sub>	Y <sub>2</sub>	Y <sub>1</sub>	Y <sub>0</sub>
D	0	0	0	0	0	0	0	0	0	0	D
D	0	0	1	0	0	0	0	0	0	D	0
D	0	1	0	0	0	0	0	0	D	0	0
D	0	1	1	0	0	0	0	D	0	0	0
D	1	0	0	0	0	0	D	0	0	0	0
D	1	0	1	0	0	D	0	0	0	0	0
D	1	1	0	0	D	0	0	0	0	0	0
D	1	1	1	D	0	0	0	0	0	0	0