Logic Design Laboratory

CSC206A

B.Tech. III Semester

Department: Computer Science and Engineering

Faculty of Engineering & Technology

Ramaiah University of Applied Sciences

Name: SUBHENDU MAJI Roll Number: 18ETCS002121

Ramaiah University of Applied Sciences

Private University Established in Karnataka State by Act No. 15 of 2013

Faculty	Engineering & Technology
Programme	B. Tech. in Computer Science and engineering
Year/Semester	3rd Semester
Name of the Laboratory	Logic Design Laboratory
Laboratory Code	CSC206A

List of Experiments

Day-1

1. Build digital circuits using logic gates. Verify using truth table.
   W=BC+~BC
   X=~AB+~AB~C+~ABCD+~AB~C~DE
   Y=BD+B(D+~E)+~D(D+F)
   Z=A~BC+~ABC+~A~BC
   AB+A(B+C)+B(B+C)
   (A~B(C+BD)+~A~B)C
   ~A~B~C+~ABC+A~B~C+A~BC+ABC
   (A+~A)(AB+ AB~C)
   X~Y~Z+~XYZ

Day-2

2. Build a circuit which is dual of the given expression. Verify using truth table.
   ~(~(AB)~(CD))=AB+CD
   ~(~(AB)C)=AB+~C
   ~(A~(BC))=~A+BC
   ~(ABC)=~A+~B+~C
   A(~(B+C)=A~B~C
   ~(~AB(C+~D)+E)=A~E+~B~E+~CD~E

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Laboratory 1

Title of the Laboratory Exercise

Introduction and Purpose of Experiment

In this laboratory exercises students get familiar with Logisim.

Build digital circuits using logic gates. Verify using truth table.

1. Aim and Objectives

   Aim

   - To use Logisim

2. Objectives

   At the end of this lab, the student will be able to

   - Explain the features and use of Logisim
   - Design digital circuits using Logisim

3. Experimental Procedure

Aim and objective
Requirement and equipment used
Simulation and realization
Verification results and Analysis
Conclusion
Limitations and Recommendations
Viva

Students are given a set of logical expression. Using Logisim students are expected to build circuit. And test.

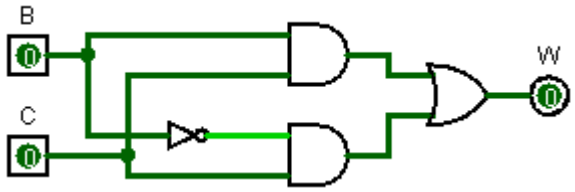
4. Questions

   a. **W=BC+~BC**
   b. **X=~AB+~AB~C+~ABCD+~AB~C~DE**
   c. **Y=BD+B(D+~E)+~D(D+F)**
   d. **Z=A~BC+~ABC+~A~BC**

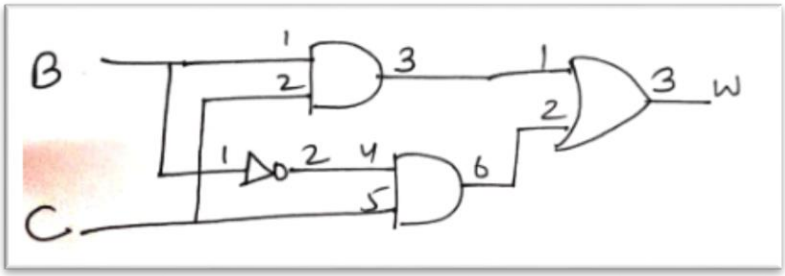
e. **AB+A(B+C)+B(B+C)**
f. **(A~B(C+BD)+~A~B)C**
g. **~A~B~C+~ABC+A~B~C+A~BC+ABC**
h. **(A+~A)(AB+ AB~C)**
i. **X~Y~Z+~XYZ**

Solutions:

a. **W=BC+~BC**



B	C	W
0	0	0
0	1	1
1	0	0
1	1	1



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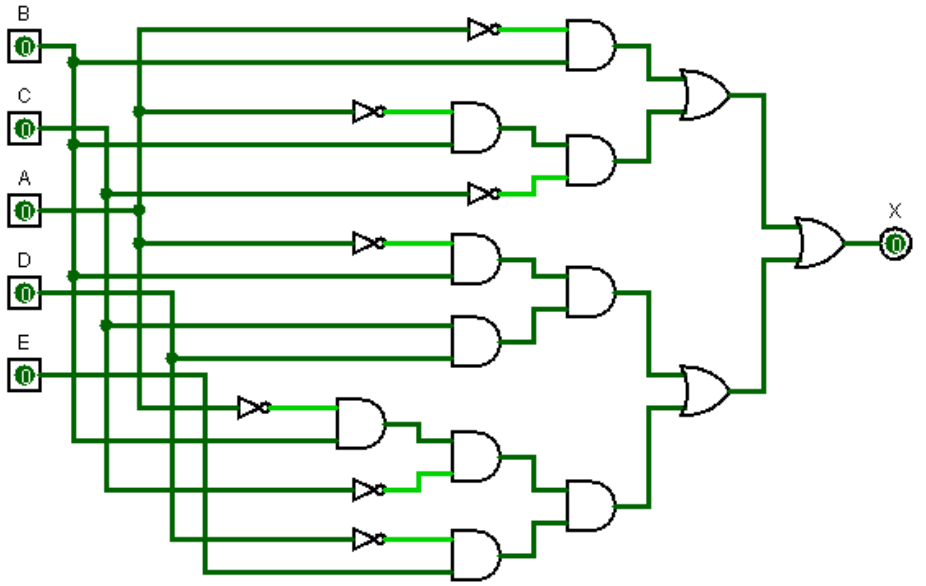
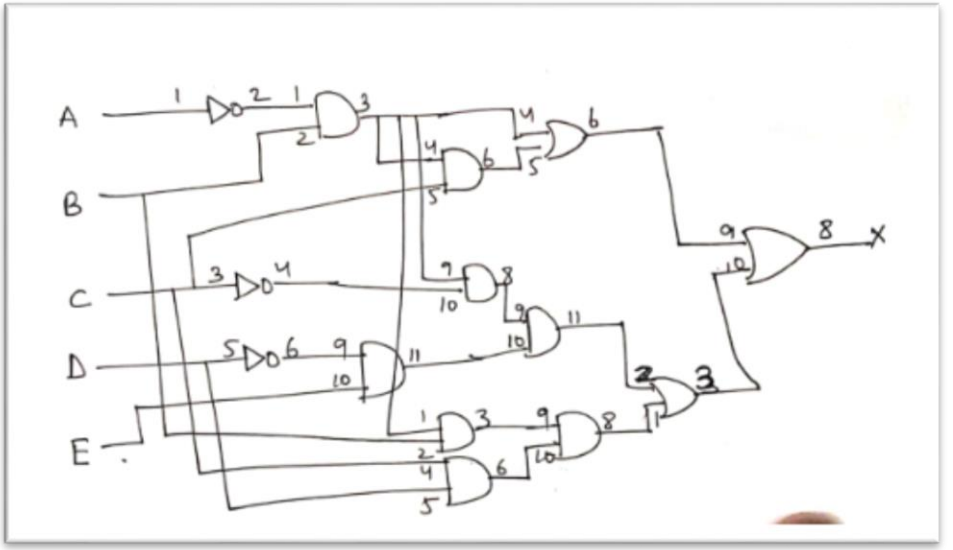
b. X=~AB+~AB~C+~ABCD+~AB~C~DE





A	B	C	D	E	X
0	0	0	0	0	0
0	0	0	0	1	0
0	0	0	1	0	0
0	0	0	1	1	0
0	0	1	0	0	0
0	0	1	0	1	0
0	0	1	1	0	0
0	0	1	1	1	0
0	1	0	0	0	1
0	1	0	0	1	1
0	1	0	1	0	1
0	1	0	1	1	1
0	1	1	0	0	1
0	1	1	0	1	1
0	1	1	1	0	1
0	1	1	1	1	1
1	0	0	0	0	0
1	0	0	0	1	0
1	0	0	1	0	0
1	0	0	1	1	0
1	0	1	0	0	0
1	0	1	0	1	0
1	0	1	1	0	0
1	0	1	1	1	0
1	1	0	0	0	0
1	1	0	0	1	0
1	1	0	1	0	0
1	1	0	1	1	0
1	1	1	0	0	0
1	1	1	0	1	0
1	1	1	1	0	0
1	1	1	1	1	0

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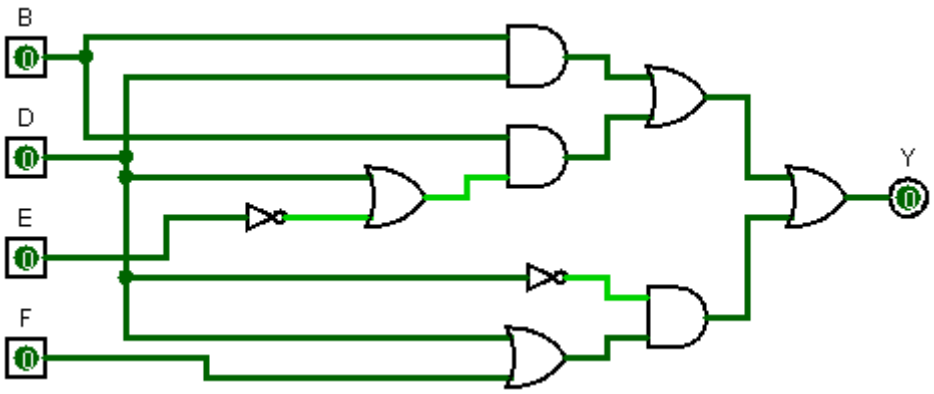
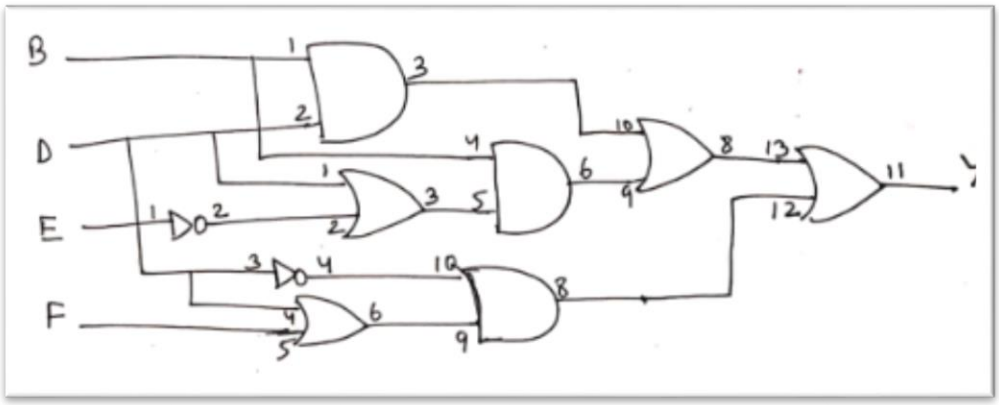
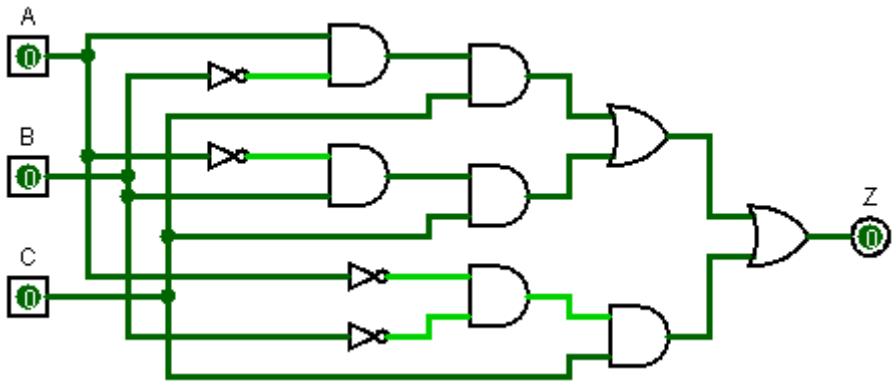
c. Y=BD+B(D+~E)+~D(D+F)



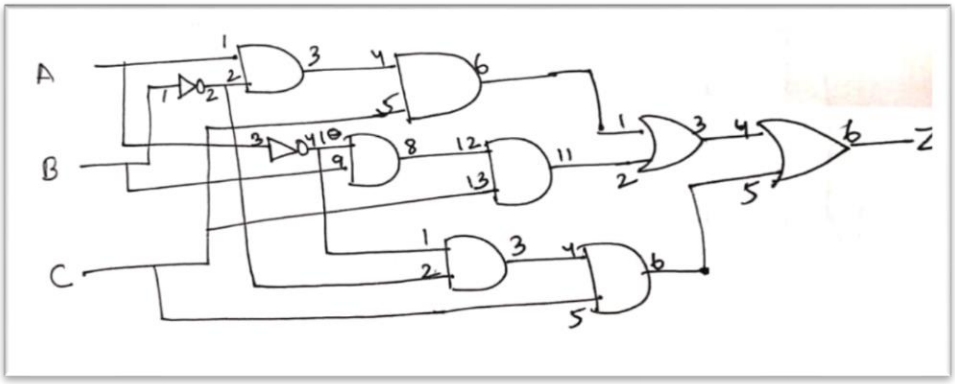


B	D	E	F	Y
0	0	0	0	0
0	0	0	1	1
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	0
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

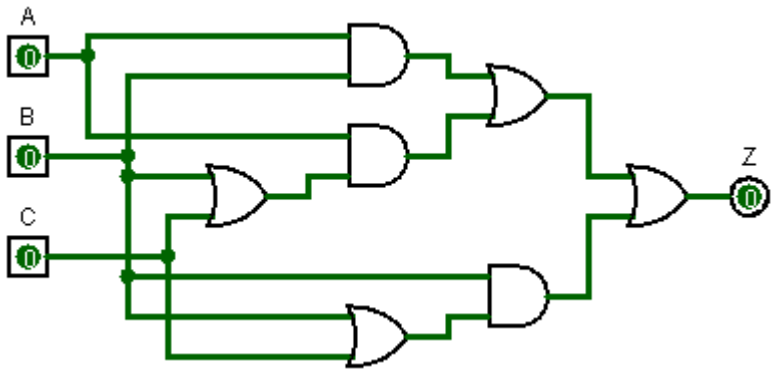
d. Z=A~BC+~ABC+~A~BC



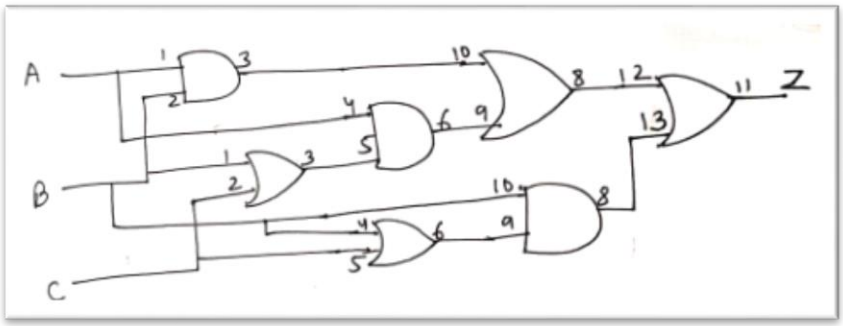
A	B	C	Z
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	0



e. AB+A(B+C)+B(B+C)



A	B	C	Z
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1



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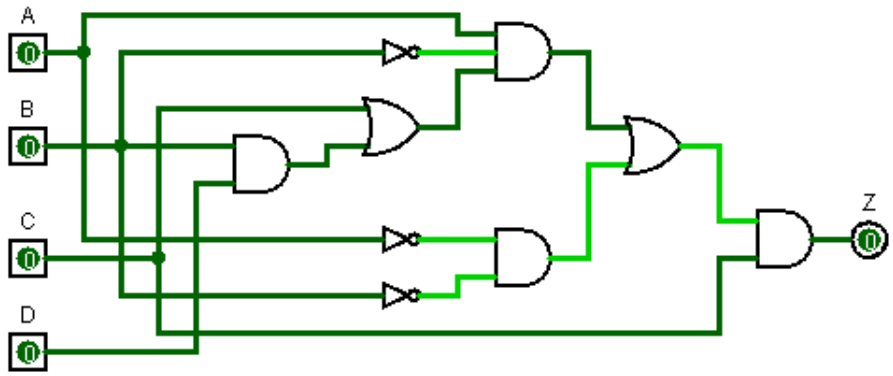
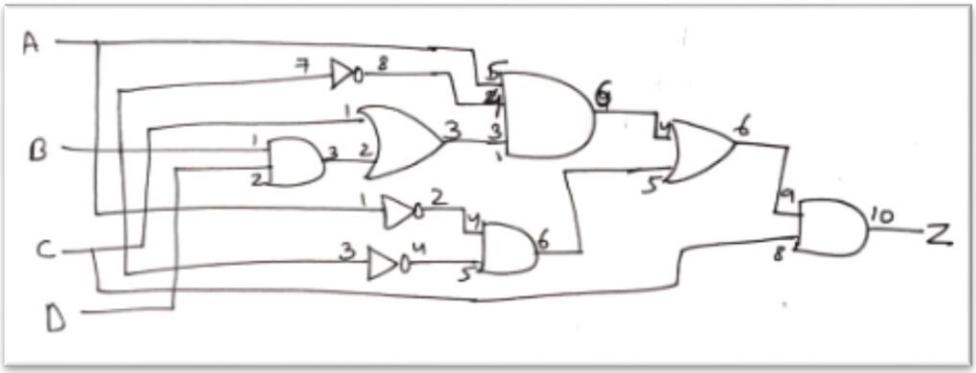
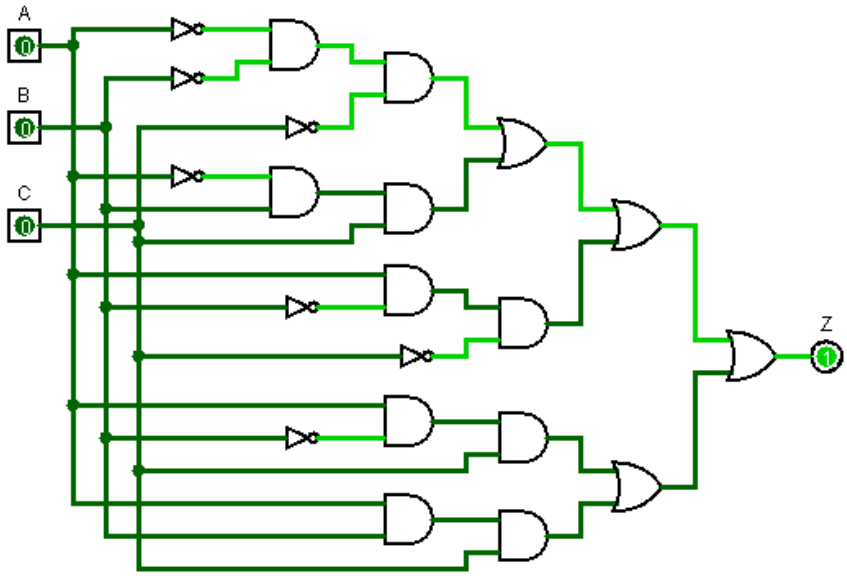
f. (A~B(C+BD)+~A~B)C



A	B	C	D	Y
0	0	0	0	0
0	0	0	1	0
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	1
1	0	1	1	1
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0



g. ~A~B~C+~ABC+A~B~C+A~BC+ABC



A	B	C	Z
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	1

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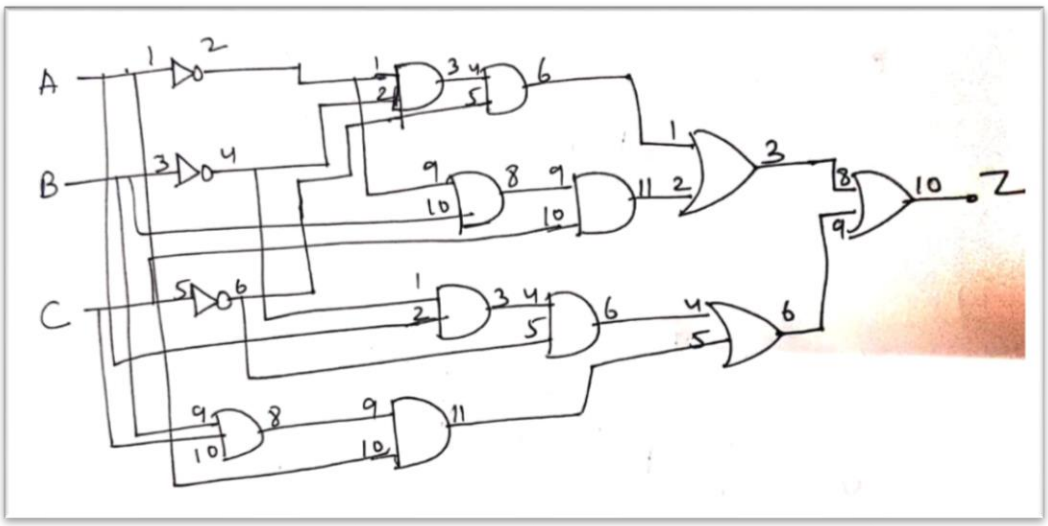
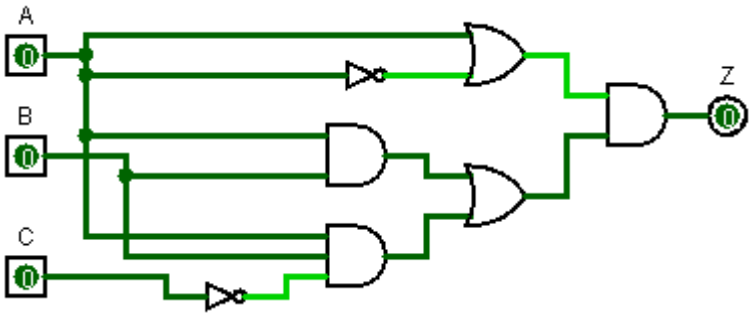
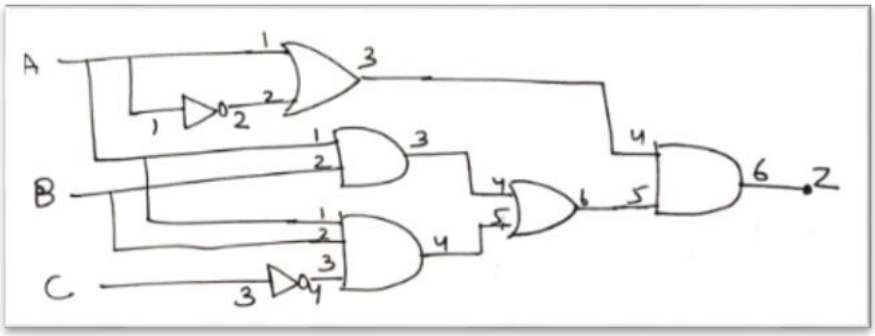


h. (A+~A)(AB+ AB~C)



A	B	C	Z
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1



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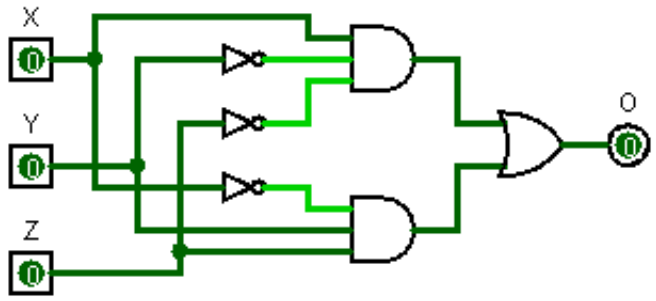
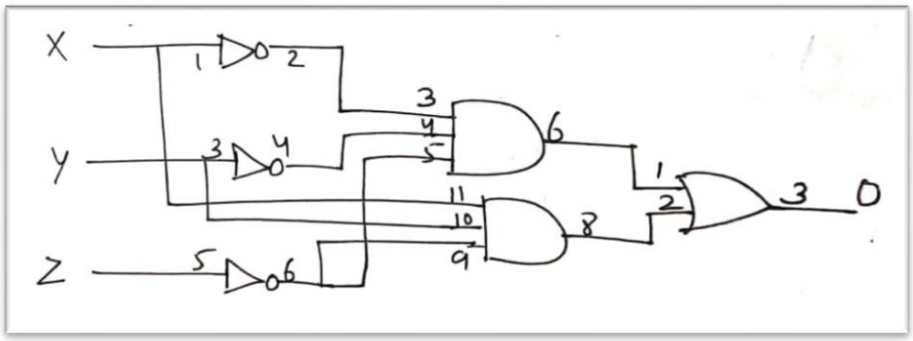
i. **X~Y~Z+~XYZ**



X	Y	Z	O
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0



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Laboratory 2

Title of the Laboratory Exercise:

Build a circuit which is dual of the given expression. Verify using truth table.

Introduction and Purpose of Experiment

1. Aim and Objectives

   Aim

   - To Design logic expression and realise the dual

2. Objectives

   At the end of this lab, the student will be able to

   - Students should be able to realise the expression and its dual

3. Experimental Procedure

Aim and objective
Requirement and equipment used
Simulation and realization
Verification results and Analysis
Conclusion
Limitations and Recommendations
Viva

4. Questions

   Build a circuit which is dual of the given expression. Verify using truth table.

   ~(~(AB)~(CD))=AB+CD
   ~(~(AB)C)=AB+~C
   ~(A~(BC))=~A+BC
   ~(ABC)=~A+~B+~C
   A(~(B+C)=A~B~C
   ~(~AB(C+~D)+E)=A~E+~B~E+~CD~E

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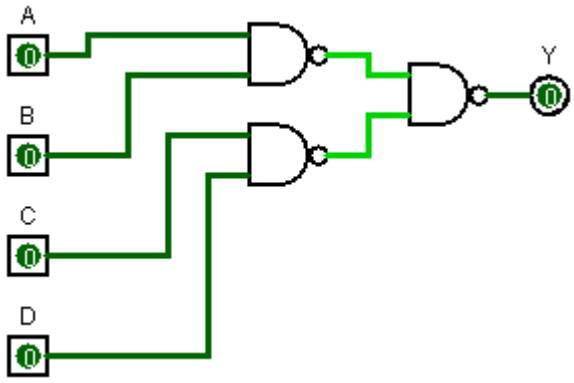
Solution:

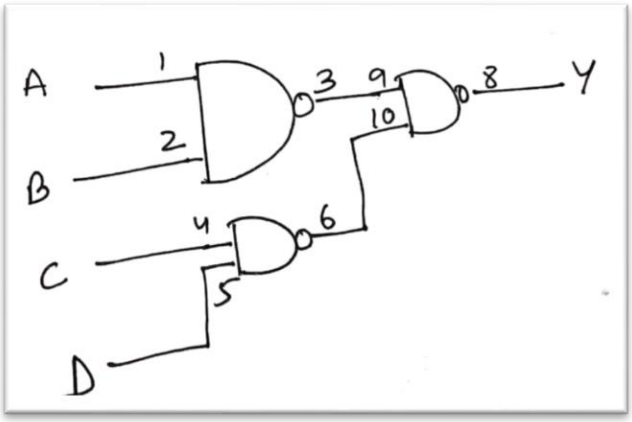
a. **~(~(AB)~(CD))=AB+CD**

LHS :



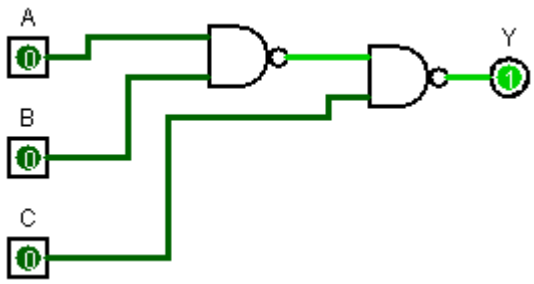
A	B	C	D	Y
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

RHS:



b. **~(~(AB)C)=AB+~C**

LHS:



A	B	C	Y
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

RHS:

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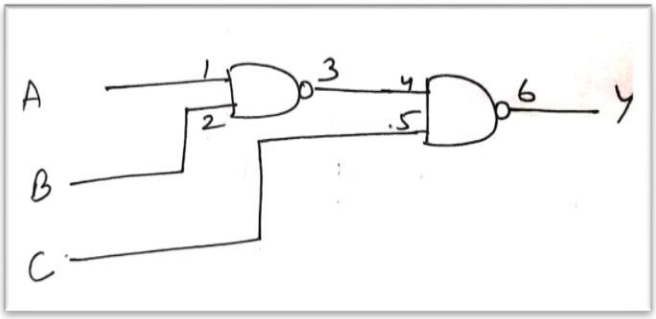
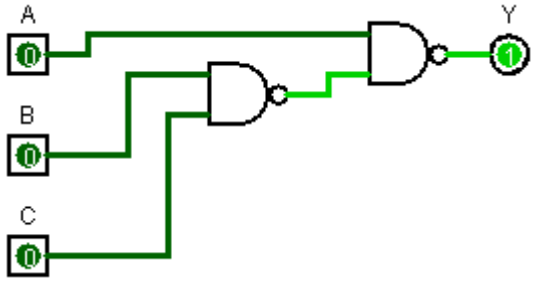


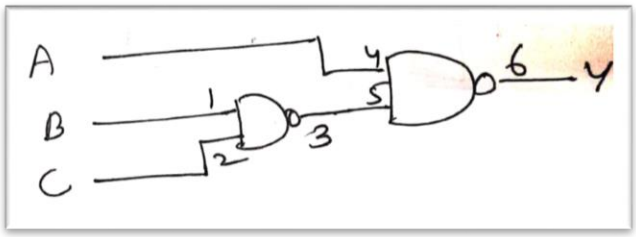
c. **~(A~(BC))=~A+BC**

LHS:



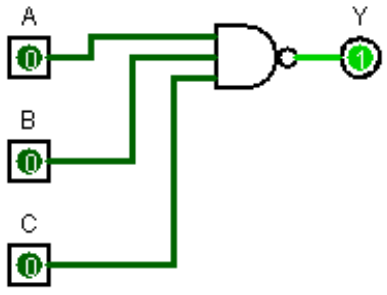
A	B	C	Y
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

RHS:



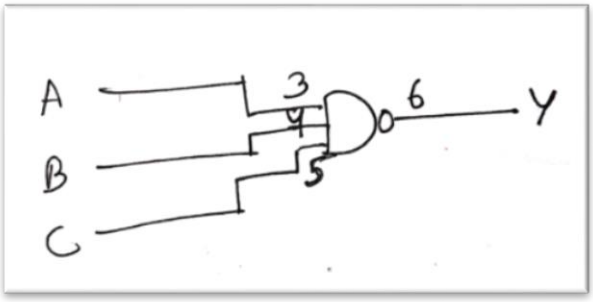
d. **~(ABC)=~A+~B+~C**

LHS:



A	B	C	Y
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

RHS



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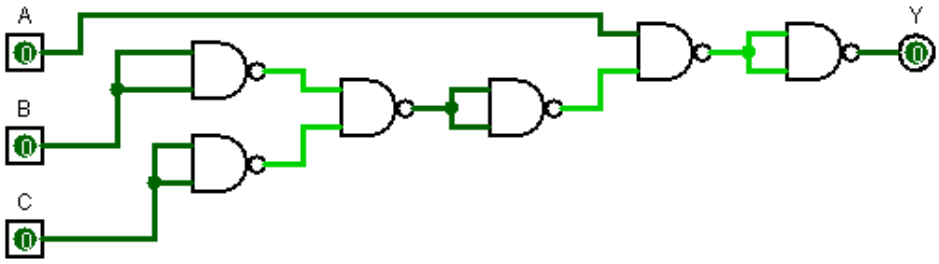
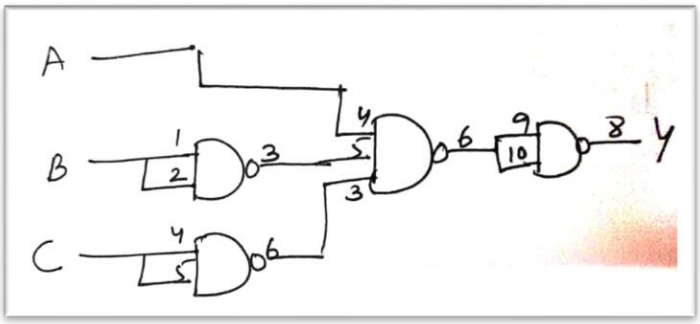
e. **A(~(B+C))=A~B~C**

LHS



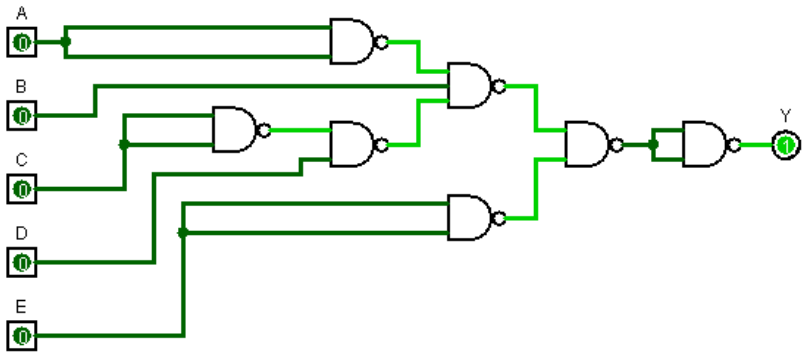
A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

RHS:

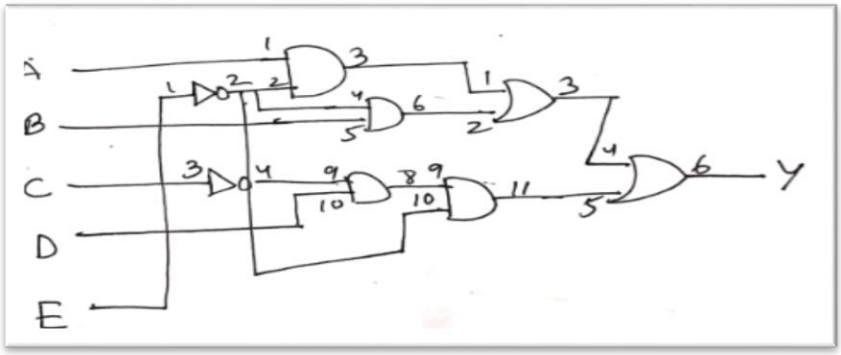


f. **~(~AB(C+~D)+E)=A~E+~B~E+~CD~E**

LHS:



RHS:



A	B	C	D	E	Y
0	0	0	0	0	1
0	0	0	0	1	0
0	0	0	1	0	1
0	0	0	1	1	0
0	0	1	0	0	1
0	0	1	0	1	0
0	0	1	1	0	1
0	0	1	1	1	0
0	1	0	0	0	0
0	1	0	0	1	0
0	1	0	1	0	1
0	1	0	1	1	0
0	1	1	0	0	0
0	1	1	0	1	0
0	1	1	1	0	0
0	1	1	1	1	0
1	0	0	0	0	1
1	0	0	0	1	0
1	0	0	1	0	1
1	0	0	1	1	0
1	0	1	0	0	1
1	0	1	0	1	0
1	0	1	1	0	1
1	0	1	1	1	0
1	1	0	0	0	1
1	1	0	0	1	0
1	1	0	1	0	1
1	1	0	1	1	0
1	1	1	0	0	1
1	1	1	0	1	0
1	1	1	1	0	1
1	1	1	1	1	0