

EG915Q-NA&BG9x&EG9x Series

Compatible Design

LTE Standard & LPWA Module Series

Version: 1.0

Date: 2023-05-12

Status: Released



At Quectel, our aim is to provide timely and comprehensive services to our customers. If you require any assistance, please contact our headquarters:

Quectel Wireless Solutions Co., Ltd.

Building 5, Shanghai Business Park Phase III (Area B), No.1016 Tianlin Road, Minhang District, Shanghai 200233, China

Tel: +86 21 5108 6236

Email: info@quectel.com

Or our local offices. For more information, please visit:

<http://www.quectel.com/support/sales.htm>.

For technical support, or to report documentation errors, please visit:

<http://www.quectel.com/support/technical.htm>.

Or email us at: support@quectel.com.

Legal Notices

We offer information as a service to you. The provided information is based on your requirements and we make every effort to ensure its quality. You agree that you are responsible for using independent analysis and evaluation in designing intended products, and we provide reference designs for illustrative purposes only. Before using any hardware, software or service guided by this document, please read this notice carefully. Even though we employ commercially reasonable efforts to provide the best possible experience, you hereby acknowledge and agree that this document and related services hereunder are provided to you on an “as available” basis. We may revise or restate this document from time to time at our sole discretion without any prior notice to you.

Use and Disclosure Restrictions

License Agreements

Documents and information provided by us shall be kept confidential, unless specific permission is granted. They shall not be accessed or used for any purpose except as expressly provided herein.

Copyright

Our and third-party products hereunder may contain copyrighted material. Such copyrighted material shall not be copied, reproduced, distributed, merged, published, translated, or modified without prior written consent. We and the third party have exclusive rights over copyrighted material. No license shall be granted or conveyed under any patents, copyrights, trademarks, or service mark rights. To avoid ambiguities, purchasing in any form cannot be deemed as granting a license other than the normal non-exclusive, royalty-free license to use the material. We reserve the right to take legal action for noncompliance with abovementioned requirements, unauthorized use, or other illegal or malicious use of the material.

Trademarks

Except as otherwise set forth herein, nothing in this document shall be construed as conferring any rights to use any trademark, trade name or name, abbreviation, or counterfeit product thereof owned by Quectel or any third party in advertising, publicity, or other aspects.

Third-Party Rights

This document may refer to hardware, software and/or documentation owned by one or more third parties ("third-party materials"). Use of such third-party materials shall be governed by all restrictions and obligations applicable thereto.

We make no warranty or representation, either express or implied, regarding the third-party materials, including but not limited to any implied or statutory, warranties of merchantability or fitness for a particular purpose, quiet enjoyment, system integration, information accuracy, and non-infringement of any third-party intellectual property rights with regard to the licensed technology or use thereof. Nothing herein constitutes a representation or warranty by us to either develop, enhance, modify, distribute, market, sell, offer for sale, or otherwise maintain production of any our products or any other hardware, software, device, tool, information, or product. We moreover disclaim any and all warranties arising from the course of dealing or usage of trade.

Privacy Policy

To implement Module functionality, certain device data are uploaded to Quectel's or third-party's servers, including carriers, chipset suppliers or customer-designated servers. Quectel, strictly abiding by the relevant laws and regulations, shall retain, use, disclose or otherwise process relevant data for the purpose of performing the service only or as permitted by applicable laws. Before data interaction with third parties, please be informed of their privacy and data security policy.

Disclaimer

- a) We acknowledge no liability for any injury or damage arising from the reliance upon the information.
- b) We shall bear no liability resulting from any inaccuracies or omissions, or from the use of the information contained herein.
- c) While we have made every effort to ensure that the functions and features under development are free from errors, it is possible that they could contain errors, inaccuracies, and omissions. Unless otherwise provided by valid agreement, we make no warranties of any kind, either implied or express, and exclude all liability for any loss or damage suffered in connection with the use of features and functions under development, to the maximum extent permitted by law, regardless of whether such loss or damage may have been foreseeable.
- d) We are not responsible for the accessibility, safety, accuracy, availability, legality, or completeness of information, advertising, commercial offers, products, services, and materials on third-party websites and third-party resources.

Copyright © Quectel Wireless Solutions Co., Ltd. 2023. All rights reserved.

About the Document

Revision History

Version	Date	Author	Description
-	2023-03-03	Lex LI/Joe MA	Creation of the document
1.0	2023-05-12	Lex LI/Olina CAO/ Barry DENG/Pearl GUO	First official release

Contents

About the Document.....	3
Contents	4
Table Index.....	5
Figure Index	6
1 Introduction	7
1.1. Special Mark.....	7
1.2. Applicable Modules	8
2 General Description	9
2.1. Product Description	9
2.1.1. General Information	11
2.2. Feature Overview	12
3 Pin Definition	15
3.1. Pin Assignment.....	15
3.2. Pin Comparison	19
4 Hardware Interface Design	25
4.1. Power Supply	25
4.2. Turn On/Off	27
4.2.1. Turn On	27
4.2.2. Turn Off	31
4.2.2.1. Turn Off with PWRKEY.....	31
4.2.2.2. Turn Off with AT Command.....	31
4.3. Reset	32
4.4. (U)SIM Interface(s).....	34
4.5. USB Interface	35
4.6. PCM and I2C Interfaces	37
4.7. UART Interfaces	37
4.8. ADC Interfaces	38
4.9. Antenna Interfaces	38
5 Recommended Footprint	42
5.1. Recommended Compatible Footprint	42
5.2. Installation Sketch Map	44
6 Appendix References	45

Table Index

Table 1: Special Mark.....	7
Table 2: Applicable Modules.....	8
Table 3: Supported Networks of the Modules	10
Table 4: Supported Functions of the Modules	10
Table 5: General Information.....	11
Table 6: Feature Overview	12
Table 7: I/O Parameter Definition.....	18
Table 8: Pin Comparison	19
Table 9: Pin Difference of VBAT_BB & VBAT_RF	25
Table 10: Power-up Timing.....	30
Table 11: Power-down Timing with PWRKEY	31
Table 12: Reset Timing.....	33
Table 13: Pin Difference of (U)SIM Interfaces.....	34
Table 14: Data Rate and Function of USB Interface.....	35
Table 15: Pin Difference of USB_VBUS.....	36
Table 16: Pin Difference of UART Interfaces	37
Table 17: Pin Difference of ADC Interfaces.....	38
Table 18: Pin Definition of BG95 Series Antenna Interfaces	39
Table 19: Pin Definition of BG96 Antenna Interfaces.....	39
Table 20: Pin Definition of EG9x Family Antenna Interface	39
Table 21: Pin Definition of EG915Q-NA Antenna Interface.....	39
Table 22: Related Documents	45
Table 23: Terms and Abbreviations	45

Figure Index

Figure 1: Pin Assignment of BG95 Series & BG96 & EG9x Family (Top View)	15
Figure 2: Pin Assignment of EG915Q-NA (Top View).....	16
Figure 3: Power Supply in Star Structure (BG95 Series)	26
Figure 4: Power Supply in Star Structure (BG96 & EG915Q-NA).....	26
Figure 5: Power Supply in Star Structure (EG9x Family)	27
Figure 6: Turn On the Modules with a Driving Circuit	27
Figure 7: Turn On the Modules with a Button	28
Figure 8: Power-up Timing (BG95 Series).....	28
Figure 9: Power-up Timing (BG96)	29
Figure 10: Power-up Timing (EG9x Family).....	29
Figure 11: Power-up Timing (EG915Q-NA)	30
Figure 12: Power-down Timing	31
Figure 13: Reference Design of RESET_N with a Driving Circuit	32
Figure 14: Reference Circuit of RESET_N by Using Button.....	32
Figure 15: Reset Timing (BG9x & EG9x Families)	33
Figure 16: Reset Timing (EG915Q-NA)	33
Figure 17: Reference Design of USB Interface (BG95 Series)	36
Figure 18: Reference Design of USB Interface (BG96 & EG9x Family & EG915Q-NA)	36
Figure 19: PCM and I2C Application with Audio Codec (BG9x & EG9x Families & EG915Q-NA)	37
Figure 20: Main Antenna Interfaces (BG9x Family & EG915Q-NA).....	40
Figure 21: Main and Rx-diversity Antenna Interfaces (EG9x Family).....	40
Figure 22: Wi-Fi Antenna Interface (BG95 Series)	41
Figure 23: GNSS Antenna Interface (EG9x and BG9x Families)	41
Figure 24: Bottom Views of BG9x & EG9x Families & EG915Q-NA.....	42
Figure 25: Recommended Compatible Footprint of BG9x & EG9x Families & EG915Q-NA	43
Figure 26: Installation Sketch Map for BG9x & EG9x Families & EG915Q-NA	44

1 Introduction

Quectel LTE Standard EG9x family (EG91 series and EG95 series) and EG915Q-NA are compatible with LPWA BG9x family (BG95 series and BG96). This document briefly describes the compatible design among these modules.

NOTE

Words marked in **blue** hereinafter indicate the differences between BG9x family, EG9x family and EG915Q-NA, unless otherwise specified.

1.1. Special Mark

Table 1: Special Mark

Mark	Definition
*	Unless otherwise specified, when an asterisk (*) is used after a function, feature, interface, pin name, AT command, or argument, it indicates that the function, feature, interface, pin, AT command, or argument is under development and currently not supported; and the asterisk (*) after a model indicates that the sample of the model is currently unavailable.

1.2. Applicable Modules

Table 2: Applicable Modules

Product Line	Module Family	Module Series	Model
LTE Standard	-	-	EG915Q-NA
	EG9x	EG91	EG91-AUX/-E/-EX/-JP/-NA/-NAX/-NAXD/-VX
		EG95	EG95-AUX/-E/-EX/-JP/-NA/-NAX/-NAXD
LPWA	BG9x	BG95	BG95-M1/-M2/-M3/-M4/-M5/-M6/-MF/-M8/-M9
		-	BG96

2 General Description

2.1. Product Description

BG95 is a series of embedded IoT (LTE Cat M1, LTE Cat NB2 ¹ and EGPRS) wireless communication modules. It supports data connectivity on LTE HD-FDD, EDGE and GPRS/EGPRS networks. It also provides GNSS and voice ² functionalities to meet your specific application demands.

BG96 is an embedded LPWA (LTE Cat M1, LTE Cat NB1, EGPRS) wireless communication module. It supports data connectivity on LTE HD-FDD, EDGE, and GPRS/EGPRS networks, and half-duplex operation in LTE networks. It also features GNSS ³ and voice ⁴ functionalities to meet your specific application demands.

EG91 series and EG95 series modules are embedded 4G wireless communication modules with Rx-diversity, supporting LTE, WCDMA, GSM wireless communication, and providing data connectivity on LTE-FDD, LTE-TDD, DC-HSDPA, HSPA+, HSDPA, HSUPA, WCDMA, EDGE and GPRS networks. They can also provide GNSS ³ and voice ⁵ functionalities.

EG915Q-NA is an LTE Standard wireless communication module. It provides data connectivity on LTE-FDD network. It also provides Wi-Fi scan ⁶ for your specific applications.

NOTE

For detailed information on the supported networks of the applicable modules, see **Table 3**.

¹ LTE Cat NB2 is backward compatible with LTE Cat NB1.

² BG95 series module supports VoLTE (Voice over LTE) under LTE Cat M1, but this function in BG95-MF/-M8/-M9 is under development. In addition, BG95-M3/-M5 modules support CS voice under GSM.

³ For EG9x family and BG96 GNSS function is optional.

⁴ BG96 supports VoLTE under LTE Cat M1 network.

⁵ EG9x family modules contain the **Data + Voice** version and the **Data-only** version.

⁶ EG915Q-NA supports Wi-Fi scan function. Wi-Fi scan and LTE network cannot be used simultaneously since they share the same antenna interface.

Table 3: Supported Networks of the Modules

Module	LTE-FDD	LTE-TDD	WCDMA	EDGE	GPRS/EGPRS
BG95 series	LTE-HD-FDD	-	-	Supported on BG95-M3/-M5/-M8	Supported on BG95-M3/-M5/-M8
BG96	LTE-HD-FDD	-	-	√	√
EG91 series	√	-	Supported on EG9x-AUX/-E/-EX/-NA/-NAX/-NAXD	Supported on EG9x-AUX/-E/-EX	Supported on EG9x-AUX/-E/-EX
EG95 series	√	Supported on EG95-JP			
EG915Q-NA	√	-	-	-	-

Table 4: Supported Functions of the Modules






Module	Voice Functionality	Wi-Fi Scan	GNSS
BG95 series	√	Supported on BG95-MF	√
BG96	√	-	○
EG9x family	○	-	○
EG915Q-NA	-	√	○

NOTE

1. “√” means supported.
2. “-” means not supported.
3. “○” means optional.
4. GNSS function for EG915Q-NA is still under development.

2.1.1. General Information

Table 5: General Information

Module	Appearance	Packaging	Dimensions (mm)	Description
BG95 series		102 LGA pins	23.6 × 19.9 × 2.2	LPWA module
BG96		102 LGA pins	26.5 × 22.5 × 2.3	LPWA module
EG91 series		106 LGA pins	EG91-E: 29.0 × 25.0 × 2.3 EG91-AUX/-EX/ -JP/-NA/-NAX/ -NAXD/-VX: 29.0 × 25.0 × 2.45	LTE Standard module
EG95 series		106 LGA pins	EG95-E: 29.0 × 25.0 × 2.3 EG95-AUX/-EX/ -JP/-NA/-NAX/ -NAXD: 29.0 × 25.0 × 2.45	LTE Standard module
EG915Q-NA		126 LGA pins	23.6 × 19.9 × 2.4	LTE Standard module

2.2. Feature Overview

The key features are compared in the table below.

Table 6: Feature Overview

Feature	BG95 Series	BG96	EG91 Series	EG95 Series	EG915Q-NA
Power Supply	BG95-M1/-M2: <ul style="list-style-type: none">Supply voltage⁷: 2.6–4.8 VTypical supply voltage: 3.3 V BG95-M3/-M5/-M6/-MF/-M8: <ul style="list-style-type: none">Supply voltage: 3.3–4.3 VTypical supply voltage: 3.8 V BG95-M4/-M9: <ul style="list-style-type: none">Supply voltage: 3.2–4.2 VTypical supply voltage: 3.8 V	<ul style="list-style-type: none">Supply voltage: 3.3–4.3 VTypical supply voltage: 3.8 V	<ul style="list-style-type: none">Supply voltage: 3.3–4.3 VTypical supply voltage: 3.8 V	<ul style="list-style-type: none">Supply voltage: 3.3–4.3 VTypical supply voltage: 3.8 V	<ul style="list-style-type: none">Supply voltage: 3.3–4.3 VTypical supply voltage: 3.8 V
Peak Current	VBAT_BB: Max. 0.6 A VBAT_RF: Max. 2.7 A	VBAT_BB: Max. 0.5 A VBAT_RF: Max. 2.0 A	VBAT_BB: Max. 0.8 A VBAT_RF: Max. 1.8 A	VBAT_BB: Max. 0.8 A VBAT_RF: Max. 1.8 A	VBAT_BB: TBD VBAT_RF: TBD
Sleep Current	LTE Cat M1 @ DRX = 1.28 s: 1.7 mA @ BG95-M1 1.68 mA @ BG95-M2 1.89 mA @ BG95-M3 1.53 mA @ BG95-M4 1.56 mA @ BG95-M5 1.42 mA @ BG95-M6 1.59 mA @ BG95-MF 1.56 mA @ BG95-M8 1.37 mA @ BG95-M9 LTE Cat NB1 @ DRX = 1.28 s: 1.55 mA @ BG95-M2 1.49 mA @ BG95-M3 1.39 mA @ BG95-M4 1.43 mA @ BG95-M5 1.31 mA @ BG95-M6 1.43 mA @ BG95-MF 1.51 mA @ BG95-M8	LTE Cat M1 @ DRX = 1.28 s: 1.54 mA LTE Cat NB1 @ DRX = 1.28 s: 2.03 mA	WCDMA PF = 64 (USB disconnected): 1.8 mA @ EG91-AUX/-EX 1.7 mA @ EG91-E 2.2 mA @ EG91-NA 2.1 mA @ EG91-NAX/-NAXD LTE PF = 64 (USB disconnected): 2.3 mA @ EG91-AUX/-EX 2.1 mA @ EG91-E 1.9 mA @ EG91-JP 2.6 mA @ EG91-NA/-NAX/-NAXD 2.4 mA @ EG91-VX	WCDMA PF = 64 (USB disconnected): 1.7 mA @ EG95-AUX 1.8 mA @ EG95-E/-EX 2.2 mA @ EG95-NA 2.0 mA @ EG95-NAX/-NAXD LTE PF = 64 (USB disconnected): 2.2 mA @ EG95-AUX 2.3 mA @ EG95-E/-EX 2.0 mA @ EG95-JP 2.6 mA @ EG95-NA/-NAX/-NAXD	LTE PF = 64 (USB disconnected): 0.68 mA

⁷ For every VBAT transition/re-insertion from 0 V, the minimum power supply voltage should be higher than 2.7 V. After the module starts up normally, the minimum safety voltage is 2.6 V. To ensure full functionality mode, the minimum power supply voltage should be higher than 2.8 V.

	1.36 mA @ BG95-M9				
Temperature Range	<ul style="list-style-type: none"> Operating temperature range ⁸: -35 to +75 °C Extended temperature range ⁹: -40 to +85 °C Storage temperature range: -40 to +90 °C 	<ul style="list-style-type: none"> Operating temperature range ⁸: -35 to +75 °C Extended temperature range ⁹: -40 to +85 °C Storage temperature range: -40 to +90 °C 	<ul style="list-style-type: none"> Operating temperature range ⁸: -35 °C to +75 °C Extended temperature range ⁹: -40 °C to +85 °C Storage temperature range: -40 °C to +90 °C 	<ul style="list-style-type: none"> Operating temperature range ⁸: -35 °C to +75 °C Extended temperature range ⁹: -40 °C to +85 °C Storage temperature range: -40 °C to +90 °C 	<ul style="list-style-type: none"> Operating temperature range ⁸: -35 °C to +75 °C Extended temperature range ⁹: -40 °C to +85 °C Storage temperature range: -40 °C to +90 °C
UART Interfaces	Main UART: <ul style="list-style-type: none"> Used for data transmission and AT command communication. Baud rate: 115200 bps by default. Default frame format: 8N1 (8 data bits, no parity, 1 stop bit). RTS and CTS hardware flow control. Debug UART: <ul style="list-style-type: none"> Used for software debugging and log output. Baud rate: fixed at 115200 bps. GNSS UART: <ul style="list-style-type: none"> Used for GNSS data and GNSS NMEA sentence output. Baud rate: 115200 bps by default. 	UART1: <ul style="list-style-type: none"> Used for data transmission and AT command communication. Baud rate: 115200 bps by default. Default frame format: 8N1 (8 data bits, no parity, 1 stop bit). RTS and CTS hardware flow control. UART2: <ul style="list-style-type: none"> Used for software debugging and log output. Baud rate: 115200 bps. UART3: <ul style="list-style-type: none"> Used for GNSS data or GNSS NMEA sentence output. Baud rate: 115200 bps. 	Main UART: <ul style="list-style-type: none"> Used for data transmission and AT command communication. Baud rate: up to 921600 bps, 115200 bps by default. RTS and CTS hardware flow control. Debug UART: <ul style="list-style-type: none"> Used for Linux console and log output. Baud rate: 115200 bps. 	Main UART: <ul style="list-style-type: none"> Used for data transmission and AT command communication. Baud rate: up to 921600 bps, 115200 bps by default. RTS and CTS hardware flow control. Debug UART: <ul style="list-style-type: none"> Used for Linux console and log output. Baud rate: 115200 bps. 	Main UART: <ul style="list-style-type: none"> Used for data transmission and AT command communication. Baud rate: 115200 bps by default. RTS and CTS hardware flow control. Debug UART: <ul style="list-style-type: none"> Used for partial log output. Baud rate: up to 3 Mbps, 115200 bps by default.
USB Interface	<ul style="list-style-type: none"> Compliant with USB 2.0 specification (slave only). Data transfer rate: up to 480 Mbps. Supports high-speed, low-speed and full-speed modes. Used for AT command communication, data transmission, GNSS NMEA sentence output, software debugging and firmware upgrade. Supports USB serial drivers for Windows 7/8/8.1/10/11, Linux 2.6–5.18, Android 4.x–12.x. 	<ul style="list-style-type: none"> Compliant with USB 2.0 specification (slave only). Data transfer rate: up to 480 Mbps. Supports high-speed and full-speed modes. Used for AT command communication, data transmission, GNSS NMEA sentence output, software debugging and firmware upgrade. Supports USB serial drivers for Windows 7/8/8.1/10/11, Linux 2.6–5.18, Android 4.x–12.x. 	<ul style="list-style-type: none"> Compliant with USB 2.0 specification (slave only). Data transfer rate: up to 480 Mbps. Supports high-speed and full-speed modes. Used for AT command communication, data transmission, GNSS NMEA sentence output, software debugging, firmware upgrade and voice over USB. Supports USB serial drivers for Windows 7/8/8.1/10/11, Linux 2.6–5.18, Android 4.x–12.x. 	<ul style="list-style-type: none"> Compliant with USB 2.0 specification (slave only). Data transfer rate: up to 480 Mbps. Supports high-speed and full-speed modes. Used for AT command communication, data transmission, GNSS NMEA sentence output, software debugging, firmware upgrade and voice over USB. Supports USB serial drivers for Windows 7/8/8.1/10/11, Linux 2.6–5.18, Android 4.x–12.x. 	<ul style="list-style-type: none"> Compliant with USB 2.0 specification (slave only). Data transfer rate: up to 480 Mbps. Supports high-speed and full-speed modes. Used for AT command communication, data transmission, software debugging, firmware upgrade and partial log output. Supports USB serial drivers for Windows 7/8/8.1/10/11, Linux 2.6–5.18*, Android 4.x–12.x*.
Digital Audio Interface	PCM interface ¹⁰ for VoLTE or GSM CS voice	PCM interface for VoLTE only	PCM interface	PCM interface	PCM interface*

⁸ Within the operating temperature range, the module meets 3GPP specifications.

⁹ Within the extended temperature range, the module remains the ability to establish and maintain functions such as voice (The voice function is only supported for BG95 series, BG96 and EG9x family, and is under development for BG95-MF/-M8/-M9), SMS, data transmission, emergency call (only for BG96), etc., without any unrecoverable malfunction. Radio spectrum and radio network are not influenced, while one or more specifications, such as P_{out}, may exceed the specified tolerances of 3GPP. When the temperature returns to the operating temperature range, the module meets 3GPP specifications again.

¹⁰ The VoLTE function of the PCM and I2C interfaces is under development for BG95-MF/-M8/-M9.

I2C Interface	I2C interface for VoLTE or GSM CS voice	I2C interface for VoLTE only	I2C interface	I2C interface	I2C interface*
(U)SIM Interface	Supported	Supported	Supported	Supported	Supported
Wi-Fi Scan	2.4 GHz (BG95-MF only)	-	-	-	2.4 GHz
Firmware Upgrade	<ul style="list-style-type: none">● USB interface● DFOTA	<ul style="list-style-type: none">● USB interface● DFOTA	<ul style="list-style-type: none">● USB interface● DFOTA	<ul style="list-style-type: none">● USB interface● DFOTA	<ul style="list-style-type: none">● USB interface● DFOTA

3 Pin Definition

3.1. Pin Assignment

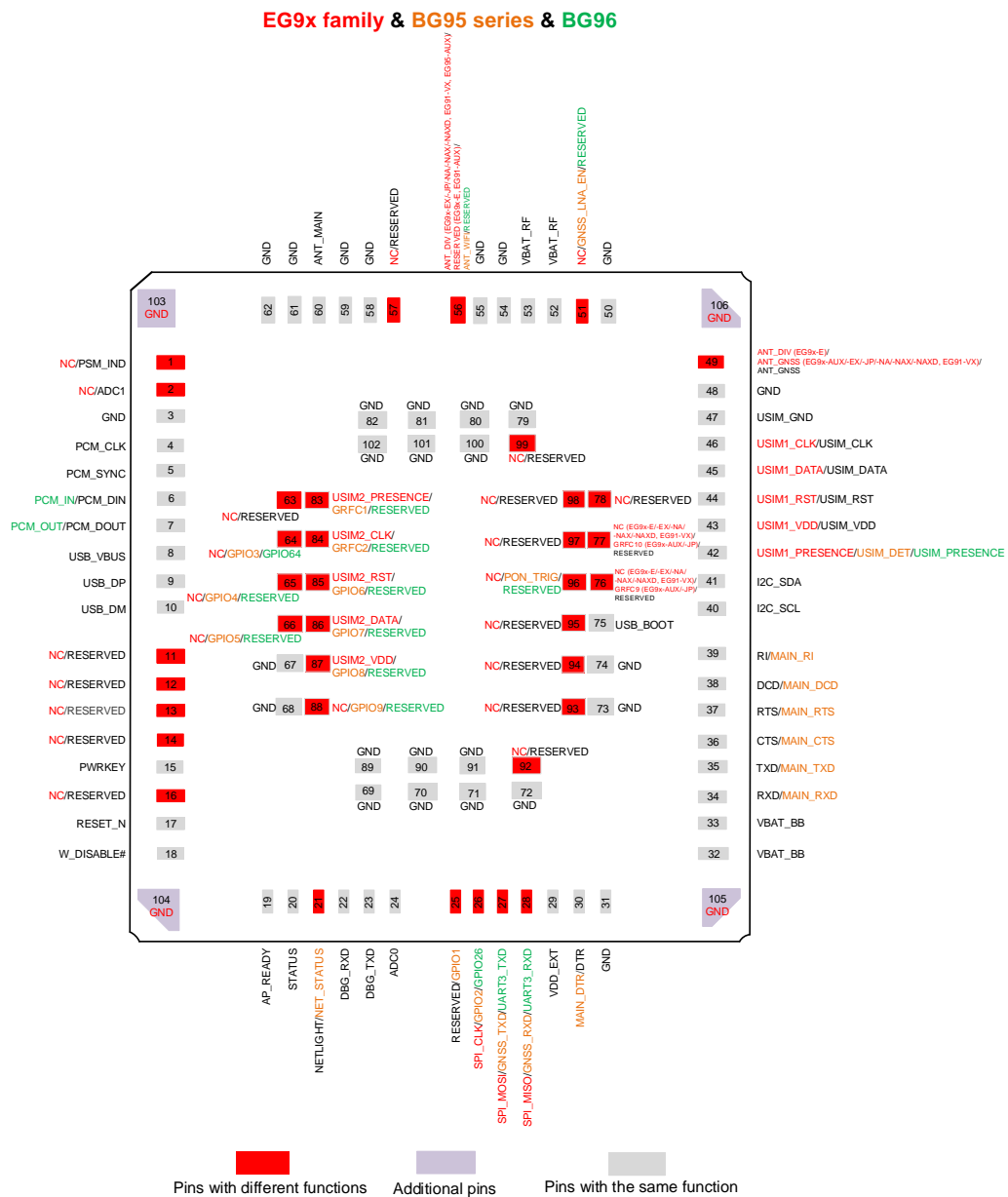


Figure 1: Pin Assignment of BG95 Series & BG96 & EG9x Family (Top View)

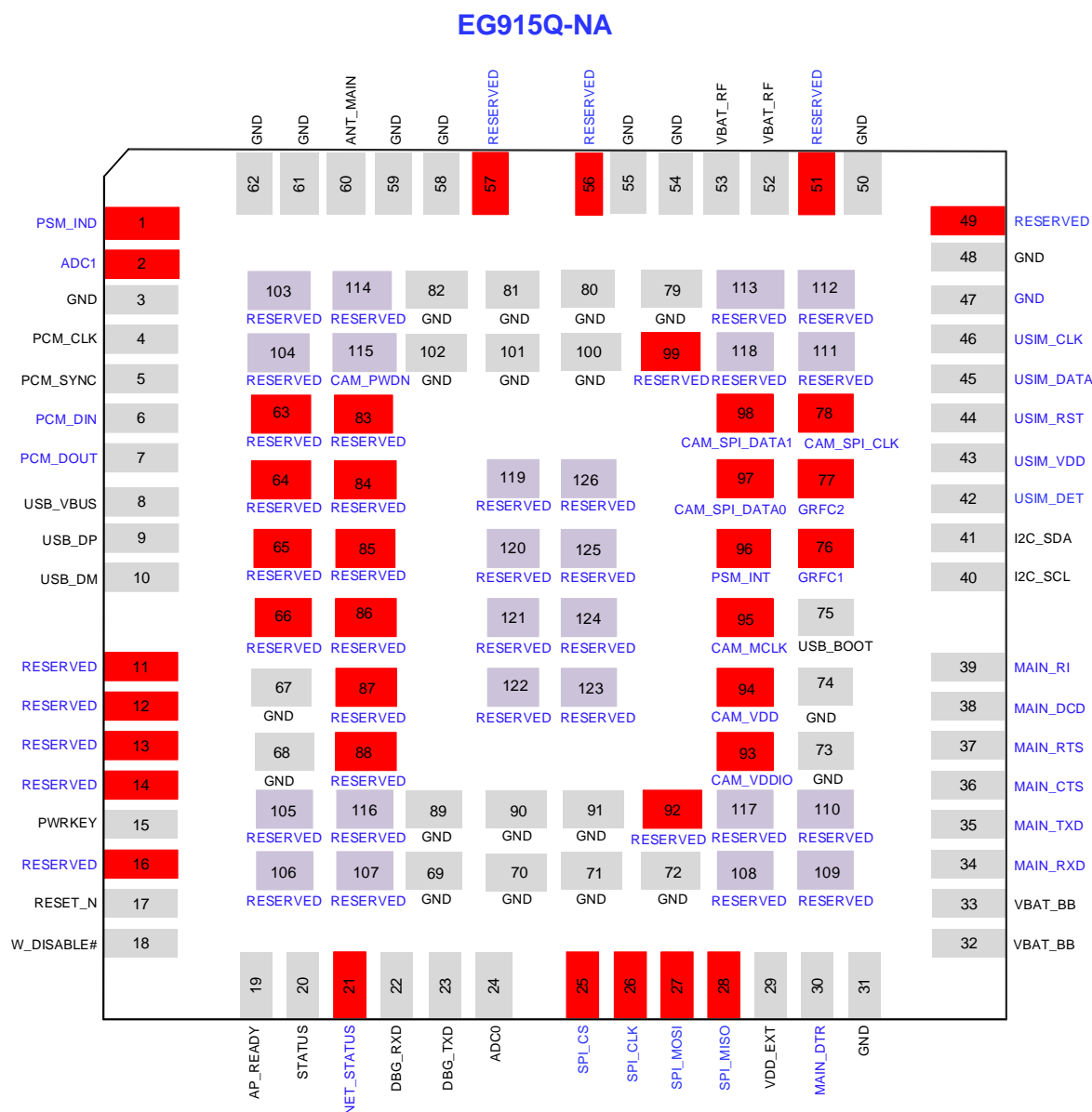


Figure 2: Pin Assignment of EG915Q-NA (Top View)

NOTE

1. Keep all RESERVED, NC and unused pins unconnected.
2. Connect GND pins to the ground in the design.
3. For BG96 and EG9x family, PWRKEY output voltage is 0.8 V because of the diode voltage drop inside the chipset.
4. **BG95 series:**
 - PWRKEY output voltage is 1.5 V because of the voltage drop inside the chipset. Due to platform reasons, the reset function is integrated into PWRKEY on the chipset. Therefore, never pull down PWRKEY to GND permanently.

- Supports ADC0 and ADC1. Do not use ADC0 and ADC1 simultaneously, as ADC1 is directly connected to ADC0 inside the module. If you intend to use the two ADC interfaces at the same time, add an external analog switch.
- **BG95-MF:**
 - Only BG95-MF supports ANT_WIFI (pin 56).
 - Does not support GPIO3 and GPIO4 interfaces (pins 64 and 65).
- Only **BG95-M4/-MF** support GNSS_LNA_EN (pin 51).
- **BG95-M4/-M9** do not support GRFC interfaces (pins 83 and 84).
- GNSS_TXD (pin 27) and GRFC2 (pin 84) and GNSS_LNA_EN (pin 51) are BOOT_CONFIG pins. Never pull them up before startup, otherwise the module cannot power on normally.
- GPIO1 (pin 25) supports fast shutdown function which is disabled by default.
- PCM and I2C interfaces are used for VoLTE or GSM CS voice only.

5. EG9x family:

- Supports Dual SIM Single Standby function.
- BOOT_CONFIG pins (SPI_CLK, USB_BOOT, PCM_CLK, PCM_SYNC) cannot be pulled up before startup.
- **EG91 series:**
 - Pin 49 is defined as ANT_GNSS on EG91-AUX/-EX/-JP/-NA/-NAX/-NAXD/-VX, while it is defined as ANT_DIV on EG91-E.
 - Pin 56 is defined as ANT_DIV on EG91-EX/-JP/-NA/-NAX/-NAXD/-VX, while it is defined as RESERVED on EG91-AUX/-E. Rx-diversity antenna is not supported on EG91-AUX.
 - Pins 76 and 77 are respectively defined as GRFC9 and GRFC10 on EG91-AUX/-JP, while they are defined as NC on EG91-E/-EX/-NA/-NAX/-NAXD/-VX.
- **EG95 series:**
 - Pin 49 is defined as ANT_GNSS on EG95-AUX/-EX/-JP/-NA/-NAX/-NAXD, while it is defined as ANT_DIV on EG95-E.
 - Pin 56 is defined as ANT_DIV on EG95-AUX/-EX/-JP/-NA/-NAX/-NAXD, while it is defined as RESERVED on EG95-E.
 - Pins 76 and 77 are respectively defined as GRFC9 and GRFC10 on EG95-AUX/-JP, while they are defined as NC on EG95-E/-EX/-NA/-NAX/-NAXD.

6. EG915Q-NA:

- If the module does not need to enter emergency download mode, USB_BOOT (pin 75) should not be pulled up to VDD_EXT before the module successfully starts up.
- In sleep mode, some pins of the main UART interface (pins 34–37), debug UART interface (pins 22 and 23), USB_BOOT (pin 75), PCM interface* (pins 4–7), I2C interface* (pins 40 and 41), and SPI interface* (pins 25–28) are powered down. The driving capacity will be lost and status indication and data transmission functions are disabled. Pay attention to it when designing circuits.

Table 7: I/O Parameter Definition

Type	Description
AI	Analog Input
AIO	Analog Input/Output
DI	Digital Input
DIO	Digital Input/Output
DO	Digital Output
OD	Open Drain
PI	Power Input
PO	Power Output

3.2. Pin Comparison

The following table describes the pin functions, I/O and DC characteristics of BG9x family, EG9x family, and EG915Q-NA.

Table 8: Pin Comparison

Pin No.	BG95 Series			BG96			EG9x Family			EG915Q-NA			Description
	Pin Name	I/O	Power Domain	Pin Name	I/O	Power Domain	Pin Name	I/O	Power Domain	Pin Name	I/O	Power Domain	
1	PSM_IND ¹¹	DO	1.8 V	PSM_IND ¹¹	DO	1.8 V	NC	-	-	PSM_IND*	DO	1.8 V	1. Indicate the module's power saving mode. 2. Not connected.
2	ADC1	AI	0.1–1.8 V	ADC1	AI	0.3–1.8 V	NC	-	-	ADC1	AI	0–1.2 V	1. General-purpose ADC interface. 2. Not connected.
3	GND	-	-	GND	-	-	GND	-	-	GND	-	-	Ground.
4	PCM_CLK	DO	1.8 V	PCM_CLK	DO	1.8 V	PCM_CLK	DIO	1.8 V	PCM_CLK*	DO	1.8 V	PCM clock.
5	PCM_SYNC	DO	1.8 V	PCM_SYNC	DO	1.8 V	PCM_SYNC	DIO	1.8 V	PCM_SYNC*	DO	1.8 V	PCM data frame sync.
6	PCM_DIN	DI	1.8 V	PCM_IN	DI	1.8 V	PCM_DIN	DI	1.8 V	PCM_DIN*	DI	1.8 V	PCM data input.
7	PCM_DOUT	DO	1.8 V	PCM_OUT	DO	1.8 V	PCM_DOUT	DO	1.8 V	PCM_DOUT*	DO	1.8 V	PCM data output.
8	USB_VBUS	AI	4.0–5.25 V	USB_VBUS	AI	3.0–5.25 V	USB_VBUS	AI	3.0–5.25 V	USB_VBUS	AI	3.0–5.25 V	USB connection detect.
9	USB_DP	AIO	-	USB_DP	AIO	-	USB_DP	AIO	-	USB_DP	AIO	-	USB differential data (+).
10	USB_DM	AIO	-	USB_DM	AIO	-	USB_DM	AIO	-	USB_DM	AIO	-	USB differential data (-).
11	RESERVED	-	-	RESERVED	-	-	NC	-	-	RESERVED	-	-	1. Reserved. 2. Not connected.
12	RESERVED	-	-	RESERVED	-	-	NC	-	-	RESERVED	-	-	1. Reserved. 2. Not connected.
13	RESERVED	-	-	RESERVED	-	-	NC	-	-	RESERVED	-	-	1. Reserved. 2. Not connected.
14	RESERVED	-	-	RESERVED	-	-	NC	-	-	RESERVED	-	-	1. Reserved. 2. Not connected.
15	PWRKEY ¹²	DI	-	PWRKEY ¹³	DI	-	PWRKEY ¹³	DI	-	PWRKEY	DI	-	Turn on/off the module.

¹¹ When PSM is enabled, the function of PSM_IND pin will be activated after the module is rebooted. When PSM_IND is in high voltage level, the module is in full functionality mode. When it is in low voltage level, the module is in PSM.

¹² For BG95 series, PWRKEY output voltage is 1.5 V because of the voltage drop inside the chipset. Due to platform reasons, the chipset has integrated the reset function into PWRKEY. Therefore, never pull down PWRKEY to GND permanently.

¹³ For BG96 and EG9x family, PWRKEY output voltage is 0.8 V because of the diode voltage drop inside the chipset.

16	RESERVED	-	-	RESERVED	-	-	NC	-	-	RESERVED	-	-	1. Reserved. 2. Not connected.
17	RESET_N	DI	1.5 V	RESET_N	DI	1.8 V	RESET_N	DI	1.8 V	RESET_N	DI	-	Reset the module.
18	W_DISABLE#	DI	1.8 V	W_DISABLE#	DI	1.8 V	W_DISABLE#	DI	1.8 V	W_DISABLE#*	DI	1.8 V	Airplane mode control.
19	AP_READY	DI	1.8 V	AP_READY	DI	1.8 V	AP_READY	DI	1.8 V	AP_READY*	DI	1.8 V	Application processor ready.
20	STATUS	DO	1.8 V	STATUS	DO	1.8 V	STATUS	DO	1.8 V	STATUS	DO	1.8 V	Indicate the module's operation status.
21	NET_STATUS	DO	1.8 V	NETLIGHT	DO	1.8 V	NETLIGHT	DO	1.8 V	NET_STATUS	DO	1.8 V	Indicate the module's network activity status.
22	DBG_RXD	DI	1.8 V	DBG_RXD	DI	1.8 V	DBG_RXD	DI	1.8 V	DBG_RXD	DI	1.8 V	Debug UART receive.
23	DBG_TXD	DO	1.8 V	DBG_TXD	DO	1.8 V	DBG_TXD	DO	1.8 V	DBG_TXD	DO	1.8 V	Debug UART transmit.
24	ADC0	AI	0.1–1.8 V	ADC0	AI	0.3–1.8 V	ADC0	AI	0.3 V– VBAT_BB	ADC0	AI	0–1.2 V	General-purpose ADC interface.
25	GPIO1 ¹⁴	DIO	1.8 V	RESERVED	-	-	RESERVED	-	-	SPI_CS*	DO	1.8 V	1. General-purpose input/output. 2. Reserved. 3. SPI chip select.
26	GPIO2	DIO	1.8 V	GPIO26	DIO	1.8 V	SPI_CLK	DO	1.8 V	SPI_CLK*	DO	1.8 V	1. General-purpose input/output. 2. SPI clock.
27	GNSS_TXD	DO	1.8 V	UART3_TXD	DO	1.8 V	SPI_MOSI	DO	1.8 V	SPI_MOSI*	DO	1.8 V	1. GNSS UART transmit. 2. UART3 transmit. 3. SPI master-out slave-in.
28	GNSS_RXD	DI	1.8 V	UART3_RXD	DI	1.8 V	SPI_MISO	DI	1.8 V	SP1_MISO*	DI	1.8 V	1. GNSS UART receive. 2. UART3 receive. 3. SPI master-in slave-out.
29	VDD_EXT	PO	1.8 V	VDD_EXT	PO	1.8 V	VDD_EXT	PO	1.8 V	VDD_EXT	PO	1.8 V	Provide 1.8 V for external circuit.
30	MAIN_DTR	DI	1.8 V	DTR	DI	1.8 V	DTR	DI	1.8 V	MAIN_DTR	DI	1.8 V	(Main) UART data terminal ready.
31	GND	-	-	GND	-	-	GND	-	-	GND	-	-	Ground.
32, 33	VBAT_BB	PI	See Table 6	VBAT_BB	PI	3.3–4.3 V	VBAT_BB	PI	3.3–4.3 V	VBAT_BB	PI	3.3–4.3 V	Power supply for the module's BB part.
34	MAIN_RXD	DI	1.8 V	RXD	DI	1.8 V	RXD	DI	1.8 V	MAIN_RXD	DI	1.8 V	(Main) UART receive.
35	MAIN_TXD	DO	1.8 V	TXD	DO	1.8 V	TXD	DO	1.8 V	MAIN_TXD	DO	1.8 V	(Main) UART transmit.
36	MAIN_CTS	DO	1.8 V	CTS	DO	1.8 V	CTS	DO	1.8 V	MAIN_CTS	DO	1.8 V	DTE clear to send signal from DCE (connect to DTE's CTS).
37	MAIN_RTS	DI	1.8 V	RTS	DI	1.8 V	RTS	DI	1.8 V	MAIN_RTS	DI	1.8 V	DTE request to send signal to DCE (connect to DTE's RTS).
38	MAIN_DCD	DO	1.8 V	DCD	DO	1.8 V	DCD	DO	1.8 V	MAIN_DCD	DO	1.8 V	(Main) UART data carrier detect.

¹⁴ Pin 25 is a general-purpose IO by default. It can be multiplexed into fast shutdown interface with **AT+QCFG="fast/poweroff"**. For details of the command, see **document [1]**.

39	MAIN_RI	DO	1.8 V	RI	DO	1.8 V	RI	DO	1.8 V	MAIN_RI	DO	1.8 V	(Main) UART ring indication.
40	I2C_SCL	OD	1.8 V only	I2C_SCL	OD	1.8 V only	I2C_SCL	OD	1.8 V	I2C_SCL*	OD	1.8 V	I2C serial clock (for external codec).
41	I2C_SDA	OD	1.8 V only	I2C_SDA	OD	1.8 V only	I2C_SDA	OD	1.8 V	I2C_SDA*	OD	1.8 V	I2C serial data (for external codec).
42	USIM_DET	DI	1.8 V	USIM_PRESENCE	DI	1.8 V	USIM1_PRESENCE	DI	1.8 V	USIM_DET	DI	1.8 V	(U)SIM card hot-plug detect.
43	USIM_VDD	PO	1.8 V	USIM_VDD	PO	1.8/3.0 V	USIM1_VDD	PO	1.8/3.0 V	USIM_VDD	PO	1.8/3.0 V	(U)SIM card power supply.
44	USIM_RST	DO	1.8 V	USIM_RST	DO	1.8/3.0 V	USIM1_RST	DO	1.8/3.0 V	USIM_RST	DO	1.8/3.0 V	(U)SIM card reset.
45	USIM_DATA	DIO	1.8 V	USIM_DATA	DIO	1.8/3.0 V	USIM1_DATA	DIO	1.8/3.0 V	USIM_DATA	DIO	1.8/3.0 V	(U)SIM card data.
46	USIM_CLK	DO	1.8 V	USIM_CLK	DO	1.8/3.0 V	USIM1_CLK	DO	1.8/3.0 V	USIM_CLK	DO	1.8/3.0 V	(U)SIM card clock.
47	USIM_GND	-	-	USIM_GND	-	-	USIM_GND	-	-	GND	-	-	1. Specified ground for (U)SIM card. 2. Ground.
48	GND	-	-	GND	-	-	GND	-	-	GND	-	-	Ground.
49	ANT_GNSS	AI	-	ANT_GNSS	AI	-	ANT_GNSS/ ANT_DIV ¹⁵	AI	-	RESERVED	-	-	1. GNSS antenna interface. 2. Diversity antenna interface. 3. Reserved.
50	GND	-	-	GND	-	-	GND	-	-	GND	-	-	Ground.
51	GNSS_LNA_EN ¹⁶	DO	-	RESERVED	-	-	NC	-	-	RESERVED	-	-	1. External LNA enable control. 2. Reserved. 3. Not connected.
52, 53	VBAT_RF	PI	See Table 6	VBAT_RF	PI	3.3–4.3 V	VBAT_RF	PI	3.3–4.3 V	VBAT_RF	PI	3.3–4.3 V	Power supply for the module's RF part.
54, 55	GND	-	-	GND	-	-	GND	-	-	GND	-	-	Ground.
56	ANT_WIFI ¹⁷	AI	-	RESERVED	-	-	ANT_DIV/ RESERVED ¹⁸	AI/-	-	RESERVED	-	-	1. Wi-Fi antenna interface. 2. Reserved. 3. Diversity antenna interface.
57	RESERVED	-	-	RESERVED	-	-	NC	-	-	RESERVED	-	-	1. Reserved. 2. Not connected.
58, 59	GND	-	-	GND	-	-	GND	-	-	GND	-	-	Ground.
60	ANT_MAIN	AIO	-	ANT_MAIN	AIO	-	ANT_MAIN	AIO	-	ANT_MAIN	AIO	-	Main antenna interface.
61, 62	GND	-	-	GND	-	-	GND	-	-	GND	-	-	Ground.

¹⁵ For EG91 series, pin 49 is defined as ANT_GNSS on EG91-AUX/-EX/-JP/-NA/-NAX/-NAXD/-VX, while it is defined as ANT_DIV on EG91-E.

For EG95 series, pin 49 is defined as ANT_GNSS on EG95-AUX/-EX/-JP/-NA/-NAX/-NAXD, while it is defined as ANT_DIV on EG95-E.

¹⁶ Only BG95-M4/-MF support GNSS_LNA_EN (pin 51).

¹⁷ Only BG95-MF supports ANT_WIFI (pin 56).

¹⁸ For EG91 series, pin 56 is defined as ANT_DIV on EG91-EX/-JP/-NA/-NAX/-NAXD/-VX, while it is defined as RESERVED on EG91-AUX/-E. Rx-diversity antenna is not supported on EG91-AUX.

For EG95 series, pin 56 is defined as ANT_DIV on EG95-AUX/-EX/-JP/-NA/-NAX/-NAXD, while it is defined as RESERVED on EG95-E.

63	RESERVED	-	-	RESERVED	-	-	NC	-	-	RESERVED	-	-	1. Reserved. 2. Not connected.
64	GPIO3 ¹⁹	DIO	1.8 V	GPIO64	DIO	1.8 V	NC	-	-	RESERVED	-	-	1. General-purpose input/output. 2. Not connected. 3. Reserved.
65	GPIO4 ¹⁹	DIO	1.8 V	RESERVED	-	-	NC	-	-	RESERVED	-	-	1. General-purpose input/output. 2. Reserved. 3. Not connected.
66	GPIO5	DIO	1.8 V	RESERVED	-	-	NC	-	-	RESERVED	-	-	1. General-purpose input/output. 2. Reserved. 3. Not connected.
67–74	GND	-	-	GND	-	-	GND	-	-	GND	-	-	Ground.
75	USB_BOOT	DI	1.8 V	USB_BOOT	DI	1.8 V	USB_BOOT	DI	1.8 V	USB_BOOT	DI	1.8 V	Force the module into emergency download mode.
76	RESERVED	-	-	RESERVED	-	-	GRFC9/NC ²⁰	DO/-	1.8 V	GRFC1*	DO	1.8 V	1. Reserved. 2. Generic RF controller. 3. Not connected.
77	RESERVED	-	-	RESERVED	-	-	GRFC10/NC ²⁰	DO/-	1.8 V	GRFC2*	DO	1.8 V	1. Reserved. 2. Generic RF controller. 3. Not connected.
78	RESERVED	-	-	RESERVED	-	-	NC	-	-	CAM_SPI_CLK*	DI	1.8 V	1. Reserved. 2. Not connected. 3. Camera SPI clock.
79–82	GND	-	-	GND	-	-	GND	-	-	GND	-	-	Ground.
83	GRFC1 ²¹	DO	1.8 V	RESERVED	-	-	USIM2_PRESENCE	DI	1.8 V	RESERVED	-	-	1. Generic RF controller. 2. Reserved. 3. (U)SIM2 card hot-plug detect.
84	GRFC2 ²¹	DO	1.8 V	RESERVED	-	-	USIM2_CLK	DO	1.8/3.0 V	RESERVED	-	-	1. Generic RF controller. 2. Reserved. 3. (U)SIM2 card clock.
85	GPIO6	DIO	1.8 V	RESERVED	-	-	USIM2_RST	DO	1.8/3.0 V	RESERVED	-	-	1. General purpose input/output. 2. Reserved. 3. (U)SIM2 card reset.
86	GPIO7	DIO	1.8 V	RESERVED	-	-	USIM2_DATA	DIO	1.8/3.0 V	RESERVED	-	-	1. General purpose input/output. 2. Reserved. 3. (U)SIM2 card data.
87	GPIO8	DIO	1.8 V	RESERVED	-	-	USIM2_VDD	PO	1.8/3.0 V	RESERVED	-	-	1. General purpose input/output. 2. Reserved. 3. (U)SIM2 card power supply.

¹⁹ BG95-MF does not support GPIO3 and GPIO4 interfaces (pins 64 and 65).²⁰ For EG91 series, pins 76 and 77 are respectively defined as GRFC9 and GRFC10 on EG91-AUX/-JP, while they are defined as NC on EG91-E/-EX/-NA/-NAX/-NAXD/-VX.
For EG95 series, pins 76 and 77 are respectively defined as GRFC9 and GRFC10 on EG95-AUX/-JP, while they are defined as NC on EG95-E/-EX/-NA/-NAX/-NAXD.²¹ BG95-M4/-M9 do not support GRFC interfaces (pins 83 and 84).

88	GPIO9	DIO	1.8 V	RESERVED	-	-	NC	-	-	RESERVED	-	-	1. General purpose input/output. 2. Reserved. 3. Not connected.
89–91	GND	-	-	GND	-	-	GND	-	-	GND	-	-	Ground.
92	RESERVED	-	-	RESERVED	-	-	NC	-	-	RESERVED	-	-	1. Reserved. 2. Not connected.
93	RESERVED	-	-	RESERVED	-	-	NC	-	-	CAM_VDDIO*	PO	1.8 V	1. Reserved. 2. Not connected. 3. Camera digital power supply.
94	RESERVED	-	-	RESERVED	-	-	NC	-	-	CAM_VDD*	PO	2.8 V	1. Reserved. 2. Not connected. 3. Camera analog power supply.
95	RESERVED	-	-	RESERVED	-	-	NC	-	-	CAM_MCLK*	DO	1.8 V	1. Reserved. 2. Not connected. 3. Master clock of the camera.
96	PON_TRIG	DI	1.8 V	RESERVED	-	-	NC	-	-	PSM_INT*	DI	1.8 V	1. Wake up the module from power saving mode. 2. Reserved. 3. Not connected.
97	RESERVED	-	-	RESERVED	-	-	NC	-	-	CAM_SPI_DATA0*	DI	1.8 V	1. Reserved. 2. Not connected. 3. Camera SPI data bit 0.
98	RESERVED	-	-	RESERVED	-	-	NC	-	-	CAM_SPI_DATA1*	DI	1.8 V	1. Reserved. 2. Not connected. 3. Camera SPI data bit 1.
99	RESERVED	-	-	RESERVED	-	-	NC	-	-	RESERVED	-	-	1. Reserved. 2. Not connected.
100–102	GND	-	-	RESERVED	-	-	GND	-	-	GND	-	-	1. Ground. 2. Reserved.
103–106	-	-	-	-	-	-	GND	-	-	RESERVED	-	-	1. Ground. 2. Reserved.
107–114	-	-	-	-	-	-	-	-	-	RESERVED	-	-	Reserved.
115	-	-	-	-	-	-	-	-	-	CAM_PWDN*	DO	1.8 V	Camera power down.
116-126	-	-	-	-	-	-	-	-	-	RESERVED	-	-	Reserved.

NOTE

1. Pins 103–106 in **purple** are additional pins on EG9x family and EG915Q-NA that are not available on BG9x family modules. Pins 107–126 in **purple** are additional pins on EG915Q-NA module that are not available on BG9x family and EG9x family modules.
2. Pins in **blue** are pins with different functions or voltage domain on BG9x family, EG9x family and EG915Q-NA modules, but the module footprint is compatible.
3. Pins in **black** are compatible pins on BG9x family, EG9x family and EG915Q-NA modules with the same functionality.
4. Keep all RESERVED, NC, and unused pins unconnected.
5. All GND pins should be connected to ground.
6. For BG95 series, BOOT_CONFIG pins (GNSS_TXD, GRFC2 and GNSS_LNA_EN) cannot be pulled up before startup, otherwise the module cannot power on normally.
7. For EG9x family, BOOT_CONFIG pins (SPI_CLK, USB_BOOT, PCM_CLK and PCM_SYNC) cannot be pulled up before startup.
8. For EG915Q-NA module, If the module does not need to enter emergency download mode, USB_BOOT (pin 75) should not be pulled up to VDD_EXT before the module successfully starts up.

4 Hardware Interface Design

4.1. Power Supply

Table 9: Pin Difference of VBAT_BB & VBAT_RF

Pin Name	Pin No.	I/O	DC Characteristics			
			BG95 Series	BG96	EG9x Family	EG915Q-NA
VBAT_BB	32, 33	PI	BG95-M1/-M2: Vmax = 4.8 V Vmin = 2.6 V Vnom = 3.3 V			
			BG95-M3/-M5/-M6/-MF/-M8: Vmax = 4.3 V Vmin = 3.3 V Vnom = 3.8 V	Vmax = 4.3 V Vmin = 3.3 V Vnom = 3.8 V	Vmax = 4.3 V Vmin = 3.3 V Vnom = 3.8 V	Vmax = 4.3 V Vmin = 3.3 V Vnom = 3.8 V
			BG95-M4/-M9: Vmax = 4.2 V Vmin = 3.2 V Vnom = 3.8 V	VBAT_BB: Imax = 0.5 A VBAT_RF: Imax = 2.0 A	VBAT_BB: Imax = 0.8 A VBAT_RF: Imax = 1.8 A	VBAT_BB: Imax = TBD VBAT_RF: Imax = TBD
			VBAT_BB: Imax = 0.6 A VBAT_RF: Imax = 2.7 A			
VBAT_RF	52, 53	PI				

NOTE

1. BG9x family are LPWA modules, which require low quiescent and leakage current. For more information about sufficient current for BG9x family, see **documents [2]** and **[3]**.
2. The power supply of EG9x family and EG915Q-NA should be able to provide sufficient current of

at least 2.0 A.

3. See the corresponding reference design documents of the modules for more details about power supply design.

● BG95 series

Use two TVS with low leakage current and suitable reverse standoff voltage to ensure power source stability. It is recommended to place them as close to VBAT pins as possible.

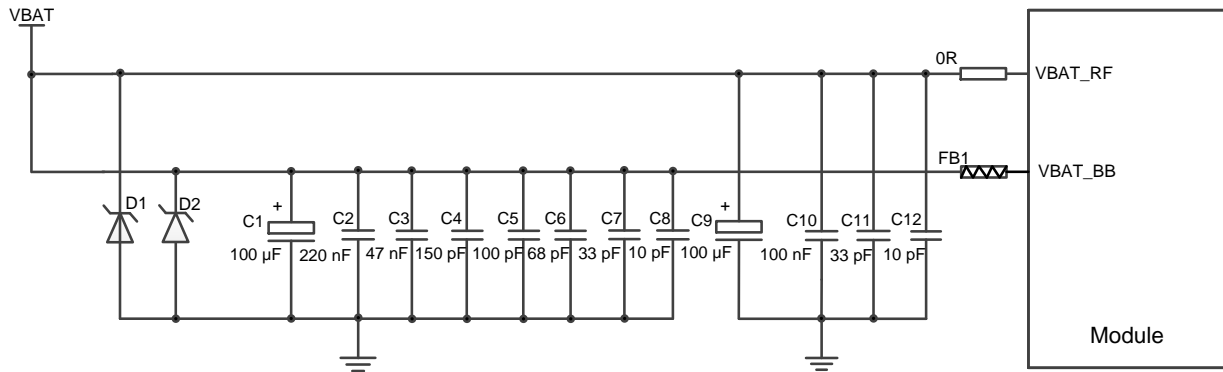


Figure 3: Power Supply in Star Structure (BG95 Series)

● BG96 & EG915Q-NA

Use a TVS with low reverse standoff voltage V_{RWM} (4.7 V), low clamping voltage V_C and high reverse peak pulse current I_{PP} to ensure power source stability. The power supply in star structure is presented in the figure below.

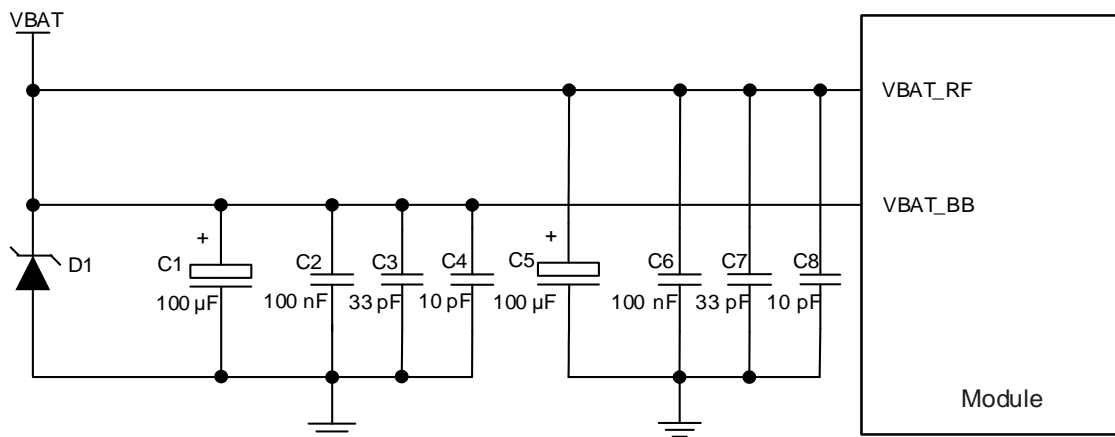


Figure 4: Power Supply in Star Structure (BG96 & EG915Q-NA)

● EG9x Family

To avoid the damage caused by electric surge and ESD, it is suggested that a TVS with recommended low reverse standoff voltage V_{RWM} (4.5 V), low clamping voltage V_C and high reverse peak pulse current I_{PP} should be used. The following figure shows power supply in star structure.

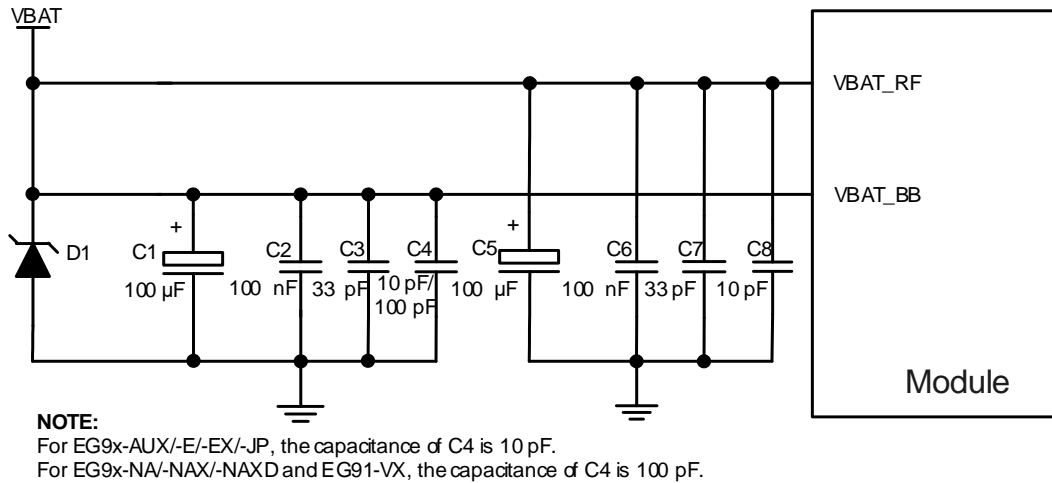


Figure 5: Power Supply in Star Structure (EG9x Family)

4.2. Turn On/Off

The turn-on/off method is the same for BG9x family, EG9x family and EG915Q-NA. The modules can be turned on or turned off after pressing PWRKEY for a certain time.

4.2.1. Turn On

Turn-on circuits of the modules are presented in the figures below.

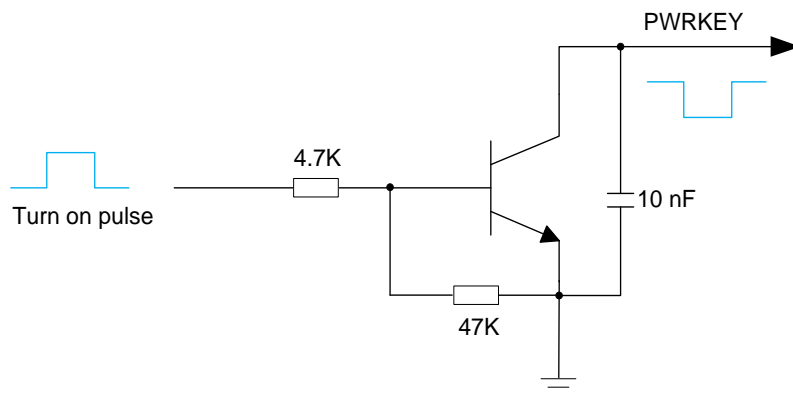


Figure 6: Turn On the Modules with a Driving Circuit

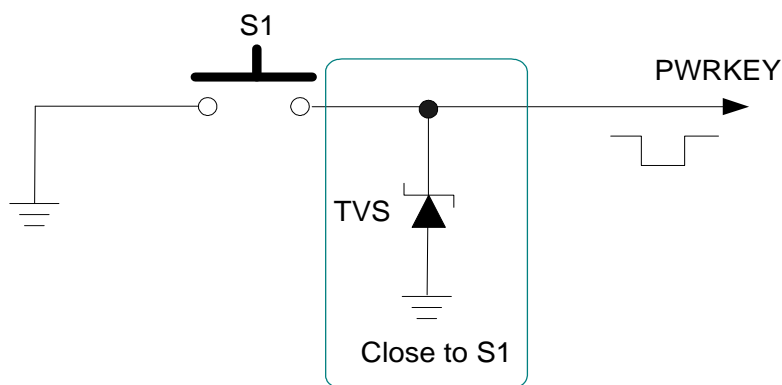


Figure 7: Turn On the Modules with a Button

The power-up timing of the modules is illustrated in the figure below.

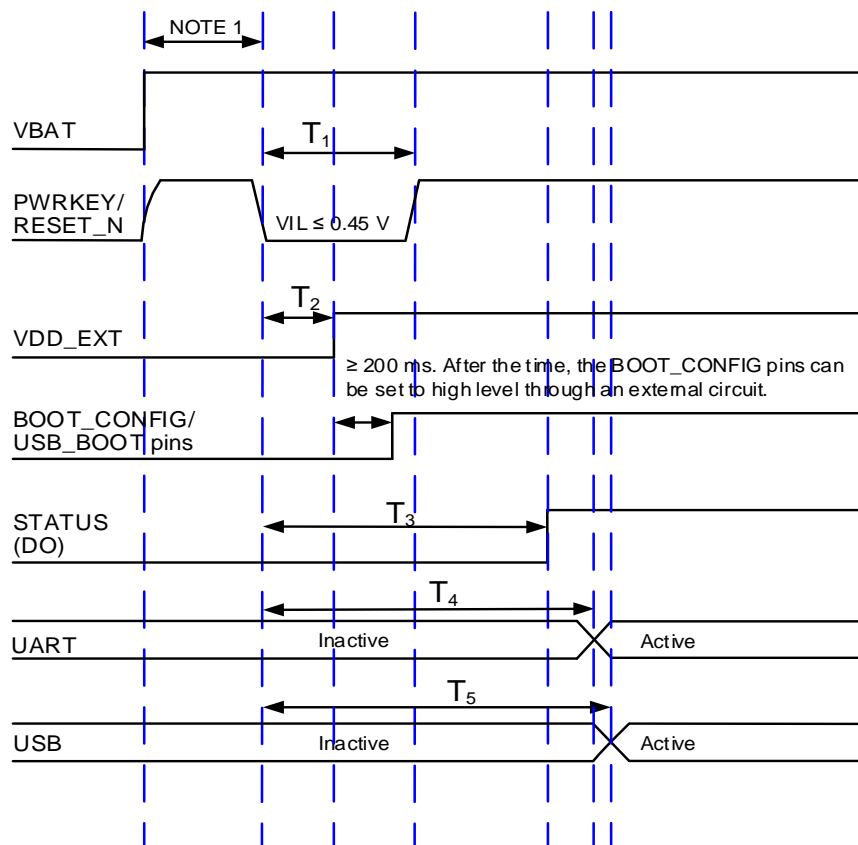


Figure 8: Power-up Timing (BG95 Series)

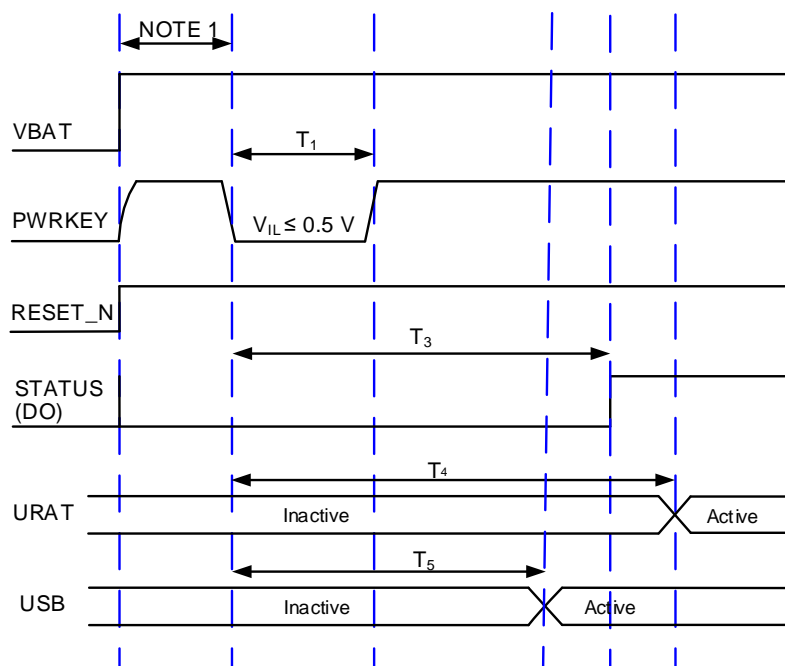


Figure 9: Power-up Timing (BG96)

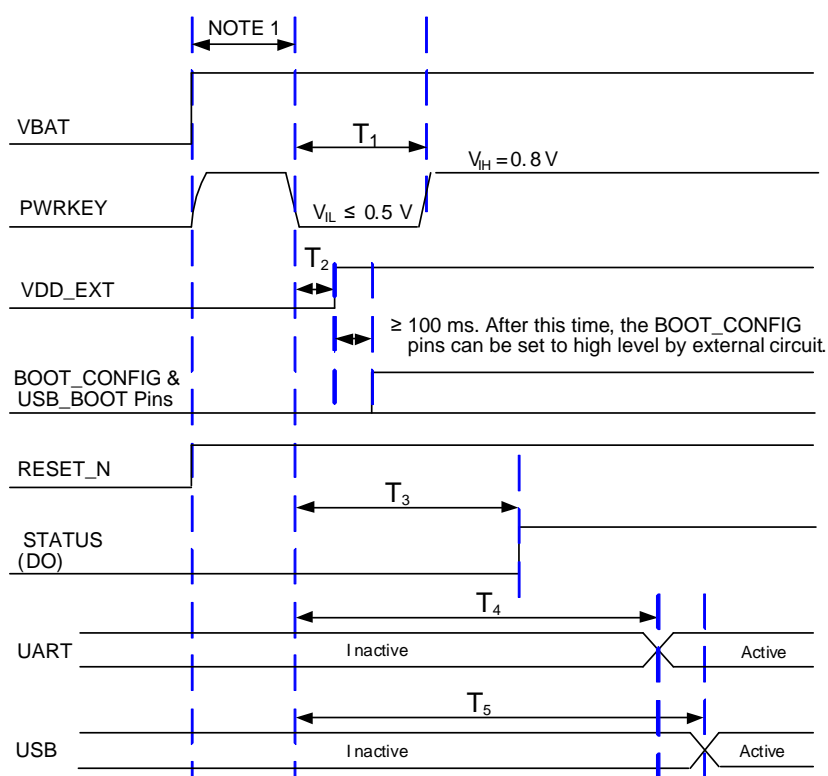


Figure 10: Power-up Timing (EG9x Family)

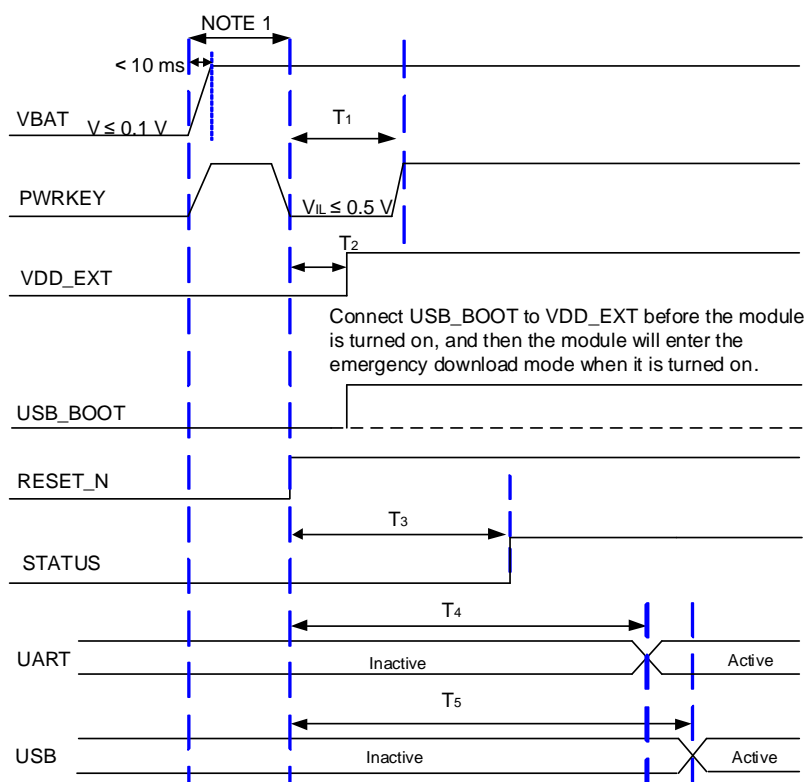


Figure 11: Power-up Timing (EG915Q-NA)

Table 10: Power-up Timing

Module	T_1	T_2	T_3	T_4	T_5
BG95 series	500–1000 ms	About 30 ms	$\geq 2.1 \text{ s}$	$\geq 2.5 \text{ s}$	$\geq 2.55 \text{ s}$
BG96	$\geq 500 \text{ ms}$	-	$\geq 4.8 \text{ s}$	$\geq 4.9 \text{ s}$	$\geq 4.2 \text{ s}$
EG9x family	$\geq 500 \text{ ms}$	About 100 ms	$\geq 10 \text{ s}$	$\geq 12 \text{ s}$	$\geq 13 \text{ s}$
EG915Q-NA	$\geq 500 \text{ ms}$	About 40 ms	$\geq 2 \text{ s}$	$\geq 10 \text{ s}$	$\geq 10 \text{ s}$

NOTE

1. Make sure that VBAT is stable before pulling down PWRKEY. After powering up VBAT, it is recommended to wait at least 30 ms before pulling down PWRKEY pin.
2. BOOT_CONFIG pins on BG95 series and EG9x family cannot be pulled up before startup.
3. PWRKEY can be pulled down directly to GND with a recommended 10 k Ω (for EG9x family) or 4.7 k Ω (for EG915Q-NA) resistor if the modules need to be powered on automatically and shutdown is not needed.

4.2.2. Turn Off

4.2.2.1. Turn Off with PWRKEY

The following is power-down timing for BG9x family, EG9x family and EG915Q-NA.

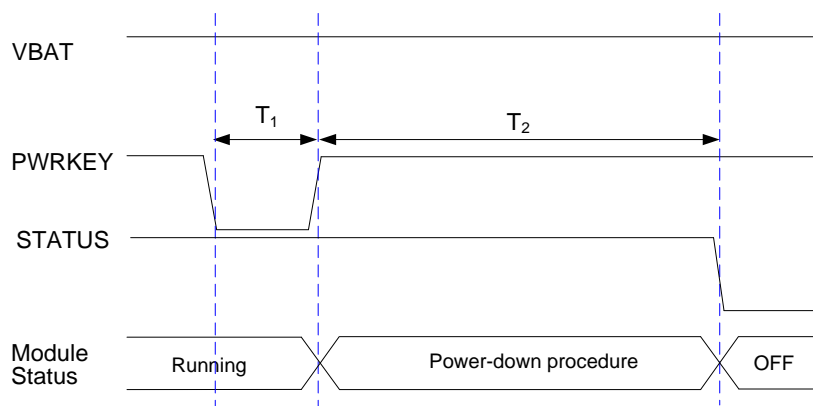


Figure 12: Power-down Timing

Table 11: Power-down Timing with PWRKEY

Module	T_1	T_2
BG95 series	650–1000 ms	≥ 1.3 s
BG96	≥ 650 ms	≥ 2 s
EG9x family	≥ 650 ms	≥ 30 s
EG915Q-NA	≥ 650 ms	≥ 1.35 s

4.2.2.2. Turn Off with AT Command

The module can also be safely turned off with **AT+QPOWD**, which is similar to turning off the module via PWRKEY pin. See [document \[4\]](#), [\[5\]](#), [\[6\]](#) and [\[7\]](#) for details about **AT+QPOWD**.

NOTE

- To avoid corrupting the data in the internal flash, do not switch off the power supply while the module is working normally. The power supply can be cut off only after the module is shut down with PWRKEY or AT command.

2. For BG95 series, PWRKEY output voltage is 1.5 V because of the voltage drop inside the chipset. Due to platform reasons, the reset function is integrated into PWRKEY on the chipset. Therefore, never pull down PWRKEY to GND permanently.
3. For BG96 and EG9x family, PWRKEY output voltage is 0.8 V because of the diode voltage drop inside the chipset.
4. For EG9x family and EG915Q-NA, when turning off the module with the AT command, keep PWRKEY at high level after the execution of the command. Otherwise, the module will be turned on automatically again after successful turn-off.

4.3. Reset

EG9x and BG9x family modules can be reset by driving RESET_N low for a certain time or directly via a button.

For EG915Q-NA, the reset function requires the joint operations of PWRKEY and RESET_N pins. The module can be reset by pulling down PWRKEY when RESET_N is at low level.

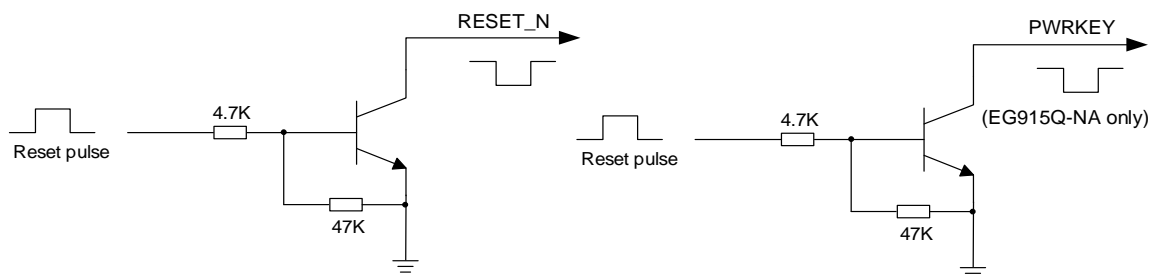


Figure 13: Reference Design of RESET_N with a Driving Circuit

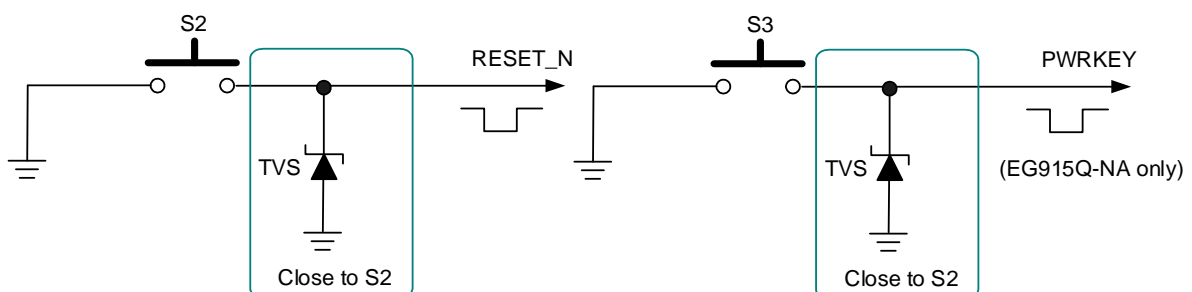


Figure 14: Reference Circuit of RESET_N by Using Button

The reset timing for BG9x and EG9x families is illustrated in the following figure.

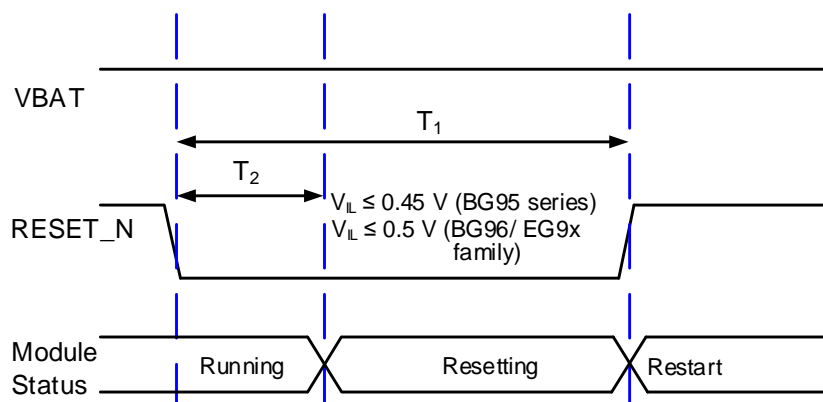


Figure 15: Reset Timing (BG9x & EG9x Families)

Table 12: Reset Timing

Module	T_1	T_2
BG95 series	$\leq 3.8 \text{ s}$	$\geq 2 \text{ s}$
BG96	$\leq 460 \text{ ms}$	$\geq 150 \text{ ms}$
EG9x family	$\leq 460 \text{ ms}$	$\geq 150 \text{ ms}$

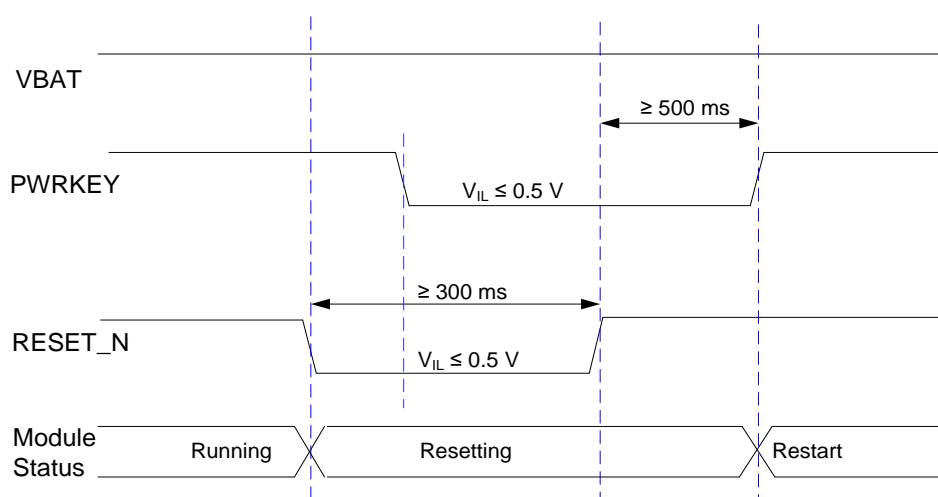


Figure 16: Reset Timing (EG915Q-NA)

NOTE

1. Use RESET_N function only if turn-off with **AT+QPOWD** and PWRKEY pin fails.
2. Ensure that there is no large capacitance on PWRKEY and RESET_N pins.
3. For BG95 series:
 - due to platform reasons, the reset function is integrated into PWRKEY on the chipset, and RESET_N is directly connected to PWRKEY inside the module.
 - RESET_N should not be pulled down to GND permanently.

4.4. (U)SIM Interface(s)

BG9x family and EG915Q-NA support one (U)SIM interface and EG9x family supports two (U)SIM interfaces.

Table 13: Pin Difference of (U)SIM Interfaces

Pin No.	BG95 Series	BG96	EG9x Family	EG915Q-NA	Comment
42	USIM_DET	USIM_PRESENCE	USIM1_PRESENCE	USIM_DET	1.8 V power domain.
43	USIM_VDD	USIM_VDD	USIM1_VDD	USIM_VDD	BG95 series: Only 1.8 V (U)SIM card is supported.
44	USIM_RST	USIM_RST	USIM1_RST	USIM_RST	
45	USIM_DATA	USIM_DATA	USIM1_DATA	USIM_DATA	BG96 & EG9x family & EG915Q-NA: Either 1.8 V or 3.0 V (U)SIM card is supported and can be identified automatically by the module.
46	USIM_CLK	USIM_CLK	USIM1_CLK	USIM_CLK	
47	USIM_GND	USIM_GND	USIM_GND	GND	-
83	GRFC1 ²²	RESERVED	USIM2_PRESENCE	RESERVED	1.8 V power domain.
84	GRFC2 ²²	RESERVED	USIM2_CLK	RESERVED	EG9x family: 1.8 V or 3.0 V (U)SIM2 card is supported.
85	GPIO6	RESERVED	USIM2_RST	RESERVED	
86	GPIO7	RESERVED	USIM2_DATA	RESERVED	BG9x family & EG915Q-NA:

²² BG95-M4/-M9 does not support GRFC interfaces (pins 83 and 84).

87	GPIO8	RESERVED	USIM2_VDD	RESERVED	(U)SIM2 interface is not supported.
----	-------	----------	-----------	----------	-------------------------------------

4.5. USB Interface

BG9x, EG9x and EG915Q-NA provide one integrated Universal Serial Bus (USB) interface, which complies with USB 2.0 specification and only supports USB slave mode.

Table 14: Data Rate and Function of USB Interface

Module	Data Rate	Function
BG95 Series	<ul style="list-style-type: none"> High-speed (480 Mbps) Full-speed (12 Mbps) Low-speed (1.5 Mbps) 	<ul style="list-style-type: none"> AT command communication Data transmission ²³ Software debugging Firmware upgrade GNSS NMEA sentence output
BG96	<ul style="list-style-type: none"> High-speed (480 Mbps) Full-speed (12 Mbps) 	<ul style="list-style-type: none"> AT command communication Data transmission ²³ Software debugging Firmware upgrade GNSS NMEA sentence output
EG9x Family	<ul style="list-style-type: none"> High-speed (480 Mbps) Full-speed (12 Mbps) 	<ul style="list-style-type: none"> AT command communication Data transmission Software debugging Firmware upgrade GNSS NMEA sentence output Voice over USB
EG915Q-NA	<ul style="list-style-type: none"> High-speed (480 Mbps) Full-speed (12 Mbps) 	<ul style="list-style-type: none"> AT command communication Data transmission Software debugging Firmware upgrade Partial log output

NOTE

The GNSS function for BG96 and EG9x family is optional.

²³ It is not recommended to use USB for data communication, as this will increase the power consumption.

Table 15: Pin Difference of USB_VBUS

Pin Name	Pin No.	I/O	DC Characteristics			
			BG95 Series	BG96	EG9x Family	EG915Q-NA
USB_VBUS	8	AI	Vmax= 5.25 V	Vmax = 5.25 V	Vmax = 5.25 V	Vmax = 5.25 V
			Vmin = 4.0 V	Vmin = 3.0 V	Vmin = 3.0 V	Vmin = 3.0 V
			Vnom = 5.0 V	Vnom = 5.0 V	Vnom = 5.0 V	Vnom = 5.0 V

For BG9x and EG9x families, it is recommended to reserve the USB interface for firmware upgrade. For EG915Q-NA, test points of USB 2.0 interface must be reserved for firmware upgrade and software debugging. Following figures illustrate the reference design of USB interface.

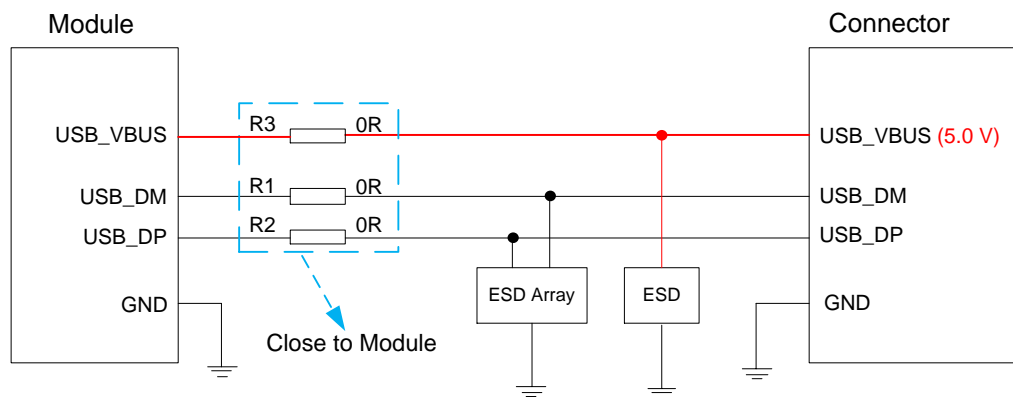


Figure 17: Reference Design of USB Interface (BG95 Series)

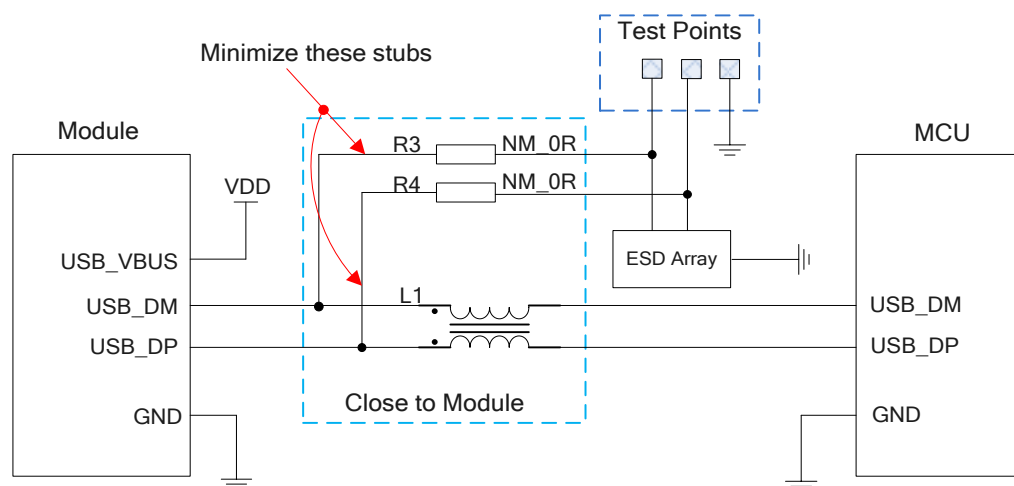


Figure 18: Reference Design of USB Interface (BG96 & EG9x Family & EG915Q-NA)

4.6. PCM and I2C Interfaces ²⁴

BG9x family, EG9x family and EG915Q-NA provide one PCM interface and one I2C interface.

For EG9x family, PCM interface supports [slave and master modes](#). For EG9x and BG9x families, I2C interface only supports [master mode](#).

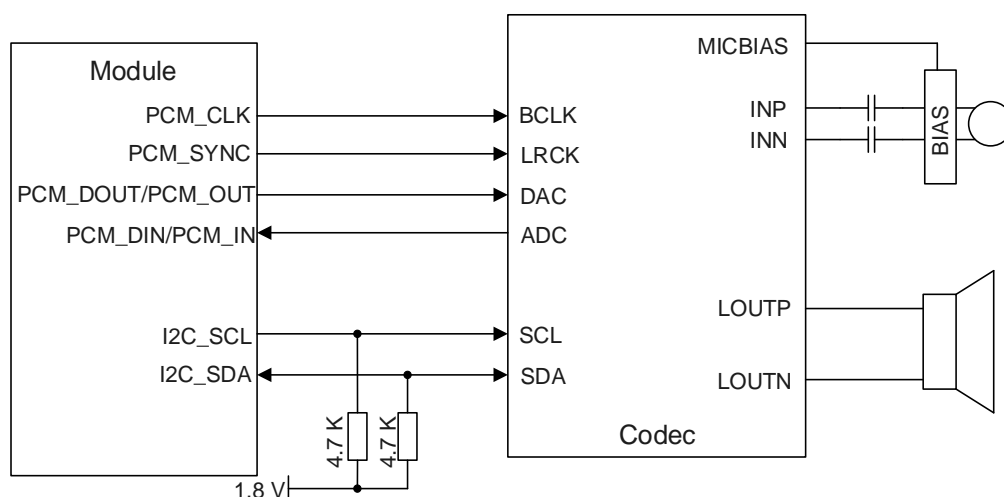


Figure 19: PCM and I2C Application with Audio Codec (BG9x & EG9x Families & EG915Q-NA)

4.7. UART Interfaces

BG9x family has [three](#) UART interfaces: main UART, debug UART and GNSS UART.

EG9x family and EG915Q-NA have [two](#) UART interfaces: main UART and debug UART.

Table 16: Pin Difference of UART Interfaces

UART	Pin No.	BG95 Series	BG96	EG9x Family	EG915Q-NA
Main UART	30	MAIN_DTR	DTR	DTR	MAIN_DTR
	34	MAIN_RXD	RXD	RXD	MAIN_RXD
	35	MAIN_TXD	TXD	TXD	MAIN_TXD
	36	MAIN_CTS	CTS	CTS	MAIN_CTS

²⁴ The PCM and I2C interfaces of EG915Q-NA are still under development.

	37	MAIN_RTS	RTS	RTS	MAIN_RTS
	38	MAIN_DCD	DCD	DCD	MAIN_DCD
	39	MAIN_RI	RI	RI	MAIN_RI
Debug UART	22	DBG_RXD	DBG_RXD	DBG_RXD	DBG_RXD
	23	DBG_TXD	DBG_TXD	DBG_TXD	DBG_TXD
GNSS UART	28	GNSS_RXD	UART3_RXD	-	-
	27	GNSS_TXD	UART3_TXD	-	-

4.8. ADC Interfaces

BG9x family and EG915Q-NA have [two](#) ADC interfaces: ADC0 and ADC1.

EG9x family has [one](#) ADC interface: ADC0.

Table 17: Pin Difference of ADC Interfaces

Pin Name	Pin No.	I/O	DC Characteristics			
			BG95 Series	BG96	EG9x Family	EG915Q-NA
ADC0	24	AI	0.1–1.8 V	0.3–1.8 V	0.3 V–VBAT_BB	0–1.2 V
ADC1	2	AI	0.1–1.8 V	0.3–1.8 V	-	0–1.2 V

4.9. Antenna Interfaces

ANT_MAIN of BG9x family, EG9x family and EG915Q-NA are compatible with each other, whereas BG95 series' GNSS and Wi-Fi antenna interfaces, BG96's GNSS antenna interface, EG9x family's Rx-diversity and GNSS antenna interfaces are not compatible.

Table 18: Pin Definition of BG95 Series Antenna Interfaces

Pin Name	Pin No.	I/O	Description	Comment
ANT_MAIN	60	AIO	Main antenna interface	50 Ω impedance.
ANT_GNSS	49	AI	GNSS antenna interface	
ANT_WIFI ²⁵	56	AI	Wi-Fi antenna interface	

Table 19: Pin Definition of BG96 Antenna Interfaces

Pin Name	Pin No.	I/O	Description	Comment
ANT_MAIN	60	AIO	Main antenna interface	50 Ω impedance.
ANT_GNSS	49	AI	GNSS antenna interface	

Table 20: Pin Definition of EG9x Family Antenna Interface

Pin Name	Pin No.	I/O	Description	Comment
ANT_MAIN	60	AIO	Main antenna interface	50 Ω impedance.
ANT_GNSS/ ANT_DIV ²⁶	49	AI	GNSS antenna interface/ Diversity antenna interface	
ANT_DIV/ RESERVED ²⁷	56	AI/ -	Diversity antenna interface/ Reserved	

Table 21: Pin Definition of EG915Q-NA Antenna Interface

Pin Name	Pin No.	I/O	Description	Comment
ANT_MAIN	60	AIO	Main antenna interface	50 Ω impedance.

It is recommended to reserve a Π -type matching circuit for better RF performance, and the Π -type matching components (R1, C1, C2 and R2, C3, C4) should be placed as close to the antenna as possible. The capacitors are not mounted by default.

²⁵ Only BG95-MF supports ANT_WIFI (pin 56).

²⁶ For EG91 series, pin 49 is defined as ANT_GNSS on EG91-AUX/-EX/-JP/-NA/-NAX/-NAXD/-VX, while it is defined as ANT_DIV on EG91-E. For EG95 series, pin 49 is defined as ANT_GNSS on EG95-AUX/-EX/-JP/-NA/-NAX/-NAXD, while it is defined as ANT_DIV on EG95-E.

²⁷ For EG91 series, pin 56 is defined as ANT_DIV on EG91-EX/-JP/-NA/-NAX/-NAXD/-VX, while it is defined as RESERVED on EG91-AUX/-E. Rx-diversity antenna is not supported on EG91-AUX. For EG95 series, pin 56 is defined as ANT_DIV on EG95-AUX/-EX/-JP/-NA/-NAX/-NAXD, while it is defined as RESERVED on EG95-E.

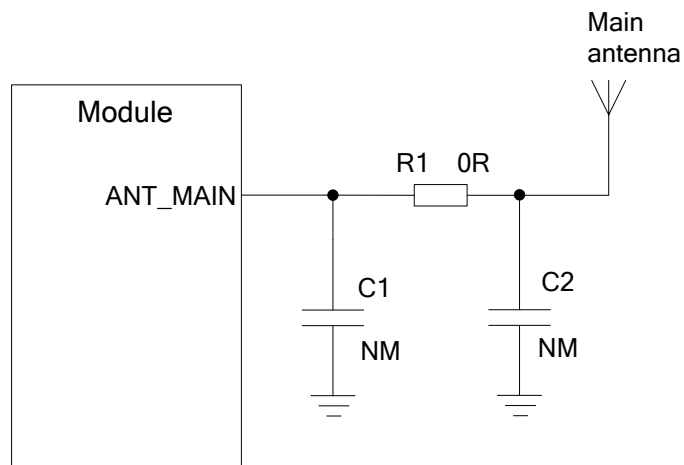


Figure 20: Main Antenna Interfaces (BG9x Family & EG915Q-NA)

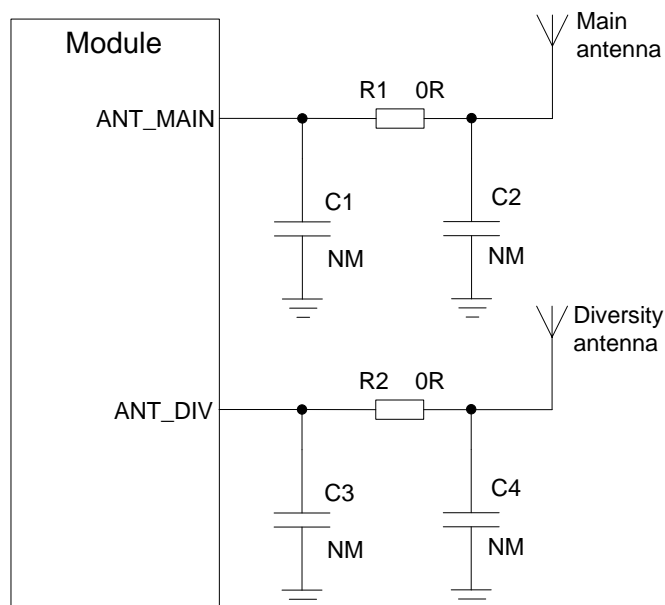


Figure 21: Main and Rx-diversity Antenna Interfaces (EG9x Family)

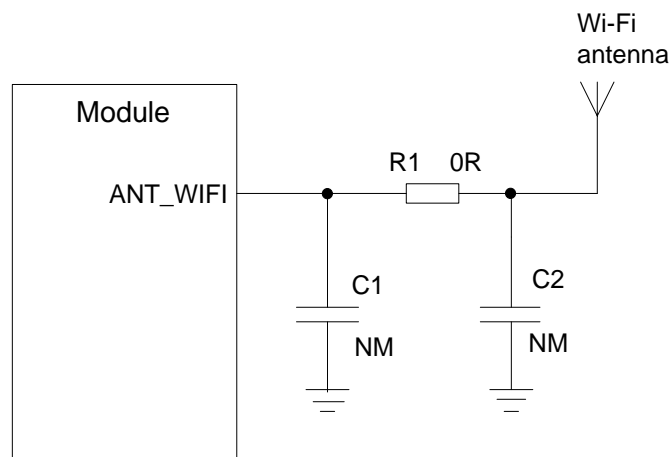


Figure 22: Wi-Fi Antenna Interface (BG95 Series)

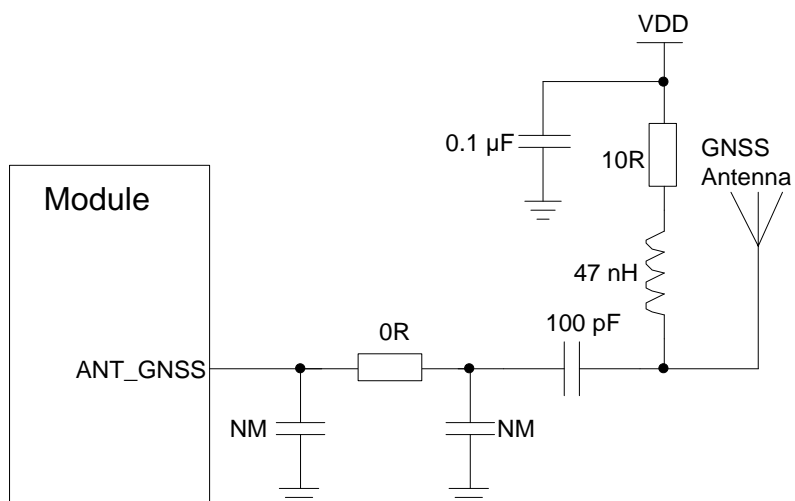


Figure 23: GNSS Antenna Interface (EG9x and BG9x Families)

NOTE

For the GNSS antenna of EG9x and BG9x families, if the module is designed with a passive antenna, then the VDD circuit is not needed.

5 Recommended Footprint

This chapter mainly describes the recommended footprint and stencil design for BG9x family, EG9x family and EG915Q-NA. All dimensions are measured in mm, and the tolerances for dimensions without tolerance values are ± 0.2 mm.

5.1. Recommended Compatible Footprint

The following figure shows the bottom views of BG9x family, EG9x family and EG915Q-NA.

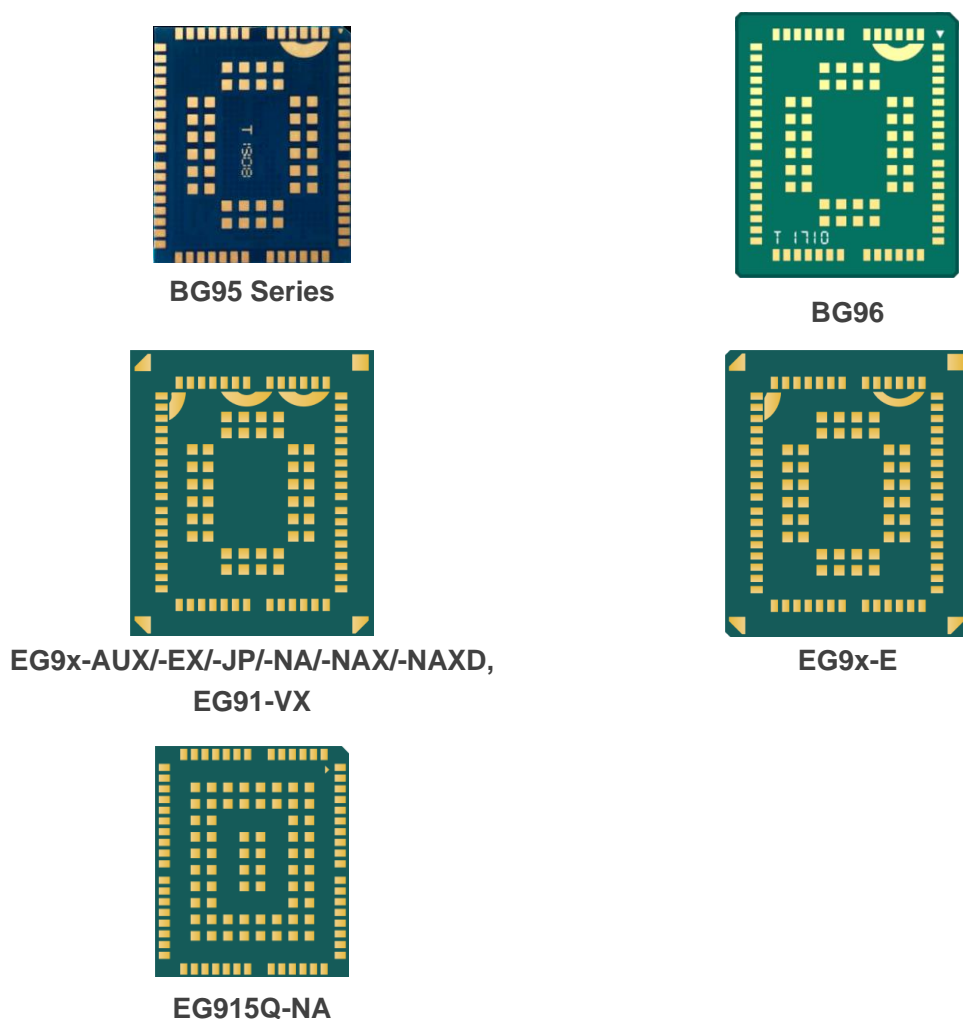


Figure 24: Bottom Views of BG9x & EG9x Families & EG915Q-NA

NOTE

Images above are for illustration purpose only and may differ from the actual module. For authentic appearance and label, please refer to the module received from Quectel.

The following figure shows the recommended compatible footprint of the modules.

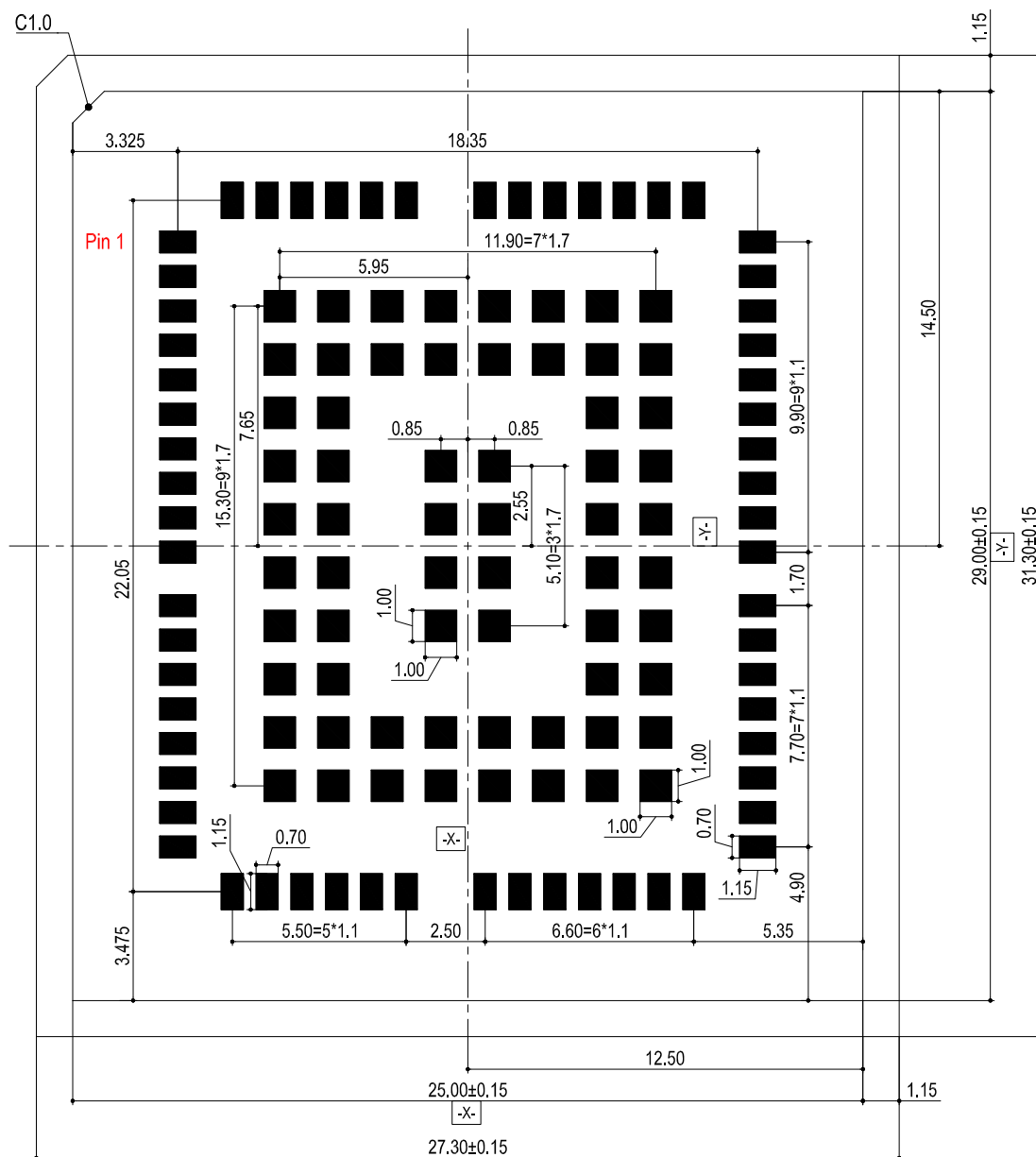


Figure 25: Recommended Compatible Footprint of BG9x & EG9x Families & EG915Q-NA

NOTE

1. The package warpage level of the module conforms to the *JEITA ED-7306* standard.
2. Keep at least 3 mm between the module and other components on the motherboard to improve soldering quality and maintenance convenience.

5.2. Installation Sketch Map

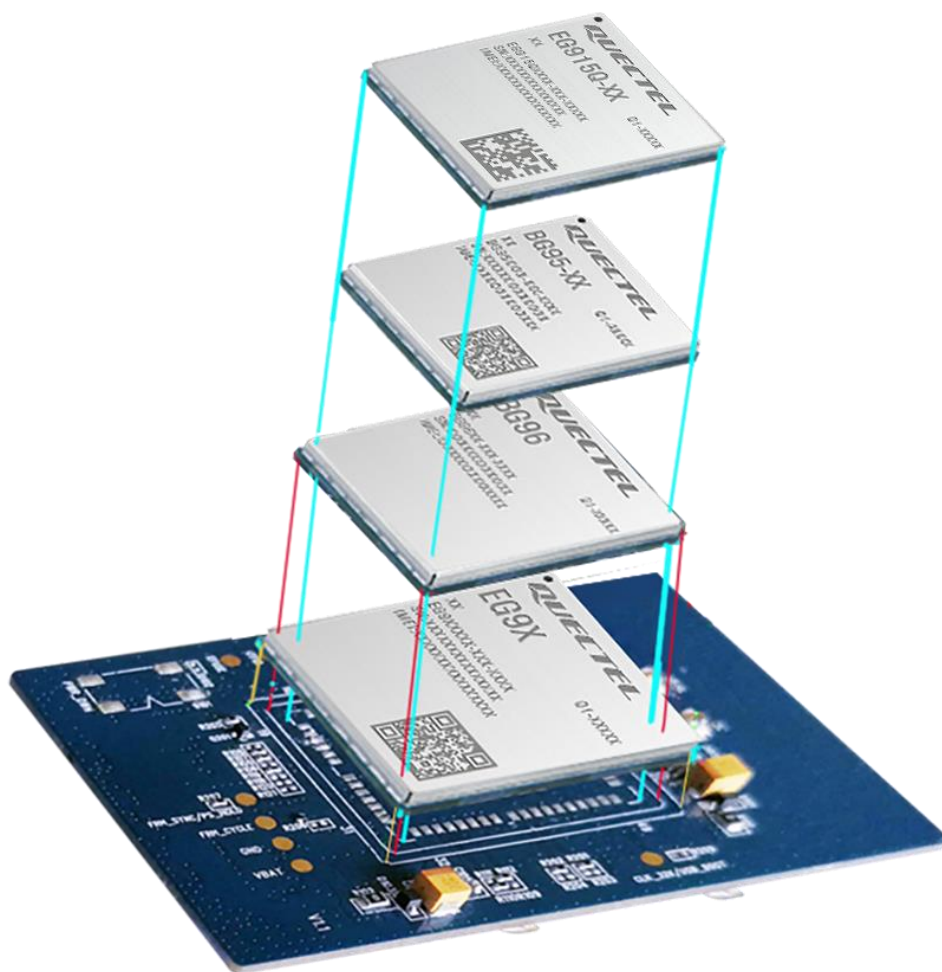


Figure 26: Installation Sketch Map for BG9x & EG9x Families & EG915Q-NA

6 Appendix References

Table 22: Related Documents

Document Name
[1] Quectel_BG95&BG77&BG600L_Series_QCFG_AT_Commands_Manual
[2] Quectel_BG95_Series_Hardware_Design
[3] Quectel_BG96_Hardware_Design
[4] Quectel_BG95&BG77&BG600L_Series_AT_Commands_Manual
[5] Quectel_BG96_AT_Commands_Manual
[6] Quectel_EC2x&EG2x-G(L)&EG9x&EM05_Series_AT_Commands_Manual
[7] Quectel_EG800Q-EU&EG915Q-NA_AT_Commands_Manual

Table 23: Terms and Abbreviations

Abbreviation	Description
bps	bits per second
CS	Coding Scheme
CTS	Clear To Send
DC-HSDPA	Dual-carrier High Speed Downlink Packet Access
DFOTA	Delta Firmware Upgrade Over The Air
DRX	Discontinuous Reception
DTR	Data Terminal Ready
EDGE	Enhanced Data Rates for GSM Evolution

EGPRS	Enhanced General Packet Radio Service
FDD	Frequency Division Duplex
GNSS	Global Navigation Satellite System
GPRS	General Packet Radio Service
GSM	Global System for Mobile Communications
HSDPA	High Speed Downlink Packet Access
HSUPA	High Speed Uplink Packet Access
I/O	Input/Output
IoT	Internet of Things
LGA	Land Grid Array
LPWA	Low-Power Wide-Area (Network)
LTE	Long Term Evolution
NMEA	NMEA (National Marine Electronics Association) 0183 Interface Standard
PCM	Pulse Code Modulation
PF	Paging Frame
PSM	Power Saving Mode
RF	Radio Frequency
Rx	Receive
SMS	Short Message Service
TDD	Time Division Duplexing
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
(U)SIM	(Universal) Subscriber Identity Module
Vmax	Maximum Voltage
Vnom	Nominal Voltage

Vmin	Minimum Voltage
VoLTE	Voice (voice calls) over LTE
WCDMA	Wideband Code Division Multiple Access