Ngveri Keywords In eSim-2.3

To convert a Verilog model into Ngspice we use the makerchip and ngveri. The makerchip is used to first simulate the file and check the resultant waveform and then the verilog file is converted. After a successful generation of the desired waveform we save the verilog file, then add the dependency files (if any) in Ngveri and convert the file into Ngspice.

While performing the conversion some of the keywords in Ngveri might throw an error while simulating. These are mainly the **names and types of the input and output ports** declared in the verilog file.

1. All the input, output and inout ports should avoid names which include **input, output, reg, wire, read, write, execute, decode, fetch** as substrings.
   Eg: input instruction_fetch_en - will result in an error.

2. All variable names that are declared as default variables in verilog at the start of the code **should not** be used to define the **size of any vector** in the **input and output ports**.
   Eg: `define WIDTH 8
   output reg [`WIDTH-1:0] pc

3. Should not use the **unknown type (x)** in variables it may throw an error while converting as it is not supported by verilator.
   Eg: `define ALU_NC 3'bxxx
   case(cmd)
   `ALU_NC :

4. Avoid using module names such as **register_file** it throws an error that file and module name are not the same although we used the same module and file name. The keyword register creates a problem.

5. Do Not use a **two dimensional vector example memory** as an **input and output port** of a module, it will throw an error.
   Eg: output reg [15:0] out_res [7:0] - will result in an error.

6. Do Not use **@** or wait commands which are not supported by verilator.

If you find any other keywords or variable names which throws an error while converting from verilog to Ngspice do let us know.