American International University – Bangladesh
Department of Electrical and Electronic Engineering
EEE4217: VLSI CIRCUIT DESIGN LAB

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VLSI Final Project
Project Title: Design and Layout of the Logic Function ((A.B)+E+(C.D))' Using Complementary CMOS Logic in Cadence Virtuoso.

Submitted to-

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Project Title: Design and Layout of the Logic Function F=((A.B)+E+(C.D))' Using Complementary CMOS Logic in Cadence Virtuoso.

Abstract: This work involves designing, simulating, laying out, and verifying the digital logic function F = ((A·B) + E + (C·D))'with complementary CMOS logic. The function acts as a NOR operation on two AND terms and one single input. It requires a structured design and an optimized layout. The implementation took place in Cadence Virtuoso using 45nm GPDK technology. The process started with sizing the transistors based on a reference inverter. This was followed by capturing the schematic and performing transient simulations to ensure the logical function worked. A stick diagram was created, organized with Euler's path A, B, E, C, D, to assist with layout planning and diffusion sharing. The final physical layout was made with careful placement of devices. Design accuracy was confirmed through DRC and LVS checks. Simulations were also conducted to assess power consumption and propagation delay. Overall, this project shows a solid understanding of transistor-level digital design and verification in an industry-standard setting.

Introduction: Complementary CMOS (Metal-Oxide-Semiconductor) logic is the foundation of nearly all modern digital integrated circuits. It offers significant benefits, including low static power loss, strong noise margins, scalability in deep submicron domains, and compatibility with high-density integration. By using both NMOS and PMOS transistors in a complementary setup, CMOS circuits ensure that only one type of transistor is active during steady-state operation. This design leads to very low power use, full voltage swings, and reliable switching performance.

The main goal of this project is to design, simulate, layout, and verify the moderately complex digital logic function F = ((A·B) + E + (C·D))'. This function represents a NOR operation applied to two AND operations along with a single input. It is crucial for hardware applications like processor control logic, memory address decoding, and conditional decision-making in embedded systems. Implementing this function in CMOS involves building a pull-down network (PDN) of NMOS transistors to represent the original Boolean expression. Meanwhile, a corresponding pull-up network (PUN) of PMOS transistors ensures proper functionality and robustness**.**

The project emphasizes several important design steps:

- Translating the Boolean logic into a transistor-level schematic using CMOS principles
- Creating an efficient stick diagram guided by Euler's path to reduce layout complexity and improve diffusion sharing
- Developing a compact, optimized, and design-rule-compliant layout in 45nm technology for realistic fabrication readiness
- Verifying design accuracy through transient simulations, Design Rule Check (DRC), and Layout Versus Schematic (LVS) verification
- Conducting post-layout analysis to assess key performance metrics such as propagation delay, power usage, and area efficiency

This hands-on design flow, carried out on the Cadence Virtuoso platform, reflects real-world VLSI development practices. It provides students and professionals with practical skills in CMOS transistor-level logic design, layout optimization, and verification methods. This experience lays a solid foundation for careers in digital systems and VLSI engineering.

Theory and Logic Design:

CMOS Implementation

Pull-Up Network (PUN):

- Two PMOS transistors, A and B, are connected in parallel to represent the dual of A·B
- A PMOS transistor, E, is connected in series with this group.
- Likewise, two PMOS transistors, C and D, are connected in parallel to form the dual of C·D
- Finally, these three parallel groups are connected in series to create the complement of the PDN.

Pull-Down Network (PDN):

- A pair of NMOS transistors, A and B, are connected in series to realize the term A·B
- Another pair of NMOS transistors, C and D, are also connected in series to form C·D
- An additional NMOS transistor, E, is placed in parallel with both the A·B and C·D branches.
- These three series branches are then combined in parallel to implement the OR operation.

Logic Breakdown

The function F = ((A·B) + E + (C·D))' can be broken down into these parts:

- Two AND operations: A·B and C·D, along with a single input E.
- One OR operation: combining the results as (A·B) + E + (C·D)
- One NOT operation: inverting the entire expression

In CMOS realization:

- The Pull-Down Network (PDN), made with NMOS transistors, directly implements the original logic expression.
- The Pull-Up Network (PUN), formed using PMOS transistors, represents the dual of the PDN to ensure the opposite behavior.

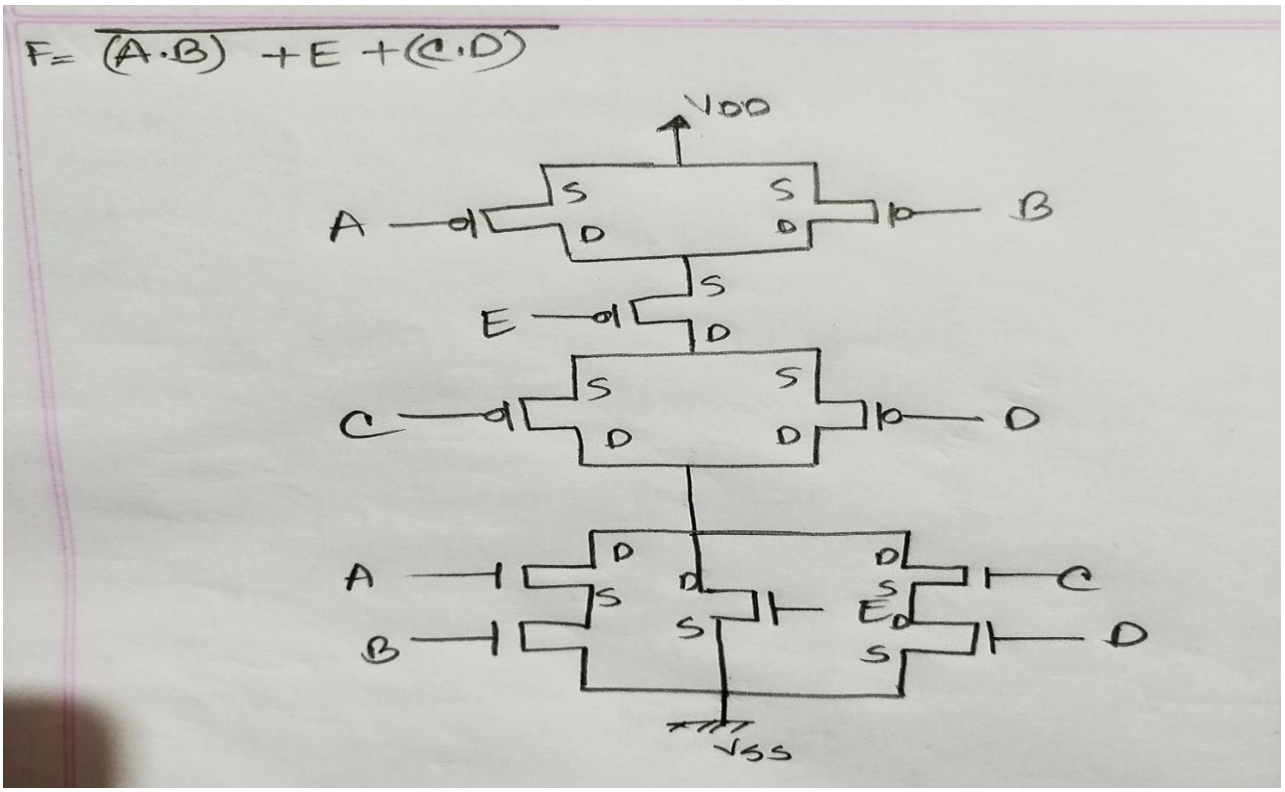


Figure 1: Logic Gate-Level Representation of the Function F = ((A·B) + E + (C·D))'

Truth Table of F = ((A·B) + E + (C·D))'for Logic Function Verification

A	B	E	C	D	A.B	C.D	A.B+E+C.D	(A.B+E+C.D)'
0	0	0	0	0	0	0	0	1
0	0	1	0	1	0	0	1	0
0	1	0	1	0	0	0	0	1
0	1	0	1	1	0	1	1	0
1	0	0	0	0	0	0	0	1
1	0	1	0	1	0	0	1	0
1	1	0	1	0	1	0	1	0

Methodology : The design was created in Cadence Virtuoso using the 45 nm CMOS technology node (gpdk045 PDK). The workflow included every stage of the VLSI design process, such as schematic creation, simulation setup, stick diagram development, layout design, and post-layout validation. The logic circuit was achieved through the following sequence of steps: $F = ((A \cdot B) + E + (C \cdot D))'$

1.Schematic Design in Virtuoso

- The circuit was created in the Virtuoso Schematic Editor XL using the gpdk045 technology library.
- The design included five PMOS and five NMOS transistors.
- Logic inputs A, B, C, D,E connected to the gates of the transistors.
- The final output node F came from the point where the pull-up and pull-down networks meet.
- The body terminals of the transistors were set to "Detached" to enable flexible placement of substrate and well contacts during layout.

2. Setting Up Transient Simulation in ADE XL:

Once the schematic was finalized, we evaluated the dynamic response using the Analog Design Environment XL (ADE XL).

Power Supply Setup:

- A DC source of 1.8 V was connected to VDD.
- GND was set at 0 V.

Input Signal Configuration:

Inputs A, B, C, D, and E received the same pulse waveforms.

- Period: 10 ns
- Voltage levels: 0 V (low) to 1.8 V (high)
- Rise time: 10 ps
- Fall time: 10 ps

Transient Analysis Procedure:

- We selected the transient ("tran")analysis option from the Choose Analyses panel.
- Under Outputs → Setup, we marked nodes A, B, C, D, E, and F as probes.
- The simulation ran using Netlist and Run.
- We examined the resulting waveforms in the ADE waveform viewer and confirmed they matched the expected logic function.

3. Stick Diagram

- A manual stick diagram was drawn using the Euler path **A–B–E–C–D** to optimize transistor placement.
- **Shared diffusion regions** were utilized to minimize layout area.
- **Source and drain terminals** were clearly marked.
- Different layers such as **polysilicon, n-diffusion, p-diffusion, Metal1, and Metal2** were represented.
- **Body contacts and VDD/GND rails** were also included in the diagram.

4. Layout Design

- The layout was initiated from the schematic using **Launch → Layout XL**.
- Devices were auto-placed via **Generate → All from Source**.

- Snap settings were configured to **any-angle (option-display → Snap mode → create anyangle)** and later set to **diagonal** with a **stop time of 10**.
- **Metal1 and Metal2** were used to route VDD, GND, inputs, and outputs.
- **Vias** were inserted between metal layers wherever necessary.
- The layout was refined manually to ensure **compactness, symmetry, and full DRC compliance**.
- The **Euler path strategy** helped reduce **diffusion breaks** and **routing congestion**.

5. Design Rule Check (DRC)

- **Pegasus → Run DRC** was executed using **45nm gpdk PDK** rule definitions.
- All **spacing, width, enclosure, and contact** constraints were validated.
- The layout **passed DRC successfully with zero violations**.

6. Layout vs. Schematic (LVS)

- **Pegasus → Run LVS** was used to compare the **extracted layout netlist** with the **original schematic**.
- Verification included:
  - Device count consistency
  - Correct pin-wise connectivity
  - Proper instance recognition
- **LVS passed with a 100% match**, confirming no errors or warnings.

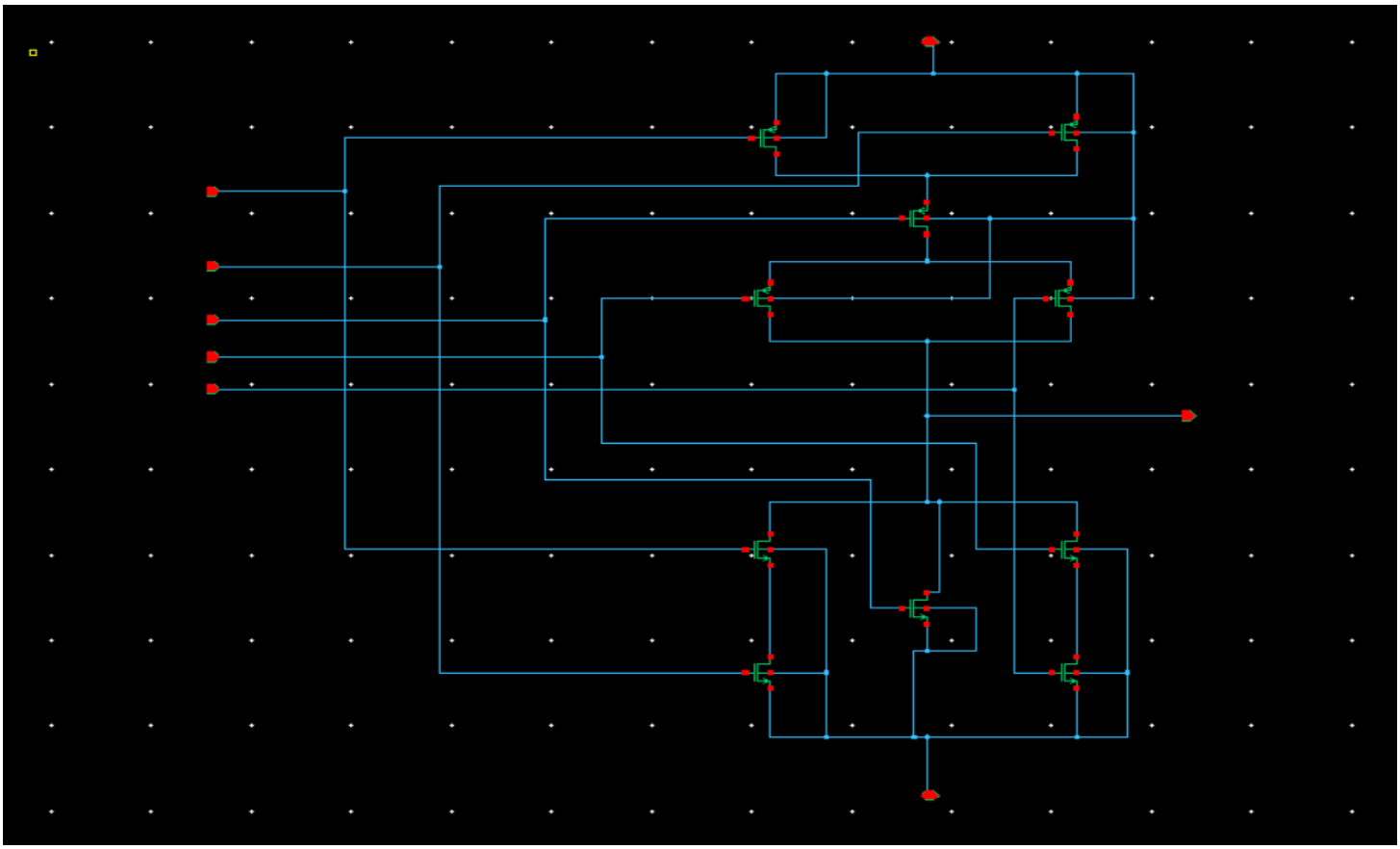


Figure 2: Transistor-Level CMOS Schematic of the Logic Function in Cadence Virtuoso For, F = ((A·B) + E + (C·D))'

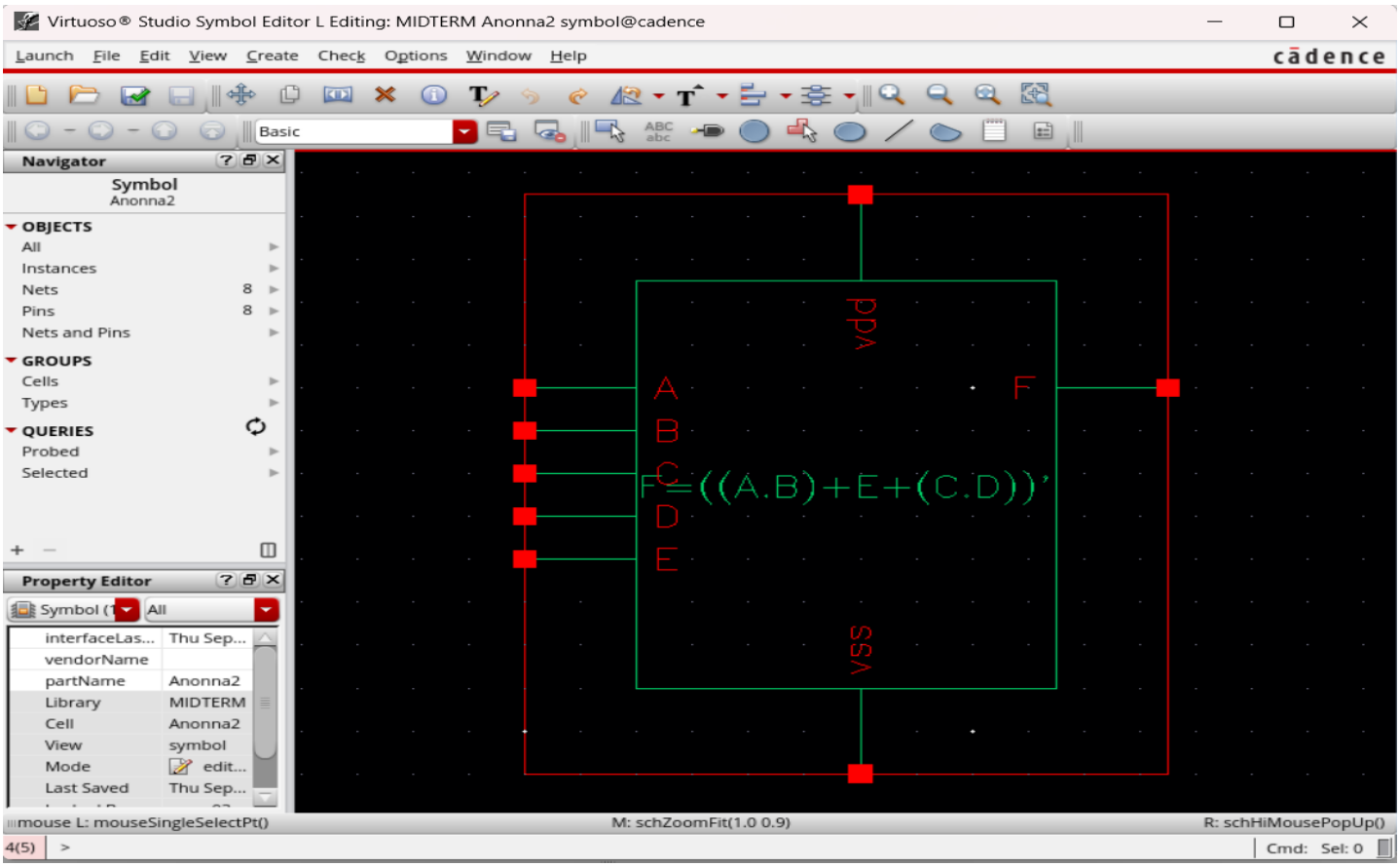


Figure 3: Custom Symbol of the Logic Function

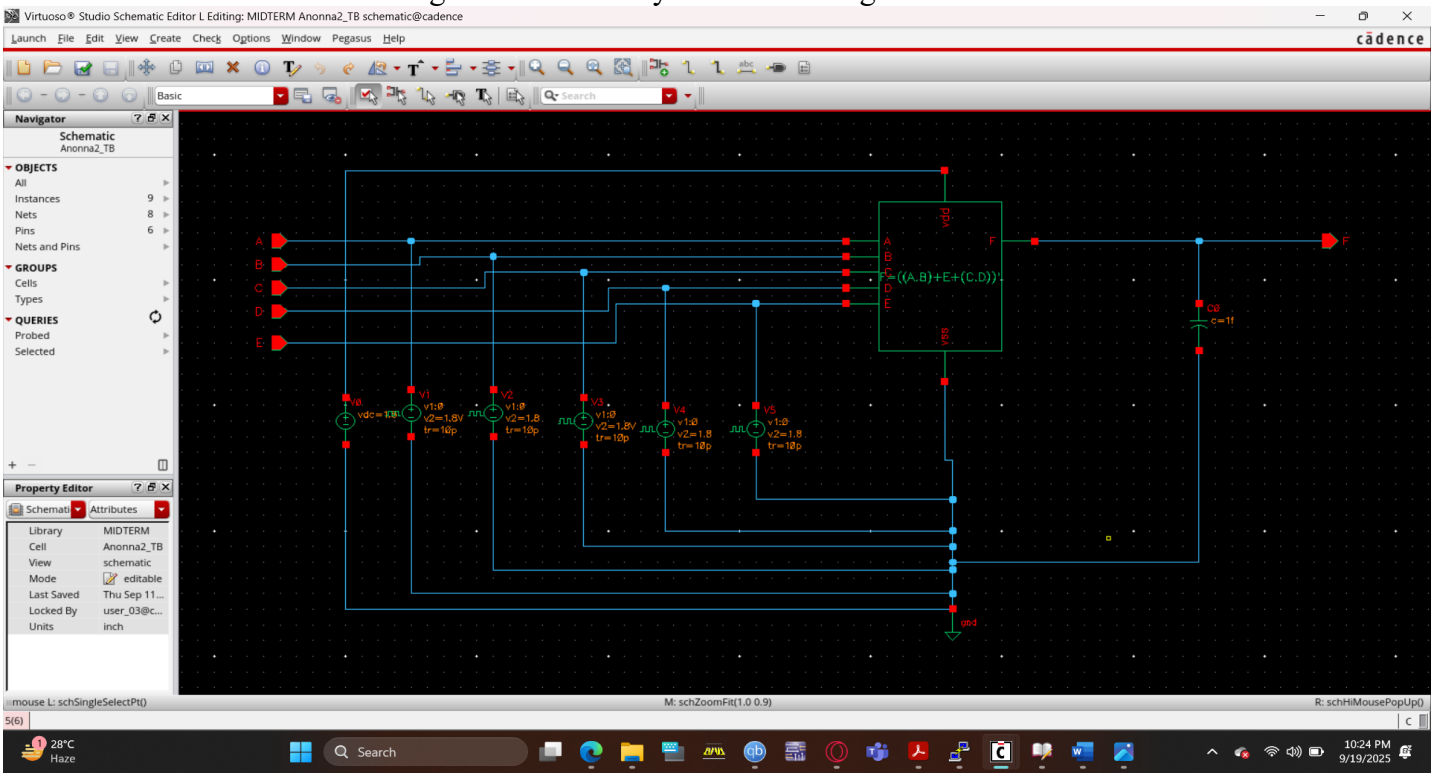


Figure 4: Logic Function , F = ((A·B) + E + (C·D))'in ADE XL

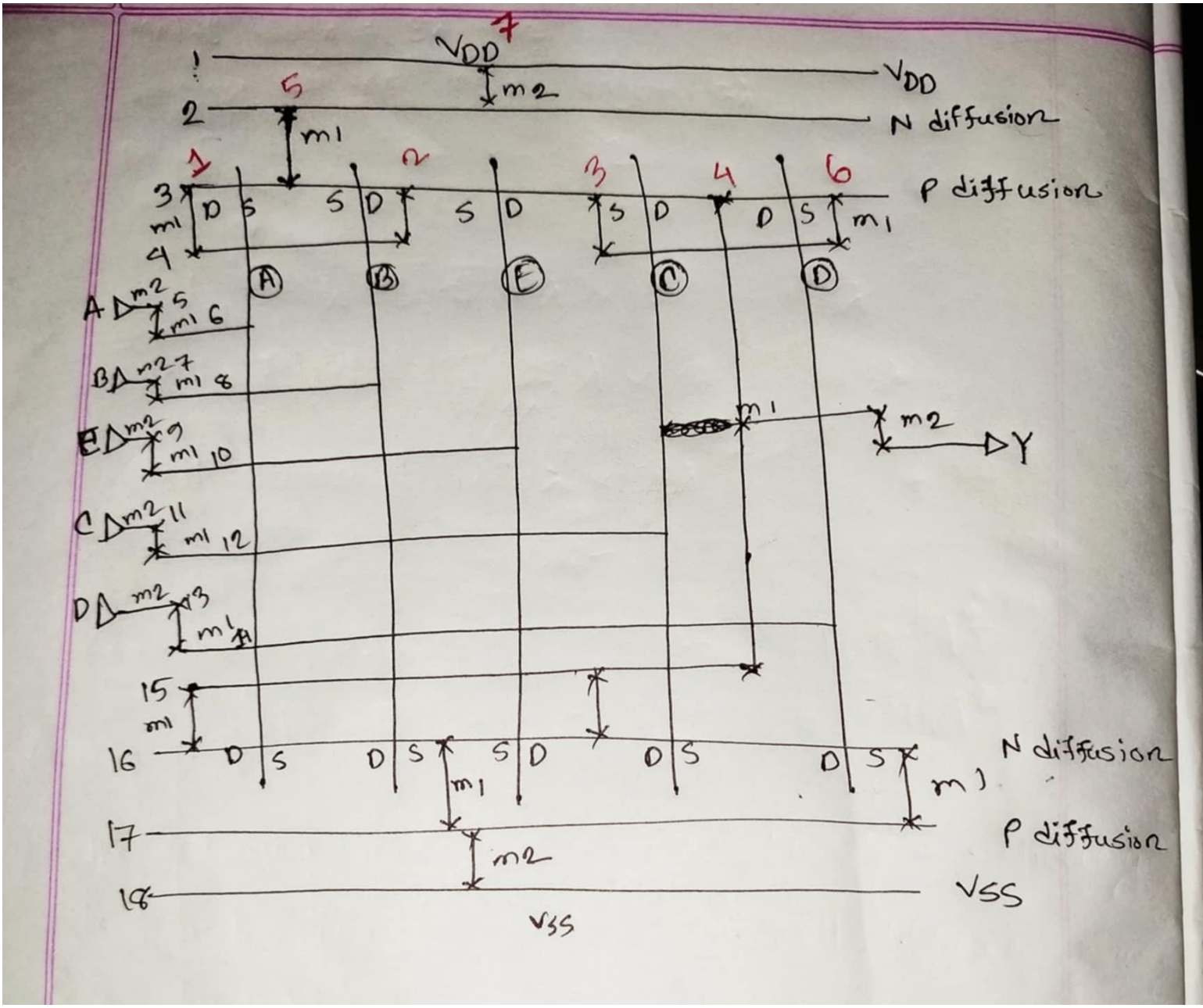


Figure 5: Stick Diagram of the Logic Function Using Euler Path: A-B-E-C-D

7. Cell Area Estimation

No horizontal metal/ diffusion tracks = 18

No of vertical metal tracks = 7

Given that every diffusion or metal track must maintain a minimum width of **4λ**, and a **4λ separation** is required between neighboring metal layeRS,

Approximate cell area = $[18 \times(4\lambda + 4\lambda)]\times[7\times(4\lambda + 4\lambda)]= 8064\lambda^2$

Simulation and Results:

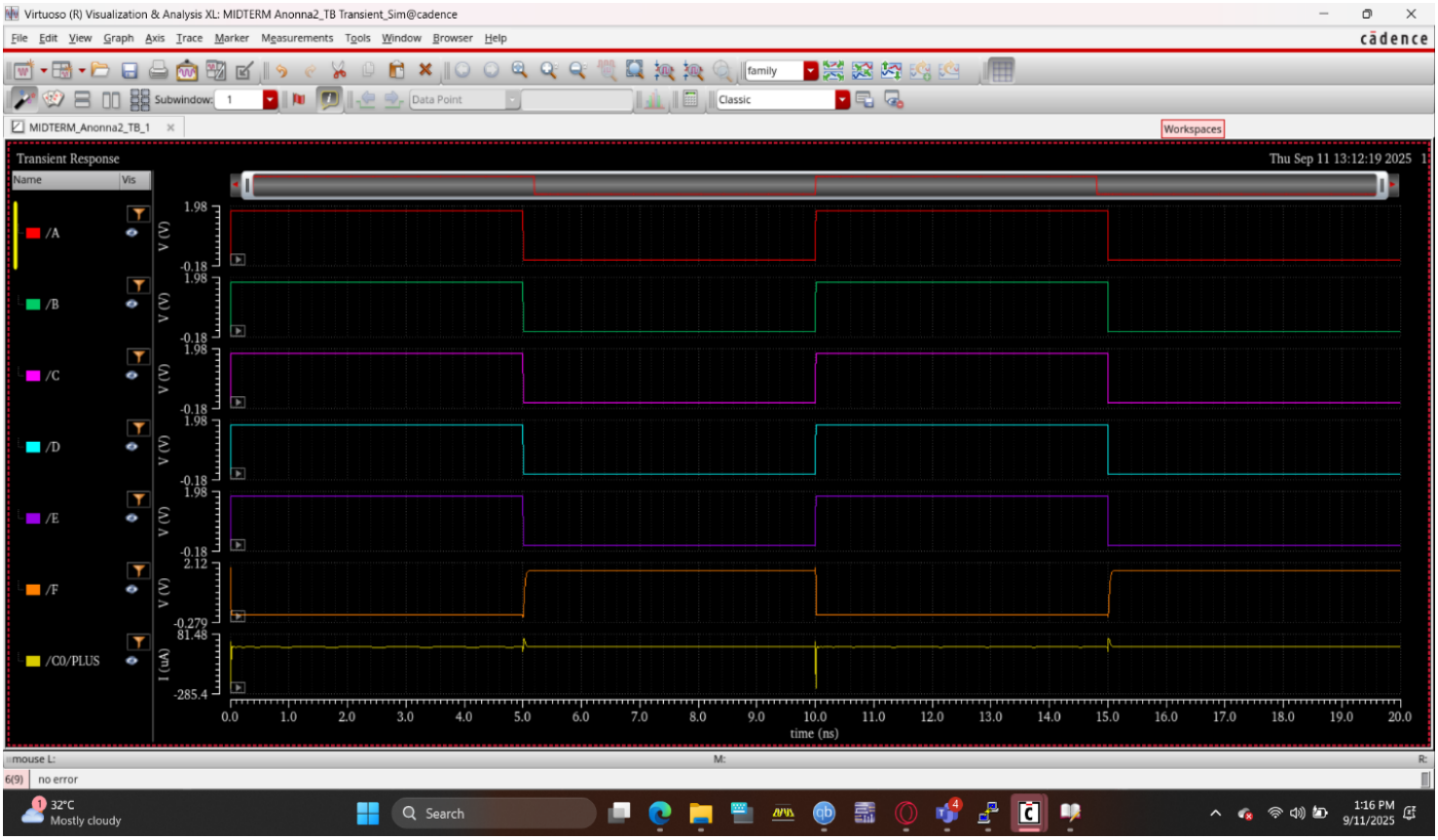
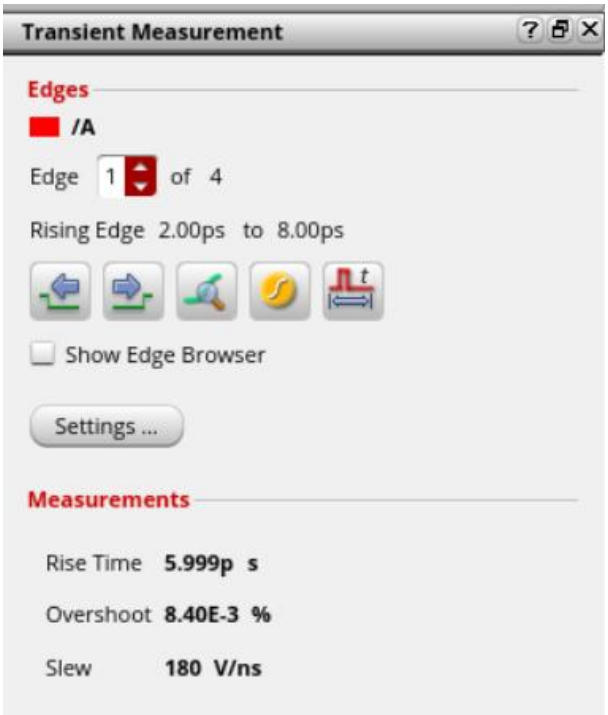
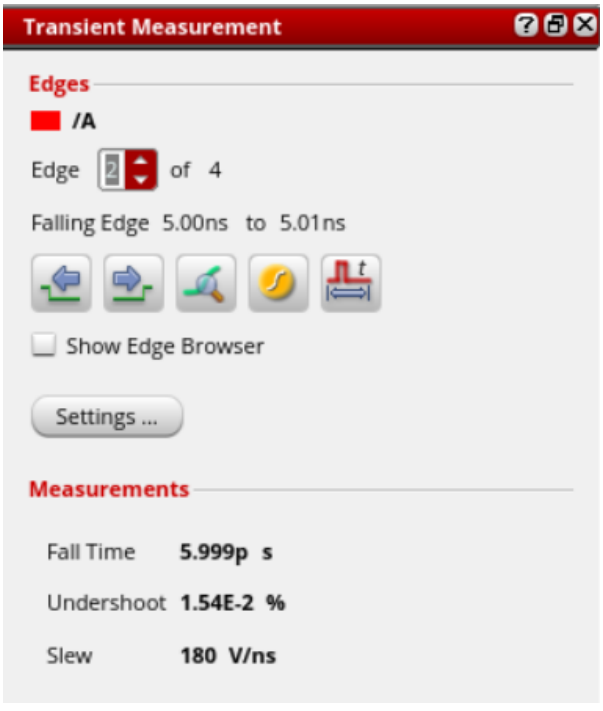
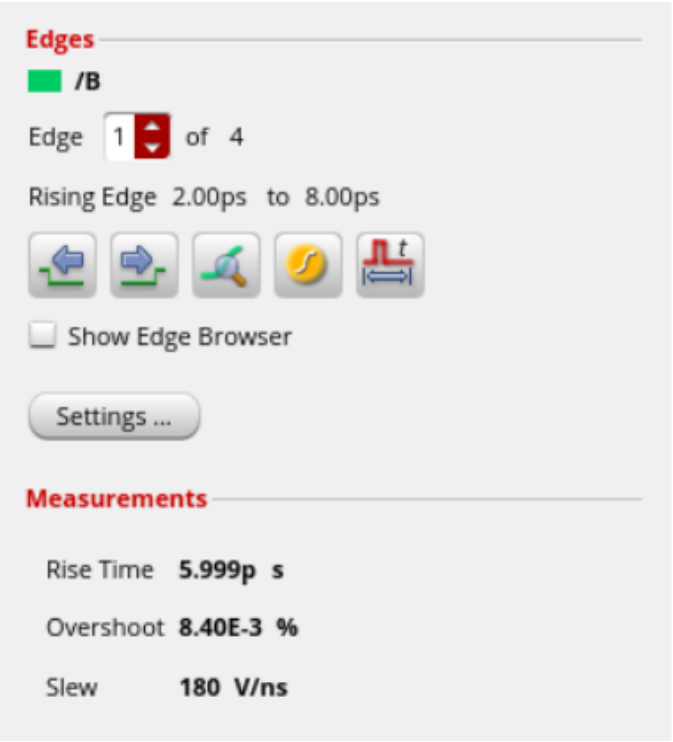
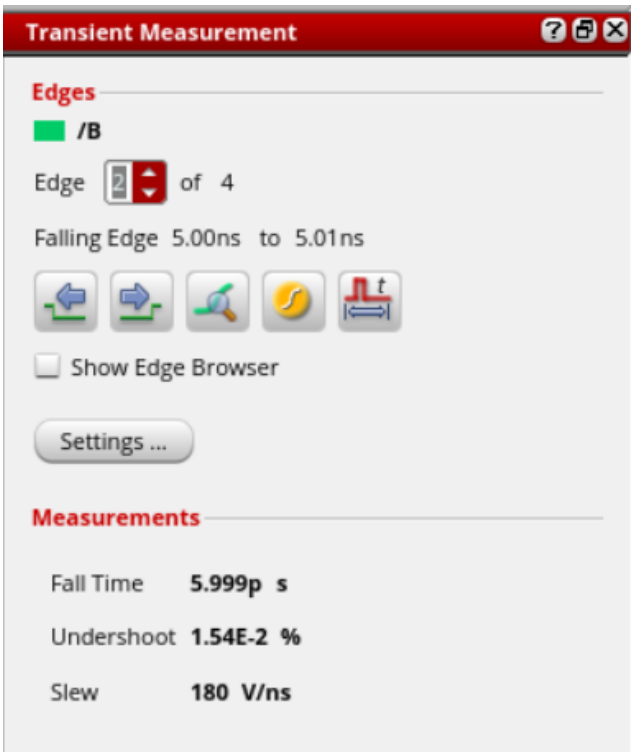


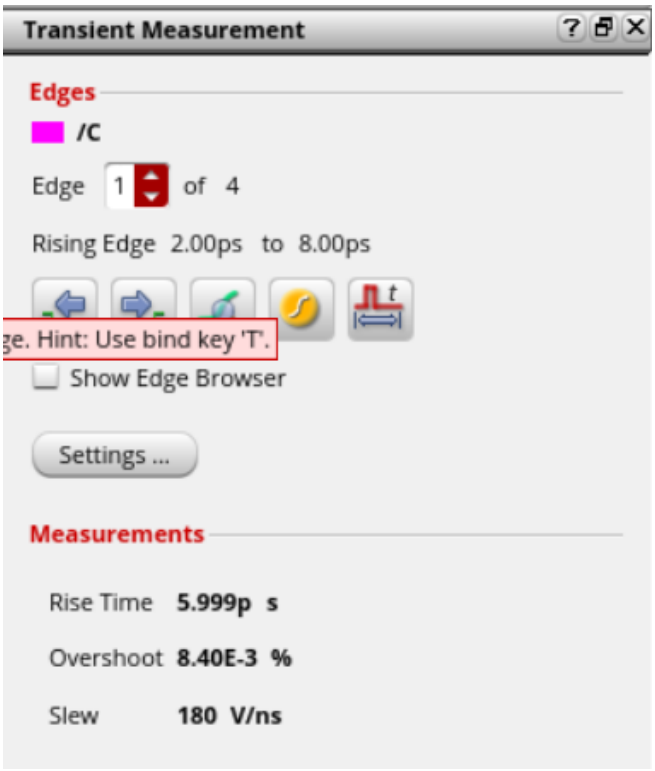
Figure 6: Transient Simulation Waveforms Showing Inputs A, B, C, D, E and Output F.

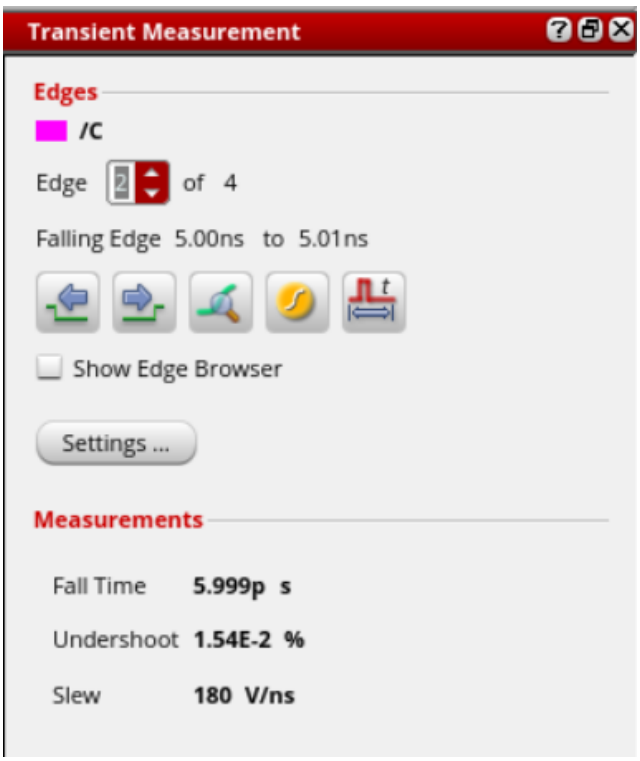


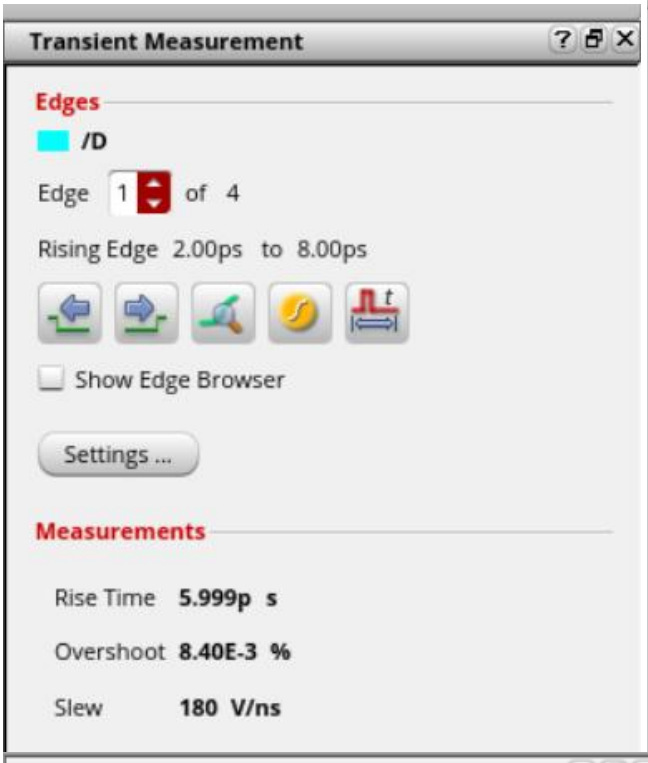


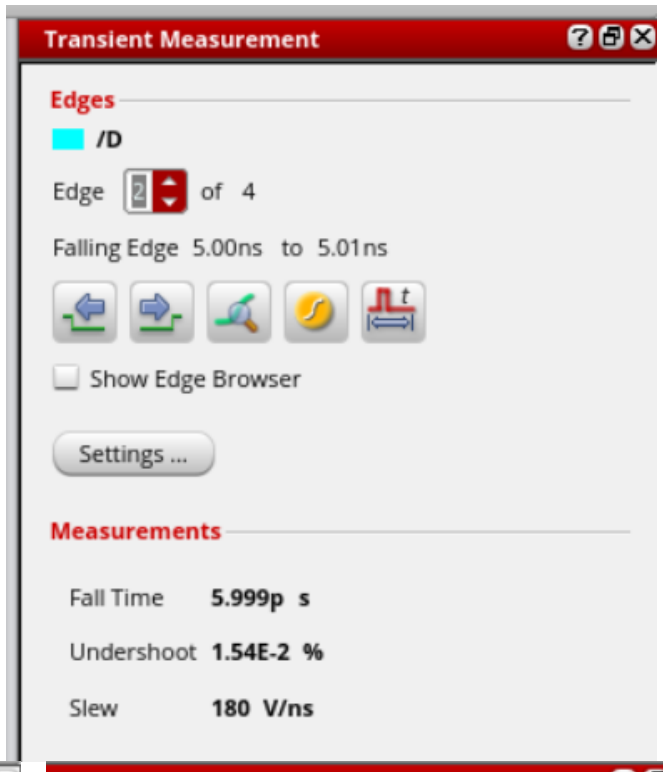

Edges
/B
Edge 1 of 4
Rising Edge 2.00ps to 8.00ps
Show Edge Browser
Settings ...
Measurements
Rise Time 5.999p s
Overshoot 8.40E-3 %
Slew 180 V/ns


Transient Measurement
Edges
/B
Edge 2 of 4
Falling Edge 5.00ns to 5.01ns
Show Edge Browser
Settings ...
Measurements
Fall Time 5.999p s
Undershoot 1.54E-2 %
Slew 180 V/ns


Transient Measurement
Edges
/C
Edge 1 of 4
Rising Edge 2.00ps to 8.00ps
ge. Hint: Use bind key 'T'.
Show Edge Browser
Settings ...
Measurements
Rise Time 5.999p s
Overshoot 8.40E-3 %
Slew 180 V/ns


Transient Measurement
Edges
/C
Edge 2 of 4
Falling Edge 5.00ns to 5.01ns
Show Edge Browser
Settings ...
Measurements
Fall Time 5.999p s
Undershoot 1.54E-2 %
Slew 180 V/ns


Transient Measurement
Edges
/D
Edge 1 of 4
Rising Edge 2.00ps to 8.00ps
Show Edge Browser
Settings ...
Measurements
Rise Time 5.999p s
Overshoot 8.40E-3 %
Slew 180 V/ns


Transient Measurement
Edges
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Edge 2 of 4
Falling Edge 5.00ns to 5.01ns
Show Edge Browser
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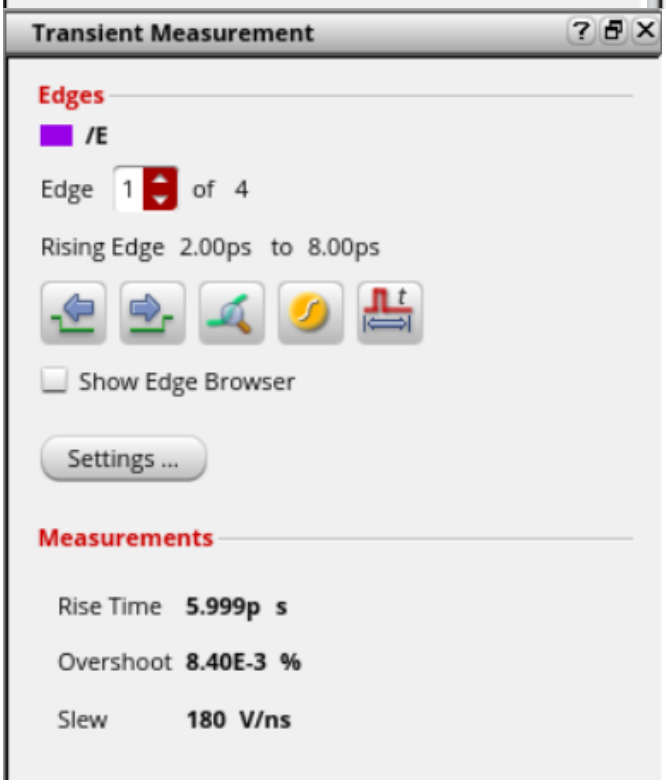
Measurements
Fall Time 5.999p s
Undershoot 1.54E-2 %
Slew 180 V/ns


Transient Measurement
Edges
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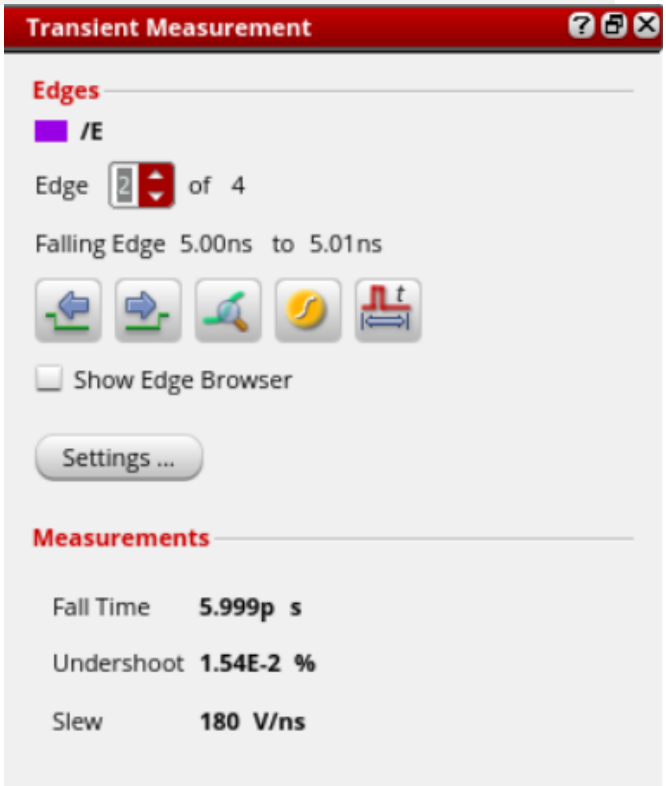
Edge 1 of 4
Rising Edge 2.00ps to 8.00ps
Show Edge Browser
Settings ...
Measurements
Rise Time 5.999p s
Overshoot 8.40E-3 %
Slew 180 V/ns


Transient Measurement
Edges
/E
Edge 2 of 4
Falling Edge 5.00ns to 5.01ns
Show Edge Browser
Settings ...
Measurements
Fall Time 5.999p s
Undershoot 1.54E-2 %
Slew 180 V/ns

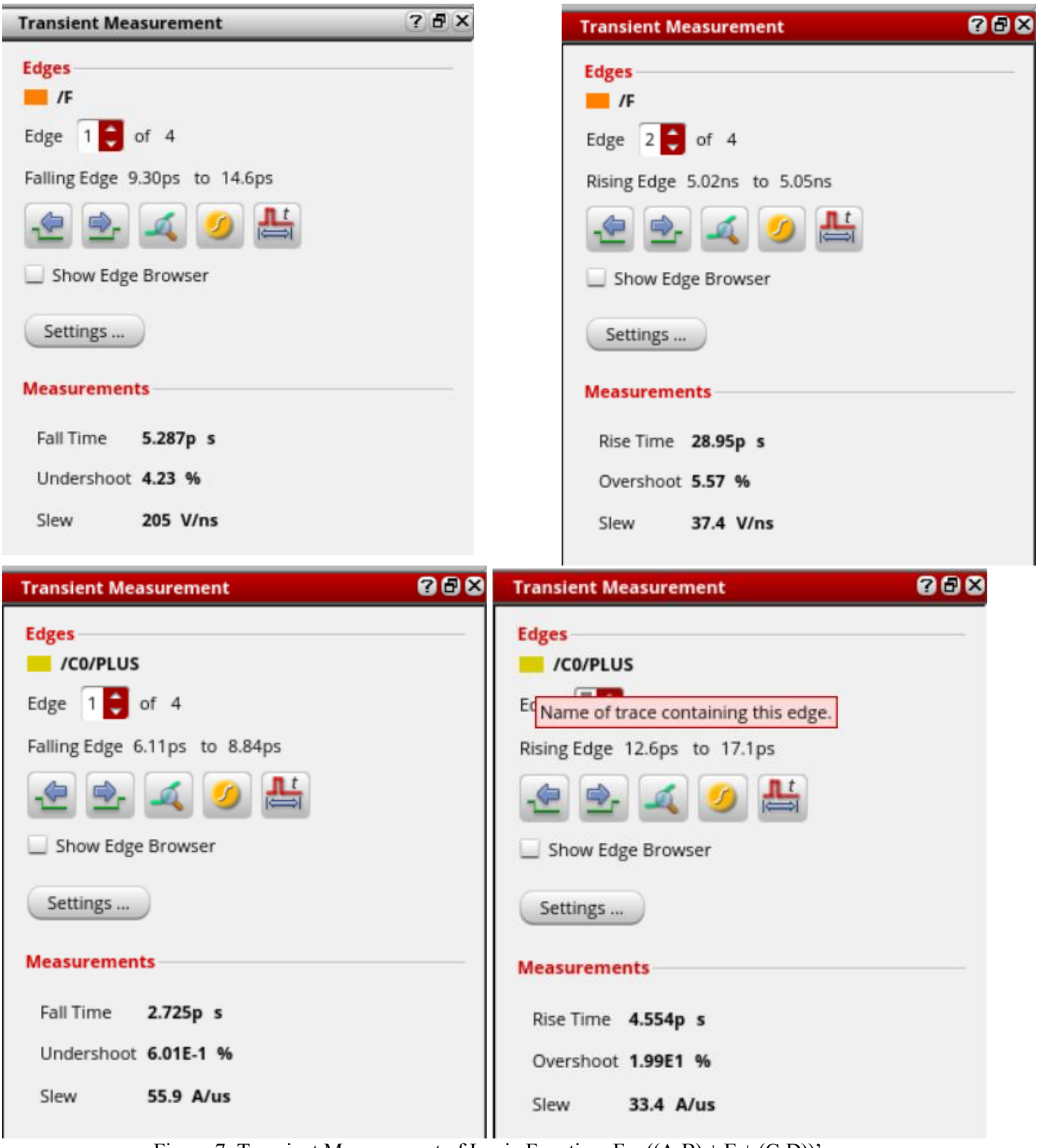


Figure 7: Transient Measurement of Logic Function $F = ((A \cdot B) + E + (C \cdot D))'$

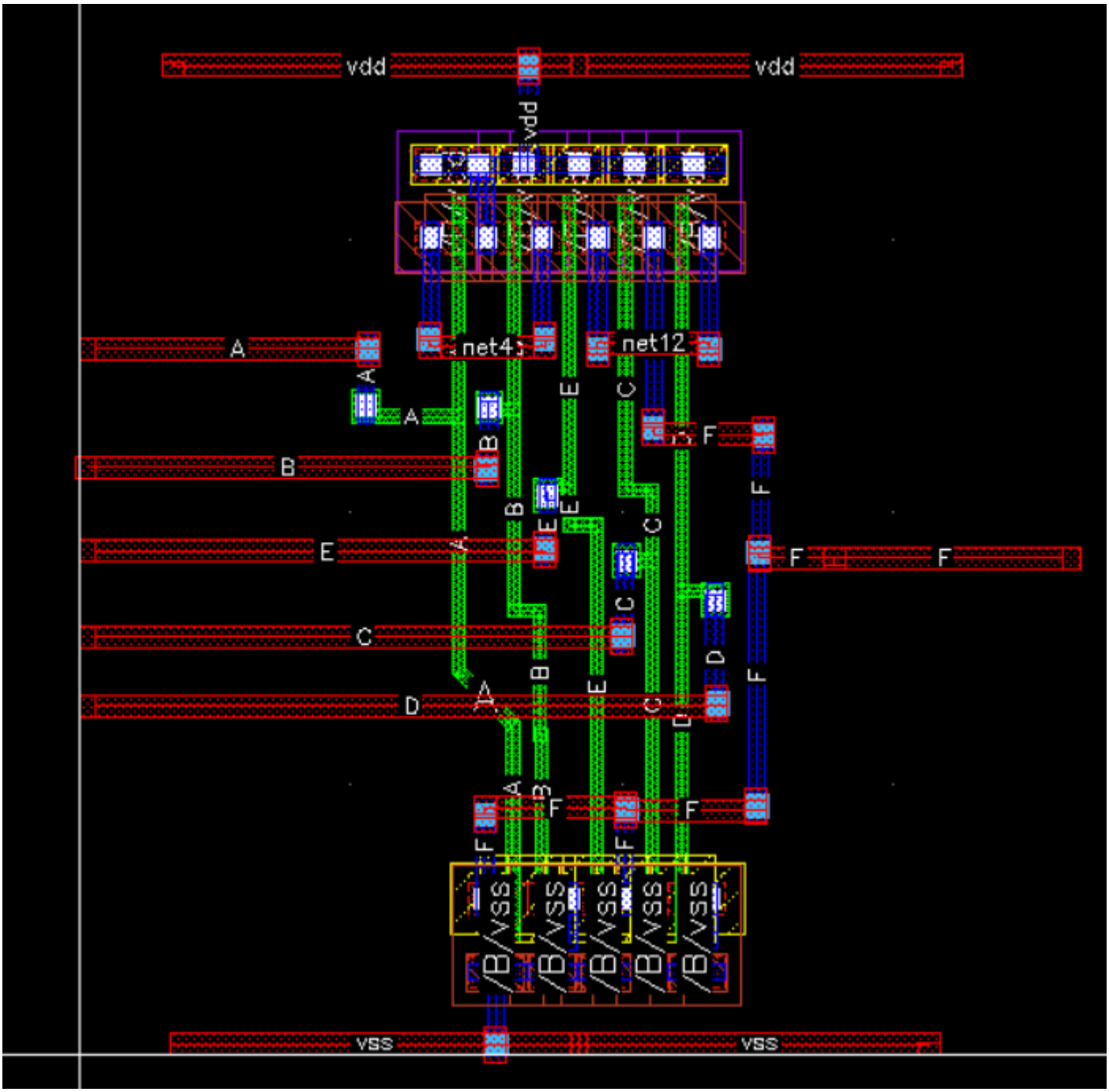


Figure 8: Physical Layout of the CMOS Logic Gate in Virtuoso Layout Editor XL.

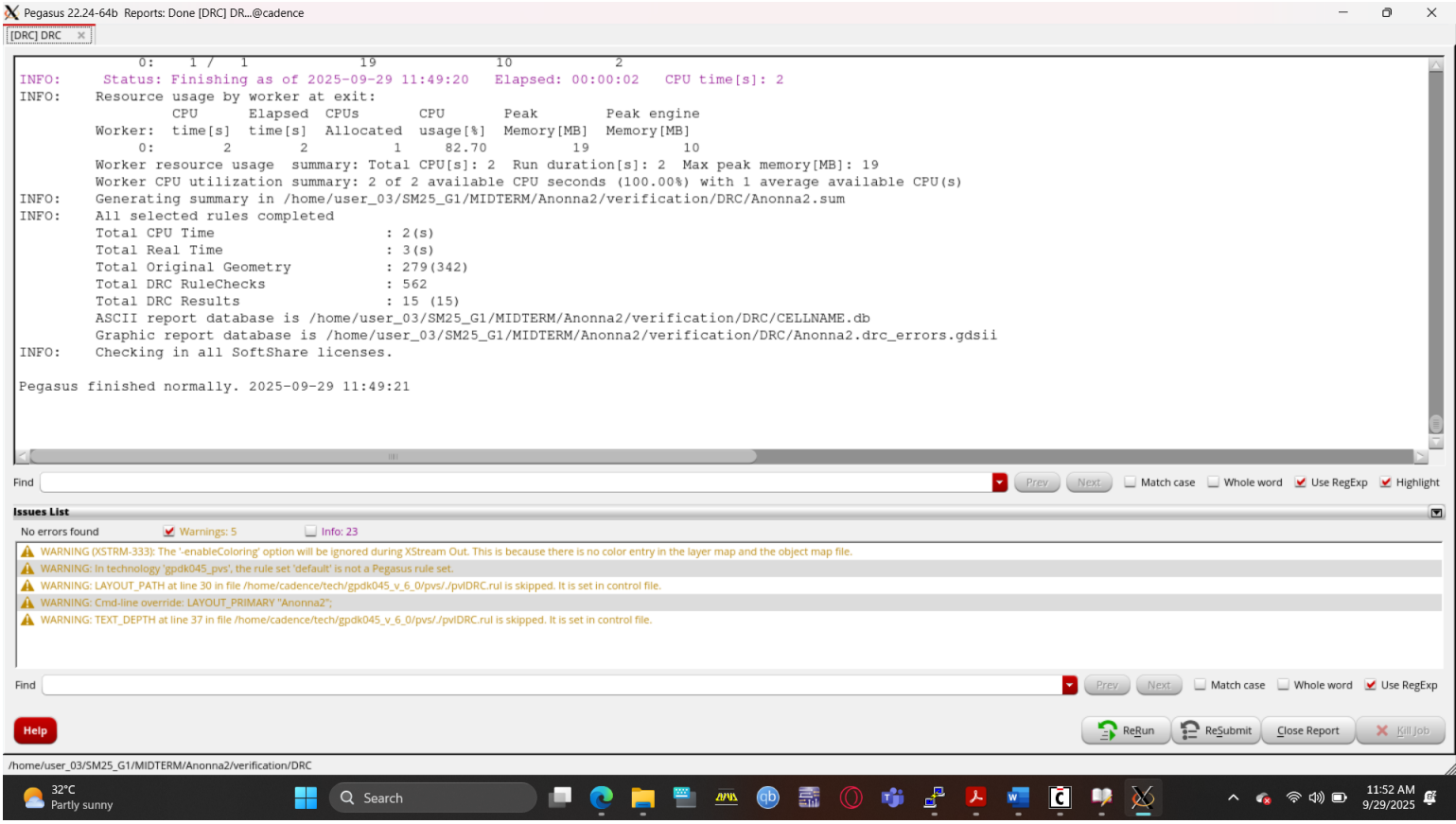


Figure 9: Clean DRC Result of Complementary CMOS Logic Function F= ((A·B) + E + (C·D))'

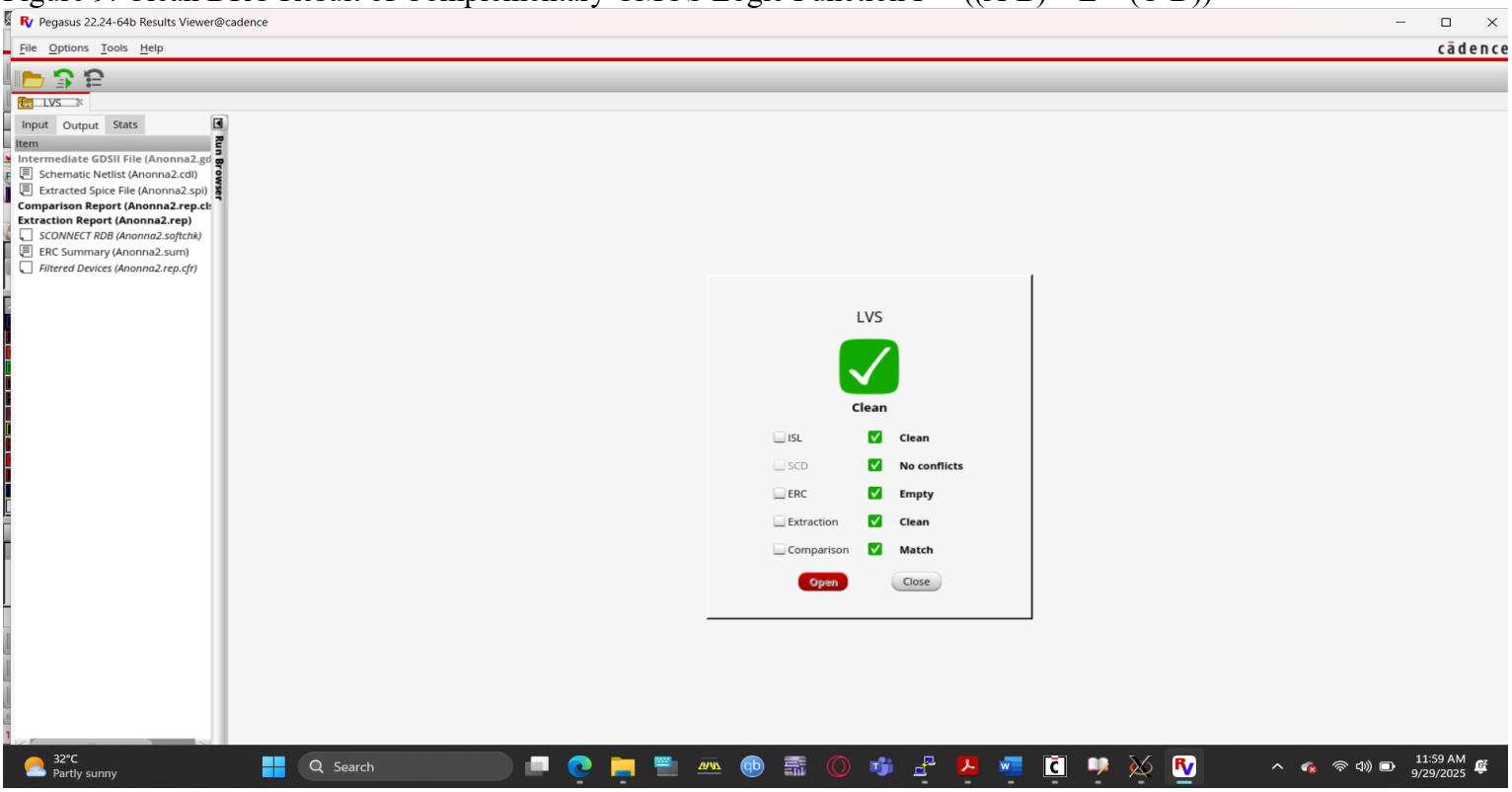


Figure 10: LVS Clean report of Logic Function F= ((A·B) + E + (C·D))' Showing Successful Net and Device Matching8. DRC and LVS Results

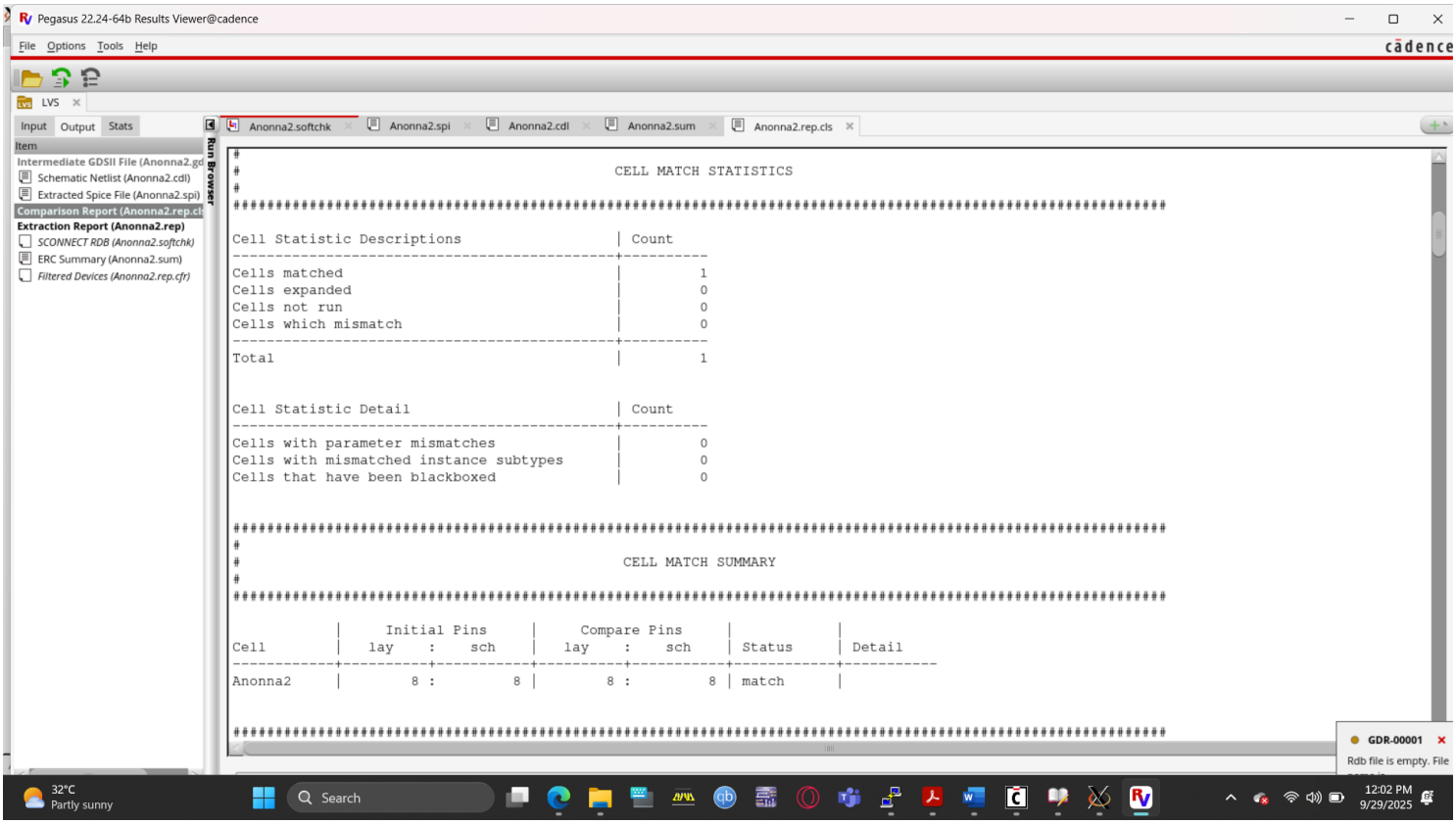
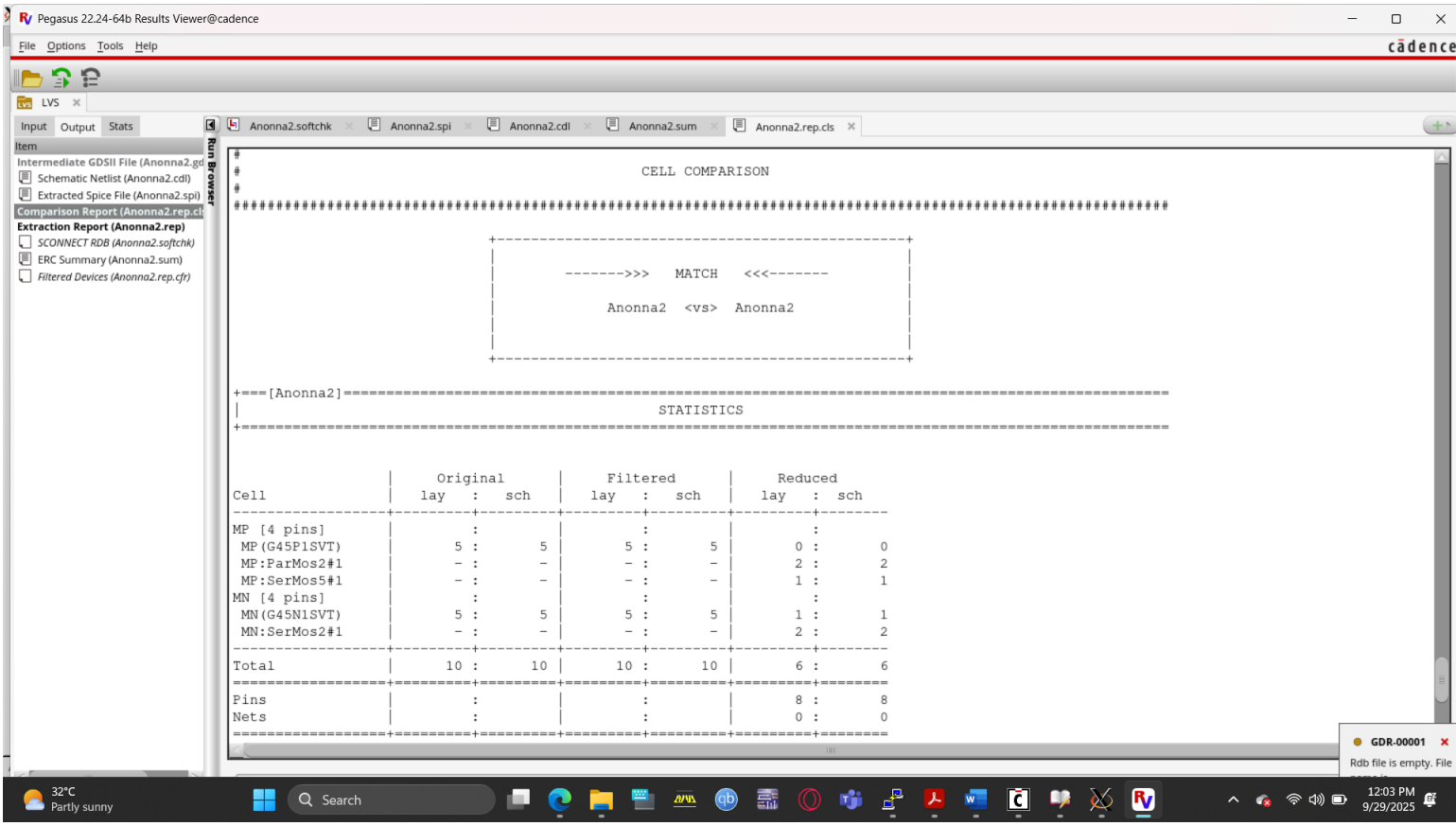


Figure 11(i): LVS Comparison Report (CELL MATCH STATISTICS) for Complementary CMOS



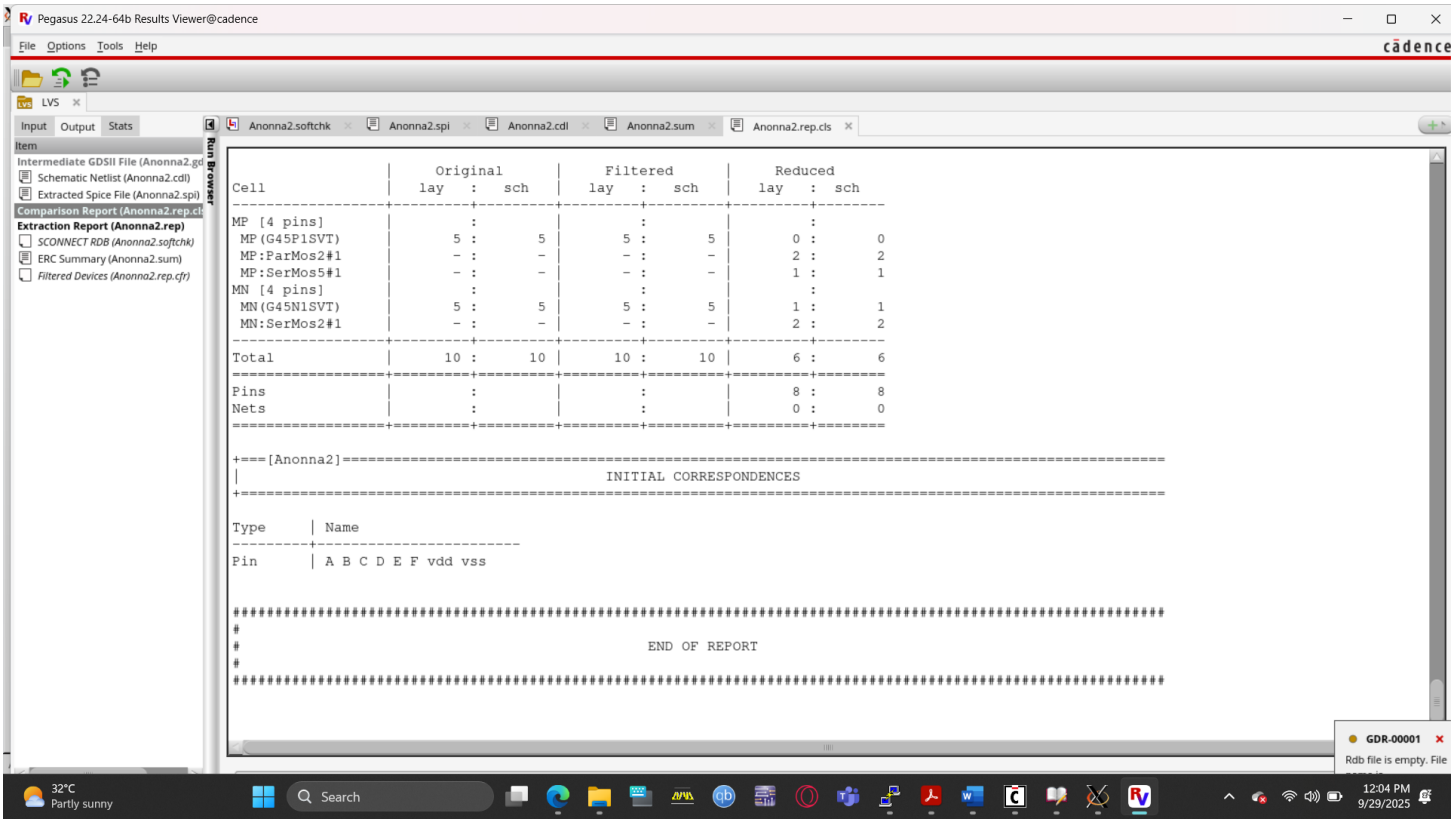


Figure 11(ii): LVS Comparison Report (CELL COMPARISON) for Complementary CMOS

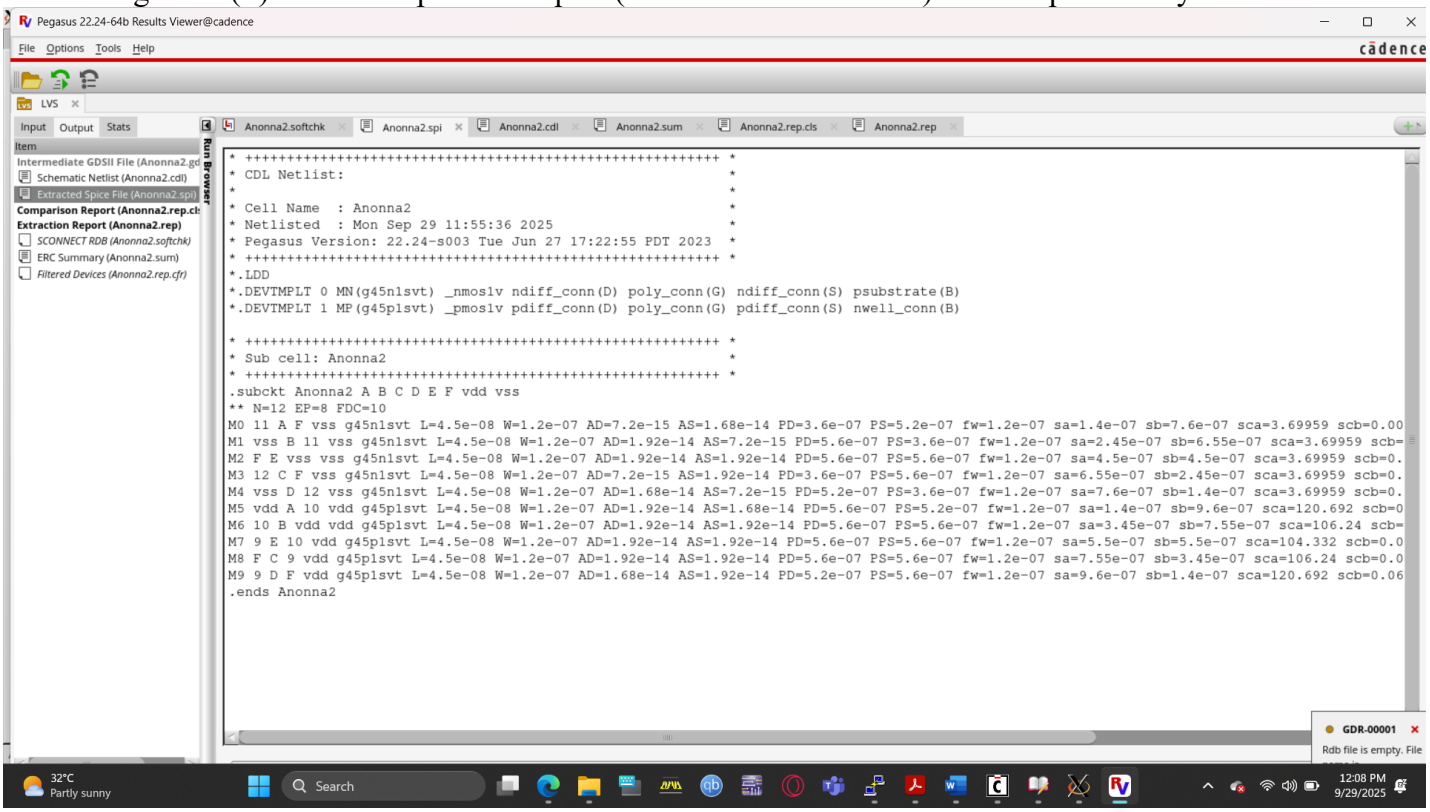


Figure 12: Extracted SPICE Netlist from LVS-Verified Layout for Logic Function F= ((A·B) + E + (C·D))'

Result Analysis:

Logic Function Under Test ,F= ((A·B) + E + (C·D))'

This is a NOR gate applied to three terms:

- Two AND operations: (A .B) and (C .D)
- One direct input: (E)

So, F is HIGH only when all three terms are LOW. If any one of them is HIGH, F goes LOW.

Simulation Setup Summary

- Tool: Cadence Virtuoso (ADE XL)
- Type: Transient analysis
- Inputs: A, B, C, D, E (digital square waves)
- Output: F, derived from the composite logic function

Input Behavior

Signal	Role	Effect on F
A, B	**AND pair**	**(A . B = 1) forces F LOW**
C, D	**AND pair**	**(C . D = 1) forces F LOW**
E	**Direct input**	**(E = 1) forces F LOW**

Each input is a square wave with a unique period, ensuring full coverage of input combinations over time. This allows you to observe every possible logical state that affects F.

Output Waveform F: Behavior and Integrity

- Voltage Levels: 0 V (LOW) and 1.8 V (HIGH)
- Transitions: Occur precisely when any of the three conditions become true
- F is HIGH only when:
  - (A . B = 0)
  - (C . D = 0)
  - (E = 0)
- F is LOW when:
  - Any one of the above evaluates to 1
- Waveform Quality:
  - No overshoot or undershoot
  - No glitches or metastability
  - Clean edges and stable logic levels

Transient Measurement of Logic Function:

Signal	Rise Time (tr) [ps]	Fall Time (tf) [ps]
A	5.999	5.999
B	5.999	5.999
C	5.999	5.999
D	5.999	5.999
E	5.999	5.999
F	5.287	28.95
CO/PULS	2.725	4.554

Figure 7 shows that the signals A, B, C, D, E, F, and CO/PULSE have similar rise and fall times. Signals A through E are around 5.999 ps. Signal F varies from 5.287 to 28.95 ps, and CO/PULSE ranges from 2.1725 to 4.554 ps. However, output F has an imbalance in its rise and fall times. This points to poorly sized transistors and mismatched pull-up and pull-down networks. Overall, the timing performance is not ideal. The circuit works within the constraints of 45nm CMOS technology, but it is not fully optimized for speed or signal quality.

Design Rule Check (DRC) Summary:

Figure 9 shows the results of the Design Rule Check (DRC) for the CMOS logic gate layout implementing the function F= ((A·B) + E + (C·D))'The DRC was performed using Pegasus DRC, which checks the layout against the design rules for the 45nm CMOS gpdk045 process. These rules include minimum feature sizes, layer spacing, contact enclosure, and well tap placements.

In this layout, we carefully positioned the NMOS and PMOS transistors, maintained enough space between polysilicon gates and diffusion areas, and kept n-well separate from p-substrate regions. We optimized the placement using an Euler path sequence (a-b-e-c-d) to minimize diffusion breaks and enable efficient routing with less area.

The DRC report showed zero violations in all checks, confirming full compliance with fabrication limits. No errors were found in critical parameters such as:

- Minimum metal width and spacing, which prevents shorts and ensures reliable signal transmission
- Correct poly-to-diffusion spacing
- Proper contact enclosure and overlap
- Appropriate well and substrate contact placements

This flawless DRC outcome confirms that the layout is manufacturable and free from errors that could lead to fabrication defects or circuit failures. It also verifies that the design is electrically sound and strictly follows physical design rules. Passing DRC is a key step in the VLSI design process, allowing us to move on to LVS verification and post-layout simulations with minimal risk of fabrication problems.

Layout Versus Schematic (LVS) Report:

Figure 10 shows the Layout Versus Schematic (LVS) results, an essential verification step in custom IC design. The LVS check ensures that the transistor-level netlist extracted from the layout matches the original schematic exactly in device count, connectivity, and terminal assignments. This verification was done with Pegasus LVS, comparing the schematic netlist from Virtuoso Schematic Editor XL against the layout netlist from Virtuoso Layout XL.

The report confirmed a perfect match between the schematic and the layout, with all devices, nets, and pins accurately identified. Specifically, all 10 transistors (5 PMOS and 5 NMOS) and their gate, drain, and source connections were correctly matched. The inputs (A, B, C, D, E) and the output (F) nodes were precisely linked between both views.

This clean LVS result certifies that the physical layout accurately implements the intended logic function and follows electrical rules. Such perfect LVS validation is crucial before moving on to post-layout simulation and fabrication since any discrepancies could lead to functional failures or incorrect behavior. Passing LVS without errors highlights the thoroughness and precision of the design process from schematic through layout.

LVS Cell Comparison Summary

Figure 11 shows a detailed cell-level device comparison performed during the LVS verification.This analysis examines the structural check at the finest level by matching each device in the layout with its equivalent in the schematic. In this project, the results confirm that each PMOS and NMOS transistor in the layout matches those in the schematic, including their width-to-length (W/L) ratios, source and drain connections, and gate assignments.

Additionally, the figure confirms the correct mapping of input and output pins for the logic function. Inputs A, B, C, D, and E, along with the output F, are properly positioned and connected in both the schematic and layout. The LVS tool also checked the design for any floating nodes or unconnected terminals and found none.

Passing this device-level LVS check confirms that the layout is a true and accurate physical representation of the schematic. With this verification complete, the design is ready for final post-layout simulation and the tape-out process.

Extracted SPICE netlist from the LVS-verified layout:

Figure 12 shows a part of the extracted SPICE netlist from the LVS-verified layout. This netlist includes key details for each transistor, like its type (NMOS or PMOS), dimensions (W/L), and terminal connections (gate, drain, source, and body). The extraction process also includes parasitic components such as interconnect capacitances (Cgs, Cgd, Cgb) and wire resistances. These are important for accurate timing and power analysis in post-layout simulation.

The netlist was used in post-layout transient simulations, providing a realistic view of the circuit's dynamic behavior by factoring in delays from routing and diffusion overlaps. Even with these parasitic effects, the output waveform of the circuit stayed stable and accurate. This confirmed the reliability of the layout's timing performance and overall design.

Additionally, the refined netlist extraction makes it easier to integrate into larger circuit systems or simulations with external elements. It supports hierarchical design flows. This step completes the design process, ensuring it is functionally sound and physically complete, with all layout-related effects included.

Conclusion:

In this project, we designed, simulated, and built the logic function,$F= ((A\cdot B) + E + (C\cdot D))'$ using complementary CMOS technology on the Cadence Virtuoso platform with a 45nm gpdk process. The design process followed a clear method. We started with transistor sizing and schematic creation, then moved through simulation, stick diagram development, layout creation, and ended with thorough verification using Design Rule Check (DRC) and Layout Versus Schematic (LVS).

Using Euler path optimization during stick diagram development helped create an efficient and manufacturable layout. Transient simulation results confirmed that the logical operation, signal integrity, and timing were accurate, both before and after considering parasitic effects from the layout. Clean DRC and LVS reports showed that the layout followed all electrical and fabrication rules, confirming that the design was ready for manufacturing.

Additionally, extracting the SPICE netlist after layout indicated that the circuit's performance remained strong despite parasitic effects. This project gave us valuable hands-on experience in the complete CMOS digital design process. We covered crucial stages like layout optimization, meeting fabrication constraints, and ensuring the schematic matched the layout. Overall, this work not only deepened our understanding of VLSI design principles but also provided us with practical skills needed for successful digital IC development in real-world applications.

References:

[1] American International University–Bangladesh (AIUB) VLSI Circuit Design Lab Manual.

[2] Neil Weste and David Harris. 2010. CMOS VLSI Design: A Circuits and Systems Perspective (4th. ed.). Addison-Wesley Publishing Company, USA.