DIGITAL ELECTRONICS (ECE 211) LAB MANUAL

3rd Semester (2020-21)

Department of Electronics and Communication Engineering

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List of Experiments

0. Realization of Basic Logic Gates

1. Design of Code Converters (Binary to Gray) & (Gray to Binary)

2. Design of

a) Half-Adder/Subtractor

b) Full-Adder/Subtractor

c) Multiplexers/De Multiplexers

d) ALU Design

3. Design of Decoder and Encoder/ BCD 7SSD

4. Design of Magnitude Comparator (2-bit)

5. Design and Verification of Flip-Flops using IC

6. Design of Asynchronous Counter (Any Mod, Up and Down, Jhonson and Ring)

7. Design of Synchronous Counter (Any Mod, Decade counter 74ls90)

8. Design of Universal Shift Register (Serial to Parallel, Parallel to Serial, Serial to Serial and Parallel to Parallel Converters)

9. Design & Verification of Memory (SRAM)

10. FSM Based Design Project.

EXPERIMENT 9

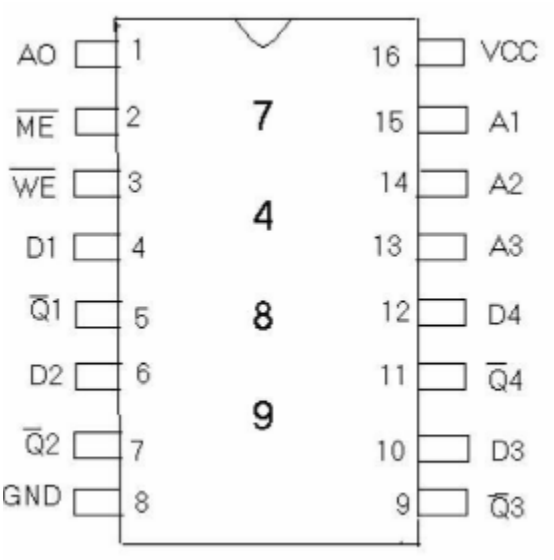
Design & Verification of Memory (SRAM) (16×4) - IC 7489

Aim: -
To study the operation of the RAM Ic7489.

Apparatus:

1. RAM IC 7489 Trainer kits.
2. Connecting wires.

Pin Diagram: -



Operation: -

• RAM IC 7489 is 16 words x 4-bit Read/Write Memory.

• The Truth Table for the RAM IC 7489 is given below.

Memory Enable	Write Enable	Operation
H	X	All data outputs are high
L	H	Read mode (data outputs are compliment of the RAM content).
L	L	Write mode (data inputs are written on to the memory; dataoutputs are compliment of the RAM content).

• The memory Enable pin is used to select 1- of-n ICs i.e. like a Chip Select signal. For simply city, the memory enable pin is permanently held low.

• The address lines are given through an up /down counter with preset capability.

• The set address switch is held high to allow the user choose any location in the RAM, using the address bits.

• The address and data bits are used to set an address and enter the data.

• The ‘Read/Write ‘switch is used to write data on to the RAM.

Procedure:

This experiment has 3 stages – Clearing the memory, data entry (Write operation) and data verification (Read operation).

Clearing the Memory: -The RAM IC 7489 is a volatile memory. This means that it will lose the data stored in it, on loss of power. However, this dose not means that the content of the memory becomes 0h, but not always. The RAM IC 7489 does not come with a ‘ Clear Memory ‘ signal.

The memory has to be cleared manually.

1. Position the ‘Stack/Queue’ switch in the ‘Queue’ position.

2. Position the ‘Set Address’ switch in the ‘1’ position.

3. Set the address bits to 0h (first byte in the memory)

4. Position the ‘Set Address’ switch in the ‘0’ position to disable random access and enable the counter.

5. Position the’ Read/Write ‘switch in the’ Write’ position to write data on to the memory.

6. Set the data bits to 0h (clearing the content)

7. Observe that the LEDs (D3 to D0) glow. This is to indicate that the content is 0h. Refer the truth table above and observe that the data outputs of the RAM will be compliments of the data inputs.

8. Position the ‘Increment/Decrement ‘switch in the ‘Increment’ position.

9. Press the ‘Clock’ to increment the counter to the next address. As the ‘Read /Write ‘ switch is already in the ‘Write’ position, and the data bits are set to the 0h, the content in the new location is also replaced with 0h.

Write Operation: -

1. Assume that the following data has to be written on to the RAM. The address and data are given in the hexadecimal format.
2. Position the ‘Stack/Queue’ switch in the ‘ Queue ‘position.
3. Position the’ Read/Write ‘switch in the’ Write’ position to enable the entry of data in to the RAM.
4. Position the ‘Set Address’ switch in the ‘1’ position to allow random access of memory.
5. Set the desired address (any address at random) using the address bit switches.
6. Set the desired data (refer table for the data to be entered in each location) using the data bit switches.
7. Observe that the data is indicated by the LEDs (D3 toD0). This is because the data is written on to the RAM.
8. Also observe that the data is indicated by the data outputs is the compliment of the data input (refer truth table condition ME =L and WE=L).

Address	Data
0h - 0000	Ah - 1010
1h - 0001	Bh - 1011
2h - 0010	4h - 0100
3h - 0011	7h - 0111
4h - 0100	Ch - 1100
5h - 0101	1h - 0001
6h - 0110	Fh - 1111
7h - 0111	5h - 0101
8h - 1000	8h - 1000
9h - 1001	3h - 0011
10h - 1010	Eh - 1110
11h - 1011	9h - 1001
12h - 1100	Dh - 1101
13h - 1101	0h - 0000
14h - 1110	2h - 0010
15h - 1111	6h - 0110

9. After each data entry, make a note of the location where data is entered. This is to make sure that we are not re –entering data in the same location.

10. Repeat steps 4 and 5 until data has been entered in all the addresses listed in the above table

11. Position the' Read/Write 'switch in the' Read' position, to disable data entry.

12. This completes data entry.

Read Operation: -

1. Position the 'Stack/Queue' switch in the 'Queue' position.

2. Position the 'Set Address' switch in the '0' position to allow random access of memory.

3. Position Read/Write 'switches in the' Read' position, to disable unauthorized entry of data.

4. Set the desired address (any address at random).

5. Observe that the data entered in the location is indicated by the LEDs (D3 toD0).
This is because the data was written during the data entry procedure.

6. Also observe that the data indicated by the data out puts is the compliment of the data input (refer truth table condition ME=L and WE=H).

CONCLUSION: