*Design of area-efficient approximate 4-2 compressor*

R.Suburaaj   
Mtech VLSI Design  
VIT UniversityVellore,India  
suburaaj96@gmail.com

Annamalai   
Mtech VLSI Design  
VIT UniversityVellore,India  
annamalai12578@gmail.com

Dr.V.Nithish Kumar  
Assistant Professor  
School of Electronics EngineeringVIT University  
nithishkumarv@vit.ac.in

*Abstract*— Approximate computing is a very productive approach to gain improvement in delay, power and area requirement of a circuit with increased error outputs. This paper provides a design on 4-2 compressor. Functional Verification is simulated along with total power and delay using Cadence Virtuoso. The result gives a significant reduction in area, power and delay requirements.

Keywords— Approximate computing, Compressor

# Introduction

Digital logic circuits plays an important role in recent electronic gadgets under various applications involving Digital Signal processing. Fast processing Arithmetic circuits involving addition and multiplication are popularily used in computating convolutions and filtering based applications. Various approximate adders and multipliers along with various metrics of approximate computing are discussed in [1], [2]. Exact 4-2 compressor is implemented using 80 transistors by Static CMOS logic and various low power 4-2 and 5-2 compressors are discussed in [3] .

This paper proposes an approximate low power 4-2 compressor with considerable decrease in total delay. Section 2 deals with existing low power compressor proposed in [4] and Section 3 deals with proposed low power 4-2 compressor. Section 4 elaborates the simulation results .Conclusion is provided in Section 5.

# EXISTING 4-2 COMPRESSOR

## Reference [4] proposed a 4-2 Compressor as shown in Fig.1.The sum and carry equations respectively are

sum = (1)

carry = (2)

Various approximate compressors are also proposed in [5],[6].Truth Table of the existing approximate compressor is shown in Fig.1.Logic Diagram of the above expressions is shown in Fig.2

TABLE1: TRUTH TABLE of 4-2 Compressor

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| A | B | C | D | CARRY | SUM | DIFFERENCE |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 1 | 0 | 1 | -1 |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 0 | 1 | 0 |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| 1 | 0 | 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | 0 | 1 | -1 |
| 1 | 1 | 0 | 1 | 1 | 1 | 0 |
| 1 | 1 | 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 1 | 1 | 1 | 1 | -1 |

Fig.1

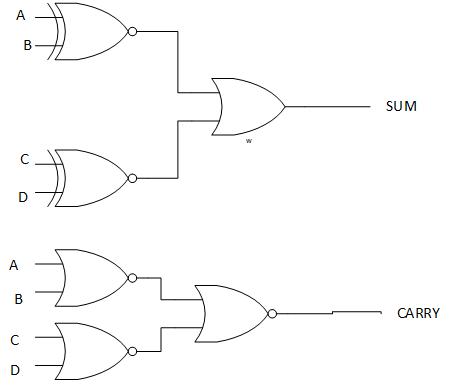


Fig.2

4 Incorrect outputs are found out of 16 output combinations. The error rate is 25%.

# PROPOSED 4-2 COMPRESSOR

The sum expression in [(1) utilizes EX-NOR gate, which accounts for more area, power and delay in the circuit. Hence, a NOR gate can used since it gives 3 out of 4 outputs matching the EX-NOR gate. No change in carry expression so that the circuit can be still optimized, making it complement to sum. The optimized sum and carry expressions are

= (3)

= (4)

Truth Table of the proposed approximate compressor is shown in Fig.3.Logic Diagram of the above expressions is shown in Fig.4.

TABLE2: TRUTH TABLE of PROPOSED 4-2 COMPRESSOR

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  |  |  |  |  |  |  |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 1 | 0 | 1 | -1 |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 | 1 | 0 | -1 |
| 1 | 0 | 0 | 0 | 0 | 1 | 0 |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| 1 | 0 | 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | 1 | 0 | -1 |
| 1 | 1 | 0 | 0 | 0 | 1 | -1 |
| 1 | 1 | 0 | 1 | 1 | 0 | -1 |
| 1 | 1 | 1 | 0 | 1 | 0 | -1 |
| 1 | 1 | 1 | 1 | 1 | 0 | -2 |

Fig.3

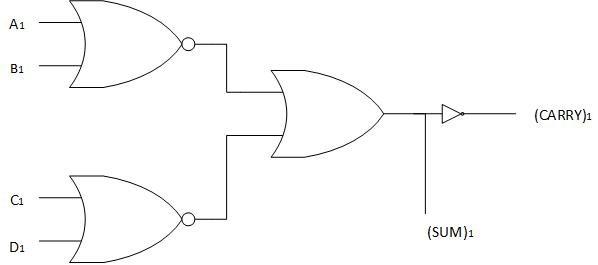


Fig.4

8 incorrect outputs are found out of 16 outputs. The error rate is 50% due to approximations in logic of the circuit.

# SIMULATION RESULTS

The proposed approximate 4-2 compressor is implemented using Static CMOS Logic with Cadence Virtuoso in 180nm library. Functional Verification is done and verified with truth table. Power Consumption and Delay are simulated and compared with existing technique as shown in Table 2 and Table 3 respectively. Number of transistors are also compared in Table 4.

TABLE 2: COMPARISON OF POWER VALUES

|  |  |  |
| --- | --- | --- |
|  | (W) | (W) |
| Existing Model | 7.572 × | 155.29× |
| Proposed Model | 1.32× | 65.35× |

TABLE 3: COMPARISON OF DELAY VALUES

|  |  |
| --- | --- |
|  | Delay (s) |
| Existing Model | 67 × |
| Proposed Model | 52.59× |

TABLE 4 COMPARISON OF NO. OF TRANSISTORS

|  |  |
| --- | --- |
|  | No of transistors used |
| Existing Model | 32 |
| Proposed Model | 10 |

From the table 2, the total power consumption is reduced to 40.79% of the existing model power.

From table 3, the total delay is reduced to 78.4% of the existing model delay. From the table 4, the transistor count is reduced to 31.25% of the existing model transistors requirement. Therefore, the proposed model can be used in applications where the high error rate can be tolerated because of low power, delay and area requirements.

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