DESIGN OF LOW POWER SINGLE-ENDED 6T SRAM ARCHITECTURE

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Abstract— In this paper we implement a low power 8 X 8 Single-Ended 6-T SRAM Architecture compared to the existing architecture.

Keywords— SRAM, Single-Ended, Low Power

I. INTRODUCTION

Previously proposed low power architectures are mentioned as follows. Authors have used conventional 6-T SRAM with different total area for depending upon the position of the bits present in the pixel ,where more area is allocated for MSB when compared to LSB [1]. This is due to the fact that more area per bit cell reduces the Bit-Error Rate (BER) [1].An array involving both 10-T and 8-T SRAM cells reduces the total active power consumed , and a Split-data-aware (SDA) technique improves the write margin and write power efficiency [2].The 6-T SRAM architecture uses three different supply voltages for improving SNM during read and write operation and reduce the leakage current during the retention mode [3].A Write-assist cell along with virtual ground biasing scheme increases the read and write SNM ratio and improves the speed of operation [4].A Hybrid SRAM array involving both conventional 6-T and 8-T SRAM cells are used in pixel, where the first half of the pixel is filled with conventional 8-T SRAM cells and second half is filled with conventional 6-T SRAM cells [5]. But, the read and write peripheral circuits become complex since the 8-T SRAM has an unique read-decoupled structure [5].

The paper has been organized as follows. Section II explains about the implementation of existing 8 X 8 Single-Ended 6-T SRAM Architecture. Section III explains about the modified low power 8 X 8 Single Ended 6-T SRAM Architecture. Section IV provides details on simulations and results obtained using Cadence Virtuoso.

II. EXISTING ARCHITECTURE

Single-Ended 6-T SRAM is used as a basic block in this architecture, which is proposed in [6]. Single 6-T SRAM Cell requires one Word Line and one Bit Line for Read and Write operations respectively [6].This reduces the power consumption to nearly 50% compared to Conventional 6-T SRAM Cell [6]. In order to improve the write margin, PDL should always be in cut-off region so that gate terminal should be tied to the ground [6]. But this decreases hold-0 margin. Hence, PDL is made as low threshold voltage transistor, channel length of PUL is made high and WBL is off to improve the hold-0 margin.
The Single-Ended 6-T SRAM cell is shown in fig.1

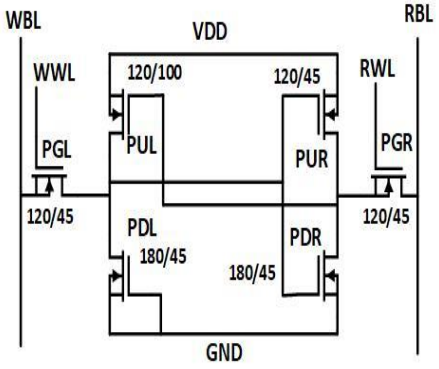

Fig-1 Single Ended 6-T SRAM cell [6]

The Single Ended 6-T SRAM Architecture is shown in fig.2.

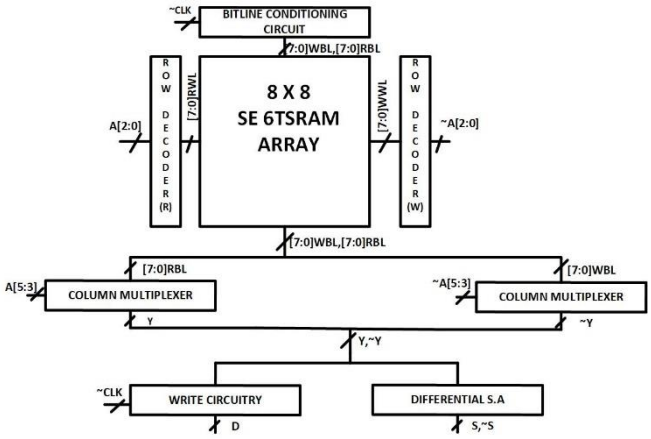

Fig.2 Existing architecture [6]

The two 3 X 8 Row decoders, (one for Read(R) and one for Write (W)) is shown in fig.3 .The AND gates present in 3 X 8 row decoder is based on Pseudo-NMOS logic is shown in fig.4.

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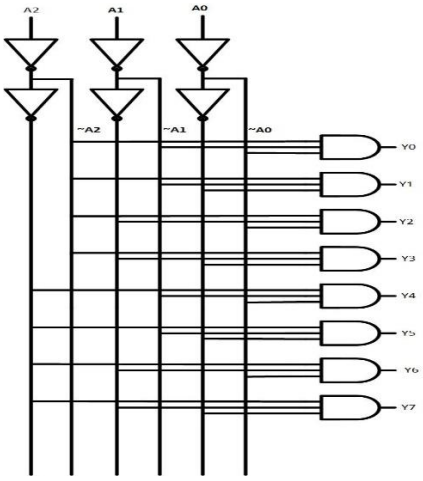

Fig.3 Row Decoder [7]

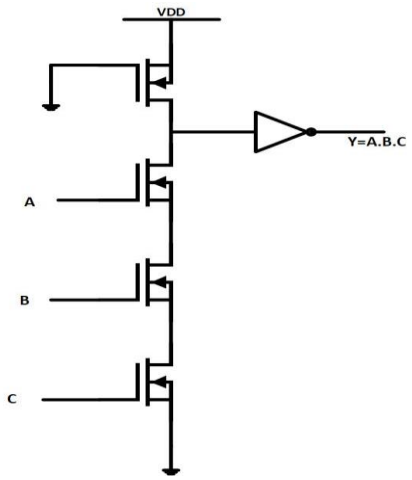

Fig.4 Pseudo –NMOS 3-input AND gate

These Row Decoders are used to connect all their respective word lines ([7:0] RWL, [7:0] WWL]) present in the Single-Ended 6-T SRAM array .The Address Bits A [2:0] and ~A [2:0] are the input to Row Decoders (R) and (W) respectively. Since the Bit Lines need to be pre-charged during Read and Write operations, the Bit-line conditioning circuit (as shown in fig.5) is connected to [7:0] WBL and [7:0] RBL respectively and is enabled using ~CLK.

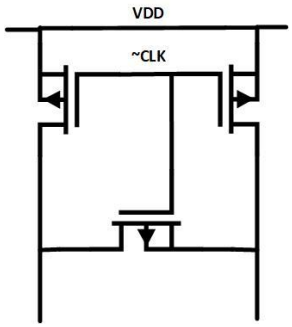

Fig.5 Bit-line conditioning circuit [7]

Also the two column Multiplexers (shown in fig.6) are connected to [7:0] WBL and [7:0] RBL and they are connected to inputs A [5:3] and ~A [5:3] respectively.

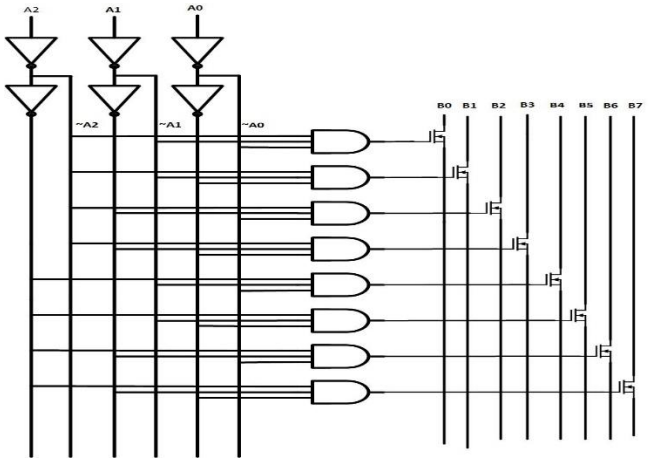

Fig.6 Column Multiplexer [7]

Their outputs ~Y and Y are connected to output pins of Write circuitry and input pins of Differential Sense Amplifier (as shown in fig.7). D is connected as input pin to write circuitry and it is controlled by clock input ~CLK. S and ~S are connected to the output pins of the Differential Sense Amplifier (as shown in fig.8). ~CLK is the complement of CLK signal respectively.

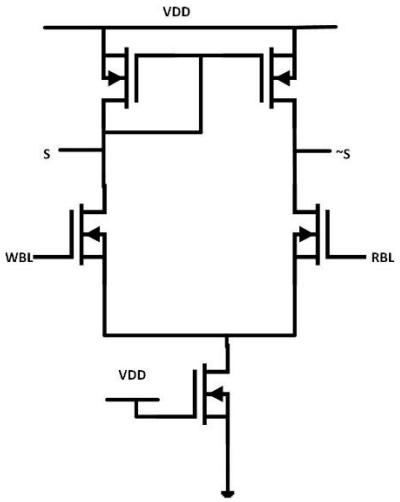

Fig.7 Differential Amplifier [7]

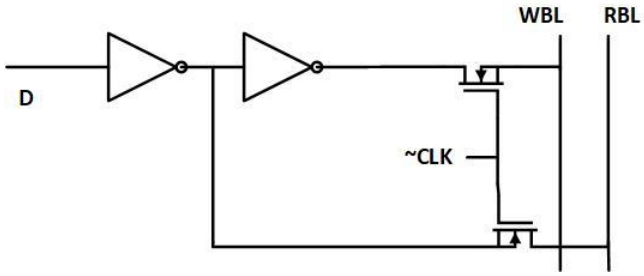

Fig.8 Write Circuitry

III. MODIFIED ARCHITECTURE

The 8 X 8 Single-Ended 6-T SRAM modified architecture is shown in fig.9

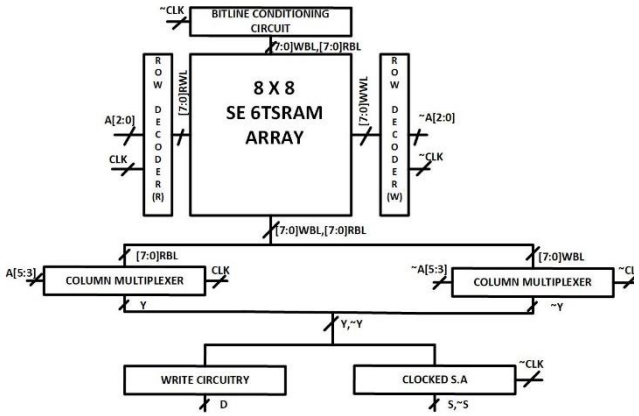

Fig.9 Modified Architecture

The two 3 X 8 Row decoders (one for Read(R) and one for Write (W)) consist of Dynamic-AND gates and are controlled by CLK and ~CLK respectively .

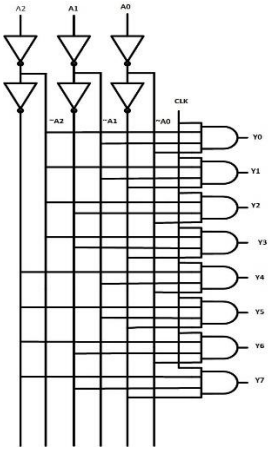

Fig.10 Modified Row Decoder

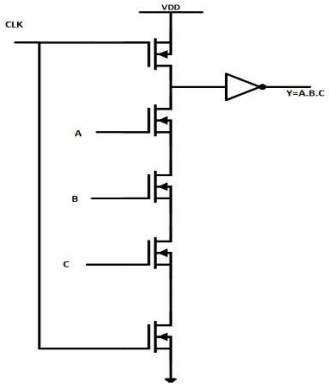

Fig.11 3-input AND gate using Dynamic Logic

Also, the two column multiplexers consist of Dynamic-AND gates and are controlled by CLK and ~CLK respectively.

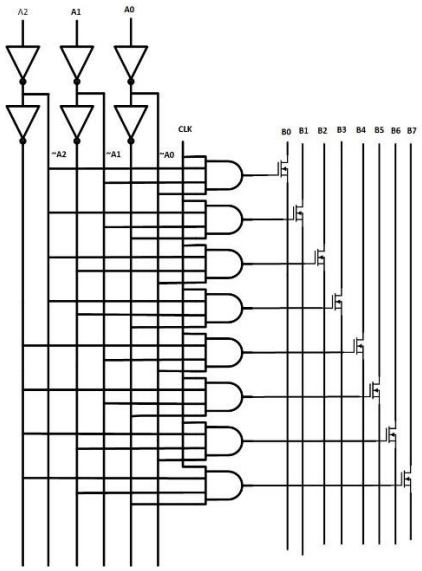

Fig.12 Modified Column Multiplexer

Clocked Sense Amplifiers are used instead of Differential Sense Amplifiers and it is controlled by ~CLK (shown in fig.13).

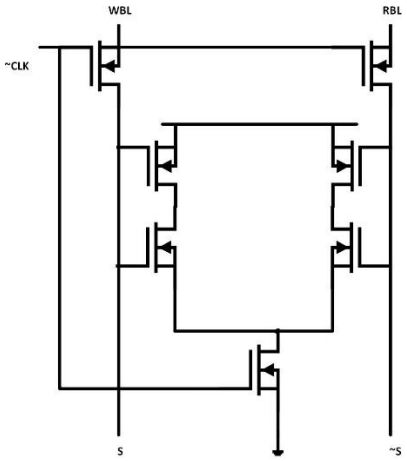

Fig.13 Clocked Sense Amplifier [7]

IV. RESULTS

The Existing and Modified Architecture is implemented with Cadence Virtuoso using GPDK 45nm library. The supply voltage is 0.45 V. The Power consumed by existing Single-Ended 6T SRAM Architecture is 557.3nW.This Power is the sum of read and write operations carried out in all the cells present in the Architecture. Power Consumed by the modified Single-Ended 6T SRAM is 339.9nW.

Architecture	Power Consumed(nW)
Existing	557.3
Modified	339.9

Hence, the Total Power consumed is reduced using modified Architecture.

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