ECE6025 LOW POWER IC DESIGN

PROJECT REPORT

By

AJINKYA SURESHRAO KAUTIKWAR (Reg. No.: 18MVD0061)

SUBURAAJ R (Reg. No.: 18MVD0072)

ANNAMALAI S (Reg. No.: 18MVD083)

Low Power High Speed Dynamic Comparator

M.Tech VLSI Design

Winter Semester 2018-2019

SCHOOL OF ELECTRONICS ENGINEERING

VIT UNIVERSITY

VELLORE-632014, TAMIL NADU, INDIA

MARCH 2019

Introduction:

High speed low power comparators plays an important role in the present high speed analog-to-digital converters (ADCs). Designing High speed comparator is challenging as reducing the channel length of the MOSFET leads to reduction in dynamic power, but increase in leakage power is a major issue in reducing the performance of the comparator.

Previous proposed Comparators:

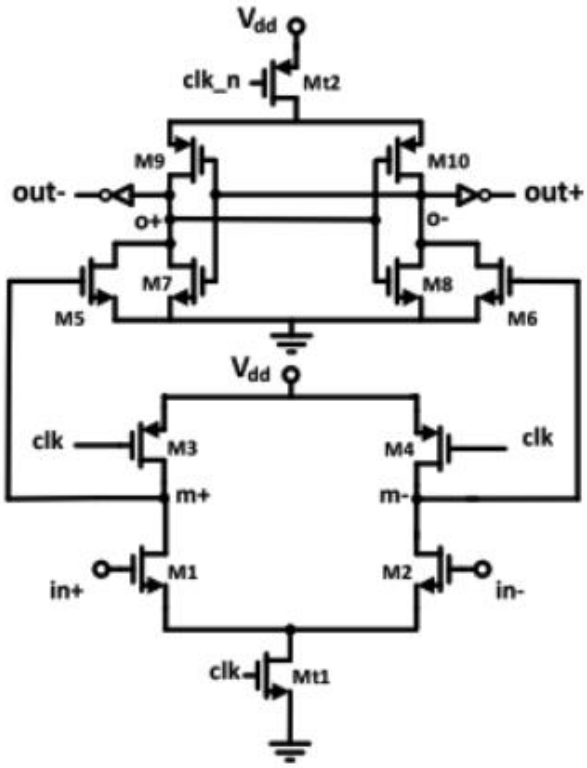

Fig.1 Conventional Double Tail Comparator

- Known as Conventional Double Tail Comparator
- During reset phase(clk=0),M_{t1} and $\mathrm{M_{t2}}$ - OFF; M_3 and $\mathrm{M_4}$ - ON charges m+ and m- to V_{DD} and o+ and o- to GND .9003559859
- During latching phase(clk=Vdd), M_{t1} and $\mathrm{M_{t2}}$ - On, and m+ and m- is pulled to gnd.
- Voltages at m+ and am- depends on the differential input voltage
- When Vin+ >Vin-,o+ is logic 1 and o- is logic 0 respectively.

- Advantages: less stacked transistors, and hence operates at low voltages. Low Offset and High Speed.
- Dis-Advantage: Comparator offset is sensitive to input Vcm variations

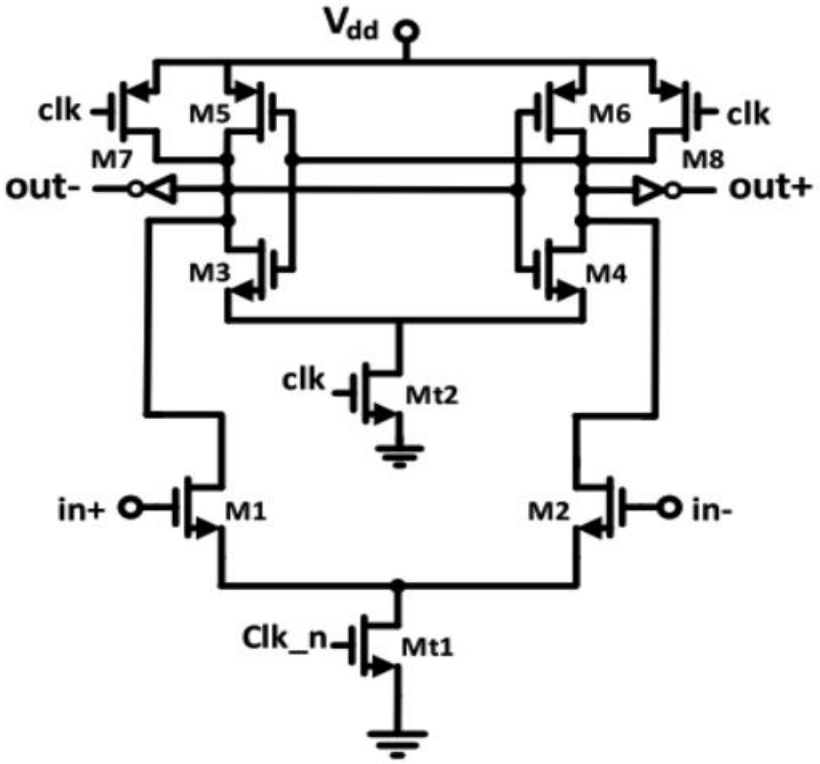

Fig.2 Comparator [2]

- Amplification Phase(clk=0): M_{t1} is ON;M_7 and M_8 are ON;
- When in+>in-,Va+ is pulled to ground at faster rate than Va-.
- Vout+ and Vout- is equal to Va+ and Va- since it is separated in-between by two inverters respectively
- Latching Phase(clk=V_{DD}): M_{t1}, M_7 and M_8 -OFF ;M_{t2}=ON and M_{3-6} cross coupled inverters starts regeneration
- Dis-Advantage: Since a+ and a- are connected to the latching nodes of the cross-coupled inverters the load capacitance increases and hence reduces speed.Static Power dissipation is also present

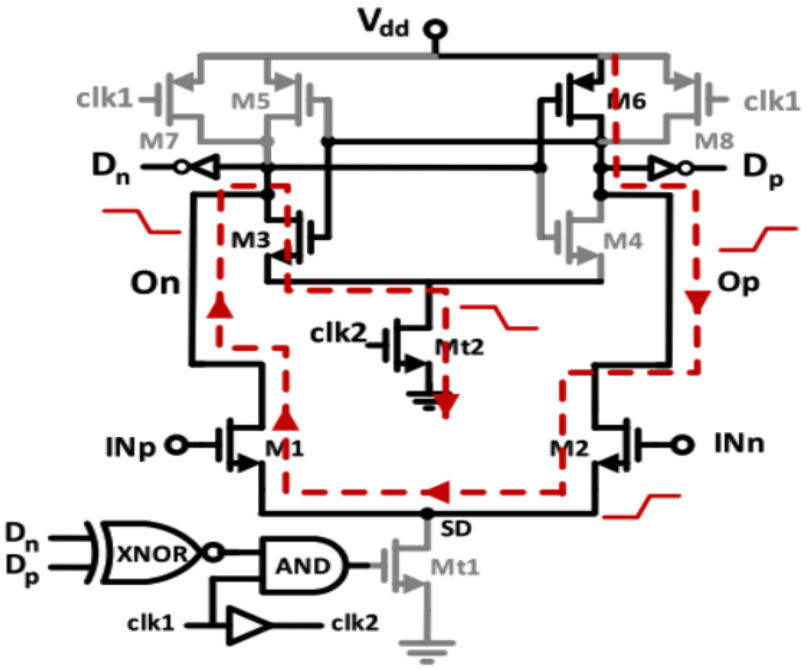

Fig.3 Comparator [4]

- clk2 is delayed signal of clk1.
- Reset Phase:clk1,clk2=low; M_7 and M_8 -ON and pulls o-and o+ to Vdd and hence Dp and Dn to gnd
- Latching Phase: when clk1=high ,M_{t1}-ON and pulls o- and o+ to gnd; when clk2 =high, regeneration occurs as cross-coupled inverters are pulled depending in+ and in-.The outputs D_n and D_p turns off M_{t1} through XNOR and AND gates to avoid static power dissipation.
- Dis-advantage: The outputs of M1 and M2 is directly connected to the nodes o- and o+ increase capacitance and reduces the speed
- A hidden static current path exists in the latching phase, which significantly impacts the power and speed of comparator.

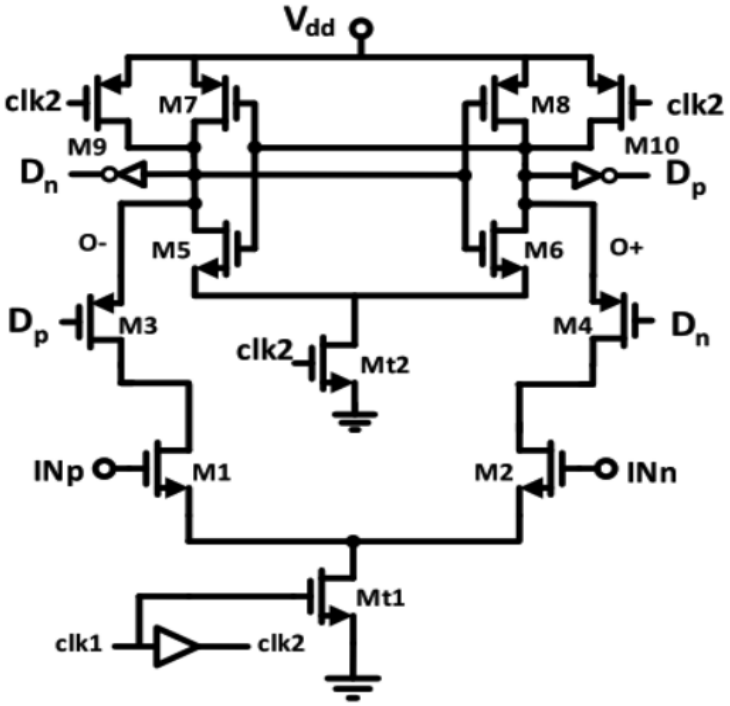

Fig.4 Dynamic Comparator

- Reset phase(clk=0):clk1 and clk2 – low; M_{t1}, M_{t2} – off; M_9, M_{10} charge the o+ and o- nodes to V_{dd}. Also, M_3 and M_4 - ON and the a+ and a- is pulled up to V_{dd}
- Latching phase(clk=Vdd):M_3 , M_4 -on and M_{t1} will be turned on, and hence o- and o+ is pulled to gnd.
- As soon as clk2 goes to high, the regeneration starts as the outputs Dn and Dp of cross-coupled inverters are pulled depending on inp and inn.
- After the decision is made, M_3 and M_4 is OFF and static power dissipation is zero.
- Advantages: Load Capacitance is reduced:No static power dssipation due to hidden current path

Modified Low Power High Speed Dynamic Comparator:

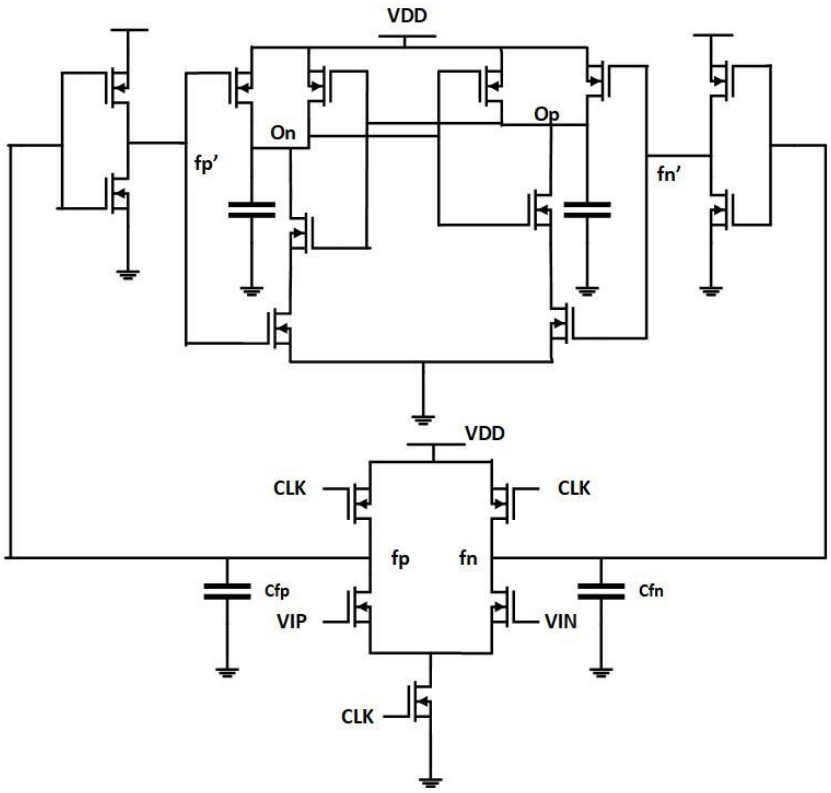

Fig.5 Modifed Comparator using NAND Latch

- During precharge or Reset phase(CLK = 0), M5-OFF and hence no static power dissipation due to absence of current flow from Vdd to gnd.
- M1,M2-ON and hence Vfn and Vfp is pulled to Vdd, and hence the output of both inverters Vfp' and Vfn' becomes zero.
- Hence M10,M11 is ON and output nodes are pre-charged to Vdd.
- During comparison or decision making phase(CLK=Vdd), M1,M2-OFF and M5-ON and hence the pre-charged Capacitor voltage Cfp and Cfn are discharged from Vdd to ground.
- Discharge rates depend upon the input voltages applied VIP and VIN.
- When VIP >VIN ,VOP becomes logic '1' and VON becomes logic '0'.

Advantages of NAND Latch:

If the inputs s' and r' of NAND latch circuit are kept at logic 1 then the output will have no change/transition. Therefore, power consumption will reduce.

Only one clock pulse is enough to complete both reset and latching phase, which reduces delay and saves power.

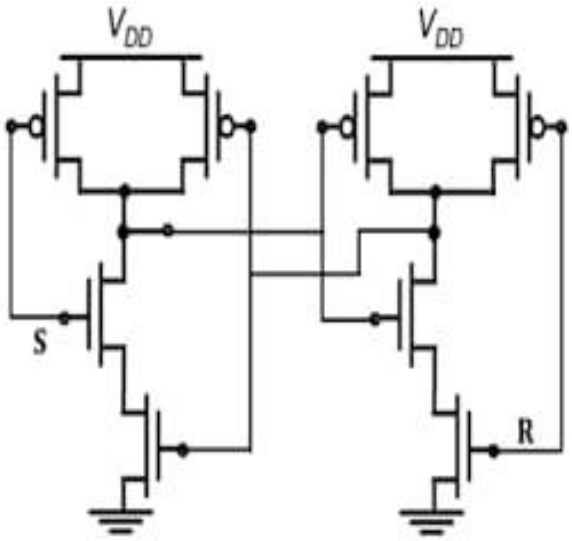

Fig.6 NAND Latch Circuit

Result:

The existing and the modified Comparators are simulated in Cadence Virtuoso using GPDK 90nm library. The Average Dynamic Power is tabulated below. The Operating Frequency is 4GHz .The rang of supply voltage provided is 0.8-1V.

	Average Dynamic Power
Existing Dynamic Comparator	29.58uW
Modified Comparator	1.59uW

Hence, the reduction in power has been obtained using Modified Comparator.