IMPLEMENTATION OF CORDIC ALGORITHM

ECE5014 ASIC DESIGN LAB REPORT

SLOT : L49+L50

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1. Abstract

CORDIC algorithm are used in various image processing application oriented algorithms like Direct Cosine Transform (DCT), GABOUR filter, FFT etc. They are used in finding Legendre Polynomial, which plays a major role in space applications and even in 3G and 4G Communication systems. This paper focusses on implementation of CORDIC algorithm based on 32-bit Pipelined Architecture under rotational mode of operation.

Keywords: CORDIC, Pipe-lined, rotational mode

2. Literature Review

CORDIC Algorithm can be realized using 8 Bit Parallel Architecture configuration [1].But, the dis – advantages faced with this is the number of iterations is proportional to precision. Hence, this architecture is not suitable for High-Speed applications

Also, Scale Factor Problems includes Scale-free CORDIC based on Taylor approach, on Radix-4 Modified Booth Recording- Modification of CORDIC algorithm, leading one bit detection technique, Domain folding elimination are dominant in implementation of CORDIC Algorithm [2].Usage of Constant Multiplier creates a heavy hardware problem [2].

Also, we can use two arc-tan look up tables, one in degree and the other in radians respectively [3].Also, we may determine the Cartesian co-ordinates of a complex number represented in Euler's form r. $e^{i\theta}$ [3].But ,this may increase the complexity of the algorithm and depends on the application where it is used.

Also, we can use Residue Number System for the internal Computation [4].But the disadvantage we face is conversion of two's complement number to residue number system.

Also, the CORDIC Algorithm is used to implement the butterflies instead of constant Multiplers [5].This reduces the need for more Look –Up Tables and increases the Signal to Noise ratio by 25db.

Hybrid Architecture can also be used for CORDIC Algorithm [6].Hybrid architecture decomposes the initial angle of rotation into two angular sets [6]. One angular set is input to the parallel architecture CORDIC processor [6]. The second processor does not use LUTs and takes decision on the basis of bits of the angular set input to it thus, saves time and increases computation speed [6].

Also, we can implement the Fourier transform using CORDIC algorithm [7]. Also, orthogonal frequency division multiplexing can be done by the method of encoding digital data on multiple carrier frequencies in CORDIC Algorithm [8].By making use of this approach, area reduction is achieved by replacing adders in 4 stages of sine and cosine blocks with MUXs [8].

Also, we can introduces angle recording (ARD) and scaling free (SCFE) CORDIC algorithms [9].Also,one may use ADPLL system phase detection system has been realised by generating a signal using Hilbert transform and calculating the instantaneous phase using CORDIC algorithm [10].The aim is to achieve a more efficient PLL with faster lock time [10].

Extension to CORDIC Algorithm with Polar to Rectangular Transformation and vice versa, inverse CORDIC functions, Linear and Hyperbolic Functions are discussed [11]. Processors like Iterative and Parallel architecture are discussed [11].

3. Block Diagram of Architecture

- Three adder/subtractor with di as control signal is required per iteration
- The result of every iteration enters into the pipelined register leads to high throughput.
- Improvement of the angle by one bit per iteration.

$$x^{i+1} = K_i[x^i - y^i d_i 2^{-i}]$$

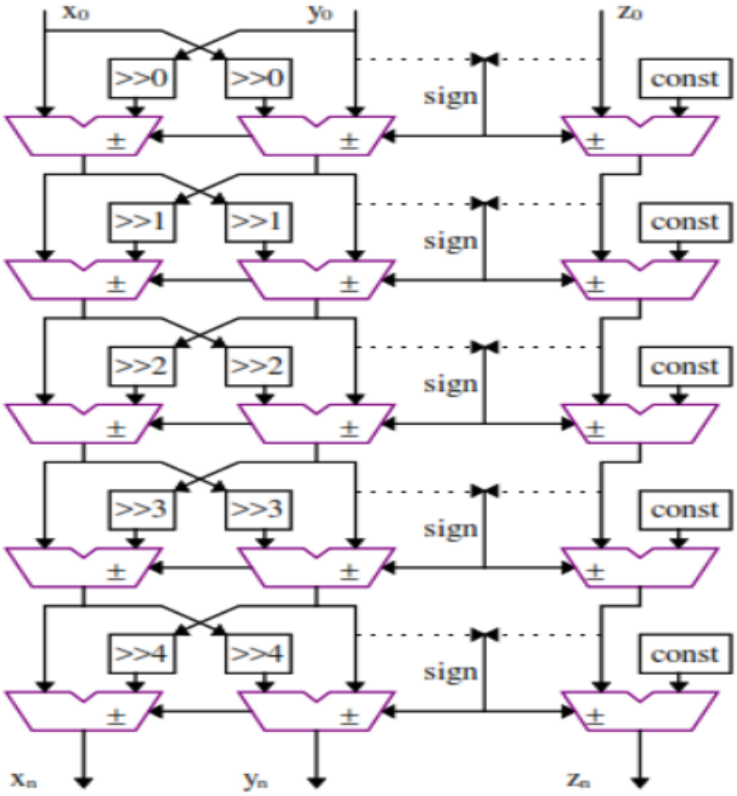
$$y^{i+1} = K_i[y^i + x^i d_i 2^{-i}]$$

$$z^{i+1} = z_i - d_i tan^{-1}(2^{-i})$$

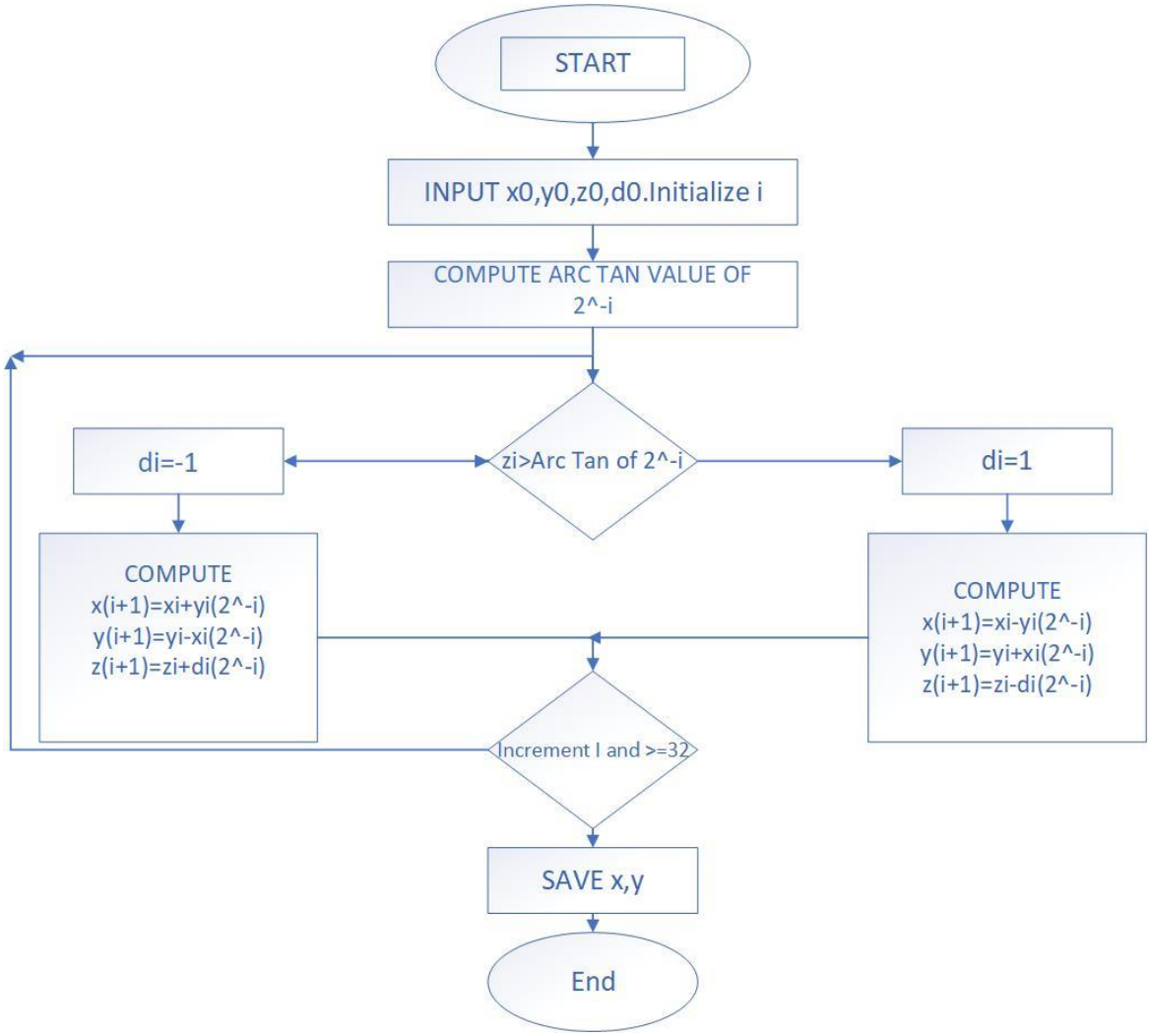
where $K_i = \prod_n(1/cos\Theta^{(i)}) = \prod_n(\sqrt{1 + 2^{(-2i)}})$

where n is total number of iterations. Thus if n value is known, then scaling factor can be pre-computed and then final values x^n and y^n can corrected by $(1/K_i)$. In circular rotation mode ,start the algorithm by considering $x^{(0)} = (1/K_n)$ and $y^{(0)} = 0$.

- $tan^{-1}(2^{-i})$ are pre-computed and scaled in binary range
- $d_i = \begin{cases} -1 & if\ z_i < 0 \\ +1 & otherwise \end{cases}$
- z_i is evaluated by using the sign bit.



4. Methodology



5. RTL Code With Test Bench

CORDIC.v

```
`timescale 1 ns/100 ps

module CORDIC (clock, angle, Xin, Yin, Xout, Yout);

   parameter XY_SZ = 16;

   localparam STG = XY_SZ;
```

```
input                       clock;
input  signed       [31:0] angle;
input  signed  [XY_SZ-1:0] Xin;
input  signed  [XY_SZ-1:0] Yin;
output signed    [XY_SZ:0] Xout;
output signed    [XY_SZ:0] Yout;
wire signed [XY_SZ:0] X [0:STG-1];
wire signed [XY_SZ:0] Y [0:STG-1];
wire signed    [31:0] Z [0:STG-1];

wire  signed [1:0] quadrant;
assign   quadrant = angle[31:30];
reg signed [16:0] temp_xin;
reg signed [16:0] temp_yin;
reg signed [31:0] temp_z;
always @(posedge clock)
begin
   case (quadrant)
      2'b00,
      2'b11:
      begin
         temp_xin  <= Xin;
         temp_yin <= Yin;
         temp_z <= angle;
      end

      2'b01:
      begin
       temp_xin <= -Yin;
         temp_yin <= Xin;
      temp_z <= {2'b00,angle[29:0]};
      end

      2'b10:
      begin
         temp_xin <= Yin;
         temp_yin <= -Xin;
        temp_z <= {2'b11,angle[29:0]};
      end

   endcase
```

```
   end
    assign X[0] = temp_xin;
    assign Y[0] = temp_yin;

    assign Z[0] = temp_z;


   genvar i;

   generate
   for (i=0; i < (STG-1); i=i+1)
   begin: XYZ


      sub
c1(.clock(clock),.x_in(X[i]),.y_in(Y[i]),.angle_in(Z[i]),.k(i),.angle_out(Z[i+1
]),.x_out(X[i+1]),.y_out(Y[i+1]));
   end
   endgenerate

   assign Xout = X[STG-1];
   assign Yout = Y[STG-1];

endmodule



module sub(clock,angle_in,x_in,y_in,k,angle_out,x_out,y_out);
input clock;
input [3:0]k;
input signed [16:0] x_in;
input signed[16:0] y_in;
input signed [31:0] angle_in;
output  signed [16:0] x_out;
output  signed[16:0] y_out;
output  signed [31:0]angle_out;

reg signed[16:0] temp_x_out;
reg signed[16:0] temp_y_out;
reg signed[31:0] temp_angle_out;
```

```
assign x_out=temp_x_out;
assign y_out=temp_y_out;
assign angle_out=temp_angle_out;


wire signed [31:0] atan_table [0:30];


   assign atan_table[00] = 32'b00100000000000000000000000000000;
   assign atan_table[01] = 32'b00010010111001000000010100011101;
   assign atan_table[02] = 32'b00001001111111011001110000101011;
   assign atan_table[03] = 32'b00000101000100010001000111010100;
   assign atan_table[04] = 32'b00000010100010110000110101000011;
   assign atan_table[05] = 32'b00000001010001011101011111100001;
   assign atan_table[06] = 32'b00000000101000101111011000011110;
   assign atan_table[07] = 32'b00000000010100010111110001010101;
   assign atan_table[08] = 32'b00000000001010001011111001010011;
   assign atan_table[09] = 32'b00000000000101000101111100101110;
   assign atan_table[10] = 32'b00000000000010100010111110011000;
   assign atan_table[11] = 32'b00000000000001010001011111001100;
   assign atan_table[12] = 32'b00000000000000101000101111100110;
   assign atan_table[13] = 32'b00000000000000010100010111110011;
   assign atan_table[14] = 32'b00000000000000001010001011111001;
   assign atan_table[15] = 32'b00000000000000000101000101111101;
   assign atan_table[16] = 32'b00000000000000000010100010111110;
   assign atan_table[17] = 32'b00000000000000000001010001011111;
   assign atan_table[18] = 32'b00000000000000000000101000101111;
   assign atan_table[19] = 32'b00000000000000000000010100011000;
   assign atan_table[20] = 32'b00000000000000000000001010001100;
   assign atan_table[21] = 32'b00000000000000000000000101000110;
   assign atan_table[22] = 32'b00000000000000000000000010100011;
   assign atan_table[23] = 32'b00000000000000000000000001010001;
   assign atan_table[24] = 32'b00000000000000000000000000101000;
   assign atan_table[25] = 32'b00000000000000000000000000010100;
   assign atan_table[26] = 32'b00000000000000000000000000001010;
   assign atan_table[27] = 32'b00000000000000000000000000000101;
   assign atan_table[28] = 32'b00000000000000000000000000000010;
   assign atan_table[29] = 32'b00000000000000000000000000000001;
   assign atan_table[30] = 32'b00000000000000000000000000000000;
```

```
      wire                    Z_sign;
      wire signed  [16:0] X_shr, Y_shr;

      assign X_shr = x_in >>> k;
      assign Y_shr = y_in >>> k;


      assign Z_sign = angle_in[31];

      always @(posedge clock)
      begin

      temp_x_out     <= Z_sign ? x_in + Y_shr                    : x_in -
Y_shr;
      temp_y_out     <= Z_sign ? y_in - X_shr                   : y_in + X_shr;
      temp_angle_out <= Z_sign ? angle_in + atan_table[k]       : angle_in -
atan_table[k];
      end
         endmodule
```

CORDIC TESTBENCH.v

```
`timescale 1 ns/100 ps
module CORDIC_TESTBENCH;

  localparam width = 16; //width of x and y

  // Inputs
  reg signed[width-1:0] Xin, Yin;
  reg signed[31:0] angle;
  reg clk;
  reg signed  [63:0] i;
wire signed [width-1:0] COSout, SINout;

  localparam An = 32000/1.647;

  initial
  begin

    //set initial values
    angle = 32'b0;
    Xin = An;     // Xout = 32000*cos(angle)
    Yin = 0;      // Yout = 32000*sin(angle)
```

```
    //set clock
    clk = 'b0;
  end

     always
     #5 clk = ~clk;


    initial
    begin
      #500

        for (i = 0; i <= 360; i = i + 1)
       begin
      angle = ((1 << 32)*i)/360;
      #200
      $display ("angle = %d, xout = %d, yout = %d",i, COSout, SINout);
    end


   #200 $write("Simulation has finished");
   $stop;

  end

  CORDIC
s1(.clock(clk),.angle(angle),.Xin(Xin),.Yin(Yin),.Xout(COSout),.Yout(SINout));

  // Monitor the output

endmodule
```

6. RTL Simulation Results (part of simulation report)

```
 [18mvd0072@synopsysserver RTL]$ ./simv7
Chronologic VCS simulator copyright 1991-2018
Contains Synopsys proprietary information.
Compiler version O-2018.09-SP1_Full64; Runtime version O-2018.09-SP1_Full64;
Apr  6 16:03 2019
angle =                    0, xout =       31994, yout =           2
angle =                    1, xout =       31988, yout =         562
angle =                    2, xout =       31974, yout =        1120
angle =                    3, xout =       31949, yout =        1676
```

```
angle =  4, xout =  31916, yout =  2234
angle =  5, xout =  31871, yout =  2792
angle =  6, xout =  31819, yout =  3346
angle =  7, xout =  31756, yout =  3902
angle =  8, xout =  31681, yout =  4455
angle =  9, xout =  31600, yout =  5005
angle = 10, xout =  31508, yout =  5556
angle = 11, xout =  31407, yout =  6105
angle = 12, xout =  31294, yout =  6655
angle = 13, xout =  31176, yout =  7197
angle = 14, xout =  31043, yout =  7741
angle = 15, xout =  30906, yout =  8280
angle = 16, xout =  30754, yout =  8821
angle = 17, xout =  30598, yout =  9352
angle = 18, xout =  30431, yout =  9885
angle = 19, xout =  30251, yout = 10416
angle = 20, xout =  30062, yout = 10945
angle = 21, xout =  29868, yout = 11466
angle = 22, xout =  29661, yout = 11987
angle = 23, xout =  29453, yout = 12498
angle = 24, xout =  29230, yout = 13011
angle = 25, xout =  29000, yout = 13519
angle = 26, xout =  28757, yout = 14028
angle = 27, xout =  28508, yout = 14525
angle = 28, xout =  28251, yout = 15020
angle = 29, xout =  27984, yout = 15514
angle = 30, xout =  27708, yout = 15999
angle = 31, xout =  27424, yout = 16480
angle = 32, xout =  27136, yout = 16955
angle = 33, xout =  26831, yout = 17429
angle = 34, xout =  26525, yout = 17889
angle = 35, xout =  26208, yout = 18352
angle = 36, xout =  25886, yout = 18804
angle = 37, xout =  25550, yout = 19258
angle = 38, xout =  25212, yout = 19697
angle = 39, xout =  24864, yout = 20136
angle = 40, xout =  24508, yout = 20564
angle = 41, xout =  24146, yout = 20991
angle = 42, xout =  23776, yout = 21411
angle = 43, xout =  23401, yout = 21817
angle = 44, xout =  23016, yout = 22223
angle = 45, xout =  22622, yout = 22623
```

```
angle =                 46, xout =       22223, yout =       23016
angle =                 47, xout =       21817, yout =       23401
angle =                 48, xout =       21411, yout =       23776
angle =                 49, xout =       20991, yout =       24146
angle =                 50, xout =       20564, yout =       24508
angle =                 51, xout =       20136, yout =       24864
angle =                 52, xout =       19697, yout =       25212
angle =                 53, xout =       19258, yout =       25550
angle =                 54, xout =       18804, yout =       25886
angle =                 55, xout =       18352, yout =       26208
angle =                 56, xout =       17889, yout =       26525
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angle =                 59, xout =       16480, yout =       27424
angle =                 60, xout =       15999, yout =       27708
angle =                 61, xout =       15514, yout =       27984
angle =                 62, xout =       15020, yout =       28251
angle =                 63, xout =       14525, yout =       28508
angle =                 64, xout =       14028, yout =       28757
angle =                 65, xout =       13519, yout =       29000
angle =                 66, xout =       13011, yout =       29230
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angle =                 83, xout =        3902, yout =       31756
angle =                 84, xout =        3346, yout =       31819
angle =                 85, xout =        2792, yout =       31871
angle =                 86, xout =        2234, yout =       31916
angle =                 87, xout =        1676, yout =       31949
```

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angle =                 211, xout =      -27423, yout =      -16480
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angle =                 213, xout =      -26838, yout =      -17423
```

```
angle =                214, xout =      -26522, yout =      -17893
angle =                215, xout =      -26207, yout =      -18354
angle =                216, xout =      -25881, yout =      -18810
angle =                217, xout =      -25553, yout =      -19256
angle =                218, xout =      -25211, yout =      -19699
angle =                219, xout =      -24863, yout =      -20138
angle =                220, xout =      -24509, yout =      -20565
angle =                221, xout =      -24147, yout =      -20991
angle =                222, xout =      -23777, yout =      -21411
angle =                223, xout =      -23396, yout =      -21823
angle =                224, xout =      -23013, yout =      -22227
angle =                225, xout =      -22622, yout =      -22625
angle =                226, xout =      -22227, yout =      -23013
angle =                227, xout =      -21823, yout =      -23396
angle =                228, xout =      -21411, yout =      -23777
angle =                229, xout =      -20991, yout =      -24147
angle =                230, xout =      -20565, yout =      -24509
angle =                231, xout =      -20138, yout =      -24863
angle =                232, xout =      -19699, yout =      -25211
angle =                233, xout =      -19256, yout =      -25553
angle =                234, xout =      -18810, yout =      -25881
angle =                235, xout =      -18354, yout =      -26207
angle =                236, xout =      -17893, yout =      -26522
angle =                237, xout =      -17423, yout =      -26838
angle =                238, xout =      -16957, yout =      -27133
angle =                239, xout =      -16480, yout =      -27423
angle =                240, xout =      -15999, yout =      -27707
angle =                241, xout =      -15512, yout =      -27985
angle =                242, xout =      -15022, yout =      -28248
angle =                243, xout =      -14527, yout =      -28505
angle =                244, xout =      -14028, yout =      -28756
angle =                245, xout =      -13521, yout =      -28997
angle =                246, xout =      -13013, yout =      -29227
angle =                247, xout =      -12500, yout =      -29450
angle =                248, xout =      -11979, yout =      -29668
angle =                249, xout =      -11462, yout =      -29871
angle =                250, xout =      -10937, yout =      -30069
angle =                251, xout =      -10414, yout =      -30252
angle =                252, xout =       -9888, yout =      -30427
angle =                253, xout =       -9355, yout =      -30596
angle =                254, xout =       -8815, yout =      -30760
angle =                255, xout =       -8282, yout =      -30904
```

```
angle =                256, xout =       -7739, yout =      -31045
angle =                257, xout =       -7197, yout =      -31176
angle =                258, xout =       -6649, yout =      -31300
angle =                259, xout =       -6105, yout =      -31407
angle =                260, xout =       -5554, yout =      -31510
angle =                261, xout =       -5003, yout =      -31602
angle =                262, xout =       -4451, yout =      -31685
angle =                263, xout =       -3900, yout =      -31758
angle =                264, xout =       -3344, yout =      -31821
angle =                265, xout =       -2788, yout =      -31875
angle =                266, xout =       -2232, yout =      -31918
angle =                267, xout =       -1676, yout =      -31949
angle =                268, xout =       -1116, yout =      -31978
angle =                269, xout =        -558, yout =      -31992
angle =                270, xout =          -2, yout =      -31995
angle =                271, xout =         558, yout =      -31988
angle =                272, xout =        1116, yout =      -31974
angle =                273, xout =        1676, yout =      -31949
angle =                274, xout =        2232, yout =      -31916
angle =                275, xout =        2788, yout =      -31871
angle =                276, xout =        3344, yout =      -31819
angle =                277, xout =        3900, yout =      -31756
angle =                278, xout =        4451, yout =      -31681
angle =                279, xout =        5003, yout =      -31600
angle =                280, xout =        5554, yout =      -31508
angle =                281, xout =        6105, yout =      -31407
angle =                282, xout =        6649, yout =      -31294
angle =                283, xout =        7197, yout =      -31176
angle =                284, xout =        7739, yout =      -31043
angle =                285, xout =        8282, yout =      -30906
angle =                286, xout =        8815, yout =      -30754
angle =                287, xout =        9354, yout =      -30598
angle =                288, xout =        9889, yout =      -30431
angle =                289, xout =       10414, yout =      -30251
angle =                290, xout =       10937, yout =      -30062
angle =                291, xout =       11462, yout =      -29868
angle =                292, xout =       11979, yout =      -29661
angle =                293, xout =       12500, yout =      -29453
angle =                294, xout =       13013, yout =      -29230
angle =                295, xout =       13521, yout =      -29000
angle =                296, xout =       14028, yout =      -28757
angle =                297, xout =       14527, yout =      -28508
```

```
angle =                 298, xout =       15022, yout =      -28251
angle =                 299, xout =       15512, yout =      -27984
angle =                 300, xout =       15999, yout =      -27708
angle =                 301, xout =       16480, yout =      -27425
angle =                 302, xout =       16957, yout =      -27135
angle =                 303, xout =       17423, yout =      -26831
angle =                 304, xout =       17893, yout =      -26525
angle =                 305, xout =       18354, yout =      -26208
angle =                 306, xout =       18810, yout =      -25886
angle =                 307, xout =       19256, yout =      -25550
angle =                 308, xout =       19699, yout =      -25212
angle =                 309, xout =       20138, yout =      -24864
angle =                 310, xout =       20564, yout =      -24508
angle =                 311, xout =       20991, yout =      -24146
angle =                 312, xout =       21411, yout =      -23776
angle =                 313, xout =       21823, yout =      -23401
angle =                 314, xout =       22227, yout =      -23016
angle =                 315, xout =       22623, yout =      -22623
angle =                 316, xout =       23012, yout =      -22224
angle =                 317, xout =       23395, yout =      -21818
angle =                 318, xout =       23776, yout =      -21412
angle =                 319, xout =       24146, yout =      -20992
angle =                 320, xout =       24508, yout =      -20566
angle =                 321, xout =       24862, yout =      -20137
angle =                 322, xout =       25210, yout =      -19698
angle =                 323, xout =       25552, yout =      -19259
angle =                 324, xout =       25880, yout =      -18805
angle =                 325, xout =       26206, yout =      -18353
angle =                 326, xout =       26521, yout =      -17890
angle =                 327, xout =       26837, yout =      -17430
angle =                 328, xout =       27134, yout =      -16956
angle =                 329, xout =       27424, yout =      -16481
angle =                 330, xout =       27708, yout =      -16000
angle =                 331, xout =       27986, yout =      -15515
angle =                 332, xout =       28249, yout =      -15021
angle =                 333, xout =       28506, yout =      -14526
angle =                 334, xout =       28757, yout =      -14029
angle =                 335, xout =       28998, yout =      -13520
angle =                 336, xout =       29228, yout =      -13012
angle =                 337, xout =       29451, yout =      -12499
angle =                 338, xout =       29669, yout =      -11988
angle =                 339, xout =       29872, yout =      -11467
```

```
angle =                  340, xout =       30070, yout =      -10946
angle =                  341, xout =       30253, yout =      -10417
angle =                  342, xout =       30427, yout =       -9883
angle =                  343, xout =       30596, yout =       -9352
angle =                  344, xout =       30760, yout =       -8820
angle =                  345, xout =       30904, yout =       -8279
angle =                  346, xout =       31045, yout =       -7740
angle =                  347, xout =       31176, yout =       -7196
angle =                  348, xout =       31300, yout =       -6654
angle =                  349, xout =       31407, yout =       -6104
angle =                  350, xout =       31510, yout =       -5555
angle =                  351, xout =       31602, yout =       -5004
angle =                  352, xout =       31685, yout =       -4454
angle =                  353, xout =       31758, yout =       -3901
angle =                  354, xout =       31821, yout =       -3345
angle =                  355, xout =       31875, yout =       -2791
angle =                  356, xout =       31918, yout =       -2233
angle =                  357, xout =       31949, yout =       -1675
angle =                  358, xout =       31978, yout =       -1119
angle =                  359, xout =       31992, yout =        -561
angle =                  360, xout =       31994, yout =           2
Simulation has finished$stop at time 729000 Scope: CORDIC_TESTBENCH File:
CORDIC_TESTBENCH.v Line: 48
```

7. Synthesis Setup

7.1. Libraries used:

- **Saed90nm.db :** 1 or 2 lines about this lib.
- **TSMC (tcb018gbwp7ttc.db):** 1 or 2 lines about this lib.
- **SCL (tsl18fs120_scl_ss.db):** 1 or 2 lines about this lib.

7.2. Constraints used:

- **create_clock -period 40.0 [get_ports clk]** : Creates a clock object and defines its waveform in the current design.
- **set_clock_latency -source -max 0.9 [get_clocks clk]:** Sets the external clock source latency as 1.5ns or 1500ps.
- **set_clock_latency -max 0.9 [get_clocks clk]:** The maximum internal clock network insertion delay or latency is 300ps or 0.3 ns.
- **set_clock_uncertainty -setup 0.2 [get_clocks clk]:** sets the source clock uncertainty to 1 ns.
- **set_clock_uncertainty -hold 0.1 [get_clocks clk]:** sets the source clock uncertainty to 1 ns.

- **set_clock_transition 0.12 [get_clocks clk] :** Sets the transition time at the clock pins of all sequential devices clocked by the specified ideal clocks.
- **set_input_delay –max 0.7 -clock clk [get_ports input_port_name]:** Sets maximum input delay on pins or input ports relative to a clock signal.
- **set_output_delay -max 0.8 -clock clk [get_ports output_port_name] :** Sets maximum output delay on pins or output ports relative to a clock signal.

8. Synthesis Report (Area , Power,Timing)

8.1. Using library: saed90nm.db

8.1.1. Area report

```
****************************************
Report : area
Design : CORDIC
Version: O-2018.06-SP4
Date   : Wed Mar 20 10:08:17 2019
****************************************

Information: Updating design information... (UID-85)
Library(s) Used:

    saed90nm_typ_ht (File:
/home/userdata/18mvd0061/asicproject/ref/models/saed90nm_typ_ht.db)

Number of ports:                         8274
Number of nets:                         18677
Number of cells:                         9044
Number of combinational cells:           7718
Number of sequential cells:              1056
Number of macros/black boxes:               0
Number of buf/inv:                       1632
Number of references:                      25

Combinational area:             106934.168637
Buf/Inv area:                     9024.307434
Noncombinational area:           26276.658875
Macro/Black Box area:                0.000000
Net Interconnect area:            7264.021908

Total cell area:                133210.827512
Total area:                     140474.849420
```

8.1.2. Power report (without saif file):

```
****************************************
Report : power
        -analysis_effort low
Design : CORDIC
Version: O-2018.06-SP4
Date   : Wed Mar 20 10:50:37 2019
****************************************


Library(s) Used:
```

saed90nm_typ_ht (File: /home/userdata/18mvd0061/asicproject/ref/models/saed90nm_typ_ht.db)

Operating Conditions: TYPICAL Library: saed90nm_typ_ht
Wire Load Model Mode: segmented

Design	Wire Load Model	Library
CORDIC	8000	saed90nm_typ_ht
sub_0	16000	saed90nm_typ_ht
sub_1	16000	saed90nm_typ_ht
sub_2	16000	saed90nm_typ_ht
sub_3	16000	saed90nm_typ_ht
sub_4	16000	saed90nm_typ_ht
sub_5	16000	saed90nm_typ_ht
sub_6	16000	saed90nm_typ_ht
sub_7	16000	saed90nm_typ_ht
sub_8	16000	saed90nm_typ_ht
sub_9	16000	saed90nm_typ_ht
sub_10	16000	saed90nm_typ_ht
sub_11	16000	saed90nm_typ_ht
sub_12	16000	saed90nm_typ_ht
sub_13	16000	saed90nm_typ_ht
sub_14	16000	saed90nm_typ_ht
sub_1_DW01_sub_0	8000	saed90nm_typ_ht
sub_1_DW01_add_0	8000	saed90nm_typ_ht
sub_1_DW01_add_1	8000	saed90nm_typ_ht
sub_1_DW01_sub_1	8000	saed90nm_typ_ht
sub_1_DW01_sub_2	8000	saed90nm_typ_ht
sub_1_DW01_add_2	8000	saed90nm_typ_ht
sub_2_DW01_sub_0	8000	saed90nm_typ_ht
sub_2_DW01_add_0	8000	saed90nm_typ_ht
sub_2_DW01_add_1	8000	saed90nm_typ_ht
sub_2_DW01_sub_1	8000	saed90nm_typ_ht
sub_2_DW01_sub_2	8000	saed90nm_typ_ht
sub_2_DW01_add_2	8000	saed90nm_typ_ht
sub_3_DW01_sub_0	8000	saed90nm_typ_ht
sub_3_DW01_add_0	8000	saed90nm_typ_ht
sub_3_DW01_add_1	8000	saed90nm_typ_ht
sub_3_DW01_sub_1	8000	saed90nm_typ_ht
sub_3_DW01_sub_2	8000	saed90nm_typ_ht
sub_3_DW01_add_2	8000	saed90nm_typ_ht
sub_4_DW01_sub_0	8000	saed90nm_typ_ht
sub_4_DW01_add_0	8000	saed90nm_typ_ht
sub_4_DW01_add_1	8000	saed90nm_typ_ht
sub_4_DW01_sub_1	8000	saed90nm_typ_ht
sub_4_DW01_sub_2	8000	saed90nm_typ_ht
sub_4_DW01_add_2	8000	saed90nm_typ_ht
sub_5_DW01_sub_0	8000	saed90nm_typ_ht
sub_5_DW01_add_0	8000	saed90nm_typ_ht
sub_5_DW01_add_1	8000	saed90nm_typ_ht
sub_5_DW01_sub_1	8000	saed90nm_typ_ht
sub_5_DW01_sub_2	8000	saed90nm_typ_ht
sub_5_DW01_add_2	8000	saed90nm_typ_ht
sub_6_DW01_sub_0	8000	saed90nm_typ_ht

```
sub_6_DW01_add_0       8000              saed90nm_typ_ht
sub_6_DW01_add_1       8000              saed90nm_typ_ht
sub_6_DW01_sub_1       8000              saed90nm_typ_ht
sub_6_DW01_sub_2       8000              saed90nm_typ_ht
sub_6_DW01_add_2       8000              saed90nm_typ_ht
sub_7_DW01_sub_0       8000              saed90nm_typ_ht
sub_7_DW01_add_0       8000              saed90nm_typ_ht
sub_7_DW01_add_1       8000              saed90nm_typ_ht
sub_7_DW01_sub_1       8000              saed90nm_typ_ht
sub_7_DW01_sub_2       8000              saed90nm_typ_ht
sub_7_DW01_add_2       8000              saed90nm_typ_ht
sub_8_DW01_sub_0       8000              saed90nm_typ_ht
sub_8_DW01_add_0       8000              saed90nm_typ_ht
sub_8_DW01_add_1       8000              saed90nm_typ_ht
sub_8_DW01_sub_1       8000              saed90nm_typ_ht
sub_8_DW01_sub_2       8000              saed90nm_typ_ht
sub_8_DW01_add_2       8000              saed90nm_typ_ht
sub_9_DW01_sub_0       8000              saed90nm_typ_ht
sub_9_DW01_add_0       8000              saed90nm_typ_ht
sub_9_DW01_add_1       8000              saed90nm_typ_ht
sub_9_DW01_sub_1       8000              saed90nm_typ_ht
sub_9_DW01_sub_2       8000              saed90nm_typ_ht
sub_9_DW01_add_2       8000              saed90nm_typ_ht
sub_10_DW01_sub_0      8000              saed90nm_typ_ht
sub_10_DW01_add_0      8000              saed90nm_typ_ht
sub_10_DW01_add_1      8000              saed90nm_typ_ht
sub_10_DW01_sub_1      8000              saed90nm_typ_ht
sub_10_DW01_sub_2      8000              saed90nm_typ_ht
sub_10_DW01_add_2      8000              saed90nm_typ_ht
sub_11_DW01_sub_0      8000              saed90nm_typ_ht
sub_11_DW01_add_0      8000              saed90nm_typ_ht
sub_11_DW01_add_1      8000              saed90nm_typ_ht
sub_11_DW01_sub_1      8000              saed90nm_typ_ht
sub_11_DW01_sub_2      8000              saed90nm_typ_ht
sub_11_DW01_add_2      8000              saed90nm_typ_ht
sub_12_DW01_sub_0      8000              saed90nm_typ_ht
sub_12_DW01_add_0      8000              saed90nm_typ_ht
sub_12_DW01_add_1      8000              saed90nm_typ_ht
sub_12_DW01_sub_1      8000              saed90nm_typ_ht
sub_12_DW01_sub_2      8000              saed90nm_typ_ht
sub_12_DW01_add_2      8000              saed90nm_typ_ht
sub_13_DW01_sub_0      8000              saed90nm_typ_ht
sub_13_DW01_add_0      8000              saed90nm_typ_ht
sub_13_DW01_add_1      8000              saed90nm_typ_ht
sub_13_DW01_sub_1      8000              saed90nm_typ_ht
sub_13_DW01_sub_2      8000              saed90nm_typ_ht
sub_13_DW01_add_2      8000              saed90nm_typ_ht
sub_14_DW01_sub_0      8000              saed90nm_typ_ht
sub_14_DW01_add_0      8000              saed90nm_typ_ht
sub_14_DW01_add_1      8000              saed90nm_typ_ht
sub_14_DW01_sub_1      8000              saed90nm_typ_ht
sub_14_DW01_sub_2      8000              saed90nm_typ_ht
sub_14_DW01_add_2      8000              saed90nm_typ_ht
sub_0_DW01_sub_0       8000              saed90nm_typ_ht
sub_0_DW01_add_0       8000              saed90nm_typ_ht
```

```
sub_0_DW01_add_1       8000              saed90nm_typ_ht
sub_0_DW01_sub_1       8000              saed90nm_typ_ht
sub_0_DW01_sub_2       8000              saed90nm_typ_ht
sub_0_DW01_add_2       8000              saed90nm_typ_ht


Global Operating Voltage = 1.2
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000ff
    Time Units = 1ns
    Dynamic Power Units = 1uW    (derived from V,C,T units)
    Leakage Power Units = 1pW


  Cell Internal Power  =   2.3012 mW   (76%)
  Net Switching Power  = 713.2278 uW   (24%)
                         ---------
Total Dynamic Power    =   3.0144 mW  (100%)

Cell Leakage Power     =   2.0777 mW


                 Internal         Switching           Leakage            Total
Power Group      Power            Power               Power              Power   (   %    )
Attrs
--------------------------------------------------------------------------------------------------
----
io_pad             0.0000           0.0000            0.0000            0.0000  (   0.00%)
memory             0.0000           0.0000            0.0000            0.0000  (   0.00%)
black_box          0.0000           0.0000            0.0000            0.0000  (   0.00%)
clock_network      0.0000           0.0000            0.0000            0.0000  (   0.00%)
register         654.3065         274.6859        4.4475e+08        1.3737e+03  (  26.98%)
sequential         0.0000           0.0000            0.0000            0.0000  (   0.00%)
combinational  1.6469e+03         438.5415        1.6330e+09        3.7184e+03  (  73.02%)
--------------------------------------------------------------------------------------------------
----
Total          2.3012e+03 uW       713.2274 uW     2.0777e+09 pW     5.0921e+03 uW
```

8.1.3. Power report (with saif file):

```
    ****************************************
    Report : power
             -analysis_effort low
    Design : CORDIC
    Version: O-2018.06-SP4
    Date   : Wed Mar 20 10:08:44 2019
    ****************************************


    Library(s) Used:

        saed90nm_typ_ht (File:
    /home/userdata/18mvd0061/asicproject/ref/models/saed90nm_typ_ht.db)
```

```
Operating Conditions: TYPICAL   Library: saed90nm_typ_ht
Wire Load Model Mode: segmented

Design        Wire Load Model            Library
------------------------------------------------
CORDIC                 8000              saed90nm_typ_ht
sub_0                  16000             saed90nm_typ_ht
sub_1                  16000             saed90nm_typ_ht
sub_2                  16000             saed90nm_typ_ht
sub_3                  16000             saed90nm_typ_ht
sub_4                  16000             saed90nm_typ_ht
sub_5                  16000             saed90nm_typ_ht
sub_6                  16000             saed90nm_typ_ht
sub_7                  16000             saed90nm_typ_ht
sub_8                  16000             saed90nm_typ_ht
sub_9                  16000             saed90nm_typ_ht
sub_10                 16000             saed90nm_typ_ht
sub_11                 16000             saed90nm_typ_ht
sub_12                 16000             saed90nm_typ_ht
sub_13                 16000             saed90nm_typ_ht
sub_14                 16000             saed90nm_typ_ht
sub_1_DW01_sub_0       8000              saed90nm_typ_ht
sub_1_DW01_add_0       8000              saed90nm_typ_ht
sub_1_DW01_add_1       8000              saed90nm_typ_ht
sub_1_DW01_sub_1       8000              saed90nm_typ_ht
sub_1_DW01_sub_2       8000              saed90nm_typ_ht
sub_1_DW01_add_2       8000              saed90nm_typ_ht
sub_2_DW01_sub_0       8000              saed90nm_typ_ht
sub_2_DW01_add_0       8000              saed90nm_typ_ht
sub_2_DW01_add_1       8000              saed90nm_typ_ht
sub_2_DW01_sub_1       8000              saed90nm_typ_ht
sub_2_DW01_sub_2       8000              saed90nm_typ_ht
sub_2_DW01_add_2       8000              saed90nm_typ_ht
sub_3_DW01_sub_0       8000              saed90nm_typ_ht
sub_3_DW01_add_0       8000              saed90nm_typ_ht
sub_3_DW01_add_1       8000              saed90nm_typ_ht
sub_3_DW01_sub_1       8000              saed90nm_typ_ht
sub_3_DW01_sub_2       8000              saed90nm_typ_ht
sub_3_DW01_add_2       8000              saed90nm_typ_ht
sub_4_DW01_sub_0       8000              saed90nm_typ_ht
sub_4_DW01_add_0       8000              saed90nm_typ_ht
sub_4_DW01_add_1       8000              saed90nm_typ_ht
sub_4_DW01_sub_1       8000              saed90nm_typ_ht
sub_4_DW01_sub_2       8000              saed90nm_typ_ht
sub_4_DW01_add_2       8000              saed90nm_typ_ht
sub_5_DW01_sub_0       8000              saed90nm_typ_ht
sub_5_DW01_add_0       8000              saed90nm_typ_ht
sub_5_DW01_add_1       8000              saed90nm_typ_ht
sub_5_DW01_sub_1       8000              saed90nm_typ_ht
sub_5_DW01_sub_2       8000              saed90nm_typ_ht
sub_5_DW01_add_2       8000              saed90nm_typ_ht
sub_6_DW01_sub_0       8000              saed90nm_typ_ht
sub_6_DW01_add_0       8000              saed90nm_typ_ht
sub_6_DW01_add_1       8000              saed90nm_typ_ht
```

sub_6_DW01_sub_1	8000	saed90nm_typ_ht
sub_6_DW01_sub_2	8000	saed90nm_typ_ht
sub_6_DW01_add_2	8000	saed90nm_typ_ht
sub_7_DW01_sub_0	8000	saed90nm_typ_ht
sub_7_DW01_add_0	8000	saed90nm_typ_ht
sub_7_DW01_add_1	8000	saed90nm_typ_ht
sub_7_DW01_sub_1	8000	saed90nm_typ_ht
sub_7_DW01_sub_2	8000	saed90nm_typ_ht
sub_7_DW01_add_2	8000	saed90nm_typ_ht
sub_8_DW01_sub_0	8000	saed90nm_typ_ht
sub_8_DW01_add_0	8000	saed90nm_typ_ht
sub_8_DW01_add_1	8000	saed90nm_typ_ht
sub_8_DW01_sub_1	8000	saed90nm_typ_ht
sub_8_DW01_sub_2	8000	saed90nm_typ_ht
sub_8_DW01_add_2	8000	saed90nm_typ_ht
sub_9_DW01_sub_0	8000	saed90nm_typ_ht
sub_9_DW01_add_0	8000	saed90nm_typ_ht
sub_9_DW01_add_1	8000	saed90nm_typ_ht
sub_9_DW01_sub_1	8000	saed90nm_typ_ht
sub_9_DW01_sub_2	8000	saed90nm_typ_ht
sub_9_DW01_add_2	8000	saed90nm_typ_ht
sub_10_DW01_sub_0	8000	saed90nm_typ_ht
sub_10_DW01_add_0	8000	saed90nm_typ_ht
sub_10_DW01_add_1	8000	saed90nm_typ_ht
sub_10_DW01_sub_1	8000	saed90nm_typ_ht
sub_10_DW01_sub_2	8000	saed90nm_typ_ht
sub_10_DW01_add_2	8000	saed90nm_typ_ht
sub_11_DW01_sub_0	8000	saed90nm_typ_ht
sub_11_DW01_add_0	8000	saed90nm_typ_ht
sub_11_DW01_add_1	8000	saed90nm_typ_ht
sub_11_DW01_sub_1	8000	saed90nm_typ_ht
sub_11_DW01_sub_2	8000	saed90nm_typ_ht
sub_11_DW01_add_2	8000	saed90nm_typ_ht
sub_12_DW01_sub_0	8000	saed90nm_typ_ht
sub_12_DW01_add_0	8000	saed90nm_typ_ht
sub_12_DW01_add_1	8000	saed90nm_typ_ht
sub_12_DW01_sub_1	8000	saed90nm_typ_ht
sub_12_DW01_sub_2	8000	saed90nm_typ_ht
sub_12_DW01_add_2	8000	saed90nm_typ_ht
sub_13_DW01_sub_0	8000	saed90nm_typ_ht
sub_13_DW01_add_0	8000	saed90nm_typ_ht
sub_13_DW01_add_1	8000	saed90nm_typ_ht
sub_13_DW01_sub_1	8000	saed90nm_typ_ht
sub_13_DW01_sub_2	8000	saed90nm_typ_ht
sub_13_DW01_add_2	8000	saed90nm_typ_ht
sub_14_DW01_sub_0	8000	saed90nm_typ_ht
sub_14_DW01_add_0	8000	saed90nm_typ_ht
sub_14_DW01_add_1	8000	saed90nm_typ_ht
sub_14_DW01_sub_1	8000	saed90nm_typ_ht
sub_14_DW01_sub_2	8000	saed90nm_typ_ht
sub_14_DW01_add_2	8000	saed90nm_typ_ht
sub_0_DW01_sub_0	8000	saed90nm_typ_ht
sub_0_DW01_add_0	8000	saed90nm_typ_ht
sub_0_DW01_add_1	8000	saed90nm_typ_ht
sub_0_DW01_sub_1	8000	saed90nm_typ_ht

```
sub_0_DW01_sub_2       8000              saed90nm_typ_ht
sub_0_DW01_add_2       8000              saed90nm_typ_ht


Global Operating Voltage = 1.2
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000ff
    Time Units = 1ns
    Dynamic Power Units = 1uW    (derived from V,C,T units)
    Leakage Power Units = 1pW


  Cell Internal Power  = 867.2046 uW   (95%)
  Net Switching Power  =  48.0338 uW    (5%)
                         ---------
Total Dynamic Power    = 915.2384 uW  (100%)

Cell Leakage Power     =   2.0763 mW


                 Internal         Switching           Leakage            Total
Power Group      Power            Power               Power              Power   (   %
)  Attrs
--------------------------------------------------------------------------------------------
--------
io_pad             0.0000           0.0000            0.0000            0.0000  (
0.00%)
memory             0.0000           0.0000            0.0000            0.0000  (
0.00%)
black_box          0.0000           0.0000            0.0000            0.0000  (
0.00%)
clock_network      0.0000           0.0000            0.0000            0.0000  (
0.00%)
register         707.7507          24.4593        4.4445e+08        1.1767e+03  (
39.33%)
sequential         0.0000           0.0000            0.0000            0.0000  (
0.00%)
combinational    159.4551          23.5744        1.6318e+09        1.8149e+03  (
60.67%)
--------------------------------------------------------------------------------------------
--------
Total            867.2058 uW       48.0337 uW     2.0763e+09 pW     2.9915e+03 uW
```

8.1.4 Timing Report:

```
****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : CORDIC
Version: O-2018.06-SP4
Date   : Wed Mar 20 10:50:36 2019
****************************************
```

```
 # A fanout number of 1000 was used for high fanout net computations.

Operating Conditions: TYPICAL   Library: saed90nm_typ_ht
Wire Load Model Mode: segmented

  Startpoint: XYZ[0].c1/temp_x_out_reg[1]
              (rising edge-triggered flip-flop clocked by clock)
  Endpoint: XYZ[1].c1/temp_y_out_reg[16]
            (rising edge-triggered flip-flop clocked by clock)
  Path Group: clock
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  sub_14             16000                 saed90nm_typ_ht
  sub_13             16000                 saed90nm_typ_ht
  sub_12             16000                 saed90nm_typ_ht
  sub_11             16000                 saed90nm_typ_ht
  sub_10             16000                 saed90nm_typ_ht
  sub_9              16000                 saed90nm_typ_ht
  sub_8              16000                 saed90nm_typ_ht
  sub_7              16000                 saed90nm_typ_ht
  sub_6              16000                 saed90nm_typ_ht
  sub_5              16000                 saed90nm_typ_ht
  sub_4              16000                 saed90nm_typ_ht
  sub_3              16000                 saed90nm_typ_ht
  sub_2              16000                 saed90nm_typ_ht
  sub_1              16000                 saed90nm_typ_ht
  CORDIC             8000                  saed90nm_typ_ht
  sub_0              16000                 saed90nm_typ_ht
  sub_14_DW01_add_2  8000                  saed90nm_typ_ht
  sub_14_DW01_sub_2  8000                  saed90nm_typ_ht
  sub_14_DW01_sub_1  8000                  saed90nm_typ_ht
  sub_14_DW01_add_1  8000                  saed90nm_typ_ht

  Point                                                   Incr       Path
  --------------------------------------------------------------------------
  clock clock (rise edge)                                 0.00       0.00
  clock network delay (ideal)                             1.00       1.00
  XYZ[0].c1/temp_x_out_reg[1]/CLK (DFFX1)                 0.00 #     1.00 r
  XYZ[0].c1/temp_x_out_reg[1]/Q (DFFX1)                   0.38       1.38 f
  XYZ[0].c1/x_out[1] (sub_0)                              0.00       1.38 f
  XYZ[1].c1/x_in[1] (sub_14)                              0.00       1.38 f
  XYZ[1].c1/U214/Q (AO22X1)                               0.23       1.61 f
  XYZ[1].c1/U215/Q (AO221X1)                              0.15       1.76 f
  XYZ[1].c1/U221/Q (AO221X1)                              0.26       2.02 f
  XYZ[1].c1/add_153/B[1] (sub_14_DW01_add_1)              0.00       2.02 f
  XYZ[1].c1/add_153/U1_1/CO (FADDX1)                      0.66       2.69 f
  XYZ[1].c1/add_153/U1_2/CO (FADDX1)                      0.34       3.03 f
  XYZ[1].c1/add_153/U1_3/CO (FADDX1)                      0.34       3.37 f
  XYZ[1].c1/add_153/U1_4/CO (FADDX1)                      0.34       3.71 f
  XYZ[1].c1/add_153/U1_5/CO (FADDX1)                      0.34       4.05 f
  XYZ[1].c1/add_153/U1_6/CO (FADDX1)                      0.34       4.39 f
  XYZ[1].c1/add_153/U1_7/CO (FADDX1)                      0.34       4.73 f
```

```
  XYZ[1].c1/add_153/U1_8/CO (FADDX1)                      0.34       5.07 f
  XYZ[1].c1/add_153/U1_9/CO (FADDX1)                      0.34       5.41 f
  XYZ[1].c1/add_153/U1_10/CO (FADDX1)                     0.34       5.75 f
  XYZ[1].c1/add_153/U1_11/CO (FADDX1)                     0.34       6.09 f
  XYZ[1].c1/add_153/U1_12/CO (FADDX1)                     0.34       6.43 f
  XYZ[1].c1/add_153/U1_13/CO (FADDX1)                     0.34       6.78 f
  XYZ[1].c1/add_153/U1_14/CO (FADDX1)                     0.34       7.12 f
  XYZ[1].c1/add_153/U1_15/CO (FADDX1)                     0.33       7.44 f
  XYZ[1].c1/add_153/U1_16/Q (XOR3X1)                      0.17       7.61 r
  XYZ[1].c1/add_153/SUM[16] (sub_14_DW01_add_1)           0.00       7.61 r
  XYZ[1].c1/U135/Q (AO22X1)                               0.20       7.81 r
  XYZ[1].c1/temp_y_out_reg[16]/D (DFFX1)                  0.03       7.84 r
  data arrival time                                                  7.84

  clock clock (rise edge)                                10.00      10.00
  clock network delay (ideal)                             1.00      11.00
  XYZ[1].c1/temp_y_out_reg[16]/CLK (DFFX1)                0.00      11.00 r
  library setup time                                     -0.09      10.91
  data required time                                                10.91
  ------------------------------------------------------------------------
  data required time                                                10.91
  data arrival time                                                 -7.84
  ------------------------------------------------------------------------
  slack (MET)                                                        3.07
```

8.2. Using library: TSMC

8.2.1.Area report

```
****************************************
Report : area
Design : CORDIC
Version: O-2018.06-SP4
Date   : Wed Mar 20 11:55:01 2019
****************************************

Information: Updating design information... (UID-85)
Warning: Design 'CORDIC' contains 1 high-fanout nets. A fanout number of 1000 will be used
for delay calculations involving these nets. (TIM-134)
Library(s) Used:

    tcb018gbwp7ttc (File:
/home/synopsys/TSMCHOME/digital/Front_End/timing_power_noise/NLDM/tcb018gbwp7t_270a/tcb018
gbwp7ttc.db)

Number of ports:                         8274
Number of nets:                         17944
Number of cells:                         8311
Number of combinational cells:           7150
Number of sequential cells:              1056
Number of macros/black boxes:               0
Number of buf/inv:                       2038
Number of references:                      27

Combinational area:             149346.042807
```

```
     Buf/Inv area:                    13706.828590
     Noncombinational area:           57083.981941
     Macro/Black Box area:                0.000000
     Net Interconnect area:      undefined  (Wire load has zero net area)

     Total cell area:                206430.024748
     Total area:                 undefined
```

8.2.2. Power report (without saif file):

```
****************************************
Report : power
        -analysis_effort low
Design : CORDIC
Version: O-2018.06-SP4
Date   : Wed Mar 20 11:55:05 2019
****************************************


Library(s) Used:

    tcb018gbwp7ttc (File:
/home/synopsys/TSMCHOME/digital/Front_End/timing_power_noise/NLDM/tcb018gbwp7t_270a/tcb018gbwp7t
tc.db)


Operating Conditions: NCCOM   Library: tcb018gbwp7ttc
Wire Load Model Mode: segmented

Design        Wire Load Model            Library
------------------------------------------------
CORDIC                 ZeroWireload      tcb018gbwp7ttc
sub_0                  ZeroWireload      tcb018gbwp7ttc
sub_1                  ZeroWireload      tcb018gbwp7ttc
sub_2                  ZeroWireload      tcb018gbwp7ttc
sub_3                  ZeroWireload      tcb018gbwp7ttc
sub_4                  ZeroWireload      tcb018gbwp7ttc
sub_5                  ZeroWireload      tcb018gbwp7ttc
sub_6                  ZeroWireload      tcb018gbwp7ttc
sub_7                  ZeroWireload      tcb018gbwp7ttc
sub_8                  ZeroWireload      tcb018gbwp7ttc
sub_9                  ZeroWireload      tcb018gbwp7ttc
sub_10                 ZeroWireload      tcb018gbwp7ttc
sub_11                 ZeroWireload      tcb018gbwp7ttc
sub_12                 ZeroWireload      tcb018gbwp7ttc
sub_13                 ZeroWireload      tcb018gbwp7ttc
sub_14                 ZeroWireload      tcb018gbwp7ttc
sub_1_DW01_sub_0       ZeroWireload      tcb018gbwp7ttc
sub_1_DW01_add_0       ZeroWireload      tcb018gbwp7ttc
sub_1_DW01_add_1       ZeroWireload      tcb018gbwp7ttc
sub_1_DW01_sub_1       ZeroWireload      tcb018gbwp7ttc
sub_1_DW01_sub_2       ZeroWireload      tcb018gbwp7ttc
sub_1_DW01_add_2       ZeroWireload      tcb018gbwp7ttc
sub_2_DW01_sub_0       ZeroWireload      tcb018gbwp7ttc
sub_2_DW01_add_0       ZeroWireload      tcb018gbwp7ttc
```

sub_2_DW01_add_1	ZeroWireload	tcb018gbwp7ttc
sub_2_DW01_sub_1	ZeroWireload	tcb018gbwp7ttc
sub_2_DW01_sub_2	ZeroWireload	tcb018gbwp7ttc
sub_2_DW01_add_2	ZeroWireload	tcb018gbwp7ttc
sub_3_DW01_sub_0	ZeroWireload	tcb018gbwp7ttc
sub_3_DW01_add_0	ZeroWireload	tcb018gbwp7ttc
sub_3_DW01_add_1	ZeroWireload	tcb018gbwp7ttc
sub_3_DW01_sub_1	ZeroWireload	tcb018gbwp7ttc
sub_3_DW01_sub_2	ZeroWireload	tcb018gbwp7ttc
sub_3_DW01_add_2	ZeroWireload	tcb018gbwp7ttc
sub_4_DW01_sub_0	ZeroWireload	tcb018gbwp7ttc
sub_4_DW01_add_0	ZeroWireload	tcb018gbwp7ttc
sub_4_DW01_add_1	ZeroWireload	tcb018gbwp7ttc
sub_4_DW01_sub_1	ZeroWireload	tcb018gbwp7ttc
sub_4_DW01_sub_2	ZeroWireload	tcb018gbwp7ttc
sub_4_DW01_add_2	ZeroWireload	tcb018gbwp7ttc
sub_5_DW01_sub_0	ZeroWireload	tcb018gbwp7ttc
sub_5_DW01_add_0	ZeroWireload	tcb018gbwp7ttc
sub_5_DW01_add_1	ZeroWireload	tcb018gbwp7ttc
sub_5_DW01_sub_1	ZeroWireload	tcb018gbwp7ttc
sub_5_DW01_sub_2	ZeroWireload	tcb018gbwp7ttc
sub_5_DW01_add_2	ZeroWireload	tcb018gbwp7ttc
sub_6_DW01_sub_0	ZeroWireload	tcb018gbwp7ttc
sub_6_DW01_add_0	ZeroWireload	tcb018gbwp7ttc
sub_6_DW01_add_1	ZeroWireload	tcb018gbwp7ttc
sub_6_DW01_sub_1	ZeroWireload	tcb018gbwp7ttc
sub_6_DW01_sub_2	ZeroWireload	tcb018gbwp7ttc
sub_6_DW01_add_2	ZeroWireload	tcb018gbwp7ttc
sub_7_DW01_sub_0	ZeroWireload	tcb018gbwp7ttc
sub_7_DW01_add_0	ZeroWireload	tcb018gbwp7ttc
sub_7_DW01_add_1	ZeroWireload	tcb018gbwp7ttc
sub_7_DW01_sub_1	ZeroWireload	tcb018gbwp7ttc
sub_7_DW01_sub_2	ZeroWireload	tcb018gbwp7ttc
sub_7_DW01_add_2	ZeroWireload	tcb018gbwp7ttc
sub_8_DW01_sub_0	ZeroWireload	tcb018gbwp7ttc
sub_8_DW01_add_0	ZeroWireload	tcb018gbwp7ttc
sub_8_DW01_add_1	ZeroWireload	tcb018gbwp7ttc
sub_8_DW01_sub_1	ZeroWireload	tcb018gbwp7ttc
sub_8_DW01_sub_2	ZeroWireload	tcb018gbwp7ttc
sub_8_DW01_add_2	ZeroWireload	tcb018gbwp7ttc
sub_9_DW01_sub_0	ZeroWireload	tcb018gbwp7ttc
sub_9_DW01_add_0	ZeroWireload	tcb018gbwp7ttc
sub_9_DW01_add_1	ZeroWireload	tcb018gbwp7ttc
sub_9_DW01_sub_1	ZeroWireload	tcb018gbwp7ttc
sub_9_DW01_sub_2	ZeroWireload	tcb018gbwp7ttc
sub_9_DW01_add_2	ZeroWireload	tcb018gbwp7ttc
sub_10_DW01_sub_0	ZeroWireload	tcb018gbwp7ttc
sub_10_DW01_add_0	ZeroWireload	tcb018gbwp7ttc
sub_10_DW01_add_1	ZeroWireload	tcb018gbwp7ttc
sub_10_DW01_sub_1	ZeroWireload	tcb018gbwp7ttc
sub_10_DW01_sub_2	ZeroWireload	tcb018gbwp7ttc
sub_10_DW01_add_2	ZeroWireload	tcb018gbwp7ttc
sub_11_DW01_sub_0	ZeroWireload	tcb018gbwp7ttc
sub_11_DW01_add_0	ZeroWireload	tcb018gbwp7ttc
sub_11_DW01_add_1	ZeroWireload	tcb018gbwp7ttc

```
sub_11_DW01_sub_1      ZeroWireload      tcb018gbwp7ttc
sub_11_DW01_sub_2      ZeroWireload      tcb018gbwp7ttc
sub_11_DW01_add_2      ZeroWireload      tcb018gbwp7ttc
sub_12_DW01_sub_0      ZeroWireload      tcb018gbwp7ttc
sub_12_DW01_add_0      ZeroWireload      tcb018gbwp7ttc
sub_12_DW01_add_1      ZeroWireload      tcb018gbwp7ttc
sub_12_DW01_sub_1      ZeroWireload      tcb018gbwp7ttc
sub_12_DW01_sub_2      ZeroWireload      tcb018gbwp7ttc
sub_12_DW01_add_2      ZeroWireload      tcb018gbwp7ttc
sub_13_DW01_sub_0      ZeroWireload      tcb018gbwp7ttc
sub_13_DW01_add_0      ZeroWireload      tcb018gbwp7ttc
sub_13_DW01_add_1      ZeroWireload      tcb018gbwp7ttc
sub_13_DW01_sub_1      ZeroWireload      tcb018gbwp7ttc
sub_13_DW01_sub_2      ZeroWireload      tcb018gbwp7ttc
sub_13_DW01_add_2      ZeroWireload      tcb018gbwp7ttc
sub_14_DW01_sub_0      ZeroWireload      tcb018gbwp7ttc
sub_14_DW01_add_0      ZeroWireload      tcb018gbwp7ttc
sub_14_DW01_add_1      ZeroWireload      tcb018gbwp7ttc
sub_14_DW01_sub_1      ZeroWireload      tcb018gbwp7ttc
sub_14_DW01_sub_2      ZeroWireload      tcb018gbwp7ttc
sub_14_DW01_add_2      ZeroWireload      tcb018gbwp7ttc
sub_0_DW01_sub_0       ZeroWireload      tcb018gbwp7ttc
sub_0_DW01_add_0       ZeroWireload      tcb018gbwp7ttc
sub_0_DW01_add_1       ZeroWireload      tcb018gbwp7ttc
sub_0_DW01_sub_1       ZeroWireload      tcb018gbwp7ttc
sub_0_DW01_sub_2       ZeroWireload      tcb018gbwp7ttc
sub_0_DW01_add_2       ZeroWireload      tcb018gbwp7ttc


Global Operating Voltage = 1.8
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000pf
    Time Units = 1ns
    Dynamic Power Units = 1mW    (derived from V,C,T units)
    Leakage Power Units = 1nW


  Cell Internal Power  =  22.0327 mW   (91%)
  Net Switching Power  =   2.1519 mW    (9%)
                         ---------
Total Dynamic Power    =  24.1847 mW  (100%)

Cell Leakage Power     = 768.3253 nW


                 Internal         Switching           Leakage            Total
Power Group      Power            Power               Power              Power   (   %    )
Attrs
--------------------------------------------------------------------------------------------------
--
io_pad             0.0000           0.0000            0.0000            0.0000  (   0.00%)
memory             0.0000           0.0000            0.0000            0.0000  (   0.00%)
black_box          0.0000           0.0000            0.0000            0.0000  (   0.00%)
clock_network      0.0000           0.0000            0.0000            0.0000  (   0.00%)
```

```
register          16.8659            0.5224          202.7353           17.3885  (  71.90%)
sequential         0.0000            0.0000            0.0000            0.0000  (   0.00%)
combinational      5.1669            1.6295          565.5900            6.7969  (  28.10%)
--------------------------------------------------------------------------------------------------
--
Total             22.0327 mW         2.1519 mW       768.3253 nW        24.1854 mW
```

8.2.3. Power report (with saif file):

```
****************************************
Report : power
        -analysis_effort low
Design : CORDIC
Version: O-2018.06-SP4
Date   : Wed Mar 20 12:02:40 2019
****************************************


Library(s) Used:

    tcb018gbwp7ttc (File:
/home/synopsys/TSMCHOME/digital/Front_End/timing_power_noise/NLDM/tcb018gbwp7t_270a/tcb018gbwp7
ttc.db)


Operating Conditions: NCCOM   Library: tcb018gbwp7ttc
Wire Load Model Mode: segmented

Design        Wire Load Model            Library
------------------------------------------------
CORDIC                 ZeroWireload      tcb018gbwp7ttc
sub_0                  ZeroWireload      tcb018gbwp7ttc
sub_1                  ZeroWireload      tcb018gbwp7ttc
sub_2                  ZeroWireload      tcb018gbwp7ttc
sub_3                  ZeroWireload      tcb018gbwp7ttc
sub_4                  ZeroWireload      tcb018gbwp7ttc
sub_5                  ZeroWireload      tcb018gbwp7ttc
sub_6                  ZeroWireload      tcb018gbwp7ttc
sub_7                  ZeroWireload      tcb018gbwp7ttc
sub_8                  ZeroWireload      tcb018gbwp7ttc
sub_9                  ZeroWireload      tcb018gbwp7ttc
sub_10                 ZeroWireload      tcb018gbwp7ttc
sub_11                 ZeroWireload      tcb018gbwp7ttc
sub_12                 ZeroWireload      tcb018gbwp7ttc
sub_13                 ZeroWireload      tcb018gbwp7ttc
sub_14                 ZeroWireload      tcb018gbwp7ttc
sub_1_DW01_sub_0       ZeroWireload      tcb018gbwp7ttc
sub_1_DW01_add_0       ZeroWireload      tcb018gbwp7ttc
sub_1_DW01_add_1       ZeroWireload      tcb018gbwp7ttc
sub_1_DW01_sub_1       ZeroWireload      tcb018gbwp7ttc
sub_1_DW01_sub_2       ZeroWireload      tcb018gbwp7ttc
sub_1_DW01_add_2       ZeroWireload      tcb018gbwp7ttc
sub_2_DW01_sub_0       ZeroWireload      tcb018gbwp7ttc
sub_2_DW01_add_0       ZeroWireload      tcb018gbwp7ttc
sub_2_DW01_add_1       ZeroWireload      tcb018gbwp7ttc
```

sub_2_DW01_sub_1	ZeroWireload	tcb018gbwp7ttc
sub_2_DW01_sub_2	ZeroWireload	tcb018gbwp7ttc
sub_2_DW01_add_2	ZeroWireload	tcb018gbwp7ttc
sub_3_DW01_sub_0	ZeroWireload	tcb018gbwp7ttc
sub_3_DW01_add_0	ZeroWireload	tcb018gbwp7ttc
sub_3_DW01_add_1	ZeroWireload	tcb018gbwp7ttc
sub_3_DW01_sub_1	ZeroWireload	tcb018gbwp7ttc
sub_3_DW01_sub_2	ZeroWireload	tcb018gbwp7ttc
sub_3_DW01_add_2	ZeroWireload	tcb018gbwp7ttc
sub_4_DW01_sub_0	ZeroWireload	tcb018gbwp7ttc
sub_4_DW01_add_0	ZeroWireload	tcb018gbwp7ttc
sub_4_DW01_add_1	ZeroWireload	tcb018gbwp7ttc
sub_4_DW01_sub_1	ZeroWireload	tcb018gbwp7ttc
sub_4_DW01_sub_2	ZeroWireload	tcb018gbwp7ttc
sub_4_DW01_add_2	ZeroWireload	tcb018gbwp7ttc
sub_5_DW01_sub_0	ZeroWireload	tcb018gbwp7ttc
sub_5_DW01_add_0	ZeroWireload	tcb018gbwp7ttc
sub_5_DW01_add_1	ZeroWireload	tcb018gbwp7ttc
sub_5_DW01_sub_1	ZeroWireload	tcb018gbwp7ttc
sub_5_DW01_sub_2	ZeroWireload	tcb018gbwp7ttc
sub_5_DW01_add_2	ZeroWireload	tcb018gbwp7ttc
sub_6_DW01_sub_0	ZeroWireload	tcb018gbwp7ttc
sub_6_DW01_add_0	ZeroWireload	tcb018gbwp7ttc
sub_6_DW01_add_1	ZeroWireload	tcb018gbwp7ttc
sub_6_DW01_sub_1	ZeroWireload	tcb018gbwp7ttc
sub_6_DW01_sub_2	ZeroWireload	tcb018gbwp7ttc
sub_6_DW01_add_2	ZeroWireload	tcb018gbwp7ttc
sub_7_DW01_sub_0	ZeroWireload	tcb018gbwp7ttc
sub_7_DW01_add_0	ZeroWireload	tcb018gbwp7ttc
sub_7_DW01_add_1	ZeroWireload	tcb018gbwp7ttc
sub_7_DW01_sub_1	ZeroWireload	tcb018gbwp7ttc
sub_7_DW01_sub_2	ZeroWireload	tcb018gbwp7ttc
sub_7_DW01_add_2	ZeroWireload	tcb018gbwp7ttc
sub_8_DW01_sub_0	ZeroWireload	tcb018gbwp7ttc
sub_8_DW01_add_0	ZeroWireload	tcb018gbwp7ttc
sub_8_DW01_add_1	ZeroWireload	tcb018gbwp7ttc
sub_8_DW01_sub_1	ZeroWireload	tcb018gbwp7ttc
sub_8_DW01_sub_2	ZeroWireload	tcb018gbwp7ttc
sub_8_DW01_add_2	ZeroWireload	tcb018gbwp7ttc
sub_9_DW01_sub_0	ZeroWireload	tcb018gbwp7ttc
sub_9_DW01_add_0	ZeroWireload	tcb018gbwp7ttc
sub_9_DW01_add_1	ZeroWireload	tcb018gbwp7ttc
sub_9_DW01_sub_1	ZeroWireload	tcb018gbwp7ttc
sub_9_DW01_sub_2	ZeroWireload	tcb018gbwp7ttc
sub_9_DW01_add_2	ZeroWireload	tcb018gbwp7ttc
sub_10_DW01_sub_0	ZeroWireload	tcb018gbwp7ttc
sub_10_DW01_add_0	ZeroWireload	tcb018gbwp7ttc
sub_10_DW01_add_1	ZeroWireload	tcb018gbwp7ttc
sub_10_DW01_sub_1	ZeroWireload	tcb018gbwp7ttc
sub_10_DW01_sub_2	ZeroWireload	tcb018gbwp7ttc
sub_10_DW01_add_2	ZeroWireload	tcb018gbwp7ttc
sub_11_DW01_sub_0	ZeroWireload	tcb018gbwp7ttc
sub_11_DW01_add_0	ZeroWireload	tcb018gbwp7ttc
sub_11_DW01_add_1	ZeroWireload	tcb018gbwp7ttc
sub_11_DW01_sub_1	ZeroWireload	tcb018gbwp7ttc

```
sub_11_DW01_sub_2      ZeroWireload      tcb018gbwp7ttc
sub_11_DW01_add_2      ZeroWireload      tcb018gbwp7ttc
sub_12_DW01_sub_0      ZeroWireload      tcb018gbwp7ttc
sub_12_DW01_add_0      ZeroWireload      tcb018gbwp7ttc
sub_12_DW01_add_1      ZeroWireload      tcb018gbwp7ttc
sub_12_DW01_sub_1      ZeroWireload      tcb018gbwp7ttc
sub_12_DW01_sub_2      ZeroWireload      tcb018gbwp7ttc
sub_12_DW01_add_2      ZeroWireload      tcb018gbwp7ttc
sub_13_DW01_sub_0      ZeroWireload      tcb018gbwp7ttc
sub_13_DW01_add_0      ZeroWireload      tcb018gbwp7ttc
sub_13_DW01_add_1      ZeroWireload      tcb018gbwp7ttc
sub_13_DW01_sub_1      ZeroWireload      tcb018gbwp7ttc
sub_13_DW01_sub_2      ZeroWireload      tcb018gbwp7ttc
sub_13_DW01_add_2      ZeroWireload      tcb018gbwp7ttc
sub_14_DW01_sub_0      ZeroWireload      tcb018gbwp7ttc
sub_14_DW01_add_0      ZeroWireload      tcb018gbwp7ttc
sub_14_DW01_add_1      ZeroWireload      tcb018gbwp7ttc
sub_14_DW01_sub_1      ZeroWireload      tcb018gbwp7ttc
sub_14_DW01_sub_2      ZeroWireload      tcb018gbwp7ttc
sub_14_DW01_add_2      ZeroWireload      tcb018gbwp7ttc
sub_0_DW01_sub_0       ZeroWireload      tcb018gbwp7ttc
sub_0_DW01_add_0       ZeroWireload      tcb018gbwp7ttc
sub_0_DW01_add_1       ZeroWireload      tcb018gbwp7ttc
sub_0_DW01_sub_1       ZeroWireload      tcb018gbwp7ttc
sub_0_DW01_sub_2       ZeroWireload      tcb018gbwp7ttc
sub_0_DW01_add_2       ZeroWireload      tcb018gbwp7ttc


Global Operating Voltage = 1.8
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000pf
    Time Units = 1ns
    Dynamic Power Units = 1mW    (derived from V,C,T units)
    Leakage Power Units = 1nW


  Cell Internal Power  =  12.8745 mW   (99%)
  Net Switching Power  = 110.2280 uW    (1%)
                         ---------
Total Dynamic Power    =  12.9847 mW  (100%)

Cell Leakage Power     = 770.2385 nW


                 Internal         Switching           Leakage            Total
Power Group      Power            Power               Power              Power   (   %    )
Attrs
--------------------------------------------------------------------------------------------
---
io_pad             0.0000           0.0000            0.0000           0.0000  (   0.00%)
memory             0.0000           0.0000            0.0000           0.0000  (   0.00%)
black_box          0.0000           0.0000            0.0000           0.0000  (   0.00%)
clock_network      0.0000           0.0000            0.0000           0.0000  (   0.00%)
register          12.4811        3.4894e-02         203.1776          12.5162  (  96.39%)
```

```
sequential         0.0000            0.0000            0.0000            0.0000  (   0.00%)
combinational      0.3934        7.5333e-02          567.0609            0.4693  (   3.61%)
--------------------------------------------------------------------------------------------------
---
Total             12.8745 mW         0.1102 mW       770.2384 nW        12.9855 mW
```

8.2.4 Timing Report:

```
****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : CORDIC
Version: O-2018.06-SP4
Date   : Wed Mar 20 11:55:02 2019
****************************************

 # A fanout number of 1000 was used for high fanout net computations.

Operating Conditions: NCCOM   Library: tcb018gbwp7ttc
Wire Load Model Mode: segmented

  Startpoint: Yin[0] (input port clocked by clock)
  Endpoint: temp_xin_reg[16]
            (rising edge-triggered flip-flop clocked by clock)
  Path Group: clock
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  CORDIC             ZeroWireload          tcb018gbwp7ttc

  Point                                    Incr       Path
  -----------------------------------------------------------
  clock clock (rise edge)                  0.00       0.00
  clock network delay (ideal)              1.00       1.00
  input external delay                     4.00       5.00 f
  Yin[0] (in)                              0.00       5.00 f
  U67/ZN (INVD1BWP7T)                      0.05       5.05 r
  U188/Z (AN2D0BWP7T)                      0.14       5.19 r
  U186/Z (AN2D0BWP7T)                      0.15       5.33 r
  U184/Z (AN2D0BWP7T)                      0.15       5.48 r
  U182/Z (AN2D0BWP7T)                      0.15       5.62 r
  U180/Z (AN2D0BWP7T)                      0.15       5.77 r
  U178/Z (AN2D0BWP7T)                      0.15       5.92 r
  U176/Z (AN2D0BWP7T)                      0.15       6.06 r
  U174/Z (AN2D0BWP7T)                      0.15       6.21 r
  U172/Z (AN2D0BWP7T)                      0.15       6.35 r
  U170/Z (AN2D0BWP7T)                      0.15       6.50 r
  U168/Z (AN2D0BWP7T)                      0.15       6.64 r
  U166/Z (AN2D0BWP7T)                      0.15       6.79 r
  U164/Z (AN2D0BWP7T)                      0.15       6.93 r
  U162/Z (AN2D0BWP7T)                      0.15       7.08 r
  U160/Z (AN2D0BWP7T)                      0.11       7.19 r
```

```
  U159/Z (CKXOR2D0BWP7T)                   0.20       7.39 f
  U50/Z (AO21D0BWP7T)                      0.14       7.53 f
  temp_xin_reg[16]/D (DFQD1BWP7T)          0.00       7.53 f
  data arrival time                                   7.53

  clock clock (rise edge)                 10.00      10.00
  clock network delay (ideal)              1.00      11.00
  clock uncertainty                       -1.00      10.00
  temp_xin_reg[16]/CP (DFQD1BWP7T)         0.00      10.00 r
  library setup time                      -0.02       9.98
  data required time                                  9.98
  ---------------------------------------------------------
  data required time                                  9.98
  data arrival time                                  -7.53
  ---------------------------------------------------------
  slack (MET)                                         2.46
```

8.3. Using library: SCL

8.3.1.Area report

```
****************************************
Report : area
Design : CORDIC
Version: O-2018.06-SP4
Date   : Wed Mar 20 11:50:03 2019
****************************************

Information: Updating design information... (UID-85)
Warning: Design 'CORDIC' contains 1 high-fanout nets. A fanout number of 1000 will be used
for delay calculations involving these nets. (TIM-134)
Library(s) Used:

    tsl18fs120_scl_ss (File:
/home/synopsys/pdk/scl_pdk/stdlib/fs120/liberty/lib_flow_ss/tsl18fs120_scl_ss.db)

Number of ports:                         8274
Number of nets:                         19314
Number of cells:                         9681
Number of combinational cells:           8355
Number of sequential cells:              1056
Number of macros/black boxes:               0
Number of buf/inv:                       2269
Number of references:                      27

Combinational area:             214700.723053
Buf/Inv area:                    15496.629945
Noncombinational area:           62916.481934
Macro/Black Box area:                0.000000
Net Interconnect area:            7626.815272

Total cell area:                277617.204987
Total area:                     285244.020259
```

8.3.2. Power report (without saif file):

```
****************************************
```

```
Report : power
        -analysis_effort low
Design : CORDIC
Version: O-2018.06-SP4
Date   : Wed Mar 20 11:50:06 2019
****************************************


Library(s) Used:

    tsl18fs120_scl_ss (File:
/home/synopsys/pdk/scl_pdk/stdlib/fs120/liberty/lib_flow_ss/tsl18fs120_scl_ss.db)


Operating Conditions: tsl18fs120_scl_ss   Library: tsl18fs120_scl_ss
Wire Load Model Mode: segmented

Design        Wire Load Model            Library
------------------------------------------------
CORDIC                 8000              tsl18fs120_scl_ss
sub_0                  35000             tsl18fs120_scl_ss
sub_1                  35000             tsl18fs120_scl_ss
sub_2                  35000             tsl18fs120_scl_ss
sub_3                  35000             tsl18fs120_scl_ss
sub_4                  35000             tsl18fs120_scl_ss
sub_5                  35000             tsl18fs120_scl_ss
sub_6                  35000             tsl18fs120_scl_ss
sub_7                  35000             tsl18fs120_scl_ss
sub_8                  35000             tsl18fs120_scl_ss
sub_9                  35000             tsl18fs120_scl_ss
sub_10                 35000             tsl18fs120_scl_ss
sub_11                 35000             tsl18fs120_scl_ss
sub_12                 35000             tsl18fs120_scl_ss
sub_13                 35000             tsl18fs120_scl_ss
sub_14                 35000             tsl18fs120_scl_ss
sub_1_DW01_sub_0       4000              tsl18fs120_scl_ss
sub_1_DW01_add_0       4000              tsl18fs120_scl_ss
sub_1_DW01_add_1       4000              tsl18fs120_scl_ss
sub_1_DW01_sub_1       4000              tsl18fs120_scl_ss
sub_1_DW01_sub_2       4000              tsl18fs120_scl_ss
sub_1_DW01_add_2       4000              tsl18fs120_scl_ss
sub_2_DW01_sub_0       4000              tsl18fs120_scl_ss
sub_2_DW01_add_0       4000              tsl18fs120_scl_ss
sub_2_DW01_add_1       4000              tsl18fs120_scl_ss
sub_2_DW01_sub_1       4000              tsl18fs120_scl_ss
sub_2_DW01_sub_2       4000              tsl18fs120_scl_ss
sub_2_DW01_add_2       4000              tsl18fs120_scl_ss
sub_3_DW01_sub_0       4000              tsl18fs120_scl_ss
sub_3_DW01_add_0       4000              tsl18fs120_scl_ss
sub_3_DW01_add_1       4000              tsl18fs120_scl_ss
sub_3_DW01_sub_1       4000              tsl18fs120_scl_ss
sub_3_DW01_sub_2       4000              tsl18fs120_scl_ss
sub_3_DW01_add_2       4000              tsl18fs120_scl_ss
sub_4_DW01_sub_0       4000              tsl18fs120_scl_ss
sub_4_DW01_add_0       4000              tsl18fs120_scl_ss
```

sub_4_DW01_add_1	4000	tsl18fs120_scl_ss
sub_4_DW01_sub_1	4000	tsl18fs120_scl_ss
sub_4_DW01_sub_2	4000	tsl18fs120_scl_ss
sub_4_DW01_add_2	4000	tsl18fs120_scl_ss
sub_5_DW01_sub_0	4000	tsl18fs120_scl_ss
sub_5_DW01_add_0	4000	tsl18fs120_scl_ss
sub_5_DW01_add_1	4000	tsl18fs120_scl_ss
sub_5_DW01_sub_1	4000	tsl18fs120_scl_ss
sub_5_DW01_sub_2	4000	tsl18fs120_scl_ss
sub_5_DW01_add_2	4000	tsl18fs120_scl_ss
sub_6_DW01_sub_0	4000	tsl18fs120_scl_ss
sub_6_DW01_add_0	4000	tsl18fs120_scl_ss
sub_6_DW01_add_1	4000	tsl18fs120_scl_ss
sub_6_DW01_sub_1	4000	tsl18fs120_scl_ss
sub_6_DW01_sub_2	4000	tsl18fs120_scl_ss
sub_6_DW01_add_2	4000	tsl18fs120_scl_ss
sub_7_DW01_sub_0	4000	tsl18fs120_scl_ss
sub_7_DW01_add_0	4000	tsl18fs120_scl_ss
sub_7_DW01_add_1	4000	tsl18fs120_scl_ss
sub_7_DW01_sub_1	4000	tsl18fs120_scl_ss
sub_7_DW01_sub_2	4000	tsl18fs120_scl_ss
sub_7_DW01_add_2	4000	tsl18fs120_scl_ss
sub_8_DW01_sub_0	4000	tsl18fs120_scl_ss
sub_8_DW01_add_0	4000	tsl18fs120_scl_ss
sub_8_DW01_add_1	4000	tsl18fs120_scl_ss
sub_8_DW01_sub_1	4000	tsl18fs120_scl_ss
sub_8_DW01_sub_2	4000	tsl18fs120_scl_ss
sub_8_DW01_add_2	4000	tsl18fs120_scl_ss
sub_9_DW01_sub_0	4000	tsl18fs120_scl_ss
sub_9_DW01_add_0	4000	tsl18fs120_scl_ss
sub_9_DW01_add_1	4000	tsl18fs120_scl_ss
sub_9_DW01_sub_1	4000	tsl18fs120_scl_ss
sub_9_DW01_sub_2	4000	tsl18fs120_scl_ss
sub_9_DW01_add_2	4000	tsl18fs120_scl_ss
sub_10_DW01_sub_0	4000	tsl18fs120_scl_ss
sub_10_DW01_add_0	4000	tsl18fs120_scl_ss
sub_10_DW01_add_1	4000	tsl18fs120_scl_ss
sub_10_DW01_sub_1	4000	tsl18fs120_scl_ss
sub_10_DW01_sub_2	4000	tsl18fs120_scl_ss
sub_10_DW01_add_2	4000	tsl18fs120_scl_ss
sub_11_DW01_sub_0	4000	tsl18fs120_scl_ss
sub_11_DW01_add_0	4000	tsl18fs120_scl_ss
sub_11_DW01_add_1	4000	tsl18fs120_scl_ss
sub_11_DW01_sub_1	4000	tsl18fs120_scl_ss
sub_11_DW01_sub_2	4000	tsl18fs120_scl_ss
sub_11_DW01_add_2	4000	tsl18fs120_scl_ss
sub_12_DW01_sub_0	4000	tsl18fs120_scl_ss
sub_12_DW01_add_0	4000	tsl18fs120_scl_ss
sub_12_DW01_add_1	4000	tsl18fs120_scl_ss
sub_12_DW01_sub_1	4000	tsl18fs120_scl_ss
sub_12_DW01_sub_2	4000	tsl18fs120_scl_ss
sub_12_DW01_add_2	4000	tsl18fs120_scl_ss
sub_13_DW01_sub_0	4000	tsl18fs120_scl_ss
sub_13_DW01_add_0	4000	tsl18fs120_scl_ss
sub_13_DW01_add_1	4000	tsl18fs120_scl_ss

```
sub_13_DW01_sub_1      4000              tsl18fs120_scl_ss
sub_13_DW01_sub_2      4000              tsl18fs120_scl_ss
sub_13_DW01_add_2      4000              tsl18fs120_scl_ss
sub_14_DW01_sub_0      4000              tsl18fs120_scl_ss
sub_14_DW01_add_0      4000              tsl18fs120_scl_ss
sub_14_DW01_add_1      4000              tsl18fs120_scl_ss
sub_14_DW01_sub_1      4000              tsl18fs120_scl_ss
sub_14_DW01_sub_2      4000              tsl18fs120_scl_ss
sub_14_DW01_add_2      4000              tsl18fs120_scl_ss
sub_0_DW01_sub_0       4000              tsl18fs120_scl_ss
sub_0_DW01_add_0       4000              tsl18fs120_scl_ss
sub_0_DW01_add_1       4000              tsl18fs120_scl_ss
sub_0_DW01_sub_1       4000              tsl18fs120_scl_ss
sub_0_DW01_sub_2       4000              tsl18fs120_scl_ss
sub_0_DW01_add_2       4000              tsl18fs120_scl_ss


Global Operating Voltage = 1.62
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000pf
    Time Units = 1ns
    Dynamic Power Units = 1mW    (derived from V,C,T units)
    Leakage Power Units = 1pW


  Cell Internal Power  =   8.9778 mW   (67%)
  Net Switching Power  =   4.3486 mW   (33%)
                         ---------
Total Dynamic Power    =  13.3264 mW  (100%)

Cell Leakage Power     =   3.7609 uW


                 Internal         Switching           Leakage            Total
Power Group      Power            Power               Power              Power   (   %
)  Attrs
--------------------------------------------------------------------------------------------
--------
io_pad             0.0000           0.0000            0.0000            0.0000  (
0.00%)
memory             0.0000           0.0000            0.0000            0.0000  (
0.00%)
black_box          0.0000           0.0000            0.0000            0.0000  (
0.00%)
clock_network      0.0000           0.0000            0.0000            0.0000  (
0.00%)
register           6.1161           1.6089        8.3118e+05            7.7259  (
57.96%)
sequential         0.0000           0.0000            0.0000            0.0000  (
0.00%)
combinational      2.8617           2.7397        2.9297e+06            5.6043  (
42.04%)
--------------------------------------------------------------------------------------------
--------
```

```
     Total              8.9778 mW         4.3486 mW     3.7609e+06 pW        13.3302 mW
```

8.3.3. Power report (with saif file):

```
****************************************
Report : power
        -analysis_effort low
Design : CORDIC
Version: O-2018.06-SP4
Date   : Wed Mar 20 12:10:23 2019
****************************************


Library(s) Used:

    tsl18fs120_scl_ss (File:
/home/synopsys/pdk/scl_pdk/stdlib/fs120/liberty/lib_flow_ss/tsl18fs120_scl_ss.db)


Operating Conditions: tsl18fs120_scl_ss   Library: tsl18fs120_scl_ss
Wire Load Model Mode: segmented

Design        Wire Load Model            Library
------------------------------------------------
CORDIC                 8000              tsl18fs120_scl_ss
sub_0                  35000             tsl18fs120_scl_ss
sub_1                  35000             tsl18fs120_scl_ss
sub_2                  35000             tsl18fs120_scl_ss
sub_3                  35000             tsl18fs120_scl_ss
sub_4                  35000             tsl18fs120_scl_ss
sub_5                  35000             tsl18fs120_scl_ss
sub_6                  35000             tsl18fs120_scl_ss
sub_7                  35000             tsl18fs120_scl_ss
sub_8                  35000             tsl18fs120_scl_ss
sub_9                  35000             tsl18fs120_scl_ss
sub_10                 35000             tsl18fs120_scl_ss
sub_11                 35000             tsl18fs120_scl_ss
sub_12                 35000             tsl18fs120_scl_ss
sub_13                 35000             tsl18fs120_scl_ss
sub_14                 35000             tsl18fs120_scl_ss
sub_1_DW01_sub_0       4000              tsl18fs120_scl_ss
sub_1_DW01_add_0       4000              tsl18fs120_scl_ss
sub_1_DW01_add_1       4000              tsl18fs120_scl_ss
sub_1_DW01_sub_1       4000              tsl18fs120_scl_ss
sub_1_DW01_sub_2       4000              tsl18fs120_scl_ss
sub_1_DW01_add_2       4000              tsl18fs120_scl_ss
sub_2_DW01_sub_0       4000              tsl18fs120_scl_ss
sub_2_DW01_add_0       4000              tsl18fs120_scl_ss
sub_2_DW01_add_1       4000              tsl18fs120_scl_ss
sub_2_DW01_sub_1       4000              tsl18fs120_scl_ss
sub_2_DW01_sub_2       4000              tsl18fs120_scl_ss
sub_2_DW01_add_2       4000              tsl18fs120_scl_ss
sub_3_DW01_sub_0       4000              tsl18fs120_scl_ss
sub_3_DW01_add_0       4000              tsl18fs120_scl_ss
sub_3_DW01_add_1       4000              tsl18fs120_scl_ss
```

```
sub_3_DW01_sub_1       4000              tsl18fs120_scl_ss
sub_3_DW01_sub_2       4000              tsl18fs120_scl_ss
sub_3_DW01_add_2       4000              tsl18fs120_scl_ss
sub_4_DW01_sub_0       4000              tsl18fs120_scl_ss
sub_4_DW01_add_0       4000              tsl18fs120_scl_ss
sub_4_DW01_add_1       4000              tsl18fs120_scl_ss
sub_4_DW01_sub_1       4000              tsl18fs120_scl_ss
sub_4_DW01_sub_2       4000              tsl18fs120_scl_ss
sub_4_DW01_add_2       4000              tsl18fs120_scl_ss
sub_5_DW01_sub_0       4000              tsl18fs120_scl_ss
sub_5_DW01_add_0       4000              tsl18fs120_scl_ss
sub_5_DW01_add_1       4000              tsl18fs120_scl_ss
sub_5_DW01_sub_1       4000              tsl18fs120_scl_ss
sub_5_DW01_sub_2       4000              tsl18fs120_scl_ss
sub_5_DW01_add_2       4000              tsl18fs120_scl_ss
sub_6_DW01_sub_0       4000              tsl18fs120_scl_ss
sub_6_DW01_add_0       4000              tsl18fs120_scl_ss
sub_6_DW01_add_1       4000              tsl18fs120_scl_ss
sub_6_DW01_sub_1       4000              tsl18fs120_scl_ss
sub_6_DW01_sub_2       4000              tsl18fs120_scl_ss
sub_6_DW01_add_2       4000              tsl18fs120_scl_ss
sub_7_DW01_sub_0       4000              tsl18fs120_scl_ss
sub_7_DW01_add_0       4000              tsl18fs120_scl_ss
sub_7_DW01_add_1       4000              tsl18fs120_scl_ss
sub_7_DW01_sub_1       4000              tsl18fs120_scl_ss
sub_7_DW01_sub_2       4000              tsl18fs120_scl_ss
sub_7_DW01_add_2       4000              tsl18fs120_scl_ss
sub_8_DW01_sub_0       4000              tsl18fs120_scl_ss
sub_8_DW01_add_0       4000              tsl18fs120_scl_ss
sub_8_DW01_add_1       4000              tsl18fs120_scl_ss
sub_8_DW01_sub_1       4000              tsl18fs120_scl_ss
sub_8_DW01_sub_2       4000              tsl18fs120_scl_ss
sub_8_DW01_add_2       4000              tsl18fs120_scl_ss
sub_9_DW01_sub_0       4000              tsl18fs120_scl_ss
sub_9_DW01_add_0       4000              tsl18fs120_scl_ss
sub_9_DW01_add_1       4000              tsl18fs120_scl_ss
sub_9_DW01_sub_1       4000              tsl18fs120_scl_ss
sub_9_DW01_sub_2       4000              tsl18fs120_scl_ss
sub_9_DW01_add_2       4000              tsl18fs120_scl_ss
sub_10_DW01_sub_0      4000              tsl18fs120_scl_ss
sub_10_DW01_add_0      4000              tsl18fs120_scl_ss
sub_10_DW01_add_1      4000              tsl18fs120_scl_ss
sub_10_DW01_sub_1      4000              tsl18fs120_scl_ss
sub_10_DW01_sub_2      4000              tsl18fs120_scl_ss
sub_10_DW01_add_2      4000              tsl18fs120_scl_ss
sub_11_DW01_sub_0      4000              tsl18fs120_scl_ss
sub_11_DW01_add_0      4000              tsl18fs120_scl_ss
sub_11_DW01_add_1      4000              tsl18fs120_scl_ss
sub_11_DW01_sub_1      4000              tsl18fs120_scl_ss
sub_11_DW01_sub_2      4000              tsl18fs120_scl_ss
sub_11_DW01_add_2      4000              tsl18fs120_scl_ss
sub_12_DW01_sub_0      4000              tsl18fs120_scl_ss
sub_12_DW01_add_0      4000              tsl18fs120_scl_ss
sub_12_DW01_add_1      4000              tsl18fs120_scl_ss
sub_12_DW01_sub_1      4000              tsl18fs120_scl_ss
```

```
sub_12_DW01_sub_2      4000              tsl18fs120_scl_ss
sub_12_DW01_add_2      4000              tsl18fs120_scl_ss
sub_13_DW01_sub_0      4000              tsl18fs120_scl_ss
sub_13_DW01_add_0      4000              tsl18fs120_scl_ss
sub_13_DW01_add_1      4000              tsl18fs120_scl_ss
sub_13_DW01_sub_1      4000              tsl18fs120_scl_ss
sub_13_DW01_sub_2      4000              tsl18fs120_scl_ss
sub_13_DW01_add_2      4000              tsl18fs120_scl_ss
sub_14_DW01_sub_0      4000              tsl18fs120_scl_ss
sub_14_DW01_add_0      4000              tsl18fs120_scl_ss
sub_14_DW01_add_1      4000              tsl18fs120_scl_ss
sub_14_DW01_sub_1      4000              tsl18fs120_scl_ss
sub_14_DW01_sub_2      4000              tsl18fs120_scl_ss
sub_14_DW01_add_2      4000              tsl18fs120_scl_ss
sub_0_DW01_sub_0       4000              tsl18fs120_scl_ss
sub_0_DW01_add_0       4000              tsl18fs120_scl_ss
sub_0_DW01_add_1       4000              tsl18fs120_scl_ss
sub_0_DW01_sub_1       4000              tsl18fs120_scl_ss
sub_0_DW01_sub_2       4000              tsl18fs120_scl_ss
sub_0_DW01_add_2       4000              tsl18fs120_scl_ss


Global Operating Voltage = 1.62
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000pf
    Time Units = 1ns
    Dynamic Power Units = 1mW    (derived from V,C,T units)
    Leakage Power Units = 1pW


  Cell Internal Power  =   5.5942 mW   (94%)
  Net Switching Power  = 333.8173 uW    (6%)
                         ---------
Total Dynamic Power    =   5.9280 mW  (100%)

Cell Leakage Power     =   3.7609 uW


                 Internal         Switching           Leakage            Total
Power Group      Power            Power               Power              Power   (   %    )
Attrs
--------------------------------------------------------------------------------------------
---
io_pad             0.0000           0.0000            0.0000            0.0000  (   0.00%)
memory             0.0000           0.0000            0.0000            0.0000  (   0.00%)
black_box          0.0000           0.0000            0.0000            0.0000  (   0.00%)
clock_network      0.0000           0.0000            0.0000            0.0000  (   0.00%)
register           5.3382           0.1390        8.3118e+05            5.4780  (  92.35%)
sequential         0.0000           0.0000            0.0000            0.0000  (   0.00%)
combinational      0.2560           0.1948        2.9297e+06            0.4538  (   7.65%)
--------------------------------------------------------------------------------------------
---
Total              5.5942 mW        0.3338 mW     3.7609e+06 pW         5.9318 mW
```

8.3.4 Timing Report:

```
****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : CORDIC
Version: O-2018.06-SP4
Date   : Wed Mar 20 11:50:04 2019
****************************************

 # A fanout number of 1000 was used for high fanout net computations.

Operating Conditions: tsl18fs120_scl_ss   Library: tsl18fs120_scl_ss
Wire Load Model Mode: segmented

  Startpoint: XYZ[0].c1/temp_x_out_reg[1]
              (rising edge-triggered flip-flop clocked by clock)
  Endpoint: XYZ[1].c1/temp_y_out_reg[16]
            (rising edge-triggered flip-flop clocked by clock)
  Path Group: clock
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  sub_14             35000                 tsl18fs120_scl_ss
  sub_13             35000                 tsl18fs120_scl_ss
  sub_12             35000                 tsl18fs120_scl_ss
  sub_11             35000                 tsl18fs120_scl_ss
  sub_10             35000                 tsl18fs120_scl_ss
  sub_9              35000                 tsl18fs120_scl_ss
  sub_8              35000                 tsl18fs120_scl_ss
  sub_7              35000                 tsl18fs120_scl_ss
  sub_6              35000                 tsl18fs120_scl_ss
  sub_5              35000                 tsl18fs120_scl_ss
  sub_4              35000                 tsl18fs120_scl_ss
  sub_3              35000                 tsl18fs120_scl_ss
  sub_2              35000                 tsl18fs120_scl_ss
  sub_1              35000                 tsl18fs120_scl_ss
  CORDIC             8000                  tsl18fs120_scl_ss
  sub_0              35000                 tsl18fs120_scl_ss
  sub_14_DW01_add_2  4000                  tsl18fs120_scl_ss
  sub_14_DW01_sub_2  4000                  tsl18fs120_scl_ss
  sub_14_DW01_sub_1  4000                  tsl18fs120_scl_ss
  sub_14_DW01_add_1  4000                  tsl18fs120_scl_ss

  Point                                                   Incr       Path
  ------------------------------------------------------------------------
  clock clock (rise edge)                                 0.00       0.00
  clock network delay (ideal)                             1.00       1.00
  XYZ[0].c1/temp_x_out_reg[1]/CP (dfnrq1)                 0.00 #     1.00 r
  XYZ[0].c1/temp_x_out_reg[1]/Q (dfnrq1)                  0.83       1.83 r
  XYZ[0].c1/x_out[1] (sub_0)                              0.00       1.83 r
  XYZ[1].c1/x_in[1] (sub_14)                              0.00       1.83 r
  XYZ[1].c1/U259/ZN (aoi221d1)                            0.23       2.06 f
  XYZ[1].c1/U265/ZN (oai221d1)                            0.63       2.70 r
```

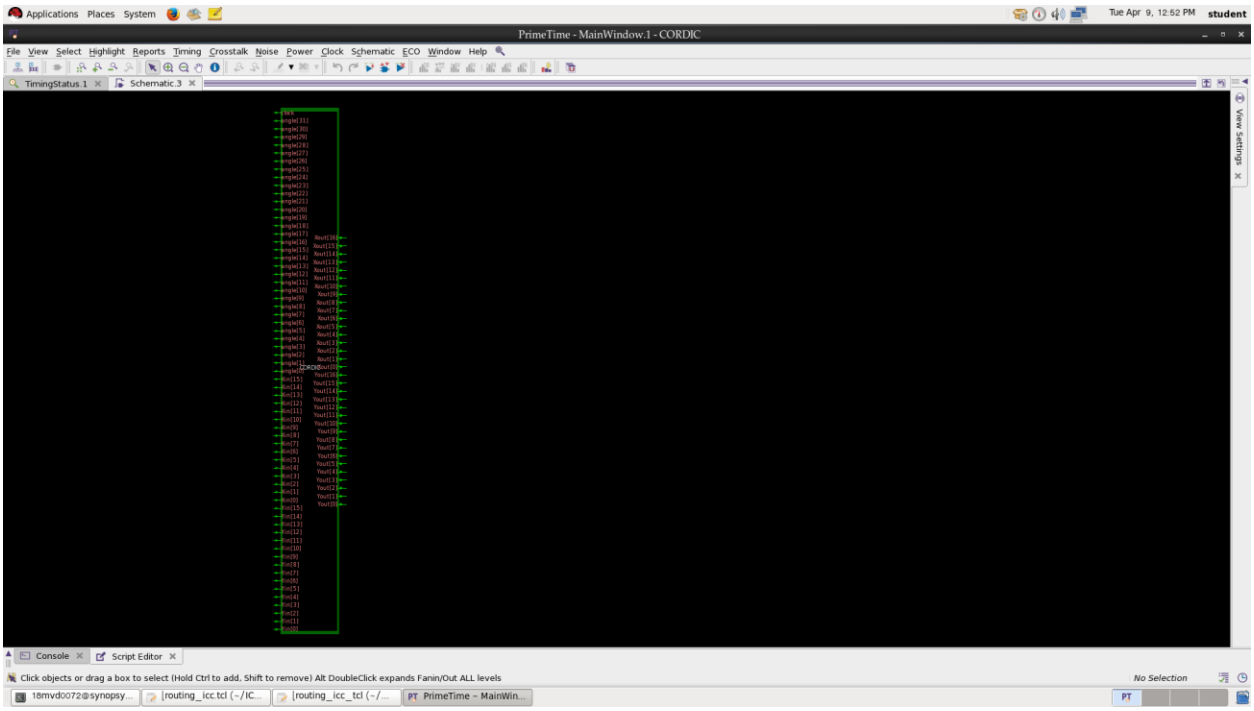
```
XYZ[1].c1/sub_153/B[1] (sub_14_DW01_sub_1)              0.00       2.70 r
XYZ[1].c1/sub_153/U3/ZN (inv0d0)                        0.41       3.10 f
XYZ[1].c1/sub_153/U2_1/CO (ad01d1)                      0.63       3.73 f
XYZ[1].c1/sub_153/U2_2/CO (ad01d1)                      0.41       4.14 f
XYZ[1].c1/sub_153/U2_3/CO (ad01d1)                      0.41       4.55 f
XYZ[1].c1/sub_153/U2_4/CO (ad01d1)                      0.41       4.96 f
XYZ[1].c1/sub_153/U2_5/CO (ad01d1)                      0.41       5.37 f
XYZ[1].c1/sub_153/U2_6/CO (ad01d1)                      0.41       5.78 f
XYZ[1].c1/sub_153/U2_7/CO (ad01d1)                      0.41       6.19 f
XYZ[1].c1/sub_153/U2_8/CO (ad01d1)                      0.41       6.60 f
XYZ[1].c1/sub_153/U2_9/CO (ad01d1)                      0.41       7.01 f
XYZ[1].c1/sub_153/U2_10/CO (ad01d1)                     0.41       7.42 f
XYZ[1].c1/sub_153/U2_11/CO (ad01d1)                     0.41       7.83 f
XYZ[1].c1/sub_153/U2_12/CO (ad01d1)                     0.41       8.24 f
XYZ[1].c1/sub_153/U2_13/CO (ad01d1)                     0.41       8.65 f
XYZ[1].c1/sub_153/U2_14/CO (ad01d1)                     0.41       9.06 f
XYZ[1].c1/sub_153/U2_15/CO (ad01d1)                     0.36       9.42 f
XYZ[1].c1/sub_153/U2_16/Z (xr03d1)                      0.55       9.97 f
XYZ[1].c1/sub_153/DIFF[16] (sub_14_DW01_sub_1)          0.00       9.97 f
XYZ[1].c1/U139/Z (aor22d1)                              0.26      10.23 f
XYZ[1].c1/temp_y_out_reg[16]/D (dfnrq1)                 0.00      10.23 f
data arrival time                                                 10.23

clock clock (rise edge)                                10.00      10.00
clock network delay (ideal)                             1.00      11.00
XYZ[1].c1/temp_y_out_reg[16]/CP (dfnrq1)                0.00      11.00 r
library setup time                                     -0.16      10.84
data required time                                                10.84
-----------------------------------------------------------------------------
data required time                                                10.84
data arrival time                                                -10.23
-----------------------------------------------------------------------------
slack (MET)                                                       0.60
```

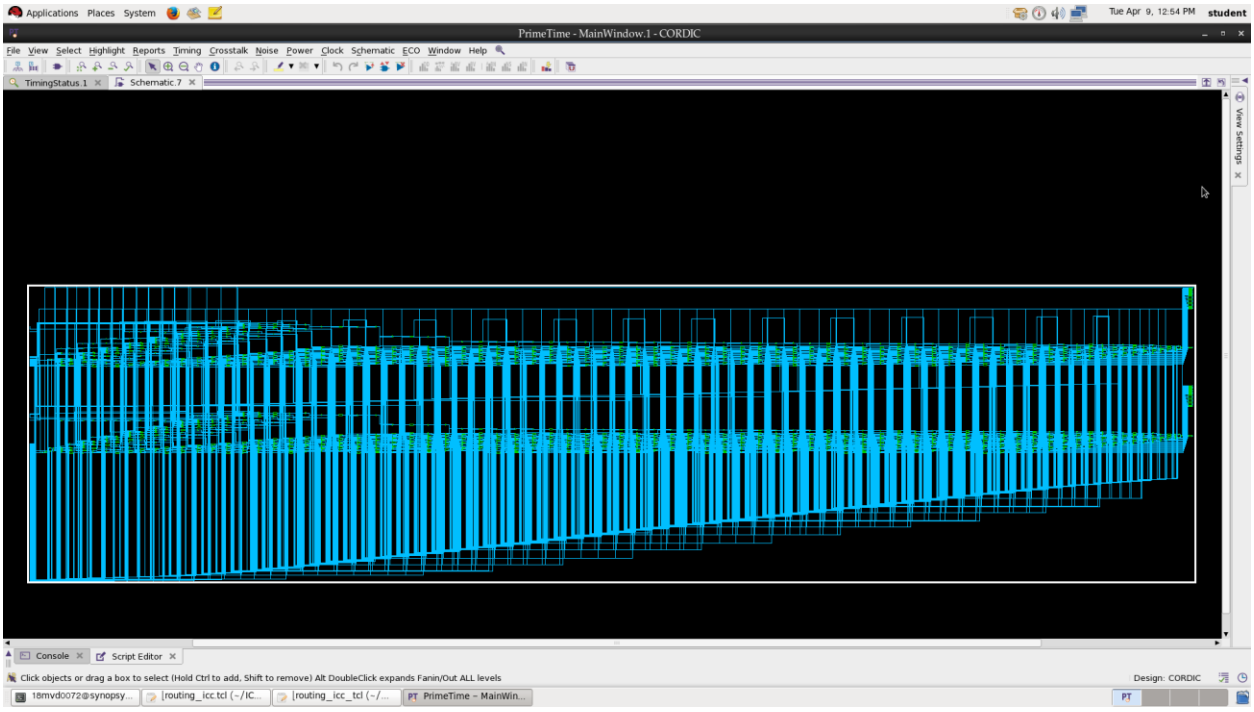
9. Timing Report from PT

9.1. SCL Library:

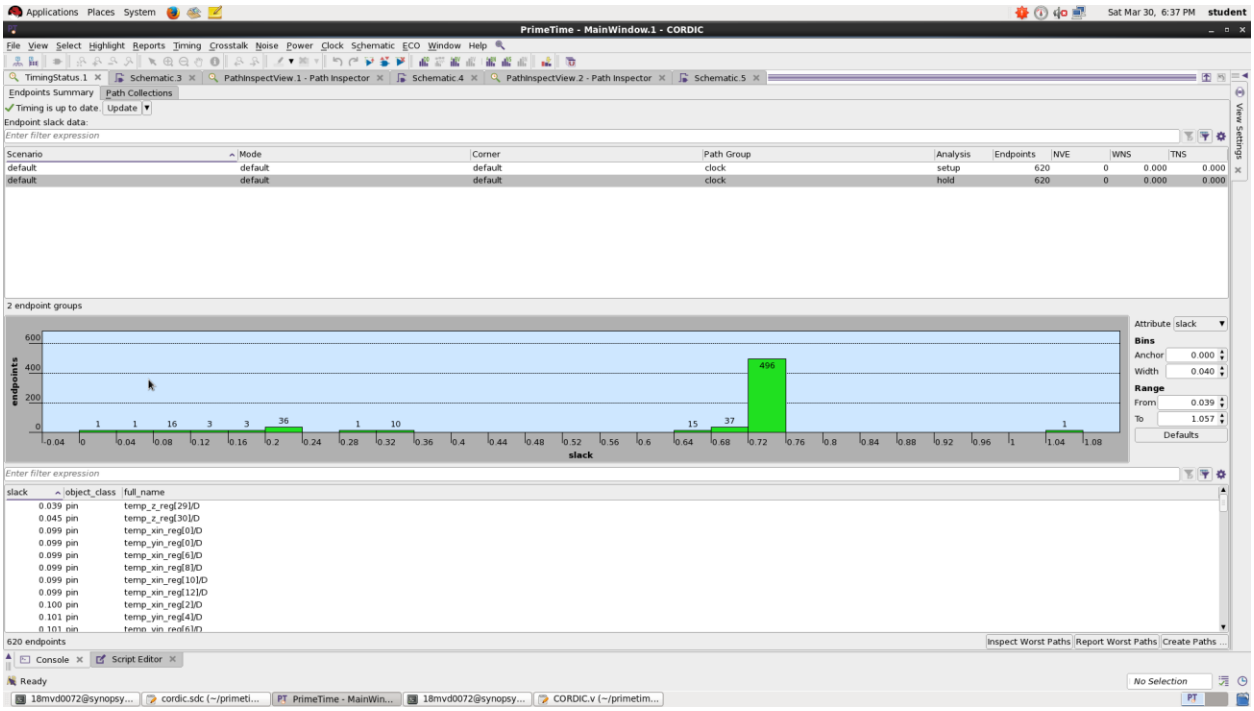
Block View:



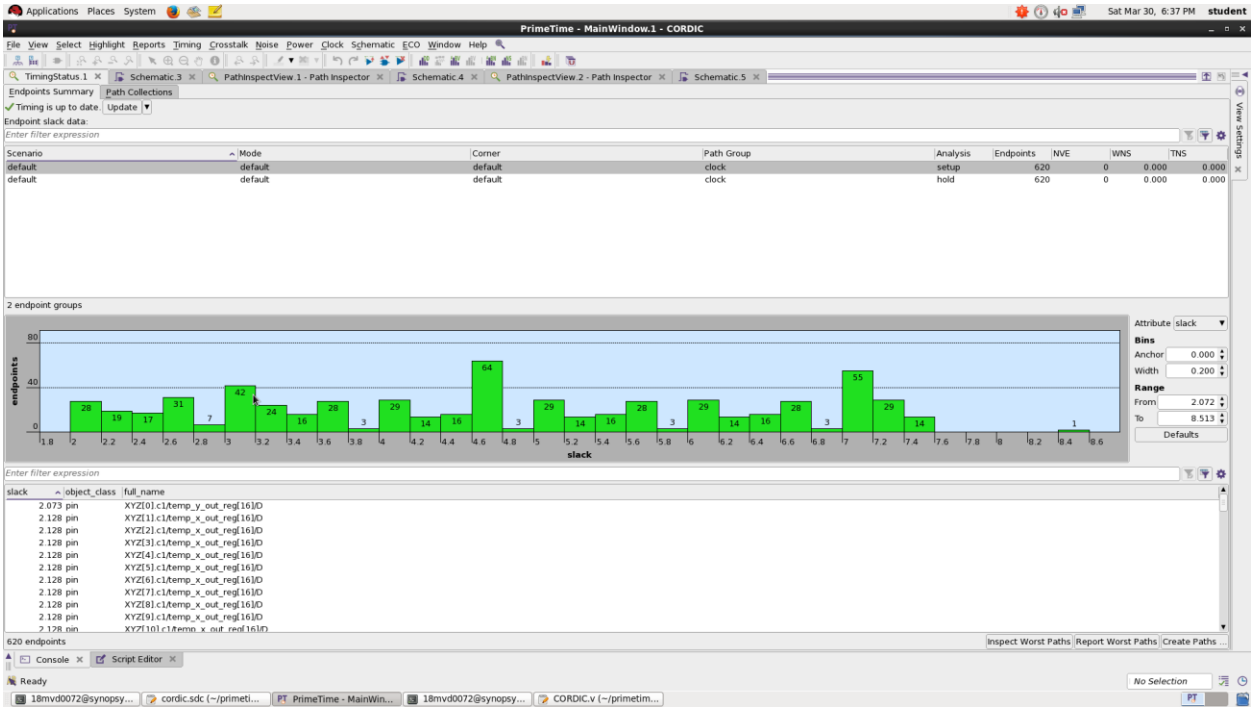
Gate-Level View:



Constraint for Setup time:



Constraint for Hold Time:



10. Comparison Table

Sl No	Reports	Without saif		
		Saed library	tsmc library	scl library
1	Area Report	133210.827512	206430.024748	277617.204987
2	Power Report	5.0921e+03 uW	24.1847 mW	13.3302 mW
3	Timing Report	MET Slack=3.07	MET Slack=2.46	MET Slack=0.6

Sl No	Reports	With saif		
		Saed library	tsmc library	scl library
1	Area Report	133210.827512	206430.024748	277617.204987
2	Power Report	2.9915e+03 uW	12.9855 mW	5.9318 mW
3	Constraint Report	MET	MET	MET
4	Timing Report	MET Slack=3.07	MET Slack=2.46	MET Slack=0.6

11. Physical Design Setup

```
Information: No layer mapping file is specified. Assume layer names are the
same between the technology library and the ITF. (RCEX-071)
Error: Library 'CORDIC.mw' already exists. (MWUI-004)
Loading db file
'/home/synopsys/pdk/scl_pdk/stdlib/fs120/liberty/lib_flow_ss/tsl18fs120_scl_ss.
db'
Warning: Unit conflict found: Milkyway technology file current unit is mA; main
library current unit is uA. (IFS-007)
Loading db file '/home/synopsys/installs/icc/O-2018.06-
SP4/libraries/syn/gtech.db'
Loading db file '/home/synopsys/installs/icc/O-2018.06-
SP4/libraries/syn/standard.sldb'
Information: linking reference library :
/home/synopsys/pdk/scl_pdk/stdlib//fs120/mw/fs120_scl. (PSYN-878)
  Loading link library 'tsl18fs120_scl_ss'
  Loading link library 'gtech'
Reading ddc file '/home/userdata/18mvd0072/primetime/CORDIC_topo1.ddc'.
Loaded 1 design.
```

```
Current design is 'CORDIC'.
Current design is 'CORDIC'.

  Linking design 'CORDIC'
  Using the following designs and libraries:
  --------------------------------------------------------------------------
  CORDIC
/home/userdata/18mvd0072/primetime/CORDIC_topo1.ddc
  tsl18fs120_scl_ss (library)
/home/synopsys/pdk/scl_pdk/stdlib/fs120/liberty/lib_flow_ss/tsl18fs120_scl_ss.d
b

Info: Creating auto CEL.
Information: Performing CEL netlist consistency check. (MWDC-118)
Information: CEL consistency check PASSED. (MWDC-119)
Information: Saved design named CORDIC. (UIG-5)
Information: Saved design named CORDIC. (UIG-5)
Current design is 'CORDIC'.

  Linking design 'CORDIC'
  Using the following designs and libraries:
  --------------------------------------------------------------------------
  CORDIC
/home/userdata/18mvd0072/primetime/CORDIC_topo1.ddc
  tsl18fs120_scl_ss (library)
/home/synopsys/pdk/scl_pdk/stdlib/fs120/liberty/lib_flow_ss/tsl18fs120_scl_ss.d
b

Information: Saved design named CORDIC. (UIG-5)
1
icc_shell> source ./floorplan_icc.tcl
 + VUE INFO: Please click Verification->IC Validator VUE in LayoutWindow menu
to launch VUE.

 + VUE INFO: Found a usable port: 2445

Information: Loaded Icv extension from /home/synopsys/installs/icvalidator/O-
2018.06-SP2-4 (GUI-024)
Information: Visibility is turned ON for cells and cell contents because the
task is set to Block Implementation (GUI-026)
Preparing data for query..................
```

12. Physical Synthesis Report (Each abstraction level)

12.1. Floorplan

```
****************************************
Report     : Virtual Flat Placement
Design     : CORDIC
Version    : O-2018.06-SP4
Date       : Sat Apr  6 16:57:43 2019
****************************************

Total wirelength: 88988.82
Number of 100x100 tracks cell density regions: 36
Number of low (< 10%) cell density regions: 0 (0.000%)
Number of high (> 200%) cell density regions: 0 (0.000%)
Maximum cell density: 63.70% (at 260 100 314 152)
Checking hard macro to hard macro overlaps...
Number of hard macro to hard macro overlaps: 0
Checking hard macro to std cell overlaps...
Number of hard macro to std cell overlaps: 0
Checking plan group to plan group overlaps...
Number of plan group to plan group overlaps: 0
Number of TL cells overlapping PG: 0
Number of cells violating core area: 0
Total number of cells violating plan group or core area: 0
Transferring Data to Milkyway ...
*** global placement done.
Begin Overlap Removal...
Reference Point: Lower Left-hand corner of Core Base Array
[begin initializing data for legality checker]

Initializing Data Structure ...
INFO: legalizer_via_spacing_check_mode 0
  Reading technology information ...
    Technology table contains 4 routable metal layers
    This is considered as a 4-metal-layer design
    Reading library information from DB ...
  Reading misc information ...
    array <unit> has 0 vertical and 66 horizontal rows
  Checking information read in ...
    design style = Horizontal masters, Horizontal rows

  Preprocessing design ...
    splitting rows by natural obstacles ...
... design style 0
```

```
... number of base array 1 0
INFO:... use original rows...
[end initializing data for legality checker]
Information: Running legalization in Fast-Mode! (DPI-029)

****************************************
  Report : Chip Summary
  Design : CORDIC
  Version: O-2018.06-SP4
  Date   : Sat Apr  6 16:57:43 2019
****************************************
Std cell utilization: 60.96%  (26916/(44154-0))
(Non-fixed + Fixed)
Std cell utilization: 60.96%  (26916/(44154-0))
(Non-fixed only)
Chip area:            44154    sites, bbox (100.00 100.00 474.64 469.60) um
Std cell area:        26916    sites, (non-fixed:26916  fixed:0)
                      1815     cells, (non-fixed:1815   fixed:0)
Macro cell area:      0        sites
                      0        cells
Placement blockages:  0        sites, (excluding fixed std cells)
                      0        sites, (include fixed std cells & chimney
area)
                      0        sites, (complete p/g net blockages)
Routing blockages:    0        sites, (partial p/g net blockages)
                      0        sites, (routing blockages and signal pre-
route)
Lib cell count:       20
Avg. std cell width:  4.68 um
Site array:           unit     (width: 0.56 um, height: 5.60 um, rows: 66)
Physical DB scale:    1000 db_unit = 1 um

****************************************
  Report : Legalize Displacement
  Design : CORDIC
  Version: O-2018.06-SP4
  Date   : Sat Apr  6 16:57:43 2019
****************************************

avg cell displacement:    1.799 um ( 0.32 row height)
max cell displacement:    5.587 um ( 1.00 row height)
std deviation:            1.027 um ( 0.18 row height)
```

```
number of cell moved:      1815 cells (out of 1815 cells)

Total 0 cells has large displacement (e.g. > 16.800 um or 3 row height)

Information: Fast-Mode Legalization Done! (DPI-030)
Completed Overlap Removal.
Information: connected 1815 power ports and 1815 ground ports
Geometry mapping begins.
Removing all the files with the prefix CORDIC in the directory ./pna_output
Parasitics Operating Condition is max
Using [2 x 2] Fat Wire Table for M1
Using [2 x 2] Fat Wire Table for M2
Using [2 x 2] Fat Wire Table for M3
Using [2 x 2] Fat Wire Table for TOP_M

TLU+ File =
/home/synopsys/pdk/scl_pdk/design_kit/icc_tech/tluplus/RCE_TS18SL_SCL_STAR_R
CXT_4M1L_TYP.tlup
TLU+ File =

--------- Sanity Check on TLUPlus Files -------------
1. Checking the conducting layer names in ITF and mapping file ...
[ Passed! ]
2. Checking the via layer names in ITF and mapping file ...
[ Passed! ]
3. Checking the consistency of Min Width and Min Spacing between MW-tech and
ITF ...
[ Passed! ]
----------------- Check Ends ------------------
TLU+ based extraction:
Resistance based on max model.
Using operating temperature of  25.00 degree Celsius.
Getting the info of via resistance from TLU+ model
lower mask id 1, upper mask id 2, via layer 41, resistivity 6.000000
lower mask id 2, upper mask id 3, via layer 43, resistivity 6.000000
lower mask id 3, upper mask id 4, via layer 49, resistivity 2.500000
Ignoring all CONN views
Warning: No power/ground pads are specified and no virtual pads are defined.
(PNA-138)
Number of pad instances: 0
Error: All the P/G pads do not have power ports, or all the power ports are
not connected to power or ground net logically. (PNA-006)
```

```
Creating PNS Replay file ./pna_output/pns_replay.tcl
Power network synthesis failed.
Error: No synthesized power network. (PNA-067)
Using [2 x 2] Fat Wire Table for M1
Using [2 x 2] Fat Wire Table for M2
Using [2 x 2] Fat Wire Table for M3
Using [2 x 2] Fat Wire Table for TOP_M
Prerouting standard cells horizontally:
 [Prerouter] CPU = 00:00:00, Elapsed = 00:00:00
        Peak Memory =      460M Data =        0M
Geometry mapping begins.
Removing all the files with the prefix CORDIC in the directory ./pna_output
Parasitics Operating Condition is max
Using [2 x 2] Fat Wire Table for M1
Using [2 x 2] Fat Wire Table for M2
Using [2 x 2] Fat Wire Table for M3
Using [2 x 2] Fat Wire Table for TOP_M
TLU+ based extraction:
Resistance based on max model.
Using operating temperature of  25.00 degree Celsius.
Getting the info of via resistance from TLU+ model
lower mask id 1, upper mask id 2, via layer 41, resistivity 6.000000
lower mask id 2, upper mask id 3, via layer 43, resistivity 6.000000
lower mask id 3, upper mask id 4, via layer 49, resistivity 2.500000
Warning: No power/ground pads are specified and no virtual pads are defined.
(PNA-138)
Number of pad instances: 0
Error: All the P/G pads do not have power ports, or all the power ports are
not connected to power or ground net logically. (PNA-006)
PNA failed.
Warning: No scan chain found. (VFP-425)
CPU time for freeing timing design =    0:00:00
Elapsed time for freeing timing design =    0:00:00
num_cpus = 1
flip_chip = 0
*** Performing global placement...
Transferring Data From Milkyway...
Number of plan group pins = 0
Auto detecting hierarchy nodes for grouping ...
Warning: No hierarchy information in design. Hierarchy gravity turned off.
(VFP-415)
  0 blocks freed
```

```
  0 bytes freed
Placement Effort Level: Low
Placement Design Stats
Num std     cells  = 1815 (fixed = 0)
Num macros  cells  = 0 (fixed = 0)
Num IOs     cells  = 0
Num bump    cells  = 0
Num LS/ISO  cells  = 0
Num no type cells  = 0
Num other   cells  = 0
Num cells with no net connections = 0
Num non-zero wt nets = 2361
Num     zero wt nets = 0
A net with highest fanout (26) is n163
grouping macros ...
0 macro arrays generated automatically.
0 array cells created
No large HMs were processed
coarse place 50% done.
coarse place 75% done.
coarse place 100% done.
******************************************
Report     : Virtual Flat Placement
Design     : CORDIC
Version    : O-2018.06-SP4
Date       : Sat Apr  6 16:57:44 2019
******************************************

Total wirelength: 87827.43
Number of 100x100 tracks cell density regions: 36
Number of low (< 10%) cell density regions: 0 (0.000%)
Number of high (> 200%) cell density regions: 0 (0.000%)
Maximum cell density: 63.46% (at 314 205 367 258)
Checking hard macro to hard macro overlaps...
Number of hard macro to hard macro overlaps: 0
Checking hard macro to std cell overlaps...
Number of hard macro to std cell overlaps: 0
Checking plan group to plan group overlaps...
Number of plan group to plan group overlaps: 0
Number of TL cells overlapping PG: 0
Number of cells violating core area: 0
Total number of cells violating plan group or core area: 0
```

```
Transferring Data to Milkyway ...
*** global placement done.
Begin Overlap Removal...
Reference Point: Lower Left-hand corner of Core Base Array
[begin initializing data for legality checker]

Initializing Data Structure ...
INFO: legalizer_via_spacing_check_mode 0
  Reading technology information ...
    Technology table contains 4 routable metal layers
    This is considered as a 4-metal-layer design
    Reading library information from DB ...
  Reading misc information ...
    array <unit> has 0 vertical and 66 horizontal rows
  Checking information read in ...
    design style = Horizontal masters, Horizontal rows

  Preprocessing design ...
    splitting rows by natural obstacles ...
... design style 0
... number of base array 1 0
INFO:... use original rows...
[end initializing data for legality checker]
Information: Running legalization in Fast-Mode! (DPI-029)

****************************************
  Report : Chip Summary
  Design : CORDIC
  Version: O-2018.06-SP4
  Date   : Sat Apr  6 16:57:44 2019
****************************************
Std cell utilization: 60.96%  (26916/(44154-0))
(Non-fixed + Fixed)
Std cell utilization: 60.96%  (26916/(44154-0))
(Non-fixed only)
Chip area:            44154    sites, bbox (100.00 100.00 474.64 469.60) um
Std cell area:        26916    sites, (non-fixed:26916  fixed:0)
                      1815     cells, (non-fixed:1815   fixed:0)
Macro cell area:      0        sites
                      0        cells
Placement blockages:  0        sites, (excluding fixed std cells)
```

```
                      0        sites, (include fixed std cells & chimney
area)
                      0        sites, (complete p/g net blockages)
Routing blockages:    0        sites, (partial p/g net blockages)
                      0        sites, (routing blockages and signal pre-
route)
Lib cell count:       20
Avg. std cell width:  4.68 um
Site array:           unit     (width: 0.56 um, height: 5.60 um, rows: 66)
Physical DB scale:    1000 db_unit = 1 um

****************************************
  Report : Legalize Displacement
  Design : CORDIC
  Version: O-2018.06-SP4
  Date   : Sat Apr  6 16:57:44 2019
****************************************

avg cell displacement:    1.647 um ( 0.29 row height)
max cell displacement:    5.713 um ( 1.02 row height)
std deviation:            0.920 um ( 0.16 row height)
number of cell moved:      1815 cells (out of 1815 cells)

Total 0 cells has large displacement (e.g. > 16.800 um or 3 row height)

Information: Fast-Mode Legalization Done! (DPI-030)
Completed Overlap Removal.
Information: linking reference library :
/home/synopsys/pdk/scl_pdk/stdlib//fs120/mw/fs120_scl. (PSYN-878)
Information: Loading local_link_library attribute {tsl18fs120_scl_ss.db}.
(MWDC-290)

  Linking design 'CORDIC'
  Using the following designs and libraries:
  --------------------------------------------------------------------------
  CORDIC                      CORDIC.CEL
  tsl18fs120_scl_ss (library)
/home/synopsys/pdk/scl_pdk/stdlib/fs120/liberty/lib_flow_ss/tsl18fs120_scl_s
s.db

Warning: Timer is in zero interconnect delay mode. (TIM-177)
Information: Updating graph... (UID-83)
```

```
Warning: Timer is in zero interconnect delay mode. (TIM-177)
Information: Updating design information... (UID-85)
************************************************
Report : check_physical_design
Stage  : pre_place_opt
Design : CORDIC
Version: O-2018.06-SP4
Date   : Sat Apr  6 16:57:47 2019
************************************************
Total messages: 0 errors, 32 warnings

-----------------------------------------------
Other Warning Summary for check_physical_design
-----------------------------------------------

  ------------------------------------------------------------------------------
-
  ID            Occurrences     Title
  ------------------------------------------------------------------------------
-
  PSYN-261      1               Capacitance of layer %s varies more than the
sp...
  PSYN-266      2               Missing %s nets in the floorplan.
  PSYN-1042     29              Port '%s' cannot inherit its location,
because ...
  ------------------------------------------------------------------------------
-
dump check_physical_design result to file
./cpd_pre_place_opt_2019Apr06165746_4059/index.html
Output DEF file
Information: Writing ROWS statement (DDEFW-014)
Information: Completed ROWS statement  (DDEFW-016)
Information: Writing TRACKS statement (DDEFW-014)
Information: Completed TRACKS statement  (DDEFW-016)
Information: Writing GCELLGRID statement (DDEFW-014)
Information: Completed GCELLGRID statement  (DDEFW-016)
Information: Writing COMPONENTS section (DDEFW-014)
Information: Completed COMPONENTS 1000/1815 (DDEFW-015)
Information: Completed COMPONENTS section  (DDEFW-016)
Information: Writing PINS section (DDEFW-014)
Information: Completed PINS section  (DDEFW-016)
Information: Writing SPECIALNETS section (DDEFW-014)
```

```
Information: Completed SPECIALNETS section  (DDEFW-016)
Information: Writing NETS section (DDEFW-014)
Information: Completed NETS 1000/2391 (DDEFW-015)
Information: Completed NETS 2000/2391 (DDEFW-015)
Information: Completed NETS section  (DDEFW-016)
DEF output completed
floorplan done!!!!!
icc_shell> source ./placement_icc.tcl
```

12.2. Placement

```
****************************************
  Report : Chip Summary
  Design : CORDIC
  Version: O-2018.06-SP4
  Date   : Sat Apr  6 16:59:32 2019
****************************************
Std cell utilization: 61.46%  (27139/(44154-0))
(Non-fixed + Fixed)
Std cell utilization: 61.46%  (27139/(44154-0))
(Non-fixed only)
Chip area:            44154    sites, bbox (100.00 100.00 474.64 469.60) um
Std cell area:        27139    sites, (non-fixed:27139  fixed:0)
                      1843     cells, (non-fixed:1843   fixed:0)
Macro cell area:      0        sites
                      0        cells
Placement blockages:  0        sites, (excluding fixed std cells)
                      0        sites, (include fixed std cells & chimney
area)
                      0        sites, (complete p/g net blockages)
Routing blockages:    0        sites, (partial p/g net blockages)
                      0        sites, (routing blockages and signal pre-
route)
Lib cell count:       26
Avg. std cell width:  4.59 um
Site array:           unit     (width: 0.56 um, height: 5.60 um, rows: 66)
Physical DB scale:    1000 db_unit = 1 um

****************************************
  Report : Legalize Displacement
  Design : CORDIC
  Version: O-2018.06-SP4
  Date   : Sat Apr  6 16:59:32 2019
****************************************
```

```
avg cell displacement:    1.631 um ( 0.29 row height)
max cell displacement:    5.365 um ( 0.96 row height)
std deviation:            0.895 um ( 0.16 row height)
number of cell moved:      1843 cells (out of 1843 cells)

Total 0 cells has large displacement (e.g. > 16.800 um or 3 row height)


Information: Analyzing channel congestion ...
Information: Channel congestion analysis found no blockages




  Design  WNS: 0.00  TNS: 0.00  Number of Violating Paths: 0

  Nets with DRC Violations: 0
  Total moveable cell area: 85107.9
  Total fixed cell area: 0.0
  Total physical cell area: 85107.9
  Core area: (100000 100000 474640 469600)


  No hold constraints


  Timing and DRC Optimization (Stage 1)
  -------------------------------------



  Beginning Timing Optimizations
  ------------------------------

                                  TOTAL
   ELAPSED            WORST NEG   SETUP    DESIGN
     TIME      AREA      SLACK     COST    RULE COST         ENDPOINT
  --------- --------- --------- --------- --------- -------------------------
-
    0:00:07   85104.0      0.00       0.0       0.0
```

```
    0:00:07   85104.0      0.00       0.0       0.0
    0:00:07   85104.0      0.00       0.0       0.0
    0:00:07   85104.0      0.00       0.0       0.0
    0:00:07   85104.0      0.00       0.0       0.0
    0:00:07   85104.0      0.00       0.0       0.0
    0:00:07   85104.0      0.00       0.0       0.0
Warning: Warning: Target library does not have any constant lib_cells so
tool cannot replace virtual constants.  (OPT-223)
Warning: Warning: Target library does not have any constant lib_cells so
tool cannot replace virtual constants.  (OPT-223)


Note: Symbol # after min delay cost means estimated hold TNS across all
active scenarios


  Optimization Complete
  ---------------------

  Placement Optimization (Stage 1)
  --------------------------------

[begin initializing data for legality checker]

Initializing Data Structure ...
INFO: legalizer_via_spacing_check_mode 0
  Reading technology information ...
    Technology table contains 4 routable metal layers
    This is considered as a 4-metal-layer design
    Reading library information from DB ...
  Reading misc information ...
    array <unit> has 0 vertical and 66 horizontal rows
  Checking information read in ...
    design style = Horizontal masters, Horizontal rows

  Preprocessing design ...
    splitting rows by natural obstacles ...
... design style 0
... number of base array 1 0
INFO:... use original rows...
[end initializing data for legality checker]
```

```
****************************************
  Report : Chip Summary
  Design : CORDIC
  Version: O-2018.06-SP4
  Date   : Sat Apr  6 16:59:33 2019
****************************************
Std cell utilization: 61.46%  (27139/(44154-0))
(Non-fixed + Fixed)
Std cell utilization: 61.46%  (27139/(44154-0))
(Non-fixed only)
Chip area:            44154    sites, bbox (100.00 100.00 474.64 469.60) um
Std cell area:        27139    sites, (non-fixed:27139  fixed:0)
                      1843     cells, (non-fixed:1843   fixed:0)
Macro cell area:      0        sites
                      0        cells
Placement blockages:  0        sites, (excluding fixed std cells)
                      0        sites, (include fixed std cells & chimney
area)
                      0        sites, (complete p/g net blockages)
Routing blockages:    0        sites, (partial p/g net blockages)
                      0        sites, (routing blockages and signal pre-
route)
Lib cell count:       26
Avg. std cell width:  4.59 um
Site array:           unit     (width: 0.56 um, height: 5.60 um, rows: 66)
Physical DB scale:    1000 db_unit = 1 um


****************************************
  Report : pnet options
  Design : CORDIC
  Version: O-2018.06-SP4
  Date   : Sat Apr  6 16:59:33 2019
****************************************


--------------------------------------------------------------------
Layer      Blockage   Min_width   Min_height   Via_additive     Density
--------------------------------------------------------------------
M1         none          ---         ---       via additive      ---
M2         none          ---         ---       via additive      ---
M3         none          ---         ---       via additive      ---
```

```
TOP_M      none          ---         ---       via additive      ---

****************************************
  Report : Legalize Displacement
  Design : CORDIC
  Version: O-2018.06-SP4
  Date   : Sat Apr  6 16:59:33 2019
****************************************

No cell displacement.


  Placement Optimization Complete
  -------------------------------


  Design  WNS: 0.00  TNS: 0.00  Number of Violating Paths: 0

  Nets with DRC Violations: 0
  Total moveable cell area: 85107.9
  Total fixed cell area: 0.0
  Total physical cell area: 85107.9
  Core area: (100000 100000 474640 469600)


  No hold constraints


  Timing and DRC Optimization (Stage 2)
  -------------------------------------



  Beginning Timing Optimizations
  ------------------------------

                                   TOTAL
   ELAPSED            WORST NEG   SETUP    DESIGN
     TIME      AREA      SLACK     COST    RULE COST         ENDPOINT
  --------- --------- --------- --------- --------- -------------------------
-
    0:00:07   85104.0      0.00       0.0       0.0
```

```
    0:00:07   85104.0      0.00       0.0       0.0
    0:00:07   85104.0      0.00       0.0       0.0
    0:00:07   85104.0      0.00       0.0       0.0
    0:00:07   85104.0      0.00       0.0       0.0
    0:00:07   85104.0      0.00       0.0       0.0
    0:00:07   85104.0      0.00       0.0       0.0
Warning: Warning: Target library does not have any constant lib_cells so
tool cannot replace virtual constants.  (OPT-223)
Warning: Warning: Target library does not have any constant lib_cells so
tool cannot replace virtual constants.  (OPT-223)


Note: Symbol # after min delay cost means estimated hold TNS across all
active scenarios


  Optimization Complete
  ---------------------

  Placement Optimization (Stage 2)
  --------------------------------

[begin initializing data for legality checker]

Initializing Data Structure ...
INFO: legalizer_via_spacing_check_mode 0
  Reading technology information ...
    Technology table contains 4 routable metal layers
    This is considered as a 4-metal-layer design
    Reading library information from DB ...
  Reading misc information ...
    array <unit> has 0 vertical and 66 horizontal rows
  Checking information read in ...
    design style = Horizontal masters, Horizontal rows

  Preprocessing design ...
    splitting rows by natural obstacles ...
... design style 0
... number of base array 1 0
INFO:... use original rows...
[end initializing data for legality checker]
```

```
****************************************
  Report : Chip Summary
  Design : CORDIC
  Version: O-2018.06-SP4
  Date   : Sat Apr  6 16:59:33 2019
****************************************
Std cell utilization: 61.46%  (27139/(44154-0))
(Non-fixed + Fixed)
Std cell utilization: 61.46%  (27139/(44154-0))
(Non-fixed only)
Chip area:            44154    sites, bbox (100.00 100.00 474.64 469.60) um
Std cell area:        27139    sites, (non-fixed:27139  fixed:0)
                      1843     cells, (non-fixed:1843   fixed:0)
Macro cell area:      0        sites
                      0        cells
Placement blockages:  0        sites, (excluding fixed std cells)
                      0        sites, (include fixed std cells & chimney
area)
                      0        sites, (complete p/g net blockages)
Routing blockages:    0        sites, (partial p/g net blockages)
                      0        sites, (routing blockages and signal pre-
route)
Lib cell count:       26
Avg. std cell width:  4.59 um
Site array:           unit     (width: 0.56 um, height: 5.60 um, rows: 66)
Physical DB scale:    1000 db_unit = 1 um


****************************************
  Report : pnet options
  Design : CORDIC
  Version: O-2018.06-SP4
  Date   : Sat Apr  6 16:59:33 2019
****************************************


--------------------------------------------------------------------
Layer      Blockage   Min_width   Min_height   Via_additive     Density
--------------------------------------------------------------------
M1         none          ---         ---       via additive      ---
M2         none          ---         ---       via additive      ---
M3         none          ---         ---       via additive      ---
```

```
TOP_M      none          ---         ---       via additive      ---

****************************************
  Report : Legalize Displacement
  Design : CORDIC
  Version: O-2018.06-SP4
  Date   : Sat Apr  6 16:59:33 2019
****************************************

No cell displacement.


  Placement Optimization Complete
  -------------------------------


  Design  WNS: 0.00  TNS: 0.00  Number of Violating Paths: 0

  Nets with DRC Violations: 0
  Total moveable cell area: 85107.9
  Total fixed cell area: 0.0
  Total physical cell area: 85107.9
  Core area: (100000 100000 474640 469600)


  No hold constraints

[begin initializing data for legality checker]

Initializing Data Structure ...
INFO: legalizer_via_spacing_check_mode 0
  Reading technology information ...
    Technology table contains 4 routable metal layers
    This is considered as a 4-metal-layer design
    Reading library information from DB ...
  Reading misc information ...
    array <unit> has 0 vertical and 66 horizontal rows
  Checking information read in ...
    design style = Horizontal masters, Horizontal rows

  Preprocessing design ...
    splitting rows by natural obstacles ...
```

```
... design style 0
... number of base array 1 0
INFO:... use original rows...
[end initializing data for legality checker]
Warning: Die area is not integer multiples of min site height (5600),
object's width and height(574640,569600). (PSYN-523)
Warning: Die area is not integer multiples of min site width (560), object's
width and height(574640,569600). (PSYN-523)

****************************************************
Check_legality: Report for Fixed Placement Cells
Information: Use the -verbose option to get details about the legality
violations. (PSYN-054)
****************************************************
(fixed placement) Cells Not on Row            : 0
(fixed placement) Cell Overlaps               : 0
(fixed placement) Cells overlapping blockages : 0
(fixed placement) Orientation Violations      : 0
(fixed placement) Site Violations             : 0
(fixed placement) Power Strap Violations      : 0
****************************************************

****************************************************
Check_legality: Report for Non-fixed Placement Cells
Information: Use the -verbose option to get details about the legality
violations. (PSYN-054)
****************************************************
Number of Cells Not on Row            : 0
Number of Cell Overlaps               : 0
Number of Cells overlapping blockages : 0
Number of Orientation Violations      : 0
Number of Site Violations             : 0
Number of Power Strap Violations      : 0
****************************************
Information: Updating database...
Information: Disabling timing checks inside check_ilm
Information: Disabling timing checks inside check_block_abstraction
checking tluplus...
checking physical objects...
checking database...
Information: Disabling check_timing in check_physical_design
checking HFN/ideal/dont_touch nets...
```

```
Information: Disabling timing checks inside check_block_abstraction
Information: Enabling timing checks inside check_block_abstraction
checking placement constraints...
checking for unconnected tie pins...
checking for too many Restricted cells...
checking clock trees...
checking clock routing rules...
Number of Undocumented Errors: 0
************************************************
Report : check_physical_design
Stage  : pre_clock_opt
Design : CORDIC
Version: O-2018.06-SP4
Date   : Sat Apr  6 16:59:34 2019
************************************************
Total messages: 0 errors, 2 warnings

----------------------------------------
Warning Summary for check_physical_design
----------------------------------------

  ------------------------------------------------------------------------
-
  ID            Occurrences     Title
  ------------------------------------------------------------------------
-
  PSYN-523      2               Geometries are not integer multiple of width
or...
  ------------------------------------------------------------------------
-
dump check_physical_design result to file
./cpd_pre_clock_opt_2019Apr06165934_4059/index.html
Output DEF file
Information: Writing ROWS statement (DDEFW-014)
Information: Completed ROWS statement  (DDEFW-016)
Information: Writing TRACKS statement (DDEFW-014)
Information: Completed TRACKS statement  (DDEFW-016)
Information: Writing GCELLGRID statement (DDEFW-014)
Information: Completed GCELLGRID statement  (DDEFW-016)
Information: Writing COMPONENTS section (DDEFW-014)
Information: Completed COMPONENTS 1000/1843 (DDEFW-015)
Information: Completed COMPONENTS section  (DDEFW-016)
```

```
Information: Writing PINS section (DDEFW-014)
Information: Completed PINS section  (DDEFW-016)
Information: Writing SPECIALNETS section (DDEFW-014)
Information: Completed SPECIALNETS section  (DDEFW-016)
Information: Writing NETS section (DDEFW-014)
Information: Completed NETS 1000/2419 (DDEFW-015)
Information: Completed NETS 2000/2419 (DDEFW-015)
Information: Completed NETS section  (DDEFW-016)
DEF output completed
```

12.3. CTS:

```
****************************************
  Report : Chip Summary
  Design : CORDIC
  Version: O-2018.06-SP4
  Date   : Sat Apr  6 16:59:49 2019
****************************************
Std cell utilization: 61.89%  (27326/(44154-0))
(Non-fixed + Fixed)
Std cell utilization: 61.73%  (27139/(44154-187))
(Non-fixed only)
Chip area:            44154    sites, bbox (100.00 100.00 474.64 469.60) um
Std cell area:        27326    sites, (non-fixed:27139  fixed:187)
                      1858     cells, (non-fixed:1843   fixed:15)
Macro cell area:      0        sites
                      0        cells
Placement blockages:  0        sites, (excluding fixed std cells)
                      187      sites, (include fixed std cells & chimney
area)
                      0        sites, (complete p/g net blockages)
Routing blockages:    0        sites, (partial p/g net blockages)
                      0        sites, (routing blockages and signal pre-
route)
Lib cell count:       26
Avg. std cell width:  4.59 um
Site array:           unit     (width: 0.56 um, height: 5.60 um, rows: 66)
Physical DB scale:    1000 db_unit = 1 um
****************************************
  Report : Legalize Displacement
  Design : CORDIC
  Version: O-2018.06-SP4
  Date   : Sat Apr  6 16:59:49 2019
****************************************
```

```
avg cell displacement:    2.753 um ( 0.49 row height)
max cell displacement:    6.031 um ( 1.08 row height)
std deviation:            1.698 um ( 0.30 row height)
number of cell moved:        34 cells (out of 1843 cells)

Total 0 cells has large displacement (e.g. > 16.800 um or 3 row height)


  Placement Legalization Complete
  -------------------------------

Information: Updating database...
Unsetting the GR Options
LR: 3 out of 16 clock nets rerouted
LR: Clock routing service terminated
Invalidate design extracted status
Optimize clock tree Successful...
Routing clock nets...
Turn off antenna since no rule is specified
Cell Min-Routing-Layer = M1
Cell Max-Routing-Layer = TOP_M
Start Global Route ...
[Init] Elapsed real time: 0:00:00
[Init] Elapsed cpu  time: sys=0:00:00 usr=0:00:00 total=0:00:00
[Init] Stage (MB): Used    0  Alloctr    0  Proc    0
[Init] Total (MB): Used   18  Alloctr   19  Proc 2170
Printing options for 'set_route_zrt_common_options'

Printing options for 'set_route_zrt_global_options'

Begin global routing.
Constructing data structure ...
Design statistics:
Design Bounding Box (0.00,0.00,574.64,569.60)
Number of routing layers = 4
layer M1, dir Hor, min width = 0.23, min space = 0.23 pitch = 0.56
layer M2, dir Ver, min width = 0.28, min space = 0.28 pitch = 0.56
layer M3, dir Hor, min width = 0.28, min space = 0.28 pitch = 0.66
layer TOP_M, dir Ver, min width = 0.44, min space = 0.46 pitch = 1.12
Current Stage stats:
[End of Build Tech Data] Elapsed real time: 0:00:00
```

```
[End of Build Tech Data] Elapsed cpu  time: sys=0:00:00 usr=0:00:00
total=0:00:00
[End of Build Tech Data] Stage (MB): Used    0  Alloctr    0  Proc    0
[End of Build Tech Data] Total (MB): Used   19  Alloctr   20  Proc 2170
Net statistics:
Total number of nets     = 2436
Number of nets to route  = 16
Number of single or zero port nets = 29
Number of nets with min-layer-mode soft = 16
Number of nets with min-layer-mode soft-cost-medium = 16
18 nets are fully connected,
 of which 2 are detail routed and 16 are global routed.
Current Stage stats:
[End of Build All Nets] Elapsed real time: 0:00:00
[End of Build All Nets] Elapsed cpu  time: sys=0:00:00 usr=0:00:00
total=0:00:00
[End of Build All Nets] Stage (MB): Used    0  Alloctr    0  Proc    0
[End of Build All Nets] Total (MB): Used   20  Alloctr   21  Proc 2170
Average gCell capacity  6.48     on layer (1)    M1
Average gCell capacity  10.03    on layer (2)    M2
Average gCell capacity  8.45     on layer (3)    M3
Average gCell capacity  5.02     on layer (4)    TOP_M
Average number of tracks per gCell 9.98  on layer (1)    M1
Average number of tracks per gCell 10.06         on layer (2)    M2
Average number of tracks per gCell 8.47  on layer (3)    M3
Average number of tracks per gCell 5.04  on layer (4)    TOP_M
Number of gCells = 41616
Current Stage stats:
[End of Build Congestion map] Elapsed real time: 0:00:00
[End of Build Congestion map] Elapsed cpu  time: sys=0:00:00 usr=0:00:00
total=0:00:00
[End of Build Congestion map] Stage (MB): Used    0  Alloctr    0  Proc    0
[End of Build Congestion map] Total (MB): Used   20  Alloctr   21  Proc 2170
Total stats:
[End of Build Data] Elapsed real time: 0:00:00
[End of Build Data] Elapsed cpu  time: sys=0:00:00 usr=0:00:00 total=0:00:00
[End of Build Data] Stage (MB): Used    1  Alloctr    1  Proc    0
[End of Build Data] Total (MB): Used   20  Alloctr   21  Proc 2170
Current Stage stats:
[End of Blocked Pin Detection] Elapsed real time: 0:00:00
[End of Blocked Pin Detection] Elapsed cpu  time: sys=0:00:00 usr=0:00:00
total=0:00:00
```

```
[End of Blocked Pin Detection] Stage (MB): Used    0  Alloctr    0  Proc
0
[End of Blocked Pin Detection] Total (MB): Used   20  Alloctr   21  Proc
2170
Information: Using 1 threads for routing. (ZRT-444)
multi gcell levels ON

Start GR phase 0
Current Stage stats:
[End of Initial Routing] Elapsed real time: 0:00:00
[End of Initial Routing] Elapsed cpu  time: sys=0:00:00 usr=0:00:00
total=0:00:00
[End of Initial Routing] Stage (MB): Used    0  Alloctr    0  Proc    0
[End of Initial Routing] Total (MB): Used   20  Alloctr   21  Proc 2170
Initial. Routing result:
Initial. Both Dirs: Overflow =     0 Max = 0 GRCs =     0 (0.00%)
Initial. H routing: Overflow =     0 Max = 0 (GRCs =  0) GRCs =     0
(0.00%)
Initial. V routing: Overflow =     0 Max = 0 (GRCs =  0) GRCs =     0
(0.00%)
Initial. M1         Overflow =     0 Max = 0 (GRCs =  0) GRCs =     0
(0.00%)
Initial. M2         Overflow =     0 Max = 0 (GRCs =  0) GRCs =     0
(0.00%)
Initial. M3         Overflow =     0 Max = 0 (GRCs =  0) GRCs =     0
(0.00%)
Initial. TOP_M      Overflow =     0 Max = 0 (GRCs =  0) GRCs =     0
(0.00%)

Initial. Total Wire Length = 8701.77
Initial. Layer M1 wire length = 0.00
Initial. Layer M2 wire length = 0.00
Initial. Layer M3 wire length = 4770.57
Initial. Layer TOP_M wire length = 3931.20
Initial. Total Number of Contacts = 1783
Initial. Via V2_cross count = 588
Initial. Via V3_cross count = 588
Initial. Via VL count = 607
Initial. completed.

Start GR phase 1
Current Stage stats:
```

```
[End of Phase1 Routing] Elapsed real time: 0:00:00
[End of Phase1 Routing] Elapsed cpu  time: sys=0:00:00 usr=0:00:00
total=0:00:00
[End of Phase1 Routing] Stage (MB): Used    0  Alloctr    0  Proc    0
[End of Phase1 Routing] Total (MB): Used   20  Alloctr   21  Proc 2170
phase1. Routing result:
phase1. Both Dirs: Overflow =     0 Max = 0 GRCs =     0 (0.00%)
phase1. H routing: Overflow =     0 Max = 0 (GRCs =  0) GRCs =     0 (0.00%)
phase1. V routing: Overflow =     0 Max = 0 (GRCs =  0) GRCs =     0 (0.00%)
phase1. M1         Overflow =     0 Max = 0 (GRCs =  0) GRCs =     0 (0.00%)
phase1. M2         Overflow =     0 Max = 0 (GRCs =  0) GRCs =     0 (0.00%)
phase1. M3         Overflow =     0 Max = 0 (GRCs =  0) GRCs =     0 (0.00%)
phase1. TOP_M      Overflow =     0 Max = 0 (GRCs =  0) GRCs =     0 (0.00%)

phase1. Total Wire Length = 8701.77
phase1. Layer M1 wire length = 0.00
phase1. Layer M2 wire length = 0.00
phase1. Layer M3 wire length = 4770.57
phase1. Layer TOP_M wire length = 3931.20
phase1. Total Number of Contacts = 1783
phase1. Via V2_cross count = 588
phase1. Via V3_cross count = 588
phase1. Via VL count = 607
phase1. completed.

Start GR phase 2
Current Stage stats:
[End of Phase2 Routing] Elapsed real time: 0:00:00
[End of Phase2 Routing] Elapsed cpu  time: sys=0:00:00 usr=0:00:00
total=0:00:00
[End of Phase2 Routing] Stage (MB): Used    0  Alloctr    0  Proc    0
[End of Phase2 Routing] Total (MB): Used   20  Alloctr   21  Proc 2170
phase2. Routing result:
phase2. Both Dirs: Overflow =     0 Max = 0 GRCs =     0 (0.00%)
phase2. H routing: Overflow =     0 Max = 0 (GRCs =  0) GRCs =     0 (0.00%)
phase2. V routing: Overflow =     0 Max = 0 (GRCs =  0) GRCs =     0 (0.00%)
phase2. M1         Overflow =     0 Max = 0 (GRCs =  0) GRCs =     0 (0.00%)
phase2. M2         Overflow =     0 Max = 0 (GRCs =  0) GRCs =     0 (0.00%)
phase2. M3         Overflow =     0 Max = 0 (GRCs =  0) GRCs =     0 (0.00%)
phase2. TOP_M      Overflow =     0 Max = 0 (GRCs =  0) GRCs =     0 (0.00%)

phase2. Total Wire Length = 8701.77
```

```
phase2. Layer M1 wire length = 0.00
phase2. Layer M2 wire length = 0.00
phase2. Layer M3 wire length = 4770.57
phase2. Layer TOP_M wire length = 3931.20
phase2. Total Number of Contacts = 1783
phase2. Via V2_cross count = 588
phase2. Via V3_cross count = 588
phase2. Via VL count = 607
phase2. completed.
[End of Whole Chip Routing] Elapsed real time: 0:00:00
[End of Whole Chip Routing] Elapsed cpu  time: sys=0:00:00 usr=0:00:00
total=0:00:00
[End of Whole Chip Routing] Stage (MB): Used    1  Alloctr    1  Proc    0
[End of Whole Chip Routing] Total (MB): Used   20  Alloctr   21  Proc 2170

Congestion utilization per direction:
Average vertical track utilization   =  0.60 %
Peak    vertical track utilization   = 20.00 %
Average horizontal track utilization =  0.81 %
Peak    horizontal track utilization = 33.33 %

Current Stage stats:
[GR: Done] Elapsed real time: 0:00:00
[GR: Done] Elapsed cpu  time: sys=0:00:00 usr=0:00:00 total=0:00:00
[GR: Done] Stage (MB): Used    0  Alloctr    0  Proc    0
[GR: Done] Total (MB): Used   20  Alloctr   21  Proc 2170
GR Total stats:
[GR: Done] Elapsed real time: 0:00:00
[GR: Done] Elapsed cpu  time: sys=0:00:00 usr=0:00:00 total=0:00:00
[GR: Done] Stage (MB): Used    1  Alloctr    1  Proc    0
[GR: Done] Total (MB): Used   20  Alloctr   21  Proc 2170
Updating congestion ...
Final total stats:
[End of Global Routing] Elapsed real time: 0:00:00
[End of Global Routing] Elapsed cpu  time: sys=0:00:00 usr=0:00:00
total=0:00:00
[End of Global Routing] Stage (MB): Used    0  Alloctr    0  Proc    0
[End of Global Routing] Total (MB): Used   18  Alloctr   19  Proc 2170

Start track assignment

Printing options for 'set_route_zrt_common_options'
```

```
Printing options for 'set_route_zrt_track_options'

Information: Using 1 threads for routing. (ZRT-444)

[Track Assign: Read routes] Elapsed real time: 0:00:00
[Track Assign: Read routes] Elapsed cpu  time: sys=0:00:00 usr=0:00:00
total=0:00:00
[Track Assign: Read routes] Stage (MB): Used    0  Alloctr    0  Proc    0
[Track Assign: Read routes] Total (MB): Used   15  Alloctr   15  Proc 2170

Start initial assignment

Assign Horizontal partitions, iteration 0
Routed partition 1/11
Routed partition 2/11
Routed partition 3/11
Routed partition 4/11
Routed partition 5/11
Routed partition 6/11
Routed partition 7/11
Routed partition 8/11
Routed partition 9/11
Routed partition 10/11
Routed partition 11/11

Assign Vertical partitions, iteration 0
Routed partition 1/11
Routed partition 2/11
Routed partition 3/11
Routed partition 4/11
Routed partition 5/11
Routed partition 6/11
Routed partition 7/11
Routed partition 8/11
Routed partition 9/11
Routed partition 10/11
Routed partition 11/11

Number of wires with overlap after iteration 0 = 361 of 2018
```

```
[Track Assign: Iteration 0] Elapsed real time: 0:00:00
[Track Assign: Iteration 0] Elapsed cpu  time: sys=0:00:00 usr=0:00:00
total=0:00:00
[Track Assign: Iteration 0] Stage (MB): Used    0  Alloctr    0  Proc    0
[Track Assign: Iteration 0] Total (MB): Used   15  Alloctr   16  Proc 2170

Reroute to fix overlaps

Assign Horizontal partitions, iteration 1
Routed partition 1/11
Routed partition 2/11
Routed partition 3/11
Routed partition 4/11
Routed partition 5/11
Routed partition 6/11
Routed partition 7/11
Routed partition 8/11
Routed partition 9/11
Routed partition 10/11
Routed partition 11/11

Assign Vertical partitions, iteration 1
Routed partition 1/11
Routed partition 2/11
Routed partition 3/11
Routed partition 4/11
Routed partition 5/11
Routed partition 6/11
Routed partition 7/11
Routed partition 8/11
Routed partition 9/11
Routed partition 10/11
Routed partition 11/11

[Track Assign: Iteration 1] Elapsed real time: 0:00:00
[Track Assign: Iteration 1] Elapsed cpu  time: sys=0:00:00 usr=0:00:00
total=0:00:00
[Track Assign: Iteration 1] Stage (MB): Used    0  Alloctr    0  Proc    0
[Track Assign: Iteration 1] Total (MB): Used   15  Alloctr   16  Proc 2170

Number of wires with overlap after iteration 1 = 37 of 1804
```

```
Wire length and via report:
---------------------------
Number of M1 wires: 10            : 0
Number of M2 wires: 538                   V2_cross: 609
Number of M3 wires: 807                   V3_cross: 597
Number of TOP_M wires: 449                VL: 623
Total number of wires: 1804               vias: 1829

Total M1 wire length: 21.4
Total M2 wire length: 149.1
Total M3 wire length: 4886.8
Total TOP_M wire length: 3928.5
Total wire length: 8985.8

Longest M1 wire length: 4.4
Longest M2 wire length: 1.7
Longest M3 wire length: 263.2
Longest TOP_M wire length: 207.9


[Track Assign: Done] Elapsed real time: 0:00:00
[Track Assign: Done] Elapsed cpu  time: sys=0:00:00 usr=0:00:00
total=0:00:00
[Track Assign: Done] Stage (MB): Used    0  Alloctr    0  Proc    0
[Track Assign: Done] Total (MB): Used   14  Alloctr   15  Proc 2170
Printing options for 'set_route_zrt_common_options'

Printing options for 'set_route_zrt_detail_options'

[Dr init] Elapsed real time: 0:00:00
[Dr init] Elapsed cpu  time: sys=0:00:00 usr=0:00:00 total=0:00:00
[Dr init] Stage (MB): Used    2  Alloctr    2  Proc    0
[Dr init] Total (MB): Used   17  Alloctr   17  Proc 2170
Total number of nets = 2436, of which 0 are not extracted
Total number of open nets = 2389, of which 0 are frozen
Information: Using 1 threads for routing. (ZRT-444)
Start DR iteration 0: uniform partition
Routed  5/121 Partitions, Violations =  0
Routed  8/121 Partitions, Violations =  0
Routed  9/121 Partitions, Violations =  1
Routed  12/121 Partitions, Violations = 1
```

```
Routed  13/121 Partitions, Violations = 1
Routed  14/121 Partitions, Violations = 1
Routed  17/121 Partitions, Violations = 1
Routed  18/121 Partitions, Violations = 0
Routed  19/121 Partitions, Violations = 0
Routed  20/121 Partitions, Violations = 0
Routed  23/121 Partitions, Violations = 0
Routed  24/121 Partitions, Violations = 0
Routed  25/121 Partitions, Violations = 0
Routed  26/121 Partitions, Violations = 0
Routed  27/121 Partitions, Violations = 0
Routed  28/121 Partitions, Violations = 0
Routed  30/121 Partitions, Violations = 0
Routed  31/121 Partitions, Violations = 0
Routed  32/121 Partitions, Violations = 2
Routed  33/121 Partitions, Violations = 2
Routed  34/121 Partitions, Violations = 2
Routed  35/121 Partitions, Violations = 2
Routed  36/121 Partitions, Violations = 2
Routed  38/121 Partitions, Violations = 2
Routed  39/121 Partitions, Violations = 2
Routed  40/121 Partitions, Violations = 1
Routed  41/121 Partitions, Violations = 1
Routed  42/121 Partitions, Violations = 1
Routed  43/121 Partitions, Violations = 1
Routed  44/121 Partitions, Violations = 1
Routed  45/121 Partitions, Violations = 1
Routed  47/121 Partitions, Violations = 1
Routed  48/121 Partitions, Violations = 1
Routed  49/121 Partitions, Violations = 1
Routed  50/121 Partitions, Violations = 0
Routed  51/121 Partitions, Violations = 0
Routed  52/121 Partitions, Violations = 0
Routed  53/121 Partitions, Violations = 1
Routed  54/121 Partitions, Violations = 1
Routed  55/121 Partitions, Violations = 1
Routed  58/121 Partitions, Violations = 1
Routed  59/121 Partitions, Violations = 1
Routed  60/121 Partitions, Violations = 1
Routed  61/121 Partitions, Violations = 1
Routed  62/121 Partitions, Violations = 1
Routed  63/121 Partitions, Violations = 0
```

```
Routed  64/121 Partitions, Violations = 0
Routed  69/121 Partitions, Violations = 0
Routed  70/121 Partitions, Violations = 0
Routed  71/121 Partitions, Violations = 0
Routed  72/121 Partitions, Violations = 0
Routed  73/121 Partitions, Violations = 0
Routed  74/121 Partitions, Violations = 0
Routed  79/121 Partitions, Violations = 0
Routed  80/121 Partitions, Violations = 0
Routed  81/121 Partitions, Violations = 1
Routed  82/121 Partitions, Violations = 1
Routed  83/121 Partitions, Violations = 1
Routed  88/121 Partitions, Violations = 1
Routed  89/121 Partitions, Violations = 0
Routed  90/121 Partitions, Violations = 0
Routed  91/121 Partitions, Violations = 0
Routed  96/121 Partitions, Violations = 0
Routed  97/121 Partitions, Violations = 0
Routed  98/121 Partitions, Violations = 0
Routed  103/121 Partitions, Violations =        0
Routed  104/121 Partitions, Violations =        0
Routed  109/121 Partitions, Violations =        0

DRC-SUMMARY:
        @@@@@@@ TOTAL VIOLATIONS =      0

[Iter 0] Elapsed real time: 0:00:00
[Iter 0] Elapsed cpu  time: sys=0:00:00 usr=0:00:00 total=0:00:00
[Iter 0] Stage (MB): Used    9  Alloctr    9  Proc    0
[Iter 0] Total (MB): Used   24  Alloctr   25  Proc 2170

End DR iteration 0 with 121 parts

Finish DR since reached 0 DRC

[DR] Elapsed real time: 0:00:00
[DR] Elapsed cpu  time: sys=0:00:00 usr=0:00:00 total=0:00:00
[DR] Stage (MB): Used    0  Alloctr    0  Proc    0
[DR] Total (MB): Used   15  Alloctr   15  Proc 2170
[DR: Done] Elapsed real time: 0:00:00
[DR: Done] Elapsed cpu  time: sys=0:00:00 usr=0:00:00 total=0:00:00
[DR: Done] Stage (MB): Used    0  Alloctr    0  Proc    0
```

```
[DR: Done] Total (MB): Used   15  Alloctr   15  Proc 2170

DR finished with 0 open nets, of which 0 are frozen

DR finished with 0 violations

DRC-SUMMARY:
        @@@@@@@ TOTAL VIOLATIONS =      0



Total Wire Length =                     8964 micron
Total Number of Contacts =              1802
Total Number of Wires =                 1250
Total Number of PtConns =               433
Total Number of Routed Wires =         1250
Total Routed Wire Length =             8850 micron
Total Number of Routed Contacts =        1802
        Layer            M1 :          31 micron
        Layer            M2 :         187 micron
        Layer            M3 :        4821 micron
        Layer         TOP_M :        3926 micron
        Via              VL :         621
        Via        V3_cross :         593
        Via        V2_cross :         576
        Via   V2_cross(rot) :          12


Redundant via conversion report:
--------------------------------

  Total optimized via conversion rate =  0.00% (0 / 1802 vias)

    Layer V2         =  0.00% (0      / 588     vias)
        Un-optimized = 100.00% (588     vias)
    Layer V3         =  0.00% (0      / 593     vias)
        Un-optimized = 100.00% (593     vias)
    Layer TOP_V      =  0.00% (0      / 621     vias)
        Un-optimized = 100.00% (621     vias)

  Total double via conversion rate    =  0.00% (0 / 1802 vias)
```

```
    Layer V2         =  0.00% (0      / 588     vias)
    Layer V3         =  0.00% (0      / 593     vias)
    Layer TOP_V      =  0.00% (0      / 621     vias)

  The optimized via conversion rate based on total routed via count =  0.00%
(0 / 1802 vias)

    Layer V2         =  0.00% (0      / 588     vias)
        Un-optimized = 100.00% (588     vias)
    Layer V3         =  0.00% (0      / 593     vias)
        Un-optimized = 100.00% (593     vias)
    Layer TOP_V      =  0.00% (0      / 621     vias)
        Un-optimized = 100.00% (621     vias)


Total number of nets = 2436
0 open nets, of which 0 are frozen
Total number of excluded ports = 0 ports of 0 unplaced cells connected to 0
nets
                                 0 ports without pins of 0 cells connected
to 0 nets
                                 0 ports of 0 cover cells connected to 0
non-pg nets
Total number of DRCs = 0
Total number of antenna violations = antenna checking not active
Total number of voltage-area violations = no voltage-areas defined
Topology ECO iteration 1 ended with 0 qualifying violations.
Updating the database ...
Information: RC extraction has been freed. (PSYN-503)
Routing of clock nets Successful.
RC Extraction...

  Loading design 'CORDIC'
****************************************
Report : clock tree
Design : CORDIC
Version: O-2018.06-SP4
Date   : Sat Apr  6 16:59:52 2019
****************************************

Information: Float pin scale factor for the 'max' operating condition of
scenario 'default' is set to 1.000 (CTS-375)
```

```
======================= Clock Tree Summary ========================
Clock                Sinks     CTBuffers ClkCells  Skew      LongestPath
TotalDRC   BufferArea
--------------------------------------------------------------------------------
-------------------
clock                580       15        15        0.0189    0.3024      0
586.4320
clock_opt completed Successfully

****************************************
Report : clock tree
Design : CORDIC
Version: O-2018.06-SP4
Date   : Sat Apr  6 16:59:52 2019
****************************************

Information: Float pin scale factor for the 'max' operating condition of
scenario 'default' is set to 1.000 (CTS-375)

============ Global Skew Report ================

Clock Tree Name               : "clock"
Clock Period                  : 10.00000
Clock Tree root pin           : "clock"
Number of Levels              : 3
Number of Sinks               : 580
Number of CT Buffers          : 15
Number of CTS added gates     : 0
Number of Preexisting Gates   : 0
Number of Preexisting Buf/Inv : 0
Total Number of Clock Cells   : 15
Total Area of CT Buffers      : 586.43201
Total Area of CT cells        : 586.43201
Max Global Skew               : 0.01894
Number of MaxTran Violators   : 0
Number of MaxCap Violators    : 0
Number of MaxFanout Violators : 0


Operating Condition              worst
Clock global Skew                0.019
```

```
Longest path delay               0.302
Shortest path delay              0.283

The longest path delay end pin: XYZ[5].c1/temp_x_out_reg[8]/CP
The shortest path delay end pin: temp_yin_reg[8]/CP

The longest Path:
Pin                                        Cap       Fanout    Trans
Incr      Arri
-------------------------------------------------------------------------------
------------------------
clock                                      0.000            1  0.000
0.000     0.000     r
clock                                      0.025            2  0.000
0.000     0.000     r
bufbda_G1B2I1/I                            0.025            1  0.000
0.000     0.000     r
bufbda_G1B2I1/Z                            0.069            6  0.101
0.121     0.121     r
bufbda_G1B1I7/I                            0.069            1  0.101
0.000     0.121     r
bufbda_G1B1I7/Z                            0.167           58  0.176
0.181     0.302     r
XYZ[5].c1/temp_x_out_reg[8]/CP             0.167            0  0.176
0.000     0.302     r
[clock delay]
0.302
-------------------------------------------------------------------------------
------------------------

The Shortest Path:
Pin                                        Cap       Fanout    Trans
Incr      Arri
-------------------------------------------------------------------------------
------------------------
clock                                      0.000            1  0.000
0.000     0.000     r
clock                                      0.025            2  0.000
0.000     0.000     r
bufbda_G1B2I2/I                            0.025            1  0.000
0.000     0.000     r
```

```
bufbda_G1B2I2/Z                              0.077            7  0.109
0.125     0.125     r
bufbd7_G1B1I9/I                              0.077            1  0.109
0.000     0.125     r
bufbd7_G1B1I9/Z                              0.107           37  0.127
0.159     0.283     r
temp_yin_reg[8]/CP                           0.107            0  0.127
0.000     0.283     r
[clock delay]
0.283
-------------------------------------------------------------------------------
------------------------


Cell CORDIC.err existed already. Replace it ...

============================================
==        Check Pin-Spot Min-Grid         ==
============================================


============================================
==         Check Pin out of bound         ==
============================================


No out-of-bound error found

============================================
==             Check Min-Grid             ==
============================================

No min-grid error found

============================================
==        Check for blocked ports         ==
============================================

  Checked        1/3 SBoxes
  Checked        2/3 SBoxes
  Checked        3/3 SBoxes
```

```
No blocked port was detected

[        CHECK DESIGN] CPU = 0:00:00, Elapsed = 0:00:00

[        CHECK DESIGN] Peak Memory =    493M Data =      6M

Update error cell ...
```

12.4. Routing:

```
Turn off antenna since no rule is specified
Cell Min-Routing-Layer = M1
Cell Max-Routing-Layer = TOP_M
Start Global Route ...
[Init] Elapsed real time: 0:00:00
[Init] Elapsed cpu  time: sys=0:00:00 usr=0:00:00 total=0:00:00
[Init] Stage (MB): Used    0  Alloctr    0  Proc    0
[Init] Total (MB): Used   19  Alloctr   19  Proc 2208
Printing options for 'set_route_zrt_common_options'
-concurrent_redundant_via_effort_level                  :        high
-concurrent_redundant_via_mode                          :
insert_at_high_cost
-post_detail_route_redundant_via_insertion              :        high

Printing options for 'set_route_zrt_global_options'

Begin global routing.
Constructing data structure ...
Design statistics:
Design Bounding Box (0.00,0.00,574.64,569.60)
Number of routing layers = 4
layer M1, dir Hor, min width = 0.23, min space = 0.23 pitch = 0.56
layer M2, dir Ver, min width = 0.28, min space = 0.28 pitch = 0.56
layer M3, dir Hor, min width = 0.28, min space = 0.28 pitch = 0.66
layer TOP_M, dir Ver, min width = 0.44, min space = 0.46 pitch = 1.12
Current Stage stats:
[End of Build Tech Data] Elapsed real time: 0:00:00
[End of Build Tech Data] Elapsed cpu  time: sys=0:00:00 usr=0:00:00
total=0:00:00
[End of Build Tech Data] Stage (MB): Used    0  Alloctr    0  Proc    0
[End of Build Tech Data] Total (MB): Used   19  Alloctr   20  Proc 2208
Net statistics:
Total number of nets     = 2436
Number of nets to route  = 16
```

```
Number of single or zero port nets = 29
Number of nets with min-layer-mode soft = 16
Number of nets with min-layer-mode soft-cost-medium = 16
18 nets are fully connected,
 of which 18 are detail routed and 0 are global routed.
Current Stage stats:
[End of Build All Nets] Elapsed real time: 0:00:00
[End of Build All Nets] Elapsed cpu  time: sys=0:00:00 usr=0:00:00
total=0:00:00
[End of Build All Nets] Stage (MB): Used    0  Alloctr    0  Proc    0
[End of Build All Nets] Total (MB): Used   20  Alloctr   21  Proc 2208
Average gCell capacity  6.48     on layer (1)    M1
Average gCell capacity  10.03    on layer (2)    M2
Average gCell capacity  8.45     on layer (3)    M3
Average gCell capacity  5.02     on layer (4)    TOP_M
Average number of tracks per gCell 9.98  on layer (1)    M1
Average number of tracks per gCell 10.06         on layer (2)    M2
Average number of tracks per gCell 8.47  on layer (3)    M3
Average number of tracks per gCell 5.04  on layer (4)    TOP_M
Number of gCells = 41616
Current Stage stats:
[End of Build Congestion map] Elapsed real time: 0:00:00
[End of Build Congestion map] Elapsed cpu  time: sys=0:00:00 usr=0:00:00
total=0:00:00
[End of Build Congestion map] Stage (MB): Used    0  Alloctr    0  Proc    0
[End of Build Congestion map] Total (MB): Used   20  Alloctr   21  Proc 2208
Total stats:
[End of Build Data] Elapsed real time: 0:00:00
[End of Build Data] Elapsed cpu  time: sys=0:00:00 usr=0:00:00 total=0:00:00
[End of Build Data] Stage (MB): Used    1  Alloctr    1  Proc    0
[End of Build Data] Total (MB): Used   20  Alloctr   21  Proc 2208
Current Stage stats:
[End of Blocked Pin Detection] Elapsed real time: 0:00:00
[End of Blocked Pin Detection] Elapsed cpu  time: sys=0:00:00 usr=0:00:00
total=0:00:00
[End of Blocked Pin Detection] Stage (MB): Used    0  Alloctr    0  Proc
0
[End of Blocked Pin Detection] Total (MB): Used   20  Alloctr   21  Proc
2208
Information: Using 1 threads for routing. (ZRT-444)
multi gcell levels ON
```

```
Start GR phase 0
Current Stage stats:
[End of Initial Routing] Elapsed real time: 0:00:00
[End of Initial Routing] Elapsed cpu  time: sys=0:00:00 usr=0:00:00
total=0:00:00
[End of Initial Routing] Stage (MB): Used    0  Alloctr    0  Proc    0
[End of Initial Routing] Total (MB): Used   20  Alloctr   21  Proc 2208
Initial. Routing result:
Initial. Both Dirs: Overflow =     0 Max = 0 GRCs =     0 (0.00%)
Initial. H routing: Overflow =     0 Max = 0 (GRCs =  0) GRCs =     0
(0.00%)
Initial. V routing: Overflow =     0 Max = 0 (GRCs =  0) GRCs =     0
(0.00%)
Initial. M1         Overflow =     0 Max = 0 (GRCs =  0) GRCs =     0
(0.00%)
Initial. M2         Overflow =     0 Max = 0 (GRCs =  0) GRCs =     0
(0.00%)
Initial. M3         Overflow =     0 Max = 0 (GRCs =  0) GRCs =     0
(0.00%)
Initial. TOP_M      Overflow =     0 Max = 0 (GRCs =  0) GRCs =     0
(0.00%)

Initial. Total Wire Length = 0.00
Initial. Layer M1 wire length = 0.00
Initial. Layer M2 wire length = 0.00
Initial. Layer M3 wire length = 0.00
Initial. Layer TOP_M wire length = 0.00
Initial. Total Number of Contacts = 0
Initial. Via V2_cross count = 0
Initial. Via V3_cross count = 0
Initial. Via VL count = 0
Initial. completed.

Start GR phase 1
Current Stage stats:
[End of Phase1 Routing] Elapsed real time: 0:00:00
[End of Phase1 Routing] Elapsed cpu  time: sys=0:00:00 usr=0:00:00
total=0:00:00
[End of Phase1 Routing] Stage (MB): Used    0  Alloctr    0  Proc    0
[End of Phase1 Routing] Total (MB): Used   20  Alloctr   21  Proc 2208
phase1. Routing result:
phase1. Both Dirs: Overflow =     0 Max = 0 GRCs =     0 (0.00%)
```

```
phase1. H routing: Overflow =     0 Max = 0 (GRCs =  0) GRCs =     0 (0.00%)
phase1. V routing: Overflow =     0 Max = 0 (GRCs =  0) GRCs =     0 (0.00%)
phase1. M1         Overflow =     0 Max = 0 (GRCs =  0) GRCs =     0 (0.00%)
phase1. M2         Overflow =     0 Max = 0 (GRCs =  0) GRCs =     0 (0.00%)
phase1. M3         Overflow =     0 Max = 0 (GRCs =  0) GRCs =     0 (0.00%)
phase1. TOP_M      Overflow =     0 Max = 0 (GRCs =  0) GRCs =     0 (0.00%)

phase1. Total Wire Length = 0.00
phase1. Layer M1 wire length = 0.00
phase1. Layer M2 wire length = 0.00
phase1. Layer M3 wire length = 0.00
phase1. Layer TOP_M wire length = 0.00
phase1. Total Number of Contacts = 0
phase1. Via V2_cross count = 0
phase1. Via V3_cross count = 0
phase1. Via VL count = 0
phase1. completed.

Start GR phase 2
Current Stage stats:
[End of Phase2 Routing] Elapsed real time: 0:00:00
[End of Phase2 Routing] Elapsed cpu  time: sys=0:00:00 usr=0:00:00
total=0:00:00
[End of Phase2 Routing] Stage (MB): Used    0  Alloctr    0  Proc    0
[End of Phase2 Routing] Total (MB): Used   20  Alloctr   21  Proc 2208
phase2. Routing result:
phase2. Both Dirs: Overflow =     0 Max = 0 GRCs =     0 (0.00%)
phase2. H routing: Overflow =     0 Max = 0 (GRCs =  0) GRCs =     0 (0.00%)
phase2. V routing: Overflow =     0 Max = 0 (GRCs =  0) GRCs =     0 (0.00%)
phase2. M1         Overflow =     0 Max = 0 (GRCs =  0) GRCs =     0 (0.00%)
phase2. M2         Overflow =     0 Max = 0 (GRCs =  0) GRCs =     0 (0.00%)
phase2. M3         Overflow =     0 Max = 0 (GRCs =  0) GRCs =     0 (0.00%)
phase2. TOP_M      Overflow =     0 Max = 0 (GRCs =  0) GRCs =     0 (0.00%)

phase2. Total Wire Length = 0.00
phase2. Layer M1 wire length = 0.00
phase2. Layer M2 wire length = 0.00
phase2. Layer M3 wire length = 0.00
phase2. Layer TOP_M wire length = 0.00
phase2. Total Number of Contacts = 0
phase2. Via V2_cross count = 0
phase2. Via V3_cross count = 0
```

```
phase2. Via VL count = 0
phase2. completed.
[End of Whole Chip Routing] Elapsed real time: 0:00:00
[End of Whole Chip Routing] Elapsed cpu  time: sys=0:00:00 usr=0:00:00
total=0:00:00
[End of Whole Chip Routing] Stage (MB): Used    1  Alloctr    1  Proc    0
[End of Whole Chip Routing] Total (MB): Used   20  Alloctr   21  Proc 2208

Congestion utilization per direction:
Average vertical track utilization   =  0.59 %
Peak    vertical track utilization   = 13.33 %
Average horizontal track utilization =  0.67 %
Peak    horizontal track utilization = 33.33 %

Current Stage stats:
[GR: Done] Elapsed real time: 0:00:00
[GR: Done] Elapsed cpu  time: sys=0:00:00 usr=0:00:00 total=0:00:00
[GR: Done] Stage (MB): Used    0  Alloctr    0  Proc    0
[GR: Done] Total (MB): Used   20  Alloctr   21  Proc 2208
GR Total stats:
[GR: Done] Elapsed real time: 0:00:00
[GR: Done] Elapsed cpu  time: sys=0:00:00 usr=0:00:00 total=0:00:00
[GR: Done] Stage (MB): Used    1  Alloctr    1  Proc    0
[GR: Done] Total (MB): Used   20  Alloctr   21  Proc 2208
Updating congestion ...
Final total stats:
[End of Global Routing] Elapsed real time: 0:00:00
[End of Global Routing] Elapsed cpu  time: sys=0:00:00 usr=0:00:00
total=0:00:00
[End of Global Routing] Stage (MB): Used    0  Alloctr    0  Proc    0
[End of Global Routing] Total (MB): Used   19  Alloctr   19  Proc 2208

Start track assignment

Printing options for 'set_route_zrt_common_options'
-concurrent_redundant_via_effort_level                  :        high
-concurrent_redundant_via_mode                          :
insert_at_high_cost
-post_detail_route_redundant_via_insertion              :        high

Printing options for 'set_route_zrt_track_options'
```

```
Information: Using 1 threads for routing. (ZRT-444)

[Track Assign: Read routes] Elapsed real time: 0:00:00
[Track Assign: Read routes] Elapsed cpu  time: sys=0:00:00 usr=0:00:00
total=0:00:00
[Track Assign: Read routes] Stage (MB): Used    0  Alloctr    0  Proc    0
[Track Assign: Read routes] Total (MB): Used   15  Alloctr   16  Proc 2208

        There were 74 out of 6626 pins with no spots.

Printing options for 'set_route_zrt_common_options'
-concurrent_redundant_via_effort_level                  :        high
-concurrent_redundant_via_mode                          :
insert_at_high_cost
-post_detail_route_redundant_via_insertion              :        high

Printing options for 'set_route_zrt_detail_options'

[Dr init] Elapsed real time: 0:00:00
[Dr init] Elapsed cpu  time: sys=0:00:00 usr=0:00:00 total=0:00:00
[Dr init] Stage (MB): Used    2  Alloctr    2  Proc    0
[Dr init] Total (MB): Used   17  Alloctr   18  Proc 2208
Total number of nets = 2436, of which 0 are not extracted
Total number of open nets = 2389, of which 0 are frozen
Information: Using 1 threads for routing. (ZRT-444)
Start DR iteration 0: uniform partition
Routed  5/121 Partitions, Violations =  0
Routed  8/121 Partitions, Violations =  0
Routed  9/121 Partitions, Violations =  0
Routed  12/121 Partitions, Violations = 0
Routed  13/121 Partitions, Violations = 0
Routed  14/121 Partitions, Violations = 0
Routed  17/121 Partitions, Violations = 0
Routed  18/121 Partitions, Violations = 0
Routed  19/121 Partitions, Violations = 0
Routed  20/121 Partitions, Violations = 0
Routed  23/121 Partitions, Violations = 0
Routed  24/121 Partitions, Violations = 0
Routed  25/121 Partitions, Violations = 0
Routed  26/121 Partitions, Violations = 0
Routed  27/121 Partitions, Violations = 0
Routed  28/121 Partitions, Violations = 0
```

```
Routed  30/121 Partitions, Violations = 0
Routed  31/121 Partitions, Violations = 0
Routed  32/121 Partitions, Violations = 0
Routed  33/121 Partitions, Violations = 0
Routed  34/121 Partitions, Violations = 0
Routed  35/121 Partitions, Violations = 0
Routed  36/121 Partitions, Violations = 0
Routed  38/121 Partitions, Violations = 0
Routed  39/121 Partitions, Violations = 0
Routed  40/121 Partitions, Violations = 0
Routed  41/121 Partitions, Violations = 0
Routed  42/121 Partitions, Violations = 0
Routed  43/121 Partitions, Violations = 0
Routed  44/121 Partitions, Violations = 0
Routed  45/121 Partitions, Violations = 0
Routed  47/121 Partitions, Violations = 0
Routed  48/121 Partitions, Violations = 0
Routed  49/121 Partitions, Violations = 0
Routed  50/121 Partitions, Violations = 0
Routed  51/121 Partitions, Violations = 0
Routed  52/121 Partitions, Violations = 0
Routed  53/121 Partitions, Violations = 0
Routed  54/121 Partitions, Violations = 0
Routed  55/121 Partitions, Violations = 0
Routed  58/121 Partitions, Violations = 0
Routed  59/121 Partitions, Violations = 0
Routed  60/121 Partitions, Violations = 0
Routed  61/121 Partitions, Violations = 0
Routed  62/121 Partitions, Violations = 0
Routed  63/121 Partitions, Violations = 0
Routed  64/121 Partitions, Violations = 0
Routed  69/121 Partitions, Violations = 0
Routed  70/121 Partitions, Violations = 0
Routed  71/121 Partitions, Violations = 0
Routed  72/121 Partitions, Violations = 0
Routed  73/121 Partitions, Violations = 0
Routed  74/121 Partitions, Violations = 0
Routed  79/121 Partitions, Violations = 0
Routed  80/121 Partitions, Violations = 0
Routed  81/121 Partitions, Violations = 0
Routed  82/121 Partitions, Violations = 0
Routed  83/121 Partitions, Violations = 0
```

```
Routed  88/121 Partitions, Violations = 0
Routed  89/121 Partitions, Violations = 0
Routed  90/121 Partitions, Violations = 0
Routed  91/121 Partitions, Violations = 0
Routed  96/121 Partitions, Violations = 0
Routed  97/121 Partitions, Violations = 0
Routed  98/121 Partitions, Violations = 0
Routed  103/121 Partitions, Violations =        0
Routed  104/121 Partitions, Violations =        0
Routed  109/121 Partitions, Violations =        0

DRC-SUMMARY:
        @@@@@@@ TOTAL VIOLATIONS =      0

[Iter 0] Elapsed real time: 0:00:00
[Iter 0] Elapsed cpu  time: sys=0:00:00 usr=0:00:00 total=0:00:00
[Iter 0] Stage (MB): Used    9  Alloctr    9  Proc    0
[Iter 0] Total (MB): Used   24  Alloctr   25  Proc 2208

End DR iteration 0 with 121 parts

Finish DR since reached 0 DRC

[DR] Elapsed real time: 0:00:00
[DR] Elapsed cpu  time: sys=0:00:00 usr=0:00:00 total=0:00:00
[DR] Stage (MB): Used    0  Alloctr    0  Proc    0
[DR] Total (MB): Used   15  Alloctr   16  Proc 2208

DR finished with 0 violations
DRC-SUMMARY:
        @@@@@@@ TOTAL VIOLATIONS =      0


Total Wire Length =                    8965 micron
Total Number of Contacts =             1802
Total Number of Wires =                1250
Total Number of PtConns =              433
Total Number of Routed Wires =       1250
Total Routed Wire Length =           8851 micron
Total Number of Routed Contacts =       1802
        Layer            M1 :         31 micron
        Layer            M2 :        187 micron
```

```
        Layer            M3 :       4821 micron
        Layer         TOP_M :       3926 micron
        Via              VL :        621
        Via        V3_cross :        593
        Via        V2_cross :        576
        Via   V2_cross(rot) :         12


Redundant via conversion report:
--------------------------------

  Total optimized via conversion rate =  0.00% (0 / 1802 vias)

    Layer V2         =  0.00% (0      / 588     vias)
        Un-optimized = 100.00% (588     vias)
    Layer V3         =  0.00% (0      / 593     vias)
        Un-optimized = 100.00% (593     vias)
    Layer TOP_V      =  0.00% (0      / 621     vias)
        Un-optimized = 100.00% (621     vias)

  Total double via conversion rate    =  0.00% (0 / 1802 vias)

    Layer V2         =  0.00% (0      / 588     vias)
    Layer V3         =  0.00% (0      / 593     vias)
    Layer TOP_V      =  0.00% (0      / 621     vias)

  The optimized via conversion rate based on total routed via count =  0.00%
(0 / 1802 vias)

    Layer V2         =  0.00% (0      / 588     vias)
        Un-optimized = 100.00% (588     vias)
    Layer V3         =  0.00% (0      / 593     vias)
        Un-optimized = 100.00% (593     vias)
    Layer TOP_V      =  0.00% (0      / 621     vias)
        Un-optimized = 100.00% (621     vias)


Printing options for 'set_route_zrt_common_options'
-concurrent_redundant_via_effort_level                  :        high
-concurrent_redundant_via_mode                          :
insert_at_high_cost
-post_detail_route_redundant_via_insertion              :        high
```

```
Printing options for 'set_route_zrt_detail_options'

[Dr init] Elapsed real time: 0:00:00
[Dr init] Elapsed cpu  time: sys=0:00:00 usr=0:00:00 total=0:00:00
[Dr init] Stage (MB): Used    2  Alloctr    2  Proc    0
[Dr init] Total (MB): Used   17  Alloctr   18  Proc 2208

Redundant via optimization will attempt to replace the following vias:

          V2    -> V2_cross_2x1    V2_cross_2x1(r) V2_cross_1x2
V2_cross_1x2(r)

          V2(r) -> V2_cross_2x1    V2_cross_2x1(r) V2_cross_1x2
V2_cross_1x2(r)

          V3    -> V3_cross_1x2    V3_cross_1x2(r) V3_cross_2x1
V3_cross_2x1(r)

          V3(r) -> V3_cross_1x2    V3_cross_1x2(r) V3_cross_2x1
V3_cross_2x1(r)

          VL    ->     VL_2x1(r)     VL_2x1        VL_1x2(r)     VL_1x2

          VL(r) ->     VL_2x1(r)     VL_2x1        VL_1x2(r)     VL_1x2

    V2_cross    -> V2_cross_2x1    V2_cross_2x1(r) V2_cross_1x2
V2_cross_1x2(r)

    V2_cross(r) -> V2_cross_2x1    V2_cross_2x1(r) V2_cross_1x2
V2_cross_1x2(r)

    V3_cross    -> V3_cross_1x2    V3_cross_1x2(r) V3_cross_2x1
V3_cross_2x1(r)

    V3_cross(r) -> V3_cross_1x2    V3_cross_1x2(r) V3_cross_2x1
V3_cross_2x1(r)


        There were 74 out of 6626 pins with no spots.
```

```
[Technology Processing] Elapsed real time: 0:00:00
[Technology Processing] Elapsed cpu  time: sys=0:00:00 usr=0:00:00
total=0:00:00
[Technology Processing] Stage (MB): Used    2  Alloctr    2  Proc    0
[Technology Processing] Total (MB): Used   17  Alloctr   18  Proc 2208

Begin Redundant via insertion ...

Routed  1/9 Partitions, Violations =    0
Routed  2/9 Partitions, Violations =    0
Routed  3/9 Partitions, Violations =    0
Routed  4/9 Partitions, Violations =    0
Routed  5/9 Partitions, Violations =    0
Routed  6/9 Partitions, Violations =    0
Routed  7/9 Partitions, Violations =    0
Routed  8/9 Partitions, Violations =    0
Routed  9/9 Partitions, Violations =    0

RedundantVia finished with 0 violations


DRC-SUMMARY:
        @@@@@@@ TOTAL VIOLATIONS =      0


Total Wire Length =                    8802 micron
Total Number of Contacts =             1802
Total Number of Wires =                1201
Total Number of PtConns =              3
Total Number of Routed Wires =       1201
Total Routed Wire Length =           8800 micron
Total Number of Routed Contacts =       1802
        Layer                M1 :         22 micron
        Layer                M2 :         52 micron
        Layer                M3 :       4805 micron
        Layer             TOP_M :       3923 micron
        Via              VL_1x2 :          6
        Via         VL(rot)_2x1 :        587
        Via         VL(rot)_1x2 :          7
        Via              VL_2x1 :         21
        Via        V3_cross_1x2 :        515
        Via   V3_cross(rot)_2x1 :         33
```

```
        Via   V3_cross(rot)_1x2 :          8
        Via        V3_cross_2x1 :         37
        Via        V2_cross_1x2 :        142
        Via   V2_cross(rot)_2x1 :         55
        Via   V2_cross(rot)_1x2 :          1
        Via        V2_cross_2x1 :        390


Redundant via conversion report:
--------------------------------

  Total optimized via conversion rate = 100.00% (1802 / 1802 vias)

    Layer V2         = 100.00% (588    / 588     vias)
        Weight 1     = 100.00% (588     vias)
        Un-optimized =  0.00% (0       vias)
    Layer V3         = 100.00% (593    / 593     vias)
        Weight 1     = 100.00% (593     vias)
        Un-optimized =  0.00% (0       vias)
    Layer TOP_V      = 100.00% (621    / 621     vias)
        Weight 1     = 100.00% (621     vias)
        Un-optimized =  0.00% (0       vias)

  Total double via conversion rate    = 100.00% (1802 / 1802 vias)

    Layer V2         = 100.00% (588    / 588     vias)
    Layer V3         = 100.00% (593    / 593     vias)
    Layer TOP_V      = 100.00% (621    / 621     vias)

  The optimized via conversion rate based on total routed via count =
100.00% (1802 / 1802 vias)

    Layer V2         = 100.00% (588    / 588     vias)
        Weight 1     = 100.00% (588     vias)
        Un-optimized =  0.00% (0       vias)
    Layer V3         = 100.00% (593    / 593     vias)
        Weight 1     = 100.00% (593     vias)
        Un-optimized =  0.00% (0       vias)
    Layer TOP_V      = 100.00% (621    / 621     vias)
        Weight 1     = 100.00% (621     vias)
        Un-optimized =  0.00% (0       vias)
```

```
[RedundantVia] Elapsed real time: 0:00:00
[RedundantVia] Elapsed cpu  time: sys=0:00:00 usr=0:00:00 total=0:00:00
[RedundantVia] Stage (MB): Used    9  Alloctr    9  Proc    0
[RedundantVia] Total (MB): Used   24  Alloctr   25  Proc 2208

Begin DRC fixing ...

[Dr init] Elapsed real time: 0:00:01
[Dr init] Elapsed cpu  time: sys=0:00:00 usr=0:00:01 total=0:00:01
[Dr init] Stage (MB): Used   10  Alloctr   10  Proc    0
[Dr init] Total (MB): Used   24  Alloctr   25  Proc 2208
Total number of nets = 2436, of which 0 are not extracted
Total number of open nets = 2389, of which 0 are frozen
Information: Using 1 threads for routing. (ZRT-444)
Finish DR since reached 0 DRC

[DR] Elapsed real time: 0:00:01
[DR] Elapsed cpu  time: sys=0:00:00 usr=0:00:01 total=0:00:01
[DR] Stage (MB): Used    7  Alloctr    7  Proc    0
[DR] Total (MB): Used   22  Alloctr   23  Proc 2208
[DR: Done] Elapsed real time: 0:00:01
[DR: Done] Elapsed cpu  time: sys=0:00:00 usr=0:00:01 total=0:00:01
[DR: Done] Stage (MB): Used    0  Alloctr    0  Proc    0
[DR: Done] Total (MB): Used   15  Alloctr   16  Proc 2208
[DR: Done] Elapsed real time: 0:00:01
[DR: Done] Elapsed cpu  time: sys=0:00:00 usr=0:00:01 total=0:00:01
[DR: Done] Stage (MB): Used    0  Alloctr    0  Proc    0
[DR: Done] Total (MB): Used   15  Alloctr   16  Proc 2208

DR finished with 0 open nets, of which 0 are frozen

DR finished with 0 violations
****************************************
Report : qor
Design : CORDIC
Version: O-2018.06-SP4
Date   : Sat Apr  6 17:01:50 2019
****************************************


  Timing Path Group 'clock'
```

```
-----------------------------------
Levels of Logic:              20.00
Critical Path Length:          8.04
Critical Path Slack:           0.76
Critical Path Clk Period:     10.00
Total Negative Slack:          0.00
No. of Violating Paths:        0.00
Worst Hold Violation:         -0.36
Total Hold Violation:         -8.18
No. of Hold Violations:       36.00
-----------------------------------


Cell Count
-----------------------------------
Hierarchical Cell Count:          0
Hierarchical Port Count:          0
Leaf Cell Count:               1858
Buf/Inv Cell Count:              90
Buf Cell Count:                  45
Inv Cell Count:                  45
CT Buf/Inv Cell Count:           15
Combinational Cell Count:      1278
Sequential Cell Count:          580
Macro Count:                      0
-----------------------------------


Area
-----------------------------------
Combinational Area:    50936.231256
Noncombinational Area: 34754.221024
Buf/Inv Area:           1709.190022
Total Buffer Area:          1244.97
Total Inverter Area:         464.22
Macro/Black Box Area:      0.000000
Net Area:                  0.000000
Net XLength        :       50873.83
Net YLength        :       48199.33
-----------------------------------
Cell Area:             85690.452280
Design Area:           85690.452280
```

```
  Net Length        :        99073.16


  Design Rules
  ----------------------------------
  Total Number of Nets:          2405
  Nets With Violations:             0
  Max Trans Violations:             0
  Max Cap Violations:               0
  ----------------------------------


  Hostname: synopsysserver

  Compile CPU Statistics
  ----------------------------------------
  Resource Sharing:                   4.32
  Logic Optimization:                 4.48
  Mapping Optimization:               3.24
  ----------------------------------------
  Overall Compile Time:              21.27
  Overall Compile Wall Clock Time:   22.61

  --------------------------------------------------------------------

  Design  WNS: 0.00  TNS: 0.00  Number of Violating Paths: 0


  Design (Hold)  WNS: 0.36  TNS: 8.18  Number of Violating Paths: 36

  --------------------------------------------------------------------



ROPT:    (SETUP) WNS: 0.0000 TNS: 0.0000  Number of Violating Path: 0
ROPT:    (HOLD) WNS: 0.3616 TNS: 8.1791  Number of Violating Path: 36
ROPT:    Number of DRC Violating Nets: 0
ROPT:    Number of Route Violation: 0
Output DEF file
Information: Writing ROWS statement (DDEFW-014)
Information: Completed ROWS statement  (DDEFW-016)
Information: Writing TRACKS statement (DDEFW-014)
```

```
Information: Completed TRACKS statement  (DDEFW-016)
Information: Writing GCELLGRID statement (DDEFW-014)
Information: Completed GCELLGRID statement  (DDEFW-016)
Information: Writing VIAS section (DDEFW-014)
Information: Completed VIAS section  (DDEFW-016)
Information: Writing COMPONENTS section (DDEFW-014)
Information: Completed COMPONENTS 1000/1858 (DDEFW-015)
Information: Completed COMPONENTS section  (DDEFW-016)
Information: Writing PINS section (DDEFW-014)
Information: Completed PINS section  (DDEFW-016)
Information: Writing SPECIALNETS section (DDEFW-014)
Information: Completed SPECIALNETS section  (DDEFW-016)
Information: Writing NETS section (DDEFW-014)
Information: Completed NETS 1000/2434 (DDEFW-015)
Information: Completed NETS 2000/2434 (DDEFW-015)
Information: Completed NETS section  (DDEFW-016)
DEF output completed
```

13. EDA Tool Details

The following tools have been used here and all these are provided by Synopsys.

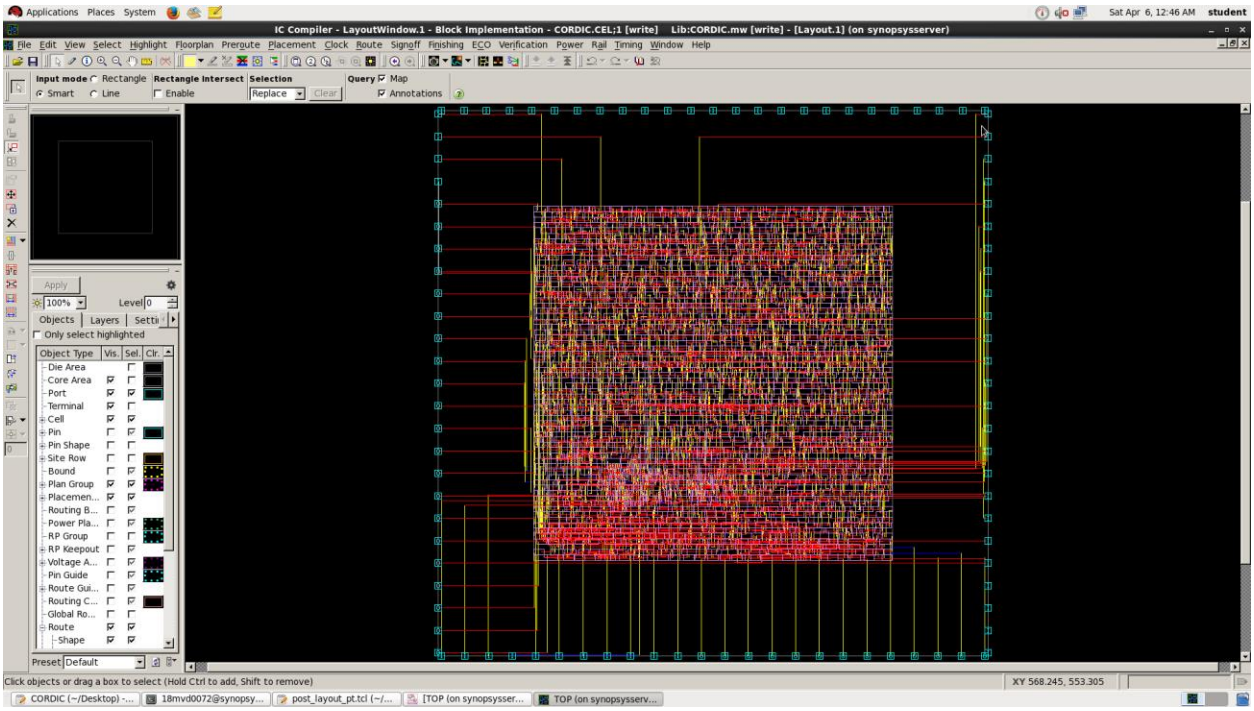
13.1. dc_shell: This is the design compiler. This supports both flat and hierarchical designs.

13.2. dc_topo: This is known as design compiler graphical. This delivers superior quality of results and streamlines the flow for a faster, more predictable design implementation.

13.3. pt_shell: Prime Time is static timing analysis tool from Synopsys.

13.4. icc_shell: The IC compiler place and route system , is a single, convergent, chip-level physical implementation tool.

Screenshot after Placement and Routing:



14. Conclusion:

Hence, the CORDIC Algorithm has been implemented according to Front-End and Back-End ASIC flow respectively using SCL Library.RTL Code is simulated using Synopsys VCS Compiler.Placement and Routing is done using Synopsys ICC Compiler.

15. References

[1] Dr.B.V.Uma, Sagar D.M, Kavya Sharat "Calculation of Sine and Cosine of an Angle using the CORDIC Algorithm", IJITR, International Journal Of Innovative Technology And Research Volume No.2, Issue No. 2,February – March 2014, 891 – 895.

[2] Praveen Yadav, Karan Singh, "A Review Paper on CORDIC Algorithm and Its Applications for Current Technology" International Journal of Science and Research (IJSR).

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[4] Tanya Vladimirova and Hans Tiggeler, " FPGA Implementation of Sine and Cosine Generators Using the CORDIC Algorithm" Space Centre University of Surrey, Guildford, Surrey

[5] Aimei Tang, Li Yu, Fangjian Han, Zhiqiang Zhang, CORDIC-based FFT Real-time Processing Design and FPGA Implementation, 2016 IEEE 12th International Colloquium on Signal Processing & its Applications (CSPA2016), 4 - 6 March 2016, Melaka, Malaysia

[6] Bhawna Tiwari, Nidhi Goel,Implementation of a Fast Hybrid CORDIC Architecture, Second International Conference on Computational Intelligence & Communication Technology,2016

[7] Sayantan Pramanik, Sayak Chakraborty, Rishav Saha, Ritam Banerjee, Rupkatha Basu, Ritam De, Sulagna Chatterjee,Low Latency High Throughput CORDIC based Fourier Analysis,IEEE,2015

[8] M Madhu Babu, K Rama Naidu, Implementation of Multiplexers based Pipelined CORDIC for OFDM systems, IEEE International Conference On Recent Trends In Electronics Information Communication Technology, May 20-21, 2016, India

[9] Hong-Thu Nguyen, Xuan-Thuan Nguyen, and Cong-Kha Pham,An Efficient Fixed Using A Hybrid CORDIC Algorithm,IEEE,2018

[10] Akarshika Singhal, Anjana Goen, Tanutrushna Mohapatra ,FPGA Implementation and Power Efficient CORDIC based ADPLL for Signal Processing and Application, 7 th International Conference on Communication Systems and Network Technologies,2017

[11] Ray Andraka,7th International Conference on Communication Systems and Network Technologies,2017

16. Appendix

16.1 Synthesis script in case of dc_shell:

```
set search_path "./ref/models ./ref/icons " ;

set TARGET_LIBRARY_FILES         saed90nm_typ_ht.db                  ;#
Logical technology library file

set SYMBOL_LIBRARY_FILES         saed90nm.sdb                    ;#  Symbol
library file

########################################################################
# Logical Library Settings
########################################################################
set_app_var search_path "$search_path"
set_app_var target_library $TARGET_LIBRARY_FILES
set_app_var link_library "* $target_library "
set_app_var symbol_library $SYMBOL_LIBRARY_FILES


read_verilog  ./CORDIC.v
current_design CORDIC
link
check_design
read_saif -input ../RTL/cordic_topo.saif -instance CORDIC_TESTBENCH/s1
source ./CORDIC.sdc
check_timing

set_wire_load_model -name "8000"
```

```
set_wire_load_mode segmented

compile_ultra

report_area
report_constraint
report_timing

change_names -rule verilog -hier
write -hierarchy -format verilog -output ./CORDIC_dc.v
```

16.1. Synthesis script in case of dc_topo:

```
        ###### Synthesis Script in DC-TOPO MODE #######
# Save log File#
set sh_output_log_file "logs/dc_topo.log"

## Library Paths Logical & Physical Libraries####

set LIBRARY_HOME "/home/synopsys/pdk/scl_pdk/stdlib/" ;# Parent home for
synopsys libraries

set LOGICAL_LIBRARY_PATH  "${LIBRARY_HOME}/fs120/liberty/lib_flow_ss " ;#
Additional search path to be added to the default search path
#  Target technology logical libraries

set TARGET_LIBRARY_FILES      "tsl18fs120_scl_ss.db"   ;

# milkyway reference libraries

set MW_REFERENCE_LIB_DIRS " ${LIBRARY_HOME}/fs120/mw/fs120_scl/" ;

## Give the path to the verilog files and update library files



## Sets the value of an application variable.

set_app_var search_path "${LOGICAL_LIBRARY_PATH} $search_path"
set_app_var target_library ${TARGET_LIBRARY_FILES}
set_app_var synthetic_library dw_foundation.sldb
set_app_var link_library "* $target_library dw_foundation.sldb"

lappend search_path ../RTL/CORDIC.v
```

```
#### Create Milkyway Library#########

create_mw_lib -technology
"/home/synopsys/pdk/scl_pdk/design_kit/icc_tech/icc.tf" -
mw_reference_library $MW_REFERENCE_LIB_DIRS CORDIC.mw

open_mw_lib CORDIC.mw

##### Check Library Consistency ###########
#check_library

##### Set TLU plus file and mapping file########

set_tlu_plus_files -max_tluplus
"/home/synopsys/pdk/scl_pdk/design_kit/icc_tech/tluplus/RCE_TS18SL_SCL_STA
R_RCXT_4M1L_TYP.tlup"  -tech2itf_map
"/home/synopsys/pdk/scl_pdk/design_kit/icc_tech/RCE_TS18SL_STAR_RCXT_4M1L.
map"

#########Check TLU plus file Consistency##########

check_tlu_plus_files

read_saif -input ../RTL/cordic_topo.saif -instance CORDIC_TESTBENCH/s1

## read the verilog files###################

analyze  -format verilog ../RTL/CORDIC.v
elaborate CORDIC

#### Explicitly Define Current Design ########
current_design CORDIC

######Locates all design and library components referenced in the current
design and links them to current design
link

###### checks your design for connectivity and hierarchy issues ##########
check_design  > reports/synth_check_design.rpt

######### Save ddc design before compile (Unmapped ddc) ##############
```

```
write_file -f ddc -hier -output reports/CORDIC_topo1.ddc

####### Source optimization constraint and Physical
Constraint#############

source ../constraints/cordic.sdc


########## Verify that all internal and IO paths are constrainedcheck
syntax error on the constraint file############
check_timing

source ../constraints/CORDIC_topo1.pcon
#############Buffer Multiple Port Nets - Eliminate Assign #########
#set_fix_multiple_ports_nets -all

######### Synthesize the design using compile_ultra
################################

compile_ultra

############# Convert tri to wire - Eliminate Assign #########
set_app_var verilogout_no_tri true

## Below commands report area , cell, qor, resources, and timing
information needed to analyze the design.

  report_area > reports/synth_area.rpt
  report_design > reports/synth_design.rpt
  report_cell > reports/synth_cells.rpt
  report_qor  > reports/synth_qor.rpt
  report_resources > reports/synth_resources.rpt
  report_timing > reports/synth_timing.rpt
  report_power -analysis_effort medium > reports/synth_power.rpt
  report_physical_constraints > reports/synth_phycon.rpt
  report_area -physical > reports/synth_phyarea.rpt
  report_congestion  > reports/synth_synthcon.rpt
```

```
######### Save ddc design after compile (mapped ddc) & for icc input
##############

write_file -f ddc -hier -output reports/CORDIC_topo1.ddc

######### Save verilog netlist after compile  ##############

write_file -f verilog -hier -output reports/CORDIC_topo1_dc.v
########### Write file for icc2 input ################
#write_icc2_files -out DESIGN_icc2
```

16.2. cordic.sdc (for synthesis):

```
create_clock -name clock -period 10 [get_ports clock]
set_clock_transition 0.3 [get_clocks clock]
set_clock_uncertainty -setup 1 [get_clocks clock]
set_clock_uncertainty -hold 0.1 [get_clocks clock]
set_clock_latency 0.5 -source -min [get_clocks clock]
set_clock_latency 1 -source -max [get_clocks clock]

set_input_delay -clock clock -max 4 [get_ports angle[0]]
set_input_delay -clock clock -max 4 [get_ports angle[1]]
set_input_delay -clock clock -max 4 [get_ports angle[2]]
set_input_delay -clock clock -max 4 [get_ports angle[3]]
set_input_delay -clock clock -max 4 [get_ports angle[4]]
set_input_delay -clock clock -max 4 [get_ports angle[5]]
set_input_delay -clock clock -max 4 [get_ports angle[6]]
set_input_delay -clock clock -max 4 [get_ports angle[7]]
set_input_delay -clock clock -max 4 [get_ports angle[8]]
set_input_delay -clock clock -max 4 [get_ports angle[9]]
set_input_delay -clock clock -max 4 [get_ports angle[10]]
set_input_delay -clock clock -max 4 [get_ports angle[11]]
set_input_delay -clock clock -max 4 [get_ports angle[12]]
set_input_delay -clock clock -max 4 [get_ports angle[13]]
set_input_delay -clock clock -max 4 [get_ports angle[14]]
set_input_delay -clock clock -max 4 [get_ports angle[15]]
set_input_delay -clock clock -max 4 [get_ports angle[16]]
set_input_delay -clock clock -max 4 [get_ports angle[17]]
set_input_delay -clock clock -max 4 [get_ports angle[18]]
set_input_delay -clock clock -max 4 [get_ports angle[19]]
set_input_delay -clock clock -max 4 [get_ports angle[20]]
set_input_delay -clock clock -max 4 [get_ports angle[21]]
set_input_delay -clock clock -max 4 [get_ports angle[22]]
```

```
set_input_delay -clock clock -max 4 [get_ports angle[23]]
set_input_delay -clock clock -max 4 [get_ports angle[24]]
set_input_delay -clock clock -max 4 [get_ports angle[25]]
set_input_delay -clock clock -max 4 [get_ports angle[26]]
set_input_delay -clock clock -max 4 [get_ports angle[27]]
set_input_delay -clock clock -max 4 [get_ports angle[28]]
set_input_delay -clock clock -max 4 [get_ports angle[29]]
set_input_delay -clock clock -max 4 [get_ports angle[30]]
set_input_delay -clock clock -max 4 [get_ports angle[31]]

set_input_delay -clock clock -min 0 [get_ports angle[0]]
set_input_delay -clock clock -min 0 [get_ports angle[1]]
set_input_delay -clock clock -min 0 [get_ports angle[2]]
set_input_delay -clock clock -min 0 [get_ports angle[3]]
set_input_delay -clock clock -min 0 [get_ports angle[4]]
set_input_delay -clock clock -min 0 [get_ports angle[5]]
set_input_delay -clock clock -min 0 [get_ports angle[6]]
set_input_delay -clock clock -min 0 [get_ports angle[7]]
set_input_delay -clock clock -min 0 [get_ports angle[8]]
set_input_delay -clock clock -min 0 [get_ports angle[9]]
set_input_delay -clock clock -min 0 [get_ports angle[10]]
set_input_delay -clock clock -min 0 [get_ports angle[11]]
set_input_delay -clock clock -min 0 [get_ports angle[12]]
set_input_delay -clock clock -min 0 [get_ports angle[13]]
set_input_delay -clock clock -min 0 [get_ports angle[14]]
set_input_delay -clock clock -min 0 [get_ports angle[15]]
set_input_delay -clock clock -min 0 [get_ports angle[16]]
set_input_delay -clock clock -min 0 [get_ports angle[17]]
set_input_delay -clock clock -min 0 [get_ports angle[18]]
set_input_delay -clock clock -min 0 [get_ports angle[19]]
set_input_delay -clock clock -min 0 [get_ports angle[20]]
set_input_delay -clock clock -min 0 [get_ports angle[21]]
set_input_delay -clock clock -min 0 [get_ports angle[22]]
set_input_delay -clock clock -min 0 [get_ports angle[23]]
set_input_delay -clock clock -min 0 [get_ports angle[24]]
set_input_delay -clock clock -min 0 [get_ports angle[25]]
set_input_delay -clock clock -min 0 [get_ports angle[26]]
set_input_delay -clock clock -min 0 [get_ports angle[27]]
set_input_delay -clock clock -min 0 [get_ports angle[28]]
set_input_delay -clock clock -min 0 [get_ports angle[29]]
set_input_delay -clock clock -min 0 [get_ports angle[30]]
set_input_delay -clock clock -min 0 [get_ports angle[31]]
```

```
set_input_delay -clock clock -max 4 [get_ports Xin[0]]
set_input_delay -clock clock -max 4 [get_ports Xin[1]]
set_input_delay -clock clock -max 4 [get_ports Xin[2]]
set_input_delay -clock clock -max 4 [get_ports Xin[3]]
set_input_delay -clock clock -max 4 [get_ports Xin[4]]
set_input_delay -clock clock -max 4 [get_ports Xin[5]]
set_input_delay -clock clock -max 4 [get_ports Xin[6]]
set_input_delay -clock clock -max 4 [get_ports Xin[7]]
set_input_delay -clock clock -max 4 [get_ports Xin[8]]
set_input_delay -clock clock -max 4 [get_ports Xin[9]]
set_input_delay -clock clock -max 4 [get_ports Xin[10]]
set_input_delay -clock clock -max 4 [get_ports Xin[11]]
set_input_delay -clock clock -max 4 [get_ports Xin[12]]
set_input_delay -clock clock -max 4 [get_ports Xin[13]]
set_input_delay -clock clock -max 4 [get_ports Xin[14]]
set_input_delay -clock clock -max 4 [get_ports Xin[15]]

set_input_delay -clock clock -min 0 [get_ports Xin[0]]
set_input_delay -clock clock -min 0 [get_ports Xin[1]]
set_input_delay -clock clock -min 0 [get_ports Xin[2]]
set_input_delay -clock clock -min 0 [get_ports Xin[3]]
set_input_delay -clock clock -min 0 [get_ports Xin[4]]
set_input_delay -clock clock -min 0 [get_ports Xin[5]]
set_input_delay -clock clock -min 0 [get_ports Xin[6]]
set_input_delay -clock clock -min 0 [get_ports Xin[7]]
set_input_delay -clock clock -min 0 [get_ports Xin[8]]
set_input_delay -clock clock -min 0 [get_ports Xin[9]]
set_input_delay -clock clock -min 0 [get_ports Xin[10]]
set_input_delay -clock clock -min 0 [get_ports Xin[11]]
set_input_delay -clock clock -min 0 [get_ports Xin[12]]
set_input_delay -clock clock -min 0 [get_ports Xin[13]]
set_input_delay -clock clock -min 0 [get_ports Xin[14]]
set_input_delay -clock clock -min 0 [get_ports Xin[15]]

set_input_delay -clock clock -max 4 [get_ports Yin[0]]
set_input_delay -clock clock -max 4 [get_ports Yin[1]]
set_input_delay -clock clock -max 4 [get_ports Yin[2]]
set_input_delay -clock clock -max 4 [get_ports Yin[3]]
set_input_delay -clock clock -max 4 [get_ports Yin[4]]
set_input_delay -clock clock -max 4 [get_ports Yin[5]]
set_input_delay -clock clock -max 4 [get_ports Yin[6]]
```

```
set_input_delay -clock clock -max 4 [get_ports Yin[7]]
set_input_delay -clock clock -max 4 [get_ports Yin[8]]
set_input_delay -clock clock -max 4 [get_ports Yin[9]]
set_input_delay -clock clock -max 4 [get_ports Yin[10]]
set_input_delay -clock clock -max 4 [get_ports Yin[11]]
set_input_delay -clock clock -max 4 [get_ports Yin[12]]
set_input_delay -clock clock -max 4 [get_ports Yin[13]]
set_input_delay -clock clock -max 4 [get_ports Yin[14]]
set_input_delay -clock clock -max 4 [get_ports Yin[15]]

set_input_delay -clock clock -min 0 [get_ports Yin[0]]
set_input_delay -clock clock -min 0 [get_ports Yin[1]]
set_input_delay -clock clock -min 0 [get_ports Yin[2]]
set_input_delay -clock clock -min 0 [get_ports Yin[3]]
set_input_delay -clock clock -min 0 [get_ports Yin[4]]
set_input_delay -clock clock -min 0 [get_ports Yin[5]]
set_input_delay -clock clock -min 0 [get_ports Yin[6]]
set_input_delay -clock clock -min 0 [get_ports Yin[7]]
set_input_delay -clock clock -min 0 [get_ports Yin[8]]
set_input_delay -clock clock -min 0 [get_ports Yin[9]]
set_input_delay -clock clock -min 0 [get_ports Yin[10]]
set_input_delay -clock clock -min 0 [get_ports Yin[11]]
set_input_delay -clock clock -min 0 [get_ports Yin[12]]
set_input_delay -clock clock -min 0 [get_ports Yin[13]]
set_input_delay -clock clock -min 0 [get_ports Yin[14]]
set_input_delay -clock clock -min 0 [get_ports Yin[15]]

set_output_delay -clock clock -max 4 [get_ports Xout[0]]
set_output_delay -clock clock -max 4 [get_ports Xout[1]]
set_output_delay -clock clock -max 4 [get_ports Xout[2]]
set_output_delay -clock clock -max 4 [get_ports Xout[3]]
set_output_delay -clock clock -max 4 [get_ports Xout[4]]
set_output_delay -clock clock -max 4 [get_ports Xout[5]]
set_output_delay -clock clock -max 4 [get_ports Xout[6]]
set_output_delay -clock clock -max 4 [get_ports Xout[7]]
set_output_delay -clock clock -max 4 [get_ports Xout[8]]
set_output_delay -clock clock -max 4 [get_ports Xout[9]]
set_output_delay -clock clock -max 4 [get_ports Xout[10]]
set_output_delay -clock clock -max 4 [get_ports Xout[11]]
set_output_delay -clock clock -max 4 [get_ports Xout[12]]
set_output_delay -clock clock -max 4 [get_ports Xout[13]]
set_output_delay -clock clock -max 4 [get_ports Xout[14]]
```

```
set_output_delay -clock clock -max 4 [get_ports Xout[15]]
set_output_delay -clock clock -max 4 [get_ports Xout[16]]

set_output_delay -clock clock -min 0 [get_ports Xout[0]]
set_output_delay -clock clock -min 0 [get_ports Xout[1]]
set_output_delay -clock clock -min 0 [get_ports Xout[2]]
set_output_delay -clock clock -min 0 [get_ports Xout[3]]
set_output_delay -clock clock -min 0 [get_ports Xout[4]]
set_output_delay -clock clock -min 0 [get_ports Xout[5]]
set_output_delay -clock clock -min 0 [get_ports Xout[6]]
set_output_delay -clock clock -min 0 [get_ports Xout[7]]
set_output_delay -clock clock -min 0 [get_ports Xout[8]]
set_output_delay -clock clock -min 0 [get_ports Xout[9]]
set_output_delay -clock clock -min 0 [get_ports Xout[10]]
set_output_delay -clock clock -min 0 [get_ports Xout[11]]
set_output_delay -clock clock -min 0 [get_ports Xout[12]]
set_output_delay -clock clock -min 0 [get_ports Xout[13]]
set_output_delay -clock clock -min 0 [get_ports Xout[14]]
set_output_delay -clock clock -min 0 [get_ports Xout[15]]
set_output_delay -clock clock -min 0 [get_ports Xout[16]]

set_output_delay -clock clock -max 4 [get_ports Yout[0]]
set_output_delay -clock clock -max 4 [get_ports Yout[1]]
set_output_delay -clock clock -max 4 [get_ports Yout[2]]
set_output_delay -clock clock -max 4 [get_ports Yout[3]]
set_output_delay -clock clock -max 4 [get_ports Yout[4]]
set_output_delay -clock clock -max 4 [get_ports Yout[5]]
set_output_delay -clock clock -max 4 [get_ports Yout[6]]
set_output_delay -clock clock -max 4 [get_ports Yout[7]]
set_output_delay -clock clock -max 4 [get_ports Yout[8]]
set_output_delay -clock clock -max 4 [get_ports Yout[9]]
set_output_delay -clock clock -max 4 [get_ports Yout[10]]
set_output_delay -clock clock -max 4 [get_ports Yout[11]]
set_output_delay -clock clock -max 4 [get_ports Yout[12]]
set_output_delay -clock clock -max 4 [get_ports Yout[13]]
set_output_delay -clock clock -max 4 [get_ports Yout[14]]
set_output_delay -clock clock -max 4 [get_ports Yout[15]]
set_output_delay -clock clock -max 4 [get_ports Yout[16]]

set_output_delay -clock clock -min 0 [get_ports Yout[0]]
set_output_delay -clock clock -min 0 [get_ports Yout[1]]
set_output_delay -clock clock -min 0 [get_ports Yout[2]]
```

```
set_output_delay -clock clock -min 0 [get_ports Yout[3]]
set_output_delay -clock clock -min 0 [get_ports Yout[4]]
set_output_delay -clock clock -min 0 [get_ports Yout[5]]
set_output_delay -clock clock -min 0 [get_ports Yout[6]]
set_output_delay -clock clock -min 0 [get_ports Yout[7]]
set_output_delay -clock clock -min 0 [get_ports Yout[8]]
set_output_delay -clock clock -min 0 [get_ports Yout[9]]
set_output_delay -clock clock -min 0 [get_ports Yout[10]]
set_output_delay -clock clock -min 0 [get_ports Yout[11]]
set_output_delay -clock clock -min 0 [get_ports Yout[12]]
set_output_delay -clock clock -min 0 [get_ports Yout[13]]
set_output_delay -clock clock -min 0 [get_ports Yout[14]]
set_output_delay -clock clock -min 0 [get_ports Yout[15]]
set_output_delay -clock clock -min 0 [get_ports Yout[16]]
```

16.3. CORDIC.pcon (for PD):

```
create_die_area -coordinate {{0 0} {340 250}}
#create_placement_blockage -name Blockage1 -coordinate {0 80 20 100}
#set_aspect_ratio
#set_utilization
#create_site_row
#set_port_side
#create_terminal
#set_cell_location
#create_voltage_area
#create_bounds
#create_route_guide
#create_net_shape
#create_user_shape
#set_pin_physical_constraints
#create_pin_guide
#create_via_master
#create_via
#create_track
#set_keepout_margin
#compute_polygons
```

16.4. initial_setup_icc.tcl:

```
##################################################################
### Inital design setup
##################################################################################

set sh_output_log_file "logs/init_design.log"
```

```
set LIBRARY_HOME "/home/synopsys/pdk/scl_pdk/stdlib/" ;# Parent home for
synopsys libraries

set LOGICAL_LIBRARY_PATH  "${LIBRARY_HOME}/fs120/liberty/lib_flow_ss" ;#
Additional search path to be added to the default search path

set TARGET_LIBRARY_FILES
"/home/synopsys/pdk/scl_pdk/stdlib/fs120/liberty/lib_flow_ss/tsl18fs120_scl_ss.
db"   ;#  Target technology logical libraries
## update library files
set_app_var search_path "${LOGICAL_LIBRARY_PATH} $search_path"
set_app_var target_library $TARGET_LIBRARY_FILES
set_app_var link_library "* $target_library"

set MW_REFERENCE_LIB_DIRS " ${LIBRARY_HOME}/fs120/mw/fs120_scl/" ;# milkyway
reference libraries

set mw_logic0_net VSS
set mw_logic1_net VDD

set_tlu_plus_files -max_tluplus
"/home/synopsys/pdk/scl_pdk/design_kit/icc_tech/tluplus/RCE_TS18SL_SCL_STAR_RCX
T_4M1L_TYP.tlup"
set  tech2itf_map
"/home/synopsys/pdk/scl_pdk/design_kit/icc_tech/RCE_TS18SL_STAR_RCXT_4M1L.map"

create_mw_lib -technology
"/home/synopsys/pdk/scl_pdk/design_kit/icc_tech/icc.tf" -mw_reference_library
$MW_REFERENCE_LIB_DIRS CORDIC.mw

#create_mw_lib -technology
/home/synopsys/pdk/scl_pdk/stdlib/fs120/lef/tsl180fs120_scl.lef -
mw_reference_library $MW_REFERENCE_LIB_DIRS FIFO.mw

open_mw_lib CORDIC.mw

#read_verilog
/home/synopsys/pdk/scl_pdk/stdlib/fs120/verilog/tmax_model/lib_flow_ff/verilog.
v
#read_verilog
/home/synopsys/pdk/scl_pdk/stdlib/fs120/verilog/tmax_model/lib_flow_ff/verilog_
udp.v
```

```
import_design -format "ddc"  ../CORDIC_topo1.ddc -top CORDIC

save_mw_cel  -design "CORDIC.CEL;1"

current_design CORDIC

uniquify_fp_mw_cel

link

#read_sdc /home/userdata/skl/SCL_example/Synthesis/scripts/const/fifo.sdc

save_mw_cel -as CORDIC
```

16.5 floorplan_icc.tcl:

```
gui_start
set sh_output_log_file "logs/floorplan.log"

create_floorplan -control_type aspect_ratio -core_aspect_ratio 1 -
core_utilization 0.6 -flip_first_row -left_io2core 100 -bottom_io2core 100 -
right_io2core 100 -top_io2core 100

create_fp_placement

current_design CORDIC

derive_pg_connection -power_net {VDD} -ground_net {VSS} -power_pin {VDD} -
ground_pin {VSS}


set_fp_rail_constraints -add_layer  -layer TOP_M -direction horizontal -
max_strap 10 -min_strap 3 -max_width 5 -min_width 5 -spacing minimum

set_fp_rail_constraints -add_layer  -layer M3 -direction vertical -max_strap 10
-min_strap 3 -max_width 5 -min_width 5 -spacing minimum

set_fp_rail_constraints  -set_ring -nets  {VSS VDD}  -horizontal_ring_layer {
TOP_M } -vertical_ring_layer { M3 } -ring_width 10 -ring_spacing 5 -ring_offset
5 -extend_strap core_ring

synthesize_fp_rail  -nets {VDD VSS} -voltage_supply 1.8 -synthesize_power_plan
-power_budget 80
commit_fp_rail
```

```
preroute_standard_cells -extend_for_multiple_connections  -extension_gap 16 -
connect horizontal  -remove_floating_pieces  -do_not_route_over_macros  -
fill_empty_rows  -port_filter_mode off -cell_master_filter_mode off -
cell_instance_filter_mode off -voltage_area_filter_mode off -route_type {P/G
Std. Cell Pin Conn}

analyze_fp_rail  -nets {VDD VSS} -power_budget 80 -voltage_supply 1.8

create_fp_placement -incremental all

set_zero_interconnect_delay_mode true

set timing_enable_multiple_clocks_per_reg false
report_timing
report_power
report_area
check_physical_design -stage pre_place_opt

write_def -output ./newrfidnew1_fp.def
puts "floorplan done!!!!!"
```

16.6 placement_icc.tcl:

```
gui_start
set sh_output_log_file "logs/placement_icc.log"
set_buffer_opt_strategy -effort high
#set_power_options -leakage true
#set_power_options -dynamic true -low_power_placement true
#read_saif -input ./rfid.saif -instance tb/xf


place_opt  -congestion

check_physical_design -stage pre_clock_opt

write_def -output ./rfid1_place.def
report_placement_utilization > ./rfid1_util.rpt

report_timing -delay max -max_paths 20 > ./rfid1_place.setup.rpt

report_timing -delay min -max_paths 40 > ./rfid1_place.hold.rpt
```

16.7 cts.tcl:

```
gui_start
set sh_output_log_file "logs/cts.log"
set cts_enable_clock_at_hierarchical_pin true

clock_opt -only_cts

## setup time fix
## clock_opt -only_psyn
## clock_opt -sizing
## hold_time fix
## clock_opt -only_hold_time
report_clock_tree
check_routeability

report_timing -max_paths 20 -delay max > ./rfid1_cts.setup.rpt

report_timing -max_paths 20 -delay min > ./rfid1_cts.hold.rpt
```

16.8 routing_icc.tcl:

```
gui_start
set sh_output_log_file "logs/routing_icc.log"
set_route_zrt_common_options  -post_detail_route_redundant_via_insertion high -
concurrent_redundant_via_mode insert_at_high_cost -
concurrent_redundant_via_effort_level high
route_zrt_group -all_clock_nets  -reuse_existing_global_route true
route_zrt_auto
route_opt

write_def -output ./rfid_route.def
report_placement_utilization > ./rfid_route_util.rpt
report_qor > ./rfid_route_qor.rpt
report_timing -max_paths 20 -delay max > ./rfid_route.setup.rpt
report_timing -max_paths 20 -delay min > ./rfid_route.hold.rpt
```

16.9 extract_icc.tcl:

```
##########################################################################
### Extraction
##########################################################################


set sh_output_log_file "logs/extract.log"
extract_rc  -coupling_cap  -routed_nets_only  -incremental
```

```
##write parasitic to a file for delay calculations tools (e.g PrimeTime).
write_parasitics -output ./output/CORDIC_extracted.spef -format SPEF

##Write Standard Delay Format (SDF) back-annotation file
write_sdf ./output/CORDIC_extracted.sdf

##Write out a script in Synopsys Design Constraints format
write_sdc ./const/CORDIC_extracted.sdc

##Write out a hierarchical Verilog file for the current design, extracted from
layout
#ungroup -all -flatten
write_verilog ./output/CORDIC_extracted.v

##Save the cel and report timing
report_timing -max_paths 20 -delay max > reports/CORDIC_extracted.setup.rpt
report_timing -max_paths 20 -delay min > reports/CORDIC_extracted.hold.rpt

report_power > reports/CORDIC_power.rpt

save_mw_cel -as CORDIC_extracted
```