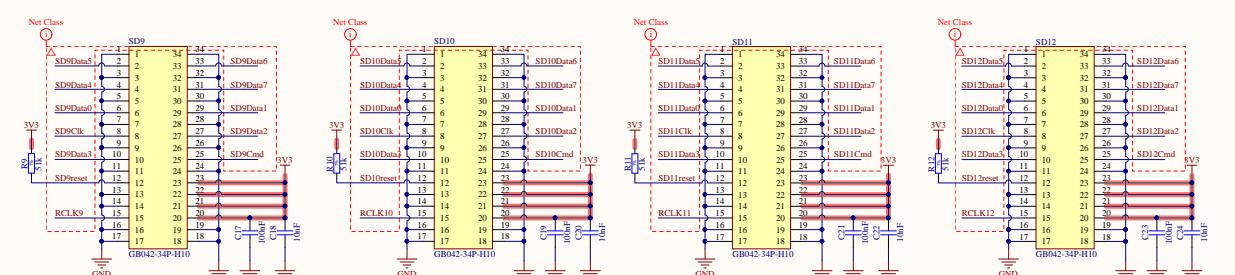
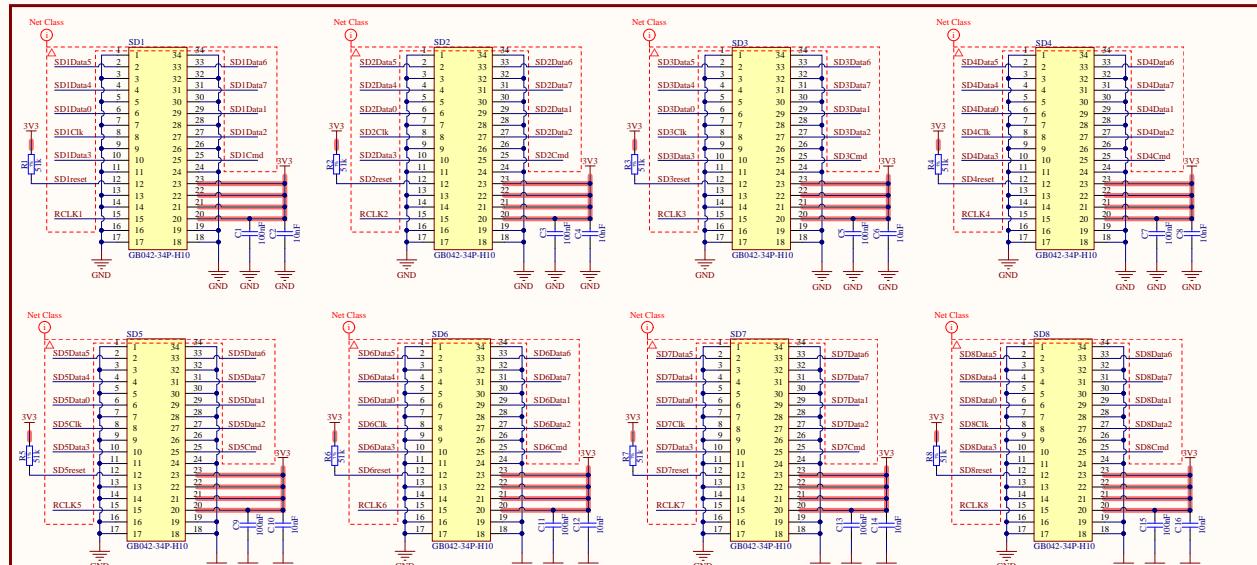
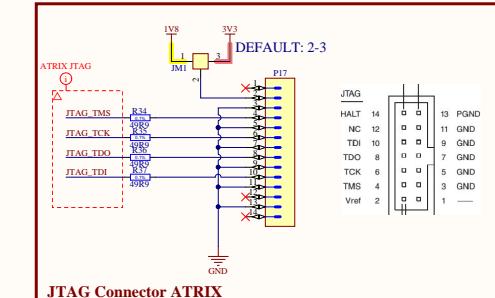


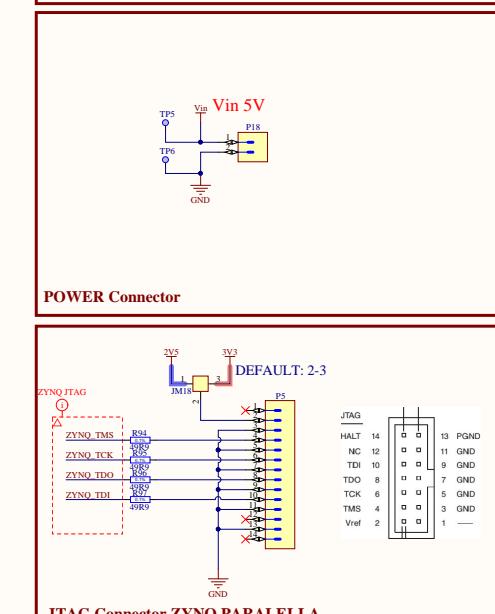
Paralella Connectors



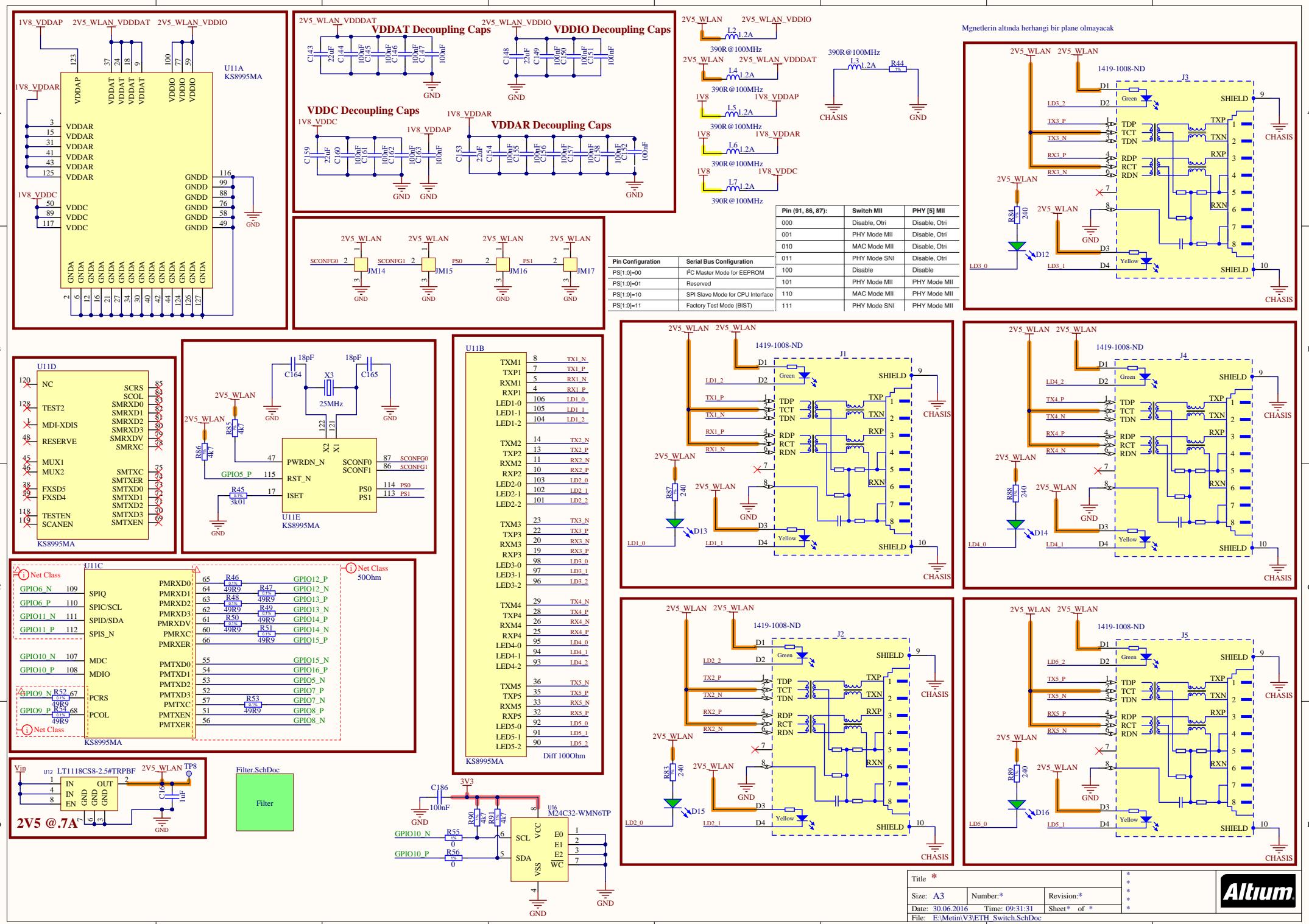
eMMC Connectors

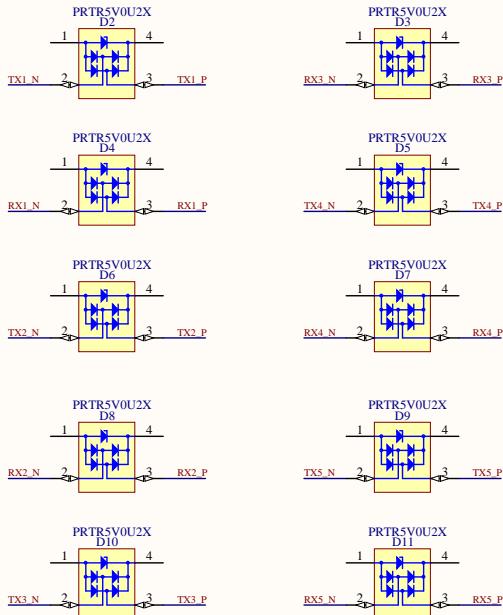
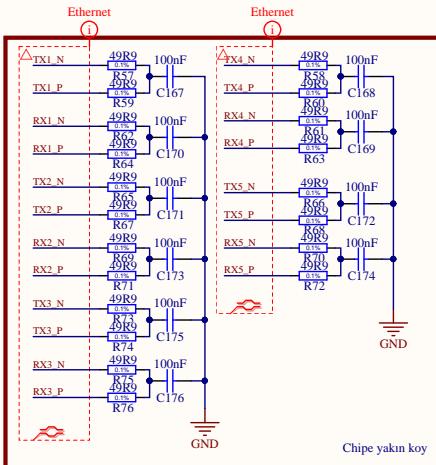


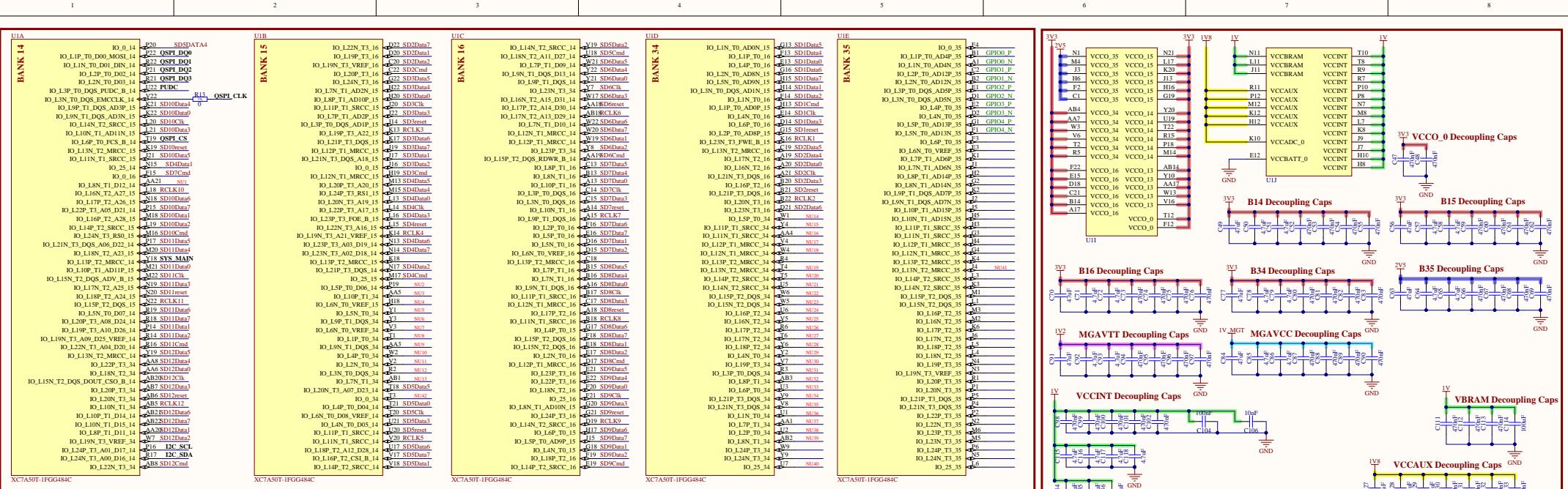
JTAG Connector ATRIX



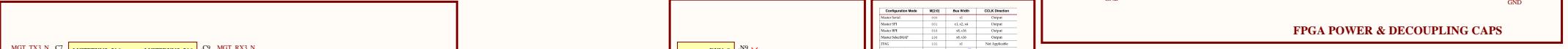
JTAG Connector ZYNQ PARALELLA



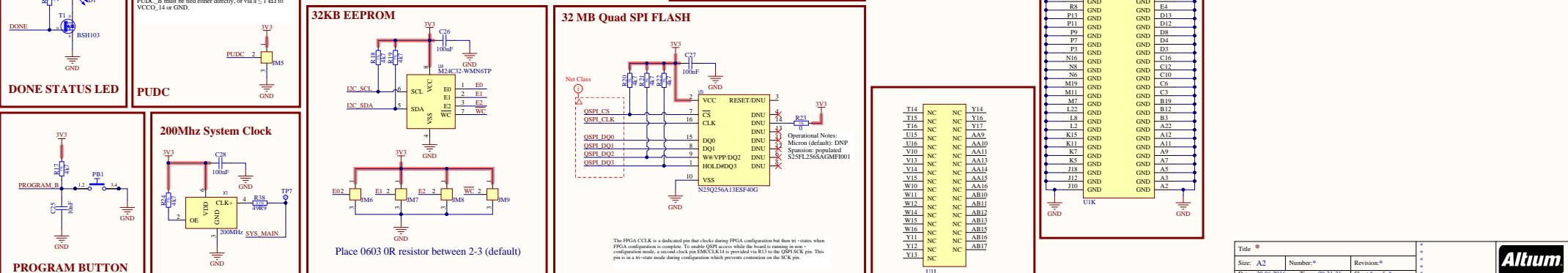




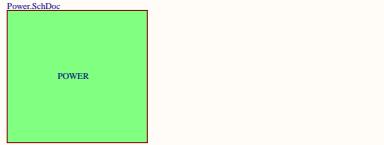
### FPGA I/O

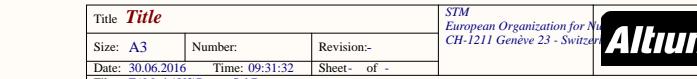
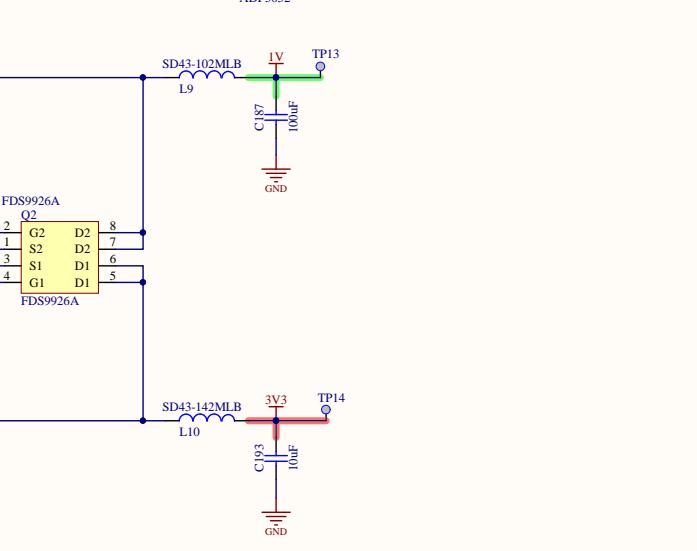
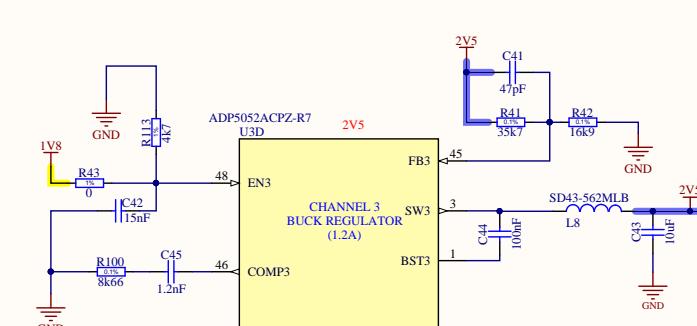
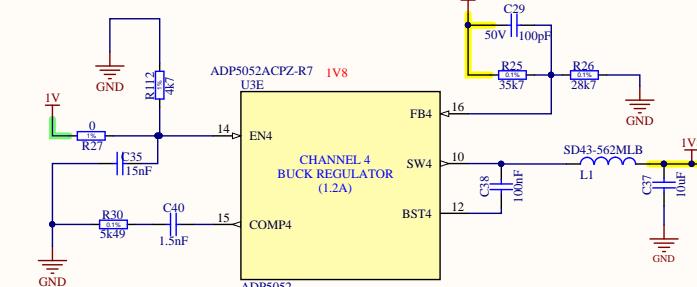
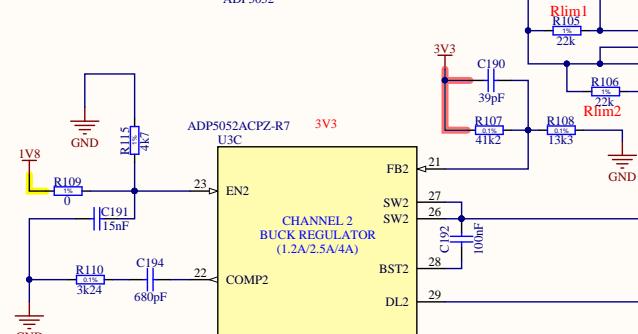
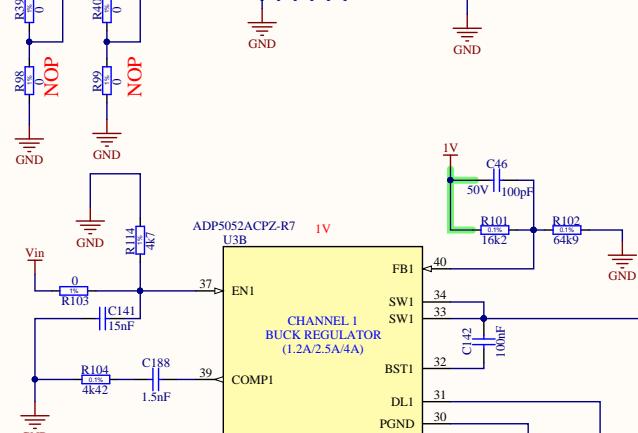
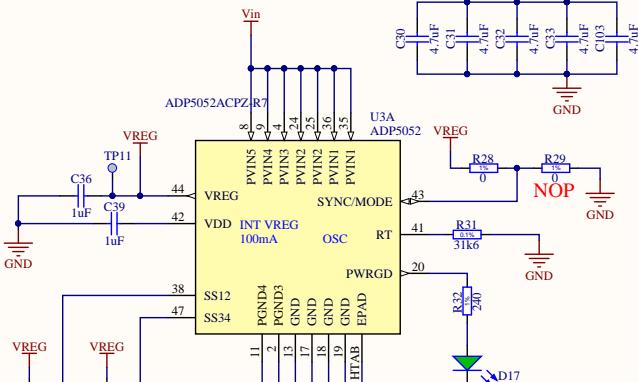
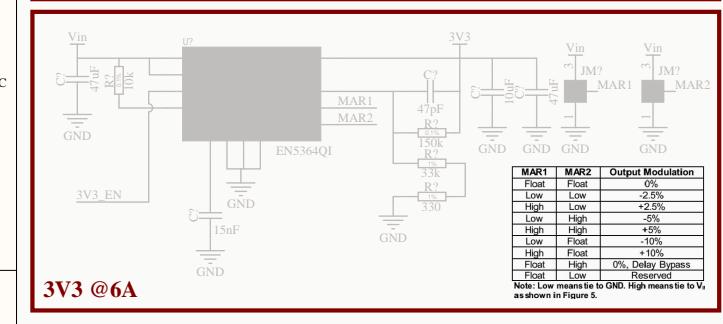
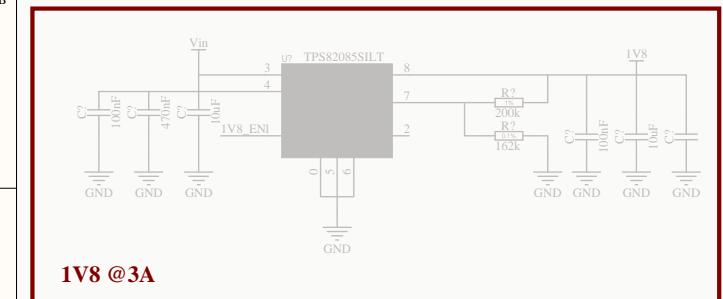
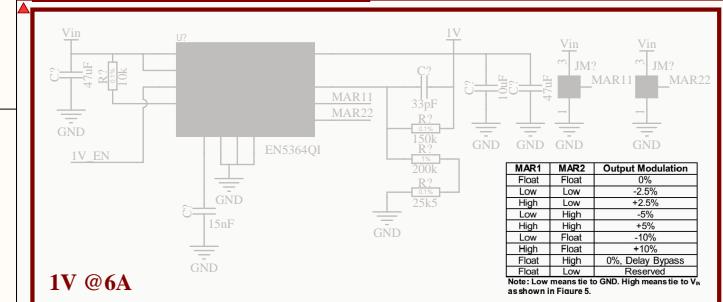
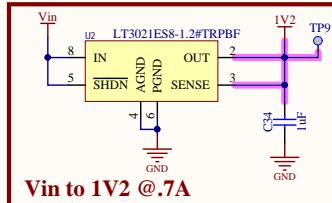


### MGT TRANSCEIVERS



### FPGA POWER & DECOUPLING CAPS

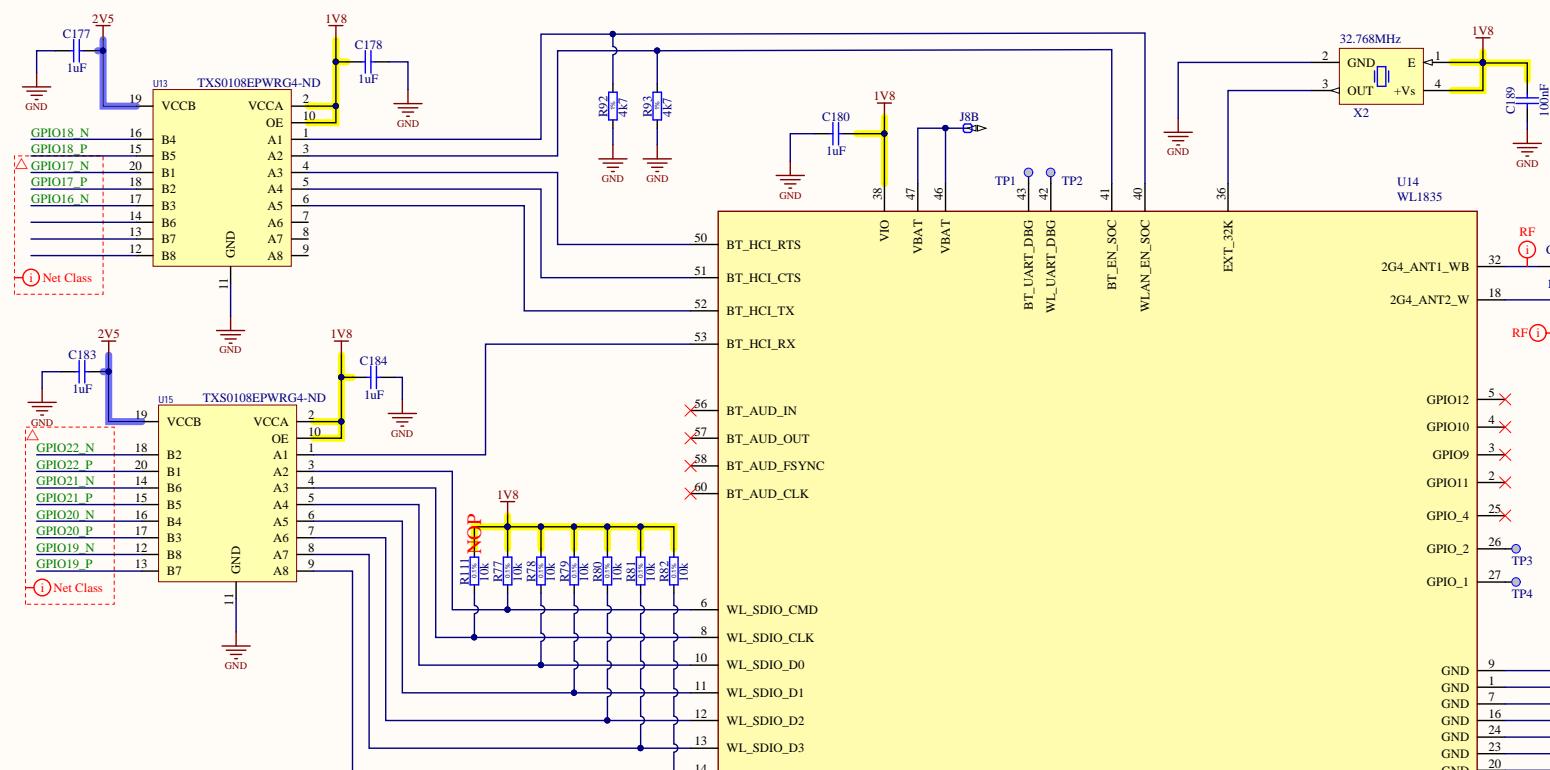




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**Altium**

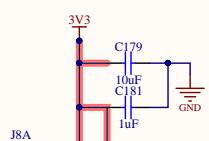
BT UART BT\_HCI\_RTS - Connect to the Host CTS  
 BT UART BT\_HCI\_CTS - Connect to the Host RTS  
 BT UART BT\_HCI\_Tx - Connect to the Host RX  
 BT UART BT\_HCI\_Rx - Connect to the Host TX



**Thermal**  
 1 The proximity of ground vias must be close to the pad.  
 2 Signal traces must not be run underneath the module on the layer where the module is mounted.

3 Have a complete ground pour in layer 2 for thermal dissipation.  
 4 Have a solid ground plane and ground vias under the module for stable system and thermal dissipation.  
 5 Increase the ground pour in the first layer and have all of the traces from the first layer on the inner layers, if possible.  
 6 Signal traces can be run on a third layer under the solid ground layer, which is below the module mounting layer.

**RF Trace and Antenna Routing**  
 7 The RF trace antenna feed must be as short as possible beyond the ground reference. At this point, the trace starts to radiate.  
 8 The RF trace bends must be gradual with an approximate maximum bend of 45 degrees with trace mitered. RF traces must not have sharp corners.  
 9 RF traces must have via stitching on the ground plane beside the RF trace on both sides.  
 10 RF traces must have constant impedance (microstrip transmission line).  
 11 For best results, the RF trace ground layer must be the ground layer immediately below the RF trace. The ground layer must be solid.  
 12 There must be no traces or ground under the antenna section.  
 13 RF traces must be as short as possible. The antenna, RF traces, and modules must be on the edge of the PCB product. The proximity of the antenna to the enclosure and the enclosure material must also be considered.



**Supply and Interface**  
 14 The power trace for VBAT must be at least 40-mil wide.  
 15 The 1.8-V trace must be at least 18-mil wide.  
 16 Make VBAT traces as wide as possible to ensure reduced inductance and trace resistance.  
 17 If possible, shield VBAT traces with ground above, below, and beside the traces.  
 18 SDIO signals traces (CLK, CMD, D0, D1, D2, and D3) must be routed in parallel to each other and as short as possible (less than 12 cm). In addition, every trace length must be the same as the others. There should be enough space between traces – greater than 1.5 times the trace width or ground – to ensure signal quality, especially for the SDIO\_CLK trace. Remember to keep these traces away from the other digital or analog signal traces. TI recommends adding ground shielding around these buses.  
 19 SDIO and digital clock signals are a source of noise. Keep the traces of these signals as short as possible. If possible, maintain a clearance around them.

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