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# Study and Design of a Full Bridge DC / DC Power Converter

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**Abstract** In this paper, a converter DC/DC for power applications is developed: battery charger for photovoltaic system, vehicle charger, helicopter power supply. It consists of using a Full-Bridge DC/DC converter which is controlled by a new analog control, designed and analyzed during this work. This control has been dimensioned so that it ensures a smooth switching of the transistors, which makes it possible to reduce the losses of power, and consequently increases the efficiency of the overall system. It allows also to increase the current and to lower the voltage to the desired value; a large generated current which reaches 50A.

**Keywords** Suply Power, DC-DC Converter, PV System, Battery, Efficiency, PWM Signal

## 1. Introduction

Although the field of power electronics has experienced a significant degree of maturity. While, this field suffers from low efficiency and the high cost of electronic circuits. As an example, conventional DC / DC converters (Boost, Buck, ...) are easy to implement, they only require a single PWM signal to control the power switch. While, this type of converters are intended for limited applications in current and voltage [1-4]. To fix this problem, there are several structures of DC / DC converters of alternative power which are used in power applications [8-18].Bor-Ren Lin et al. [17] proposed a full-bridge DC/DC converter with parallel-connected output and without output inductor, which makes it possible to generate a voltage and a current successively 48V and 20A under a chopping frequency of 100 kHz. This structure has a yield of 90.2%. In the Ref. [18], Texas Instrument has proposed a powerful DC / DC converter structure with a performance of 93%, it can generate a voltage of 12V and a current of 50A. However, in the same reference [18], the authors have not showed and given the operating principle of the UCC28950 command used.

In this context, the study of the functioning a new DC / DC power converter is investigated; It is the full bridge (FB) DC / DC converter [18]. Then, an analog control is developed, which ensures the transistors soft switching. In order to develop a high-performance product, we used high-performance electronic components (transistor and diode) based on silicon carbide. The electrothermal study of these components, allowed us to control their power losses, by following the evolution of their temperature during their operation. The obtained results are compared with those of converter designed and realized by Texas Instrument [18]. This comparison shows that the system designed in this work presents similar results to that of Texas Instrument.

The paper is organized as follows. In Sec. II, we introduce the structure and the operation of a controlled Full Bridge DC / DC converter, where the description and dimensioning in terms of the converter are given. In Sec. III, the results and interpretations are presented by comparison of the performance of the designed controller and those of the UCC28950 Controller. A study of the losses in a transistor of the DC / DC converter is evaluated. Finally, a conclusion is summarized at Sec. IV.

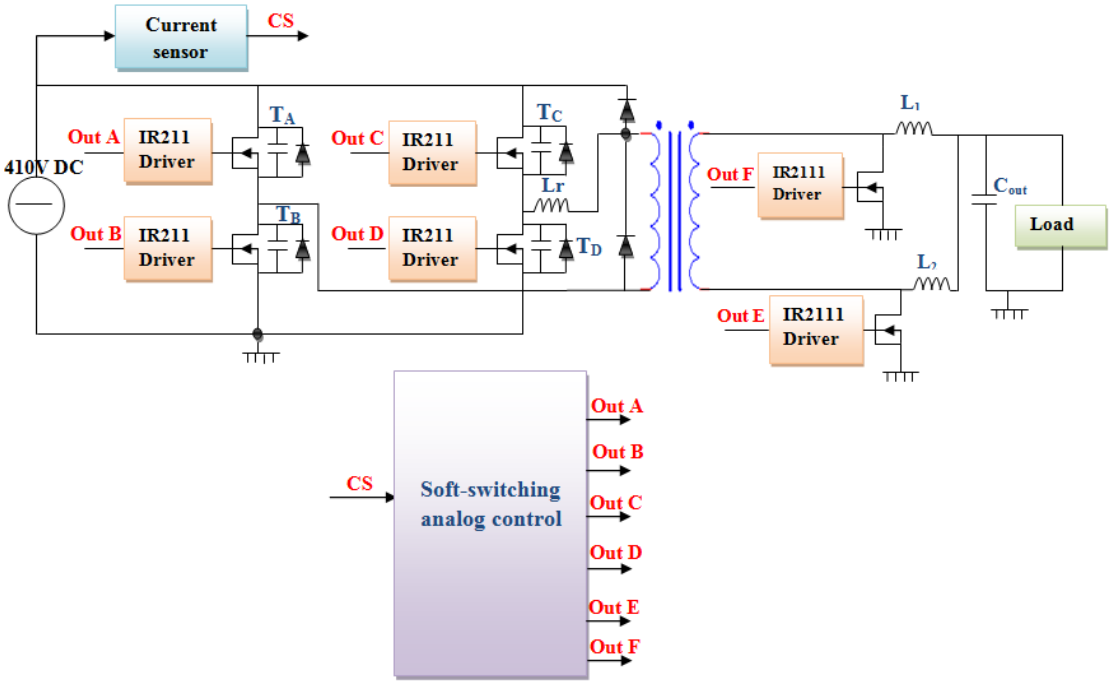



**Figure 1.** Controlled Full Bridge DC / DC Converter by a Soft Switching Analog Control

## 2. Converter Full Bridge DC / DC with a New Analog Control

It is a full Bridge power DC / DC converter (Figure 1), sized according to well-defined specifications, for charging batteries for PV installations. This converter allows to deliver at the output a voltage of 12V, a high current of 50A to accelerate the charging of the batteries, and it operates at a hash frequency. In our contribution, we have developed an analog control, which ensures a smooth control of the six transistors of the converter. In order to improve these performances, we have equipped this converter with silicon carbide-based transistors (C2M0025120D) and diodes (C3D04060A) [22].

### 2.1. Full Bridge DC/DC Converter

2.1.1. Description of the Full Bridge DC / DC Converter

Figure 2 shows a DC / DC converter phase shifted in full bridge. As the transistors $T_A$, $T_B$, $T_C$, and $T_D$ form the complete bridge on the primary side of the transformer $T_2$, they switch with a duty cycle of almost 0.5. Next, $T_E$, and $T_F$ represent the transistors on the secondary side of the transformer T2.While, $L_{Out}$ and $C_{Out}$ form the output filter. The inductance $L_r$ is intended to assist the $T_2$ transformer leakage inductance, during resonant operation with the internal capacitance of the Mosfet, and facilitates zero voltage switching (ZVT).Then, in order to design a high-performance product, we used silicon carbide-based transistors (C2M0025120D). To follow their operations, we carried out an electrothermal study of this transistor (figure 3 and 4), which allows us to follow the evolution of the junction temperature during its operation. From Figure 3A, we deduce the equation of the current drain-source (IDS) of the transistor Eq.(1), which is the difference between the direct current IG1 Eq.(2) and the inverse one IG2 Eq.(3) [20].

$$I_{DS} = I_{G1}(V_P - V_s) - I_{G2}(V_P - V_D) \quad (1)$$

$$I_{G1} = I_S * [\ln(1 + \exp[\frac{V_P - V_s}{2 * U_T}])]^2 \quad (2)$$

$$I_{G2} = I_S * [\ln(1 + \exp[\frac{V_P - V_D}{2 * U_T}])]^2 \quad (3)$$

By replacing equations (2) and (3) as well as the formula of the nip (Vp) in that of (1), we obtain the final equation of the current Drain-Source (Ids) Eq.( 4) [ 21].

Figure 3B shows the results of simulation and those of datasheet [22], the variation of the resistance Drain-Source (Rdson) as a function of the temperature, for a value of current of 50A. It appears that the electrothermal model developed during this work has a precision close to the optimal operating conditions (datasheet), even in the case of very high temperatures (150 ° C), which confirms the characteristic of operation at high temperature. SIC transistors. Then, in Fig. 3C, we have represented the variation of the drain-source current (Ids) as a function of the voltage at the output of the transistor SIC (Vds) for different Grid-Source voltage values (Vgs) and a temperature of 25 °. C. It appears that there is a very good agreement between the simulation results, represented by lines, and those of datasheet, represented by lines.

$$I_{DS} = 2 * g_m * U_T^{\ 2} * K_S([\ln(1+e^{(V_{DS}-V_{th})}]^2 - [\ln(1+e^{((V_{DS}-V_{th})-n*V_{DS}^{\ \alpha})})]^2) * (1+\lambda V_{DS}) \quad (4)$$

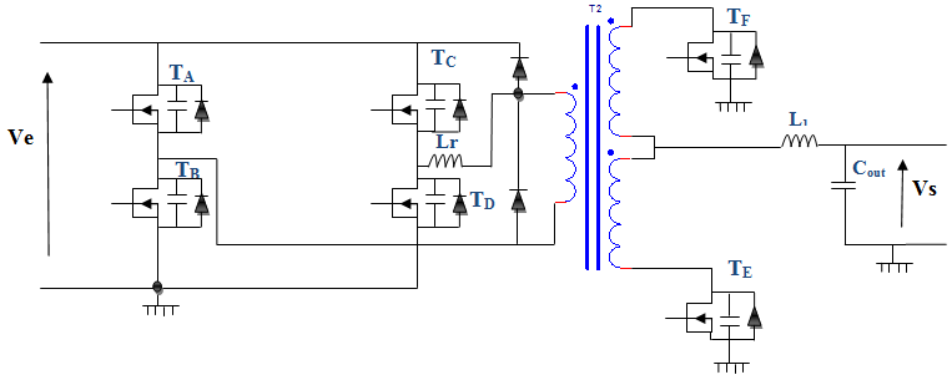
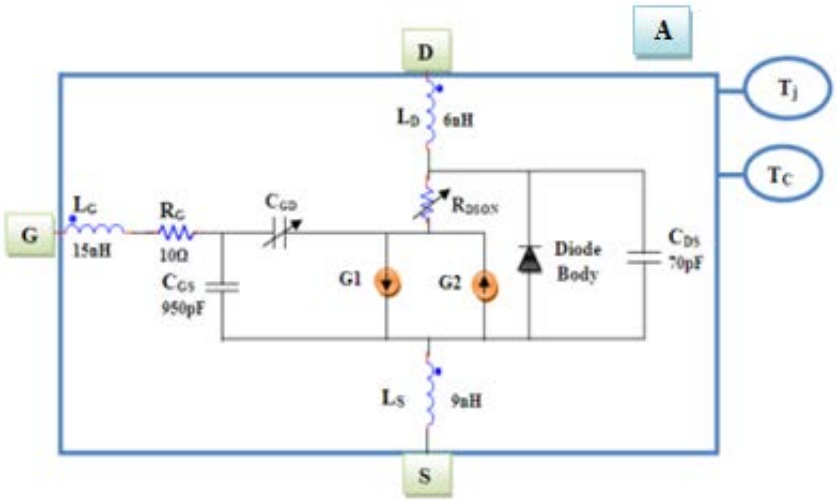
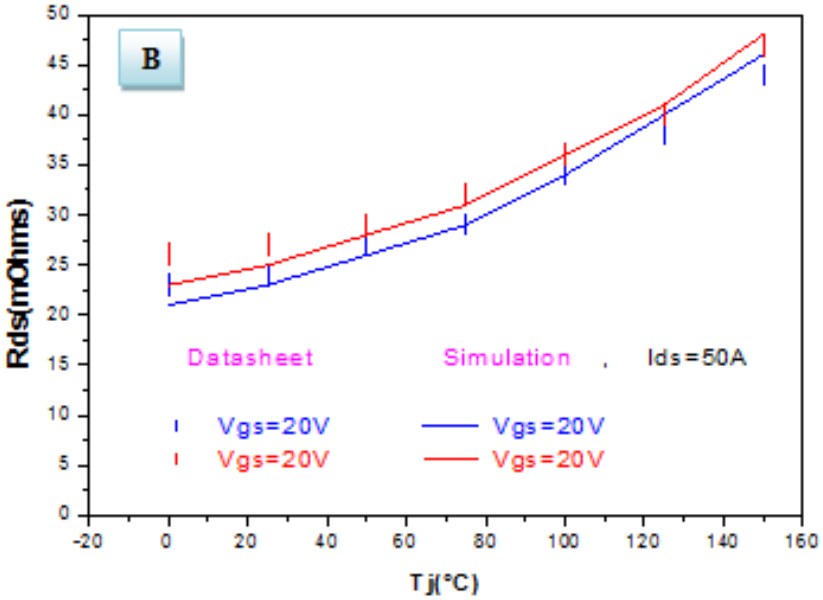



**Figure 2.** Full Bridge DC/DC converter



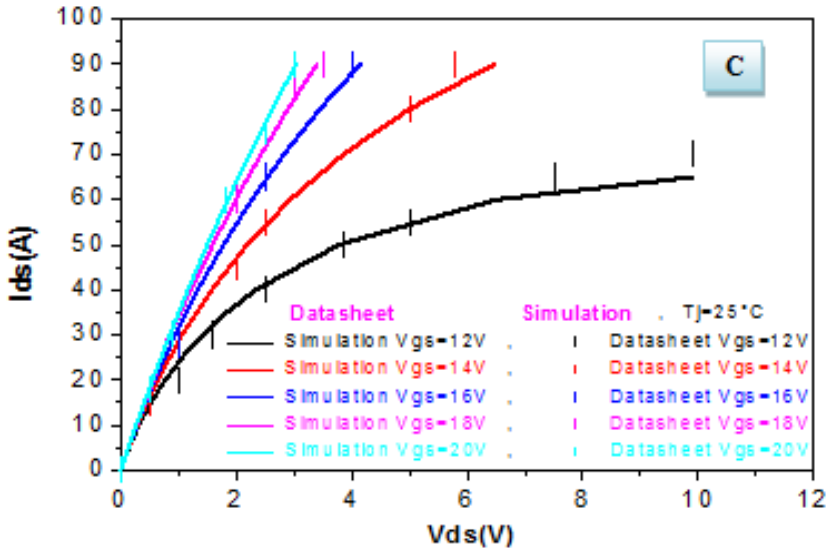



**Figure 3.** **A**: Electrical model of the power transistor SIC (C2M0080120D), **B:** Variation of resistance Rdson as a function of the junction temperature, **C:** Variation of Ids current as a function of Vds, for different values of Vgs

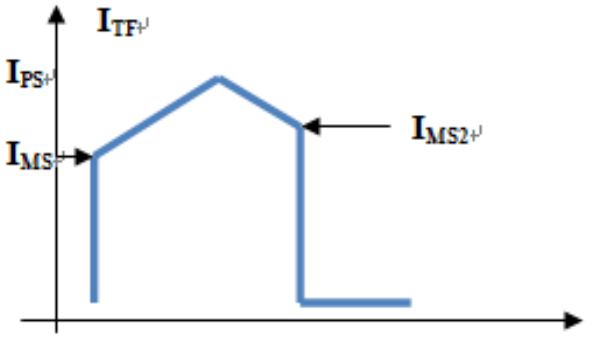



**Figure 4.** Form of the current of the transistor TF of Figure 2

2.1.2. Dimensioning of the Full Bridge DC / DC Converter

Based on the reference [18], we have dimensioned the Full Bridge converter of figure 2 according to the specifications of this application: a continuous input voltage of 410V, hashing frequency of 100 kHz transistors, a voltage 12V output and 50A output current.

Calculation of the Different Elements of the Transformer $T_2$

- **Transistor transformation ratio (n):** is calculated from equation 5: $V_{INMIN}$ is the minimum input voltage (410V), $V_{Rdson}$ is the voltage drop of the transistor, it is estimated to be 0.3V, $\alpha_{Max}$ is the value of the maximum duty cycle and $V_{Out}$ is at the output voltage of the DC / DC converter.

$$n = \frac{N_P}{N_N} = \frac{(V_{INMIN} - 2*V_{Rdson})*\alpha_{Max}}{V_{Out} + V_{Rdson}} = 21 \quad (5)$$

- **Typical cyclical report:** it is the duty cycle of the PWM signals which controls the transistors on the secondary side of the transformer ($T_E$ and $T_F$).

$$\alpha_{Typ} = \frac{(V_{Out} + V_{Rdson})*n}{(V_{IN} - 2*V_{Rdson})} \approx 0.64 \quad (6)$$

- **Ripple of inductor current $L_{Out}$:** it represents 20% of the total current at the output of the DC / DC converter.

$$\Delta I_{Lout} = \frac{P_{Out}}{V_{Out}}*0.2 = \frac{600}{12}*0.2 = 10A \quad (7)$$

- **Transformer magnetization inductance:** it allows reducing the increase of the magnetization current resulting from the increase of the signal Cs (figure 1). Its value is calculated by the following equation, Fsw is the frequency of hashing of the transistors (100kHz).

$$L_{MAG} \geq \frac{V_{IN}*(1-\alpha_{Typ})}{\frac{\Delta I_{Lout}*0.5}{n}*2*F_{SW}} = 2.92mH \quad (8)$$

Calculation of the Filter Elements in the Output

- **Output inductance ($L_{Out}$):** it represents one of the elements of the RC filter at the output of the converter.

$$L_{Out} = \frac{V_{Out}*(1-\alpha_{Typ})}{\Delta I_{Lout}*2*F_{SW}} = 2\mu H \quad (9)$$

- **Capacitor at the output ($C_{Out}$):** it is based on the ripple of the output voltage of the DC / DC converter.

The time required for the $L_{Out}$ to change 90% of its current is described by the following equation:

$$t_1 = \frac{\frac{L_{Out} * P_{Out} * 0.9}{V_{Out}}}{V_{Out}} = 7.5\mu S \quad (10)$$

In the following equation (11), we considered that 90% of the output voltage ripple ($V_{Ond}$) is due to the internal resistance of the $C_{Out}$ capacitance and the $C_{Out}$ capacitance occupies 10% of this ripple.

$$C_{Out} \geq \frac{\frac{P_{Out} * 0.9 * t_1}{V_{Out}}}{V_{ond} * 0.1} = 5.6mH \quad (11)$$

- **Equations concern the currents of transistors $T_E$ and $T_F$ on the secondary side**

The signal form of the current flowing in the transistor $T_F$ is represented in FIG. 4. The quantities $I_{PS}$, $I_{MS}$ and $I_{MS2}$ are represented by the following equations:

$$I_{PS} = \frac{P_{Out}}{V_{Out}} + \frac{\Delta I_{L_{Out}}}{2} = 55A \quad (12)$$

$$I_{MS} = \frac{P_{Out}}{V_{Out}} - \frac{\Delta I_{L_{Out}}}{2} = 45A \quad (13)$$

$$I_{MS2} = I_{PS} - \frac{\Delta I_{L_{Out}}}{2} = 50A \quad (14)$$

## 2.2. Analog Control Design with Soft Switching

The analog control designed in this work is based on the image of the input generator current and the output voltage of the DC / DC converter.

### 2.2.1. Dimensioning of the Analog Control

In order to design a simple analog control, adaptable to high power applications and meeting the great challenges of power electronics, we have designed an analog control that consists of:

- **A proportional and integral PI controller:** it consists of regulating the output voltage to a given reference. As shown in Figure 5, the proportional and integral amplifier PI is connected to its input two signals: the first is a fraction (V1) of the output voltage of the DC / DC converter (VOut), and the second is is a reference voltage or setpoint (Vref), it is set at 2.5V.

- **A progressive start-up circuit:** it is a 2.5µA current source that loads a 10n capacity (Figure 5), its purpose is to generate a progressive duty cycle in transient mode. The diodes D20 and D21 make it possible to connect to the output either the progressive start-up circuit in transient mode or the PI regulator in permanent mode (V1-Vref = 0).

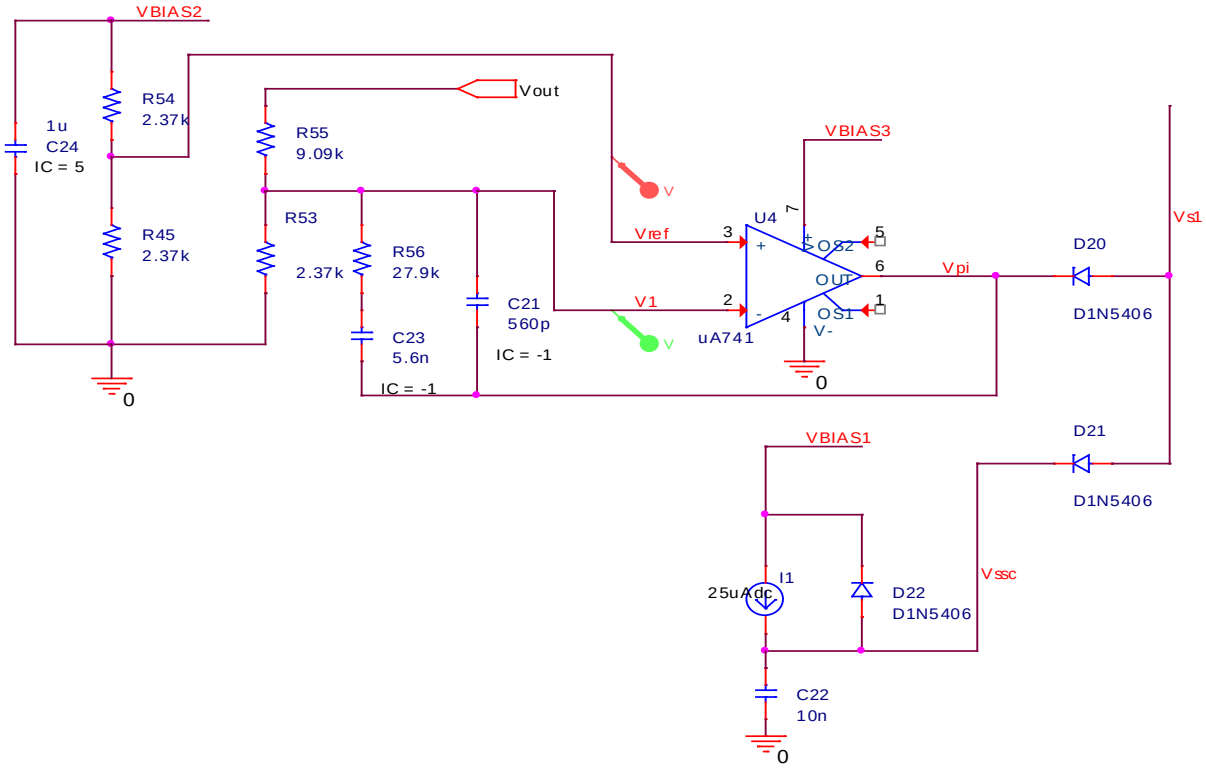



**Figure 5.** Proportional Regulator and Connected Integral of a Progressive Load Circuit

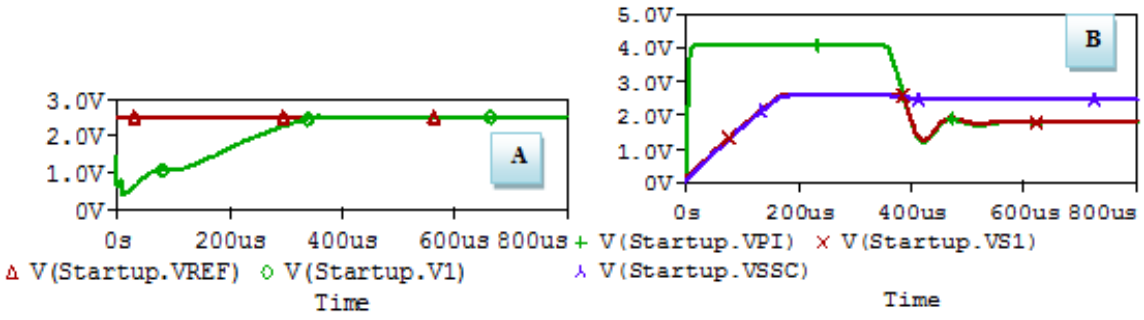



**Figure 6.** Signals Generated by the Circuit of Figure 5

We have shown in Figure 6, the simulation results, using the Pspice software. It appears that, at the transient (0 to 0.5ms), we see that in Figure 6A, the reference voltage or setpoint is set (Vref) at 2.5V. However, the voltage V1, is a fraction of the output voltage of the converter (VOut), increases gradually by almost 1V until it merges with the reference voltage. Beyond 0.5ms (steady state), it is clear that the difference between the two signals V1 and Vref is zero. Then, it is noted in FIG. 6B that the voltage Vs1 (in red), at the circuit output of FIG. 5, is equal to that generated by the progressive charging circuit VSSC (in purple). The voltage at the output of the regulator PI is equal to that of the power supply (3.2V) (in green). While at steady state, the voltage Vs1 is equal to that generated by the regulator PI (2.4V).

The acquisition of current was performed using a transformer with a transformation ratio (m) of 100 and the maximum voltage applied to the CS pin is Vp = 2V. From these data, we calculate the values of the resistors (R1 and Rcs) of Figure 7:

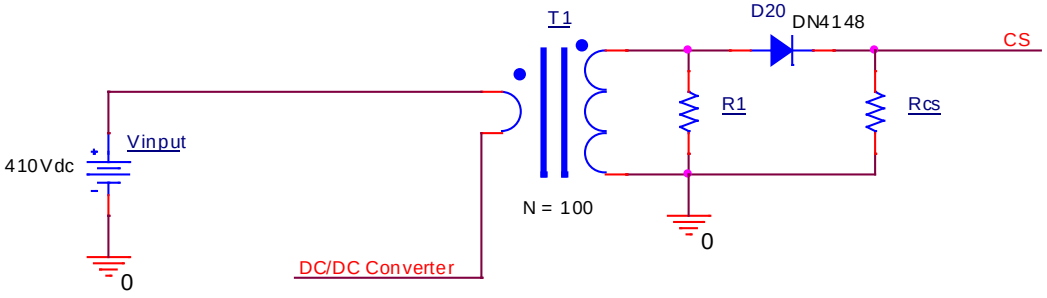



**Figure 7.** Input current acquisition circuit

$$R_{CS} = \frac{(V_p - 0.3)}{(\frac{I_{p1}}{n} * 1.1)} = 20.89\Omega \tag{15}$$

Knowing that the nominal peak current (Ip1) is described by the following equation:

$$I_{p1} = (\frac{Ps}{Vs * \eta} + \frac{\Delta I_{L1}}{2}) * \frac{1}{m} + \frac{V_{INMIN} * D_{MAX}}{L_{MAG} * 2 * F_{SW}} = 6.88 \tag{16}$$

$$R_7 = n * R_{CS} = 800\Omega \tag{17}$$

The signal representing the current image at the input of the Full Bridge DC / DC converter is added to a sawtooth signal (Vramp) (Figure 8), using a summator. Then, the obtained signal is compared with the generated signal Vs1 by the circuit of FIG. As a result, this comparison results in a PWM signal.

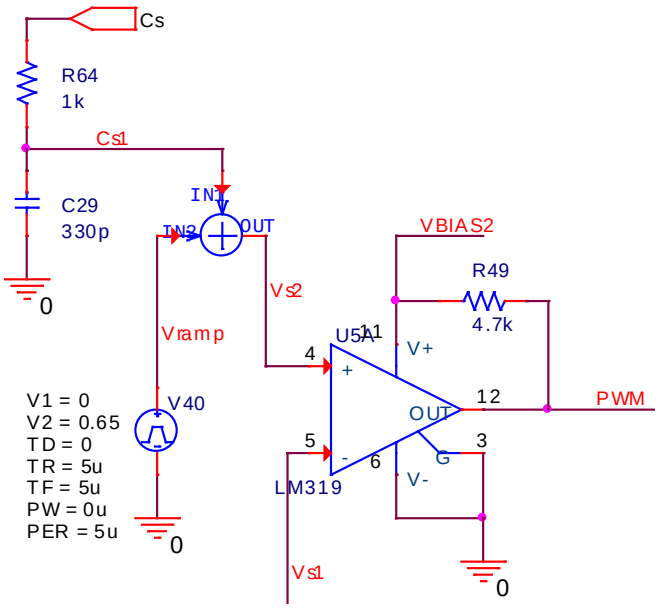



**Figure 8.** Comparison of the Image Signal of the Input Current with the Signal Vs1 of Figure 6

2.2.2. Validation the Dimentioning of the Analog Control with Soft Switching

In order to validate our study concerning the analog control, some have been done on PsPice; the results are shown in Figure 9.

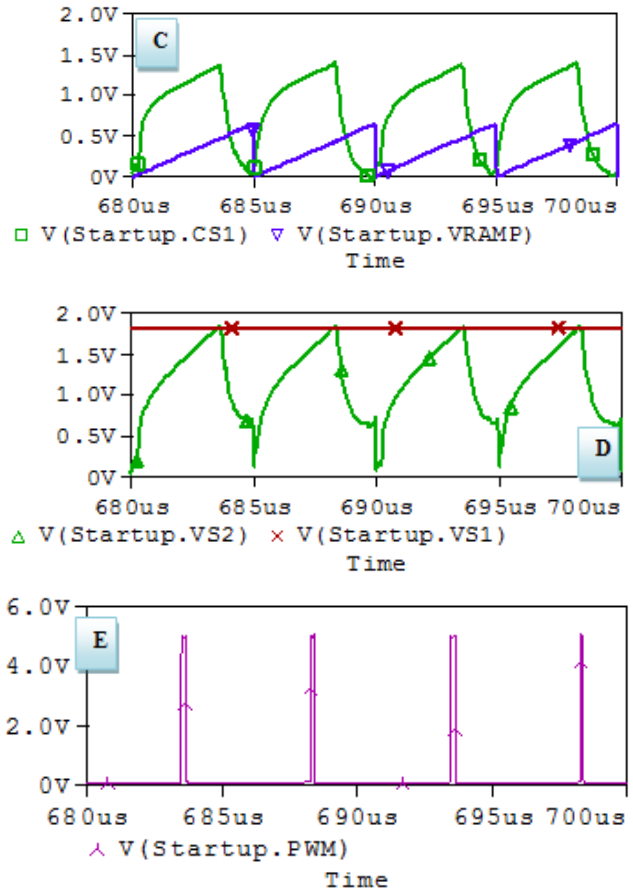



**Figure 9.** Generated Signals by the circuits of Figures 7 and 8: C: Signal Cs, image of the current at the input of the DC / DC converter (in green) and that in sawtooth (in purple); D: Comparison between a signal Vs2 of Figure 8 with that Vs1 of Figure 5; E: PWM signal at the output of the comparator of Figure 8

By connecting the PWM signal of Figure 9 E to the Flip Flop JK flip-flop input (Figure 10), its Q output changes the state only if the PWM signal connected to its CLK input is at the rising edge (Figure 11F). In order to ensure ZVS switching (soft switching), we applied a 360ns delay to the rising edge of two Q and $\overline{Q}$ of Flip Flop JK (Figure 11 G and H), this allows us to have two PWM signals QC and QD of the transistors TC and TD of Figure 2.

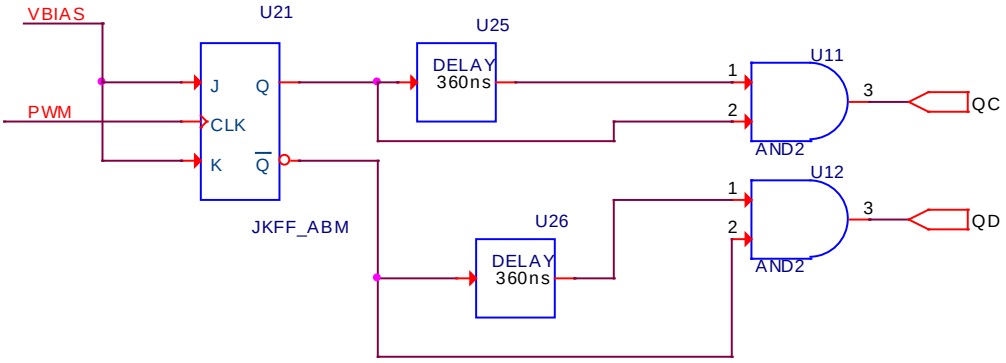



**Figure 10.** PWM signals connected to transistors $T_C$ and $T_D$

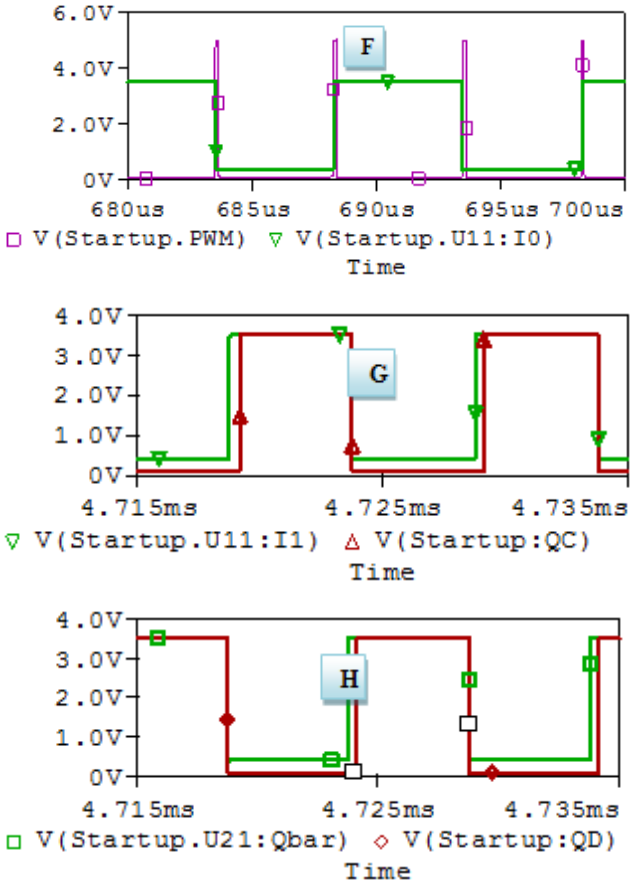



**Figure 11.** Circuit signals of Figure 10: F: PWM CLK signal flip flop JK (pink) and the output Q (green); G: Q signal shifted by 360ns (in red); H: PWM signal $\overline{Q}$ (in red) shifted by 360ns

Following the same principle, we generated the other two PWM signals from the second arm of the Full Bridge DC / DC converter (Figure 12). Such as, by connecting a CLK signal with a duty cycle of 0.05 to the CLK input of the Flip Flop JK, resulting in two Q and $\overline{Q}$ outputs. By imposing a 360ns delay on the rising edge of each output in the same way, we deduce the other two PWM signals (QA and QB) from the primary part. FIG. 13 represents the simulation results of the signals generated by the circuit of FIG. 13.

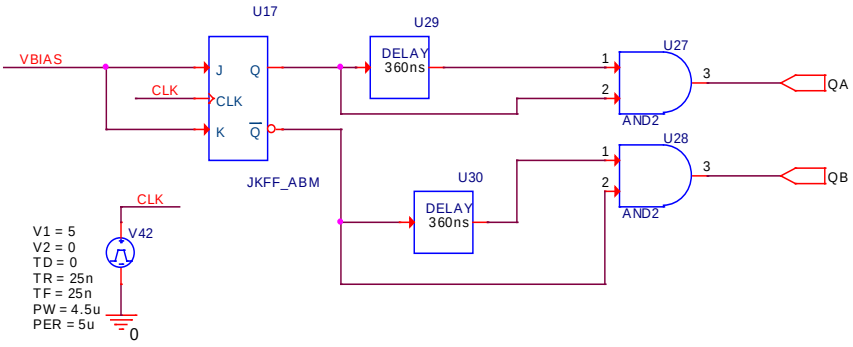



**Figure 12.** Connected PWM signals to transistors TA and TB

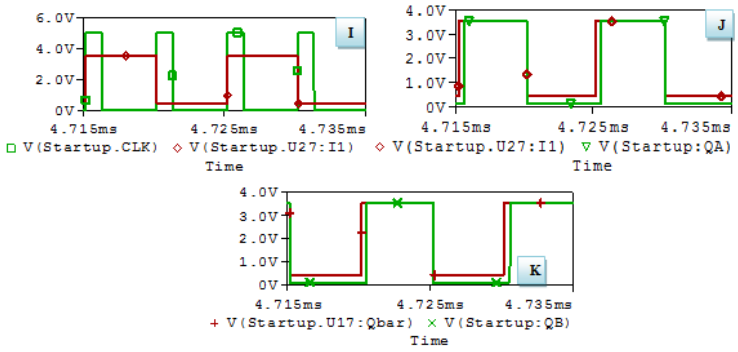



**Figure 13.** **I:** connected CLK signal (in green) to the input of Flip Flop JK and the output (in red); J: PWM signal QA (in green) obtained by shifting each rising edge of the signal to the output Q of the flip-flop JK (in red); K: PWM signal QD (in green) obtained by shifting each rising edge of the signal to the output $(Q)^{-}$of the JK flip-flop (in red)

The circuit of FIG. 15 makes it possible to generate two PWM signals, which control the transistors on the secondary side of the transformer (TE and TF) of FIG. 2. It consists in connecting the two PWM Out C and Out A signals to the two R inputs. And S of an RS flip-flop. The results obtained are shown in FIG.

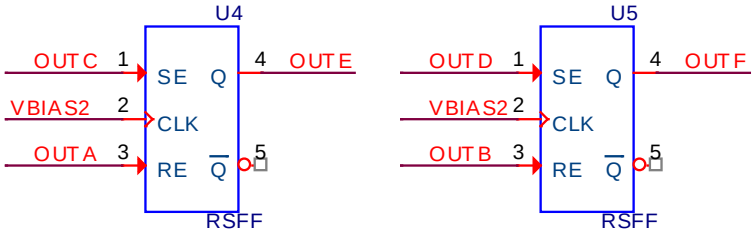



**Figure 14.** Connected PWM signals to transistors on the secondary side of the transformer

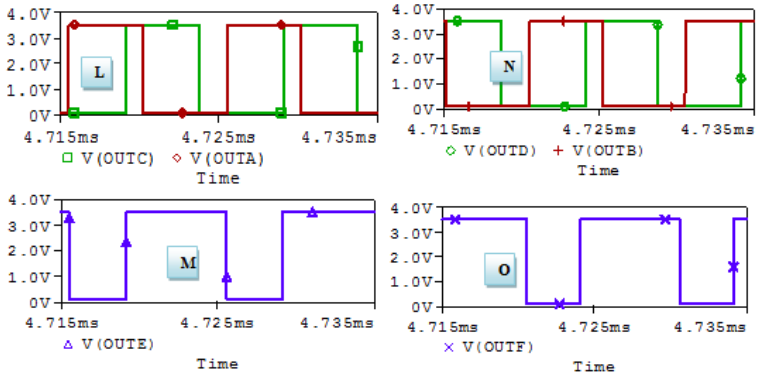



**Figure 15.** Signals of the circuit of Figure 16: L: PWM Signal QA and QC are connected to the input of an RS flip-flop. M: PWM signal Out E which controls the transistor TE of FIG. 2. N: PWM signal QB and QD are connected to the input of an RS flip-flop. O: PWM signal Out F which controls the transistor $T_F$ of FIG 2

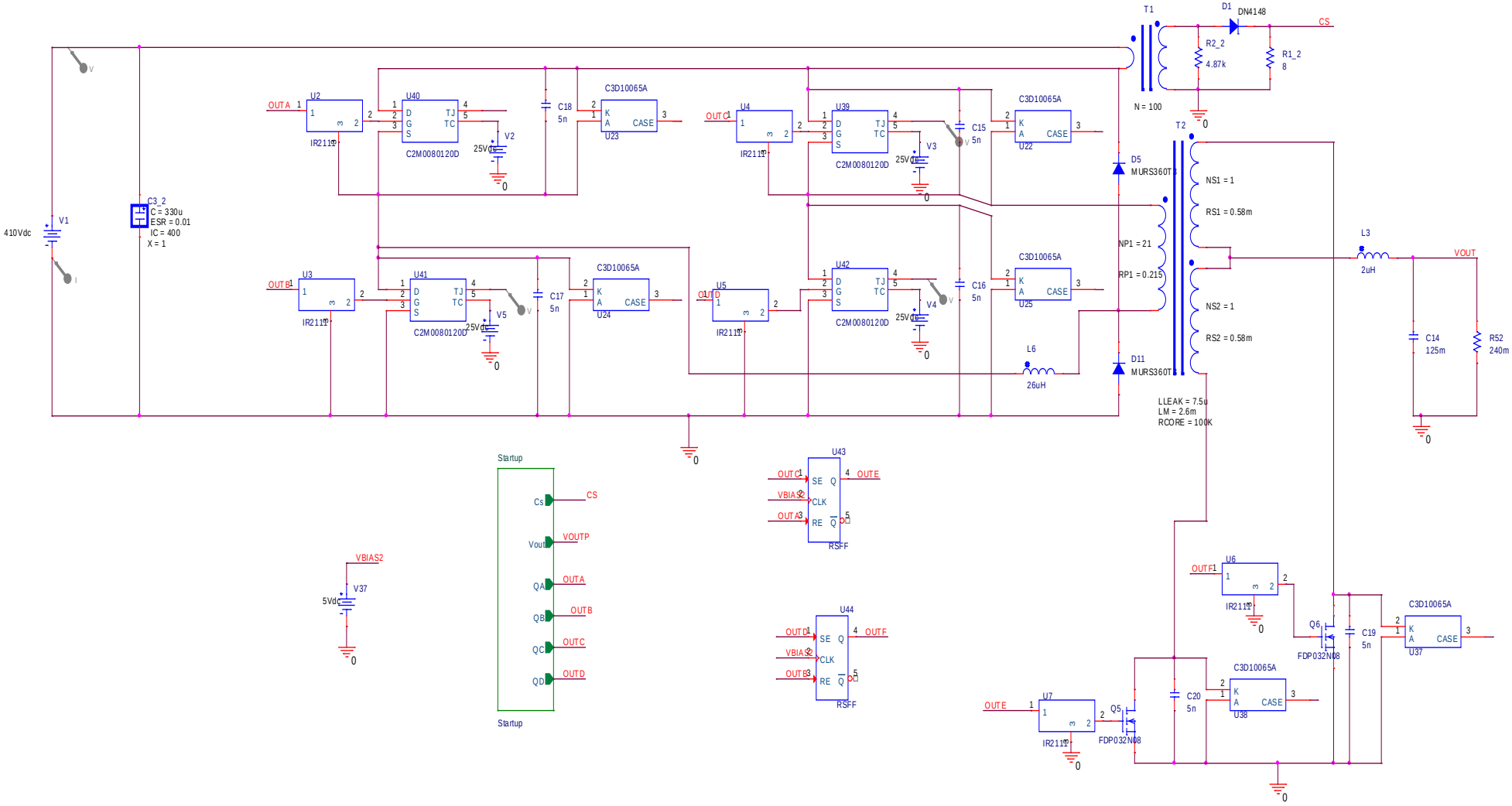



**Figure 16.** Complete Circuit of the Switching Power Supply Designed

# 3. Results and Interpretations

Figure 16 shows the complete circuit of the switching power supply, implanted in the Pspice simulator. The different values of each electronic component used were defined based on the theoretical study of paragraph II.1.2.We represent in the following, the different simulation results obtained.

### 3.1. Comparison of the Performance of the Designed Controller and Those of the UCC28950 Controller

We have shown in Figure 17 on the left, the different signals delivered by the DC / DC conversion system designed in this work. On the same figure on the right, we have represented the same signals generated by the Full Bridge DC / DC converter, designed by Texas Instrument [18]. The purpose of this comparison is to clearly show the qualities of the product designed in in work. The results obtained show that:

- The signals PWM OUTA, B, C and D generated by the two systems show that they have the same duty cycle of 0.47, the same frequency of 100 kHz. The difference in amplitude is explained by the fact that the PWM signals of the designed control have been visualized at the output of the AND gate of FIGS. 11 and 13, the maximum amplitude that can reach is 3.5V. So to amplify this amplitude, we used a driver IR2111, which allows to play a role of an adapter between the control part and the power part (DC / DC converter).
- The PWM OUTE, F signals generated by the two commands have the same duty ratio of 0.62, which validates the theoretical value calculated by equation 2, which is 0.63.

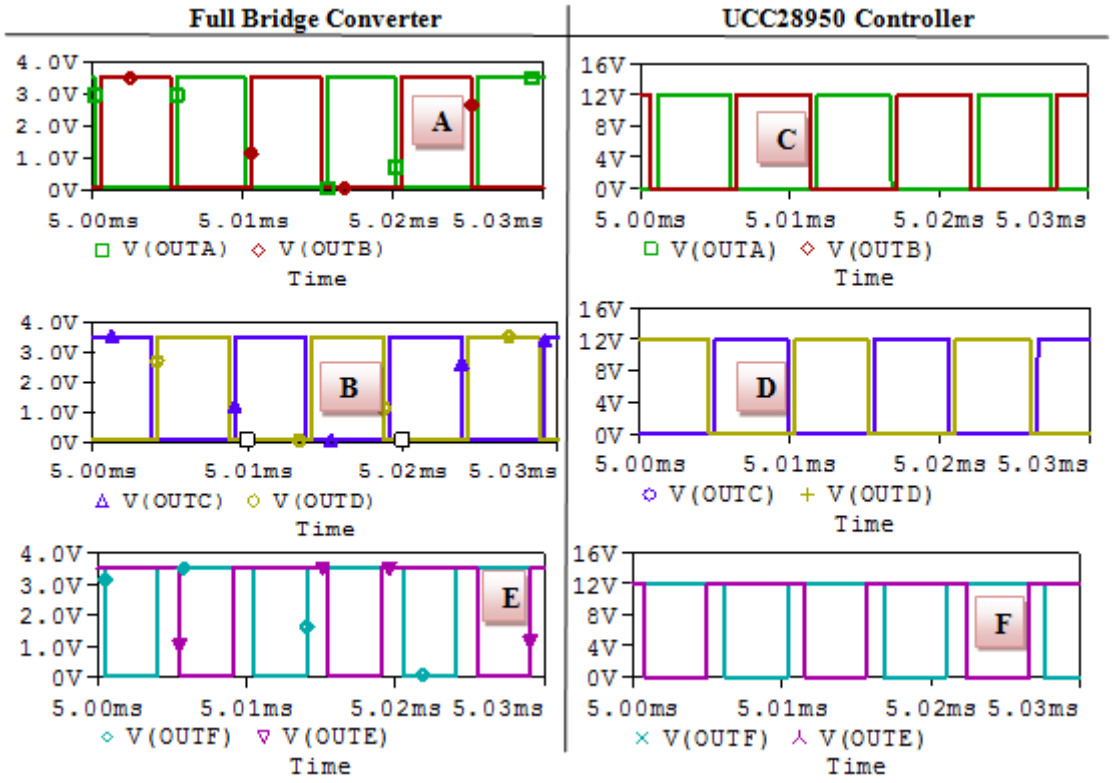



**Figure 17.** PWM OUT signals A, B, C and D on the primary side and those on secondary side OUTE, F are generated by the designed control (Figure 17A, B and E) and those generated by UCC28950 (Figure 17C, D and F).

- The voltages (figure 18 A and B) and the currents (figure 18 C and D) at the transformer input of the two controls are identical. Then the currents (figure 18 E and F), which flow in the transistor TF of the secondary part, generated by the two commands are identical and the values of the parameters IMS, IMS2 and IPS, calculated by the equations 8, 9 and 10, are almost equal to those of simulation: IMS = 46A, IMS2 = 48.5A and IPS = 56.2A.

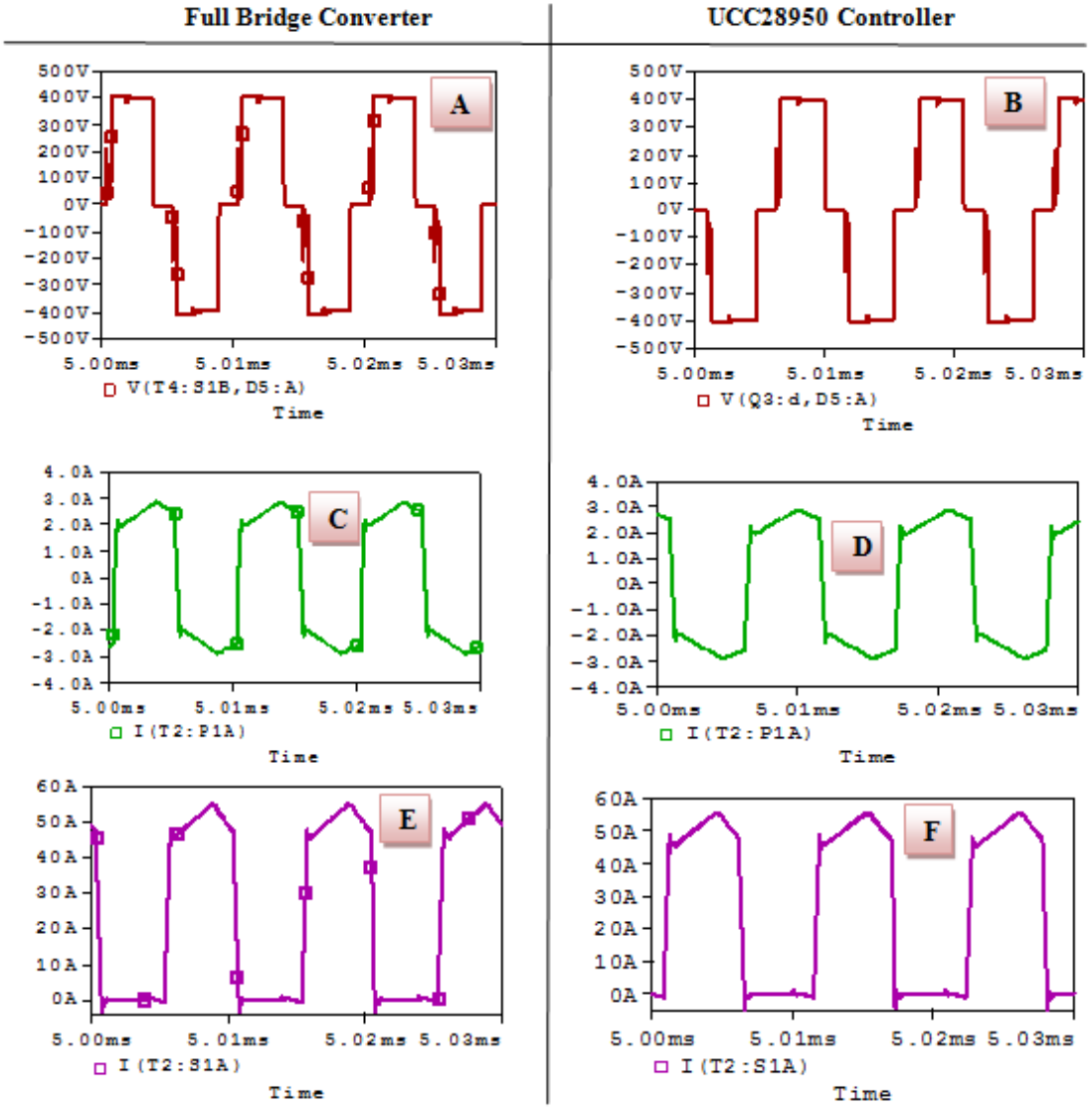



**Figure 18.** Voltages and currents at the input and at the output of the transformer of the DC / DC converter are generated by the designed control on the left and those generated by UCC28950 on the right: **A and B:** Voltage at the input of the transformer; **C and D**: Current at the input of the transformer; **E and F**: Current at the output of the transformer.

- The currents (figure 19 A and B), which flow in the inductance of the output of the DC / DC converter, of two commands are identical. Then, its ripple equals to 11A, which corresponds to that of equation 3, it is of the order of 10A.

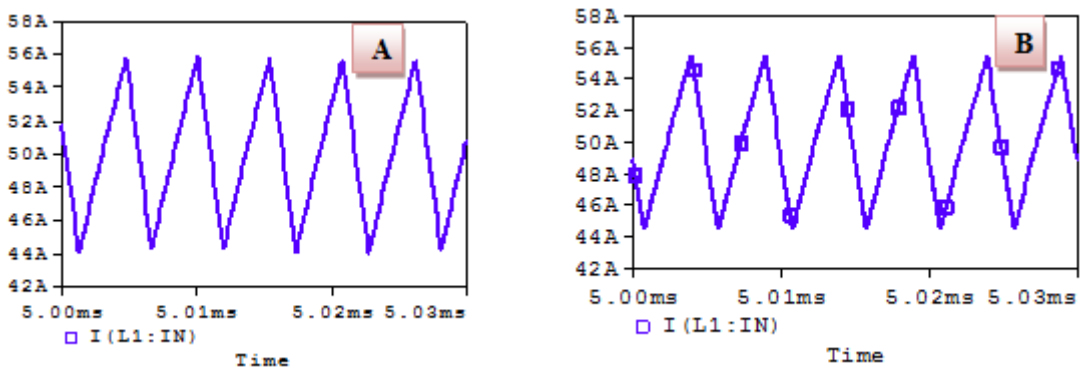



**Figure 19.** Output inductor current

- The voltage, current and power generated by the DC / DC conversion system designed (Figure 20 A and B) are successively 12V, 50A and 600W. They are identical with those generated by the UCC28950 (Figure 20 C and D).

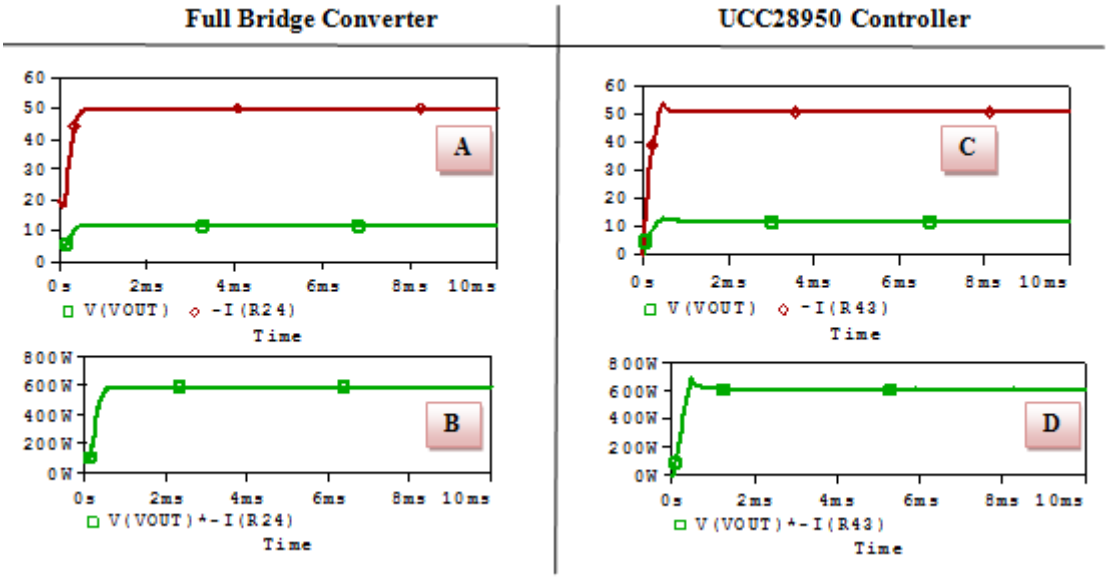



**Figure 20.** Electrical quantities at the output of the DC / DC converter generated by the two commands:**A (C):** Voltage and Current Generated by Analog Control (UCC28950) **B (D):** Power generated by the analog control (UCC28950) **E (F):** Overall efficiency of the converter controlled by the analog control (UCC28950)

- The efficiency presented by the system developed during this work is of the order of 92% (Figure 21E), it is almost identical to that generated by the Texas Instrument system, which is 93% (Figure 21F).

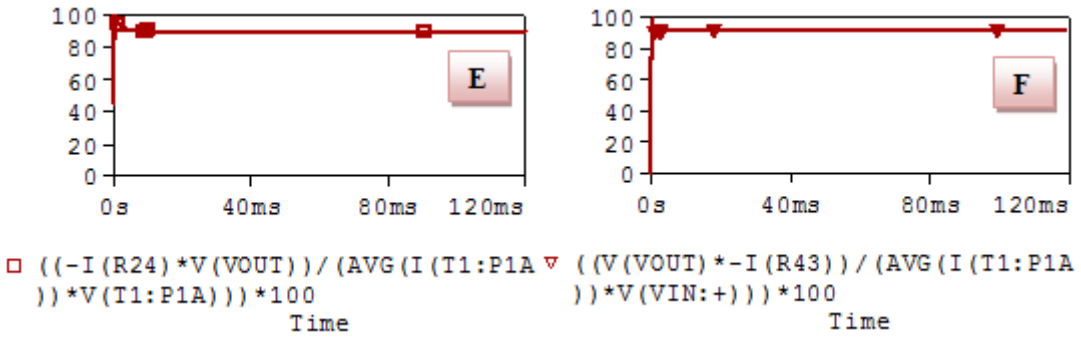



**Figure 21.** Overall efficiency of the converter controlled by the analog control (UCC28950)

### 3.2. Losses in a Transistor of the DC / DC Converter Controlled by the Analog Control

This study consists of studying the losses of powers dissipated in each transistor of the designed converter. We have shown in FIG. 22 the current of the drain C and the voltage VDS of the transistor TA of the DC / DC converter of FIG. 3. It should be noted that the current is multiplied by 100 times in order to clearly note the power losses during transistor switching. It seems that:

- At the opening of the transistor TA (Fig. 22A), it is noted that the voltage VDS switches from 0 to 400V by making a delay of some ns and the current ID goes from the max to 0 gradually, which results in a loss of a weak power. While at closing (Figure 22 B), the voltage VDS diverges directly to 0. By cons, the current ID is a delay of 1.5µs so that it switches from 0 to its maximum value. This makes the power loss in the transistor very small (Figure 22 C). Then, based on the thermal model developed during this study, the junction temperature of the four transistors of the Full Bridge converter is estimated at about 52 ° C (Figure 22D).

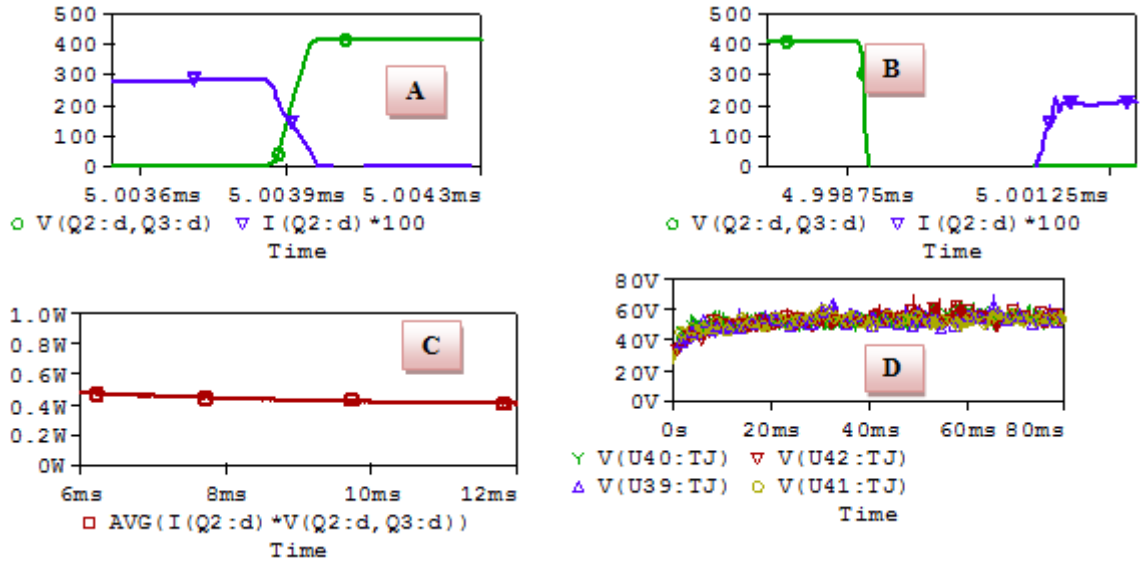



**Figure.22.** Vds voltage and Id current of the transistor TA of the DC / DC converter of Fig. 3. **A and B:** Vds voltage and current Id at the opening and closing of the transistor. **C:** Loss dissipated in the transistor TA.

## 4. Conclusions

In this paper, we have designed a high current DC / DC converter for PV applications. It is dimensioned based on the following specifications: a voltage of 12V, a current of 50A, and a hash frequency of 100 kHz. It is a full-frame DC / DC converter controlled by an analog control, developed and designed during this work. This application is specially developed for PV lighting installations, it ensures a large current adjustable according to the voltage of the batteries (12V, 24V, ...), which ensures a fast charge of the batteries. In order to improve its efficiency, we have equipped this converter with power switches based on silicon carbide. The electrothermal study carried out of the transistor used (C2M0025120D) makes it possible to clearly show these advantages with respect to the other families of transistors, which are a high response time and a high temperature resistance.

The results obtained show, on the one hand, that the product designed has efficiency, and on the other hand that they are comparable with those of the Texas Instrument converter.

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